CMOS Impedance Measurement Array for Cell Sensing

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Impedance measurement plays a vital role in determining the physical and chemical properties of live cells under different environmental conditions and aids in the development of cellular models for life science research and new medicines to fight disease. In order to improve the fidelity and spatial resolution of bio-impedance measurement systems, cell sensing platforms are being constructed using silicon chips where live cells interact with integrated microelectronic sensors through an on-chip electrode array. Our proposed complementary metal-oxide-semiconductor (CMOS) sensor array measures the impedance of complex cellular samples using a mixed-signal-based frequency response analysis (FRA) approach to extract and convert the real and imaginary parts of the cell impedance. The system is implemented using a synchronous voltage-to-frequency converter designed to operate over an input frequency range from 0.7 Hz to 2 kHz with a programmable nominal resolution up to 16 bits. Unlike previous work, we apply a switched-capacitor-based offset correction scheme to reduce the effect of multiplying integrator input offset on the sensor interface. The chip features an 8×6 surface electrode array of individually-addressable working electrodes connected to four independent impedance extraction channels for parallel data readout. The device is fabricated in a standard 0.18 μm CMOS technology, where each sensor channel consumes only 94 μW from a 1.8 V supply, and has been experimentally verified to provide linear conversion over an input current amplitude range from 40 pA to 60 nA.

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In the end I would like to acknowledge the unconditional support and love from my family, without which this thesis would not have been possible.

Dedication

This thesis is dedicated to my beloved country Pakistan and its brave people.

Table of Contents

List of Tables

List of Figures

xii

Chapter 1

Introduction

Bioimpedance analysis enables the study of the physical and chemical properties of mammalian cells under different conditions and environments. The way live cells react to external stimuli helps to determine the effect of various chemical compounds and agents on the morphology of cells. This process finds applications in the fields of drug screening, DNA testing, security monitoring [1], and water purification [2].

The motility of live cells is an important parameter in the above applications and is normally observed by time lapse microscopy. Cells are cultured and their motion pattern gives information about their activity during wound healing and cell organization processes [3]. Motility analysis has also enabled the study of the growth of cancer cells. Time lapse cameras are used to capture the cellular motion, however, this technique is limited by the need for greater speed and sensitivity at high resolution.

The process of drug testing and its effectiveness on certain chemical and physical properties of the cells is very complex and time consuming. Traditionally, *in vitro* or *in vivo* cell based assays were used for drug testing, but their results were inconsistent due to the

effect of environmental variations [6]. Most of these technologies used fluorescence based imaging systems in which the fluorescent labels (chemical compounds which re-emit light at a higher wavelength than that of the incident light source) are used to enhance the observability of the cellular samples under a fluorescence microscope [6][7]. Although this technique gives valuable information about the cell behavior, exposure to such chemical compounds and optical beams for long period of time can damage the live cells, making it harder to accurately investigate the cellular sample [8].

To address these issues, motion detection using a fully electronic approach was developed which is label free and does not require a large amount of image data processing. In this technique, a monolayer of cells is allowed to grow on gold-plated microelectrodes in a controlled environment, as shown in Fig. 1.1 [3]. A large counter electrode (CE) is used to set the reference voltage of the tissue culture medium (electrolyte) while cells are cultured on the surface of a working electrode (WE). An ac voltage V_{in} is applied to 1 MΩ resistance generating a known current I_{ref}. V_{in} is also applied between CE and WE, which produces an ac current I_{cell} containing impedance information.

This setup is connected to a lock-in amplifier to extract the cellular data. A lock-in amplifier is an electronic circuit which detects and accurately measures very small ac currents by rejecting the noise components of the system [4]. An ac input signal to be detected is multiplied by a known internal reference signal and then passed through a low-pass filter which rejects the high frequency noise. If the frequencies and phase of both signals are equal, then a dc output signal is produced which is proportional to the amplitude of the input signal. This enables us to accurately determine the amplitude of a small sinusoidal signal in a noisy environment. As the cells move and merge, the distance between cells and/or between cells and electrode changes, resulting in changed values of the cell resistance and capacitance [5]. The magnitude and phase of the ac current I_o

(which is the sum of the cell current I_{cell} and reference current I_{ref}) that goes into the lock-in amplifier also changes. This impedance variation is used to study the behavior of the cells.
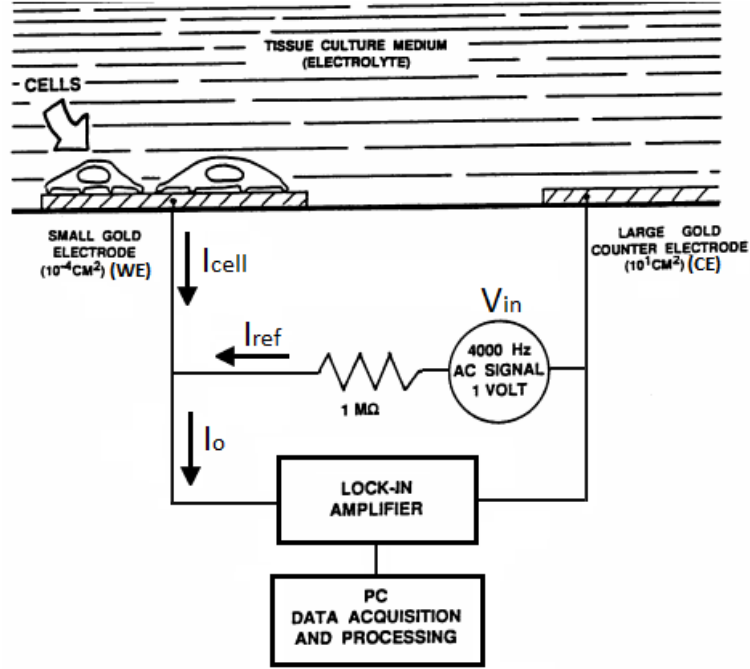
Fig. 1.1: Impedance measurement system for cell motion detection (adapted from [3]).

The pioneering work to study the motility of cells [3] using the impedance model was done by Giaever *et al.* They modeled a confluent WI-38 VA13 cell layer on the surface of the WE (shown in Fig. 1.2) and solved the first and second-order modified Bessel function [3]. In this model it is assumed that the potential above the cell surface is constant and the current flows radially through the space between the cells. The simplified impedance of the cell membrane is assumed to be purely capacitive and is given by $Z_m = 1/(j\omega C_m/2)$, where $C_m/2$ is the series equivalent capacitance of the upper and lower cell membrane and ω the radial frequency in rad/s of the applied voltage signal.
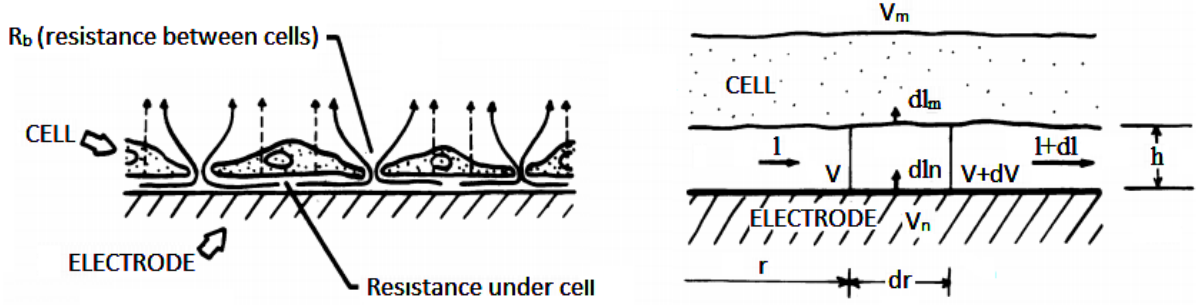
Fig. 1.2: Diagram of cells in tissue culture emphasizing the dimensions at cell-electrode interface (adapted from [3]).

In order to develop the differential equation, the space between the cells and the electrode surface is divided into infinite number of rings with inner radius r and outer radius $r + dr$, as illustrated in Fig. 1.2. The horizontal current causes the voltage change ΔV as it moves from the inner to the outer ring and the vertical current passes through the cell membrane. The modified Bessel function is given by [3]:

$$\frac{d^2V}{dr^2} + \frac{1}{r}\frac{dV}{dr} - \gamma^2 V + \beta = 0, \tag{1.1}$$

where

$$\gamma^2 = \frac{\rho}{h}\left[\frac{1}{Z_n} + \frac{1}{Z_m}\right], \tag{1.2}$$

and

$$\beta = \frac{\rho}{h}\left[\frac{V_n}{Z_n} + \frac{V_m}{Z_m}\right]. \tag{1.3}$$

In the above equations, V_n is the potential of the electrode, V_m is the potential measured at the outer cell layer, h is the height of the space between the cell and the electrode, ρ is

4

the resistivity of the cell culture medium and Z_n is the impedance of the cell-free electrode.

The solution of (1.1) is the sum of modified Bessel functions which can be solved for an impedance of a cell covered electrode Z_c, given by [3]:

$$\frac{1}{Z_c} = \frac{1}{Z_n}\left[\frac{Z_n}{Z_n + Z_m} + \frac{\frac{Z_m}{Z_n+Z_m}}{\frac{i\gamma r_c}{2}\frac{I_0(\gamma r_c)}{I_1(\gamma r_c)} + 2R_b\left(\frac{1}{Z_n} + \frac{1}{Z_m}\right)}\right], \tag{1.4}$$

and

$$\gamma r_c = \alpha\sqrt{\frac{1}{Z_n} + \frac{1}{Z_m}}, \tag{1.5}$$

where I_0 and I_1 are modified Bessel functions of the first kind of order 0 and 1, i is $\sqrt{-1}$, R_b is the lateral distance between the two cells, r_c is the radius of the cell and

$$\alpha = r_c\sqrt{\frac{\rho}{h}}. \tag{1.6}$$

It is observed from (1.4) that the total impedance depends on R_b and α, and their values can be estimated from the best fit data analysis. The resistance R_b helps to determine the amount of current flow between the cells. The parameter α is used to calculate the vertical distance h which enables the study of the surface adhesion of the cellular layer.

The traditional approach described previously [3] uses long cables to connect the electrode array to the lock-in amplifier, which adds parasitic capacitance, increases electromagnetic interference, and requires a large test setup [2]. It reduces the sensitivity and accuracy of the cell measurements leading to performance issues.

1.1 Cell Membrane Impedance Model

Human tissues are made up of cells arranged in a unique order. The basic structure of the cell consists of a phospholipid bilayer membrane which forms the cell boundary and contains protein ion channels and other molecules. This bilayer membrane does not allow the passage of the charged particles, except through the embedded ion channels. A basic model of the cell membrane is shown in Fig. 1.3.
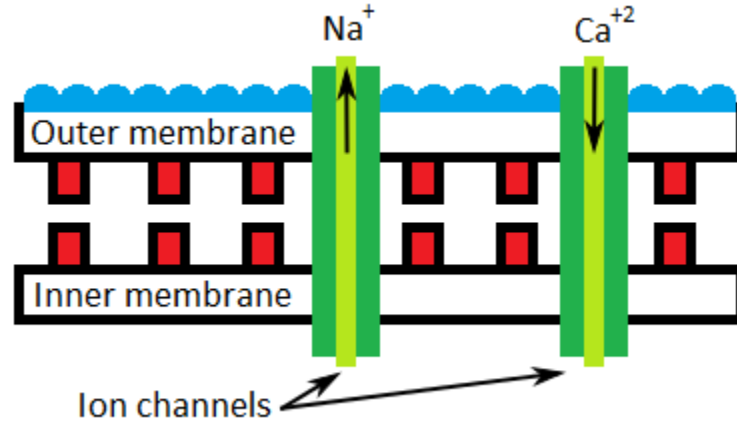
Fig. 1.3: Basic human cell membrane structure.

Ion channels are closed by default and when they are in this state the cell is said to be inactive. The outer and inner cell membrane is electrically insulating. When a ligand (molecules in living tissues which combine with cells in case of a biological event) is introduced at specific binding sites on the cell membrane, the cell is said to be activated and ion channels are opened. This allows transfer of ions Na^+, K^+, Ca^{+2}, and Cl^- through the ion channels, resulting in modified electrical properties of the cells. This forms the basis of the impedance spectroscopic technique to study the cellular response by activating a

membrane receptor, and then analyzing the current variations through the cell. Live cells in the human body communicate through G-protein coupled receptors (GPCRs) [9] and ligand gated ion channels (LGICs) [10]. The basic principle of communication is similar. As soon as the ligand-receptor interaction activates the ion channel, ions start to move in and out of the membrane, resulting in the cell impedance variation.

Such reaction of cell membrane to the activation process and generation of small currents make it possible to model the membrane structure as a combination of passive RC circuits [11][12]. Fig. 1.4 shows a circuit model representing a cellular monolayer cultured on the WE surface in the presence of an electrolyte.
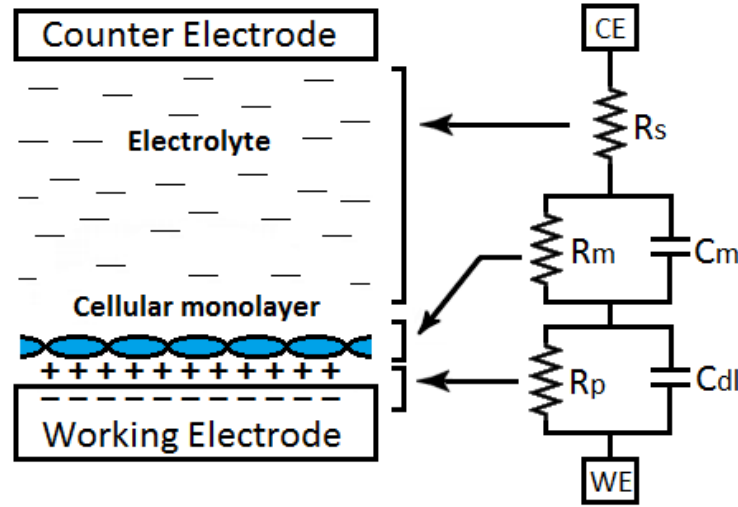
Fig. 1.4: Passive circuit model of a cellular sample and electrode-electrolyte interface.

The electrolyte resistance R_s is in series with the cell impedance, which can be modeled as a membrane capacitance C_m in parallel with membrane resistance R_m. An electrical double layer exists at the interface between the working electrode and its surrounding electrolyte due to the adsorption of ions on the surface. Some leakage current also flows

7

through the solution when the potential of the electrode is changed (polarization process). This gives rise to another impedance in series with the membrane which is modeled as a double-layer capacitance C_{dl} in parallel with a polarization resistance R_p. Since C_{dl} is normally much larger than C_m, the effect of C_{dl} can be ignored. A simplified passive circuit model of a cell membrane is shown in Fig. 1.5. Reported experimental values of a typical cell membrane resistance and capacitance are 1-2 k$\Omega\cdot$cm^2 and 1-4 μF$\cdot$cm^{-2} [2]. The range of C_m and R_m values calculated for different areas (where the area is defined as the total area of the cell membrane in contact with the WE) is given in Table 1.1.
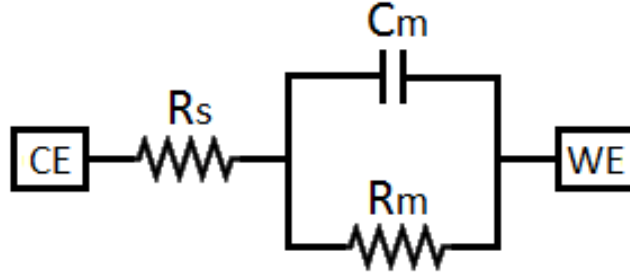
Fig. 1.5: Simplified passive circuit model of a cell membrane.

Area (μm^2)	$R_{m,min}$ (GΩ)	$R_{m,max}$ (GΩ)	$C_{m,min}$ (pF)	$C_{m,max}$ (pF)
1	100	200	0.01	0.04
10	10	20	0.1	0.4
10^2	1	2	1	4
10^3	0.1	0.2	10	40
10^4	0.01	0.02	100	400

Table 1.1: Calculated values of membrane resistance and capacitance for different electrode areas covered by a cellular layer.

1.2 Electrochemical Impedance Spectroscopy (EIS)

The general technique used to measure the cell impedance is known as electrochemical impedance spectroscopy (EIS). A small ac voltage signal at various frequencies is applied to the cellular monolayer in the presence of an electrolyte and the resulting ac current at each frequency is monitored. The ratio of input ac voltage to output current is the impedance. In cell biology, this technique of bioimpedance measurement is sometimes referred to as cellular dielectric spectroscopy (CDS) [6].

The main advantages of EIS are that it does not require the use of chemical labels and allows for real-time detection [7]. In addition to the cell sensors, EIS also finds applications in channel membrane protein biosensors [13][14], gas sensors [15] and humidity sensors [16]. Even DNA sensors can be analyzed by tracking the capacitive component of the cellular impedance [17].
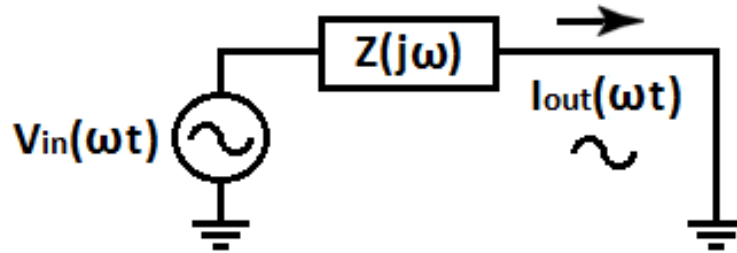
Fig. 1.6: Block diagram of a general impedance spectroscopy system.

Fig. 1.6 shows the block diagram of a general EIS system for cellular impedance measurements. Impedance $Z(j\omega)$ represents the cells being measured. If a small signal

9

voltage $V_{in}(\omega t) = A_i sin(\omega t)$, where t is the time and A_i is the input amplitude, is applied across $Z(j\omega)$, the current $I_{out}(\omega t)$ through the impedance is given by

$$I_{out}(\omega t) = A_o sin(\omega t + \phi), \tag{1.7}$$

where A_o and ϕ are the output amplitude and phase of the sensor current, respectively. The admittance $\mathbf{Y}(j\omega)$ can be written in phasor form as:

$$\mathbf{Y}(j\omega) = \frac{\mathbf{I}_{out}(j\omega)}{\mathbf{V}_{in}(j\omega)} = \frac{A_o e^{j\phi}}{A_i}, \tag{1.8}$$

where $\mathbf{I}_{out}(j\omega)$ and $\mathbf{V}_{in}(j\omega)$ are the output current and input voltage phasors, respectively. Equation (1.8) can also be expressed as

$$\mathbf{Y}(j\omega) = \frac{A_o}{A_i} cos(\phi) + j\frac{A_o}{A_i} sin(\phi) \tag{1.9}$$

using Euler's identity, where $\frac{A_o}{A_i} cos(\phi)$ is the real part and $\frac{A_o}{A_i} sin(\phi)$ is the imaginary part of the admittance. The magnitude of the admittance is given by

$$|\mathbf{Y}(j\omega)| = \frac{A_o}{A_i}, \tag{1.10}$$

and the phase is given by

$$\angle \mathbf{Y}(j\omega) = tan^{-1}\left[\frac{sin(\phi)}{cos(\phi)}\right]. \tag{1.11}$$

We have a system, where we are able to apply the input voltage and measure the output current. If we expand (1.7), we get

$$I_{out}(\omega t) = A_o cos(\phi) sin(\omega t) + A_o sin(\phi) cos(\omega t), \tag{1.12}$$

where

$$A_o cos(\phi) = Re\{A_i \mathbf{Y}(j\omega)\} = Re\{\mathbf{I}_{out}(j\omega)\}, \tag{1.13}$$

10

and

$$A_o sin(\phi) = Im\{A_i \mathbf{Y}(j\omega)\} = Im\{\mathbf{I}_{out}(j\omega)\}. \tag{1.14}$$

There are two approaches commonly used for impedance spectroscopy, namely fast Fourier transform (FFT) and frequency response analysis (FRA). These techniques are well known in the area of bio-impedance measurement and will be discussed later in the chapter.

1.2.1 Nyquist Plot

The Nyquist plot displays how the real and imaginary parts of the impedance varies over a range of stimulus frequencies. As discussed earlier, the complex cellular impedance is frequency dependent and can be analyzed by considering the passive cell model shown in Fig. 1.5. The equivalent impedance of the simplified circuit model of the cellular membrane is:

$$Z(j\omega) = \frac{(R_m + R_s)[1 + \frac{j\omega C_m R_m R_s}{R_m + R_s}]}{1 + j\omega C_m R_m}, \tag{1.15}$$

The impedance magnitude is given by

$$|Z(j\omega)| = (R_m + R_s)\sqrt{\frac{1 + (\frac{\omega C_m R_m R_s}{R_m + R_s})^2}{1 + (\omega C_m R_m)^2}}, \tag{1.16}$$

and the phase response is given by

$$\angle Z(j\omega) = -tan^{-1}\left[\frac{\omega C_m R_m^2}{R_m + R_s + \omega^2 R_s R_m^2 C_m^2}\right]. \tag{1.17}$$

A general Nyquist plot of the cellular impedance model is shown in Fig. 1.7.

11
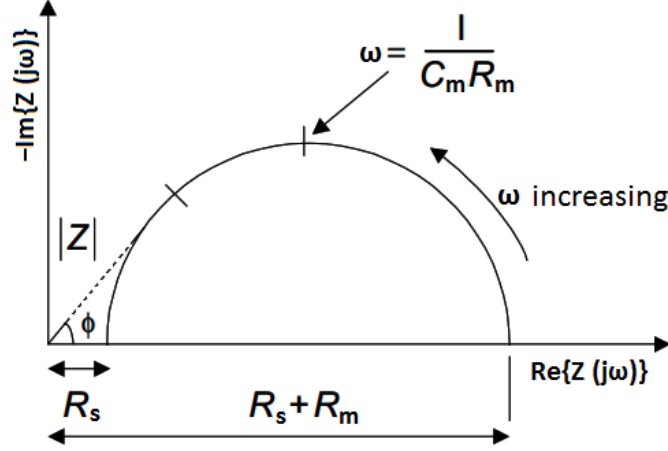
Fig. 1.7: General Nyquist plot of the cell impedance for model given in Fig. 1.5.

The center frequency of the Nyquist plot is given by $\omega = 1/(R_m C_m)$. Analysis of (1.16) shows that at very low frequencies, the capacitor can be modeled as an open circuit. The equivalent impedance is purely real and is equal to $R_s + R_m$. At very high frequencies, the capacitor can be modeled as a short circuit and the impedance is equal to the solution resistance R_s.

1.3 CMOS Integrated Circuits for Cellular Impedance Measurements

In order to address the issues related to the cell measurement systems, a more compact and robust sensor system is required. This can be achieved by integrating sensor interface circuits and an electrode array on the same complementary metal-oxide-semiconductor (CMOS) integrated circuit where the electrodes are in direct physical contact with the living cells being measured. The reduced physical distance between the sensor array and

the corresponding front-end electronics improves the measurement bandwidth and reduces susceptibility to electromagnetic interference, leading to more accurate measurements. On-chip cell sensing also provides a level of multiplexing not possible using a passive electrode array and off-chip measurement instruments.

1.3.1 Impedance Extraction Techniques

1.3.1.1 Fast Fourier Transform

FFT based methods depend on digital signal processing to extract the impedance information over a wide range of frequencies. A step or sinusoidal signal is applied to the cellular sample and the response is transmitted to a digital signal processor (DSP) after data conversion. The FFT algorithm is then applied to the time domain output to extract the real and imaginary parts of the impedance under test. A typical FFT based sensor is shown in Fig. 1.8. Its hardware requirements include an analog-to-digital converter (ADC) and a DSP kit to process the impedance data.
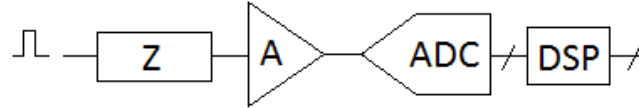
Fig. 1.8: Block diagram of the FFT approach.

1.3.1.2 Frequency Response Analysis

Frequency response analysis (FRA) is another technique that is used for EIS. It requires the sine and cosine signals which are multiplied by the input voltage signal. The result is then integrated over an entire input period to extract the real and imaginary parts of the

impedance. A block diagram of this approach is shown in Fig. 1.9. Its hardware requirements include an analog multiplier and an integrator (low-pass filter) [18]. The output current $I_{out}(\omega t)$ is multiplied by $sin(\omega t)$ and $cos(\omega t)$ to separate the real and imaginary parts. From FRA definition and (1.7), the real part of the output current is obtained by computing the following:
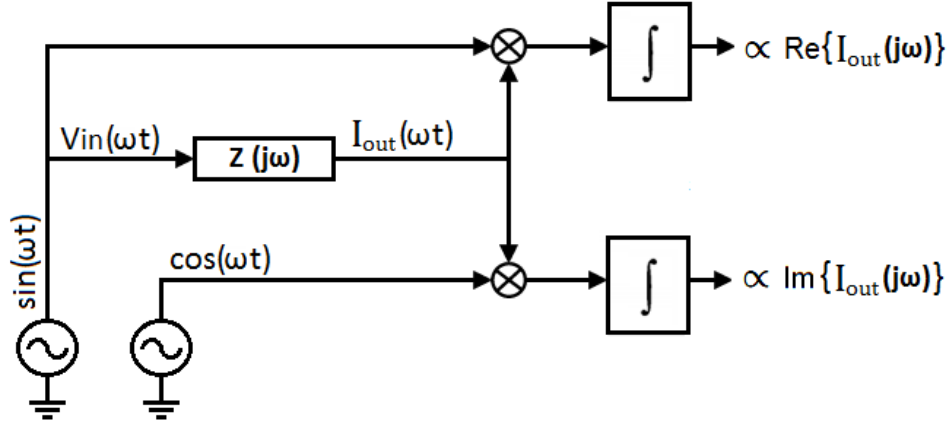
Fig. 1.9: System block diagram for a frequency response analysis approach.

$$\int_0^{NT} I_{out}(\omega t) \times sin(\omega t) \ dt = \frac{1}{2} NTA_o cos(\phi) = Re\{A_iY(j\omega)\} \times \frac{NT}{2}, \tag{1.18}$$

where T is the time period of the input sinusoidal signal, N is the number of periods, and $A_o cos(\phi)$ is the real part of the output current.

Similarly, by multiplying the output current by $cos(\omega t)$, we get the imaginary part of the cell impedance current:

$$\int_0^{NT} I_{out}(\omega t) \times cos(\omega t) \ dt = \frac{1}{2} NTA_o sin(\phi) = Im\{A_iY(j\omega)\} \times \frac{NT}{2}, \tag{1.19}$$

14

where $A_o sin(\phi)$ is the imaginary part of the output current. There are several architectures used to implement the FRA approach. These include analog impedance coherent detection and a mixed-signal lock-in amplifier architecture.

1.3.1.2.1 Analog Coherent Detection Architecture

The analog coherent detection architecture uses fully analog components to amplify and then multiply the sensor current with quadrature signals. A block diagram of the coherent detection architecture from Manickam *et al.* is shown in Fig. 1.10 [7]. A small ac voltage $V_x(\omega)$ is applied using a counter electrode and the resulting current $I_i(\omega)$ generated through the impedance under investigation is amplified by a low-noise transimpedance amplifier (TIA). The result is then multiplied with sine and cosine signals at the same frequency. The resulting signals are then filtered using a low-pass filter to remove higher-order harmonics generated during the mixing process.
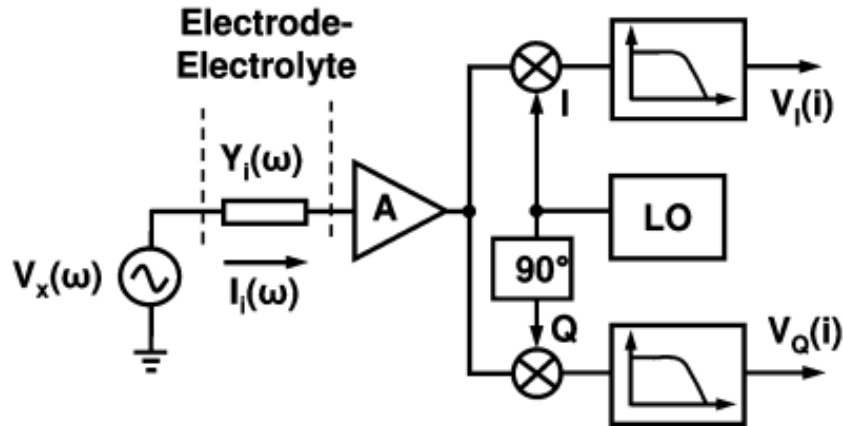
Fig. 1.10: Analog coherent detection architecture for impedance measurement from [7].

The cell admittance is given by

$$Y_i(\omega) = \frac{I_i(\omega)}{V_x(\omega)}, \qquad (1.20)$$

where $V_I(i)$ and $V_Q(i)$ are the in-phase and quadrature signals at the output of the sensor, respectively. The admittance magnitude is given by [7]

$$|Y_i(\omega)| = \frac{\sqrt{V_I^2(i) + V_Q^2(i)}}{A|V_x(\omega)|}, \qquad (1.21)$$

and the admittance phase is given by

$$\angle Y_i(\omega) = tan^{-1}\left[\frac{V_Q(i)}{V_I(i)}\right]. \qquad (1.22)$$

Performance parameters of the coherent detection system are summarized in Table 1.2. Due to the high bandwidth transimpedance amplifier and mixers, this implementation is relatively power hungry [7], which might cause biological issues as the chip heats up.

Technology	0.35 μm CMOS
Die size	2×2 mm^2
Array size	10×10
Frequency range	10 Hz – 50 MHz
Power consumption	84.8 mW
Current sensitivity	330 pA
Dynamic range	97 dB

Table 1.2: Performance parameters of the analog coherent detection architecture [7].

1.3.1.2.2 Lock-in Impedance-to-Digital Converter

An efficient impedance sensor system needs to measure the data locally, without the need of processing large amounts of cellular data which is a time consuming process. It should be able to convert analog data to digital domain, be compact, and less power hungry. This is because if the chip surface heats up, it might change the electrical properties of the cells leading to incorrect results. It should also be able to accommodate large number of on-chip electrodes to track the impedance in parallel to increase the sensor throughput [1].

Yang *et al.* proposed a lock-in impedance-to-digital converter (IDC) to implement the FRA algorithm [1]. To carry out the multiplication and integration, it makes use of a flipping capacitor and an integrator, which gives the real and imaginary parts in the analog domain. These components are then digitized by an ADC as shown in Fig. 1.11 [1].
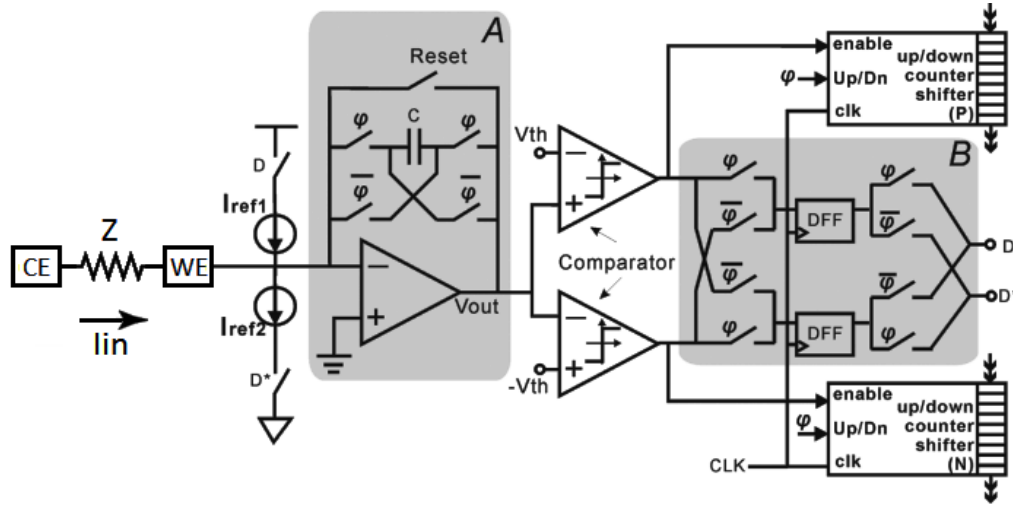
Fig. 1.11: Principle schematic of a lock-in IDC circuit, adapted from [1].

When a small ac signal V_{in} is applied across the impedance, it produces a current I_{in} which is integrated over the entire input signal time period. The clock signal φ (in phase

17

with the input ac signal) is '1' and '0' during the first and second half of the input period as shown in Fig. 1.12.
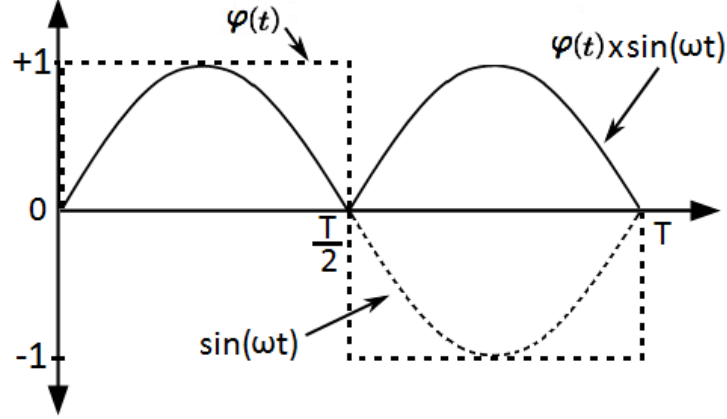
Fig. 1.12: Waveform showing φ and its multiplication with input ac signal.

Two comparators limit the integrator output between V_{th} and $-V_{th}$. During the first phase, the integrator output goes above V_{th}, flip-flop output D goes high and turns on dc current source I_{ref1}, which injects charge into the integrator and brings the output within the threshold limit. Similarly, when the integrator output goes below $-V_{th}$, D^* goes high, turning on I_{ref2} which pushes the integrator output up towards the threshold voltage. Top and bottom counters count the pulses when the integrator output is higher and lower than V_{th} and $-V_{th}$, respectively. These counts, when multiplied by the clock period and reference dc current $I_{ref,1,2}$, give the total charge injected or removed during integration. In the second half period, when φ=0, the integrator capacitor C is flipped, which reverses the charge polarity and represents the input signal multiplication by '−1'. A similar integration process is carried out during the second phase. By periodically flipping the capacitor, the input signal is multiplied by '1' and '−1', which is required by the FRA algorithm to extract the real part of impedance at the end of the integration period, and the imaginary part when φ is shifted by 90°.

1.3.1.2.2.1   Implementation of FRA Algorithm

In Fig. 1.11, the multiplication with sine and cosine signals can be implemented by flipping the integrator capacitor C periodically. When capacitor is flipped, the charged plates are swapped, resulting in current to flow in the opposite direction [1]. This is analogous to multiplying the input signal by '1' and '-1' which represents the current flow in one direction from 0 to $T/2$ and then in the opposite direction from $T/2$ to T, respectively [1].

The mathematical representation of the capacitor flipping technique to implement FRA algorithm is now discussed. To get the real part, multiplier signal $\varphi(t)$ needs to be in phase with $sin(\omega t)$ and is defined as:

$$\varphi(t) = \begin{cases} 1, \ 0 \leq t < T/2 \\ \text{-}1, \ T/2 \leq t < T \ . \end{cases} \tag{1.23}$$

The multiplication of $\varphi(t)$ from (1.23) by the input current and then integration, gives the real part of the output current:

$$\int_0^{NT} I_{out}(\omega t) \times \varphi(t) \ \mathrm{d}t = \frac{2}{\pi} NTA_o cos(\phi), \tag{1.24}$$

where $A_o cos(\phi)$ is the real part of the output current, similar to (1.18). To obtain the imaginary part, $\varphi(t)$ in phase with the $cos(\omega t)$ is defined as:

$$\varphi(t) = \begin{cases} 1, \ 0 \leq t < T/4 \\ \text{-}1, \ T/4 \leq t < 3T/4 \\ 1, \ 3T/4 \leq t < T \ . \end{cases} \tag{1.25}$$

19

This time the multiplication of $\varphi(t)$ from (1.25) by the input current and then integration, gives the imaginary part (1.26):

$$\int_0^{NT} I_{out}(\omega t) \times \varphi(t) \ \mathrm{d}t = \frac{2}{\pi} NT A_o sin(\phi), \tag{1.26}$$

where, $A_o sin(\phi)$ is the imaginary part of the output current, similar to (1.19).

The analog coherent detection approach provides a measurement bandwidth up to 50 MHz at the expense of relatively high power consumption (84.8 mW). The lock-in amplifier on the other hand consumes only 6 μW power but the bandwidth of the sensor is very low. It can measure impedance over a frequency range from 1 mHz to 10 kHz and has linearity up to 78 fA of input current, making it more sensitive to smaller currents as compared to the coherent detection technique which can detect around 330 pA of input current. The performance parameters of the lock-in IDC system are summarized in Table 1.3.

Technology	0.5 μm CMOS
Die size	3×3 mm^2
Array size	10×10
Frequency range	1 mHz – 10 kHz
Power consumption	6 μW
Current sensitivity	400 pA at f$_{in}$=1 Hz
Dynamic range	50 dB

Table 1.3: Measured performance parameters of lock-in IDC [1].

1.3.1.3   Comparison of FFT and FRA approaches

FFT based techniques have been used for quite some time to perform EIS. One advantage of the FFT-based approach is the speed of data extraction, which can be higher than the FRA-based technique. This is because a multi-frequency signal can be input and the impedance extracted over a wide band of frequencies at once, which reduces measurement time. On the other hand, the FFT approach is hardware intensive and power hungry due to the dedicated hardware required by the DSP, which implements FFT algorithm [18].

On the other hand, the FRA approach addresses the hardware issues associated with the FFT method. In contrast to FFT, FRA can have a relatively simple hardware implementation [18] comprising a multiplier, integrator, and an ADC with lower design requirements to locally process and extract the impedance information. This approach is hence suitable for a compact and low power sensor design. However, one major drawback of FRA is that it is slower as compared to FFT approach, because it only measures the impedance at one frequency at a time. Therefore it is time consuming process when FRA is used for data extraction at multiple frequencies.

In this thesis, we use an FRA approach to implement impedance extraction of live cells. The reason for pursuing FRA is that we need a compact on-chip circuit that does not require a full DSP engine. Our target is a low-frequency sensor which has low power consumption so that cells do not heat up during impedance extraction. The measurement time is also not a major concern in our application because we want to observe the cell behavior over many hours.

21

Chapter 2

System Architecture and Modeling

The purpose of this chapter is to present the architecture of the proposed CMOS impedance extraction system and develop the sensor specifications and system models which will be used to design the circuit blocks in Chapter 3. A novel approach has been adopted to implement the FRA algorithm using a synchronous voltage to frequency converter (SVFC), which is a type of ADC [19].

2.1 System Architecture

The architecture of the proposed impedance measurement system is shown in Fig. 2.1. For parallel data readout, the system comprises four channels containing an IDC and an 8×6 working electrode array. The size of each electrode is 85 μm×85 μm and is formed using the top-metal aluminum layer of the CMOS process. Live cellular samples will eventually be cultured on the surface of the electrode array. There is also a counter electrode built on-chip to set the potential of the electrolyte during the measurement process.
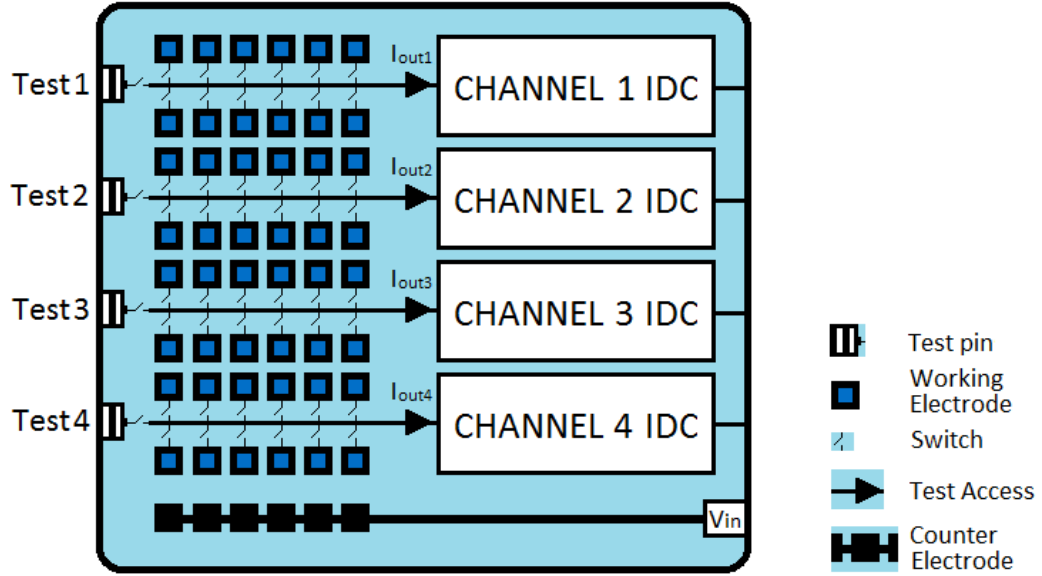
Fig. 2.1: Block diagram of the multi-channel impedance measurement system.

Working electrodes are controlled using on-chip switches which are operated by a flip-flop scan chain. External pins have also been provided to test each IDC channel independently using known input currents. Each channel has a dedicated bank of working electrodes, and therefore, the impedance of multiple cellular samples can be extracted simultaneously with distributed measurement workload.

2.2 System Specifications

Impedance sensor systems are required to measure the input current levels to extract the real and imaginary parts of the complex cellular impedance. The values of membrane resistance and capacitance determine the sensor input current level over a range of frequencies applied during EIS. Consider the simplified model of the cell membrane impedance in Fig. 1.5. For the electrode size of our chip and assuming the electrode is fully covered by the cellular monolayer, the typical values of membrane resistance, capacitance, and solution resistance from Section 1.1 are: R_m=27.68 MΩ, C_m=72.25 pF, and R_s=250 kΩ, respectively. The Nyquist plot of this cellular impedance is shown in Fig. 2.2 .
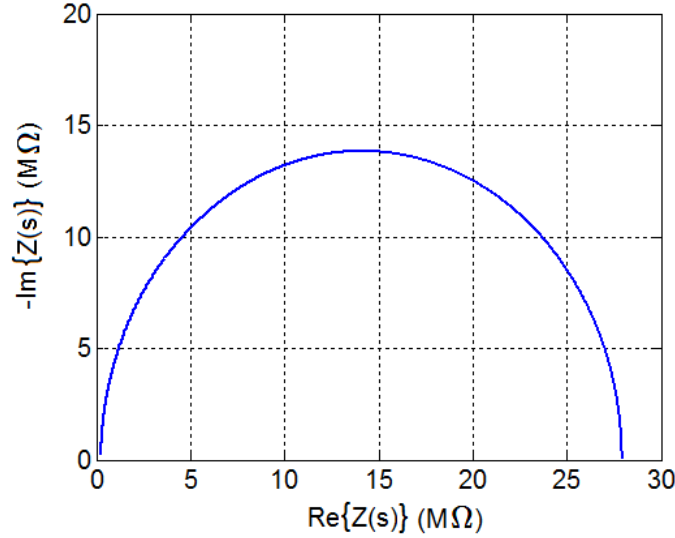
Fig. 2.2: Nyquist plot of typical cellular impedance for 85 μm×85 μm working electrode area.

To simplify the analysis, we assume that only the cell membrane capacitance is variable. The smallest input current level the sensor must measure is dictated by the smallest

24

capacitance change that the cell would undergo over the frequency range of interest. In this work, we have targeted a frequency range from 0.1 Hz to 2 kHz. Assuming the membrane capacitance increases by 1%, the magnitude and phase of the current before and after the capacitance change is shown in Fig. 2.3. A nominal input signal amplitude of 10 mV$_{pk}$ is used for the analysis to avoid a non-linear response.
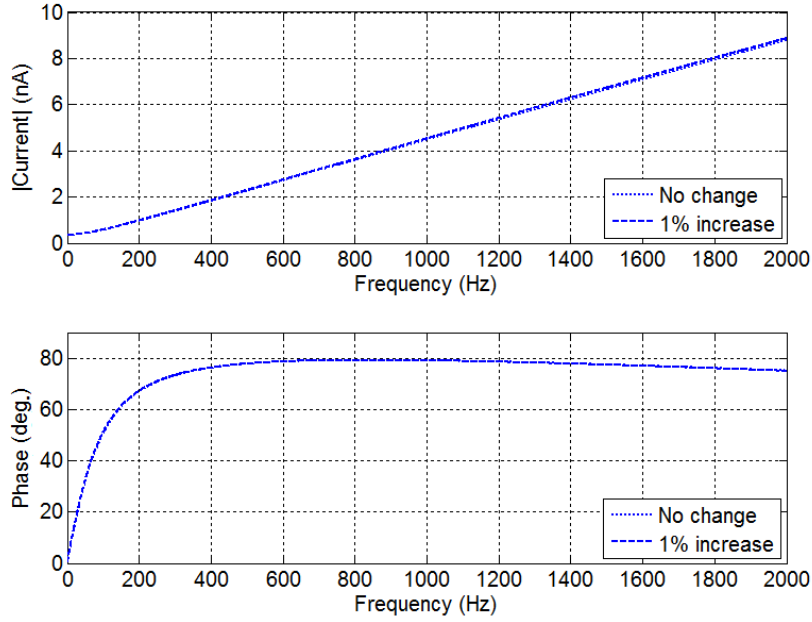
Fig. 2.3: Effect of 1% increase in C_m value on (a) magnitude (b) phase of input current level.

The change in the magnitude and phase of the input current level is shown in Fig. 2.4. It can be observed that 1% variation in the membrane capacitance causes a maximum of 85 pA change in the input current for input frequencies up to 2 kHz. In addition a phase change of $\pm 0.25^o$ occurs over this frequency interval.

From the plot given in Fig. 2.3, the maximum input sensor current is 10 nA for the given electrode area and frequency range. However, to provide flexibility, we have assumed
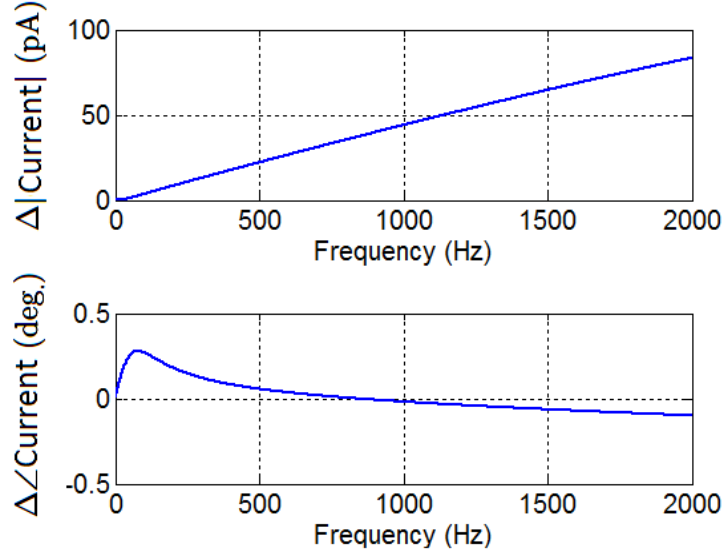
Fig. 2.4: Change in output current magnitude and phase due to 1% membrane capacitance increase.

a maximum (full-scale) current I_{FS} of 50 nA. The smallest current I_{LSB} that can be represented by the sensor is given by

$$I_{LSB} = \frac{I_{FS}}{2^N},\tag{2.1}$$

where N is the number of bits of resolution of the IDC. Assuming a 10-bit nominal resolution, the calculated least significant bit (LSB) current is 48.8 pA. Smaller currents can be measured by increasing the resolution of the sensor, which will be discussed later in this chapter.

As explained previously, power consumption is also an important design parameter in sensor systems used for EIS. We have targeted a power consumption of under 150 μW per IDC channel.

2.3 Novel Implementation of FRA Algorithm

Various schemes have been developed to implement the FRA algorithm for impedance extraction such as in [1]. As explained in section 1.3.1.2.2, the input signal multiplication by '1' and '−1' in the first and second half of the input period, respectively, is implemented by flipping the integrator capacitor periodically. Although it makes use of the entire integration period to extract the information, it is prone to charge injection effects from the switch network around the capacitor. The op amp input offset voltage also leads to an input offset current which gets integrated. This adds an offset error to the final digital value. In this design, a new algorithm and approach has been developed to extract the impedance components.

In our approach, we use half the integration period for impedance extraction, unlike the technique described in [1]. During the other half of the integration period, we automatically store the input offset voltage of the integrator op amp. This offset voltage is then subtracted during the integration phase to reduce the offset. To carry out the traditional EIS, a sinusoidal voltage signal is applied to the cultured cells. Equation (1.7) gives the amplitude and phase information of the output current. This information is then transformed into real and imaginary parts using the FRA algorithm.

A block diagram of our proposed impedance extraction system is shown in Fig. 2.5. An input voltage $V_{in}(\omega t)$ is applied to the cell impedance $Z(j\omega)$, resulting in current $I_{out}(\omega t)$. In order to extract the real part, *select* address line of 2×1 MUX is set to '0'. The signal $sin(\omega t)$ is multiplied by $A_o sin(\omega t + \phi)$ and then integrated over time period T of the input signal given by $T = \frac{2\pi}{\omega}$. The integrator output is converted to the digital domain, providing the real part at a particular frequency. Similarly, to extract the imaginary part, the select line is set to '1', and $cos(\omega t)$ is multiplied by the input current, giving the imaginary part.

27
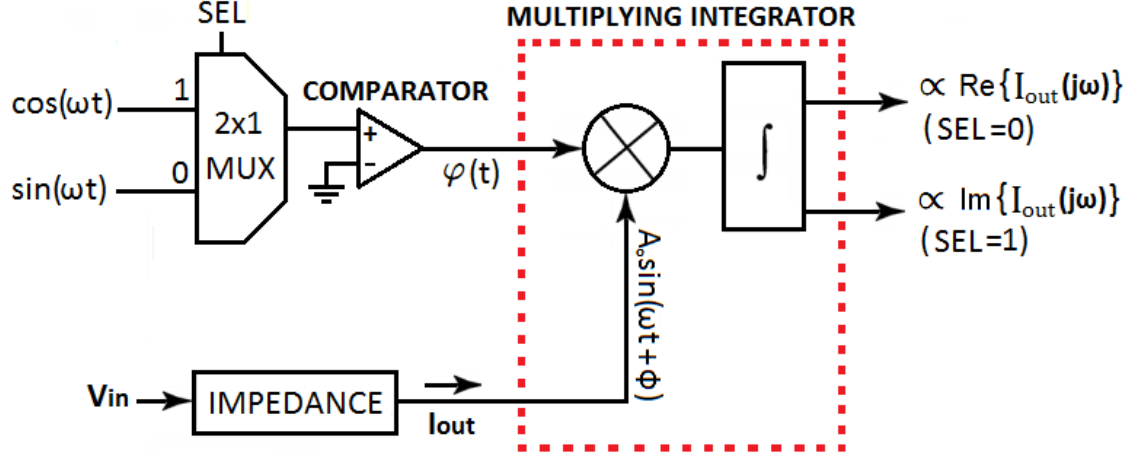
Fig. 2.5: Block diagram showing the proposed impedance extraction approach based on the FRA algorithm.

2.3.1 Real Part Extraction

The multiplier signal $\varphi(t)$ in phase with the input signal $sin(\omega t)$, as shown in Fig. 2.6 (a), is defined as:

$$\varphi(t) = \begin{cases} 1, \ 0 \leq t < T/2 \\ 0, \ T/2 \leq t < T \ . \end{cases} \quad (2.2)$$

To apply the FRA algorithm, the current $I_{out}(\omega t)$ is multiplied by signal $\varphi(t)$ and integrated over period T, given by (2.3).

$$\int_0^T I_{out}(\omega t) \times \varphi(t) \ \mathrm{d}t = \quad (2.3)$$

$$\int_0^{\frac{T}{2}} A_o sin(\omega t + \phi) \times (1) \ \mathrm{d}t + \int_{\frac{T}{2}}^T A_o sin(\omega t + \phi) \times (0) \ \mathrm{d}t \quad (2.4)$$

$$= \frac{1}{\pi} T A_o cos(\phi). \tag{2.5}$$

For N input periods, the total input charge from (2.5) is given by $\frac{1}{\pi} NTA_o cos(\phi)$, where $A_o cos(\phi)$ is the real part of the output current.

2.3.2 Imaginary Part Extraction

To obtain the imaginary part of $I_{out}(\omega t)$, the multiplier signal $\varphi(t)$ is in phase with $cos(\omega t)$, as shown in Fig. 2.6 (b) and is defined as:

$$\varphi(t) = \begin{cases} 1, \ 0 \leq t < T/4 \\ 0, \ T/4 \leq t < 3T/4 \\ 1, \ 3T/4 \leq t < T \ . \end{cases} \tag{2.6}$$

The impedance current $I_{out}(\omega t)$ is multiplied by $\varphi(t)$ and integrated over period T, given by

$$\int_0^T I_{out}(\omega t) \times \varphi(t) \ \mathrm{d}t = \tag{2.7}$$

$$\int_0^{\frac{T}{4}} A_o sin(\omega t + \phi) \times (1) \ \mathrm{d}t + \int_{\frac{T}{4}}^{\frac{3T}{4}} A_o sin(\omega t + \phi) \times (0) \ \mathrm{d}t + \int_{\frac{3T}{4}}^T A_o sin(\omega t + \phi) \times (1) \ \mathrm{d}t \tag{2.8}$$

$$= \frac{1}{\pi} T A_o sin(\phi). \tag{2.9}$$

For N input periods, the total input charge from (2.9) is given by $\frac{1}{\pi} NTA_o sin(\phi)$, where $A_o sin(\phi)$ is the imaginary part of the output current.
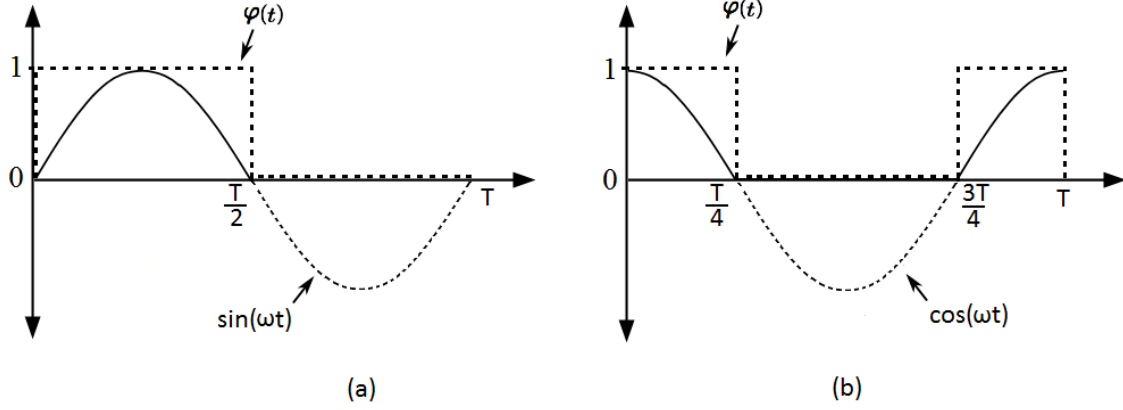
Fig. 2.6: Multiplier signal $\varphi(t)$ definition. (a) In phase with $sin(\omega t)$ (b) in phase with $cos(\omega t)$.

2.4   Impedance-to-Digital Converter Design

To realize the algorithm explained in the previous section in hardware, an SVFC architecture has been adopted. A voltage-to-frequency converter (VFC) consists of an oscillator whose frequency is linearly proportional to the control voltage; the higher the input voltage the higher the output digital count. A clocked VFC is called an SVFC [19]. Impedance extraction system based on an SVFC is developed, which makes use of a multiplying integrator and digital circuitry for FRA implementation, as shown in Fig. 2.7. Multiplication and integration can be achieved by operating the feedback switch of the integrator using a periodic signal $\varphi(t)$. The output of the multiplying integrator gives the analog value that is proportional to the real and imaginary parts of the output current and is digitized by a 16-bit counter. This digital data is transmitted serially off-chip by controlling the 16×1 MUX address lines.
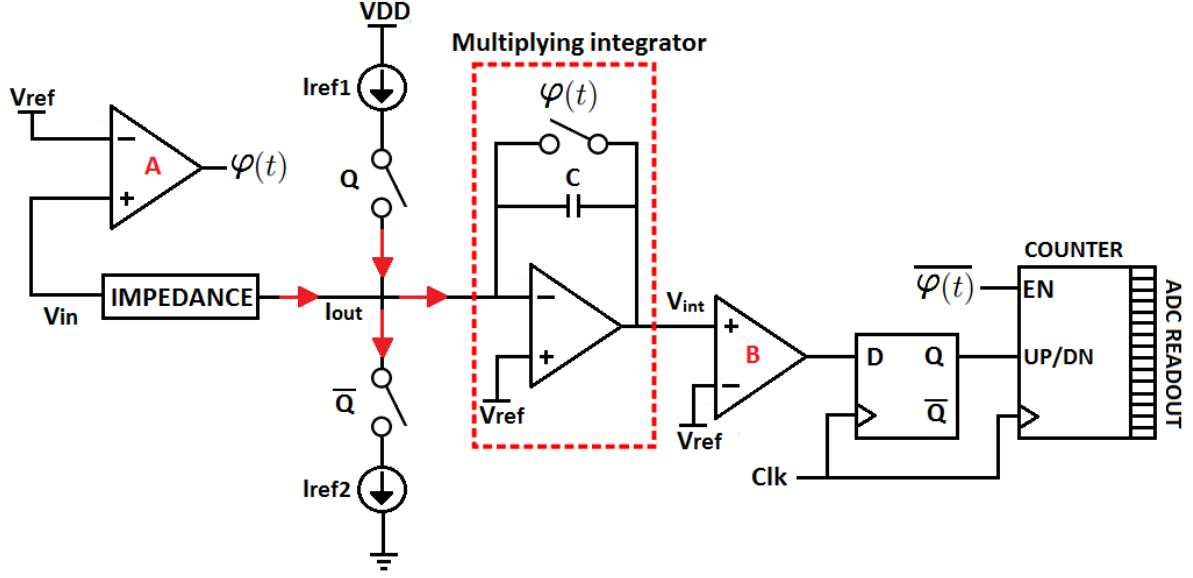
Fig. 2.7: Circuit diagram of impedance-to-digital converter built using an SVFC.

In order to get an insight of how the SVFC works, consider the waveforms shown in Fig. 2.8. When I_{out} is zero in Fig. 2.8 (a), the flip-flop output Q switches the current sources I_{ref1} and I_{ref2} at half the clock frequency, which adds and removes an equal amount of charge (assuming $I_{ref1}=I_{ref2}$) to and from the integrator. The bidirectional counter measures the time duration t_u and t_d and records an equal number of high and low pulses in this case, respectively. Therefore, the final count value at the end of the charging and discharging period is zero.

For the second case shown in Fig. 2.8 (b), I_{out} is greater than zero. The integrator output voltage V_{int} therefore ramps down for time t_d. At the next clock edge, the flip-flop output changes state and turns on the negative current source I_{ref2} which removes charge from the integrator. The integrator output voltage starts to ramp up for a time duration t_u which is proportional to the output current I_{out}. In this case, the frequency of Q is less

31

than half the clock frequency so the counter value will not be zero.
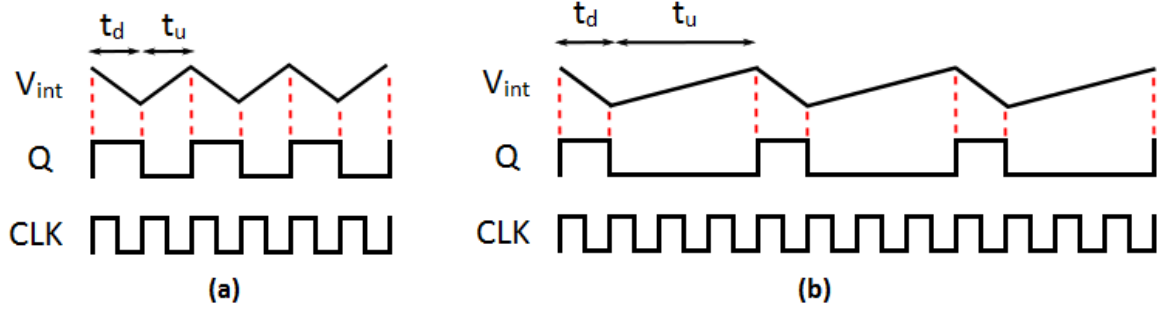
Fig. 2.8: SVFC waveforms when the output current is (a) equal to zero and (b) greater than zero.

As an example, consider the simulation waveforms of the SVFC in Fig. 2.9. An input ac voltage V_{in} of 10 mV peak amplitude and 390.6 Hz (Fig. 2.9 (a)) is applied to a 200 kΩ resistance which produces small ac current I_{out}. Signal V_{in} also goes to comparator A which generates an in-phase square wave signal $\varphi(t)$ (Fig. 2.9 (b)) which controls the feedback switch of the integrator. As mentioned earlier, in the first half period when $\varphi(t)=1$ and the feedback switch is on, the input offset of the integrator op amp is stored. During the second half period, when $\varphi(t)=0$, the feedback switch turns off and the input current starts to integrate. As the integrator output voltage (shown in Fig. 2.9 (c)) rises above the reference voltage V_{ref} (set to 900 mV in this example), the output of comparator B, and hence the flip-flop output Q, goes high (Fig. 2.9 (d)). This turns on the current source I_{ref1} which injects charge into the integrator, pushing its output below the reference voltage. Similarly, when the integrator output is lower than V_{ref}, $\overline{Q}$ goes high and turns on I_{ref2} which removes charge and brings the integrator output above V_{ref}. At the end of the integration period T (2.56 ms in this example), the measured current is digitized by a 16-bit digital counter, which is disabled as soon as $\varphi(t)$ goes high for the next input period.

32

This data is serially shifted out to a field programmable gate array (FPGA) and then to a PC via universal bus service (USB) connection to extract the impedance components from the measured current.
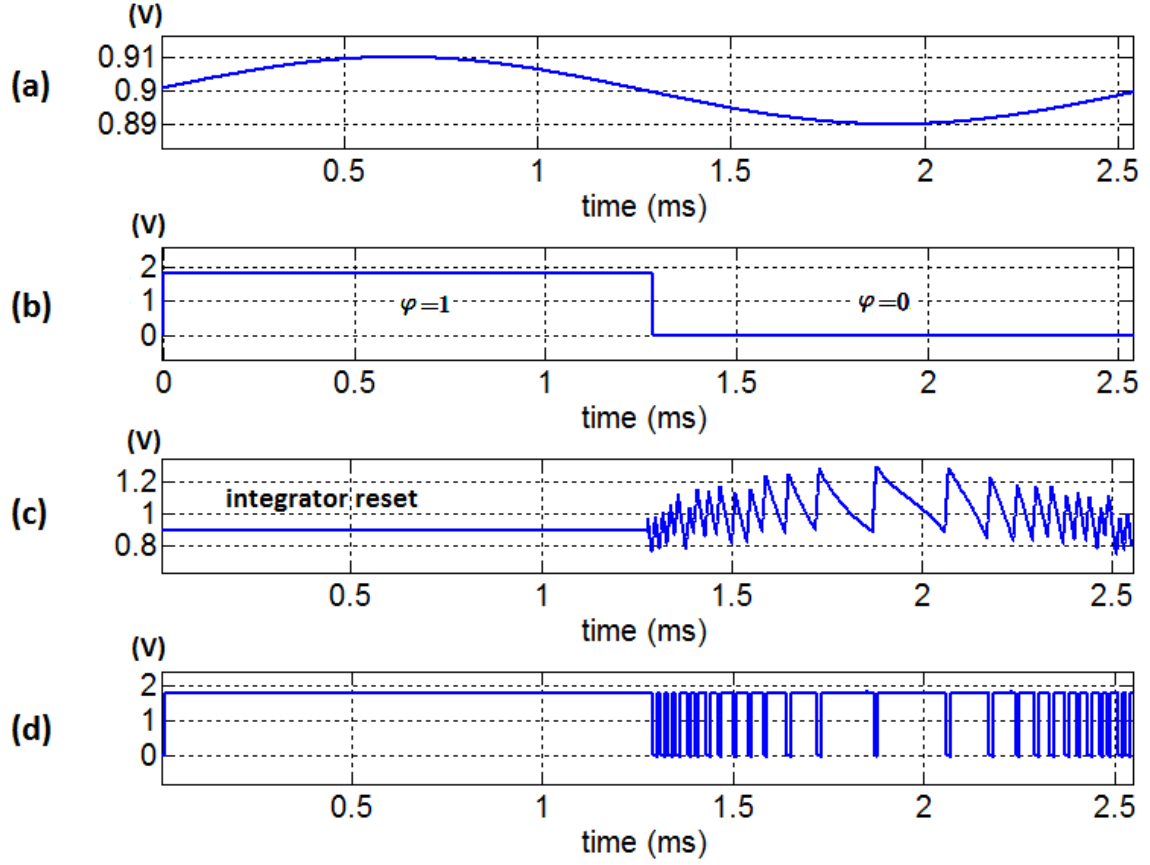
Fig. 2.9: Simulation waveforms of the SVFC based impedance sensor for 200 kΩ resistance at 390.6 Hz input signal frequency. (a) Input ac voltage signal, (b) comparator A output, (c) integrator output, and (d) flip-flop output.

2.5   Principle of Impedance Extraction

To describe the concept of impedance extraction using integrated circuit components, again consider the SVFC in Fig. 2.7. The amount of input dc current injected (I_{ref1}) and removed (I_{ref2}) from the integrator (Fig. 2.7), when multiplied by the time for which it is applied, gives the amount of charge Q_{out} transferred during the integration phase. From Fig. 2.8 (b), the integrator output voltage V_{int} at the end of the charging and discharging period must be equal to zero:

$$-\frac{I_{out} + I_{ref1}}{C}t_d + \frac{I_{ref2} - I_{out}}{C}t_u = 0. \tag{2.10}$$

Equation (2.10) can be simplified to

$$I_{out}(t_u + t_d) = I_{ref2}t_u - I_{ref1}t_d, \tag{2.11}$$

for a single charging and discharging period $t_u + t_d$. For a complete input signal period T, (2.11) can be written as

$$\int_0^T I_{out} \ \mathrm{d}t = \int_0^{t_u} I_{ref2} \ \mathrm{d}t - \int_0^{t_d} I_{ref1} \ \mathrm{d}t, \tag{2.12}$$

where $\int_0^{t_d} I_{ref1} \ \mathrm{d}t$ and $\int_0^{t_u} I_{ref2} \ \mathrm{d}t$ is the total amount of charge added and removed from the integrator in one input period.

Suppose $\sum_{i=1}^{N} D_i$ and $\sum_{i=1}^{N} D_i^*$ are the positive and negative counts when the current sources I_{ref1} and I_{ref2} are on, respectively. The charge added and removed can be calculated by multiplying positive counts by $I_{ref1}T_{clk}$ and negative counts by $I_{ref2}T_{clk}$. For the first half cycle, from t=0 to t=$T/2$, after adding residue charge CV_{res} at the integrator output, (2.12) can be written as [1]:

$$\int_0^{\frac{T}{2}} I_{out} \ \mathrm{d}t = CV_{res1} + I_{ref1}T_{clk} \sum_{i=1}^{N} D_i - I_{ref2}T_{clk} \sum_{i=1}^{N} D_i^*. \tag{2.13}$$

Similarly, for the second half cycle from t=$T/2$ to t=T, (2.11) can be written as:

$$\int_{\frac{T}{2}}^{T} I_{out} \ \mathrm{d}t = CV_{res1+res2} + I_{ref1}T_{clk} \sum_{i=N+1}^{2N} D_i - I_{ref2}T_{clk} \sum_{i=N+1}^{2N} D_i^*. \tag{2.14}$$

The total input charge from t=0 to t=T can be found by combining (2.13) and (2.14):

$$\int_0^{\frac{T}{2}} I_{out} \ \mathrm{d}t + \int_{\frac{T}{2}}^{T} I_{out} \ \mathrm{d}t \approx I_{ref}T_{clk} \left[\sum_{i=1}^{N} D_i - \sum_{i=1}^{N} D_i^* + \sum_{i=N+1}^{2N} D_i - \sum_{i=N+1}^{2N} D_i^* \right]. \tag{2.15}$$

The residue voltages CV_{res} have been ignored because their magnitude is negligible compared to the counts and can be regarded as noise over the digital counts [1]. Also, dc current sources I_{ref1} and I_{ref2} are set equal to I_{ref} which factors out $I_{ref}T_{clk}$. Now (2.15) can be simplified to

$$\int_0^{T} I_{out} \ \mathrm{d}t = I_{ref}T_{clk} \left[P_{counter1} - N_{counter1} + P_{counter2} - N_{counter2} \right], \tag{2.16}$$

where $P_{counter1}$ and $P_{counter2}$ are the positive, and $N_{counter1}$ and $N_{counter2}$ are the negative counts during the first and second half of the input period, respectively. Bidirectional counter is disabled during the first half period. Therefore, using $P_{counter1} - N_{counter1} = 0$ in (2.16) gives the expression for the total input charge:

$$\int_0^{T} I_{out} \ \mathrm{d}t = I_{ref}T_{clk}[P_{counter2} - N_{counter2}]. \tag{2.17}$$

As discussed earlier, the FRA algorithm gives the real and imaginary part of the impedance current which is found by multiplying the input current by signal $\varphi(t)$ and

then integrating it over a period T. This is effectively the amount of integrated charge during the input period. After solving (2.5) and (2.17), we get:

$$Re\{I_{out}(j\omega)\} = I_{ref}T_{clk}[P_{counter2} - N_{counter2}] \times \pi/T, \qquad (2.18)$$

where $P_{counter2} - N_{counter2}$ is the final value of the bi-directional counter at the end of the input period T and $\varphi(t)$ is in phase with $sin(\omega t)$. Same expression can be used to calculate the imaginary part of the output current $Im\{I_{out}(j\omega)\}$ when $\varphi(t)$ is in phase with $cos(\omega t)$.

The real and imaginary parts are then used to calculate the impedance under test. The impedance output current $I_{out}(\omega t) = A_o sin(\omega t + \phi)$ carries the impedance information, where A_o and ϕ are the magnitude and phase of the extracted current, respectively, and given by:

$$A_o = \sqrt{Re\{I_{out}(j\omega)\}^2 + Im\{I_{out}(j\omega)\}^2}, \qquad (2.19)$$

$$\phi = tan^{-1}\left[\frac{Im\{I_{out}(j\omega)\}}{Re\{I_{out}(j\omega)\}}\right]. \qquad (2.20)$$

The impedance can be calculated by dividing the known input signal amplitude A_i by the extracted value of the output current, as given by

$$Z(j\omega) = \frac{A_i}{A_o \angle \phi}, \qquad (2.21)$$

where '$\frac{A_i}{A_o}$' and '$-\phi$' are the magnitude and phase of the measured impedance.

2.6 Resolution of Impedance Sensor

The system is operated at a clock rate of 100 kHz. This frequency is chosen so that an input current of 100 nA and a feedback capacitor of 2 pF does not saturate the integrator. Considering the impedance measurement at a single frequency cycle, the input signal is integrated over half input period and therefore, the nominal resolution of the sensor is given by $\frac{T}{2T_{clk}}$, where T and T_{clk} are the input stimulus and clock periods, respectively. For example, if the input stimulus frequency is 390.6 Hz, then the resolution of the impedance sensor will be 128 (7-bits). In order to increase the resolution, we have to consider M number of input cycles (i.e., for a desired resolution of 8-bits, the value of M would be 2). Similarly, we can take measurements over multiple input cycles M to achieve the desired resolution by dividing (2.18) by M.

2.7 Dynamic Range Programmability

The dynamic range of a current sensor is the ratio of the maximum to the minimum value of the measured current. For this impedance sensor, the maximum value of the current is determined by the integrator saturation limit (900 mV) from the reference voltage and the minimum current can be found from (2.18). To make the dynamic range of the impedance sensor more flexible, the integrator in this design is provided with a bank of four 2 pF capacitors and reference current sources of 50 nA, 200 nA, and 1 μA. For a clock frequency of 100 kHz and input signal frequencies of 1 Hz, 10 Hz, 100 Hz and 1000 Hz, the maximum current range and the nominal resolution of the system is given in Table 2.1 for 50 nA, Table 2.2 for 200 nA, and Table 2.3 for 1 μA of input dc current.

C_F (pF)	f_{in} (Hz)	$I_{in,min}$ (pA)	$I_{in,max}$ (nA)	Nominal Resolution (bits) (for one input period)
2	1	1.6	180	17
	10	16		14
	100	160		11
	1000	1600		7
4	1	1.6	360	18
	10	16		15
	100	160		12
	1000	1600		8
6	1	1.6	540	19
	10	16		16
	100	160		12
	1000	1600		9
8	1	1.6	720	19
	10	16		16
	100	160		13
	1000	1600		9

Table 2.1: Dynamic range programmability of IDC for 50 nA reference current at 100 kHz clock.

C_F (pF)	f_{in} (Hz)	$I_{in,min}$ (pA)	$I_{in,max}$ (nA)	Nominal Resolution (bits) (for one input period)
2	1	6.3	180	15
	10	63		12
	100	630		9
	1000	6300		5
4	1	6.3	360	16
	10	63		13
	100	630		10
	1000	6300		6
6	1	6.3	540	17
	10	63		14
	100	630		10
	1000	6300		7
8	1	6.3	720	17
	10	63		14
	100	630		11
	1000	6300		7

Table 2.2: Dynamic range programmability of IDC for 200 nA reference current at 100 kHz clock.

C_F (pF)	f_{in} (Hz)	$I_{in,min}$ (nA)	$I_{in,max}$ (nA)	Nominal Resolution (bits) (for one input period)
2	1	0.0314	180	13
	10	0.314		10
	100	3.14		6
	1000	31.4		3
4	1	0.0314	360	14
	10	0.314		11
	100	3.14		7
	1000	31.4		4
6	1	0.0314	540	15
	10	0.314		11
	100	3.14		8
	1000	31.4		5
8	1	0.0314	720	15
	10	0.314		12
	100	3.14		8
	1000	31.4		5

Table 2.3: Dynamic range programmability of IDC for 1 μA reference current at 100 kHz clock.

2.8 Operational Amplifier Offset Correction

Practical operational amplifiers exhibit non-idealities including finite dc gain, limited band-width, dc offsets, etc. For this application, large dc voltage offsets can limit the signal swing of the integrator output and reduce the performance of the impedance sensor. In order to remove the effect of dc offsets in our system, we store the op amp input offset voltage during the first half cycle of the input period when the integrator is in a unity feedback configuration, and then subtract this offset during the next period.

Consider the block diagram of the offset correction circuit in Fig. 2.10. During the first half period, the value of $\varphi(t)$ is '1', which sets the integrator in a unity feedback mode (Fig. 2.11 (a)). The op amp internal offset voltage V_{os} will be stored on the capacitor $C2$. During the next half period, when $\varphi(t)$ is '0' (Fig. 2.11 (b)), $V_{ref} - V_{os}$ is applied at the non-inverting terminal of the integrator. In this phase, the offset voltage is canceled out during integration. Similarly, for the next period, offset is stored in the first half cycle and applies the correction during the second half period. The offset correction is carried out continuously during the consecutive measurement cycles to remove any uncertainty from the integrator output. It is important to note that the signals $\varphi_1(t)$ and $\varphi_2(t)$ are produced from $\varphi(t)$ using a non-overlapping clock generator discussed in the next chapter.

Fig. 2.10: Implementation of the offset correction technique.

Fig. 2.11: Offset correction circuit for (a) the first half and (b) the second half of the input period T.
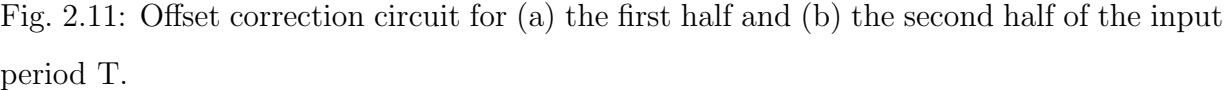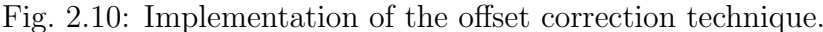
2.9   System Specifications

Table 2.4 gives the system specifications of our impedance sensor.

Parameter	Target value
Full scale current (I_{FS})	50 nA
Minimum current (I_{LSB})	48.8 pA
IDC nominal resolution	10 bit
Measurement bandwidth	2 kHz

Table 2.4: System specifications.

Chapter 3

Circuit Design

This chapter focuses on the circuit level design of the impedance sensor blocks discussed in Chapter 2. This system consists of a multiplying integrator, comparator, flip-flop, digital counter and MUX which process the impedance information and transmit the digital data to an FPGA. Transistor and component level design in a 1.8 V 0.18 μm CMOS process is presented in the following sections.

3.1 Integrator

In our impedance sensor, a multiplying integrator detects the small input current signals. A circuit diagram of an ideal integrator is shown in Fig. 3.1. The time domain output voltage $V_o(t)$ of the integrator is given by

$$V_o(t) = -\frac{1}{C} \int_0^t I_{in}(\tau) \ d\tau, \tag{3.1}$$

where C is the feedback capacitor and I_{in} is the input signal current.
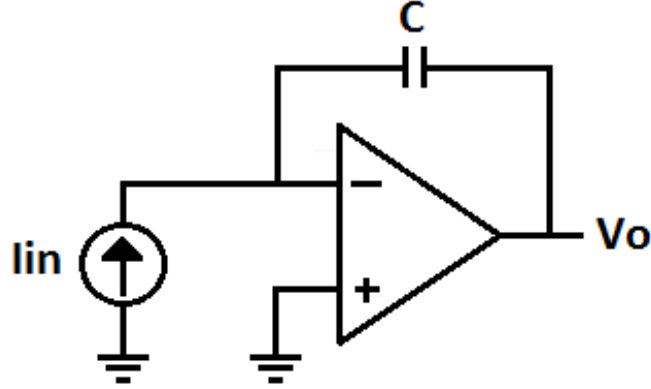
Fig. 3.1: Ideal integrator.

The transfer function $V_o(s)/I_{in}(s)$ of the ideal integrator is given by

$$\frac{V_o(s)}{I_{in}(s)} = -\frac{1}{sC}. \tag{3.2}$$

From (3.2), there is a single pole at dc so the gain of the ideal integrator starts to roll off from $\omega{=}0$ rad/s at -20 dB/dec. In practical integrators, the op amp input offset voltage causes dc current to flow into the integrator. If the circuit is allowed to integrate long enough, the integrator output will saturate. Therefore, in any practical implementation, a parallel reset switch must be included to periodically reset the charge on the capacitor.

Now we describe the response of a non-ideal integrator. Consider the open-loop transfer function $A_{OL}(s)$ of a non-ideal op amp with dc gain A_o and a dominant pole at ω_{3dB}:

$$A_{OL}(s) = \frac{A_o}{1 + \frac{s}{\omega_{3dB}}}. \tag{3.3}$$

The closed-loop transfer function $A_{CL}(s)$ of the non-ideal integrator is given by

$$A_{CL}(s) = -\frac{1}{(sC)(1 + \frac{s}{\omega_t})} \quad , \tag{3.4}$$

where ω_t is the unity-gain frequency of the op amp and is approximately equal to $A_o\omega_{3dB}$. The frequency magnitude response of a non-ideal integrator is shown in Fig. 3.2. We observe from (3.4) that there is a low frequency pole at 0 Hz. The integrator gain is very high initially, but as the input frequency increases, capacitor impedance gets smaller and the gain keeps decreasing at -20 dB/dec. At very high frequencies, there is another pole at the unity gain frequency ω_t of the open-loop response, resulting in the gain falling by -40 dB/dec.
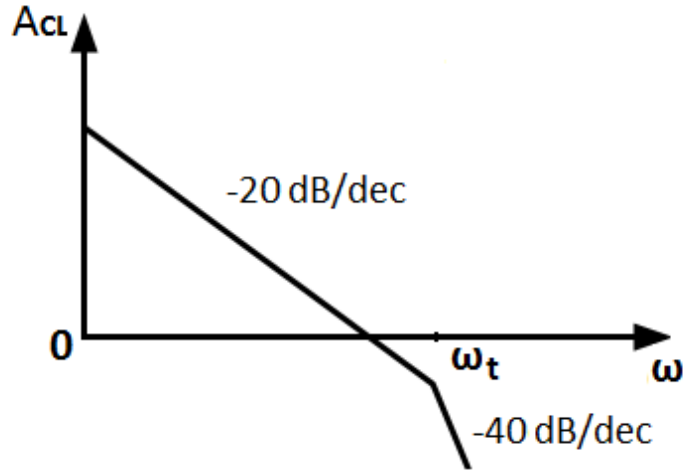
Fig. 3.2: Frequency magnitude response of a non-ideal integrator.

3.1.1   Integrator Design

From the system specifications given in Chapter 2, we selected 10-bit resolution for this system. Finite op amp dc gain leads to a steady-state error in feedback systems. Assuming a maximum of 0.5 V_{LSB} error that can be tolerated in the integrator output during the reset phase, the gain error E_G is given by:

$$E_G = \frac{0.5 V_{LSB}}{V_{FS}} \times 100\%. \tag{3.5}$$

For a 10-bit IDC, the gain error is given by:

$$E_G = \frac{1}{2} \times \frac{1}{2^{10}} \times 100\%. \tag{3.6}$$

From (3.6), required gain error is 0.05%. In unity feedback (when the feedback factor β is 1), the closed-loop response of a feedback system with an open loop dc gain A_o is given by:

$$A_{CL} = \frac{A_o}{1 + A_o}. \tag{3.7}$$

With a maximum tolerable gain error of 0.05%, the minimum required gain of the op amp, calculated from (3.7), is 2000 V/V (66 dB). This means the integrator output needs a minimum open loop gain of 66 dB to settle within a 0.5 LSB tolerance band. The clock rate in our system is 100 kHz and therefore the period is 10 μs. We want the integrator output to settle down within the desired error band before the next clock edge arrives. Taking the Laplace inverse of (3.4), we get the time domain expression of the integrator output voltage with a non-ideal op amp response:

$$V_o(t) = -\frac{I_o}{C} \ t + \frac{I_o}{C\omega_t} \left[1 - e^{-\omega_t \times t}\right] \quad \text{(for } t \geq 0\text{)}, \tag{3.8}$$

where I_o is the amplitude of an input current step and C is the integrator feedback capacitor. Equation (3.8) gives the time constant τ of a non-ideal integrator, $\tau = \frac{1}{\omega_t}$. If the integrator step response error is to be no more than 0.5 V_{LSB} after 5 μs (half the clock period) with a step input amplitude of 50 nA, the value of ω_t from (3.8) must be at least 4.5 MHz. This corresponds to a 3 dB bandwidth of 2 kHz. If a faster transient response is required, the bandwidth of the op amp should be increased accordingly which would also increase the power consumption of the system.

3.1.2 Operational Amplifier Design

There are variety of amplifier architectures available that can be used to design an integrator depending on the design specifications. For this application, we selected the telescopic cascode op amp, due to its better noise performance and low power consumption as compared to the folded cascode op amp [30]. These design parameters are important for our application, as a high power system might heat up the cells and affect the cell properties, and high noise will limit the minimum detectable current.

In order to increase the integrator output signal swing and reduce the power consumption, most of the op amp transistors are operated in the moderate inversion region. A circuit diagram of the designed telescopic cascode amplifier is shown in Fig. 3.3. The tail current is chosen to be 20 μA, which is sufficient to provide a 1 μA current to the feedback capacitor without disturbing the operating point of the op amp. The total power consumption of the op amp is 90 μW, including the bias transistor currents. An overdrive voltage of 50 mV is used for the op amp transistors to keep them in moderate inversion.

48
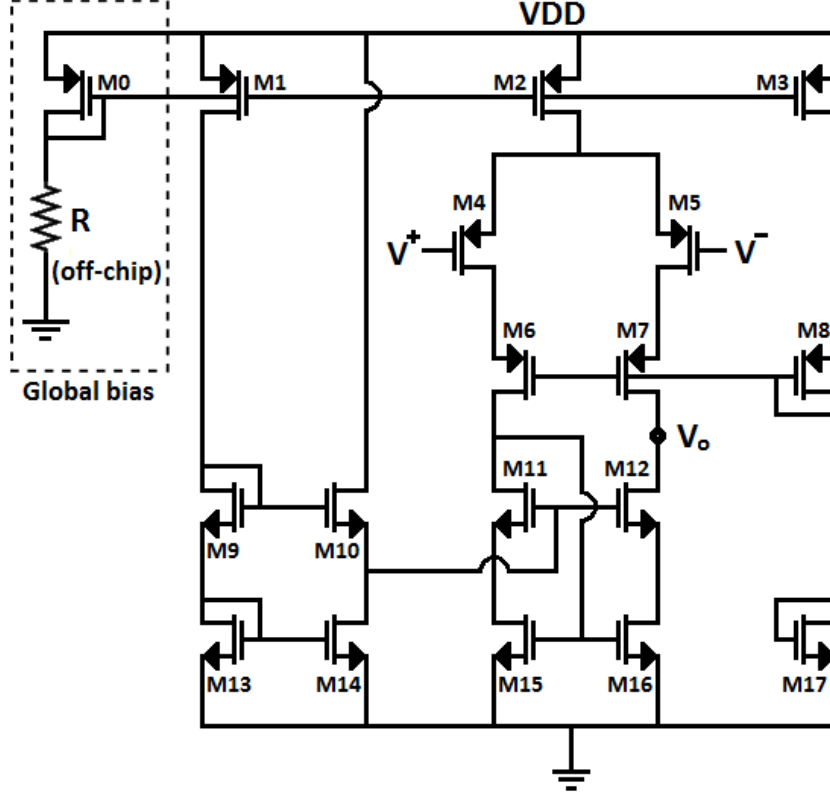
Fig. 3.3: Circuit diagram of telescopic cascode amplifier.

We have used weak inversion equations to derive the transistor dimensions because the I-V equations for moderate inversion are not well defined. The drain current I_D of a MOSFET in weak-inversion (subthreshold) [31] is given by

$$I_D = I_{DO}\frac{W}{L}e^{\frac{V_{OV}}{nV_T}},\eqno(3.9)$$

where n is the subthreshold coefficient (n$\approx$1.6), V_{OV} is the overdrive voltage of the transistor, V_T is the thermal voltage ($V_T$$\approx$26 mV), and I_{DO} is a process dependent constant given by [31]

49

$$I_{DO} = (n-1)\mu C_{ox} \left(\frac{kT}{q}\right)^2. \tag{3.10}$$

In the above equation, μC_{ox} is a technology constant and its value for 0.18 μm CMOS technology is 270 μA/V^2 and 70 μA/V^2 for NMOS and PMOS devices, respectively and kT/q gives the thermal voltage V_T.

The gain of the telescopic cascode amplifier is given by

$$A_v \approx g_{m4}[(g_{m12} \times r_{o12} \times r_{o16})//(g_{m7} \times r_{o7} \times r_{o5})], \tag{3.11}$$

where g_m and r_o are the small-signal transconductance and output resistance of a transistor, respectively. To allow for flexibility in the system, the op amp was designed to have a unity-gain bandwidth 10$\times$ greater than the specification. Using $g_m \approx 0.12$ mS and amplifier output resistance $R_{out} \approx 92$ MΩ in (3.11), the dc gain of the op amp is calculated to be 80.9 dB. To calculate the bandwidth of the op amp we use $f_{3dB} = 1/(2\pi R_{out}C_L)$ for a nominal load capacitance of 300 fF which gives 5.8 kHz and a unity gain bandwidth of 64.2 MHz. The transistor dimensions calculated from (3.9) are given in Table 3.1.

The simulated loop gain magnitude and phase response of the telescopic cascode op amp in a unity feedback configuration is shown in Fig. 3.4. The dc gain of the amplifier is 82.4 dB, the 3 dB bandwidth is 3.6 kHz, and the unity gain bandwidth ω_t is 44.2 MHz. The phase margin of the op amp is 61°, which shows that it is stable when used in a unity gain configuration.

Fig. 3.4: Simulated loop gain of the telescopic cascode op amp in unity feedback (a) magnitude (dB) (b) phase (deg.), (TT corner at 27°C).

Transistor	Width (μm)	Length (μm)
M0, M2	14	1
M1, M3	7	1
M4, M5	31	1
M6, M7, M8	31	1
M9	2	4
M10, M13, M14	2	1
M11, M12	10	1
M15, M16, M17	10	1

Table 3.1: Telescopic cascode amplifier transistor dimensions.

51

3.1.3 Op Amp Output Signal Swing

To increase the signal swing of the telescopic cascode amplifier, a wide swing cascode mirror has been designed. The width of M9 in Fig. 3.3 is set four times smaller than M10 and M13 so that overdrive voltage of M9 is $2V_{OV}$ and the overdrive voltage of M10, M13, M14 is V_{OV}. As a result, M11 and M12 are biased at $2V_{OV}+V_t$, where V_t is the transistor threshold voltage. Therefore the minimum output voltage $V_{out,min}$ of the op amp is given by [30]

$$V_{out,min} = 2V_{OV}. \tag{3.12}$$

For a 20 μA bias current and transistors designed in the moderate inversion region, the value of the minimum output voltage of the op amp from (3.12) is 100 mV. Similarly, the maximum output voltage $V_{out,max}$ of the op amp is given by

$$V_{out,max} = V_{DD} - V_{OV2} - V_{OV5} - V_{OV7}. \tag{3.13}$$

For a 50 mV overdrive voltage of the input differential transistors and 200 mV overdrive for the tail transistor M2, the maximum output voltage of the telescopic op amp from (3.13) is 1.5 V. The output swing of the op amp is defined as

$$V_{out,swing} = V_{out,max} - V_{out,min}, \tag{3.14}$$

which gives 1.4 V of output signal swing.

3.1.4   Op Amp Slew Rate

One of the practical op amp limitations is its slew rate, or the maximum rate at which the output voltage can change for a given load. If a large positive step signal is applied to the gate of transistor M4, M5 will turn on and M4 will remain in cutoff. Since there is no current flowing through the left branch of the amplifier, M15 and M16 will also be off. The tail current I_{tail} through M5 and M7 will charge the load capacitor C_L, where the positive slew rate SR^+ is given by [32]

$$SR^+ = \frac{I_{tail}}{C_L}. \tag{3.15}$$

For a 2 pF capacitive load and tail current of 20 μA, the positive slew rate of the op amp is calculated to be +10 V/μs. Similarly, a positive step response at the gate of M5 will turn this transistor off and M4, M15, and M16 will turn on. The current will flow from load capacitor to ground through M12 and M16, resulting in a negative slew rate SR^- given by

$$SR^- = -\frac{I_{tail}}{C_L}. \tag{3.16}$$

The negative slew rate of the op amp is calculated as -10 V/μs. Our IDC is capable of measuring the impedance currents up to 1 μA, therefore the maximum rate the integrator will charge for a nominal load of 2 pF is 0.5 V/μs. This shows that the sensor is not slew rate limited for this application.

3.1.5 Telescopic Cascode Amplifier Noise

Noise is a random phenomenon which is inherent in all practical systems and limits the dynamic range of the sensor. For the impedance sensor application, a telescopic cascode amplifier has been selected because of its better noise performance as compared to other op amp circuits such as a folded cascode topology.

From noise analysis of our amplifier in Fig. 3.3, transistors M6, M7, M11 and M12 do not contribute significantly to the output noise of the op amp. The input pair M4 and M5, and the load transistors M15 and M16 are the main sources of thermal noise in the op amp. The current noise power spectral density (PSD) of a MOSFET is given by $\overline{I_{n,th}^2}(f) = \frac{8}{3}kTg_m$, where k is the Boltzmann constant and T is the absolute temperature. These devices also produce low frequency noise due to traps near the $Si - SiO_2$ interface of the transistors, which is known as flicker noise. A PMOS input differential pair is used to reduce the flicker noise and enhance the input common mode range of the op amp. The flicker noise current PSD is given as $\overline{I_{n,f}^2}(f) = \frac{K}{WLC_{ox}}\frac{g_m^2}{f}$, where K is a flicker noise constant, W is the transistor width, L is the channel length, and C_{ox} is the gate oxide capacitance of the MOSFET. The total input-referred voltage noise PSD of the telescopic op amp is

$$\overline{V_{in,n}^2}(f) = \frac{16kT}{3}\left(\frac{1}{g_{m4,5}} + \frac{g_{m15,16}}{g_{m4,5}^2}\right) + \frac{2K_p}{(WL)_{4,5}C_{ox}}\frac{1}{f} + \frac{2K_n}{(WL)_{15,16}C_{ox}}\frac{1}{f}\frac{g_{m15,16}^2}{g_{m4,5}^2}. \quad (3.17)$$

The calculated value of $\overline{V_{in,n}^2}$ is 54.4 pV^2/Hz at 1 Hz and the thermal noise floor is 0.4 fV^2/Hz.

Fig. 3.5 shows the simulated input-referred noise voltage PSD of the telescopic cascode amplifier. The total integrated input-referred noise voltage of the system is 28.1 μV$_{rms}$ over a frequency range of 10 Hz to 10 kHz.

Fig. 3.5: Input-referred noise voltage PSD of the telescopic cascode amplifier.

Table 3.2 gives the performance comparison of the system specifications, designed values, and the simulation results of the telescopic cascode amplifier.

Parameters	Specifications	Designed values	Simulation results	Conditions
DC gain	>66 dB	80.9 dB	82.4 dB	-
3 dB bandwidth	>2 kHz	5.8 kHz	3.6 kHz	C_{load}=300 fF
Unity-gain bandwidth	>4.5 MHz	64.2 MHz	44.2 MHz	C_{load}=300 fF
Power/channel	<150 μW	90 μW	87.1 μW	-
Slew rate	> $\pm$0.5 V/μs	$\pm$10 V/μs	$\pm$9.7 V/μs	C_{load}=2 pF
Input noise voltage	-	19.5 μV$_{rms}$	28.1 μV$_{rms}$	10 Hz – 10 kHz
Input noise current	-	-	9.6 pA$_{rms}$	10 Hz – 10 kHz
Phase margin	>45°	-	61°	C_{load}=300 fF

Table 3.2: Op amp design specifications and simulated results.

3.2 Comparator Design

A comparator is a relational electronic circuit that is used to compare the input signal to a reference voltage. For this application, the comparator is used to compare the integrator output signal with a nominal reference voltage of 900 mV. This output is digitized using a flip-flop running at 100 kHz system clock. The comparator should be fast enough so that its output settles down within a required tolerance band before the next edge of the clock.

From the given specifications for an N-bit IDC resolution, the smallest voltage V_{min} that the comparator must resolve is given by $V_{FS}/2^N$. For our sensor application, using a 10-bit IDC and a full scale voltage of 1.8 V, V_{min} should be 1.76 mV. This comparator drives a standard cell flip-flop having an input logic high voltage V_{IH} of 1.17 V and an input logic low voltage V_{IL} of 0.63 V. From this data, the minimum gain $A_{v,min}$ of the comparator is given by

$$A_{v,min} = \frac{V_{IH} - V_{IL}}{V_{min}}. \tag{3.18}$$

The minimum value of the comparator gain required to resolve 1.76 mV is calculated to be 300 V/V (50 dB). To find the bandwidth of the comparator, we assume the comparator output $V_o(t)$ exhibits a single-pole response given by

$$V_o(t) = V_F(1 - e^{-t/\tau}), \tag{3.19}$$

where V_F is the steady-state voltage and τ is the time constant of the comparator.

The comparator output must reach the input threshold levels of the flip-flop before the next clock edge. Assuming a 0.5 LSB gain error for 10-bit resolution and that comparator output reaches V_{IH} or V_{IL} of flip-flop in 5 μs (half the clock period), the value of τ can be

found from (3.19) which gives τ=0.66 μs. Since the time constant of the first order system is given by equation $\tau = 1/(2\pi f_{3dB})$, the calculated minimum value of the comparator 3 dB bandwidth is 250 kHz.

In practical comparators, the output does not change instantaneously as the input level is switched. Rather, there is some propagation delay in the output which can be modeled as [34]:

$$t_p = \tau_c \ ln\left(\frac{2k}{2k-1}\right), \tag{3.20}$$

where t_p is the comparator propagation delay, τ_c is the time constant, and k is defined as:

$$k = \frac{V_{in}}{V_{in,min}}, \tag{3.21}$$

where V_{in} is the input voltage applied to comparator. A minimum input voltage will give the worst comparator delay. Therefore, to calculate worst delay of the comparator, V_{in} should be equal to $V_{in,min}$, which gives k=1. The maximum propagation delay of the comparator calculated from (3.20) is 450 ns.

The circuit schematic of the designed comparator is shown in Fig. 3.6 and the transistor dimensions are provided in Table 3.3. The comparator is designed to have a dc gain of 590 V/V (55.4 dB), which is sufficient to resolve the minimum input level. A buffer with minimum length devices is also used to provide extra gain and reduce the comparator loading. For the bandwidth calculation, using a nominal load of 6.93 fF from the buffer input, and output resistance of 81.2 MΩ, the value of 3 dB bandwidth of the comparator is calculated from $1/(2\pi R_{out}C_L)$ expression, which gives 280 kHz bandwidth.

Fig. 3.6: Circuit diagram of the comparator used in the IDC.

Transistor	Width (μm)	Length (μm)
M1, M2	2	6.5
M3, M4	0.5	0.18
M5, M6	2	6.5
M7, M8	0.22	0.18
M9, M10	2	10

Table 3.3: Comparator device dimensions.

Fig. 3.7 gives the simulated ac response of the designed comparator, showing a dc gain of 55.4 dB and a 3 dB bandwidth of 280 kHz.

Fig. 3.7: Magnitude of comparator frequency response from input to V_o.

The simulated transient response of the comparator is shown in Fig. 3.8, where the input signal with multiple voltage levels is compared with V_{ref} under stressed conditions (input signal period of 10 μs and voltage resolution of less than 0.5 V$_{LSB}$). The output binary signal follows the input signal relative to the reference voltage, resulting in one and zero as the input goes above and below the reference voltage, respectively.

Fig. 3.8: Transient response of the comparator.

The simulated performance and design specifications of the comparator are summarized in Table 3.4.

Parameters	Specifications	Designed values	Simulation results
DC gain (dB)	>50	55.4	55.4
Small signal 3 dB bandwidth (kHz)	>250	280	280
Power consumption (μW)	min.	1.8	1.8
Minimum resolution (mV)	<1.8	0.9	0.6
Propagation delay (ns)	-	450	394.5

Table 3.4: Comparator design specifications and performance.

3.3 DC Reference Current Source Design

The dc current sources are an integral part of the SVFC converters, as these add and remove the charge from the integrator input to keep the integrator output within the saturation limit. To provide a variable sensor dynamic range, a programmable cascode current mirror has been designed to generate 50 nA, 200 nA, and 1 μA dc currents.

Fig. 3.9: DC reference current sources I1, I2, and I3.

Fig. 3.9 shows the dc current source circuit used for the charge injection and removal from the integrator. Current sources I1, I2, and I3 are switched on depending on the current measurement range selected for the sensor. The switches S1, S2, and S3 correspond to the current sources I1, I2, and I3 respectively, which can be controlled to generate 50 nA, 200

nA, and 1 μA of currents to provide flexibility. Switches S4 and S5 are used to implement the current steering to reduce the effects of switching transients at the integrator input. The transistor level schematic of the current sources used in the sensor is shown in Fig. 3.10, where the output node A is connected to the inverting input of the integrator.

Fig. 3.10: Cascode current mirror circuit design.

The device dimensions are given in Table 3.5.

Transistor	Width (μm)	Length (μm)
M1, M2, M5, M6	1.5	40
M3, M7	6	40
M4, M8	30	40
M9, M10, M11, M12, M25	0.22	0.18
M13, M14, M15, M16, M26	0.22	0.18
M17, M18, M21, M22	1.1	100
M19, M23	4	100
M20, M24	20	100

Table 3.5: Cascode current mirror dimensions.

Due to the spice model limitation of the maximum length of the MOSFET, the transistors having lengths greater than 20 μm are built by series stacking and shorting the gates. An example of transistors M24 (NMOS) and M4 (PMOS) is illustrated in Fig. 3.11 (a) and Fig. 3.11 (b), respectively.

Fig. 3.11: Transistor channel length (a) NMOS (b) PMOS.

3.4 Non-overlapping Clock Generator

As discussed earlier, an op amp input offset correction technique which stores the offset voltage during the reset period and subtracts it from the op amp input during the following period has been implemented. The switched-capacitor circuit designed to implement this offset correction scheme requires a two-phase non-overlapping clock. A non-overlapping clock generator is often used in switched capacitor circuits where the order of switching is critical for proper operation of the circuit. Any two complementary switches on at the same time might result in charge loss.

In Fig. 2.10, the non-overlapping clocks $\varphi_1(t)$ and $\varphi_2(t)$ are used to switch the offset storage capacitor $C2$. Various non-overlapping clock generators are available [35], and we have selected a NOR based clock generator, as shown in Fig. 3.12.

Fig. 3.12: NOR gate implementation of non-overlapping clock generator.

The clock signal $\varphi(t)$ in phase with input sine signal is fed to the clock generator, producing two non-overlapping signals $\varphi_1(t)$ and $\varphi_2(t)$, as shown in Fig. 3.12. If the delay between these clocks is made very large relative to the clock period, then this would reduce the time available for settling during the integration phase. Considering this, the design

64

consists of three buffers resulting in a non-overlapping clock delay of 250 ps, as shown in Fig. 3.13.

Fig. 3.13: Non-overlapping clock waveforms: (a) Rising edge delay (b) Falling edge delay.

Table 3.6 gives the simulation results of the non-overlapping delay of the clock generator over all possible corners.

Corner	Rising edge delay (ps)	Falling edge delay (ps)
TT	249.8	256.6
SS	311.3	318.1
FF	201.5	208.8
SF	244.7	253.3
FS	256.5	261.8

Table 3.6: Simulated non-overlapping clock interval for all corners at standard 1.8 V supply voltage and 27°C temperature.

3.5 16-bit Bi-directional Counter Design

To convert the analog integrator output to a digital signal, a counter is required in order to count the flip-flop pulses at the comparator output. The counter counts up and down when the flip-flop output Q is '1' (I_{ref1} is on) and '0' (I_{ref2} is on), respectively. The total up and down counts, multiplied by the clock period, give the total time for which I_{ref1} and I_{ref2} are on. The total input charge added and removed can be calculated by multiplying the the known dc reference currents by the total time for which they are on. Therefore, a bidirectional T-flip-flop based counter is designed to meet the system requirements. A block diagram of a single stage of the counter is shown in Fig. 3.14.

Fig. 3.14: Single stage of the 16-bit counter.

In Fig. 3.14, when *enable* is high, Q starts to toggle with a frequency $f_{clk}/2$, giving the LSB Q_0 of the counter (where f_{clk} is the clock frequency). Signal *up/down* is driven by the flip-flop output which toggles high and low when the integrator output goes above or below the comparator reference voltage, respectively. The residue digital signal goes to the next stage and the bit Q_1 toggles with frequency $f_{clk}/4$, and so on.

3.6 Parallel-to-Serial Converter

Digitized real and imaginary parts of the cellular impedance are given by a 16-bit counter as described in the previous section. To reduce the number of I/O pads required for data extraction, the IDC counter bits need to be serialized so that the data can be transmitted off-chip using a single pin per channel. A MUX based parallel-to-serial converter is designed, as shown in Fig. 3.15.

Fig. 3.15: Circuit for parallel to serial converter.

In this design, the 16-bits of the IDC counter are connected to the input lines of a 16×1 MUX, with address lines driven by a 4-bit counter. During the integration phase, the *enable* input is set to zero and the 16-bit counter keeps on performing analog to digital conversion. Since the 4-bit counter is disabled and a zero address line is selected, the MUX transmits the LSB data of the 16-bit counter. To extract the impedance components of the cellular sample at the end of the integration period, the enable pin needs to be high. The

16-bit counter is eventually disabled and a 4-bit up-counter increments the MUX address, transmitting the data bits of the IDC counter serially to the MUX output, as shown in Fig. 3.16. The *test mode* pin connects a high frequency *test clock* to the 4-bit counter, which can be used to send out the IDC counter data for debugging purposes.

Fig. 3.16: Parallel-to-serial converter waveforms.

3.7   Scan Chain

A scan chain of 112 D flip-flops (DFFs) has been used to set the digital control signals on the chip, as shown in Fig. 3.17. These flip-flops have a separate reset input and are clocked externally through an FPGA. A buffer has been added at the output of each flip-flop to increase the flip-flop hold time so that the digital data can be shifted reliably at each clock edge.

Fig. 3.17: Scan chain circuit.

An extra flip-flop has been added at the end of the scan chain with its output connected to the I/O pin, in order to debug the scan chain during the chip testing. A table showing the scan chain signal pins is included in Appendix C.

3.8   Simulation Results

3.8.1   Nyquist Response

A simplified test impedance model of the cell membrane (from Fig. 1.5) is used to carry out the impedance extraction using the IDC. The solution resistance of 500 kΩ, membrane capacitance of 2 nF, and membrane resistance of 10 MΩ is used to simulate the real and imaginary parts of the impedance over a frequency range of 400 Hz. The simulated values of the real and imaginary parts are plotted and the resulting Nyquist plot is shown in Fig. 3.18. From simulation, the rms error in the real and imaginary part of the extracted impedance is 0.85% and 0.88%, respectively.

Fig. 3.18: IDC Nyquist plot of the simulated values.

3.8.2 Offset Correction

Fig. 3.19 shows the simulated output of a 7-bit IDC with and without the offset correction
circuit enabled for a 5 mV input offset voltage of the op amp.

Fig. 3.19: IDC output waveforms with and without offset correction.

Chapter 4

Experimental Results

The impedance sensor chip has been fabricated in a 1.8 V 0.18 μm CMOS technology and is shown in Fig. 4.1. The total chip area is 1.8 mm×1.5 mm. There are four independent IDC channels to extract the impedance data in parallel. A working electrode array and counter electrode are fabricated on chip to permit deposition and measurement of living cells on the surface of the chip. In the future, these electrodes will be plated with gold through a post-processing step to enable cell interfacing and electrolyte exposure.

Fig. 4.2 shows the circuit blocks in each channel of the IDC including the op amp integrator, comparator, adjustable capacitor bank, digital bidirectional counter, and programmable dc current sources. The electrical characterization of the fabricated chip is covered in this chapter under standard conditions. Chip testing using biological samples is beyond the scope of this thesis and will occur in the future.

Fig. 4.1: Photograph of the fabricated chip.

Fig. 4.2: IDC channel components

4.1 Experimental Setup

To permit electronic testing and characterization, the fabricated impedance sensor array chip is placed on a custom designed PCB (schematic in Appendix A) which is interfaced with a function generator and an FPGA to provide the analog and digital control signals. The scan chain on the chip is clocked by the FPGA and digital input data is provided at each clock edge. The chip also needs sine and cosine signals, which are used to generate the φ signal on the chip, required for real and imaginary part extraction, respectively. These signals are provided from the test board. The impedance data from the chip is collected by an FPGA and sent to a PC via a USB connection. The FPGA and USB hardware are built on a separate PCB manufactured by Opal Kelly (XEM-6010) [36]. A block diagram showing the test setup of the system is given in Fig. 4.3.

Fig. 4.3: Block diagram of the IDC chip test setup.

Static testing is useful for characterizing an IDC and provides information about gain error, offset error, differential nonlinearity (DNL), and integral nonlinearity (INL) of the system. To test the IDC for one input period at a 12-bit nominal resolution and 100 kHz clock rate, an input signal frequency of 12.2 Hz is required, where only half of the input period is utilized for impedance extraction. The input dc current sources I_{ref1} and I_{ref2} are both set to 50 nA, which is the maximum input current that saturates the integrator with a 2 pF feedback capacitor at a clock frequency of 100 kHz. Fig. 4.4 shows the measured oscilloscope waveforms of the IDC for one input period.

Fig. 4.4: IDC oscilloscope waveforms.

In the figure, waveform (a) is an input ac voltage signal with an amplitude and frequency of 10 mV$_{pk}$ and 390.6 Hz, respectively, applied across a 200 kΩ resistor on the test PCB. Waveform (b) is the corresponding φ signal and (c) shows the integrator output in the first and second half of the input period. Waveform (d) is the flip-flop output Q which controls the input dc current sources.

4.1.1 Amplitude Linearity of Impedance Sensor

To find the linear amplitude range of the impedance sensor chip, a low frequency ac voltage signal is applied across a known resistance on the test PCB and its amplitude is varied to generate the desired range of input test currents. Due to the wide range of input test currents required and limitations of the voltage source, three resistors are used to generate the current. Table 4.1 shows the resistors used and the range of currents generated.

Resistance (MΩ)	$V_{in,min}$ (mV)	$V_{in,max}$ (mV)	$I_{in,min}$	$I_{in,max}$
1	10	200	10 nA	200 nA
200	10	1000	50 pA	5 nA
1100	2.5	50	2.3 pA	45.4 pA

Table 4.1: Input voltage and resistor values used to generate test currents.

For the test values given in Table 4.1, the IDC real counts from the chip are plotted against the input test current for each channel. Fig. 4.5 shows the linear range of the impedance sensor system at 12.2 Hz after the manual offset correction. As shown in the figure, the input current is swept from 2.3 pA to 200 nA. The IDC counts increase linearly for 50 pA to 60 nA of input test current which gives the linear range of the IDC. The response of all four channels is similar within the linear range. A nonlinear IDC response is observed at small input currents because the input signal is difficult to distinguish from noise. This sets the limit to the minimum current level that can be reliably detected by the impedance sensor.

75

Fig. 4.5: Linear range of IDC channels.

4.1.2 Differential Nonlinearity Error

The differential nonlinearity (DNL) error is the difference between an actual step width for an ADC and the ideal value of 1 LSB [37]. DNL is defined as:

$$DNL = \frac{I_{i+1} - I_i}{I_{LSB}} - 1, \tag{4.1}$$

where I_i is the current at the ith code and $0 < i < 2^N - 1$. If the step width is exactly 1 LSB, then the DNL will be zero. The IDC static test setup is different from the conventional ADC setup which requires a linear ramp input to plot the DNL. Our sensor application needs an ac input signal to measure the impedance at the end of the input period. The

76

measurements are carried out at a nominal frequency of 12.2 Hz and the DNL response of all four IDC channels is shown in Fig. 4.6. For the input currents smaller than 5 nA, the maximum DNL is around 1 LSB. Whereas for currents greater than 5 nA, the maximum DNL after data interpolation of 40 LSB step width is 0.4 LSB.

Fig. 4.6: Differential nonlinearity error of the IDC channels.

4.1.3 Integral Nonlinearity Error

The integral nonlinearity (INL) error is the deviation of the values on the actual transfer function from a straight line [37]. This straight line is the best fit line of the actual curve so as to minimize the deviations. INL is defined as:

$$INL = \frac{I_i - I_0}{I_{LSB}} - i, \tag{4.2}$$

where I_0 is the current at the first code and $0 < i < 2^N - 1$. The INL of all four IDC channels is shown in Fig. 4.7. From the plot, the maximum INL ranges from -5 LSB to 2.5 LSB for a 12-bit resolution.

Fig. 4.7: Integral nonlinearity error of the IDC channels.

4.1.4 Phase Linearity of Impedance Sensor

To determine the phase response of the impedance sensor, the input current amplitude and frequency is kept constant, and its phase is varied from $-180°$ to $+180°$ with respect to the sine and cosine multiplying signals. Using an input current amplitude of 20 nA and frequency of 12.2 Hz, the normalized real and imaginary IDC counts are plotted against the input phase as shown in Fig. 4.8.

Fig. 4.8: Phase response of IDC channel 4.

The measured results are observed to fit the theoretical curve very well with an rms error of 0.41% and 0.73% for the real and imaginary parts, respectively. The Nyquist plot of the measured and theoretical values is shown in Fig. 4.9.

Fig. 4.9: Nyquist plot of the IDC for variable input phase.

4.1.5 Frequency Response

Measurement at multiple input frequencies is required by the EIS. Therefore, known test currents of 20 nA and 40 nA are generated from 500 kΩ and 250 kΩ resistors, respectively, with a 10 mV amplitude input signal. To get the frequency response magnitude of the sensor system, the input signal frequency is swept from 10 Hz to 6 kHz and the impedance is measured at each frequency. Plots of the extracted impedance against input frequency are shown in Fig. 4.10 for each IDC channel. The input terminal of the integrator is given by $-V_o/A_o$, where V_o is the integrator output voltage and A_o is the open loop gain of the op amp. Due to the op amp bandwidth limitation as the input signal frequency increases, a decrease in A_o causes the inverting terminal voltage to drop. This increases the input current and as a result, the IDC counts decrease. This causes the impedance to roll up,

as shown in the figure. The ripples in the measured impedance are due to the phase error of the integrator. The plot shown in Fig. 4.10 (c) dips down at higher frequencies due to the mismatch in the input dc current sources. The frequency response of the IDC system also depends on the input resistance as this determines the unity-gain bandwidth of the closed-loop response, whose value is 320 kHz and 160 kHz for 250 kΩ and 500 kΩ resistance, respectively. The frequency range of impedance extraction can be increased by increasing the 3 dB bandwidth of the integrator op amp.

Fig. 4.10: IDC frequency response of (a) channel 1, (b) channel 2, (c) channel 3, and (d) channel 4.

4.1.6 Signal-to-Noise Ratio and Dynamic Range

Noise limits the minimum current detection limit of any measurement system. When a known input current is applied to the IDC multiple times, the IDC output varies due to noise in the system. This response can be characterized by plotting the standard deviation (σ) of the IDC output for known input currents. For this test, the input current is swept from 2.3 pA to 200 nA and 20 samples of each current are taken. The standard deviation of the IDC output provides a measure of the system noise. Fig. 4.11 (a) and 4.11 (b) give plots of the noise against the input test current.

Fig. 4.11: Measured noise of the IDC channel output.

It is observed from the graph that the maximum standard deviation (in counts) is 9 for the desired input current range. This can be used to determine the SNR of the system, shown in Fig. 4.12, as follows:

$$SNR = \frac{\mu^2}{\sigma^2},\qquad(4.3)$$
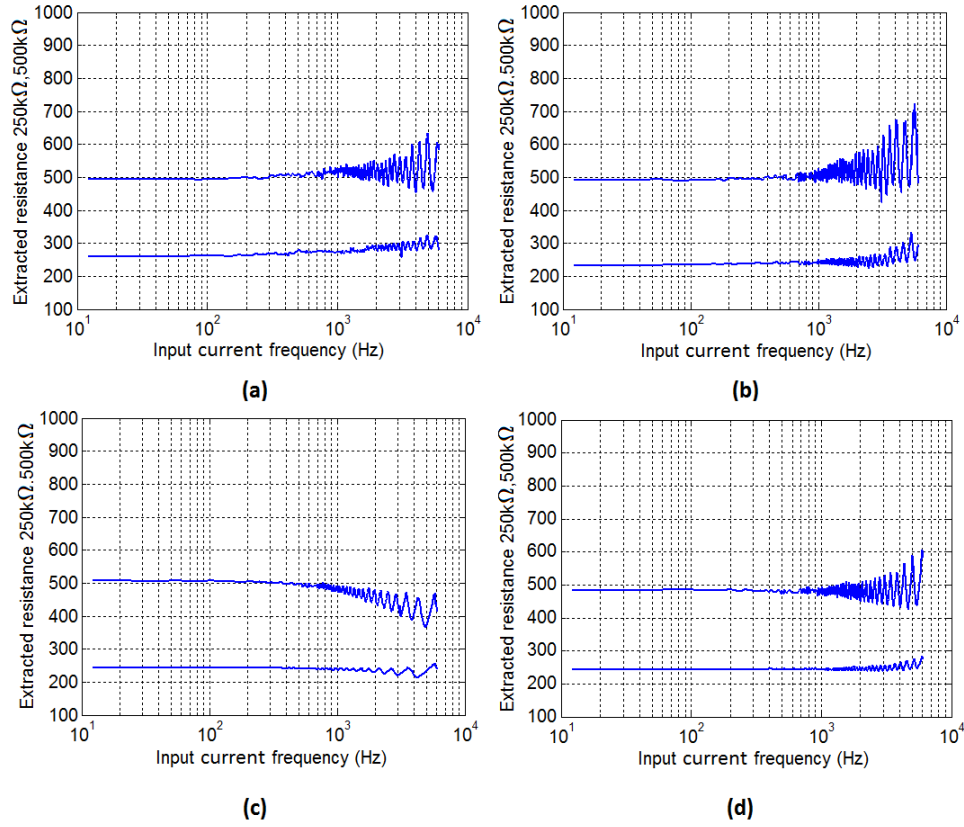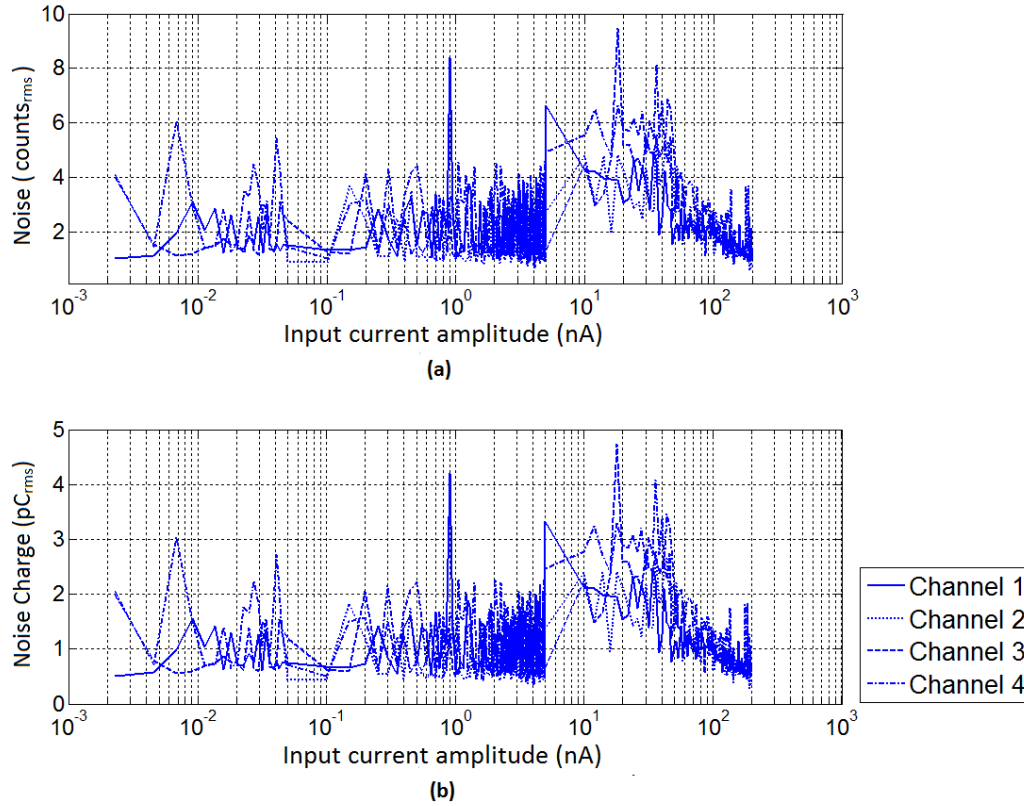
where μ is the mean value of the IDC output count at each input test current. From the plot, the SNR of IDC channels increases from 0.01 to 5×10^7 as the input current is increased from 2.3 pA to 200 nA. The limit of detection of the IDC is the value of the input current when the SNR=3. From the SNR plots, the limit of detection of the IDC channels 1, 2, 3, and 4 is 46.12 pA, 46.95 pA, 53.66 pA, and 42.45 pA, respectively. The maximum measured input current from Fig. 4.5 (b) is 60 nA. This gives us the dynamic range of our system which is 62 dB.
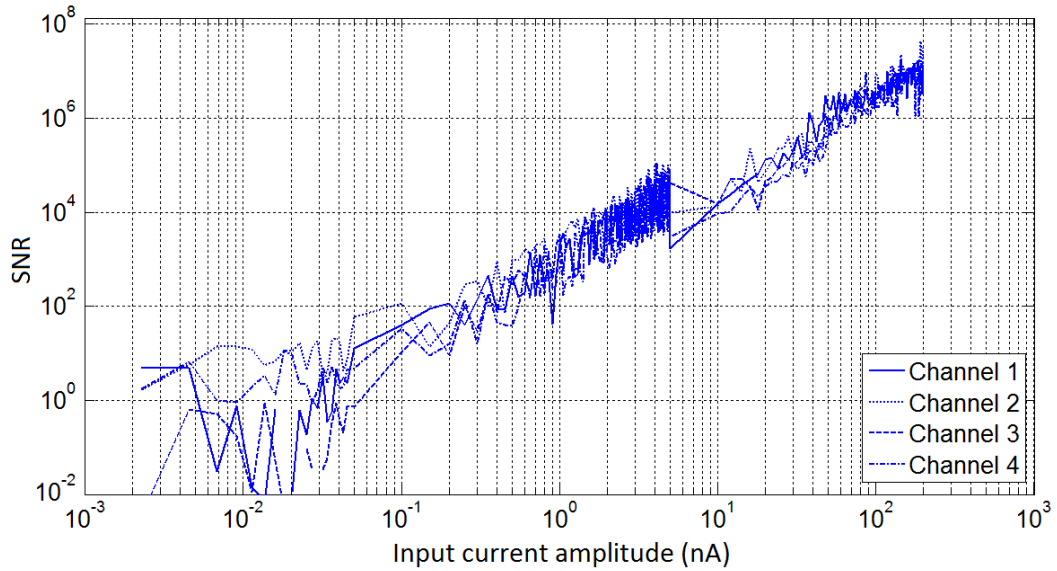
Fig. 4.12: SNR of the IDC channels.

4.1.7 Nyquist Plot

The Nyquist plot shows how the real and imaginary parts of a complex impedance are related over a range of frequencies. To test the impedance sensor, an equivalent passive cell membrane model (shown in Fig. 1.5) is used to generate a known test current on the PCB board, which is to be measured by the sensor. Values of the passive components used for testing are R_s=500 kΩ, R_m=10 MΩ, and C_m=2 nF. The input frequency is swept from 0.7625 Hz to 400 Hz. When the value of *select* signal is '0' and '1', real and imaginary part of the impedance is extracted for the given range of frequencies. The Nyquist plot of the measured impedance is shown in Fig. 4.13.
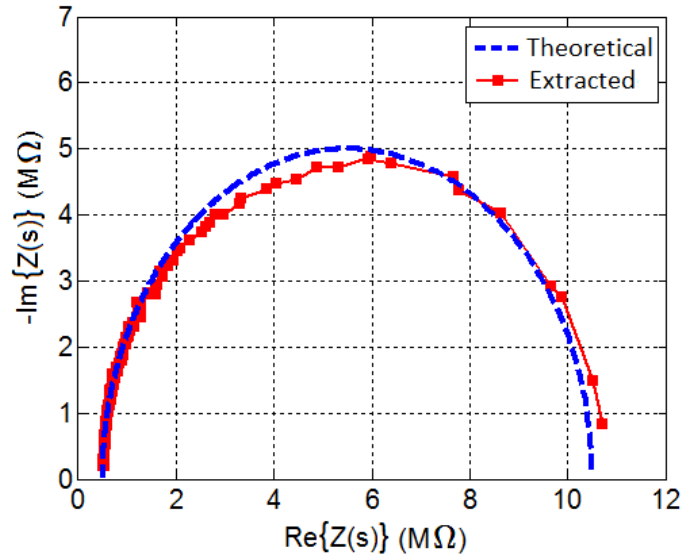
Fig. 4.13: Nyquist plot of the ideal and extracted test impedance where R_s=500 kΩ, R_m=10 MΩ, and C_m=2 nF.

From the measured results, the rms error in the real and imaginary part of the extracted impedance is 0.45% and 0.88%, respectively. The Nyquist plot however only gives infor-

mation about the real and imaginary parts but does not explain the frequency response of the extracted impedance. Therefore, the impedance magnitude and phase extracted from the chip is plotted against the input frequency as shown in Fig. 4.14. At low frequencies the equivalent impedance is 10.5 MΩ (capacitor is modeled as an open circuit). Whereas at high frequencies the capacitor can be modeled as a short circuit and the effect of R_m can be ignored. Therefore, the equivalent impedance is equal to 500 kΩ.
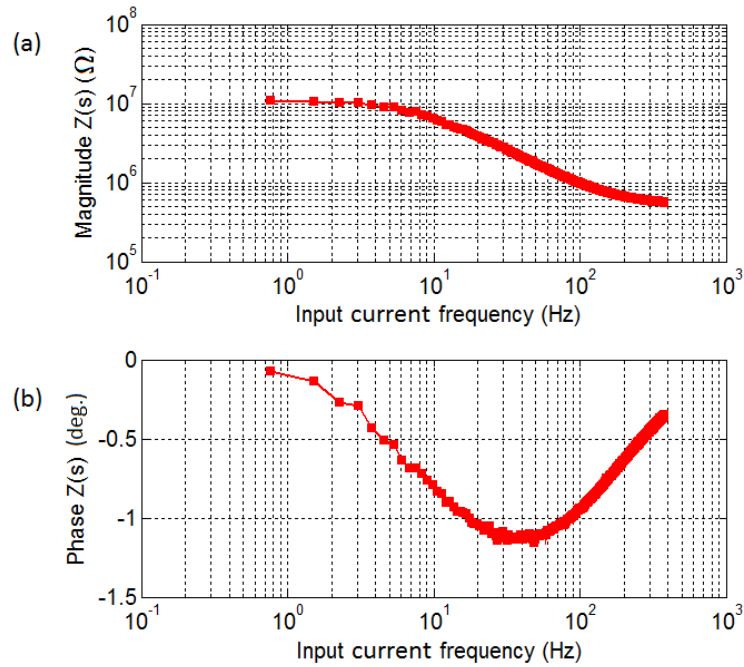

Fig. 4.14: Extracted impedance: (a) Magnitude (b) Phase.

4.1.8   Op Amp Input Offset Correction

As discussed earlier, we are implementing the offset correction by storing the input offset voltage of the op amp on the capacitor in one input period and correcting in the next period. The input frequency is swept from 10 Hz to 6 kHz, and 500 kΩ resistance is extracted with

the offset correction circuit turned on. Fig. 4.15 shows the extracted impedance plot against the input frequency. The resistance value is affected by the switching transients which makes it difficult to extract the test resistance accurately.
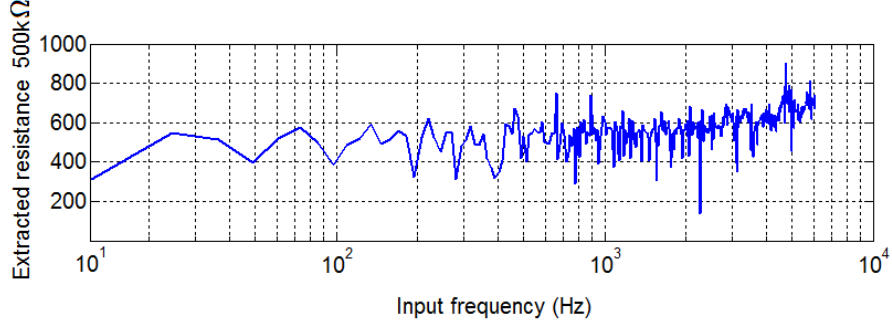
Fig. 4.15: Extracted impedance value with offset correction circuit enabled.

4.2 Comparison of the IDC channels

Table 4.2 gives the performance comparison of the IDC channels.

Parameters	Ch. 1	Ch. 2	Ch. 3	Ch. 4	Conditions
Dynamic range (dB)	62	66	62	62	f_{in}=12.2 Hz
Max. DNL (LSB)	0.46	0.43	0.43	0.44	f_{in}=12.2 Hz, I_{in} >5 nA
Max. INL (LSB)	5	4	4	3	f_{in}=12.2 Hz
3 dB bandwidth (kHz)	5	5.2	5	6	R=250 kΩ, 500 kΩ
Output noise charge (pC$_{rms}$)	4.2	2.8	4.7	4	-
Limit of detection (pA$_{peak}$)	46.1	46.9	53.7	42.4	SNR=3

Table 4.2: Performance comparison of the IDC channels.

86

Table 4.3 below provides a comparison between our impedance sensor array and Yang's design [1].

Parameters	Yang [1]	Our work
Technology	0.5 μm CMOS	0.18 μm CMOS
Supply voltage (V)	3	1.8
Chip size (mm^2)	3×3	1.8×1.5
On-chip WE array size	N/A	8×6
Power/channel (μW)	6	94
Dynamic range (dB)	50 (8-bit)	62 (10-bit)
3 dB measured bandwidth	100 Hz	5 kHz
Linear sensitivity	400 pA (f$_{in}$=1 Hz)	42 pA (f$_{in}$=12.2 Hz)
Integrator op amp offset correction	No	Yes

Table 4.3: Performance comparison with Yang [1].

Chapter 5

Conclusion

A low frequency impedance sensor design was presented in this thesis that can be programmed to measure input currents from 50 pA up to 1 μA. The system is based on an SVFC architecture. An FRA algorithm based implementation was adopted to extract the real and imaginary parts of the cellular sample. The IDC was tested using a passive cellular model and the Nyquist plot of the extracted impedance was presented. The chip was designed, laid out, and fabricated in a 0.18 μm CMOS process.

The FRA implementation presented in the dissertation is novel in this area of research. Previously, this approach has been implemented using TIAs and mixers [7] which is completely an analog design and has a high power consumption. This approach has also been implemented using mixed signal components in which a flipping capacitor forms the basis of a multiplying integrator [1] required by the FRA. In this thesis, we have presented this approach in a unique way. We implemented the FRA algorithm by resetting the integrator during the first of the input period and then integrating in the next half. The chip results are reasonable and it can be used for testing live biological samples.

APPENDICES

Appendix A

PCB Design

To test the impedance sensor, a test board has been designed on a 4-layered PCB in Mentor Graphics Pads to provide the analog and digital signals required by the chip. Adjustable voltage regulators (rated at 500 mA) are used to provide 1.8 V to the core, dvdd and avdd rings of the chip. The dc bias voltage for the comparator, integrator, PMOS current source and NMOS current source is provided by a resistor followed by a unity gain buffer, so that the voltmeter does not load the resistor while measuring the voltage. The circuit for generating bias voltages for NMOS and PMOS current mirror is shown in Fig. A.1, where the bias voltage is set by changing the value of a variable resistor. The ceramic and tantalum capacitors are also used to filter out the high frequency noise from the bias voltage.

The chip needs sine and cosine signals to extract the real and imaginary parts. These signals can be provided from external function generator. The test board also has a dedicated DDS function generator (AD9854-ASTZ) which can generate the quadrature signals on the board. It is interfaced with FPGA to set the digital signals required to produce the
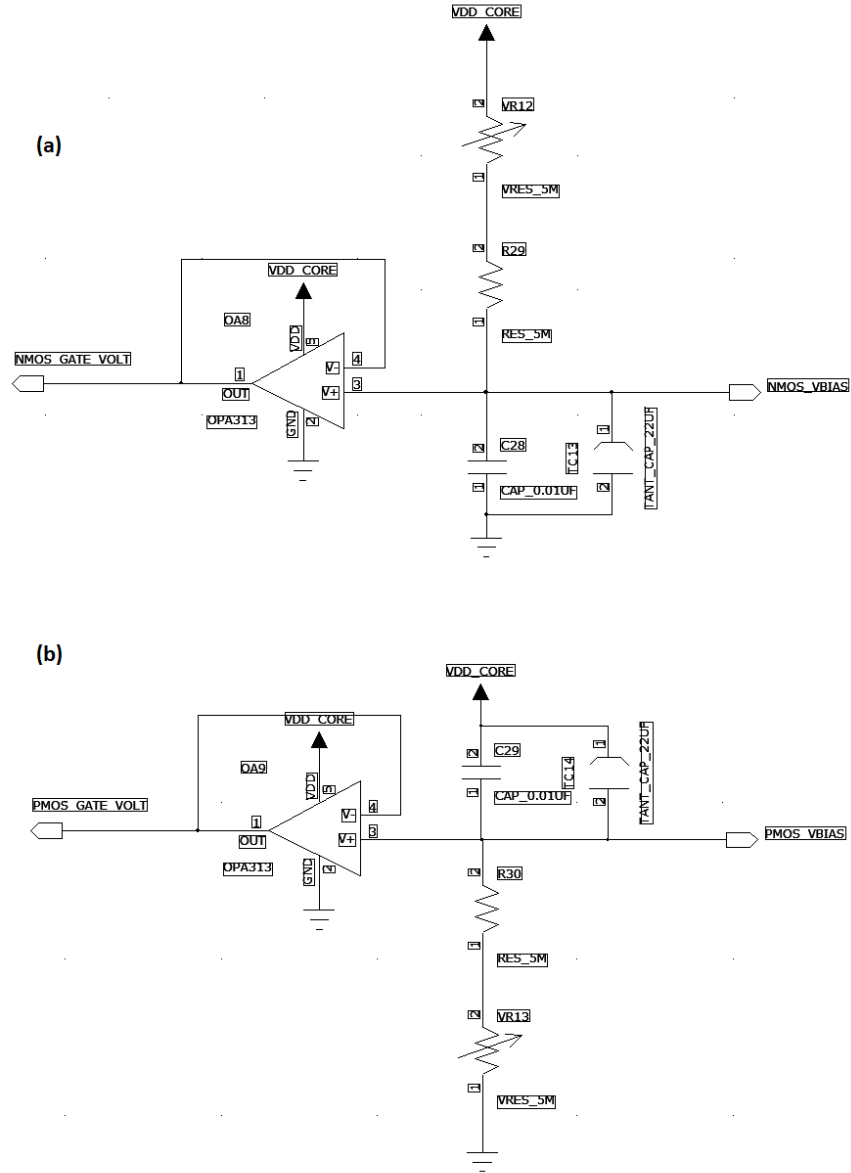
Fig. A.1: Circuit used to provide the bias voltages to the chip, (a) NMOS bias circuit (b) PMOS bias circuit.

sine and cosine waves. A test circuit has been designed to control the amplitude and dc level of the quadrature signals, shown in Fig. A.2. It also removes higher order harmonics from the DDS signals.

Fig. A.2: Circuit to control amplitude and dc level of quadrature signals.

An input buffer is used to minimize the loading on the DDS function generator, followed by a resistive divider network to change the ac signal amplitude. This signal passes through a low pass filter whose bandwidth is 20 kHz. At the non-inverting terminal of the op amp, there is another resistive divider network which is used to change the dc level of the sine/cosine signal.

To measure the dc currents I_{ref1} and I_{ref2} from the chip, a transimpedance amplifier is designed on the board, shown in Fig. A.3
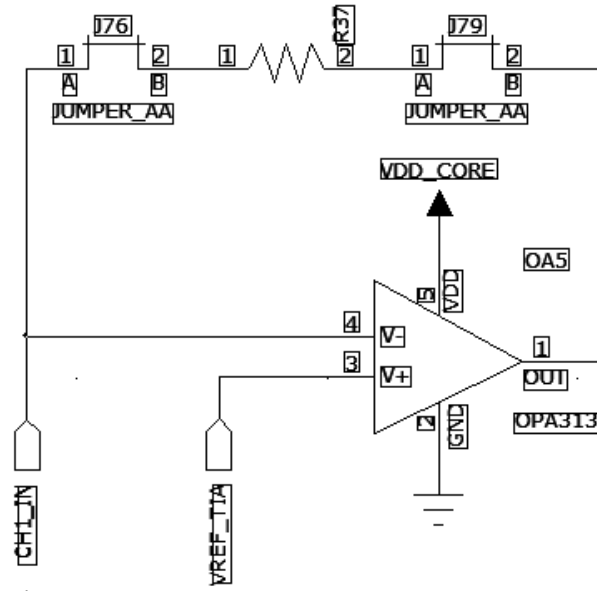
Fig. A.3: Transimpedance amplifier to measure chip currents.

Fig. A.4 shows the PCB schematic of the IDC system designed in Mentor Graphics Pads. Fig. A.5 shows the designed PCB board used for testing the impedance sensor system with Opal Kelly XEM-6010 FPGA installed on top of the board.
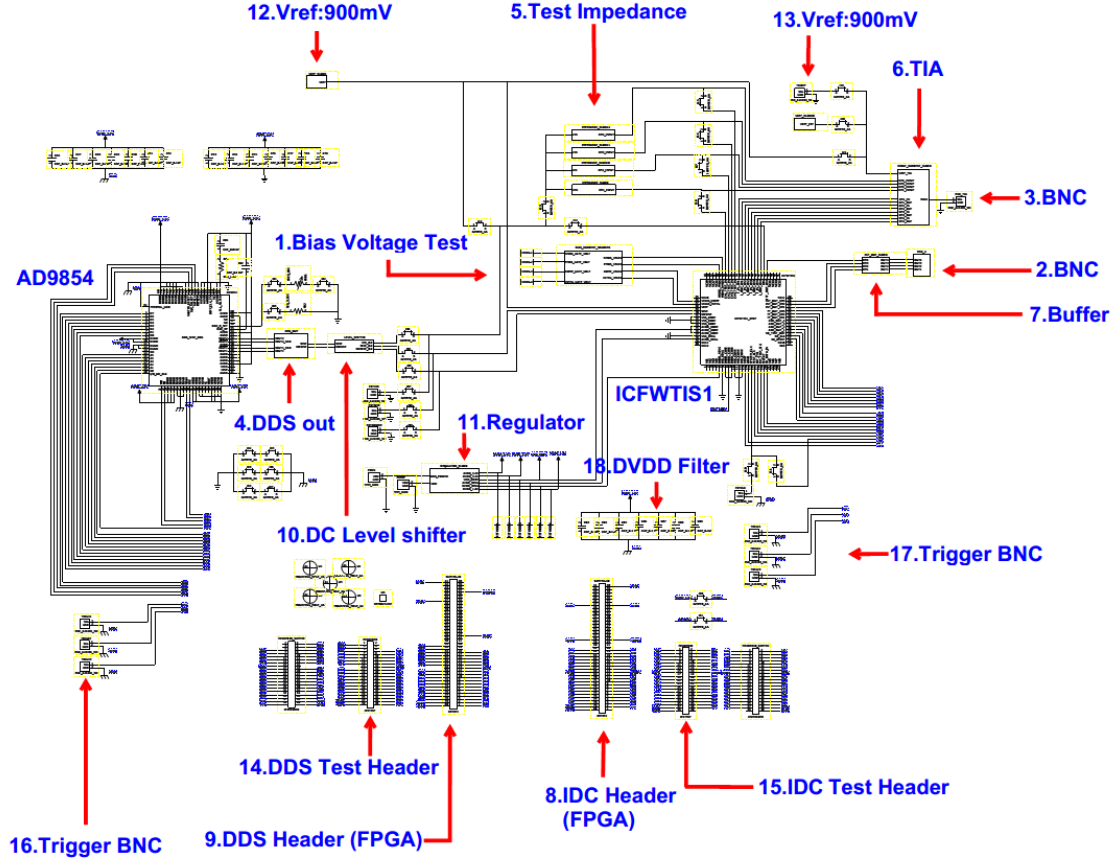
Fig. A.4: Test board schematic of the impedance sensor.
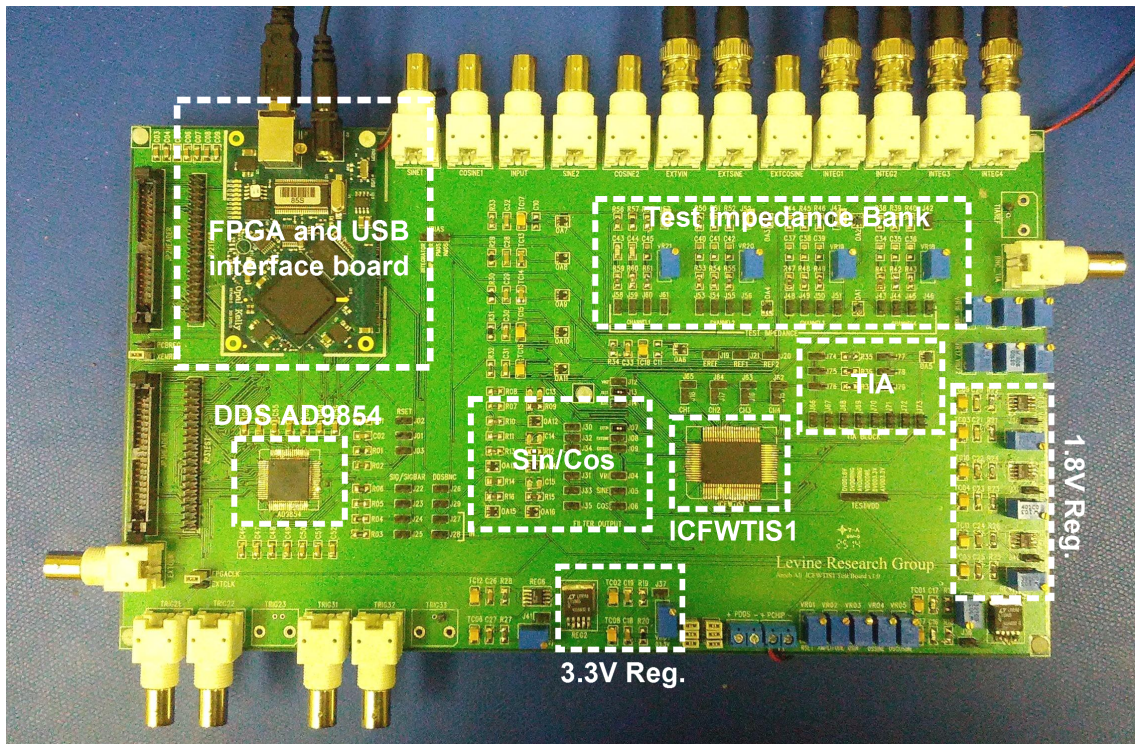
Fig. A.5: FR-4 PCB test board for the impedance sensor.

Appendix B

Chip Package and Bonding Diagram

CQFP-80 package is used for the IDC chip, Table B.1 gives the pin mapping of the chip, followed by a bonding diagram shown in Fig. B.1.

| Pin number	Chip pin	Pin number	Chip pin
1	NC	21	NC
2	NC	22	NC
3	NC	23	NC
4	NC	24	NC
5	VDD_ring	25	NC
6	VSS_ring	26	NC
7	DVDD_core	27	shift_reg_reset
8	DVDD_core	28	shift_reg_clk
9	DVDD_core	29	shift_reg_test_out
10	VSS_core	30	ADC_out_1
11	VSS_core	31	ADC_out_2
12	VSS_core	32	ADC_out_3
13	reset	33	ADC_out_4
14	load	34	ff_out_ch1
15	system_clock	35	ff_out_ch2
16	test_clock	36	ff_out_ch3
17	external_phi	37	int_out_ch1
18	integrator_test_signal	38	int_out_ch2
19	select	39	int_out_ch3
20	shift_reg_datain	40	NC

Table B.1: CQFP-80 pin mapping table (contd..)

Pin number	Chip pin	Pin number	Chip pin
41	NC	61	NC
42	NC	62	NC
43	NC	63	NC
44	NC	64	NC
45	int_out_ch4	65	NC
46	vin	66	vbias_comparator
47	i_out_ch4	67	vbias_integrator
48	i_in_ch4	68	vref
49	i_out_ch3	69	sine
50	i_in_ch3	70	cosine
51	i_out_ch2	71	VSS_core
52	i_in_ch2	72	VSS_core
53	i_out_ch1	73	VSS_core
54	i_in_ch1	74	AVDD_core
55	ch4_test_in	75	AVDD_core
56	ch3_test_in	76	AVDD_core
57	ch2_test_in	77	VSS_ring
58	ch1_test_in	78	VDD_ring
59	vbias_NMOS	79	NC
60	vbias_PMOS	80	NC

Table B.2: CQFP-80 pin mapping table.
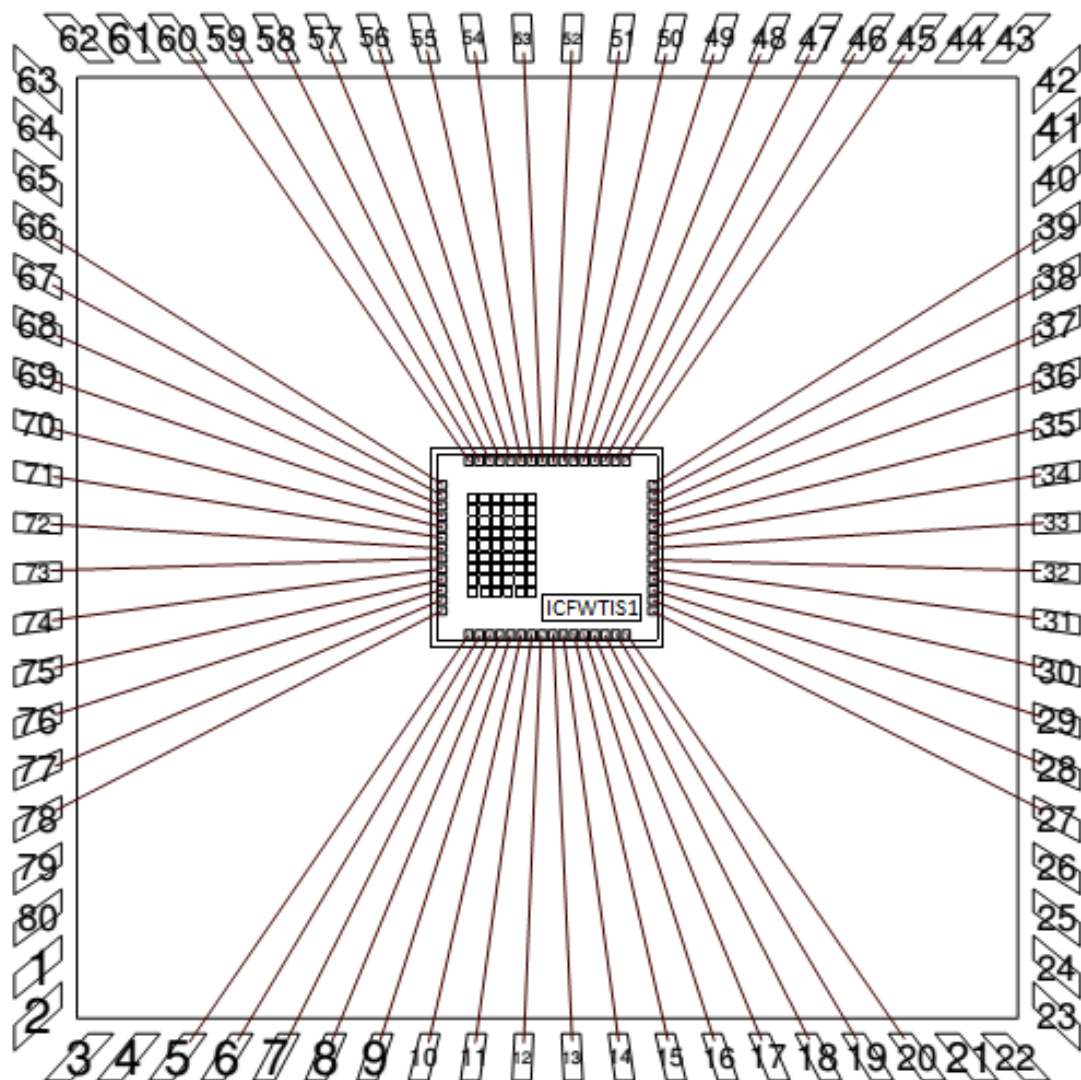
Fig. B.1: Bonding diagram of the sensor chip.

Appendix C

Scan Chain Control Signals

Scan chain bit	Symbol name	Description
Q0 (MSB)	cs_control_1	50 nA dc current source
Q1	cs_control_2	200 nA dc current source
Q2	cs_control_3	1 μA dc current source
Q3	cap_control_1	2 pF integrator capacitor
Q4	cap_control_2	2 pF integrator capacitor
Q5	cap_control_3	2 pF integrator capacitor
Q6	cap_control_4	2 pF integrator capacitor
Q7	calibration_control_up	Test PMOS current source
Q8	calibration_control_down	Test NMOS current source
Q9	control_integrator_output	Integrator output to external pin
Q10	test_control_counter	Set 16-bit counter to test mode
Q11	offset_control	Switch on/off offset correction
Q12	control_phi_external	Turns on external φ signal

Table C.1: Digital control signals of the scan chain (contd..)

Scan chain bit	Symbol name	Description
Q13	control_test_integrator	Integrator test mode
Q14	control_external_input	Enables test input from external pin
Q15-Q26	-	Channel 1 electrode enable
Q27-Q38	-	Channel 1 electrode V_{ref} enable
Q39-Q50	-	Channel 2 electrode enable
Q51-Q62	-	Channel 2 electrode V_{ref} enable
Q63-Q74	-	Channel 3 electrode enable
Q75-Q86	-	Channel 3 electrode V_{ref} enable
Q87-Q98	-	Channel 4 electrode enable
Q99-Q110	-	Channel 4 electrode V_{ref} enable
Q111 (LSB)	control_vin_CE	Enable V_{in} for CE
Q112	test_out	Test out

Table C.2: Digital control signals of the scan chain.

Circuit	Resistance
Telescopic Amplifier, R	57.3 kΩ
Comparator Circuit, R	1.2 MΩ
PMOS Current Source, R1	6.8 MΩ
NMOS Current Source, R2	8.8 MΩ

Table C.3: Biasing resistor values.

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