Modeling of a-Si:H TFT I-V Characteristics in the Forward Subthreshold Operation

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners. I understand that my thesis may be made electronically available to the public.

Abstract

The hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) are widely used as switching elements in LCD displays and large area matrix addressed senor arrays. In recent years, a-Si:H TFTs have been used as analog active components in OLED displays. However, a-Si:H TFTs exhibit a bias induced metastability. This problem causes both threshold voltage and subthreshold slope to shift with time when a gate bias is applied. These instabilities jeopardize the long-term performance of a-Si:H TFT circuits. Nevertheless a-Si:H TFTs show an exponential transfer characteristic in the subthreshold region. Moreover, the typical power consumptions for TFTs in the subthreshold region are in the order of nano-watts, thus making them suitable for low power design. For these reasons, a-Si:H TFT I-V characteristics in the forward subthreshold operation are investigated. First, we have derived the static and dynamic models of a-Si:H TFT in the forward subthreshold region. Second, we have verified our theoretical models with experimental results. Third, we have proven that a-Si:H TFT experiences no subthreshold slope degradation or threshold voltage shift in the forward subthreshold operation. Finally, we have studied a-Si:H TFT current mirror circuit applications. Measurements regarding the fidelity of current matching in the forward subthreshold region have been performed, and results are shown.

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Chapter 1

Introduction

Amorphous semiconductors were first studied in the 1950s and 1960s. The research work focused on structure disorder and its influence on the electronic properties. The semiconductor utilized was amorphous silicon (a-Si) without hydrogen. Due to high concentration of dangling bonds, unhydrogenated a-Si has a very high electron defects. The high defect density prevented a-Si from being used as a semiconductor. In 1969, Chittick et al. made the first hydrogenated amorphous silicon (a-Si:H), thereby reducing the dangling bonds of a-Si using hydrogen [1]. A few years later, Spear demonstrated the good transport properties of a-Si:H, which include a high photo conductivity, a high electrical conductivity, and a low defect density [2]. Then in 1976, the first a-Si:H p-n junction was invented [3]. In 1979, Le Comber et al. made the first a-Si:H thin film transistor (TFT) [4]. Finally, large area electronic arrays of a-Si:H devices were demonstrated by Snell in 1981 [5]. Since that date, many applications based on a-Si:H TFT technology such as liquid crystal displays, optical scanners, and radiation imagers have become available.

Compared to crystalline silicon (c-Si), a-Si:H possesses several major advantages: large-area deposition capability, low deposition temperatures, and standard fabrication processes. The maximum deposition area in c-Si technology is limited by the wafer size; currently it is approximately 12 inches. However, for a-Si:H, the current size of glass substrate is approximately 2 m by 2 m, and

in the case of roll-to-roll fabrication technology, a-Si can be deposited onto 2 km by 2 m roll made of the stainless steel or polymer foil. This capability results in a significant reduction in manufacturing costs. Low deposition temperature is another advantage of a-Si:H over c-Si. In c-Si technology, the fabrication temperature is approximately 900°C during the thermal oxidation process. The deposition temperature of a-Si:H is well below 450°C, so the use of low-cost glass substrates is possible. The current deposition technology of a-Si:H is pushing below 100°C that provides an opportunity for using flexible substrates such as plastic foils. Some of fabrication processes of a-Si:H is similar to those of c-Si. Therefore, certain equipment used in standard c-Si processes can easily be re-scaled for a-Si:H processes. As a result, these standard fabrication processes reduce capital costs.

Due to the capability of uniform deposition over a large substrate, a-Si:H technology is attractive in large area applications. The most appealing applications of a-Si:H technology are liquid crystal displays and, most recently, organic light emitting diode displays.

1.1 Liquid Crystal Displays

a-Si:H is extensively used in liquid crystal displays (LCDs). A liquid crystal is a material that possesses both properties of liquids and crystals; thus, it does not form a rigid body but appears as viscous liquid. The rod-shaped molecular structures of the liquid crystal contain strong dipoles and can be aligned by an applied electric field. LCDs use the liquid crystal's abilities to bend light. The polarized light enters the back of a liquid crystal pixel. The light passes through the liquid crystal, bending the light's polarization plane, which then passes through another polarizer. Ability of a liquid crystal media for transmitting and reflecting polarized light can be altered by the voltage applied across the liquid crystal pixel. Therefore, the pixels of LCDs are implemented so that the maximum transmission of light happens when there is no voltage applied, and the minimum

transmission, which is less than 1% of its peak intensity, occurs when the peak voltage is applied [6]. For color displays, each pixel is sub-divided into three sub-pixels, and color filters are deposited on top of each sub-pixel corresponding to the colours of red, green, and blue.

A display is made of an array of independently controlled pixels, and the number of pixels depends on the size and resolution of a particular display. Based on the addressing scheme of the pixels, LCDs can be divided into two categories: passive matrix and active matrix.

1.1.1 Passive Matrix LCD

The passive matrix LCD (PMLCD) consists of columns and rows of metal lines; the pixels are located at each intersection of these lines (Figure 1.1). Rows and columns can be driven only one at a time. Rows are driven sequentially, while columns determine which pixels are on and which are off based on image data. Pixels in different rows cannot be simultaneously addressed due to unintentional direct coupling, so the data is written row-by-row based on the row-at-once addressing scheme. Passive matrix schemes have some major design drawbacks. First, when the selected pixels are driven through by the primary signal voltage path, due to the row-at-once addressing scheme, the non-selected pixels can also be driven through due to an unwanted second signal voltage path, resulting in a kind of crosstalk. As a consequence, undesirable blurred images are produced. Second, since every pixel is addressed for only a fraction of the entire cycle time, the pixel is off for the remainder of the time and its voltage drops exponentially. Therefore, the pixel has to be driven at a higher voltage than the required to compensate the difference. The fluctuation in voltage produces a major challenge to passive matrix as it reduces the contrast and lifetime of the display. The performance degradation becomes worse as the number of rows increases. Thus, very large passive matrix displays are not feasible.

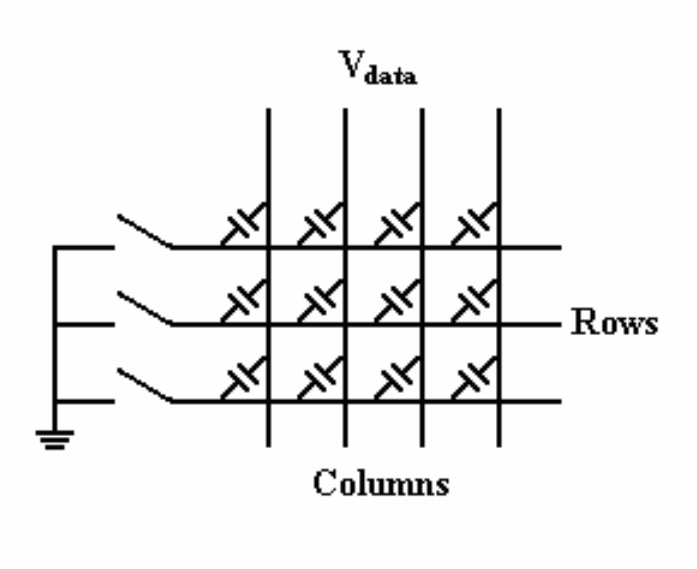


Figure 1.1. Schematic of pixel array of a PMLCD.

1.1.2 Active Matrix LCD

Figure 1.2 depicts the active matrix LCD (AMLCD) using a-Si:H TFT as the switching element to control the writing of the data to the pixel. After the data is written, the voltage is held at that level by a storage capacitor C_S, and is isolated from changes in the signal voltage. As a result, compared to the passive matrix, the active matrix has better brightness, longer lifetime, and sharper contrast. In addition, since the TFT needs less current to control the luminance of a pixel, the current in the AMLCD can be switched on and off more frequently, thereby improving the refresh rate of the display.

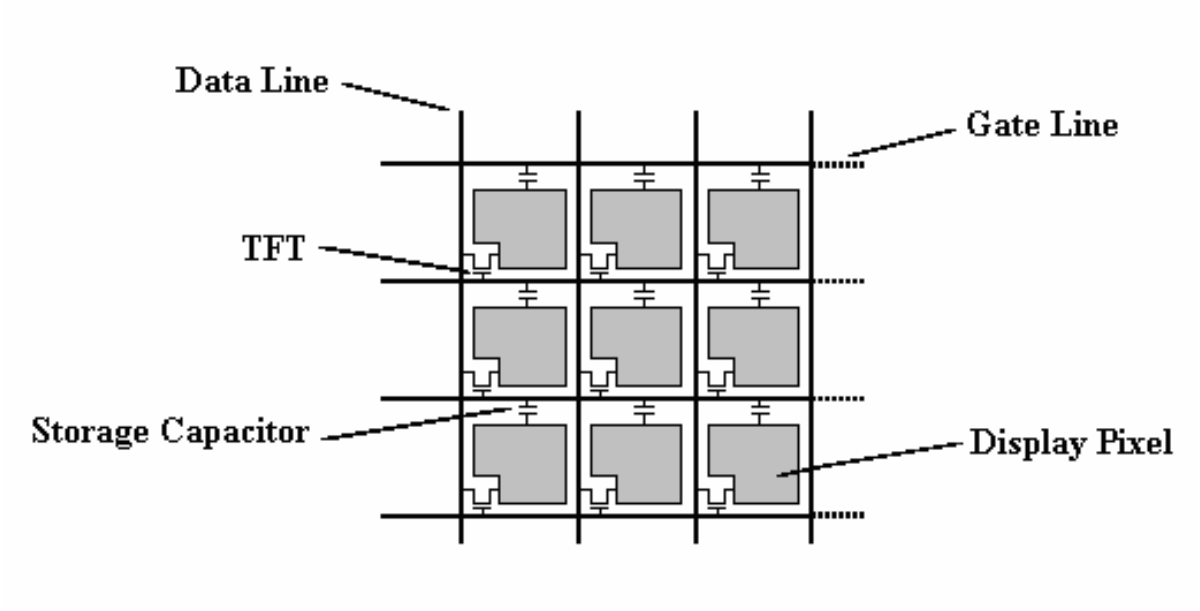


Figure 1.2. Schematic of pixel array of an AMLCD with TFTs used as switches.

1.2 Organic Light Emitting Diode Displays

Recently, a new emissive technology called organic light emitting diode (OLED) displays has been developed. In these displays, current is passed through a thin multi-layer organic material where it is converted into light. OLEDs require no backlighting, so they have high luminous efficiencies. They have also shown promise for brighter backgrounds, sharper images, better color quality, larger viewing angles, lower voltage (< 10V), and faster switching times (~ ns) [7]. OLED fabrication processes require fewer steps and have lower material costs than LCDs. Due to these advantages, OLED displays have the potential to replace LCDs and become the next dominant force in the flat panel display market. Similar to LCDs, OLED displays can be made in both active and passive matrix addressing schemes.

1.2.1 Passive Matrix OLED Display

In the array of the passive matrix OLED (PMOLED) display, electrically isolated row and column lines are arranged in a matrix. Figure 1.3 shows an external control view of a PMOLED display, where each OLED pixel is represented as an equivalent diode. PMOLED arrays use the same row-at-once addressing scheme as PMLCD arrays, where the data is written row by row to prevent unintentional direct coupling. Thus, PMOLED displays suffer similar problems to those of PMLCDs. PMOLED displays have another problem: while addressing any given pixel, a large number of non-addressed pixels become reverse biased. The long-term reverse bias causes an irreversible breakdown in OLEDs and has to be prevented by the use of a pulsed current source [8]. The selection time of each pixel decreases as the resolution of the display increases; thus, large current and high voltages for each pixel are required to achieve the desired average brightness level [9].

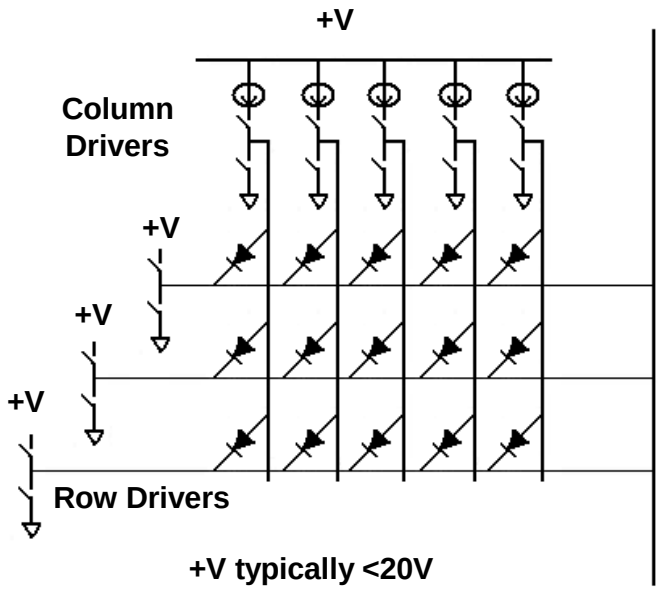


Figure 1.3. External control view of a PMOLED.

1.2.2 Active Matrix OLED Display

Similar to AMLCDs, the active matrix OLED (AMOLED) arrays use TFTs as active elements to isolate the OLED from the row and column select lines so each pixel is addressed separately. Hence, AMOLEDs avoid the problems found in PMOLEDs. Unlike AMLCDs where TFTs are used only as pixel switches, TFTs in AMOLED arrays are used both in switching and in the analog control of OLED current. When a pixel element is selected to be "ON," the information is sent to the pixel TFT, which sets the brightness of the pixel. The TFT then retains this information and continuously controls the current flowing through the OLED. Hence, the main advantage of AMOLED over PMOLED is that the OLED can be operated during the entire timeframe without the need for the large current to maintain the brightness level.

1.3 Motivation

a-Si:H TFTs are widely used in today's large area display applications such as AMLCDs. They are also used in AMOLED applications as switching devices and analog active components in the pixel circuits. However, a-Si:H TFTs show device characteristic degradation after prolonged bias stress. Both the threshold voltage (V_T) and the subthreshold slope (S) change over time when a gate bias is applied. The threshold voltage is the gate voltage required to turn the TFT on. The subthreshold slope is an important parameter characteristic of the subthreshold region and is defined as the voltage required to either increase or decrease the drain current by one decade (its unit is V/decade). These two bias induced metastability problems, especially V_T shift, seriously limit a-Si:H TFT application and effect the long-term performance of a-Si:H TFT circuits. Applications that are V_T shift intolerant usually have no means of using a-Si:H TFTs or require complicated V_T shift

compensating circuits to reduce the effect of V_T shift. Due to these reasons, other alternatives need to be explored.

a-Si:H TFTs show an exponential transfer characteristic in the subthreshold region. Since the operation is below the threshold, the effect of metastability problems may be kept minimal. Moreover, the typical power consumption of TFTs in the subthreshold region is on the order of nano-watts, making them suitable for low power design. However, the low current in the subthreshold operation could potentially cause problems in the circuit building blocks such as matching characteristics of a current mirror. As a result, detailed analysis of a-Si:H TFT current-voltage (I-V) characteristics in the forward subthreshold operation is required. A detailed model needs to be constructed, and the application to current mirrors should be examined.

1.4 Thesis Outline

In this thesis, a detailed model of a-Si:H TFT in the forward subthreshold region is derived, and this model is verified by static and dynamic experiments. The matching characteristics of current mirror circuits under the forward subthreshold operation are also studied.

Since a-Si:H TFT is the device under study in this thesis, a good understanding of the device physics is essential. Chapter 2 discusses the physics of the a-Si:H TFT and bias induced metastability. This chapter gives an overview of the a-Si:H TFT structure, the density of states distribution, and TFT static operation. The background knowledge on TFT metastability issues is also discussed.

Chapter 3 presents the derivation of the forward subthreshold static and dynamic models. It gives a complete static model, which includes model equations for the subthreshold saturation region

and for the subthreshold triode region, respectively. This chapter also presents the dynamic model that examines the subthreshold slope shift and V_T shift in the subthreshold region.

Chapter 4 covers the results of all the experiments verifying the static models derived in Chapter 3. Based on the experimental data, the empirical model equations are obtained and are compared with the theoretical model equations. This chapter also investigates the results of stress experiments and verifies them with the dynamic model mentioned in Chapter 3.

Chapter 5 studies the a-Si:H TFT current mirror circuit application. The fidelity of current matching is examined, and results are shown.

Chapter 6 concludes the thesis.

Chapter 2

a-Si:H TFT Device Characteristics

Disorder of the atomic structure is the main characteristic that differentiates a-Si from c-Si materials. The periodicity of the atomic structure is central to the theory of c-Si. However, a-Si lacks the long-range order that is in c-Si; thus, initial studies showed that a-Si material could not be used for electronic devices due to its high defect density. Later, hydrogen was introduced into the films via the glow discharge of silane gas [1], and the defect density was greatly reduced that led to the fabrication of a-Si:H p-n junction diodes, and eventually a-Si:H TFT [5].

In today's application, a-Si:H TFTs can be used as switching elements such as on-pixel switches or as analog active devices such as on-pixel amplifiers, dynamic loads, and output current drivers. However, a-Si:H TFTs exhibit device characteristic degradations that both the threshold voltage and the subthreshold slope change over time under gate bias stress. These degradations hinder the performance of a-Si:H TFT circuits.

The a-Si:H TFT structure, density of states distribution, static operation, and bias induced metastability are discussed in this chapter.

2.1 Device Structure

The commonly used TFT structure is the inverted-staggered bottom-gate TFT due to its simple fabrication process. The complete fabrication process requires five different photolithography masks: gate metal, transistor islands and channel layer, n^+ patterning layer, via layer, and top metal layer masks. Table 2.1 presents the typical thicknesses of the different layers of TFT structures [10].

Table 2.1. Typical thickness of the different layers of TFT structures.

Layer	**Thickness (nm)**
Gate metal	130
a-SiN_x:H gate dielectric	300
a-Si:H	50
a-SiN_x:H passivation layer	250
n^+μc-Si:H contact layer	50
Al metallization layer	500

Figure 2.1 shows the cross section of a-Si:H TFT, which indicates that it is a three terminal device. It consists of an undoped a-Si:H layer sandwiched between gate and passivation dielectrics (a-SiN_x:H), along with low-resistivity source and drain contacts. Therefore, the TFT has two a-Si:H/a-SiN_x:H interfaces. The a-Si:H/a-SiN_x:H interface that is deposited before a-Si:H film and closer to the gate terminal is referred to as the front interface. The interface closer to the drain and source terminals is referred to as the back interface. N-channel accumulation mode operation is most commonly used. Equivalent P-channel transistor is not used due to much lower mobility of holes in a-Si, which gives a factor of 100 drain current reduction compared to the N-channel transistor [11]. Depletion mode devices are prevented by the high defect density of doped material, which makes it difficult to deplete the channel [11].

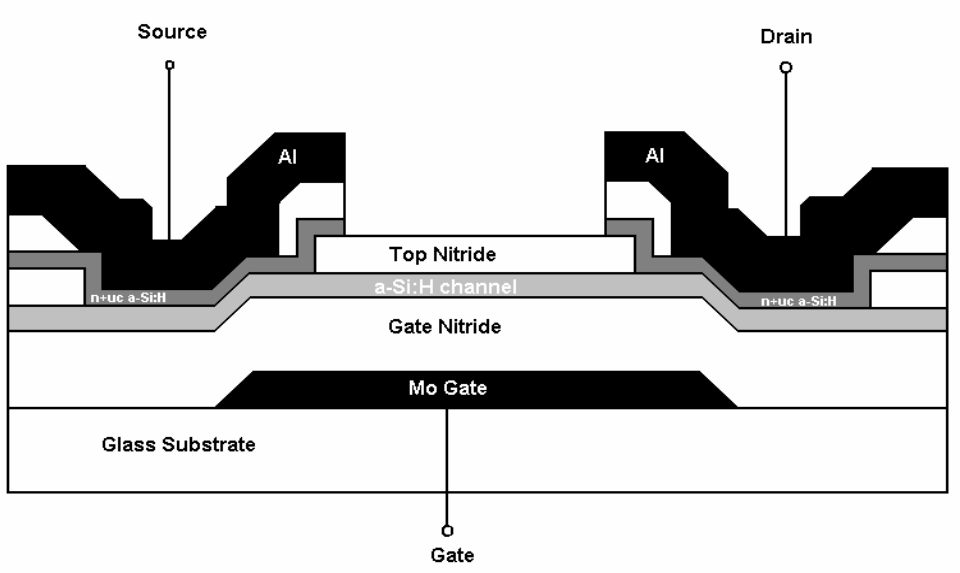


Figure 2.1. Cross-section of an inverted staggered a-Si:H TFT.

2.2 Density of States

c-Si materials possess long range order in its periodic lattice structure, resulting in a well-defined conduction band edge, valence band edge, and the band gap. Figure 2.2 illustrates the atomic structure and density of states (DOS) distribution of the c-Si [12]. For DOS distribution of c-Si, no defect states are assumed to exist in the forbidden region, and valence and conduction band edges are abrupt.

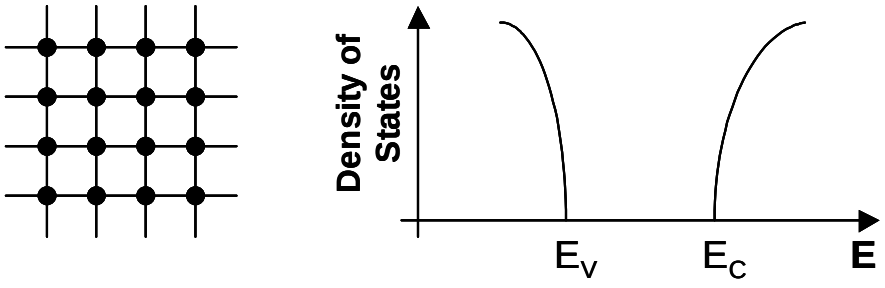


Figure 2.2. Atomic structure and DOS distribution in crystalline silicon.

a-Si materials do not possess long range order, but retain short range order characteristics of Si lattice. Compared to c-Si, a-Si also has a high density of dangling bond defects. Therefore, a-Si exhibits a complex DOS distribution. As shown in Figure 2.3, a-Si has conduction and valence bands just like c-Si, but the band tails of a-Si are extended into the forbidden gap [13]. These tail states arise from variation in bond lengths and angles in the structure. Beside the tail states, deep states also exist in a-Si. The deep states are due to dangling bonds and other microscopic point defects [11].

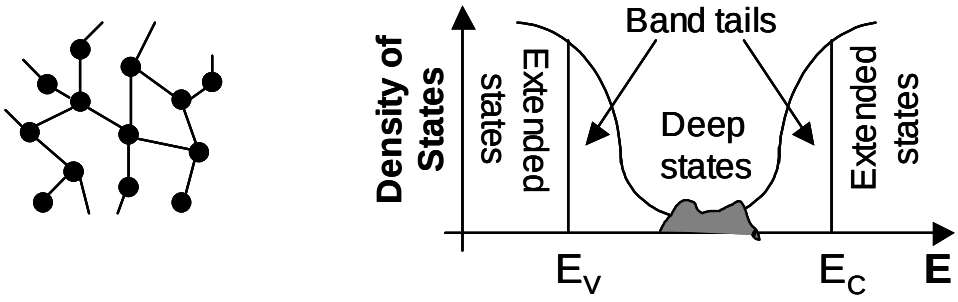


Figure 2.3. Atomic structure and DOS distribution in amorphous silicon.

The DOS distribution of a-Si in the mobility gap is asymmetrical, with the tail states near the conduction band having a narrower distribution than the tail states near the valence band. This asymmetry implies more holes have been trapped resulting in a lower hole mobility [13]. The tail states and deep states are referred as localized states. The other states are called extended states where the carriers are free to move, which are not spatially defined. The mobility of carriers in extended states is much higher than that of carriers in localized trap states. This is because in localized states, the conduction takes place by a series of trap and release events; hence, the mobility is lower than that of the carriers in extended states [11]. Due to the mobility difference in localized states and extended states, the mobility edge concept is often used in a-Si. The mobility edge is a defined cutoff line between the tail states and extended states. The mobility inside of the gap is both

temperature dependent and time dependent. It is temperature dependent due to the inherent thermal activation process, and it is time dependent due to the trap-release time distribution in the band tail and deep states [13].

2.3 A-Si:H Device Physics and Static Model

Depending on the gate-source voltage V_{GS}, different regions of operation can be identified: above-threshold, subthreshold, and Poole-Frenkel emission [14]. The subthreshold region is comprised of forward and reverse subthreshold regions. The above-threshold and forward subthreshold regions of operation are referred to as the forward region ($V_{GS} > 0$ V) of operation. The reverse subthreshold and Poole-Frenkel regions of operation are referred to as the reverse region ($V_{GS} < 0$ V) of operation, where the TFT is ideally off. Figure 2.4 displays the different regions of operation of a-Si:H TFT.

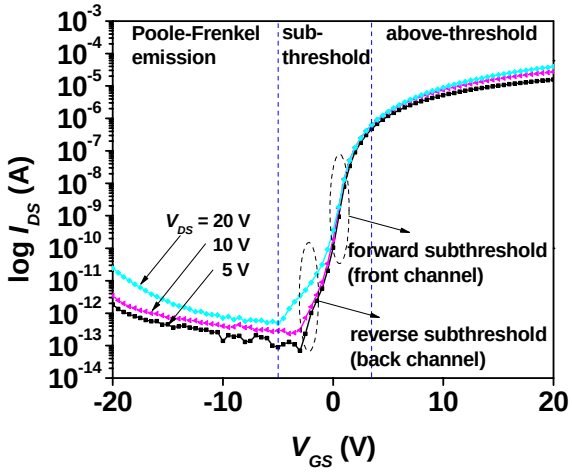


Figure 2.4. I_{DS} as a function of V_{GS} for different values of the drain-source voltage V_{DS} = 5, 10 and 20 V showing the different regions of operations.

2.3.1 Above-threshold region

In the above-threshold region ($V_{GS} > V_T$), the TFT is considered on and conducts a significant amount of current between the drain and the source terminals. In this region, the quasi-Fermi level lies close to the conduction band edge. As a result, the number of free electrons that participate in conduction increases, and the TFT can supply a high above-threshold current, which is in the range of μA [15]. The threshold voltage may be defined as the voltage at which the Fermi level enters the tail states. Depending on the value of the drain voltage V_{DS}, the above-threshold region can be divided into two sub-regions: linear region ($V_{DS} << V_{GS}$) and saturation region ($V_{DS} > V_{DSAT}$). The generic equation for the above-threshold region is written as [10]

$$I_{DS} = \frac{\mu_{eff}}{\alpha} \zeta C_i^{\alpha-1} \frac{W}{L} \left[(V_{GS} - V_T)^{\alpha} - (V_{GD} - V_T)^{\alpha} \right]. \tag{2.1}$$

Here, μ_{eff} is the effective field mobility, C_i is gate dielectric capacitance (F/cm^2), W and L are the channel width and channel length respectively. α is the power parameter and is given by $2V_{nc}/V_{th}$, where V_{nc} is a measure of the slope of the conduction band tail in a-Si:H and V_{th} is the thermal voltage. ξ is the property of a-Si:H material and is defined as [10]

$$\zeta = \frac{(q\varepsilon\alpha V_{th} N_0)^{1-\alpha/2}}{\alpha - 1} = \frac{(4.1\times10^{-16}\alpha)^{1-\alpha/2}}{\alpha - 1} \tag{2.2}$$

for a reference electron concentration $N_0 = 10^{17}$ cm^{-3}.

In the linear region, since $V_{DS} << V_{GS}$, , the drain current I_{DS} can be obtained by substituting V_{GD} by V_{GS} - V_{DS} in Eqn. (2.1) and yields [10]

$$
\begin{aligned}
I_{DS} &= \frac{\mu_{eff}}{\alpha}\zeta C_i^{\alpha-1}\frac{W}{L}\left[\left(V_{GS}-V_T\right)^{\alpha}-\left(V_{GD}-V_T\right)^{\alpha}\right] \\
&= \frac{\mu_{eff}}{\alpha}\zeta C_i^{\alpha-1}\frac{W}{L}\left[\left(V_{GS}-V_T\right)^{\alpha}-\left(V_{GS}-V_{DS}-V_T\right)^{\alpha}\right] \\
&\approx \frac{\mu_{eff}}{\alpha}\zeta C_i^{\alpha-1}\frac{W}{L}\left[\frac{\Delta\left(V_{GS}-V_T\right)^{\alpha}}{\Delta V_{DS}}\right]V_{DS} \\
&= \mu_{eff}\zeta C_i^{\alpha-1}\frac{W}{L}\left(V_{GS}-V_T\right)^{\alpha-1}V_{DS}\,.
\end{aligned}
\tag{2.3}
$$

For V_{DS} higher than the saturation voltage V_{dsat}, the TFT operates in the saturation region. The saturation voltage V_{dsat} is the voltage for which the density of mobile carriers at the drain side of the channel reduces to the pinch off condition and is given by

$$
V_{dsat} = \alpha_{sat}\left(V_{GS}-V_T\right), \tag{2.4}
$$

where α_{sat} is the saturation parameter. Therefore, substituting V_{GS} - V_{dsat} for V_{GD} in Eqn. (2.1) yields the drain current in the saturation region as [10]

$$
\begin{aligned}
I_{DS} &= \frac{\mu_{eff}}{\alpha}\zeta C_i^{\alpha-1}\frac{W}{L}\left[\left(V_{GS}-V_T\right)^{\alpha}-\left(V_{GD}-V_T\right)^{\alpha}\right] \\
&= \frac{\mu_{eff}}{\alpha}\zeta C_i^{\alpha-1}\frac{W}{L}\left[\left(V_{GS}-V_T\right)^{\alpha}-\left(V_{GS}-V_{dsat}-V_T\right)^{\alpha}\right] \\
&= \frac{\mu_{eff}}{\alpha}\zeta C_i^{\alpha-1}\frac{W}{L}\left[\left(V_{GS}-V_T\right)^{\alpha}-\left[\left(V_{GS}-V_T\right)\left(1-\alpha_{sat}\right)\right]^{\alpha}\right] \\
&= \frac{\mu_{eff}}{\alpha}\zeta C_i^{\alpha-1}\frac{W}{L}\left(V_{GS}-V_T\right)^{\alpha}\left[1-\left(1-\alpha_{sat}\right)^{\alpha}\right] \\
&= \frac{\mu_{eff}}{\alpha}\zeta C_i^{\alpha-1}\frac{W}{L}\gamma_{sat}\left(V_{GS}-V_T\right)^{\alpha},
\end{aligned}
\tag{2.5}
$$

where $\gamma_{sat} = 1-\left(1-\alpha_{sat}\right)^{\alpha}$.

If channel length modulation is included, the saturation current equation is modified as [10]

$$
I_{DS} = \frac{\mu_{eff}}{\alpha}\zeta C_i^{\alpha-1}\frac{W}{L}\gamma_{sat}\left(V_{GS}-V_T\right)^{\alpha}x_{cm}\,. \tag{2.6}
$$

Here, the parameter x_{cm} describes the channel length modulation and is defined as

$$x_{cm} = 1 + \lambda V_{DS} / L_{eff} , \tag{2.7}$$

where λ is the channel modulation parameter.

2.3.2 Subthreshold region

In the subthreshold region of operation, the TFT switches from off to on and the current changes exponentially from a low off current, which is in pA, to a high on current, which is in μA. Depending on the polarity of the gate bias, there are two sub regions: forward subthreshold and reverse subthreshold.

The forward subthreshold region is defined as $V_T > V_{GS} > V_{TS}$, where $V_{TS} \sim 0$ V is the boundary of the forward subthreshold region [15]. At the low positive gate voltage, the Fermi-level is in the middle of the band gap close to its intrinsic level, and hence, most of the induced carriers go into the deep localized states in the a-Si:H layer and into interface states at the a-Si:H/insulator interfaces. A small fraction of electrons close to the front interface in the a-Si:H bulk layer participate in conduction, which leads to a subthreshold current in the order of 10^{-12} to 10^{-8} A [15]. The drain current equation in the forward subthreshold region is defined by [16]

$$I_{DS} = I_{sub0} \frac{W}{L} \exp\left(\frac{V_{GS} - V_{TS}}{S_f} \right), \tag{2.8}$$

where I_{sub0} is the magnitude of current in the subthreshold region, and S_f is the forward subthreshold slope that can be obtained by measuring the slope of the log-linear plot of I_{DS} versus V_{GS} when the TFT operates in the subthreshold region.

In the reverse subthreshold region, due to the negative V_{GS}, electrons are repelled from the front interface, which reduces the role of the front interface in conduction. Subsequently, a high

density of interface states is present at the back interface. Therefore, a weak electron channel is formed, which provides a conduction path between the drain and source electrodes in the reverse subthreshold region [17]. The reverse subthreshold equation can be written as [16], [17]

$$I_{DS} = I_{sub0} \frac{W}{L} \exp\left(\frac{V_{GS} - V_{TS}}{S_r + \gamma_n |V_{DS}|} \right), \tag{2.9}$$

where S_r is the reverse subthreshold slope and γ_n is a unitless parameter accounting for two dimensional effects.

2.3.3 Poole-Frenkel Region

As V_{GS} becomes more negative, the TFT enters the Poole-Frenkel region where the leakage drain current increases exponentially with an increase in the negative V_{GS}. Accumulation of holes at the front interface by the negative V_{GS} provides a conduction path for this type of leakage current. This front channel conduction due to the hole generation is a result of Poole-Frenkel field-enhanced thermionic emission at the vicinity of the gate-drain overlap. The I_{DS} equation in the Poole-Frenkel region is defined as [16], [17]

$$I_{DS} = J_{OF} WOL \exp\left(\sqrt{\left| \frac{V_{GD}}{V_{PF}} + \gamma_p V_{DS} \right|} \right), \tag{2.10}$$

where J_{OF} is the effective current at zero bias, γ_p is a parameter accounting for two-dimensional effects, OL is the overlap area, and V_{PF} is the effective Poole-Frenkel voltage parameter.

A good TFT should have low V_T, low leakage current, small subthreshold slope, high ON/OFF switching ratio, and high μ_{eff}. Typical values for the a-Si:H TFT parameters are given in Table 2.2 [16].

Table 2.2. Typical values of a-Si TFT parameters.

Physical Parameters	Value	unit
V_T - threshold voltage	2 – 4	V
Leakage current	~ 10	fA
S - subthreshold slope	0.3 – 0.5	V/decade
switching ratio	10^6 - 10^8	
μ_{eff} - effective mobility	0.4 – 1	cm^2/V-s
α - power parameter	2 to 2.27	

2.4 Bias Induced Metastability

a-Si:H TFTs exhibit a slow change in V_T and the subthreshold slope after prolonged gate bias stress. For digital circuits, a small V_T shift can be tolerated but it reduces the lifetime and reliability of the system. For analog circuits, the V_T shift poses a serious bottleneck for long-term performance. The subthreshold slope shift degrades the current driving capability and hence reduces the switching speed.

The effect is metastable, and the electrical characteristics can be mostly restored by removing the bias stress and annealing the device at the high temperature. To explain this effect, two mechanisms have been proposed in the literature: (i) charge trapping, and (ii) defect state creation [18], [19].

2.4.1 Charge Trapping

Charge trapping occurs primarily in PECVD SiN insulator TFTs, where the high density of defects can trap charges when the TFT is under the gate bias stress. Electrons are injected into the insulator layer of a-Si:H TFT to cause the V_T shift. Depending on the broad distribution of energies

for the trapping levels in the a-SiN_x:H layer, two kinds of charge trapping behaviour are observed: interfacial charge trapping at the a-Si:H/a-SiN_x:H boundary, and bulk charge trapping inside of the a-SiN_x:H layer [18].

The two trapping behaviours describe how electrons are being trapped. Electrons are first trapped in the localized interfacial states at the a-Si:H/a-SiN_x:H interface; then, these electrons are thermalized to deeper energy states inside the a-SiN_x:H layer (bulk) by either multiple-trapping and emission process [20] or variable-range hopping process [18]. The interfacial charge trapping states are often called fast states due to their fast re-emission times. The density of these fast states decreases when the optical band gap of the a-SiN_x:H layer increases. The bulk charge trapping states are called slow states due to their slow re-emission times. The number of these deep traps can be reduced in a wider band gap, nitrogen-rich a-SiN_x:H layers. Since the redistribution of trapped charge does not occur by conduction in a-SiN_x:H, the mechanism shows very little temperature dependence.

2.4.2 Defect State Creation

The second mechanism related to metastability is defect state creation, in the a-Si:H layer or at the a-Si:H/a-SiN_x:H interface, which increases the density of deep gap states. This involves breaking down the weak silicon-silicon bonds of the tail states, and forming silicon dangling bonds in the deep states [21], [22].

When a positive gate bias is applied to the TFT, the electrons are accumulated at the a-Si:H/a-SiN_x:H interface. Most of these electrons reside in the conduction band tail states. The presence of electrons in the tail states results in the breaking of weak bonds and the formation of electron traps, which implies the creation of deep state defects. Consequently, the Fermi level is lowered, which is seen by the reduction of field effect mobility. The created defect states can positively shift V_T; however, only the states with energy position in the upper part of the energy gap can degrade the

subthreshold slope [23]. Defect state creation is independent of nitride, implying that state creation takes place in the a-Si:H active layer [15].

The physics of state creation and the state removal process can be explained by the defect pool model [23]. In a-Si:H, the defect pool is a large pool of potential defects consisting of silicon dangling bonds. The defect pool model explains that the density of states distribution in the mobility gap of amorphous material is dependent on the Fermi energy position during equilibration. The states in the a-Si:H distribute near the conduction band of the band gap if the Fermi level is close to the valence band, whereas they distribute near the valence band if the Fermi level is close to the conduction band.

2.4.3 Discussion

Both charge trapping and defect state creation mechanisms cause TFT V_T shift. However there are several distinctions between these two. The first difference between the two mechanisms is that charge trapping in the nitride occurs at the high gate voltage bias and long stress times, whereas defect state creation happens at lower stress voltage (below 25 V) and shorter stress times [24]. Second, depending on the polarity of the trapped carriers, i.e., electron or hole, V_T shift can be either positive or negative for charge trapping mechanism [15]. In contrast, defect state creation causes a metastable increase in the density of deep states; hence, the increase in the number of defect states causes V_T to increase positively in the N-channel TFTs [15]. Third, charge trapping is nitride related, but defect state creation is independent of nitride [15]. Lastly, charge trapping is characterized by a logarithmic time dependence and is independent of temperature [18]. Defect state creation, on the other hand, is a power law time dependence and is temperature dependent [18].

Chapter 3

Theoretical Model in Forward Subthreshold

The most common forward subthreshold model from literature is defined in Eqn. (2.8) and is rewritten here as [25], [26]

$$I_{DS} = I_{sub0} \frac{W}{L} \exp\left(\frac{V_{GS} - V_{TS}}{S_f} \right). \tag{3.1}$$

A more detailed forward subthreshold model based on Servati's work is given by [15]

$$I_{DS} = I_{sub0} \frac{W}{L} \left(\exp\left(\frac{V_{GS} - V_{TS}}{S_f} \right) - \exp\left(\frac{V_{GD} - V_{TS}}{S_f} \right) \right), \tag{3.2}$$

where V_{GD} is the gate-drain voltage. However, both Eqns. (3.1) and (3.2) fail to explain the effect of V_{DS} on I_{DS}. Furthermore, since the subthreshold current is low, few studies have been performed on the forward subthreshold operation, especially with respect to dynamic operation and circuit applications.

Although the subthreshold operation is well studied in the conventional metal-oxide-semiconductor field-effect transistor (MOSFET) models, because of a-Si:H unique device characteristics, MOSFET models cannot accurately predict the characteristics of a-Si:H TFTs due to

the presence of both free and trapped carriers. Therefore, we need to construct a detailed forward subthreshold model of a-Si:H TFTs.

This chapter presents a theoretical forward subthreshold model of a-Si:H TFT static and dynamic characteristics.

3.1 Static Characteristics

In this section, density of states, conductivity, and trapped and free carrier concentrations of a-Si:H are explained, followed by the derivation of the forward subthreshold compact model. Two sub-regions, saturation and triode, are identified, and their current equations are provided.

3.1.1 Conductivity, Trapped and Free Carrier Concentrations

Figure 3.1 plots the density of states (DOS) of the a-Si:H mobility gap [27]. The distribution of the localized states in the mobility gap is modeled by exponential distributions of tail and deep states for both acceptor-like and donor-like states. States with energies higher than the conduction band edge E_C are the extended states of the conduction band for which the electron band mobility μ_{band} holds true. μ_{band} is dependent on the disorder of a-Si:H and is approximately 13 cm^2/Vs at room temperature (300 K) [10]. Neglecting the hopping conduction for the localized states, the conductivity σ_n ($\Omega^{-1}cm^{-1}$) is mainly due to electrons excited to the extended states and is defined as

$$\sigma_n = q\mu_{band} n_{free} . \tag{3.3}$$

Here, n_{free} (cm^{-3}) is the density of free electrons in the a-Si:H bulk and is written as

$$n_{free} = N_C \exp\left(\frac{E_F - E_C}{kT}\right) = n_{fi} \exp\left(\frac{\psi}{V_{th}}\right), \tag{3.4}$$

where E_F denotes the Fermi-level, N_C is the concentration of free electrons when $E_F = E_C$, k is Boltzmann's constant, T is the temperature, V_{th} is the thermal voltage and is defined as $V_{th} = kT / q$, ψ is the band bending and is defined as $\psi = (E_F - E_i) / q$, n_{fi} is the density of free electrons for no band bending and is defined as $n_{fi} = N_C \exp(E_i - E_C) / kT$, where E_i is the intrinsic Fermi-level of a-Si:H.

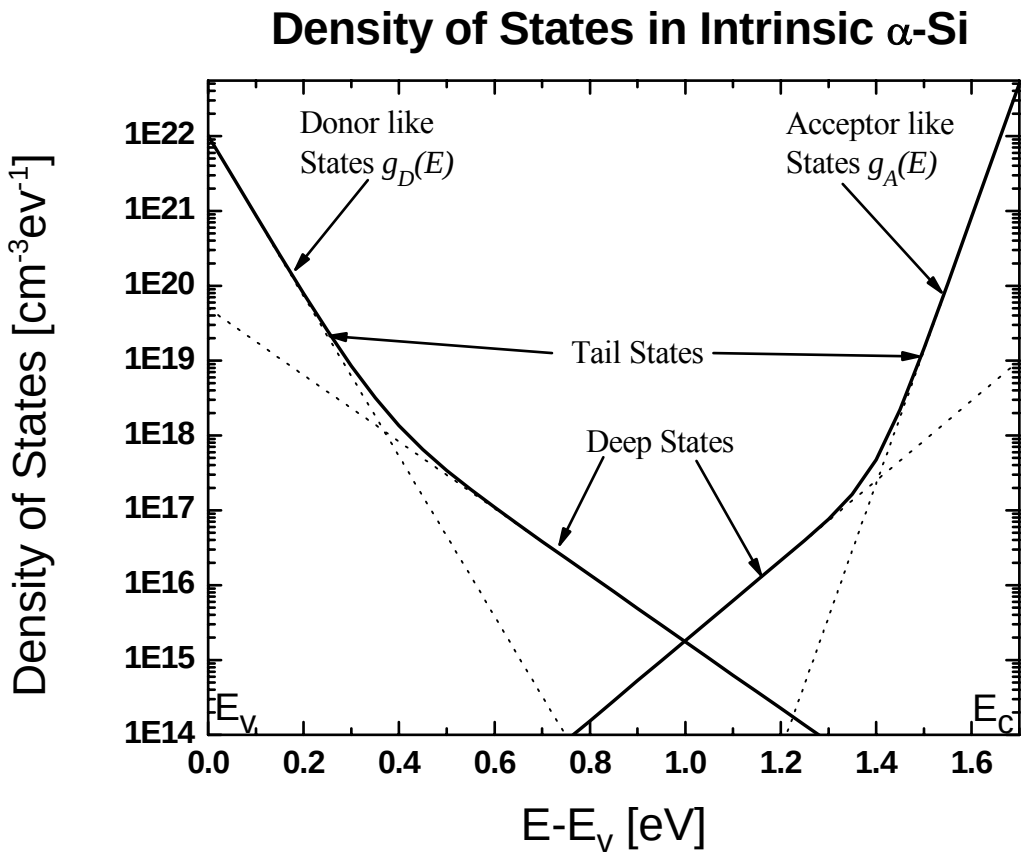


Figure 3.1. Illustration of the DOS in intrinsic a-Si:H. Adopted from [27].

The density of the trapped electrons n_t at a specific position of the Fermi level, E_F, can be defined as

$$n_t = n_{ti} \exp\left(\frac{\psi}{V_{nt}}\right) + n_{di} \exp\left(\frac{\psi}{V_{nd}}\right), \tag{3.5}$$

where n_{ti} is the density of trapped electrons when $E_F = E_i$, V_{nt} is the characteristic exponential slope of the acceptor-like tail states (conduction band tail states), n_{di} is the density of trapped electrons in the deep states, and V_{nd} is the characteristic exponential slope of the acceptor-like deep states.

3.1.2 Forward Subthreshold Compact Model

In the forward subthreshold region ($V_T > V_{GS} > V_{TS}$, where V_{TS} is the border of the forward subthreshold region), the a-Si:H TFT is switched from on to off, and the current changes exponentially from a high on current (~ μA) to a low off current (~ pA). In this region, the Fermi-level is in the middle of the band gap close to its intrinsic level. Most of the induced electrons go into the interface states at the front interface and localized acceptor-like deep states in the a-Si:H band gap. A small fraction of electrons close to the front interface participate in conduction, which leads to a small subthreshold current on the order of 1 fA to 10 nA. The characteristics of these states are a strong function of the quality of different TFT layers. The interface between the a-Si:H layer and gate insulator is referred to as the front interface. The band bending at the front interface is an important factor in determining the I-V characteristics in the forward subthreshold operation.

For an arbitrary location in the channel, the applied voltage V_a can be defined as the difference between the gate metal Fermi-level and the Fermi-level in the a-Si:H layer

$$V_a - V_{FB} = \psi_{Sf} + V_i, \tag{3.6}$$

where V_{FB} is the flat band voltage, ψ_{Sf} is the band bending at the front interface, and V_i is the voltage drop over the gate insulator layer. Gauss' Law for the electric field at the front interface E_0 yields

$$C_i V_i + Q_i = C_{ssf}\left(\psi_{Sf} - \psi_{Sf0}\right) + \varepsilon E_0. \tag{3.7}$$

Here, C_i is the gate dielectric capacitance per unit area, Q_i is the charge in the gate capacitance per unit area, C_{ssf} is the effective interface capacitance and is equal to q^2D_{ssf}, where D_{ssf} is the effective density of states at the front interface, ψ_{Sf0} is the band bending at the front interface in the absence of voltage, and ε is the a-Si:H dielectric constant. The term εE_0 is the total charge in the a-Si:H semiconductor layer per unit area, which includes free carriers and charge trapped in the localized deep or tail states. Therefore, substituting V_i from Eqn. (3.6) into Eqn. (3.7) gives

$$V_a - V_{FB} + \frac{Q_i}{C_i} = \psi_{Sf} + \frac{C_{ssf}}{C_i}\left(\psi_{Sf} - \psi_{Sf\,0}\right) + \frac{\varepsilon E_0}{C_i}, \tag{3.8}$$

which describes the band bending at the front interface as a function of V_a.

Since the density of trapped electrons at the interfaces and deep states are the main charge components in the forward subthreshold region, Eqn. (3.5) can be simplified to only consider the density of trapped electrons in the deep gap states, n_{td}

$$n_{td} = n_{di} \exp\left(\frac{\psi}{V_{nd}}\right). \tag{3.9}$$

In the subthreshold region, assume the change in band bending in the a-Si:H layer is trivial due to the small thickness of a-Si:H layer, the entire a-Si:H layer acts as a very thin layer with the average band bending at the front interface, ψ_{Sf}. Therefore, replace ψ in Eqn. (3.9) by ψ_{Sf}, the charge in the deep states of the a-Si:H layer is approximated as

$$\varepsilon E_0 = q t_{Si} n_{td} = q t_{Si} n_{di} \exp\left(\frac{\psi_{Sf}}{V_{nd}}\right). \tag{3.10}$$

Substituting Eqn. (3.10) into Eqn. (3.8) gives

$$V_a - V_{FB} + \frac{Q_i}{C_i} = \psi_{Sf} + \frac{C_{ssf}}{C_i}\left(\psi_{Sf} - \psi_{Sf\,0}\right) + \frac{q t_{Si} n_{di}}{C_i} \exp\left(\frac{\psi_{Sf}}{V_{nd}}\right). \tag{3.11}$$

Since the third term on the right hand side of Eqn. (3.11) only considers trapped electrons in the deep acceptor-like states. As mentioned before, the interface states also play an important role in the subthreshold operation. However, the interfacial and deep states cannot be distinctly separated. Therefore, to include both charge components, the Taylor's expansion is applied on the third term on the right hand side of Eqn. (3.11), which yields

$$\begin{aligned} V_a - V_{FB} + \frac{Q_i}{C_i} &\approx \psi_{Sf} + \frac{C_{ssf}}{C_i}\left(\psi_{Sf} - \psi_{Sf0}\right) + \frac{qt_{Si}n_{di}}{C_i}\left(\frac{\psi_{Sf}}{V_{nd}} + 1\right) \\ &\approx \psi_{Sf} + \frac{C_{ssf}}{C_i}\left(\psi_{Sf} - \psi_{Sf0}\right) + \frac{C_{sd}}{C_i}\left(\psi_{Sf} + V_{nd}\right) \end{aligned}, \tag{3.12}$$

where C_{sd} is the effective capacitance of the deep acceptor-like states in the a-Si:H bulk and is defined as $C_{sd} = qt_{si}n_{di} / V_{nd}$, t_{si} is the a-Si:H layer thickness. Rearranging Eqn. (3.12) for ψ_{Sf} gives

$$\psi_{Sf} = \left(V_a - V_{FB} + \frac{Q_i}{C_i} + \frac{C_{ssf}}{C_i}\psi_{Sf0} - \frac{C_{sd}}{C_i}V_{nd}\right) \Bigg/ \left(1 + \frac{C_{ssf}}{C_i} + \frac{C_{sd}}{C_i}\right) = \frac{V_a - V_{TS}}{S_f}. \tag{3.13}$$

Here, S_f is the forward subthreshold slope and can be written as

$$S_f = \left(1 + \frac{C_{ssf}}{C_i} + \frac{C_{sd}}{C_i}\right)V_{th}. \tag{3.14}$$

V_{TS} is the boundary of the forward subthreshold or the threshold voltage in the forward subthreshold region, which is defined as

$$V_{TS} \approx V_{FB} - \frac{Q_i}{C_i} - \frac{C_{ssf}}{C_i}\psi_{Sf0} + \frac{C_{sd}}{C_i}V_{nd}. \tag{3.15}$$

Based on the gradual channel approximation, the subthreshold current can be written as

$$I_{DS} = W\frac{dV_{ch}}{dx}\int_0^{t_{Si}} \sigma_n(V_{ch}, y)dy. \tag{3.16}$$

Substituting Eqn. (3.3) and Eqn. (3.4) into Eqn. (3.16), and replacing ψ by ψ_{Sf} in Eqn. (3.4) yields

$$I_{DS} = W\frac{dV_{ch}}{dx}\int_0^{t_{Si}} q\mu_{band} n_{fi} \exp\left(\frac{\psi_{Sf}}{V_{th}}\right) dy = W\frac{dV_{ch}}{dx} q\mu_{band} n_{fi} \exp\left(\frac{\psi_{Sf}}{V_{th}}\right) t_{Si}\,. \tag{3.17}$$

Substituting Eqn. (3.13) into Eqn. (3.17) and replace $V_G - V_{ch}$ for V_a, integrating from source to drain gives

$$\begin{aligned} I_{DS} &= \frac{W}{L} q\mu_{band} n_{fi} t_{Si} \int_{V_S}^{V_D} \exp\left(\frac{V_G - V_{ch} - V_{TS}}{S_f}\right) dV_{ch} \\ &= \frac{W}{L} q\mu_{band} n_{fi} t_{Si} \exp\left(\frac{V_G - V_{TS}}{S_f}\right)\left(-S_f \exp\left(\frac{-V_{ch}}{S_f}\right)\Bigg|_{V_S}^{V_D}\right), \\ &= \frac{W}{L} I_{sub0} \exp\left(\frac{V_G - V_{TS}}{S_f}\right)\left(\exp\left(\frac{-V_S}{S_f}\right) - \exp\left(\frac{-V_D}{S_f}\right)\right) \end{aligned} \tag{3.18}$$

where I_{sub0} denotes the magnitude of current in the forward subthreshold region and is defined as $I_{sub0} = q\mu_{band} n_{fi} t_{si} S_f$. Note that due to the inverted-staggered bottom-gate TFT structure, the integration is done by integrating from V_S to V_D. This is different from the MOSFET current equation, where it is integrated from 0 to V_{DS} because the gate of a MOSFET transistor is at the same structure level as the source and drain.

Eqn. (3.18) is the general current equation for the forward subthreshold region. Similar to the subthreshold model of MOSFET [28], Eqn. (3.18) encompasses of two regions of operation: the saturation region and the triode region. In the subthreshold saturation region, I_{DS} is almost independent of V_{DS}. However, in the subthreshold triode region, I_{DS} depends on V_{DS}.

3.1.2.1 Subthreshold Saturation Region

In the subthreshold saturation region, the concentration of electrons at the drain end of the channel can be approximated as zero when compared to the concentration at the source end. Any electrons in the channel that diffuse close to the drain are immediately swept into the drain by the

applied electric field in this region. Therefore, the diffusion current no longer shows dependence on the electron concentration at the drain, and the current in the TFT depends only on V_s. Eqn. (3.18) can be simplified as

$$I_{DS,fs\_sat} = I_{sub0}\frac{W}{L}\exp\left(\frac{V_{GS}-V_{TS}}{S_f}\right). \tag{3.19}$$

3.1.2.2 Subthreshold Triode Region

The subthreshold triode region describes the current operation for the small V_{DS}. By factoring out $\exp(-V_{DS} / S_f)$, Eqn. (3.18) can be modified as

$$I_{DS,fs\_Triode} = I_{sub0}\frac{W}{L}\exp\left(\frac{V_{GS}-V_{TS}}{S_f}\right)\left(1-\exp\left(\frac{-V_{DS}}{S_f}\right)\right). \tag{3.20}$$

3.2 Dynamic Characteristics

The study of metastability characteristics, such as V_T shift and subthreshold slope shift under prolonged bias stress, is critical in predicting the long-term performance of TFT circuits.

3.2.1 Subthreshold Slope Shift

As mentioned in Chapter 2, the subthreshold slope changes over time during a gate bias stress. Since the subthreshold slope is time dependent, by having t as a time parameter, Eqn. (3.14) can be rewritten as

$$S_f(t) = S_f(t=0) + \Delta S_f(t>0) = \left(1+\frac{C_{ssf}(t)}{C_i}+\frac{C_{sd}(t)}{C_i}\right)V_{th}. \tag{3.21}$$

Here, the effective interface capacitance C_{ssf} and the effective capacitance of the deep acceptor-like states C_{sd} are two time dependent parameters. The interfacial charge trapping states contribute to C_{ssf}, while the deep states in the a-Si:H bulk layer contribute to C_{sd}. How exactly these two states affect the subthreshold slope degradation under the long-term gate bias stress will be examined in Chapter 4.

3.2.2 V_T shift

Since the subthreshold operation is in the region below the threshold voltage, ideally there should be no V_T shift. However, since V_T shifts are due to the charge trapping and defect state creation, these two metastable mechanisms also exist in the subthreshold region. Therefore, theoretically there will be a V_T shift in the forward subthreshold operation or V_{TS} shift. Thus, Eqn. (3.15) can be rewritten by considering time effects as

$$V_{TS}(t) = V_{TS}(t=0) + \Delta V_{TS}(t>0) = V_{FB} - \frac{Q_i}{C_i} - \frac{C_{ssf}(t)}{C_i}\psi_{Sf0} + \frac{C_{sd}(t)}{C_i}V_{nd}\,. \tag{3.22}$$

As mentioned in Section 3.1.2, V_{TS} is derived by assuming that the change in band bending in the a-Si:H layer is trivial due to the small thickness of the a-Si:H layer. The static threshold voltage equation is defined as [15]

$$V_T = V_{FB} - \frac{Q_i}{C_i} + \psi_{ST} + \frac{C_{ssf}}{C_i}\left(\psi_{ST} - \psi_{Sf0}\right) + \frac{C_{sd}}{C_i}\left(\psi_{ST} + V_{nd}\right). \tag{3.23}$$

Therefore, the difference between V_T and V_{TS} in the static model is

$$V_T - V_{TS} = \psi_{ST}\left(1 + \frac{C_{ssf}}{C_i} + \frac{C_{sd}}{C_i}\right) = \frac{\psi_{ST}}{v_{TH}}S_f\,. \tag{3.24}$$

Here, V_{th} is the thermal voltage, which has a time independent value around 25.8 mV at the room temperature. Therefore, the difference between V_T and V_{TS} is proportional to the threshold band

bending, ψ_{ST}, and the subthreshold slope, S_f. The threshold band bending plays an important role in generating a V_T shift. The localized interfacial states are increased due to the band bending, and these charged interface states cause defect states, which increase trapping in the tail states of the a-Si:H bulk layer [11]. Since the threshold band bending is not concerned in the subthreshold operation, the effect of V_{TS} shift can be mainly contributed by the change of subthreshold slope. The next chapter will examine the V_{TS} shift in detail.

Chapter 4

Experiment, Result and Discussion

In Chapter 3, static and dynamic models of a-Si:H TFT in the forward subthreshold region are derived. In order to verify these models, static measurements and stress tests were performed. Empirical static models are built directly from the experimental data to compare with the theoretical models. The experimental setup, the static experiments, and the dynamic experiments are discussed in this chapter.

4.1 Experimental Setup

The a-Si:H TFTs used by the experiments were the inverted-staggered, bottom-gate design with a passivating silicon nitride layer on top of the a-Si:H channel layer. The samples were annealed at 175 °C for 3 hours and cooled for 4 hours before each measurement. The annealing and cooling procedures were verified to restore both TFT I-V transfer characteristics and V_T to within 5% of their original pre-stress values.

The measurement and stress tests were done on the TFTs using a parametric test system comprising the Keithley 236 source measurement units (SMUs). The experimental setup is shown in Figure 4.1. Two SMUs were used as controlled voltage source to measure the current flowing through them. The TFTs under test were on a die bonded to a dual-in-line package. The packaged

die was placed in the Keithley 236 choke, which was attached to SMUs. SMU1 and SMU2 were connected to the gate and the drain of the tested TFT respectively, and the source was connected to the system ground in all the measurements. For I_{DS} versus V_{GS} measurements, V_{DS} was set to a fixed value and a sweep of V_{GS} was taken. For I_{DS} versus V_{DS} measurements, V_{GS} was set to a fixed value and a sweep of V_{DS} was taken. One second of delay time and one second of holding time were maintained between each step of the sweep in SMUs to deal with transient current fluctuations. For the constant voltage stress tests, a fixed voltage was applied to the gate of the TFT, whereas the drain is either kept at zero bias or at a fixed voltage. After a predetermined stress time, the TFT was switched from stress to measurement, and a sweep of I_{DS} versus V_{GS} was taken. Then, the process was repeated. The stress tests could be set automatically by a timing setup in the SMUs.

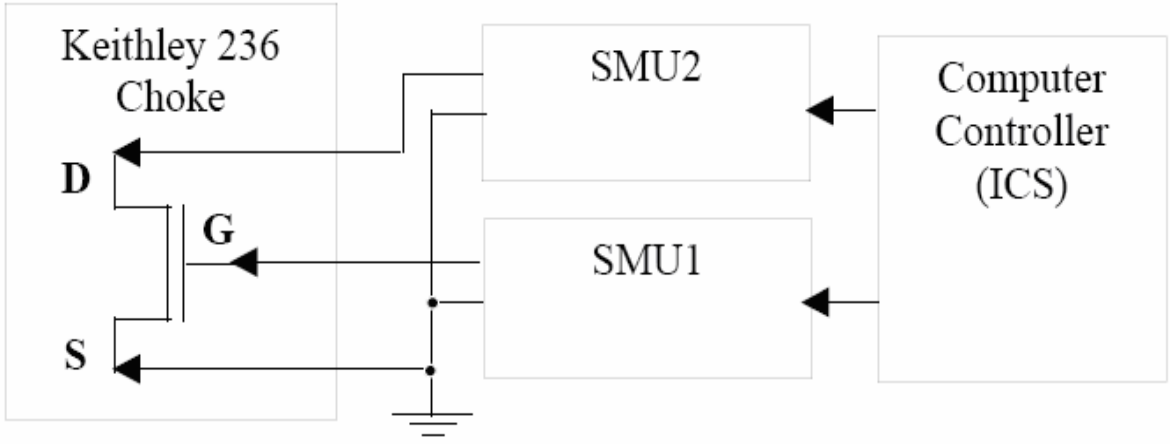


Figure 4.1. Experimental setup for TFT measurements using SMUs.

The V_T and subthreshold slope of the tested TFT were determined by either the linear or saturation extrapolation of the transfer curve of I_{DS} versus V_{GS}. Computer programs such as Excel and Matlab were used to graph and perform extrapolation. After each stress test, the TFT was annealed to restore the initial device characteristics, and the experimental procedure was repeated using a

different voltage setting or a different TFT. The measurement was done on different sizes of TFTs in order to check the dependence of TFT dimension on V_T.

4.2 Static Experiments of I-V Characteristics

Before studying the static models of the forward subthreshold operation, we need to first study the dependence of I-V characteristics on V_{DS}. Second, we need to observe the dependence on different TFT dimensions. Finally, we can obtain the empirical model equations based on the experimental data for the two sub-regions, namely, subthreshold triode region and subthreshold saturation region. Therefore, a number of static experiments were performed and are discussed in the following section.

4.2.1 I_{DS} versus V_{GS} for Different V_{DS}

We need to study the dependence of the I-V characteristics on V_{DS}, and to comprehend the role of V_{DS} in the subthreshold operation. Two tests were carried out and a 400μm/23μm TFT with $V_T \approx 2.4$ V was used. The Cadence layout of single TFTs with different dimensions is given in Appendix A. The first test measured I_{DS} versus V_{DS} for a fixed V_{GS} value. During the sweep, V_{GS} was set to 2 V and V_{DS} was swept from 0 V to 3 V with a step size of 50 mV. As seen in Figure 4.2, when V_{DS} is above 1 V, I_{DS} becomes roughly constant, which indicates that I_{DS} is virtually independent of V_{DS}. Therefore, the region is called the saturation region. When V_{DS} is below 1 V, the drain current exponentially decreases as V_{DS} decreases. Thus, the region is called triode region or linear region, similar to the above-threshold characteristics of TFT where I_{DS} is linear with V_{DS}.

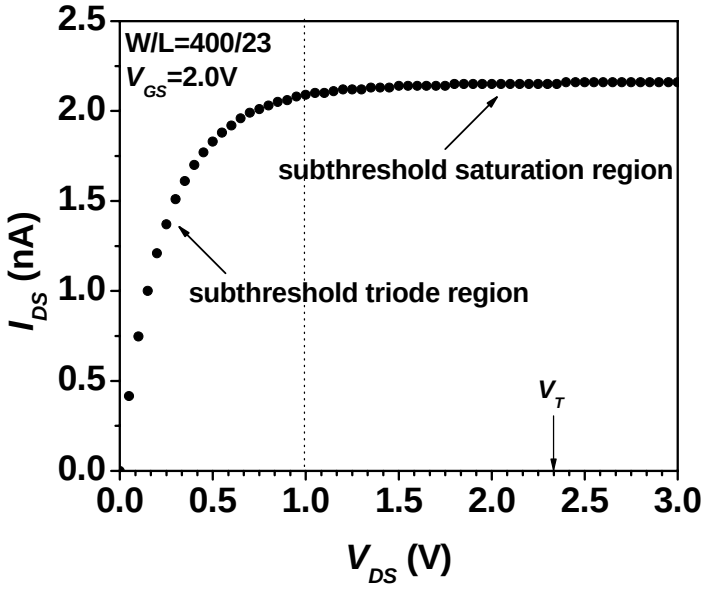


Figure 4.2. I_{DS} as a function of V_{DS} for a fixed V_{GS} value (V_{GS} = 2 V).

The second test involved sweeping of V_{GS} for different V_{DS} values from 0.5 V to 3 V. In this test, for each V_{DS} value, a sweep of V_{GS} was taken. Figure 4.3 shows log I_{DS} as a function of V_{GS} for different V_{DS}. Again this graph shows from V_{GS} = 1 V to V_{GS} = 2.4 V ($\approx V_T$), the drain current is approximately the same for each different V_{DS} value. Below V_{GS} = 1 V, I_{DS} shows the dependence on V_{DS}.

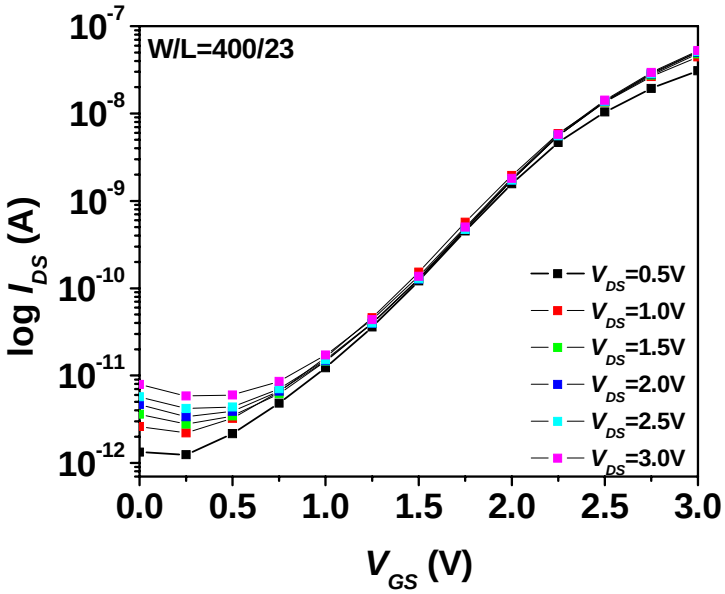


Figure 4.3. I_{DS} as a function of V_{GS} for different V_{DS} values.

4.2.2 I_{DS} versus V_{GS} for Different TFT Dimensions

Geometry dependence is an important parameter in the drain current equations. From Eqn. (3.18), we see the dependence of drain current on TFT size, which is measured by width over length (W/L). Thus, we need to verify this dependence in the experiments. Figure 4.4 illustrates the log I_{DS} versus V_{GS} for four different TFT dimensions, and Table 4.1 shows comparison of the TFT W/L ratio and its corresponding drain current.

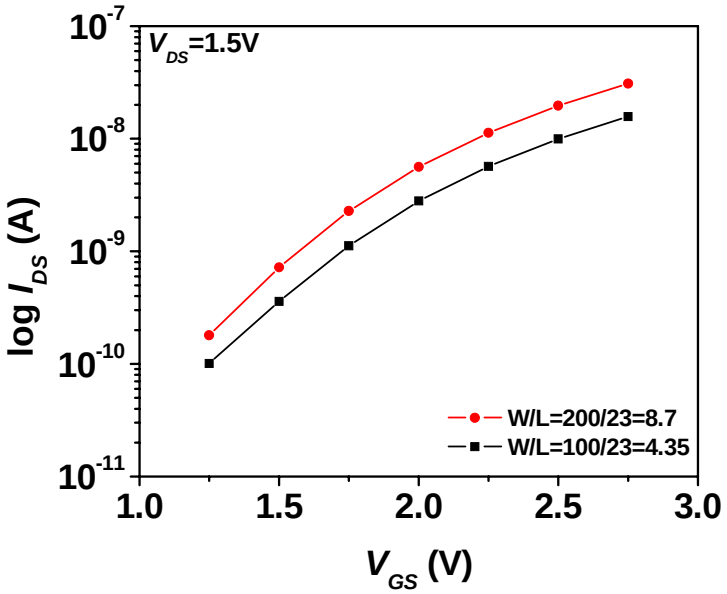


Figure 4.4. I_{DS} as a function of V_{GS} for different transistor dimensions.

Table 4.1. Comparison of the TFT width over length (W/L) ratio and the drain current ratio.

TFT Dimension (W/L)	**W/L Ratio**	**TFT Dimension Ratio**	**Measure of I_{DS} at V_{DS} = 1.5 V and V_{GS} = 2.0 V**	**I_{DS} Ratio**
100/23	4.35	reference = 1	9.96×10^{-9}	1
200/23	8.7	2	1.97×10^{-8}	2

Figure 4.4 clearly illustrates that as the W/L ratio goes up, the drain current goes up accordingly. Table 4.1 presents the numerical comparison of TFT dimension ratio with I_{DS} ratio, which demonstrates the dependence of I_{DS} on the transistor dimensions as the TFT W/L ratio increases, I_{DS} increases with the same ratio.

4.2.3 Forward Subthreshold Region

The forward subthreshold equation, Eqn. (3.18), of the a-Si:H TFT consists of two regions of operation: the saturation region and the triode region. Which of these regions the TFT operates in depends on V_{DS}. As illustrated in Figure 4.2, in the saturation region, the current is nearly independent of V_{DS}, whereas in the triode region, the current depends on V_{DS}.

4.2.3.1 Subthreshold Saturation Region

In order to build an empirical model for the subthreshold saturation region, we need to find the subthreshold slope first. The forward subthreshold slope, S_f, is an important characteristic parameter. One way of computing S_f is to measure the slope of the log-linear plot of I_{DS} versus V_{GS} when the TFT operates in the forward subthreshold region. The inverse forward subthreshold slope ($1/S_f$) is defined as

$$\frac{1}{S_f} = \frac{d \log_{10} I_{DS}}{dV_{GS}} = \left(\log_{10} e\right)\left(\frac{\Delta I_{DS}}{\Delta V_{GS}}\right). \tag{4.1}$$

Another way to write S is

$$\frac{1}{S_f} = \frac{\ln I_{DS} - \ln I'_{sub0}}{V_{GS} - V_{TS}}, \tag{4.2}$$

where

$$I'_{sub0} = I_{sub0}\frac{W}{L}. \tag{4.3}$$

Rearranging Eqn. (4.2), the empirical equation for the saturation region can be derived as

$$\ln I_{DS} = \frac{V_{GS} - V_{TS}}{S_f} + \ln I'_{sub0}. \tag{4.4}$$

By taking the exponential on both side of Eqn. (4.4) and rearranging, the empirical I_{DS} equation is obtained as

$$I_{DS,fs\_Sat} = I'_{sub0} \exp\left(\frac{V_{GS} - V_{TS}}{S_f}\right) = I_{sub0} \frac{W}{L} \exp\left(\frac{V_{GS} - V_{TS}}{S_f}\right), \tag{4.5}$$

which is same as the subthreshold saturation equation mentioned in Eqn. (3.19).

Figure 4.5 depicts the comparison of the model with experimental data for the subthreshold saturation region. The forward subthreshold slope was extracted to be 0.47 V/decade, which is a typical value for a TFT subthreshold slope. Good agreement between modeling and experimental results is obtained, and the discrepancy is less than 5%.

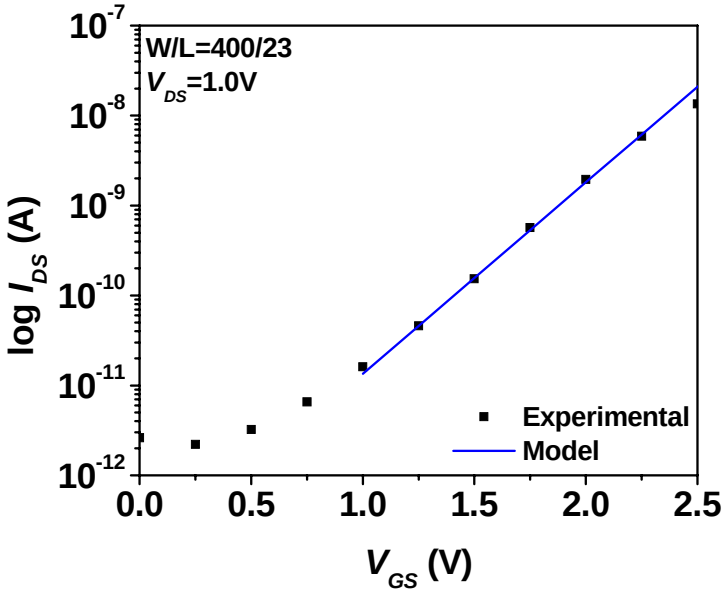


Figure 4.5. Comparison between modeling and experimental data for the subthreshold saturation region.

4.2.3.2 Subthreshold Triode Region

From Figure 4.2, as V_{DS} decreases to below 1 V and enters into the subthreshold triode region, I_{DS} begins to decrease exponentially. This phenomenon can be modeled by Matlab and trial and error. I_{DS} at V_{DS} = 1 V has the same value as I_{DS} in the saturation region. As a result, I_{DS} in the triode region should include the I_{DS} equation in saturation region and can be written as

$$I_{DS,\,fs\_Triode} = I_{sub0}\frac{W}{L}\exp\left(\frac{V_{GS}-V_{TS}}{S_f}\right)\times X\ . \tag{4.6}$$

Since I_{DS,fs_Triode} is an exponential function and the forward subthreshold slope is the same in the triode region as in the saturation region, X can be solved by Matlab. The Matlab code is provided in Appendix B. Figure 4.6 shows graphs of solving X by the trial and error approach, and Figure 4.6c) matches with the exponential curve of the triode region in Figure 4.2. Therefore X is

$$X = 1-\exp\left(\frac{-V_{DS}}{S_f}\right), \tag{4.7}$$

and the drain current in the subthreshold triode region is

$$I_{DS,Triode} = I_{sub0}\frac{W}{L}\exp\left(\frac{V_{GS}-V_{TS}}{S_f}\right)\left(1-\exp\left(\frac{-V_{DS}}{S_f}\right)\right), \tag{4.8}$$

which is same as Eqn. (3.20). The comparison between the model and experimental data (with V_{GS} = 2 V) for the subthreshold triode region is illustrated in Figure 4.7. Good agreement between modeling and experimental results is obtained, and the discrepancy is less than 5%.

Figure 4.8 shows a family of curves measured from the same TFT with V_{GS} ranging from 0.5 V to 10 V. From 0.5 V to 2.5 V, the TFT is in the forward subthreshold region, and I_{DS} is independent of V_{GS}. In these curves, the transition point from the subthreshold linear region to the

subthreshold saturation region occurs around V_{DS} = 1 V. As V_{GS} increases above 2.5 V (> V_T), the TFT enters the above-threshold region where I_{DS} is dependent on V_{DS}.

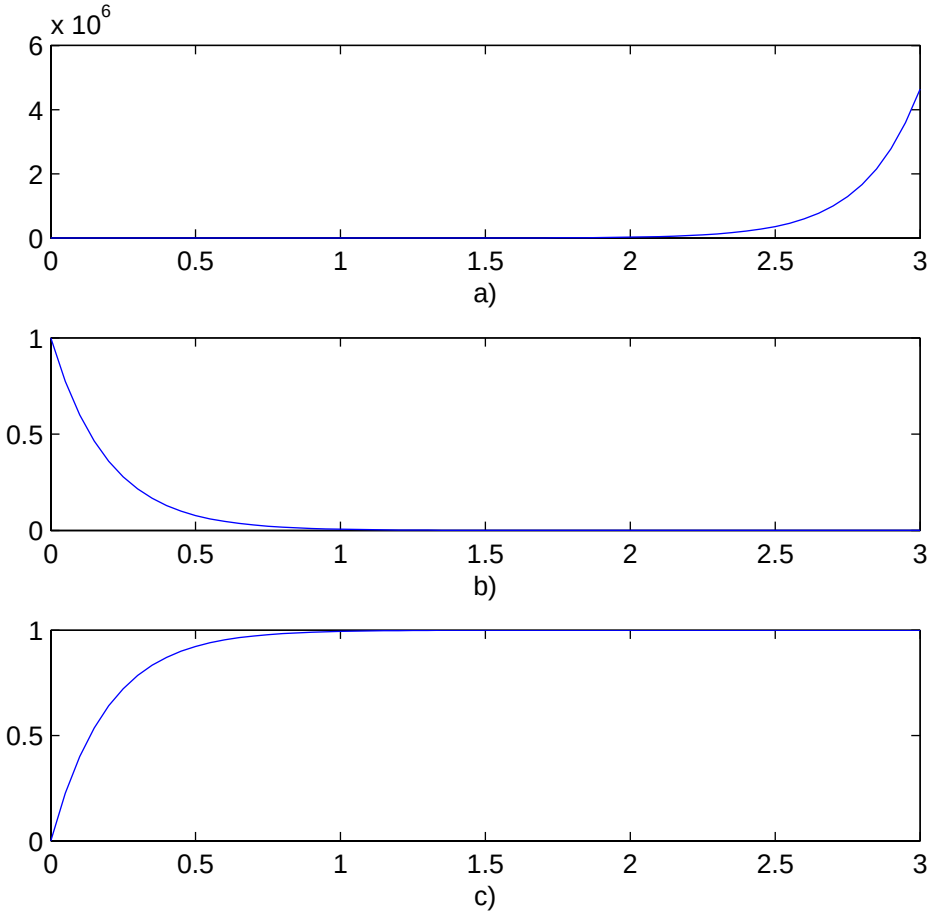


Figure 4.6. Curve fitting by Matlab for solving X term in the subthreshold triode region, a) X = $\exp(V_{DS} / S_f)$, b) $X = \exp(-V_{DS} / S_f)$, and c) $X = 1 - \exp(-V_{DS} / S_f)$.

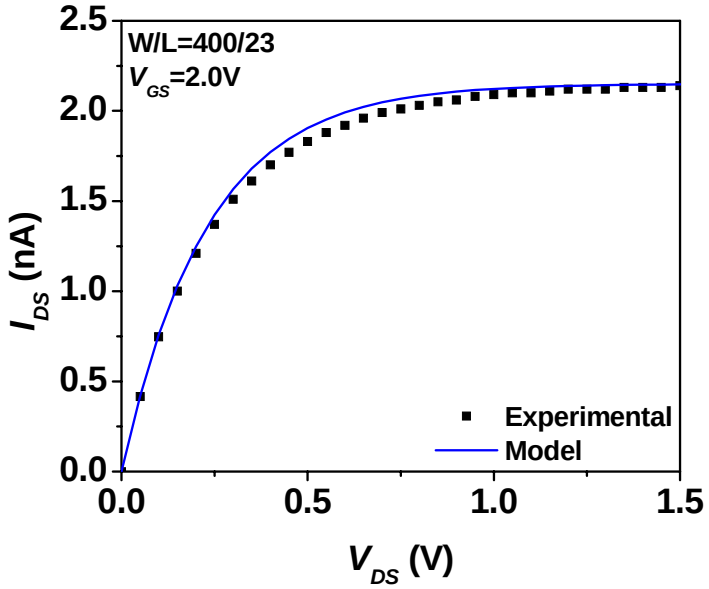


Figure 4.7. Comparison between modeling and experimental data for the subthreshold triode region.

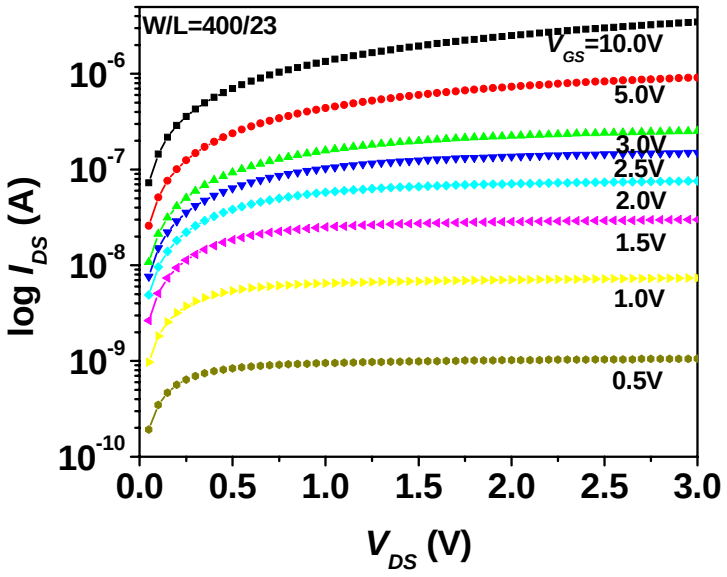


Figure 4.8. I_{DS} as a function of V_{DS} for different V_{GS} value.

4.3 Dynamic Experiments of I-V Characteristics

In this section, we need to examine dynamic characteristics in the forward subthreshold region. We first need to investigate two metastabilities, subthreshold slope and V_T shift, in the presence of constant voltage stress. The constant voltage stress experiments were carried out to gain an understanding of the dynamic characteristics of these two metastabilities. We then observe the effect of constant voltage stress on TFT in the subthreshold saturation region and subthreshold triode region, respectively.

4.3.1 Constant Voltage Stress

The simplest pixel circuit for AMOLED displays consists of 2 TFT transistors (2T circuit) as illustrated in Figure 4.9 [29]. During the programming cycle, the switching TFT (T1) is on and the data voltage is written from the data line into the pixel. As a result, the driver TFT (T2) forces a current through the OLED, which is determined by the data voltage and the characteristic parameters of T2. When T1 is turned off, the same voltage is kept by the pixel capacitance (C_P), so the voltage remains on the gate of T2 to maintain the same current flow through the OLED. Therefore, T2 is under a constant voltage stress in this circuit. The long-term bias stress causes T2 to experience a V_T shift. Since the current through the OLED depends on V_{GS} of T2, this circuit is vulnerable to any V_T increase in the TFT. The increase of V_T results in a gradual decrease of the OLED brightness, and the pixel eventually turns off. High voltage stress also causes the subthreshold slope to change, and the subthreshold slope shift degrades the current driving capability of T2. Hence, the subthreshold slope shift and V_T shift under constant voltage stress are discussed in this section.

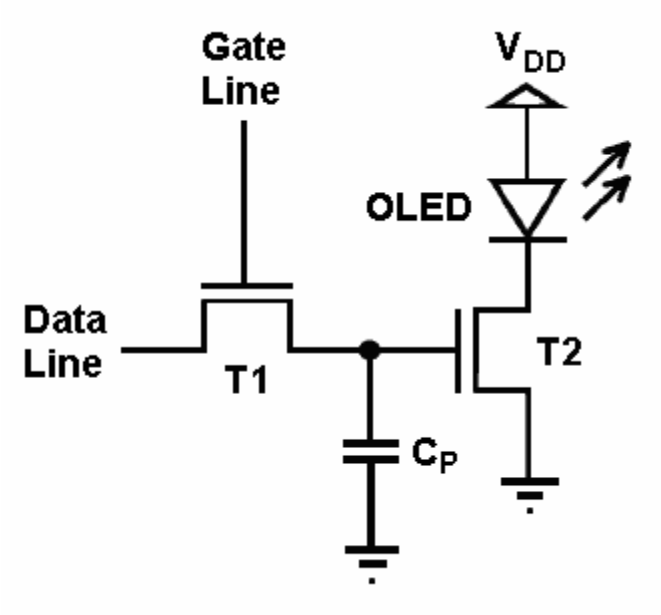


Figure 4.9. Schematic of a simple AMOLED pixel drive.

Two 12-hour constant voltage stress experiments were performed for the purpose of observing the subthreshold slope shift and V_T shift. In the first bias stress test, V_{GS} was fixed at 20 V, and V_{DS} was fixed at 0 V. In the second bias stress test, V_{GS} was set to 50 V, and V_{DS} was kept at 0 V. At every 2-hour interval, a quick V_{GS} sweep in the saturation region was executed to measure the transfer characteristics of the TFT. During the sweep, V_{DS} was set to 15 V and V_{GS} was swept from -5 V to 15 V with a step size of 0.5 V.

4.3.1.1 Subthreshold Slope Shift

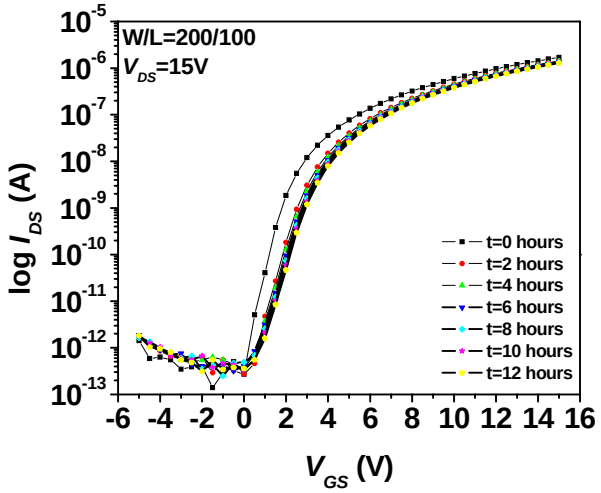
The subthreshold slope of the TFT is affected by the gate bias stress. The subthreshold slope increases with stress voltage and stress time [30], [31]. The degradation can be explained by the defect pool model. As explained by Powell [23], the subthreshold slope shift is attributed to the creation of defect states in the upper part of the band gap. The degradation for the negative bias stress is much more severe than that for the positive bias. For the negative bias, the newly created states can

contribute to the increase of the state density near the conduction band. According to the defect pool model, when a negative voltage bias is applied, the bands bend upwards and the Fermi level goes toward the valence band. This displacement of the Fermi level creates more states in the upper part of the band gap and as a result, aggravates the subthreshold slope shift even further.

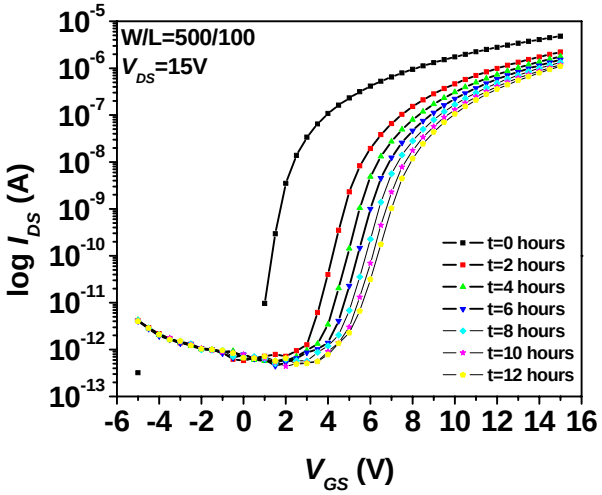
Since we are interested in the forward subthreshold region, which is above zero gate voltage, we will focus on the positive bias. For the positive bias stress, the subthreshold slope shift is negligible below 20 V since the positive bias helps to remove some of the created states in the upper part of the band gap. However, for bias above 20 V, a mild increase of subthreshold slope is observed. Figure 4.10 depicts the subthreshold slope shift for 20 V and 50 V bias stresses, and the subthreshold slope shift as a function of positive stress voltage with different stress time is illustrated in Figure 4.11.

The obtained experimental result contradicts Powell's conclusion. Powell believed that there was no change in the subthreshold slope after positive bias stress [23]. On the other hand, Tai et al. observed outcomes similar to those represented in Figure 4.11 [30], [31]. Based on their experimental results, they believed that at the high positive gate bias stress, the state creation near the conduction band prevailed over the removal of these states [30], [31]. We believe that bulk charge traps in the a-SiN_x:H layer are the cause of the subthreshold slope shift under the high positive bias stress. Our theory is proved in two steps. First, according to the defect pool model, the charge trapping mechanism becomes significant at higher voltages, usually above 25 V. Hence, at 50 V bias stress, the interfacial and bulk charge trapping are the dominant mechanisms. In the subthreshold slope equation, the interface states due to the interfacial charge trapping are already included; however, no previous models consider the bulk charge trapping states. Second, the TFT was annealed after the 50 V stress test, and its V_T was measured. By comparing with the initial V_T, we found there was small V_T shift existed after the annealing process, which we believed a permanent V_T

shift. This permanent V_T shift is due to the bulk charge trapping states in the a-SiN_x:H layer since these states can be hardly removed by the annealing process.



a)



b)

Figure 4.10. The change of Subthreshold slope in the presence of a) 20 V bias stress, b) 50 V bias stress.

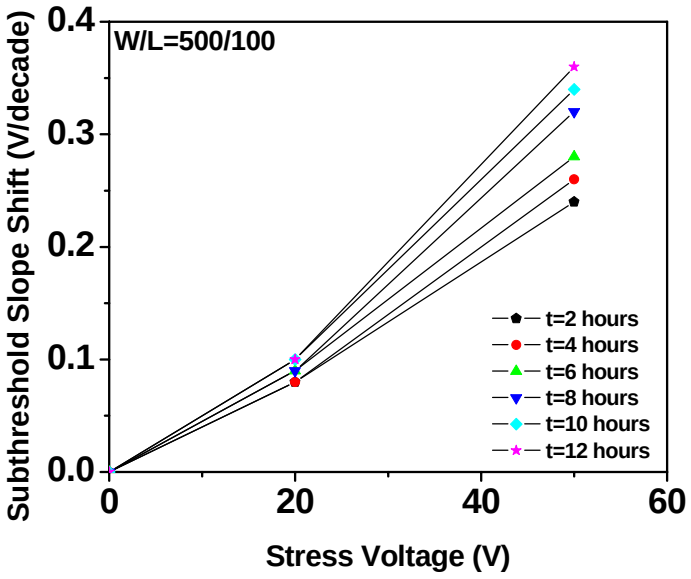
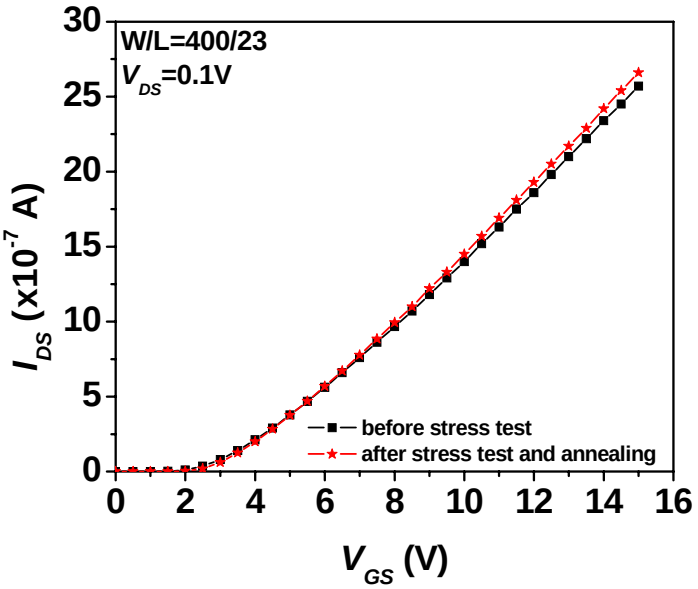


Figure 4.11. Subthreshold slope shift as a function of positive stress voltage for different stress times.

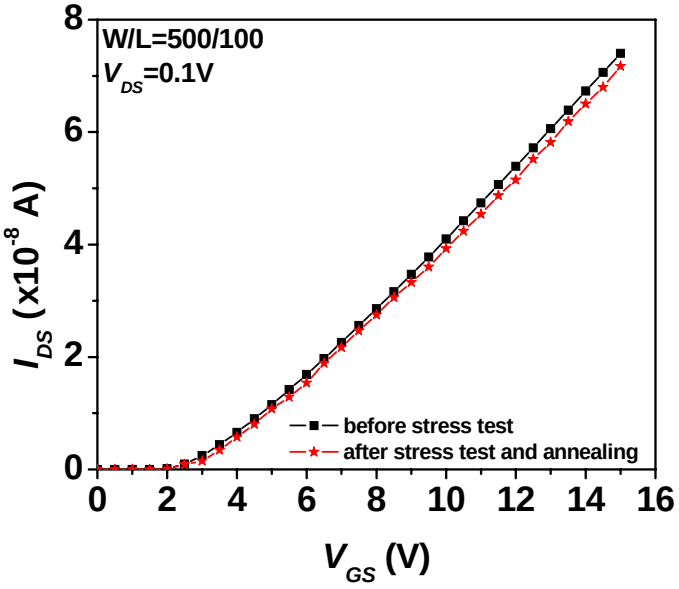
Therefore, by including the bulk charge trapping states, we can modify the forward subthreshold slope of Eqn. (3.14) as

$$S_f = \left(1 + \frac{C_{ssf}}{C_i} + \frac{C_{sd}}{C_i} + \frac{C_{sb}}{C_i}\right) V_{th}, \tag{4.9}$$

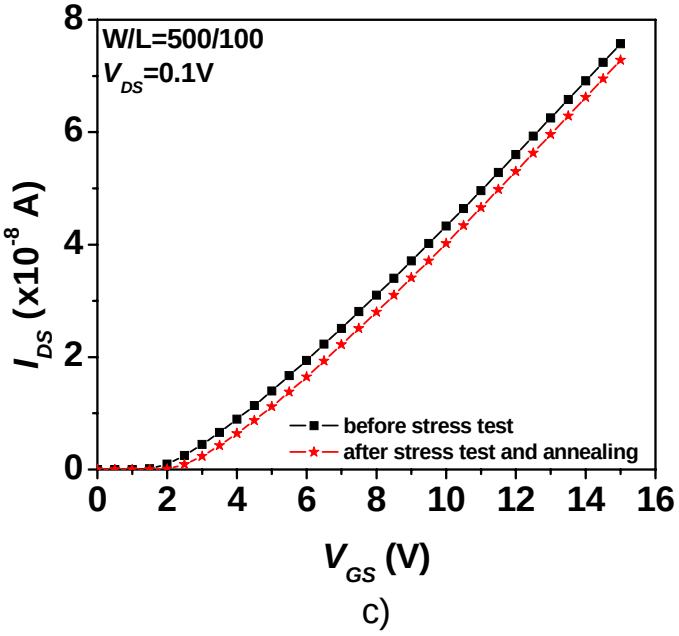
where C_{sb} is the effective capacitance of bulk charge trapping states in the a-SiN_x:H layer. Figure 4.12 shows comparisons of annealed threshold voltages before and after 12-hour stress tests for 10V, 20 V and 50 V gate bias. After the 10 V gate voltage stress test, the TFT returns to its original V_T value by the annealing process. Annealing of the second TFT after the 20 V gate bias stress gives similar observation. However, the comparison of annealed V_T before and after the 50 V bias stress confirms an approximately 0.5 V permanent V_T shift. Nevertheless, since the subthreshold slope shift is negligible for a below 20 V bias stress, the subthreshold slope shift can be neglected in the forward subthreshold operation and will be verified by experimental results in Section 4.3.2.


W/L=400/23
V_{DS}=0.1V
I_{DS} (x10^{-7} A)
V_{GS} (V)
before stress test
after stress test and annealing

a)


W/L=500/100
V_{DS}=0.1V
I_{DS} (x10^{-8} A)
V_{GS} (V)
before stress test
after stress test and annealing

b)



c)

Figure 4.12. Comparison of annealed V_T before and after 12-hour stress tests for a) 10 V bias stress, b) 20 V bias stress, c) 50 V bias stress.

4.3.1.2 V_T shift

As mentioned in Chapter 2, two metastability mechanisms, namely charge trapping and defect state creation, cause V_T to shift in TFT. As stated by Powell's experimental results, defect state creation dominated for gate biases less than 25 V and charge trapping became significant at higher gate voltages. The critical voltage at which charge trapping overtakes defect state creation depends on the band gap of the silicon nitride.

Defect state creation is characterized by a power law dependence on the V_T shift over time. As indicated by Powell, the V_T shift over time can be defined as

$$\Delta V_T(t) = A\left(V_{ST} - V_{Ti}\right)^{\alpha} t^{\beta}, \tag{4.10}$$

where A is the temperature dependent parameter, V_{ST} is the stress voltage at TFT gate, V_{Ti} is the initial V_T, α is the power parameter and is a unity value for the defect state creation mechanism, t is the bias stress time duration, and β represents the temperature dependence of the V_T shift. Figure 4.13 illustrates the V_T shift with respect to time for a 12-hour, 20 V constant gate bias stress test. Good agreement between Eqn. (4.10) and experimental results is obtained for A = 0.044 and β = 0.27. The values of A and β are extracted by MAPLE software.

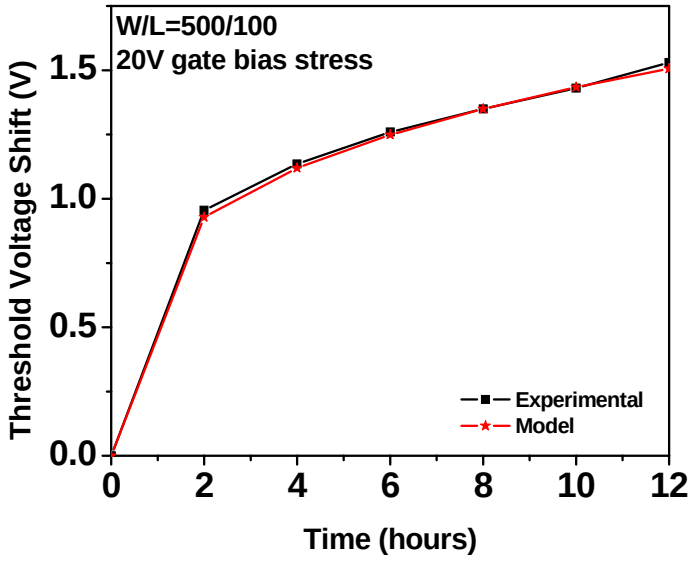


Figure 4.13. V_T shift as a function of stress time for a 12-hour, 20 V constant voltage stress test.

Charge trapping is associated with a logarithmic time dependence, which can be represented as

$$\Delta V_T(t) = r_d \log\left(1 + \frac{t}{t_0}\right). \tag{4.11}$$

Here, r_d is a constant, and t_0 is some characteristic value of time. Figure 4.14 depicts the V_T shift as a function of stress time for a 12-hour, 20 V constant bias stress test. Clearly, the V_T shift is more

severe at the high constant gate bias stress. The experimental results are consistent with Eqn. (4.11), and r_d and t_0 are extracted by MAPLE to be 3.35 and 0.16, respectively.

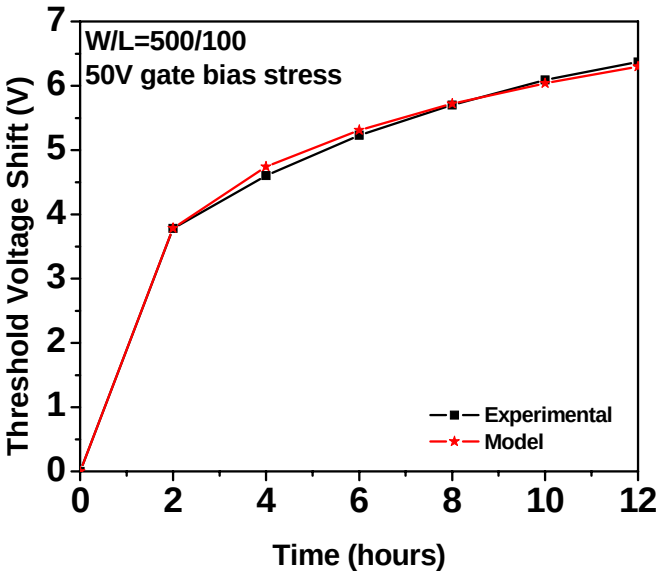


Figure 4.14. V_T shift as a function of stress time for a 12-hour, 50 V constant voltage stress test.

Given the effect of bulk charge trapping on the subthreshold characteristics of a-Si:H TFTs, the threshold voltage model as defined in Eqn. (3.22) may be modified to include the effect of bulk charge trapping as

$$V_T = V_{FB} - \frac{Q_i}{C_i} + \psi_{ST} + \left(\frac{C_{ssf} + C_{sb}}{C_i}\right)\left(\psi_{ST} - \psi_{Sf0}\right) + \frac{C_{sd}}{C_i}\left(\psi_{ST} + V_{nd}\right). \tag{4.12}$$

4.3.2 Forward Subthreshold Region

As mentioned in Chapter 3, we need to verify the subthreshold slope shift and V_T shift in the forward subthreshold regions of operation. The forward subthreshold region of operation

encompasses two operations: the saturation region and triode region. We first examine the saturation region, then the triode region. Constant voltage stress experiments in the subthreshold regions were carried out.

4.3.2.1 Subthreshold Saturation Region

The subthreshold saturation region is defined as $V_{GS} < V_{DS} < V_T$ and $V_{DS} > 1$ V. Hence, during the constant voltage stress test, V_{DS} was set to 2 V, and V_{GS} was set to 0.5 V. A 50-hour voltage stress experiment was performed. At every 10-hour interval, a quick V_{GS} sweep in the linear region was executed to measure the transfer characteristics of the TFT. During the sweep, V_{DS} was set to 1 V and V_{GS} was swept from -5 V to 10 V with a step size of 0.5 V. Figure 4.15 illustrates the subthreshold slope characteristics under 50-hour constant voltage stress in the subthreshold saturation region. Figure 4.16 depicts the threshold voltage variation for the same stress test. From the graph, no visible subthreshold slope shift or V_T shift is found.

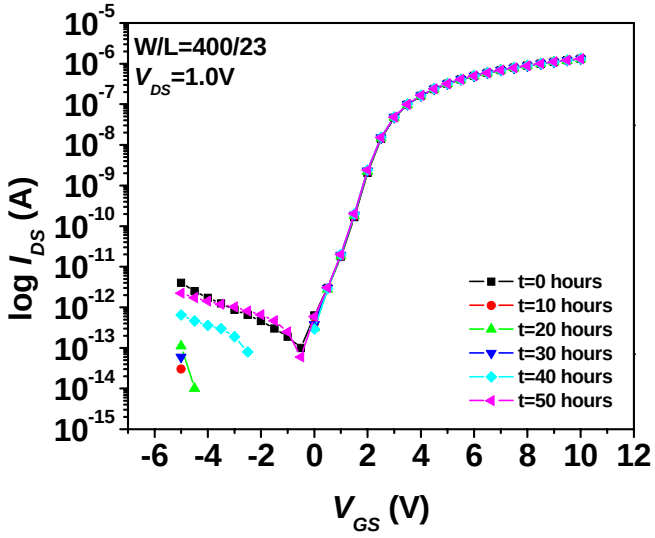


Figure 4.15. Subthreshold slope characteristics under a 50-hour constant voltage stress in the subthreshold saturation region.

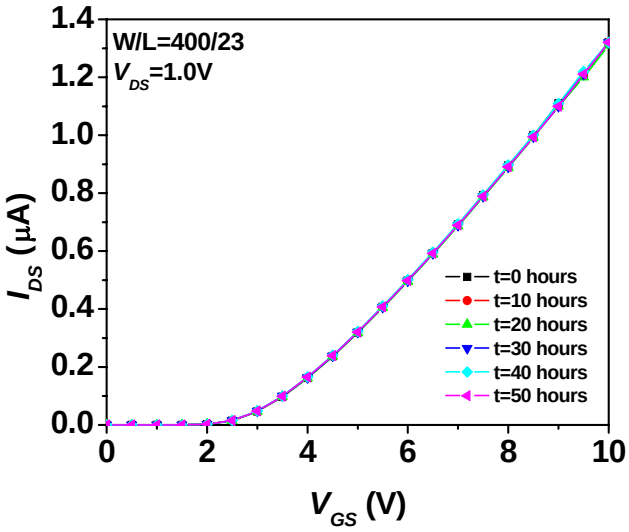


Figure 4.16. Threshold voltage characteristics under a 50-hour constant voltage stress in the subthreshold saturation region.

4.3.2.2 Subthreshold Triode Region

The constant voltage stress test for the subthreshold triode region of operation is similar to the saturation one. In this test, since the subthreshold triode region is defined as $V_{DS} < V_{GS} < V_T$ and $V_{DS} <$ 1 V. Therefore, for the constant voltage stress test, V_{DS} was set to 0.5 V, and V_{GS} was set to 1 V. The stress duration was 50 hours as well, and a V_{GS} sweep was performed at every 10-hour interval. During the sweep, V_{DS} was set to 1 V, and V_{GS} was sweep from -5 V to 10 V with a step size of 0.5 V. From Figure 4.17 and Figure 4.18, neither a noticeable subthreshold slope shift nor V_T shift is found.

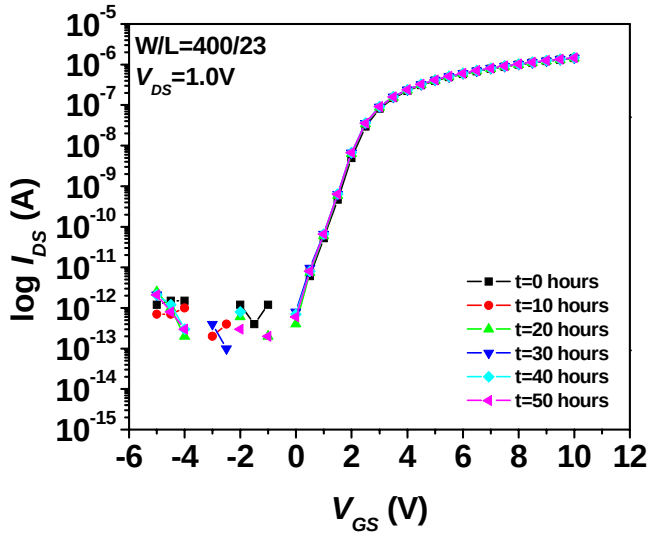


Figure 4.17. Subthreshold slope characteristics under a 50-hour constant voltage stress in the subthreshold triode region.

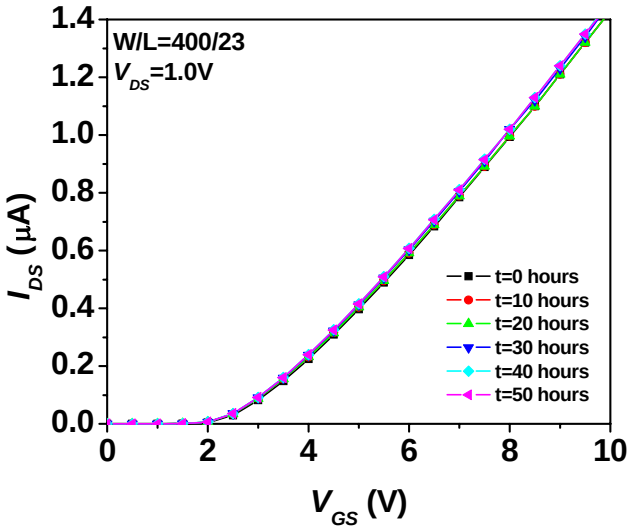


Figure 4.18. Threshold voltage characteristics under a 50-hour constant voltage stress in the subthreshold triode region.

Chapter 5

Current Mirror Circuit Application

As discussed in Chapter 3, the gate of the driver TFT of the 2T pixel circuit is subjected to a constant voltage stress, thereby causing the shift of V_T in that TFT. To overcome the V_T shift, a current mirror based current-programmed pixel circuit is often used in the AMOLED circuitry. The current mirror consists of two identical transistors whose gates are connected as shown in Figure 5.1 [32]. The input transistor T1 is diode-connected as the drain is shorted to the gate to convert the input current to a voltage at the gate. The output transistor T2 can theoretically supply the same current as the input current because both transistors have the same gate voltage. Accurate current mirroring takes place only when T2 remains in the saturation region because T1 is always in saturation since its gate and drain are diode-connected. As long as the V_T of both transistors is the same or increases by the same amount, the operation of a current mirror is independent of any V_T shift. Therefore, the OLED current in these circuits should be independent of any V_T shift in the driver TFT as long as it stays in the saturation region of operation.

A current-programmed OLED pixel circuit based on the current mirror circuit family was introduced in recent years [33]. Figure 5.2 depicts the schematic of a current-programmed pixel circuit [29], [33]. The driver TFT of this pixel circuit is subject to a constant current stress instead of a voltage stress as in the simple pixel driver circuit in Figure 4.9. However, just like the voltage

stress, the current stress also induces V_T shift. Since there is no visible V_T shift in the TFT subthreshold operation, it is advantageous to design a current-programmed pixel circuit in the forward subthreshold region.

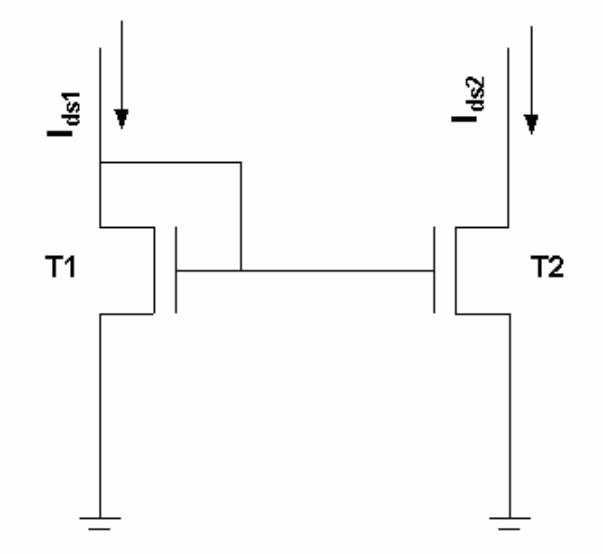


Figure 5.1. Schematic of a simple current mirror.

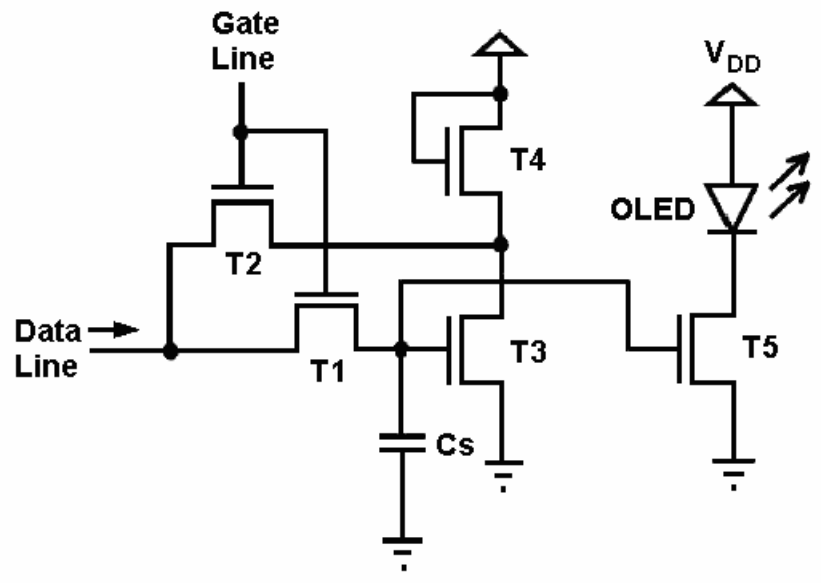


Figure 5.2. Schematic of a current-programmed pixel circuit.

5.1 Current Mirror Matching Experiments

Two static experiments on a TFT current mirror circuit were performed. The layout of current mirror circuits is given in Appendix C. The first experiment consisted of a static measurement, of a current mirror on a die, using a probe station. The second experiment was a static measurement of the same current mirror, but from a packaged die and measured by SMUs.

The simple Wilson current mirror as shown in Figure 5.1 was used in both experiments. The transistors T1 and T2 are the same dimension: 65/23; hence, the current ratio is 1:1. The extracted V_T is approximately 2.5 V for T1 and T2, respectively.

In the first experiment, the input current I_{DS1} was swept from 0 to 1 nA, V_{DS} of T2 (V_{DS2}) was swept from 2 V to 5 V, and the output current I_{DS2} was measured. A comparison of I_{DS1} (reference) and I_{DS2} is illustrated in Figure 5.3. As the value of V_{DS2} increases, I_{DS2} increases accordingly. For V_{DS2} = 4.5 V, I_{DS2} matches approximately with I_{DS1} from 0 A to 0.4 nA. At I_{DS1} = 0.4 nA, V_{GS2} value corresponds to 2.43 V, which is below the V_T value of T2. This observation shows a relatively good current matching characteristic in the forward subthreshold operation of a current mirror on a die.

In the second experiment, the same current mirror design on a die bonded to a dual-in-line package was used. The packaged die was placed in the Keithley 236 choke and measured by SMUs. I_{DS1} was swept from 0 to 1 nA as well, V_{DS2} was swept from 1 V to 4 V, and the output current I_{DS2} was measured. A comparison of I_{DS1} and I_{DS2} is illustrated in Figure 5.4, and a large discrepancy between the reference line and I_{DS2} current lines is observed. However, for V_{DS2} = 4 V, the I_{DS2} current line is approximately parallel to the reference line starting from I_{DS1} = 0.4 nA. This remark might demonstrate that a current matching could happen at a higher I_{DS1} value with a constant offset. The constant offset or discrepancy might be due to the bonding from the die to pins on the dual-in-line package, resulting in an increase of leakage current.

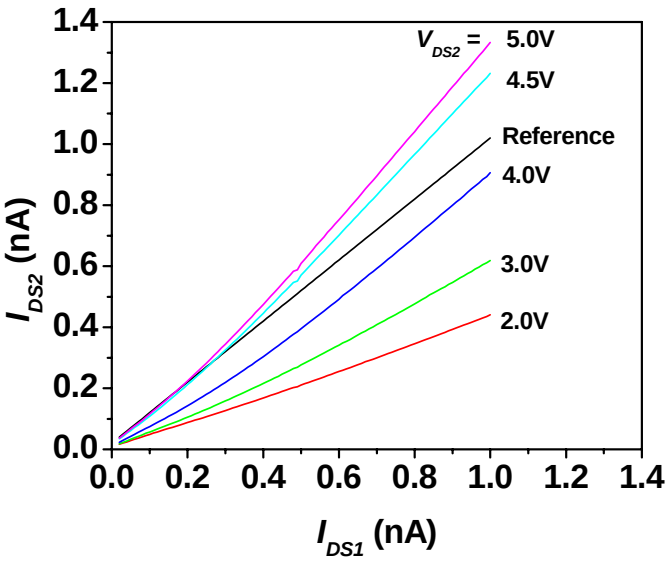


Figure 5.3. I_{DS1} versus I_{DS2} of the current mirror (65/23|65/23) on a die.

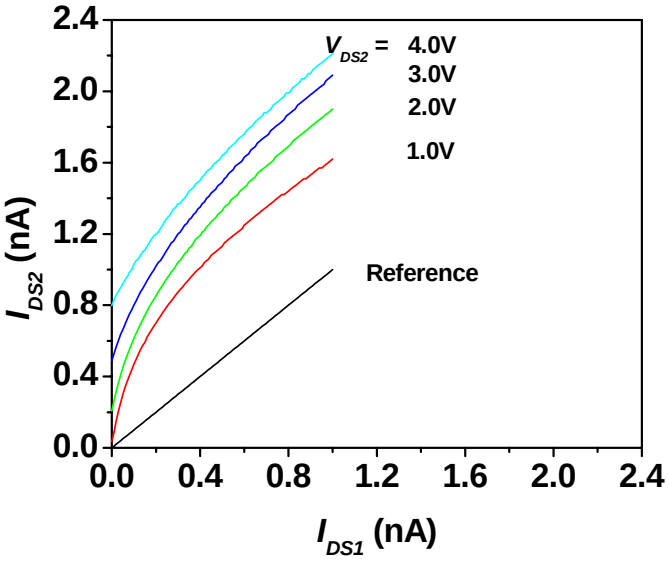


Figure 5.4. I_{DS1} versus I_{DS2} of the current mirror (65/23|65/23) on a packaged die.

5.2 Discussion

From the current mirror matching experiments, the single stage TFT current mirror on a die demonstrated a good current matching characteristic in the forward subthreshold operation. The same experimental procedures were repeated on two other current mirrors, and they both displayed results similar to what was shown in Figure 5.3. However, the current mirror measurement from the packaged die did not show a good matching capability. This result was verified again on two current mirrors from a different packaged die, and we observed similar constant offsets between the I_{DS2} current line and the reference line.

Due to the low subthreshold current and geometry mismatch, current mirror operation in the forward subthreshold region can be a challenge. Designing large dimensional TFT current mirrors are suggested to reduce the geometry mismatch. The widths of T1 and T2 are recommended to exceed 100 μm. Currently, several large dimensional TFT current mirrors are under design, and they will be used to verify the above recommendation.

Since the current mirrors under test are all single stage current mirrors, we need to investigate the current matching characteristics of multistage current mirrors.

Chapter 6

Conclusion

In recent years, AMOLED displays are achieving more popularity than any other display technology. AMOLED display pixel circuits require operation of TFTs in mixed digital and analog operation. However, a-Si:H TFTs exhibit a bias induced metastability phenomena. Both the threshold voltage and the subthreshold slope change over time in the presence of a gate bias. The bias induced metastability problems seriously limit a-Si:H TFT application and jeopardize the long-term performance of AMOLED display pixel circuits. These pixel circuits often require complicated V_T shift compensating circuits, thereby increasing cost and complexity. Therefore, other alternatives such as TFT operations in the subthreshold region are of great interest. Since the current in the subthreshold region is very low and in the range of nA, which is approximately 3 orders below the above-threshold current, people have little interest in studying and modeling this region.

This thesis examined the device modeling of a-Si:H TFT in the forward subthreshold operation. The ability to accurately predict the I-V characteristics of a-Si:H TFTs in the forward subthreshold operation is the starting point for designing circuits in this region.

a-Si:H forward subthreshold operation demonstrates several advantages for circuit design. First, it has an exponential characteristic similar to what bipolar junction transistors (BJTs) provide, TFT circuit designs requiring the exponential current output could benefit from this characteristic.

Second, the typical power consumptions are in the order of nano-watts, which lead to design of very low power dissipation circuits. Third, since the operation is below V_T, the effect of metastability problems can be minimized.

The detailed analysis and derivation of the forward subthreshold static models were presented. Two sub-regions in the forward subthreshold region were identified: the saturation region and the triode region. Their I-V characteristics were studied, and the current equations for each region were derived. The dynamic characteristics were also examined. Dynamic models were provided for the subthreshold slope shift and V_T shift in the forward subthreshold region.

Static and dynamic experiments were performed to verify our theoretical models. Good agreement between modeling and experimental results were obtained, and the discrepancy was less than 5%. Based on the experimental data, the empirical model equations were also obtained, and they were identical to the theoretical ones. High gate bias stress experiments were conducted in order to study the characteristics of the subthreshold slope degradation and V_T shift. The metastability phenomena due to the effect of bulk charge traps were observed. As a result, new subthreshold slope and V_T equations are constructed by taking these bulk charge trapping states into consideration. Although the existence of charge trapping states and defect states could still induce metastability phenomena in the subthreshold region, no visible subthreshold slope shift or V_T shift were observed in the 50-hour constant gate bias stress experiments. Thus, the charge trapping states and defect states were considered relatively small and could not trigger any metastable effect in the forward subthreshold operation.

The a-Si:H TFT current mirror circuit application in the forward subthreshold operation were studied. The fidelity of current matching was examined. We found that the single stage TFT current mirror on a die demonstrated a good current matching characteristic in the forward subthreshold operation. However, the current mirror measurement from the packaged die did not show a good

matching capability. Due to a low subthreshold current and geometry mismatch, operating a current mirror in the forward subthreshold region can be a challenge. Therefore, designing large dimension TFT current mirrors are recommended in order to reduce geometry mismatch.

Appendix A

Layout of Single TFTs with Different Dimensions

- Die name: MULTIPROJ_AFRIN
- Designer: Afrin Sultana
- General purpose: To determine dependence of threshold voltage shift on TFT length, width or geometry.
- Total number of TFTs: 15 TFTs

TFT no.	Width (μm)	Length (μm)	Geometry
10	46	23	Conventional
1	100	23	Conventional
2	200	23	Conventional
5	400	23	Conventional
13	500	23	Conventional
14	1000	23	Conventional
15	100	100	Conventional
9	200	100	Conventional
8	500	100	Conventional
7	200	200	Conventional
12	400	200	Conventional
11	500	200	Conventional
6	1000	200	Conventional
4	200	23	Meander
3	200	23	Circular

- Picture of the die in .jpeg format:

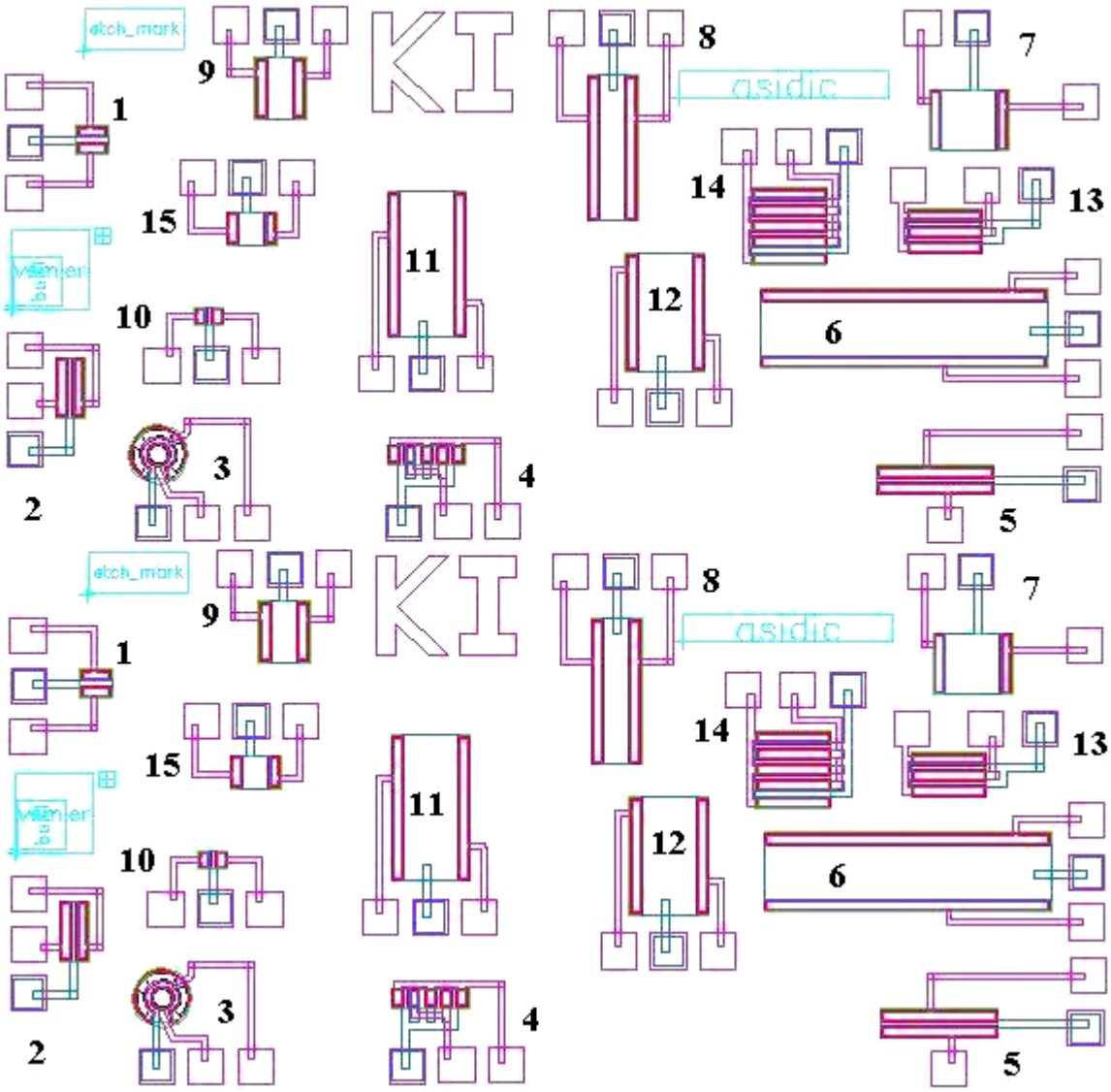


Figure A.1. Cadence layout of single TFTs with different dimensions.

Appendix B

MATLAB Program for Curve Fitting

```
% finding X term in IDS equation of the subthreshold triode region
clear;
VDS=[0 0.05 0.1 0.15 0.2 0.25 0.3 0.35 0.4 0.45 0.5 0.55 0.6 0.65 0.7 0.75 0.8 0.85 0.9 0.95 1 1.05
1.1 1.15 1.2 1.25 1.3 1.35 1.4 1.45 1.5 1.55 1.6 1.65 1.7 1.75 1.8 1.85 1.9 1.95 2 2.05 2.1 2.15 2.2
2.25 2.3 2.35 2.4 2.45 2.5 2.55 2.6 2.65 2.7 2.75 2.8 2.85 2.9 2.95 3];

%forward subthreshold slope
S_f=0.45;

%log factor, since S_f is obtained from a semi-log graph, therefore its
%value needs to be converted.
log_factor=1/log10(exp(1));

%obtain the right S_f by dividing S_f by log_factor
S_f_1=S_f/log_factor;

%curve fitting
%1) it's exponential function in the triode region
%2) it depends on the value to VDS
%3) the subthreshold slope is the same in the triode region as in the
%saturation region, therefore, VDS/S_f
%from 1) to 3), we can obtain exp(VDS/S_f_1)
IDS1=exp(VDS/S_f_1);
IDS2=exp(-VDS/S_f_1);
IDS3=1-exp(-VDS/S_f_1);
subplot(3,1,1),plot(VDS,IDS1),XLABEL('a)');
subplot(3,1,2),plot(VDS,IDS2),XLABEL('b)');
subplot(3,1,3),plot(VDS,IDS3),XLABEL('c)');
```

Appendix C

Layout of TFT Current Mirrors

- Die name: 03SANJIV_B
- Designer: Sanjiv Sambandan
- General purpose: To study current sources (especially how to compensate current mismatch in current mirrors).
- Total number of TFTs: 52 TFTs, 23 Circuit Components

Circuit	Description
C1	Wilson current mirror-65/23|65/23
C2	Wilson current mirror-130/23|65/46
C3	Wilson current mirror-65/23|65/23
C4	Wilson current mirror-65/23|65/23
C5	Wilson current mirror-260/23|65/23
C6	Wilson current mirror-65/23|65/92
C7	Wilson current mirror-65/23|65/23
C8	TFT-260/23
C9	TFT-260/23
C10	TFT-65/23
C11	TFT-65/23
C12	TFT-65/23
C13	Wilson current mirror-260/23|65/23
C14	Wilson current mirror-65/23|65/92
C15	Wilson current mirror-65/23|65/23
C16	Wilson current mirror-65/23|65/23
C17	Wilson current mirror-65/23|260/23
C18	Wilson current mirror-65/23|65/23
C19	Cascode current mirror-5/23|65/23|65/23|65/23

C20	Cascode current mirror-5/46|65/46|65/46|65/46
C21	Cascode current mirror-5/23|65/92|65/23|65/92
C22	Current cmp. Feedback ckt
C23	TFT-65/23

- Picture of the die in .jpeg format:

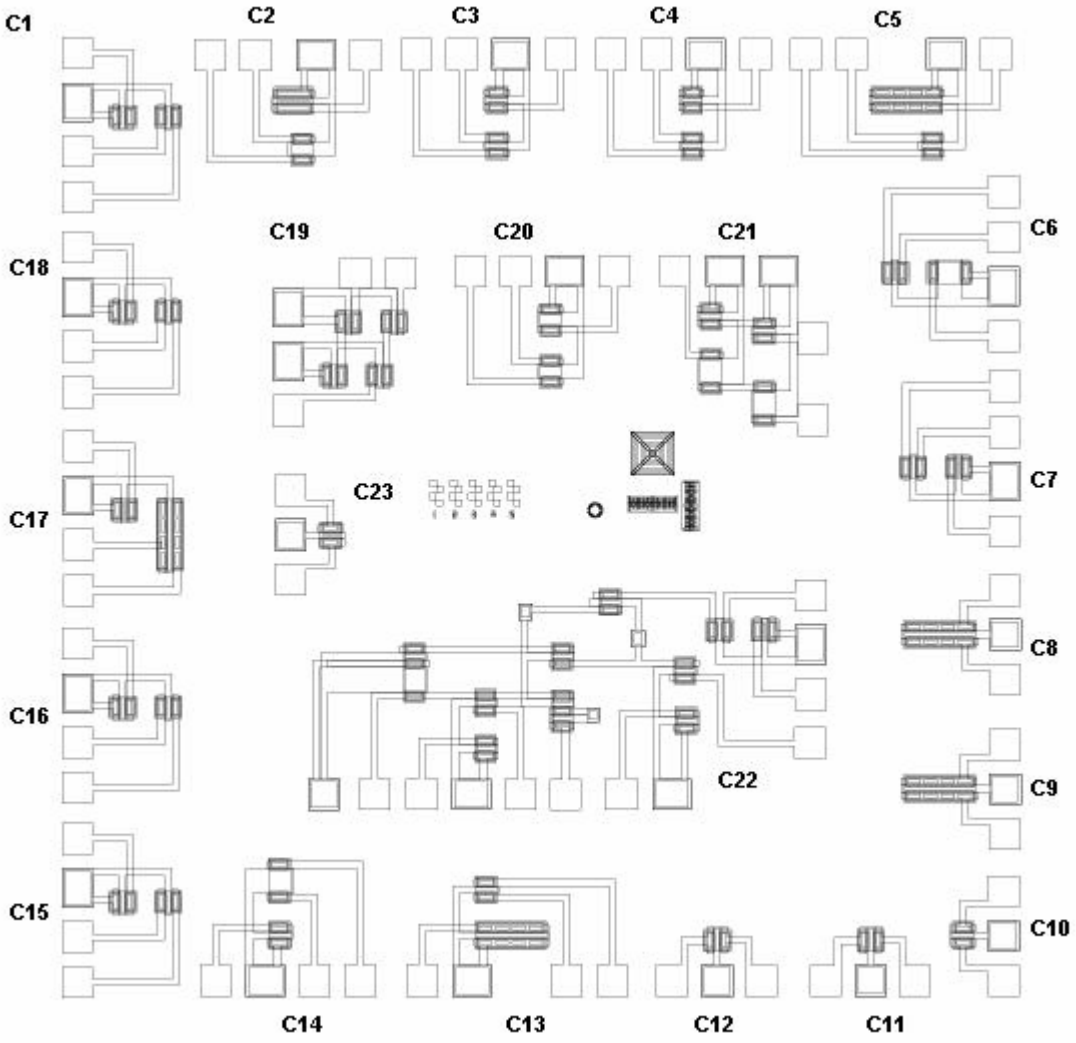


Figure C.1. Cadence layout of different current mirrors.

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