

Design, Fabrication and Validation
of a CMOS-MEMS
Kelvin Probe Force Microscope

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Geoffrey Lee

Abstract

The Kelvin Probe Force Microscope is a type of scanning probe instrument that is used to discern the different work functions of a sample. A sharp probe at the end of a cantilever is lowered onto a substrate where electrostatic forces, caused by the difference in work function cause the cantilever to oscillate at the modulated frequency. Using this instrument, high resolution images can be obtained, mapping the surface electronic characteristics. However, developments of this instrument have generally been limited to obtaining higher resolution images as well as reducing noise in the output, limiting the widespread appeal of this expensive instrument. There exist many applications where extremely cheap, low footprint and easy-to-use Kelvin Probe Force Microscopes would be beneficial.

In order to cheaply produce this microscope in batch, a post-processed CMOS-MEMS device is utilized. The polysilicon resistors act as a strain gauge such that a conventional optical system will not have to be employed. The ability to use integrated bimorph actuators on chip allow for movement of the cantilever without the employment of large piezoelectric stages with creep effects. Embedded electronics can be fabricated with the CMOS process alongside the MEMS device, allowing full integration of an on board amplifier and read out system. In general, a large table top system can be minimized onto the size of a <1 mm² area, a microcontroller and a computer.

In this work, a Kelvin Probe Force Microscope is designed, fabricated and validated. A MEMS device was designed following similar characteristics of a generic cantilever beam. The stiffness, length, resonant frequency, and other tip characteristics can be mimicked with careful design. The resultant designs were fabricated using a CMOS-MEMS process. In order to obtain a sharper tip with modified characteristics, various methods were employed; such as gallium-aluminum alloy tip formation as well as electroless plating onto the tip of the device.

Finally, the resultant device is tested against a sample. It was seen that the MEMS device followed similar characteristics of the conventional microscope itself, validating the equations that define the method. Bimorph actuators were tested to show movement, allowing the integration of the cantilever with the XYZ-stage. Work function changes are observed while scanning different materials.

It is shown throughout the course of this thesis, that a true Kelvin Probe Force Microscope can be designed, fabricated and validated using CMOS-MEMS technology.

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Dedication

For those who have made me who I am today.

For those who will influence me in the future.

And for those who keep pushing onwards.

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1. Introduction

Scanning probe microscopy (SPM) techniques have been an extremely popular characterization technique for various topic areas. A tip attached to a cantilever is dragged across a surface to obtain a topological image. The ability to obtain 3D images of a surface without any depositions during sample preparation allows this technique to preserve all surface characteristics. Atomic resolution of the SPM allows for in depth analysis of a wide range of materials. Altering the SPM technique – such as tracking electrostatic forces or magnetic forces – can provide the user with a range of data, allowing for proper characterization of the sample at hand.

In particular, the Kelvin Probe Force Microscope (KPFM) was developed to map the work function, and therefore, the surface potential of a sample. The KPFM apparatus consists of a conducting cantilever with a tip, a set of piezoelectric stages, a laser, a photodiode and the sample. This set up functions through the use of a controller with a lock-in amplifier to help track a small signal embedded within noise [1].

The increased sophistication of this technique allows for careful monitoring of many materials, such as graphene, in the evolving field of transistor design [2]. It has been recently reported that the KPFM was able to visualize the charge distribution in an atom [3], showing areas of positive and negative charge, similar to theoretical depictions of electron cloud probabilities. Towards the more practical regime, the ability to detect changes in surface potential can be used for failure analysis of transistor devices in processors as well as locally detecting the charge of a species flowing within a liquid sensor [4].

While the apparatus is able to capture high resolution features, miniaturization and integration of scanning arrays would elevate the technique towards industrial testing, in particular, transistor testing of processors. It is projected that the testing of a single transistor within a processor will soon exceed the cost of producing the transistor itself. Other non-linearities of the SPM, such as creep, bowing and hysteresis cause artifacts and other anomalies in the resultant images. This lowers the overall efficacy of the technique.

Micro Electro-Mechanical Systems (MEMS) have shown a great maturation within the past decade. With the advent of multiple MEMS technology, such as the CMOS-MEMS process, MEMS have become much more affordable, while providing the user a multitude of options for device design. Large efforts towards integration and innovation have resulted in large developments to CMOS-MEMS technology, mainly focusing into areas of RF devices [5], as well as system-on-a-chip sensor devices [6].

The CMOS-MEMS process suggests the possibility of realizing a MEMS-based KPFM device with full integration. The advantages offered by using MEMS in a SPM device can be the miniaturization of the conventional instrument [7]. All of the features contained within the instrument can be miniaturized to an area smaller than 1 mm^2 . The large components within the conventional SPM device can be replicated within the MEMS device. The piezoelectric stage components can be replaced with MEMS actuators, and the optical sensing mechanism can be replaced with a piezoresistive strain gauge.

1.1. Motivation

Scanning probe techniques have existed for nearly 30 years [8]. Every year, there are new developments within the technology. Some of the recent achievements within this field include biological sampling [9], faster scan speeds [10], higher resolution [3], and the development of a multitude of different operation modes.

One of the main constants in SPM technology lies within the apparatus itself. The sensing tip is connected to a cantilever beam that deflects upon the observation of a force. Typically, an optical system is used to detect the deflection of a cantilever beam, although piezoresistive sensors have also been used. However, the widely used laser and optical system allows a laser to reflect off the backside of a cantilever onto a photodiode. As the tip moves, the cantilever deflects, causing the beam to shift on the photodiode. The movement of the system is controlled by a piezotube, which is a series of piezoelectric materials, meant to move either the cantilever beam, or the sample (depending on the system) in an XYZ direction.

The collection of data points of where the laser hits the photodiode results in an image. The resultant apparatus, containing these components can result in a large footprint, often occupying large tablespots. The inclusion of vibration isolation to lessen the effects on the laser also expands the size of the entire system. And while the piezotube offers reliable stage movement, it also encounters various nonlinearities such as hysteresis, creep and bowing. This causes the resultant image to distort [11].

The cost of an SPM is also high. With scan speeds that can cover a small area in a relatively large amount of time, it is not economically viable to use the devices in mass testing. For this reason, most SPM apparatuses are sold to research or niche industries. In order to expand into more predominant industries, such as transistor testing, multiprobe arrays must be developed. Currently, apparatuses such as the Zyvex multiprober are used to characterize devices. A series of 8 probes are placed into a scanning electron

microscope (SEM), where a system of translational stages is used to move the probes in an XYZ direction. However, this introduces new complexities into the system. The SEM is a highly expensive characterization tool that must operate at a vacuum level. The charging induced by the electron gun may also cause distortions of the image during probing. The probes, if mismanaged may also cause damage to the system. If a multiarray of SPM devices can be realized, they can be utilized in the same manner of the Zyvex prober, offering a cheaper, less damaging and possibly easier to use and maintain solution.

In particular, the KPFM technique is well suited for characterizing transistor devices, as the topology of thin film transistors have small topological differences, but the work functions of the materials contrast greatly. In addition, embedded materials will show varied surface potentials during the KPFM scan [12].

Many other industries have also begun to adopt new nanotechnologies into their products. Quantum dots have begun its infiltration into many developing technologies, such as displays, due to their high colour contrasts [13]. The quantum dot fills with electrons, which allows for extremely precise electronic measurements, also perfectly suited for a KPFM. Batch creation of a MEMS-KPFM would be able to mitigate the cost of the technique, allowing for immersion into various industries.

In the long run, by developing a cheap KPFM device with resolution only an order of magnitude less than conventional tools, a cheap, reliable instrument would open the doorway for new markets. The idea of a cheap microscope opens new realms in industry, where current SPM technologies have not made penetrating strides; allowing many innovations in the realm of nanotechnology to prosper. Providing these cheap microscopes to the education may also help to inspire students to excel in areas of science and technology [14].

1.2. Objective

There are various objectives explored within the scope of this project. The end goal of this project is to work towards a CMOS-MEMS based KPFM device, capable of discerning the work functions of different materials. There are many aspects to complete throughout the duration of this project, and as such, it is important to break down the final project into a large number of goals.

There are three main topic areas that lead to the end goal of developing a fully functioning CMOS-MEMS based KPFM device:

KPFM Device Modelling and Design:

In order to create a functioning MEMS device, it is important to design a device that closely corresponds to its contemporary ideals. In this case, it is important to reach the correct spring constant and resonant frequencies. Since one of the goals is to replace the laser and photodiode system with a piezoresistive sensing bridge, it is important to understand the correct placement of the strain sensing devices. The goal of this section is to design a KPFM device that has similar characteristics to the conventional instrument with the corresponding optimal stress sensor placement. The XYZ-stage is also simulated to determine the characteristics of movement.

Tip Fabrication:

The use of CMOS-MEMS technology limits the tip sharpness. In order to create a high resolution device, the limiting factor, the tip, must be sharpened. However, due to the fragility of the CMOS-MEMS devices, new methods of tip sharpening are explored. In addition, future work concerns a conductive contact between the tip of the device and the sample. The aluminum layers of the CMOS-MEMS device often oxidizes as soon as it is exposed to atmosphere. The goal of this section is to use various techniques to help sharpen a post-processed CMOS-MEMS cantilever tip, as well as plating the device with a known material to stop degradation through oxidization.

KPFM Sensing and Stage Actuation:

The most important portion of the project is to demonstrate a working KPFM device. Without experimental validation, the topic at hand will not be realized. In this work, the simulated and designed, CMOS-MEMS devices are fabricated and released. The goal of this section is to validate the KPFM device. Various experiments are carried out to match the characteristics of the cantilever beam to the equations that govern this measurement method. In addition, the XYZ-stages are tested to determine their efficacy of obtaining an image.

1.3. Outline

The thesis is separated into six chapters. Chapter 1 introduces the idea of the KPFM and its general shortcomings. The concept of CMOS-MEMS based KPFM device is introduced to replace the conventional KPFM, mitigating many of the shortcomings. The motivation behind KPFM miniaturization and MEMS integration is explained, and the general objectives are outlined.

Chapter 2 contains a literature survey of the uses of the KPFM and the developing technologies surrounding the conventional system. While used mostly exclusively as a tool, it is important to understand the types of samples and environmental conditions that is subjected to the KPFM. Tip sharpening is also an important part of creating a high resolution KPFM. Various classical and contemporary methods of tip formation are discussed in order to develop an understanding of how tip formation can be approached for a CMOS-MEMS device. Finally, MEMS devices are discussed. State of the art sensing and actuation systems are discussed. The advantages or shortcomings are explained in detail, to understand which system would be optimal for use in a CMOS-MEMS KPFM system.

Chapter 3 contains the design considerations for a CMOS-MEMS KPFM device. A thorough discussion on the theory of KPFM is outlined, from which a set of criteria and requirements will be outlined. KPFM beam stiffness, conductivity, and sensitivity are considered in the design of the device. Following the design considerations, an initial KPFM device can be realized. Through this, a CMOS-MEMS process is considered. The fabrication process is also outlined to help understand the structure of the device. Simulations are performed, and device geometry is optimized to realize a stiff, high sensitivity KPFM design.

Chapter 4 presents experimental results specifically geared towards material modifications for CMOS-MEMS devices. In order to obtain a sharp tip for any type of CMOS-MEMS SPM device, the device must be further post processed, as the design rules for the initial process will not create a sharp tip. Experiments involving electroless plating of palladium and nickel are presented in order to show the efficacy of plating slowly oxidizing materials. Experiments involving the creation of sharp gallium-aluminum tips are explored.

Chapter 5 presents the experimental validation of the CMOS-MEMS KPFM device. The device is tested against various samples, and the results are compared against the equations that govern the KPFM method. The resultant design shows that a KPFM device can be realized with piezoresistive strain gauges created from the polysilicon gate layer of the CMOS-MEMS process. The XYZ-stage is also tested to show that it is plausible to obtain an image of the work function.

Chapter 6 concludes the thesis and the work performed. It outlines the future work involved with the project, including plasma enhanced tip formation as well as full integration between the device and the XYZ-stage.

2. Literature Review

This chapter presents a literature review of the relevant subject areas. In order to understand the process used to build a MEMS based KPFM structure, it is important to understand the underlying SPM technology. Section 2.1 shows the scanning probe microscopy basics, outlining the various components that make up a conventional scanning probe instrument. Afterward, a discussion of the KPFM and its general components is shown. Finally, the developments in KPFM and its various specific uses are outlined.

The secondary objective of this work is to develop a valid method for tip modification and formation on the MEMS based microscope. Section 2.2 of the literature review contains a basic overview of the importance of sharp tips, and the different methods used in order to develop sharp probe tips.

Section 2.3 provides a background into the MEMS technology used in this work, as well as developments of SPM integration with MEMS technology. The advantages and disadvantages of using certain sensor or actuator applications for the MEMS devices are explored.

2.1. Scanning Probe Microscopy Basics

SPM is a branch of microscopy that began with the scanning tunneling microscope (STM), invented in 1981. [8] The scanning probe microscope is an important tool with a variety of uses. To label and explain them all would be a lengthy task, as new methods are currently spurning from the utilization of the SPM. The most common use of the SPM is a functional mode called atomic force microscopy (AFM), invented in 1985 [15]. This mode allows the user to obtain a surface topology of a sample on the atomic level. This is important for characterization of small scale devices. The AFM is often used due to its inherent ability to image a surface without vacuum, special coatings and use within different mediums. The AFM also allows the user to image a surface in three dimensions, which is not possible with other popular characterization tools such as the scanning electron microscope.

On the other hand, there are also disadvantages associated with the SPM. This includes slow imaging speeds as well as small imaging areas. If there is a specific area of interest in a sample, imaging with the SPM almost becomes an overwhelmingly time consuming task. To counter this disadvantage, a large

amount of research has gone into SPM arrays, therefore, increasing the size of the scan area while keeping the scan times relatively similar [16].

In order to further develop SPM technology, the underlying physics and device operation must be understood.

Before understanding the physics behind the scanning probe microscope, it is important to identify the system, and how all the portions correlate together to obtain an image. In general, there are two different methods in designing a conventional SPM. The first type of SPM moves the probe across the surface of a stationary sample, whereas the second type has a stationary probe, and the sample stage is moved instead. While both types of SPM contain the same devices, the placement of the piezoelectrics can be different (ie. for a moving sample stage, the piezoelectrics control the stage).

The main aspects of the generic SPM are:

- Cantilever
- Tip
- Laser source
- Photodetector
- Piezoelectrics for fine positioning
- Motors for coarse positioning
- Controller
- System used to drive oscillations in cantilever for dynamic modes

A probe is attached to a cantilever. The motor based coarse positioning system and piezoelectric fine positioning system are used to lower the cantilever onto the sample. As the cantilever moves across the surface via fine piezoelectric stages, the forces from the sample interact with the sharp tip, causing deflections in the cantilever. A laser is reflected off the backside of the beam onto the photodetector. As the tip moves across the surface, the changes in the attributes of the cantilever (whether it changes in deflection, amplitude, or frequency), the recorded outputs from the photodetector are outputted as an image [17]. In addition, a controller is utilized to help track the movements of the positioning system, feedback control, etc. Also, depending on the operation mode of the SPM, actuators can be used to drive the cantilever, oscillating it at specific frequencies or amplitudes. This can be seen in Figure 1 [18].

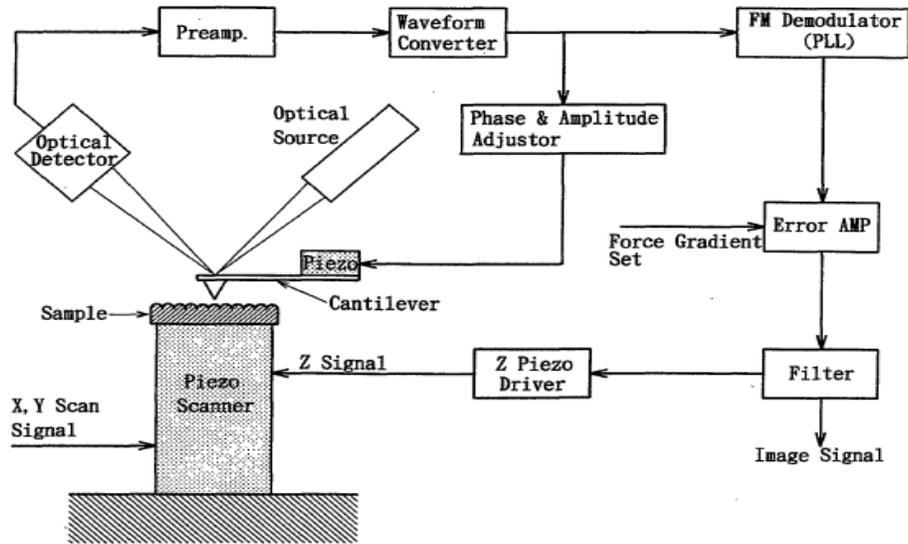


Figure 1: Basic flow diagram of a conventional AFM [18]

However, there are other systems which do not incorporate a photodetector or a laser. Piezoresistive sensors are placed in cantilevers, such that upon deflection, the extension of the material causes the resistance to change. This is detected through a bridge circuit that is external to the piezoresistive cantilever. This can be seen in Figure 2 [19].

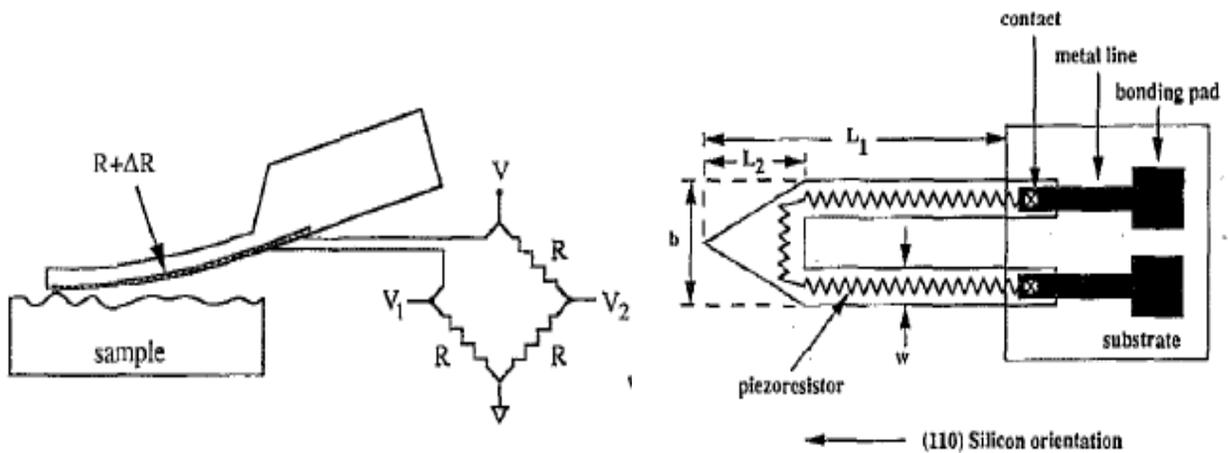


Figure 2: Outline of a piezoresistive cantilever [19]

2.1.1. Background Topics of the Kelvin Probe Microscope

Essentially, the KPFM is a tool that utilizes the SPM system to detect local contact potential difference, first described by Lord Kelvin [20]. Subsequently, a simpler method of detecting this contact potential difference was developed in 1932, where a voltage was applied to stop an oscillation when two dissimilar materials were brought together [21]. It was noted that when the materials are brought in proximity with each other, charge can build up due to the intrinsic contact potential difference of the materials. While oscillated, this acting capacitor can induce a measureable charge transfer via an electrometer. Upon applying a voltage to minimize the contact potential difference, the charge transfer detected on the electrometer becomes negligible.

The first KPFM was discovered in 1991, where a gold coated cantilever and tip was brought towards a platinum surface. The schematic is seen in Figure 3 [1].

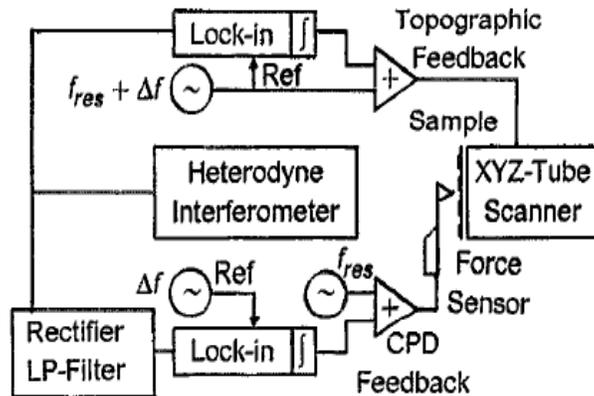


Figure 3: Flow diagram of a conventional KPFM instrument [1]

In this set up, the gold coated cantilever is brought towards the sample, where it is forcefully oscillated above its resonant frequency, $\Delta f + f_{res}$. The heterodyne interferometer allows the motion of the cantilever to be tracked. While the topographic image is measured from the changes in frequency from the forced signal, the second lock in amplifier observes Δf . Due to the signal mixing, a Δf term appears when the cantilever is forcefully oscillated, and disappears when the contact potential difference is minimized. Measuring the contact potential difference is important in many different applications, especially when the topography is not very distinguishable, but large differences in electrical properties exist. [1]. The contrast of the height measurement, Figure 4a is not as distinguishable as it is in Figure 4b. While the paper quotes that the work functions observed are hard to quantify against actual data, due to the various impurities on the cantilever probe tip and the surface, it was shown that contrasting work functions can be

observed over a sample with low vertical resolution. Since this time, improvements have been made to both software and hardware to improve the image quality of the surfaces observed, as seen in the topology and work function images in Figure 4c and 4d.

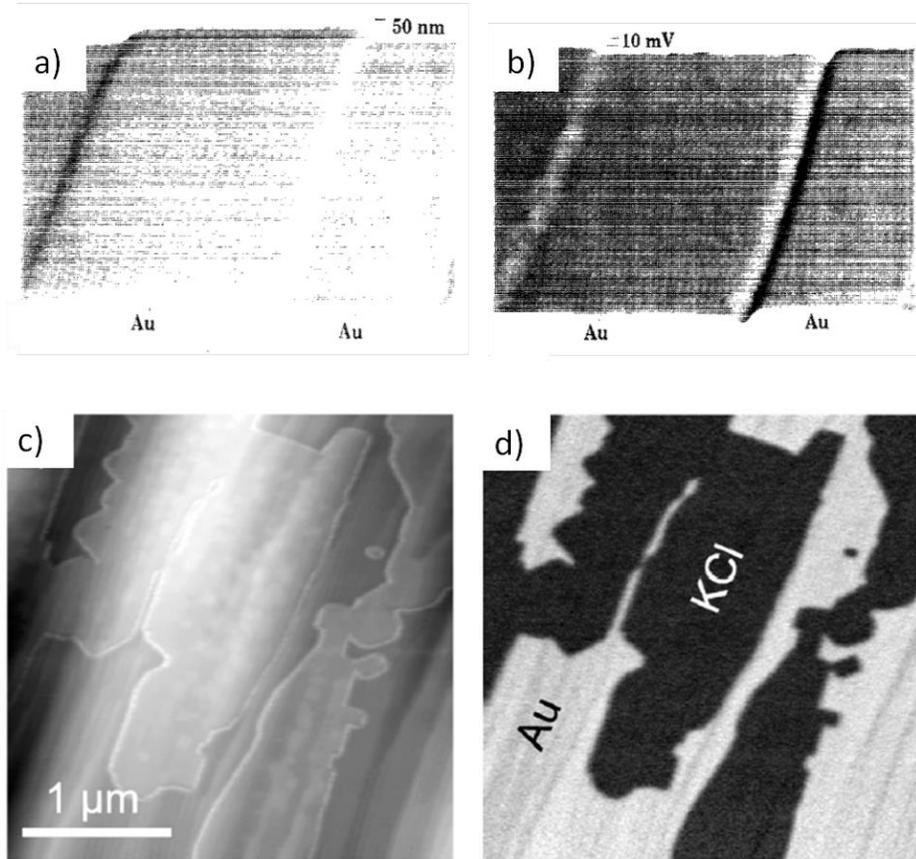


Figure 4: (a) Height measurement with AFM in the past, (b) Work function measurement with KPFM in the past[1], (c) Height measurement with AFM with improvements, (d) Height measurements with KPFM with improvements [22]

Long strides have been made past this point to develop the KPFM. There are two main methods of KPFM, amplitude modulated KPFM and frequency modulated KPFM. In amplitude modulated KPFM, the cantilever is generally oscillated at the resonant frequency. One lock- amplifier is used to determine the amplitude of the electrostatic force that exists between the tip and the sample, since the signals are typically noisy and small. Once the contact potential difference has been nullified, the beam no longer oscillates at the resonant frequency, but continues to resonate at the second harmonic. This second harmonic is generally used to track topography [22]. On the other hand, frequency modulated KPFM, forcefully oscillates the cantilever off resonance. Side bands are created around the resonant frequency from the forced oscillations. Two lock in amplifiers are used to demodulate the sideband signals, and determine the amplitude of the sidebands. A bias is applied to eliminate the amplitude of the sidebands [22].

2.1.2. Developments in Applications of KPFM for Nanomaterials

Much of the development for the progression of the KPFM lies in obtaining higher and higher resolution images for basic nanomaterials. There has been a rise in the field of nanotechnology within the past few decades; the shrinking of materials has opened new doors towards the discovery of new electronic properties. The need for characterization of specific electronic properties has become an increasingly important topic.

For example, the development of quantum dots has led to a variety of applications. While the AFM may characterize the size of the quantum dot, it is unable to probe for the electronic properties, as seen in Figure 5. The purpose of the quantum dot is to monitor a set energy level for electrons. The effects of charging can be seen by measuring the electrical properties of the quantum dot before and after charging. This charging is performed by injecting electrons into the quantum dots by allowing a biased probe to come into close proximity with the material. This was held for an extended period of time to allow the electrons to fully saturate the material. It was observed that while the size of the particles did not change, the charge of the material itself had changed from approximately 66 mV to 429 mV [23]. Figure 5a shows the vertical profile on the left and the surface charge on the right. Figure 5b shows the same images after the quantum dots are injected with electrons. While the height difference is not observed, however, the surface charge vastly differs.

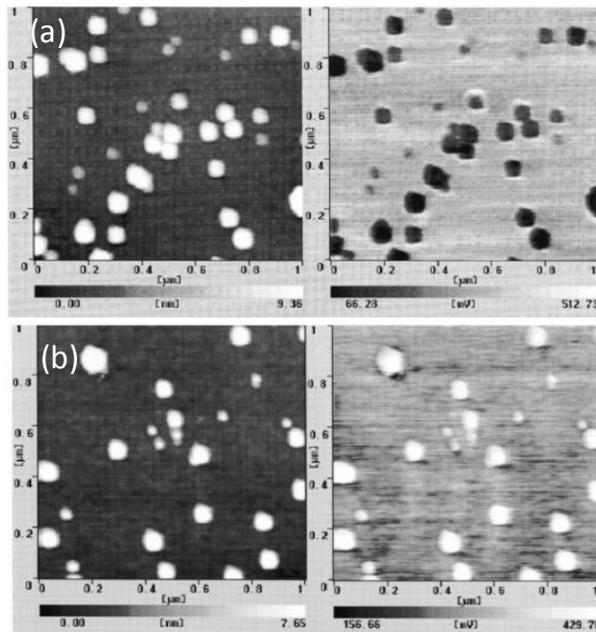


Figure 5: (a) AFM and KPFM quantum dots before charging. (b) AFM and KPFM quantum dots after charging. [23]

The charge transfer of metallic catalysts is an important characteristic to measure, especially in the case of energy applications, such as batteries and fuel cells [24]. The work function of the nanomaterial can be changed due to different processing conditions, and can be characterized with the use of a KPFM. When the nanoparticle is exposed to air, as opposed to a nitrogen environment, the size of the particle does not change by a large margin, however, it can be observed that the work function is shifted [25]. A change in the work function can cause charge transfer to flow opposite to the desired direction.

Self-assembled monolayers (SAM) are becoming an increasingly popular material. Once placed upon a surface, the materials conform to a certain configuration. The type and size of the structure that forms, directly correlate to the electronic properties of the material, as well as the substrate that holds the material. A SAM is deposited on both silica and mica. While both of the structures take on 6 nm features, the work function difference between the materials on the two different sample substrates differ by 10 mV. Since most SAMs are used for specific applications in sensing, it is important to know the electronic characteristics [26]. Other characterization tools falter in this type of characterization, as AFM will not be able to detect the charging properties of the material. A scanning electron microscope may be utilized to take an image of these structures, but ultimately, may only take qualitative data on the electronic structure through processes such as electron beam charging. This will distort any kind of quantitative observation.

With the ability to track the surface charge of a material, the KPFM takes this one step further by tracking the electron densities within a single molecule. Distinct quantitative observations have led to in depth understanding of molecular nature fundamentals. An AFM was used to directly observe the topography of the molecules, while a KPFM scan revealed the electron densities, seen in Figure 6 [3]. The realm of high resolution KPFM allows for the determination of changes in bond energy, and electron densities during reactions.

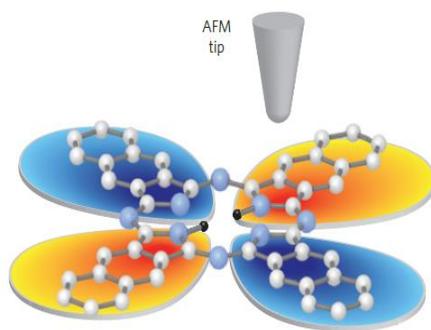


Figure 6: Stylized high resolution KPFM imaging of a molecule [3]

Although a large amount of the development is aimed at higher resolution images, there are many applications in which lower resolution KPFM can be used. The tracking of pH in microfluidic solutions

[27] by investigating the charge behaviour of free H^+ ions in solution can be detrimental in industry and research. In situ measurement of liquid systems can help to monitor real time reactions of microfluidic channels without stopping flow and measuring the output. This is greatly important for research in medicine, where the effects of the medicine traveling through microfluidic channels can be monitored, streamlining the process.

2.1.3. Developments in Applications of KPFM for Electronics

The development of novel electronics also has heavy KPFM involvement. The ability to probe electronic characteristics during operation provides unique opportunities for the KPFM to give quantitative data of the device at hand [9, 28].

Among the most important are new materials for transistor devices. One example of a new material is graphene oxide, an extremely flat material with little change in topography. Figure 7 shows a deposited layer of graphene oxide that overlaps two gold electrodes. Figure 7a shows a topographical map of the transistor. Figure 7b shows the KPFM image of the device under operation. One volt is applied between the two electrodes, and the KPFM is used to track the electronic properties of the graphene oxide over the gap between the gold electrodes, as seen in Figure 7c. The potential decay over the material shows how the material may react upon operation as a field effect transistor device [29].

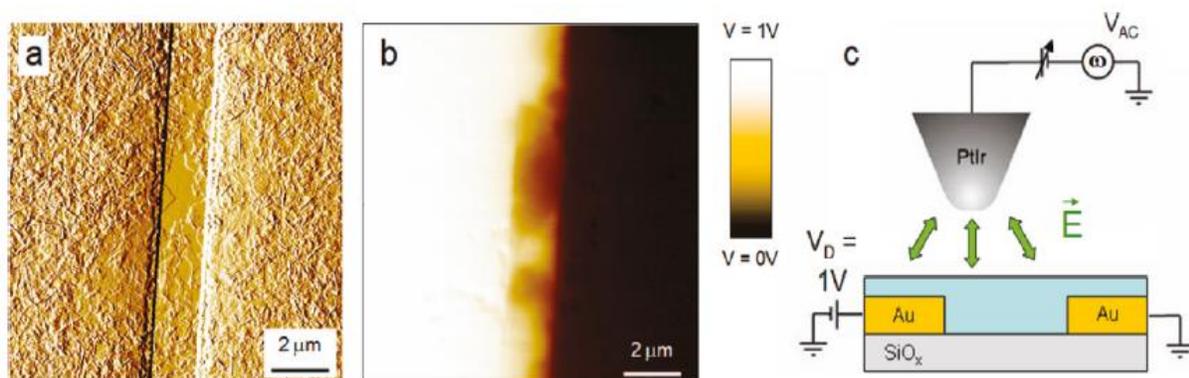


Figure 7: (a) Topography of device with AFM, (b) Surface charge map with KPFM, (c) Functional set up [29]

While the outputs of a transistor can be monitored during operation to understand the voltage between the drain and the source, as well as the gate and the source, there is no easy method of directly probing the

material. If a material fails to provide certain characteristics, and shows no changes at the topographic level, the KPFM may be able to detect the presence of an electronic disconnect, showing certain failure modes for transistors, as seen in Figure 8 [30]. At certain drain to gate voltages, the changes in surface charge gives clues to the methods of failure observed in the transistor being tested. Figure 8a shows the KPFM and AFM images of the transistor upon different loading. While the AFM image shows no topographical differences, one can see a large accumulation of stress from electrical overloading. Figure 8b shows the SEM image of the area scanned, and Figure 8c shows the SEM image of the resultant damage.

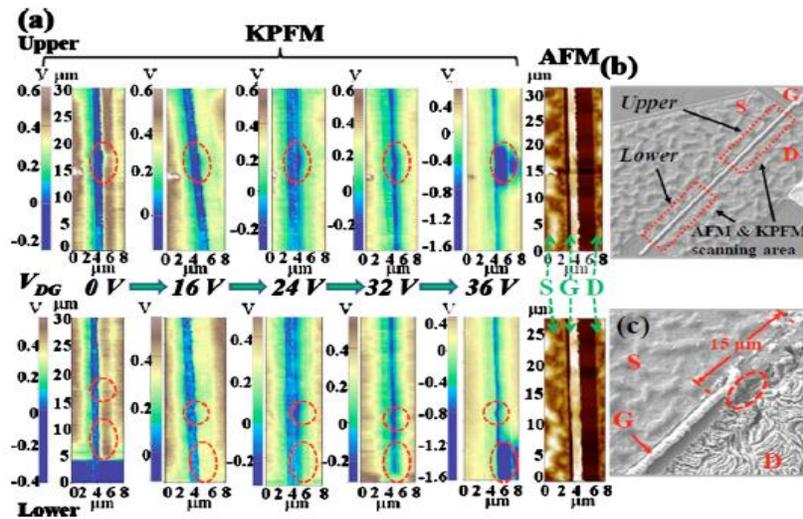


Figure 8: (a) KPFM and AFM image of the transistor, (b) SEM image of transistor, (c) SEM image after failure [30]

MEMS are an important area for testing. RF capacitive switches operate by creating an extremely large electric field, which electrostatically displaces a free moving beam. However, after one use, the film does not fully discharge automatically, and instead, stay within with film. Subsequent operation of the MEMS device results in a change in actuation voltage. This persists until the device has fully discharged. Figure 9 shows the time scale in which the charge dissipates, monitored with the use of a KPFM [31]. The U refers to bias applied to match the surface charge of the MEMS device, and X is the length upon the KPFM scan region.

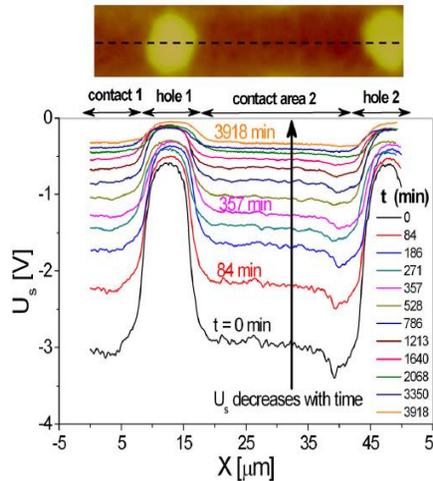


Figure 9: Time scale at which charges dissipate in a MEMS device via KPFM. [31]

The silicon nitride film with purposely placed holes, is charged with an underlying metal layer to approximately 3 V. The KPFM is used to take a measurement of the surface potential. It should be noted, that the scan holes show only approximately 0 V, as there may be material in the underlying layer affecting the forces that act upon the tip. The surrounding surface charge may also cause fringe effects on the tip as well, resulting in a surface potential that is not equal to 0. The device is allowed to discharge on its own, while the KPFM takes timed measurements over the period of 3918 minutes [31].

2.1.4. Other Developments in KPFM Technology

While the KPFM is most consistently used as a tool for high resolution imaging of electrical characteristics, there is new work in the actual technology itself, to improve factors such as noise and increasing the number of operational conditions.

The technique is often performed in vacuum in order to increase the signal from the cantilever. The advent of multi frequency mode allows for higher resolution in the lateral mode [32] while in air. Using multiple frequencies to scan the sample, a higher resolution can be seen through sensitivity increase and lower noise. Two scans are performed in air, and using different resonant modes, allows higher resolution scans of the scanning of topography and the surface potential, as seen in Figure 10.

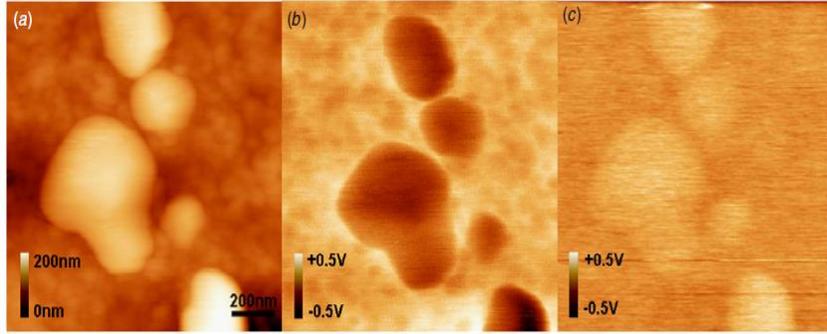


Figure 10: (a) AFM image of a sample. (b) KPFM scan with multifrequency mode. (c) KPFM scan without multifrequency modes [32]

Another noise reduction technique involves narrowing the window for the signal to interact with the sample [33]. Designed around the concept of a coaxial line, a conductive cantilever is coated with an adhesive titanium layer. Layers of insulative material are grown around the cantilever using chemical vapour deposition, followed by a final layer of titanium and gold. The resulting KPFM tip, seen in Figure 11, only interacts with the sample with a tiny window. This allows the lateral resolution to increase by reducing the amount of fringe electric field that may present influences on the sample during the scan. A bias is applied to the shell to ensure that no charge build up occurs between itself and the inner tip. This increase in capacitance would alter experimental data. As well, a capacitor is added parallel to the voltage supply for the outer shell. This eliminates the AC coupling into the shell.

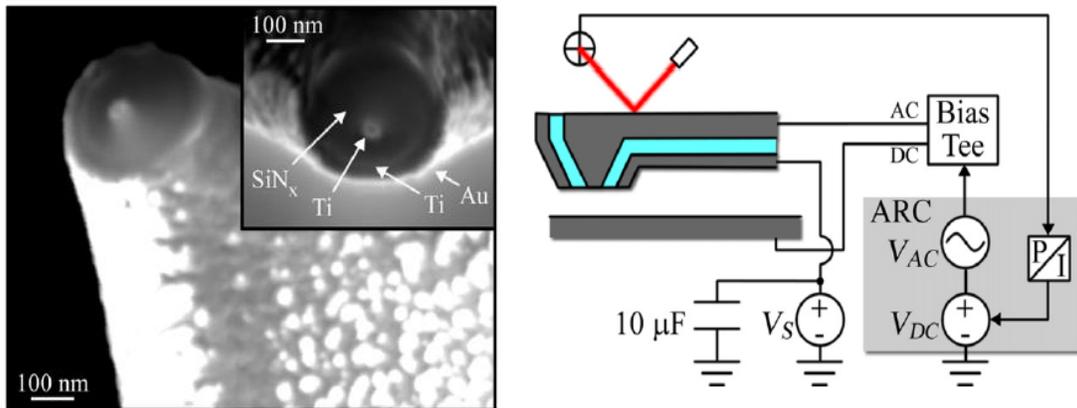


Figure 11: KPFM with coaxial tip [33]

While remaining undone for the KPFM, projects such as the IBM Millipede project have tried to increase the number of cantilevers into an array type structure. This allows for large area scanning for quick acquisition of data [16].

2.2. Tip Geometry and Modification

The geometry of the tip at the end of the cantilever is important. The shape of the tip may determine the accuracy of the produced image. The optimal tip would be a long cylinder with an infinitesimally small radius. Due to many physical limitations, no tip can theoretically be smaller than an atom, and a tip containing a long chain of atoms with a diameter of one atom is generally not physically possible. It may also not be practical, as any bending towards this tip will cause instantaneous fracture. In general, a high aspect ratio tip with a one atom tip is still generally the most sought after geometry.

Without a small radius, the tip will simply glance over any features smaller than itself. This will mean that small features such as a trench will not be observed, seen in Figure 12a. In order to detect any sort of small feature, an extremely small tip radius is needed. A tip without a steep sidewall will also produce an incomplete image. This can be seen in Figure 12b. Measurements with a low aspect ratio tip will detect small features, but if the trench size exceeds the aspect ratio of the tip, the resolved image will be that of the tip itself. On the other hand, if the tip runs over a feature with steeper sidewalls than the tip, the angle of the tip will be characterized instead of the feature itself, as seen in Figure 12c.

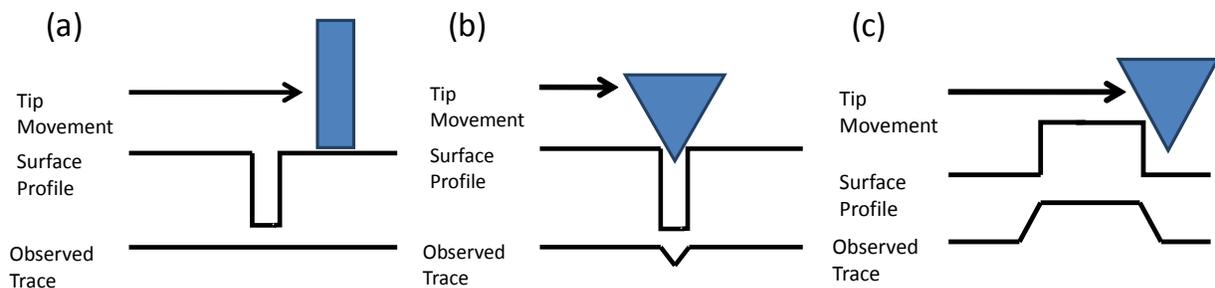


Figure 12: Effects of tip radius on surface imaging

In order to create a successful SPM system, it is important to develop an extremely sharp and sturdy tip. The limiting factor in creating a high resolution image is the sharpness of the tip. The hardness of the tip is another important aspect; a tip that quickly dulls will need constant replacement. Current research in tip technologies focuses on these two aspects. Research is also performed on in situ sharpening after the tips have become dull. The various different methods used to create SPM tips present its own advantages and disadvantages, and will be investigated throughout the rest of this section.

2.2.1. Methods of Tip Sharpening

There are various methods to create sharp SPM tips. The most commonly used methods include:

- Isotropic/Anisotropic Under Etching [34, 35]
- Silicon Mould [36, 37]
- Nanotube Attachment [38-43]
- Focused ion beam [44, 45]
- Electron Beam Deposition [46]
- Plasma Etching [47]
- Electrochemical Etching [48]
- Silver Gallium Needles [49]
- Reflowing Metal [50]

Isotropic/anisotropic under etching is a vastly popular method of tip fabrication. This process involves creating a tip on a premade cantilever. The cantilever is created by depositing a silicon nitride film on the front and backside of a silicon membrane. A cantilever shape is resolved through patterning of the silicon nitride on the backside. On the tip side, a small patch of silicon nitride remains on top of the crystalline silicon. A silicon etch is performed. A long etching cycle causes under etch of the silicon underneath the mask. Since the etch occurs only at the surface of the liquid/solid interface, both isotropic and anisotropic etches will result in a tapering of the material directly underneath the mask, as seen in Figure 13 [34]. Upon a certain point in time, the etch will reduce the amount of silicon to the point where there is no material in contact with the silicon nitride. This causes the silicon nitride mask to fall off, thus ending the tip fabrication process.

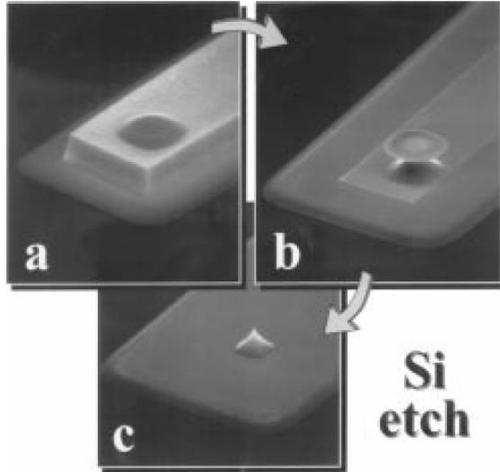


Figure 13: Tip creation through silicon underetch [34]

The materials involved with creating these tips are extremely cheap. The entire process is wafer sized; hence the throughput is extremely high. The material used to create the tip, silicon, is extremely hard and wear resistant. The tip radius can theoretically be up to 1 atom, however, involves careful etching times. Since the etch process occurs in a wet environment, careful control of the etching times are difficult.

The silicon mould is another vastly popular method in tip fabrication. A silicon wafer is coated with a masking layer and a dry etch is performed to create an initial trench in the crystalline silicone. The wafer is submerged in KOH and allowed to etch until the side walls are straight due to the orientation of the crystalline silicon. The straight (110) side walls allow for an extremely high aspect ratio tip, while the tips terminating at the (111) plane create a 69° tip. Afterward, metal is deposited into the finely defined trenches. The rest of the silicon is etched away in a KOH solution, leaving a metal cantilever and tip created from the trenches in the silicon, as seen in Figure 14 [36].

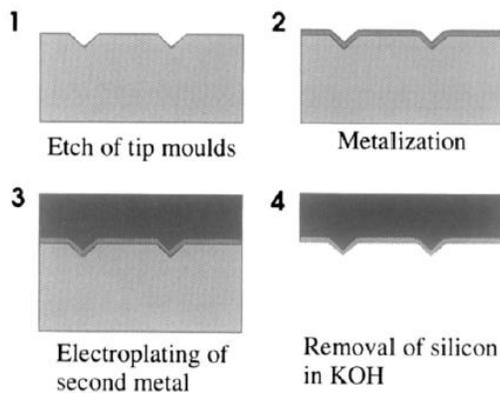


Figure 14: Tip fabrication using a silicon mould [36]

The advantage of using this method is the high throughput of cantilevers that can be made at once. The cantilevers are created using metal, hence allows them to be functional in conductive SPM applications. The electroplating of additional metal on top of the mould allows for an increase in the stiffness. However, the metal is not as stiff as the silicon, limiting its use to non-resonating, contact modes of SPM. The tip radius also suffers, as products of moulds may not be fully representative of the trench from which it was fabricated. The metal is also more prone to dulling than silicon.

Nanotube attachment has been an extremely popular new topic in tip fabrication. The high aspect ratio, low radius of curvature and high stiffness of a nanotube makes the probe material extremely valuable, and widely used in new tip technologies, as seen in Figure 15. As nanotubes, such as the carbon nanotube, can be designed to be conductive, most SPM modes can use such materials as tips.

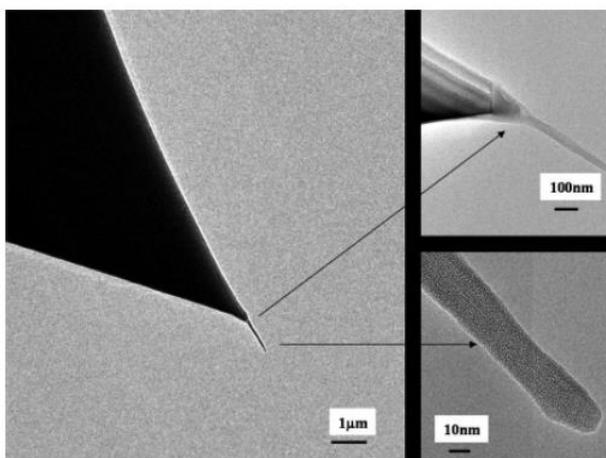


Figure 15: Carbon nanotube based cantilever tip [38]

There are various methods to attach a nanotube onto a substrate, including controlled self-assembly within a dielectrophoretic field [38], picking nanotubes from a surface [39], direct growth from a tip [40,41,42], and attached using magnetic field alignment [43].

Tips curvature can fall as low as 1 nm [39] in some cases, and can withstand multiple uses without dulling [41]. While the tips are generally excellent for imaging, the shortcoming of using these tips includes the large amount of time needed for fabrication, especially for CVD grown nanotubes. The throughput of these tips is generally on the order of cantilevers; maintaining mass production with low variance nanotubes currently still present a problem.

The focused ion beam (FIB) is another method for tip fabrication. The FIB is able to either add material to an existing surface, or remove material from an existing surface. Both methods can be used to create a sharp tip on a SPM probe [44]. Focusing a high energy ion in a certain spot will result in high level

bombardments against the surface, slowly eroding away the tip. On the other hand, additive FIB allows for ion implantation on the exposed area. After implantation, an electron beam source is directed towards the ionic implants, causing growth at the ion saturated apex of a tip. This results in an extremely slow and expensive process that benefits only one cantilever at a time, however, at the same time, allows many different materials to become a tip.

Electron beam deposition (EBD) is similar to the additive FIB method. The cantilever is placed into an SEM, and the electron beam is focused onto the tip area. The surrounding contaminants in the chamber, such as oxygen and carbon species are directed towards the beam, forming a small, but sharp structure [44]. While the sharpness of the tip can reach approximately 30 nm, the tip is not conductive, and cannot be used for methods such as the KPFM. As well, the throughput is only at the range of individual tip formations, where individual tips are made over the period of 600 seconds [45].

Plasma etching is an important tip sharpening technique. Some tips undergo slight plasma etching after processing to help remove a small amount of material from the tip. Once placed in a plasma source, such as Cl_2 [46], the high electric field lines from the sharp tip causes disproportionate etching, and allows higher etch rates from the sloped walls of the tip, as seen in Figure 16. The advantage of this method is the wafer sized throughput, and the increasing sharpness with a small etching time. However, the dry etching process still indiscriminately etches the entire substrate as the ion bombardment still occurs over the sample, although some more than others. Very sensitive devices may receive damage from prolonged exposure to the plasma.

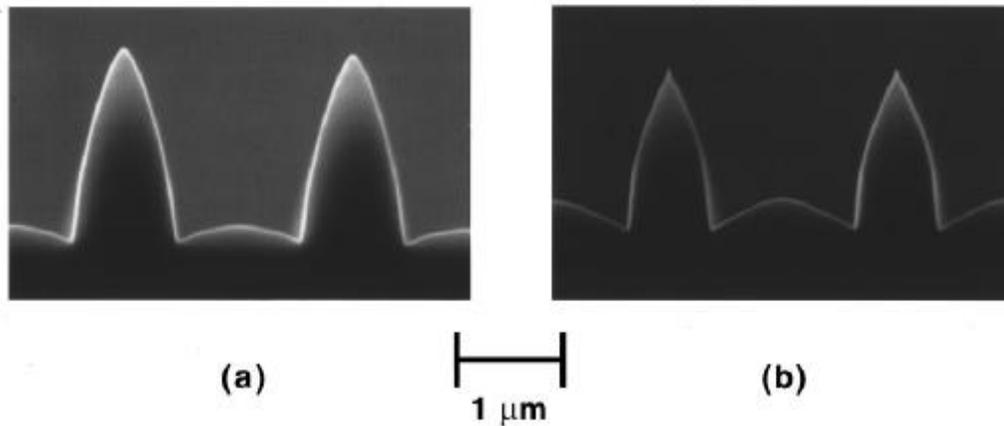


Figure 16: Effects of plasma induced tip sharpening

Electrochemical etching is a popular method for STM tips, which require no cantilever or laser to measure deflection. This tolerance allows methods such as electrochemical etching to produce extremely fine tips. A conductive wire is placed into an electrochemical bath. An electrochemical reaction is

performed on the wire, slowly reducing the width [48]. Since a constant bias is applied between the terminal of the electrochemical bath plate and the wire, the current density increases with the thinning wire. Upon breaking of the wire, the current density immediately drops, and a circuit is used to immediately halt the reaction. The result is an extremely sharp tip in the order of 20 nm.

Another newly developed method of growing tips involves dipping a silver coated cantilever into a gallium droplet [49]. Gallium is known to break down the lattice of most metals, forming an alloy. Upon dipping a metal coated tip into gallium, the gallium instantly begins to break the metal coating, creating structures at the interface. Slow removal of the tip from the gallium droplet allows the gallium/metal mixture to form a sharp tip, as seen in Figure 17. After a few days of rest, the free liquid gallium will terminate as it fully alloys with the metal, forming a hard brittle tip. While the method allows for extremely high aspect ratio sharp tips, the throughput is fairly low; one cantilever at a time. However, the conductive metal allows for KPFM measurements.

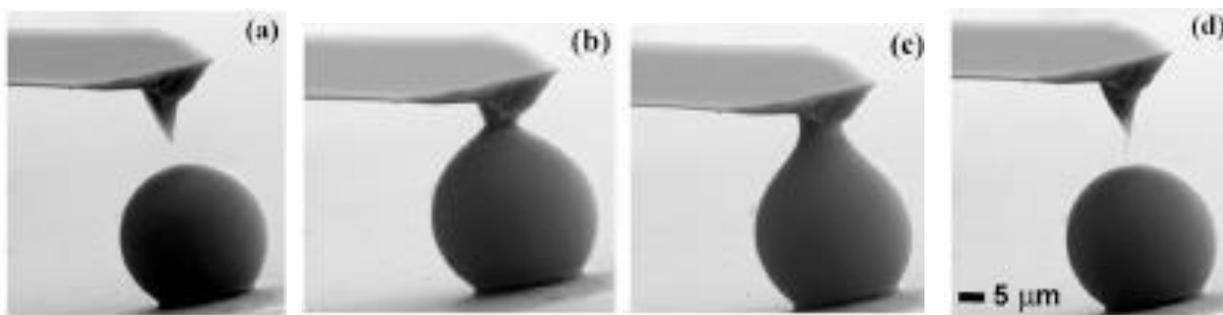


Figure 17: Tip fabrication using gallium to form sharp geometries

The last method to be introduced involves reflowing metal from a tip. A laser is pulsed on a platinum indium wire to reflow it while strong electric fields cause migration of the molten alloy [50]. The process of forming a cone through strong electric field is called the Taylor Cone. Since the melting temperature of indium is much lower than that of platinum, the pulsed laser will only melt one of the two metals, allowing stability during the reflowing process.

Table 1 describes the outcomes of various experiments discussed in this section. The tip radius, cone angle, sidewall angle, height, throughput and usable materials are outlined. Figure 18 demonstrates the measurements.

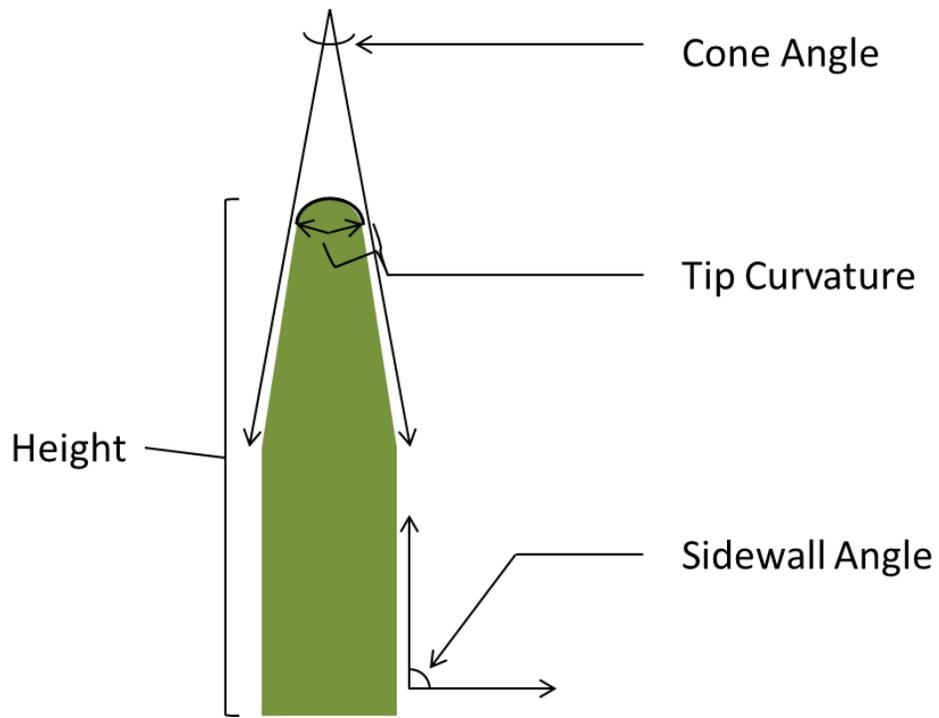


Figure 18: Measurement angles of tip sharpness

Table 1: Summary of Tip Fabrication Methods and Measurements

Method	Tip Radius	Cone Angle	Sidewall Angle	Height	Throughput	Usable Materials
Underetch [34]	<10 nm	--	--	6-7 μm	Wafer sized	Silicon
Underetch [35]	<20 nm	35°	--	1.5 μm	Wafer Sized	Boron-doped silicon
Mould [36]	~50 nm	69°	90°	<15 μm	Wafer Sized	Chrome/gold
Mould [36]	250 nm	69°	--	2-4 μm	Wafer Sized	SU-8 and Nickel
Carbon nanotube assembly through dielectrophoretic field [37]	20 nm	12°	--	700 nm	Individual Cantilever	CNT on silicon
Physisorption of carbon nanotube to tip [38]	1 nm	--	90°	--	Individual Cantilever	CNT on commercial tip
Direct growth of carbon nanotubes [42]	2-10 nm	--	90°	30-100 nm	Wafer Sized	CNT on Si
Focused Ion Beam [45]	30 nm	--	--	--	Individual Tip	Silicon
Electron Beam Deposition [46]	~30 nm	--	--	0.5-1 μm	Individual Tip	Carbon/Oxygen species
Plasma Etching [47]	22 nm	35°	80°		Wafer Sized	Silicon
Electrochemical Etching [48]	~20 nm	10°	--	--	Individual Tip	Tungsten
Gallium Needles [49]	25 nm	--	~90°	33 μm	Individual Tip	Gallium/Silver
In Situ Sharpening [50]	31 nm	--	--	24 μm	Individual Tip	Platinum Iridium

2.3. SPM-MEMS Integration

The integration of MEMS and SPM is not a new subject area. Since the conventional SPM tip is created through a microfabrication process, the continual development of a fully functioning MEMS based SPM system is not completely farfetched. Within the past two decades, giant leaps in MEMS technology has helped to bring SPM technology upon a new frontier.

There are many advantages for introducing MEMS technology into the line of SPM. For example, due to the high resonant frequencies of MEMS devices, faster scans can be produced. Scanning tunneling microscopes can be fabricated using MEMS technology as it only requires the detection of a minute current. The use of MEMS allows for batch fabrication, and is seen in work such as [51]. Basic high speed SPM probes have also been produced using MEMS technology [52]. Using the high frequency

characteristics of a MEMs device, a resonant frequency of 200 kHz can be observed, actuated through electrostatic forces. An optical system is used to detect the deflection of the structure as it oscillates over the surface. This allows for a reported scanning speed of 5 mm/s, while resolving images with 250 nm features.

Another important aspect of integrating SPM with MEMS technology is the integration of force sensors. By removing the laser system in a conventional SPM device, a large amount of space and weight of the tool is alleviated. In addition, no time is needed to align the laser to the cantilever beam. While STM only requires the detection of minute currents, which can be done off of the device, many other SPM modes require the detection of the displacement from the cantilever beam. This is usually performed with two different methods: capacitive and piezoresistive sensors.

Capacitive sensors, also known as comb drive sensors, are extremely established. A voltage difference is applied to an array of interdigitated beams, as seen in Figure 19, creating a charge build up; producing a capacitance.

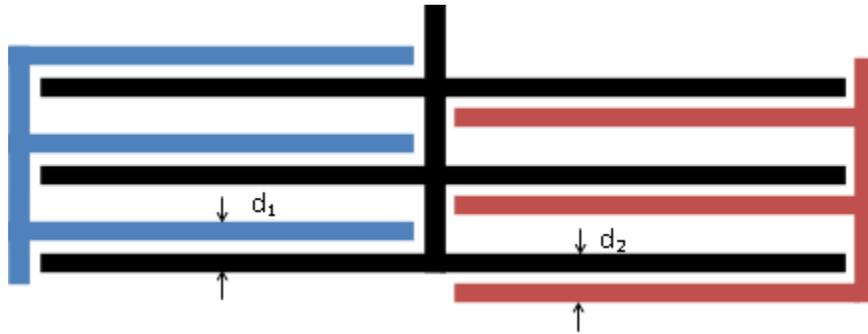


Figure 19: Interdigitated beams for sensing applications

Figure 19 shows a stationary blue and red set of beams. The black pair of beams are translational in the up-down direction. As the black set of beam moves up, d_1 decreases, causing the capacitance C_1 to increase. At the same time, d_2 increases, causing capacitance C_2 to decrease. This is in accordance to the general formula for capacitance:

$$C = \frac{\epsilon_0 \epsilon_r A}{d} \quad (2.1)$$

where ϵ_0 and ϵ_r are the dielectric constant and permittivity of the material, A is the area of the electrodes, and d is the distance between the two electrodes. In this case, everything except d is a constant. A $+V_s$ signal is then placed on the set of blue beams, while a $-V_s$ signal is placed on the red beam. The resultant voltage on the black beam is:

$$V_{out} = V_s \left(\frac{C_1 - C_2}{C_1 + C_2} \right) \quad (2.2)$$

which can be approximated to:

$$V_{out} = V_s \left(\frac{\Delta d}{d} \right) \quad (2.3)$$

where Δd is the change in distance during movement. This type of sensor has been seen widely in literature as a generic force sensor [53], and is used widely in the construction of a MEMS accelerometer [54]. Increasing the number of fingers will increase the signal to noise ratio, as the larger capacitance and change in capacitance will become larger, proportionately. Whenever the translational beam moves, through the application of an external force, the displacement can be quantitatively tracked through measuring the voltage. A 6-axis capacitive sensor with a cantilever probe has been shown with the ability to detect micro and nano-newtons of force, which allows the possibility of an active SPM [55].

The piezoresistive sensor is another popular MEMS sensor [56, 57]. Changing the dimensions of a material will cause the resistance of the material to change. This is often referred to as the gauge factor, G_f , which is given by:

$$G_f = \frac{1}{\epsilon} \frac{\Delta R}{R} \quad (2.4)$$

where ϵ is the strain that the material experiences, and ΔR is the change in resistance that the material experiences, and R is the resistance before straining. Simply, it relates the change in resistance while the beam is deformed. Gauge factors range from material to material, from 100 in p-type silicon to less than 1 with conventional metals [58].

Using a piezoresistors, there are three main methods of easily reading the output; current-source, half-bridge, and the full bridge. This can be seen in Figure 20. The current source configuration allows a current to be driven across the piezoresistors. As the resistance changes, the measureable voltage across the resistor also changes. The resistance of the setup can be described with Ohm's Law. However, as current flows through the resistor, the resistor will also experience changes in length due to thermal expansion. The lumped thermal effects will result in an inaccurate reading.

On the other hand, the half bridge configuration places two resistors with the same value within the system. If they are placed in such a configuration that they heat up equally, the ratio between the two resistors will remain constant, and the voltage readout at V_1 remains the same. In this setting, $V_1 = V_s (R_2 / (R_1 + R_2))$, as with a voltage divider, and the sensitivity of the system is approximately V_s / R .

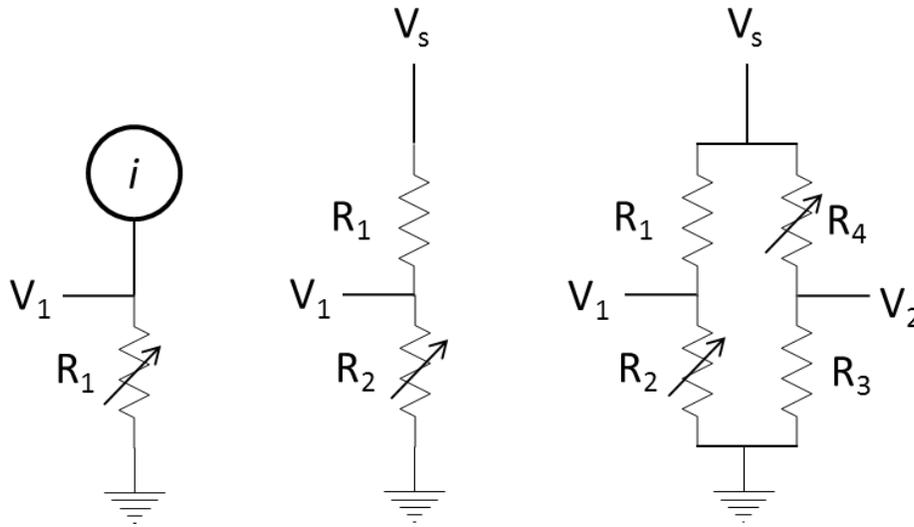


Figure 20: Various strain gauge measurement techniques

In the full bridge scenario, four resistors are placed in such a way that they are all equally heated, as with the half bridge, to eliminate thermal noise. Since the resistors change on the opposite side of the bridge, the signal is essentially doubling that of the half bridge. The sensitivity of this bridge is approximately $2V_s/R$.

The piezoresistors are placed at the points where the highest amount of stress that is delivered to the beam, as this will produce the largest change in resistance, giving a larger signal to noise ratio. While analytical equations have been developed to model general beam designs, more complex MEMS cantilevers require the assistance of finite element analysis in order to track the areas of highest stress.

In general, the points of highest stresses are located at the faces of the base of the beam, where the largest amount of strain occurs. This assumes that the spring constant of the entire beam is the same. When different spring constants exist on the same cantilever, the portion with the lowest spring constant generally receives more of the strain. This is easily seen in a finite element analysis (FEA) in Figure 21. The areas of green have no stress, while areas of blue contain areas of compressive stress, and areas of red contains areas of tensile stress.

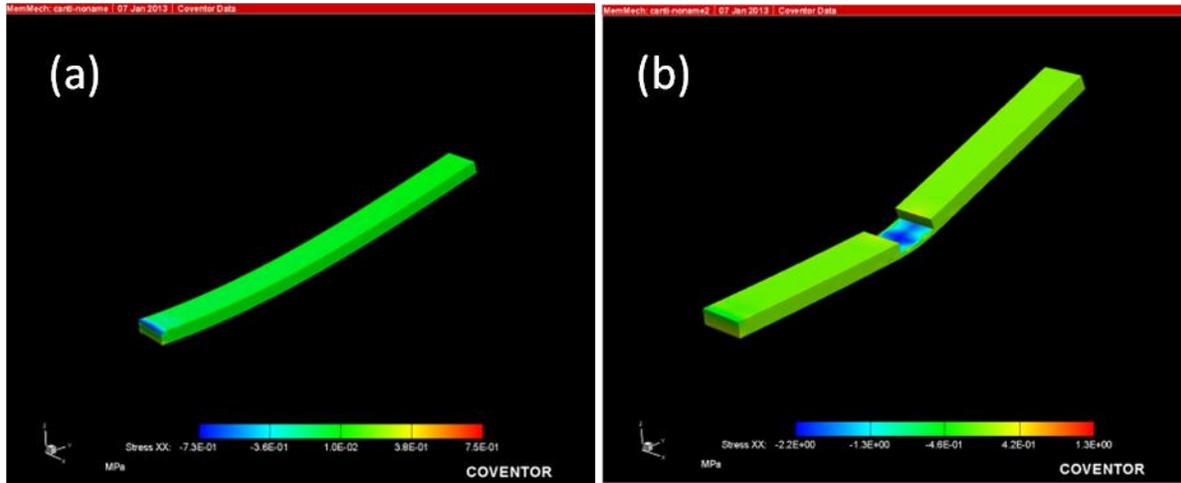


Figure 21: Finite element analysis on stress of beams with different geometry

From Figure 21a, it is easy to see that the piezoresistors should be placed at the very left, where the beam contains areas of stress, whereas in Figure 21b, it should be placed in the middle, where the stress is the highest.

The last important aspect of MEMS integration is the introduction of microscopic XYZ-stages. The use of thermal, electrostatic and magnetic actuation is a popular topic in MEMS. In the case of [59], a comb drive is used to electrostatically move a beam. A set of interdigitated beams are placed parallel to the direction of the intended movement. This can be seen in Figure 22.

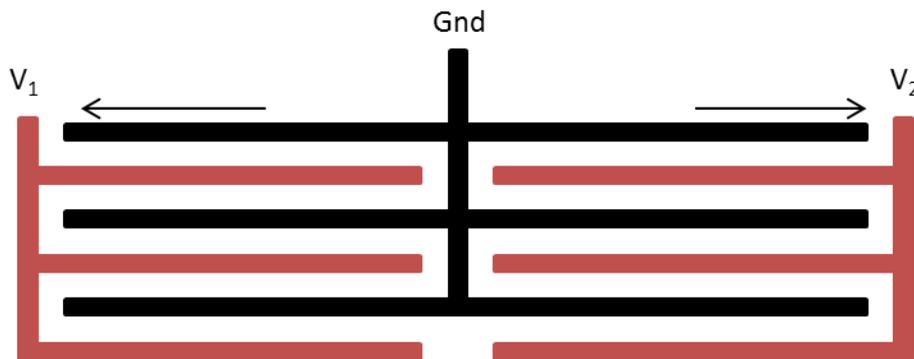


Figure 22: Translational MEMS stage based on interdigitated capacitors

When a large voltage is placed between the stationary fingers and the translational fingers, they are pulled towards each other due to electrostatic charge build up. This method allows for relatively high displacements that require low work requirements, as there is no current flowing through the system. However, a large amount of space is required in order to build a large system of fingers that can displace a beam a considerable distance.

Thermal actuation is another solution for MEMS-XYZ stages. As current passes through a resistor, the material begins to heat due to Joule heating. Charged particles flow through a circuit, from the influence of an electric field. As the particles hit the ions of a conductive path, energy is given off in the form of heat. Raising the current causes more particle collision, and results in a higher output of thermal energy. Due to the size of MEMS devices, Joule heating can cause controlled deformations of a device, resulting in physical displacements.

There are many different thermal actuator designs. Chevron, hot-arm, cold-arm and bimorph actuators are shown in Figure 23a, 23b and 23c respectively. Chevron actuators have been modeled extensively [60, 61]. They function by using Joule heating to deliver an equal distribution of heat through the chevron arms, as the resistances of both arms are similar. This allows the equal thermal expansion in the direction of the point in the chevron. This displaces the point forward in a straight path. These devices are used extensively, and reported in [62]. While the amount of displacement is much less than other methods, the extremely stiff spring constant in all three cardinal directions gives an advantage.

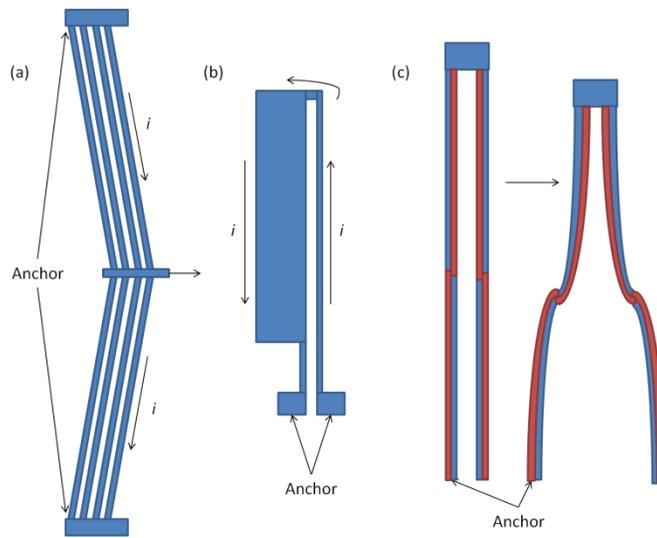


Figure 23: Different types of thermal actuators

The hot-arm, cold-arm actuators allow the Joule heating through material layers with different resistances. A higher resistance will yield a higher current density, resulting in a hotter arm. From Figure 23b, the thin arm is higher in sheet resistance, due to the geometry of the cross section. The temperature difference will cause the thinner hot-arm to expand more than the cold arm, hence deforming the structure [63]. This method generally yields low Z spring constant due to the length of the beam being proportional to the amount of displacement.

Bimorph actuators encase two materials with vastly different thermal expansion coefficients. Typical lateral bimorph actuators have been made from silicon dioxide and aluminum layer using CMOS-MEMS based processes. The thermal expansion coefficient of aluminum is roughly an order of magnitude larger than that of silicon dioxide. Due to the high temperature fabrication process, once the bimorphs have been released, residual stresses cause the beams to self-assemble into a stress free state, resulting in an initial displacement. Current is passed through a set of resistors, made of polysilicon in the CMOS process, which heats the beams of the bimorph actuator. The aluminum encased in the beam expands, causing the structure to move towards its pre-released state. Further addition to the temperature allows the beam to move further than its pre-released form. Certain geometric configurations shown in Figure 24 reduce the parasitic movement in non-lateral directions. Works such as [7, 64] have shown that bimorphs can create an XY-stage. Thermal coupling from one actuator to another may cause the stage to move in an unwanted direction. However, correction factors can be introduced to limit obscurities from the coupling.

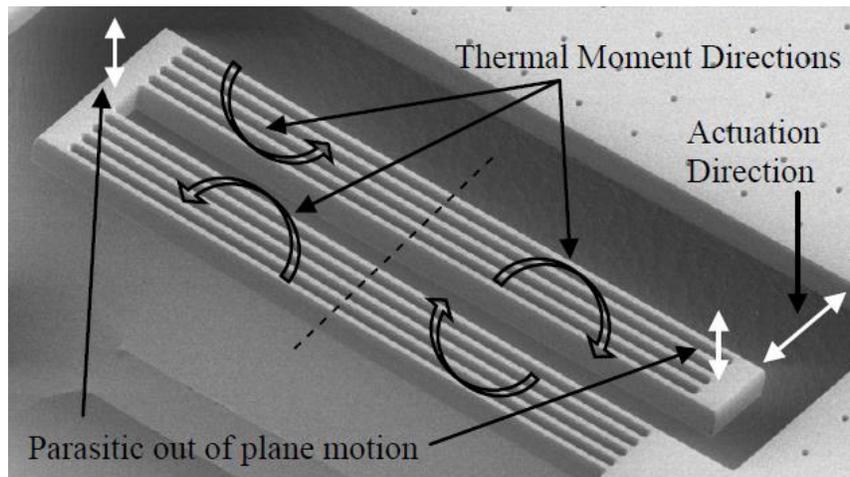


Figure 24: Demonstration of bimorph actuator

A popular medium for SPM-MEMS integration is through the CMOS-MEMS process. With the continual development of silicon technologies, the CMOS process has been able to evolve quickly. Within the past few decades, the reduction in the technology feature size has allowed for high levels of innovation. While contemporary processes are in the 46 nm range, processes in the 350 nm range have become cheaper and cheaper. Because of this fact, many technologies and processes have been developed to create a MEMS device from the CMOS process [65].

Throughout the past decade, a large number of new works have demonstrated the feasibility of this technology. In [cmosmemssensor], the technology is used to create a humidity sensor, incorporating a comb drive sensor. By far, the CMOS-MEMS sensor is one of the quickest ways to develop an extremely

sturdy, low stress comb drive sensor. The highly vertical walls of the finished device produce a high signal to noise ratio without consuming a large amount of space.

Another advantage of the CMOS-MEMS process is the ability to create a floating parallel plate capacitor that yields a high Q. The capabilities of using this device as a resonator with a Q of at least 4000 are documented in [66]. An application of these resonators is to create RF-MEMS devices. As noted in [5], the process is used to create a CMOS-MEMS variable capacitor with large tuning variability. The variability can be piezoresistively sensed using integrated polysilicon piezoresistors.

In the realm of CMOS-MEMS AFM's, the first device with integrated circuits was shown in [67] where an array of cantilever beams with integrated piezoresistive sensors and CMOS readout circuitry was fabricated on the same chip. The changes of piezoresistance resulting from the deflection of the cantilevers are amplified and recorded. The cantilevers contain a Z-dimensional bimorph actuator which allows the cantilever to controllably deflect while maintaining the same force feedback.

Further work has been shown in [7] where integrated bimorph beams create an XYZ-stage that compliments a fully functional cantilever beam with piezoresistive sensing. Thus far, a contact mode device has been created with future work related to dynamic mode SPM.

The use of KPFM has not been demonstrated with MEMS devices, however, using a similar idea, a current controlled Kelvin probe method has been developed [27]. In this work, a microscopic probe is fabricated with a conductive tip. As the tip vibrates close to the sample, charge transfer will occur, creating a current that can be measured. The bias delivered to the sample is changed until there is no current. At this point, the contact potential difference is observed. However, this device suffers as the current detected from the Kelvin probe is already quite tiny. The tip current is observed to be approximately 500 fA, which means that the signal must be extremely low noise in order to take an accurate measurement.

3. KPFM Design and Simulation

Most of the KPFM progress is directed towards materials characterization research. The instrument cannot be adapted to industry due to its immense cost and low throughput for a decently niche set of applications. To obtain a precise image, a large amount of set up time, trial and error, as well as luck can play a role in getting a truly sub-atomic image. In most cases, other methods, although not optimal, can be utilized instead. The goal of this research is to combine the KPFM with MEMS technology. This not only helps to limit the cost, but also increases the ease of use and increase throughput with the possibility of cantilever arrays.

In order to construct a KPFM, it is important to understand the underlying theory and basics behind the technique, how it functions, and how a cantilever is utilized to track the forces that the tip experiences.

3.1. Theory

The KPFM is an important tool in understanding the work function and local surface charges. The work function, ϕ , is a property of all materials. It is the amount of energy that is needed to remove an electron from the surface of a material. In other words, it is a measure of electron volts between the Fermi energy level and vacuum. In a given atom, there exist many states for an electron to reside. As the number of atoms begins to increase, the material begins to build bulk properties (the energy levels begin to broaden, creating an energy band). In a metal, for example, the conduction band and valence band are merged together (there is no band gap). However, there exists a Fermi energy, which is the highest occupied space. Within this band, electrons are confined to the atom at varying energies. Once enough energy has been given to an electron to pass the Fermi energy, they are free to roam within the material lattice. This is called the conduction band. Beyond the conduction band, the electron is able to escape the surface of the material itself. This is known as the vacuum level.

The amount of energy to eject the electron from the surface is called the work function. The work function is closely related to the contact potential difference, V_{CPD} , as defined by:

$$\Delta\phi = eV_{CPD} \quad (3.1)$$

Additional impurities and charges add to the contact potential difference. When two materials with different work functions (Figure 25a) come into close contact, the Fermi energy levels will align, while

their respective work functions will remain the same (Figure 25b). The difference between the work functions is called the contact potential difference [20]. At this point, due to the voltage difference, a current will flow to align the Fermi levels. A charge will build up between the materials due to the difference in V_{CPD} . A bias, V_{DC} , can be applied between the two materials at the same magnitude, but opposite direction of the contact potential difference such that the vacuum levels align (Figure 25c). When the vacuum levels align, the charges will disappear. Initially, experiments were carried out with an electroscope, such that when charge transfer occurs, the electrons that have gathered at the material edge will cause the gold leaf to displace.

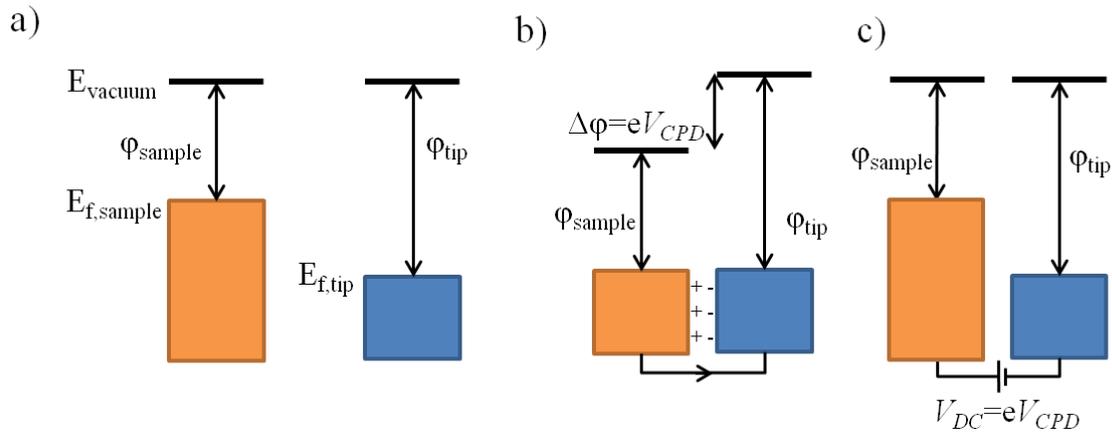


Figure 25: KPFM operation principle

In the interest of KPFM, the charges that build on the surface of the materials will create a force that will affect the deflection of the cantilever. Once the V_{DC} is aligned with the V_{CPD} , the charges disappear along with the force. This is detectable with the KPFM. If the work function of the tip is known, then the work function of the sample can be measured to an absolute value. However, relative measurements of the work function can show many specific properties of the sample at hand. Samples with different materials will have different work functions. Impurities and different crystal orientations will also alter the resultant work function. Hence, the absolute work function is not necessary in order to obtain an image.

The KPFM measures the local contact potential difference, which is influenced not only by the bulk material properties, but the surface as well. A fully crystalline lattice will roughly have a similar contact potential difference, V_{CPD} across the sample surface (this is assuming that this is not in a sub-atomic resolution where there will be small changes in the V_{CPD} due to very small spacing between atoms). On the other hand, a crystalline lattice with an extra atomic absorbates will increase the local surface energies due to extra states outside of the bulk regime. The KPFM will be able to detect a relatively large change in comparison with the rest of the crystal lattice.

The actual measurements performed by the KPFM are realized by applying both an AC and DC voltage component to the KPFM tip. The AC signal, V_{AC} generates oscillating electrical forces, F_{es} , that exist between the tip and the sample. The DC voltage, V_{DC} , is used to change the Fermi energy in order to match the vacuum energy. The overall electrostatic force experienced between the tip and sample is given by:

$$F_{es}(z) = -\frac{1}{2}\Delta V^2 \frac{dC(z)}{dz} \quad (3.2)$$

The C represents the capacitance with respect to the height difference between the tip and the sample. The voltage given in the equation above is a combination of the difference between the V_{CPD} and the V_{DC} voltage as well as the AC signal:

$$\Delta V = (V_{CPD} \pm V_{DC}) + V_{AC} \sin(\omega t) \quad (3.3)$$

The term is squared, which equals to:

$$F_{es}(z) = -\frac{1}{2}[(V_{CPD} \pm V_{DC}) + V_{AC} \sin(\omega t)]^2 \frac{dC(z)}{dz} \quad (3.4)$$

$$F_{es}(z) = -\frac{dC(z)}{dz} \left[\frac{1}{2}(V_{DC} \pm V_{CPD})^2 \right] - \frac{dC(z)}{dz} (V_{DC} \pm V_{CPD})V_{AC} \sin(\omega t) + \frac{dC(z)}{dz} \frac{1}{4}V_{AC}^2 [\cos(2\omega t) - 1] \quad (3.5)$$

The electrostatic force is divided into three separate portions:

$$F_{DC} = -\frac{dC(z)}{dz} \left[\frac{1}{2}(V_{DC} \pm V_{CPD})^2 + \frac{1}{4}V_{AC}^2 \right] \quad (3.6)$$

$$F_{\omega} = -\frac{dC(z)}{dz} (V_{DC} \pm V_{CPD})V_{AC} \sin(\omega t) \quad (3.7)$$

$$F_{2\omega} = \frac{dC(z)}{dz} \frac{1}{4}V_{AC}^2 [\cos(2\omega t)] \quad (3.8)$$

The F_{DC} portion describes the static deflection of the tip. The F_{ω} and $F_{2\omega}$ can be used to determine the contact potential difference. As one can see, the signal output given by the cantilever will be the sum of all the forces. With a sine and cosine term in the force equation, the signal becomes a mixture of both waves. As the $V_{cpd}=V_{DC}$, the F_{DC} and F_{ω} term disappear, leaving the $F_{2\omega}$ term. Once the wave seen in the result is twice that of the AC signal, the F_{DC} and F_{ω} will be equal to 0 [22].

Both the topology and the surface potential can be captured at the same time. Since the surface potential is influenced by the potential difference and the offset, the first frequency oscillation will be used to track the work function. On the other hand, the second harmonic frequency is based only on the height difference between the sample and the substrate since the AC signal is always constant.

To replace the KPFM system with a MEMS device, it is important to start with similar characteristics. This chapter deals with the development of a KPFM cantilever beam. In order to have a successful KPFM system, the proof of concept of the integrated KPFM CMOS-MEMS device must be validated. A mechanical and electrical simulation of the device is presented, as well as preliminary research data.

To quote, a KPFM system can operate in either frequency modulated, amplitude modulated or lift mode. Each of these modes requires a cantilever beam of a different stiffness. More commonly, lift mode is not used due to the low resolution. In the case of frequency modulated KPFM, the cantilever stiffness is upwards towards 50 N/m [22], operating at a resonant frequency in the 100 kHz regime, with a Q of over 100 [1]. This mode allows the cantilever to approach the sample very closely. The high spring constant prevents the sticking of the beam to the water layer, and allows for a much more intimate scan, allowing a higher resolution. A signal far from the resonant frequency is driven to operate the device. Side bands form from the mixing of the signals, which are observed with a lock in amplifier. Once the bias matches the potential difference, the sidebands disappear, thus tracking the surface charge.

On the other hand, amplitude modulated KPFM tracks the beam's amplitude. When the surface charge of the cantilever and the sample align, the amplitude of oscillation will be zero. To ensure a high signal to noise ratio, a beam without an aligned work function should be oscillating at high amplitudes. This means that the cantilever must be placed further from the surface, and typically results in a lower spring (1-10 N/m) constant to ensure high amplitudes [22]. The cantilever is usually operated at the resonant frequency to let the Q contribute to the amplitude signal, which means typical Q values should also be very high.

3.2. Design Considerations

When considering MEMS implementation, it is important to mimic the structural characteristics of the conventional cantilever. Since typical KPFM cantilevers are created with metal coatings, similarly, the MEMS-KPFM must also be metal. This is to ensure that the voltage signal is delivered to the tip, allowing interaction with the sample.

In the case of mechanical stiffness, the beam should be in the range of 1-50 N/m, depending on the mode of KPFM operation. In order to obtain a high stiffness, certain criteria must be met. The spring constant, k , of a cantilever beam is determined analytically using the formula:

$$k = \frac{Ewt^3}{4L^3} \quad (3.9)$$

where E is the Young's Modulus, w is the width of the beam, t is the thickness, and L is the length. The higher the spring constant, the stiffer the beam becomes. The length, width and thickness of a Z-directional stiffness is demonstrated in Figure 26. To increase the stiffness of the beam, it can be analytically observed that the length should be limited, while the width and thickness of the beam should be increased. However, increasing the thickness of the beam is no simple task. In terms of microfabrication, the length of time to create the device scales with the thickness of the beam. This is due to the precise and controlled depositions used to create the device. Creating a beam that is 20 μm instead of 1 μm would take at least 20 times the amount of time. This does not factor in other detrimental effects during etching. A large amount of time is needed to etch high thickness films anisotropically. Also, extremely thick cantilever beams may suffer through high levels of stress, causing unwanted deformations.

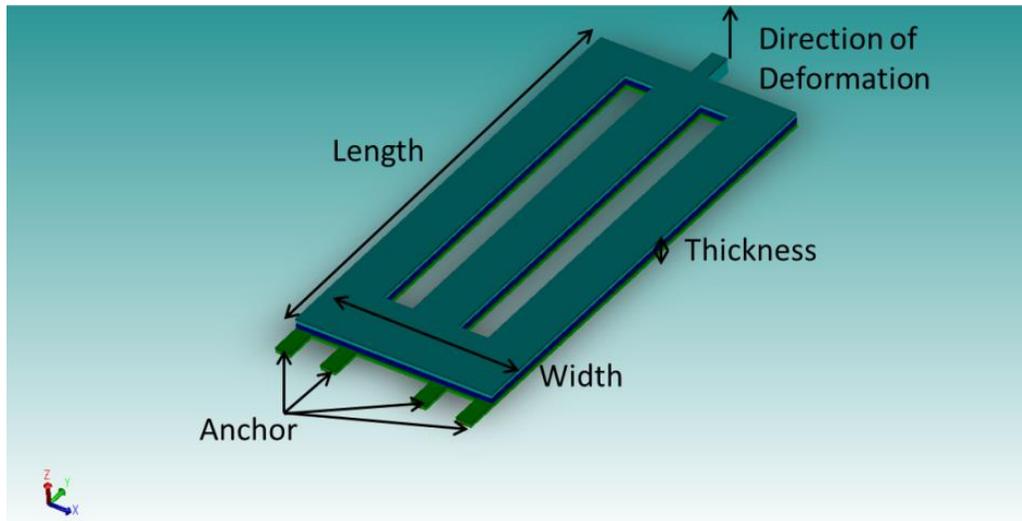


Figure 26: Stiffness of a beam based on Z-directional stiffness

One may consider shortening the beam to mitigate the decrease in the stiffness value; however, this produces another problem. When considering the use of piezoresistors, the resistance change is due to the amount of strain of the material. To produce this strain, a larger bending moment must be applied to the beam. This large bending moment is dependent on the length of the beam. This concludes that a longer beam results in a larger signal from the piezoresistors. Optimization can be performed to determine a

beam geometry for a certain spring constant to give high levels of stress output. It also implies that a longer length, lower spring constant would be more optimal for a piezo-sensing cantilever. In this case, since amplitude modulated KPFM uses spring constants from 1-10 N/m, piezoresistive cantilevers would be the preferred method of displacement sensing.

In terms of capacitive sensing, to create a large change in capacitance, the parallel fingers must have a high thickness, to increase the capacitance value. In order to obtain a high signal to noise ratio, a large amount of fingers must be present. Also, since KPFM involves the use of a signal, parasitic coupling could disturb the sensing capabilities of the device. In any case, shielding should be considered in such a design. The advantage of using the capacitive sensors is the ability to increase the spring constant of the beam with more ease. In the case of the piezoresistive beam, the sensor is generally placed at the end of the beam, where the cantilever will be deformed out of plane. This puts the stiffness in the hands of the thickness of the process, and the length of the beam. In terms of a capacitive sensor, the beam is deformed in plane, and the “thickness” refers to the width of the beam, since it will be dependent on the Y dimensional spring constant, as seen in Figure 27. Referring to equation 3.8, this means that the stiffness is cubically dependent on the lateral width of the beam. This allows the same processing thickness (or number of layers) to be the same, and varying the width of the beam will determine (at least to a greater degree) the stiffness. Changing the geometry to support a high Y-dimensional stiffness is much simpler than changing the Z-dimensional geometry. Hence, in the case of capacitive sensing, it may be more practical for use as a frequency modulated KPFM.

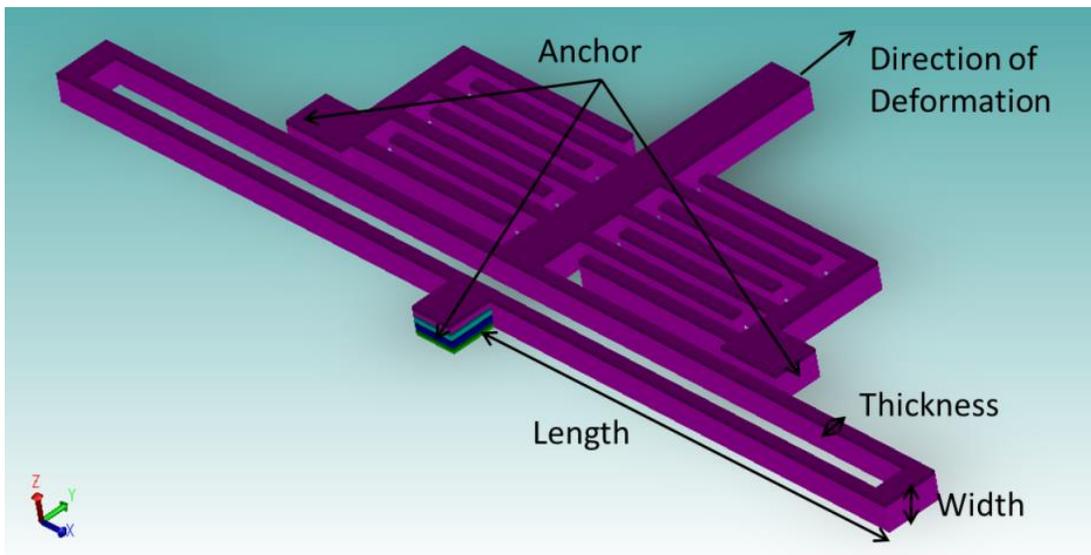


Figure 27: Stiffness of a beam based on Y-directional stiffness

For the purposes of this thesis, while both have been fabricated, only the piezoresistive device is shown for brevity.

3.3. Fabrication Process

The easiest method to incorporate all these constraints is to use the CMOS-MEMS process. Due to the reduced cost, and consistency in CMOS-processing technology, CMOS-MEMS is quickly becoming an important contender in MEMS fabrication technologies. It also incorporates many important aspects to fully realize a MEMS KPFM. The fabrication process used to process the CMOS devices as a loose die is offered by the Taiwanese Semiconductor Manufacturing Company (TSMC) in partnership through the Canadian Microsystems Corporation (CMC).

The 0.35 μm CMOS-MEMS process is used to fabricate devices for experimental validation in this work. The 0.35 μm CMOS-MEMS process contains 4 planarized aluminum metal layers. For conventional CMOS systems, these are used as routing layers. For the development of MEMS technologies, the aluminum is used as a structural layer, as well as routing for internal sensing circuitry. The stack of 4 aluminum layers with a layer of insulative oxide in between allows for the fabrication of thick structures, which is important in the fabrication of stiff cantilever beams. Following the provided design rules, the 0.35 μm CMOS process allows for a conservative MEMS structure that are 1 μm in width, which also allows for heavy miniaturization.

The 4 aluminum layers can be used as routing with the use of tungsten via holes. During the fabrication process, holes are etched into the insulative oxide layer, which is later filled with tungsten. These tungsten plugs are used to connect the insulated aluminum layers together.

The 0.35 μm CMOS-MEMS process also includes 2 polysilicon layers. In generic CMOS processes, these two polysilicon layers are used for transistors. However, in the CMOS-MEMS process, these are used as piezoresistive sensors. The two different polysilicon layers provide different resistivity values. The higher resistivity polysilicon is used in the mechanical design as it is better suited towards strain sensing applications. These polysilicon layers can be connected to the bottom aluminum routing layer through tungsten via holes.

The CMOS chip can be seen in Figure 28. The four aluminum layers (green), named M1, M2, M3 and M4 are insulated from each other with an oxide layer (light grey). However, the layers may be connected

together through tungsten via holes (orange). Below the metal stacks, a polysilicon layer (red) can be identified. These are used as the piezoresistive sensors.

In addition, the CMOS process also allows for embedded electronics. The doping of the substrate before the deposition of aluminum metallization layers allows for transistors to be created, allowing integrated circuitry that may interact with the device. Often, on chip amplifiers can be created, allowing amplification of the signal before being read by an instrument, hence, improving the signal to noise ratio. Readout circuitry can also be utilized using the embedded electronics, hence creating a self-sustaining device with minimal outside influence.

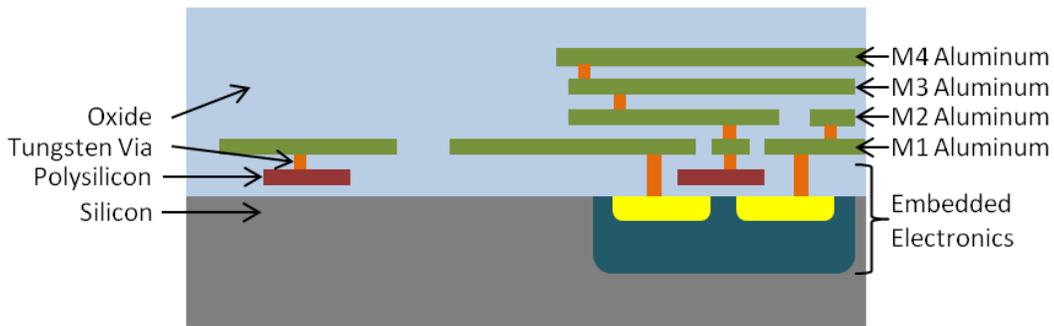


Figure 28: Fabricated CMOS Device

Once the CMOS design returns from the foundry, a post-processing etch must be performed in order to release the structures. The designs come in the form of a loose die, with a cross section not unlike that which is shown in Figure 28. Since there is a possibility of the loose die interacting with the environment between post fabrication and receiving, the die must first be cleaned. Each individual die is placed into a small beaker with a small amount of acetone, enough to cover the die. Each die is allowed to sonicate in the acetone beaker for a minute. This allows many of the organic materials to be removed from the surface of the die. Afterward, the chips are placed into DI water, as evaporating the acetone covered chip may result in an unwanted film. After a minute of soaking in the DI water, the loose die is removed and placed on a preheated Petri dish, where the die is allowed to air dry under a nitrogen environment.

A post-processing technique is then used to release the mechanical structures. The first step is to remove the oxide layer such that the silicon is exposed, as seen in Figure 29. The loose die is placed into a reactive ion etching (RIE) system with a specific oxide etching recipe. The specific process used to release this set of devices involves etching the die with a constant 50 sccm flow of pure CHF_3 . The ICP and RIE power of this recipe is 200 W and 52 W respectively. This power allows the reaction between the CHF_3 and the oxide to slowly remove the oxide layer, creating Teflon based polymer around the chamber. This polymer slows down the etching process, as the Teflon deposits on the chamber walls, and may be

subsequently redeposited back onto the loose die. This results in longer etch times, which may cause unwanted milling of the aluminum, weakening the device and allowing for premature failure. Hence, to prevent overly long etches, the chamber was cleaned every 30 minutes of oxide etching, removing the polymer from the chamber. The processing time to remove the oxide layer, without the cleaning step, is approximately 2 hours.

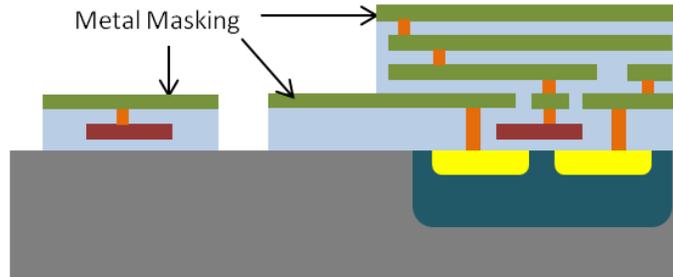


Figure 29: Post silicon oxide etch

The aluminum metal layers act as a mask for the underlying oxide layer. Only the exposed oxide is etched away in this fairly anisotropic process. Fairly straight side walls can be resolved through this process, although a conservative measure is placed upon the polysilicon resistors. These are kept at least 1 μm away from the edges of the metal masking. This is to ensure that later silicon processing will not etch away the polysilicon resistors. Also, all important features such as the tungsten via holes are kept further from the edge of the metal masking to ensure that they are not exposed.

After the silicon is completely exposed, the next step is performed. The recipe involves flowing 30 sccm of SF_6 with a RIE power of 50 W. This process allows for the exposed silicon to etch. Unlike the previous anisotropic etch, this isotropic etch allows underetching of the silicon, allowing for the release of the structure. The polymer deposited on the side walls of the device in the previous step help to preserve the vertical side walls, as well as protects the polysilicon from etching away. A larger structure will take a longer time to be released; this is seen in Figure 30. Creating large structures will ensure that the devices can be properly anchored, while smaller beams will be released into a free floating device that may interact sensitively with the environment. This process is run for 1 minute, before stopping for 1 minute to limit the residual heat generated from the plasma. The resultant thermal expansion, due to the difference in the coefficients of thermal expansion (CTE) between the aluminum and oxide layer, may cause cracking in the device. Approximately 15-20 minutes of processing time is necessary to fully release the structures.

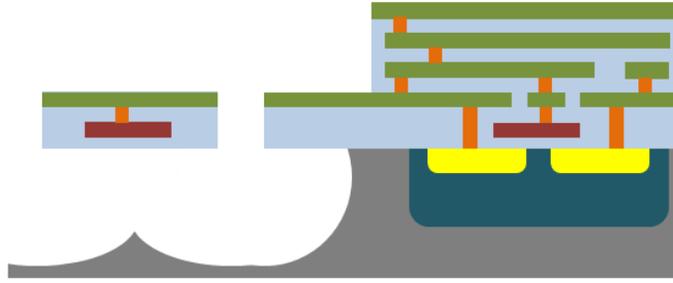


Figure 30: Silicon etching in the CMOS-MEMS release process

After the devices are released, the CTE will result in stresses within the structure. The structures deform to relieve the stress, as seen in Figure 31. Due to the nature of the material and processing temperatures, the aluminum will experience parasitic tensile stresses and the oxide layer will experience parasitic compressive stresses. Stacking 4 layers of metal will prevent mass deformation.

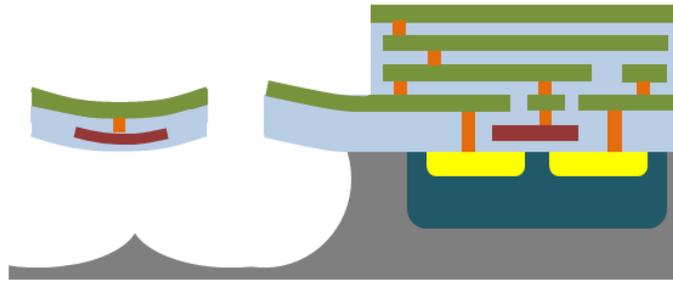


Figure 31: Deformations from residual stress after post-processing

3.4. Beam Simulation and Design

An FEA is performed in a commercial MEMS software called Coventorware to determine the stiffness of the beam, and the area of the highest stress. Two cantilevers with similar geometries are realized; each one with a different methods of piezoresistor placement. Both methods involve a full bridge circuit. The cantilever beam is created with a length of 135 μm , and a width of 65 μm . The cantilever beam will be created using the aluminum layers: M1, M2 and M3. The M4 will be used as the tip that protrudes further out of the cantilever. In addition, holes are added to the cantilever beam in places that do not largely influence the beam stiffness. These holes are added in order to aid the release process. Since under etching requires a large amount of time, the addition of holes will help to reduce the processing time. This

may save the top metal from deterioration from the plasma during the etching process. A further $15\ \mu\text{m} \times 5\ \mu\text{m}$ protrusion will jet out of the cantilever in order to hold the tip away from the cantilever. The piezoresistors are located at the base of the cantilever with M1 acting as the metal mask. The metal mask acts to protect the polysilicon from the silicon etch in the RIE. Only M1 is placed over the polysilicon piezoresistor, as increasing the thickness will reduce the amount of applied strain on the piezoresistor. The dimensions of the M1 covering the piezoresistors are $10\ \mu\text{m} \times 5\ \mu\text{m}$ and are placed behind the cantilever. The polysilicon underneath has a size of $8\ \mu\text{m} \times 2\ \mu\text{m}$. The M1 metal can be reduced in width to increase the applied stress, but at the same time, will vastly lower the spring constant. The final beam size is $145\ \mu\text{m} \times 65\ \mu\text{m}$. An FEA is first performed to understand the characteristics of this beam.

Figure 32 shows an FEA of the proposed design. Through the use of FEA, it is determined that the areas of highest stress are located near the base of the resistor. The piezoresistors located at the base of the cantilever shows a maximum stress of $7.3\ \text{MPa}$ when $1\ \mu\text{N}$ of force is applied in the Z direction to the tip. A displacement of $0.39\ \mu\text{m}$ shows that the stiffness of the beam is approximately $2.56\ \text{N/m}$, using the formula:

$$k = \frac{F}{d} \tag{3.10}$$

where the stiffness k , is the force applied divided by the displacement observed.

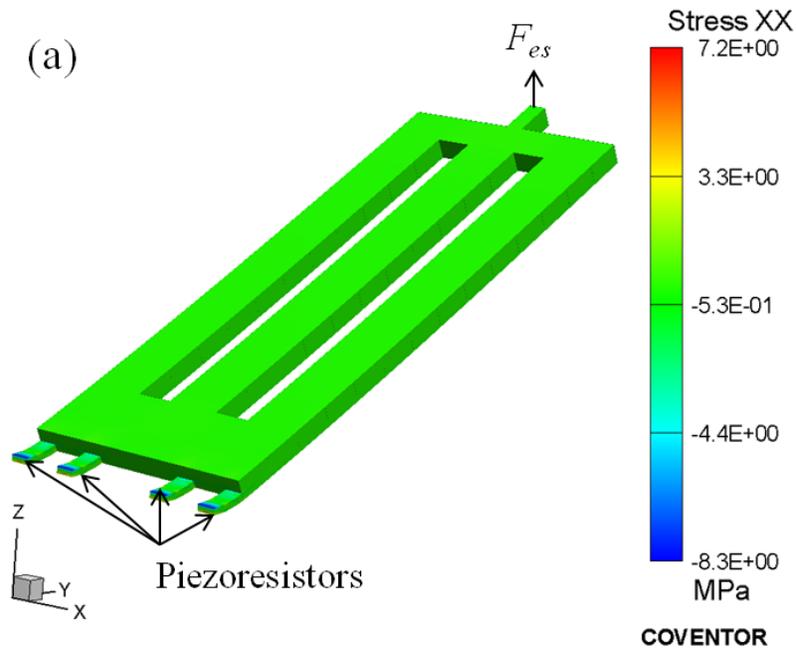


Figure 32: Finite element analysis of first proposed cantilever geometry

Assuming each resistor has R resistance, and deflect at the same rate, the resistors all experience stress in the same direction. Due to this, there is only one method to create a full bridge sensor. Figure 33 shows the piezoresistors within the bridge. Dummy resistors must be placed to balance the bridge and to dissipate thermal lumping effects from the current running through the piezoresistors. Since they only operate with tensile stress, the sensors may only be placed on the opposite side of the bridge, else, negating the effect of the bridge. When applying V_s to power the bridge, the voltage output will be:

$$V_{output} = V_1 - V_2 = V_s \left(\frac{R_2 + \Delta R}{R_1 + R_2 + \Delta R} \right) - V_s \left(\frac{R_3}{R_3 + R_4 + \Delta R} \right) \quad (3.11)$$

Since all the polysilicon resistors are the same size, they will each share the same resistances:

$$V_{output} = V_s \left(\frac{R + \Delta R}{2R + \Delta R} \right) - V_s \left(\frac{R}{2R + \Delta R} \right) = V_s \left(\frac{\Delta R}{2R + \Delta R} \right) \quad (3.12)$$

The change in resistance is linearly dependant on the stresses that are applied onto the polysilicon; the larger the stress, the larger the voltage signal output.

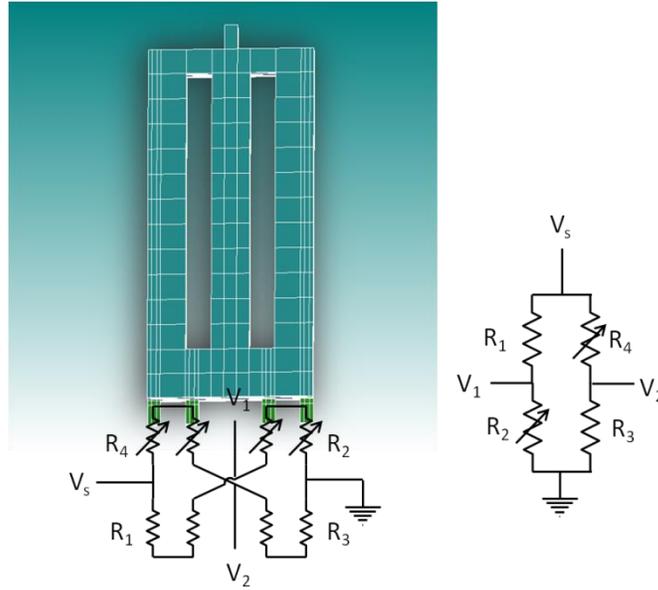


Figure 33: Full bridge configuration of first proposed cantilever geometry

In order to increase the spring constant of the beam, the length must be shortened, and the width must be increased. FEA was performed to determine the changing spring constant with respect to length; this can be seen in Figure 34. In this case, the length of the metal stack is increased. The length of the piezoresistor and the metal on top does not change. Again, a $1 \mu\text{N}$ force is applied to the tip of the cantilever. The maximum observable stress on the piezoresistor is also plotted as a function of length, as

seen in Figure 35. The maximum observable stress on the piezoresistor is based on the observance of this force.

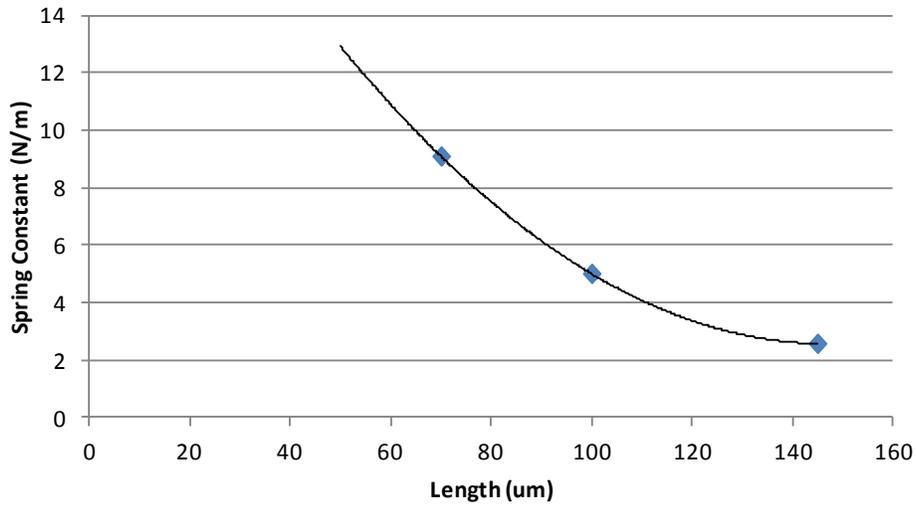


Figure 34: The effects of changing length with respect to spring constant of first proposed geometry

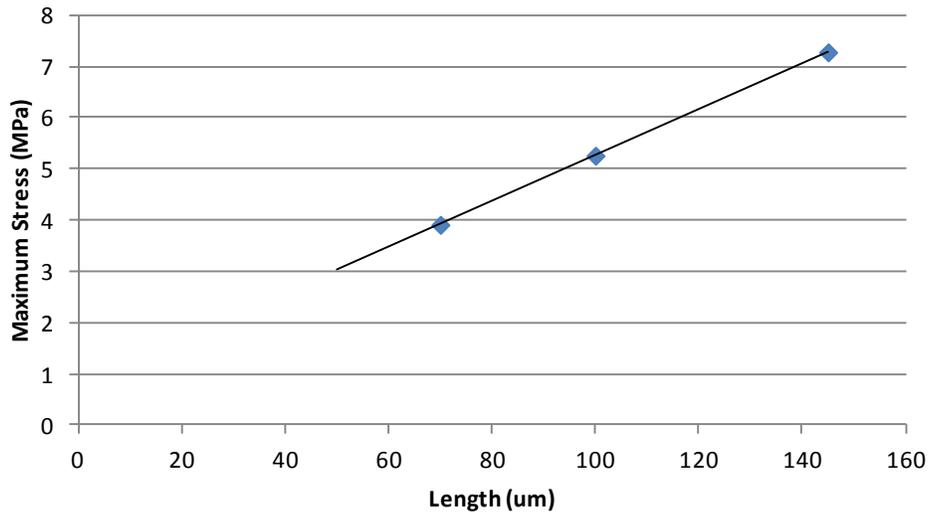


Figure 35: The effects of changing length with respect to maximum observed stress of first proposed geometry

Extrapolation is performed on three data points observed through FEA. Figure 34, again shows that at around a length of 65 μm , the stiffness of the cantilever will approach 10 N/m. From extrapolation, shown in Figure 35, the results show that the maximum observable stress is approximately 3.75 MPa when the length is 65 μm .

On the other hand, changing the width can also determine the stiffness of the beam. Figure 36 shows the effects of changing the cantilever width with the spring constant. Figure 37 shows the maximum observable stress on the piezoresistors while changing the width.

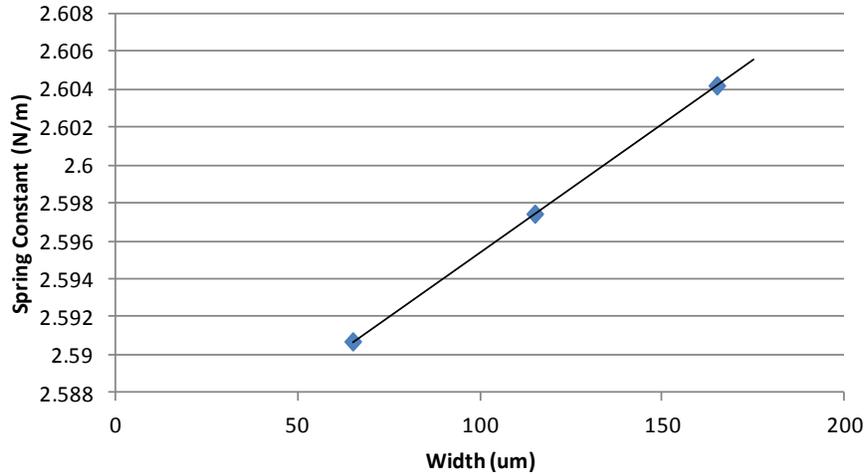


Figure 36: The effects of changing width with respect to the spring constant of the first proposed geometry

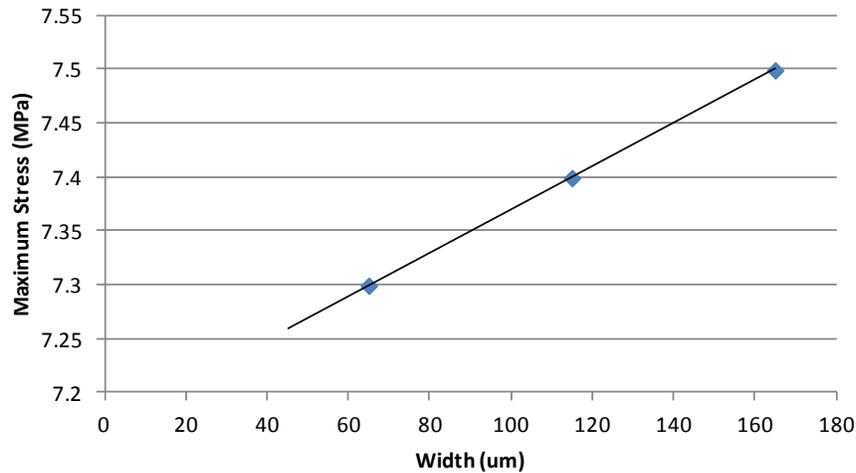


Figure 37: The effects of changing with respect to maximum observed stress of first proposed geometry

The width is extrapolated until the spring constant reaches 10 N/m; this width approaches 7418 μm . The maximum observable stress also increases. While the maximum stress does increase linearly with the width, the fact is that a 7418 μm width is unmanufacturable. Due to fabrication errors and yield percent from defects, this device has a high chance of failure. The stresses of large devices on the scale of 7.5 mm will probably be immensely high as well. The fabrication facility also does not accept designs that are larger than 5 μm x 5 μm .

One may consider changing both the length and width at the same time to obtain a spring constant of 10 N/m with a high maximum observable stress, but changing the length affects the stress in a much more detrimental way in comparison with the width.

It can be observed also, that only one direction of stress is observed in the piezoresistive sensors at one time. This means that only two of the piezoresistors may change in direction without negating the effects of the bridge. By incorporating the compressive stresses that also exist when a cantilever is displaced, a full bridge with two compressive resistors and two tensile resistors can increase the effective signal of the bridge. This leads to the second cantilever design, where the resistors are placed perpendicular to the cantilever instead of parallel.

Much like the previous design, the base cantilever is the same size; 135 μm x 65 μm with a 15 μm x 5 μm block that extends from the end of the cantilever for the tip. The M1 shielding the piezoresistor is 8.5 μm x 3 μm . This is pictured in Figure 38.

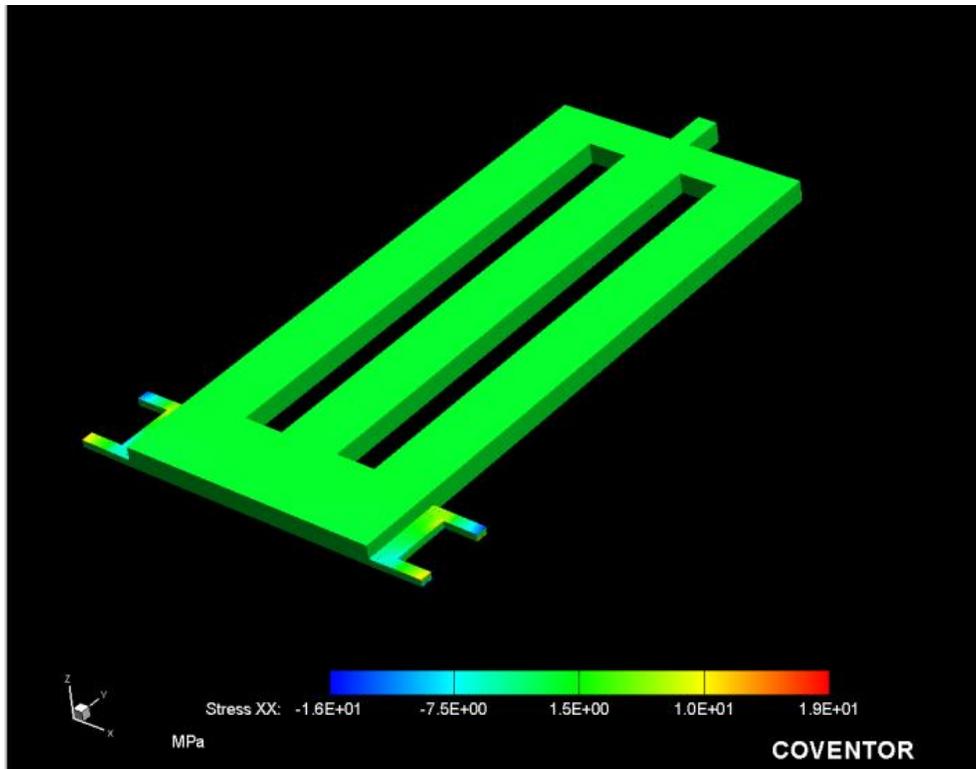


Figure 38: Finite element analysis of second proposed design

With the application of 1 μN of force on the tip, the cantilever deflects 0.12 μm . This gives the cantilever a spring constant of 8.33 N/m. The highest levels of stress are found at the edges of the support beam that

holds the cantilever. Two of the beams show 19 MPa of tensile stress (red), while the other two beams experience a compressive stress (blue) of approximately 16 MPa. Hence, the maximum difference in stress is 35 MPa, which is 5 times the value of the previous design. In addition, the spring constant is much closer to 10 N/m. The geometry does not need to be altered much in order to fulfill the requirements for a KPFM cantilever.

However, it should be noted that an additional signal line must be applied to the tip in order to use KPFM. The M1 lines shielding the piezoresistor are used to both deliver power the bridge circuit as well as sense the output voltage; hence, an additional line must be used to bring the signal to the tip of the cantilever.

In order to reduce the mitigation of stress onto the M1 beams, an additional bar should be placed on the axis of rotation. This is conveniently located between the piezoresistors that undergo compressive stress, and the piezoresistors that undergo tensile stress. A stack of beams with all three metal layers allows for a grounded shielding layer that will reduce the coupling effects been the signal line and the piezoresistors.

Another FEA is performed to obtain the stiffness and stress characteristics. This is seen in Figure 39. Figure 40 shows the piezoresistors of the same design under stress.

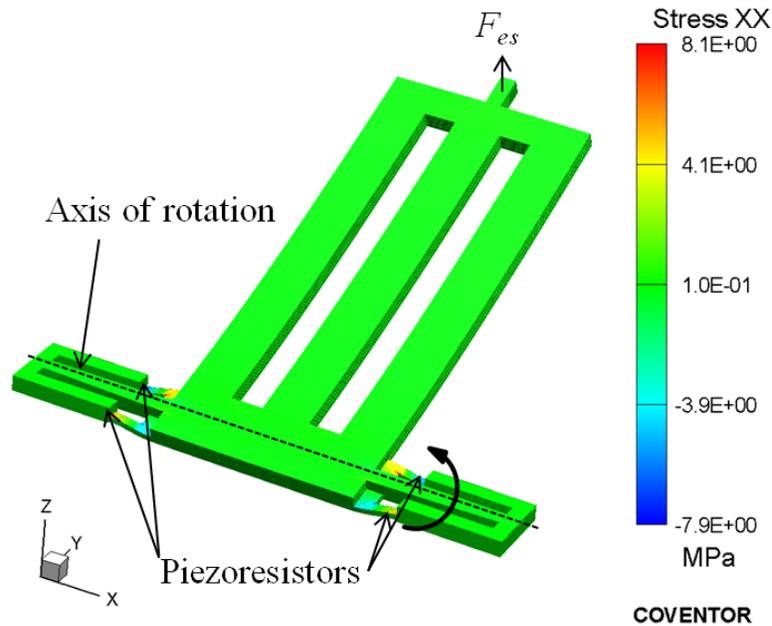


Figure 39: Finite element analysis of third proposed design

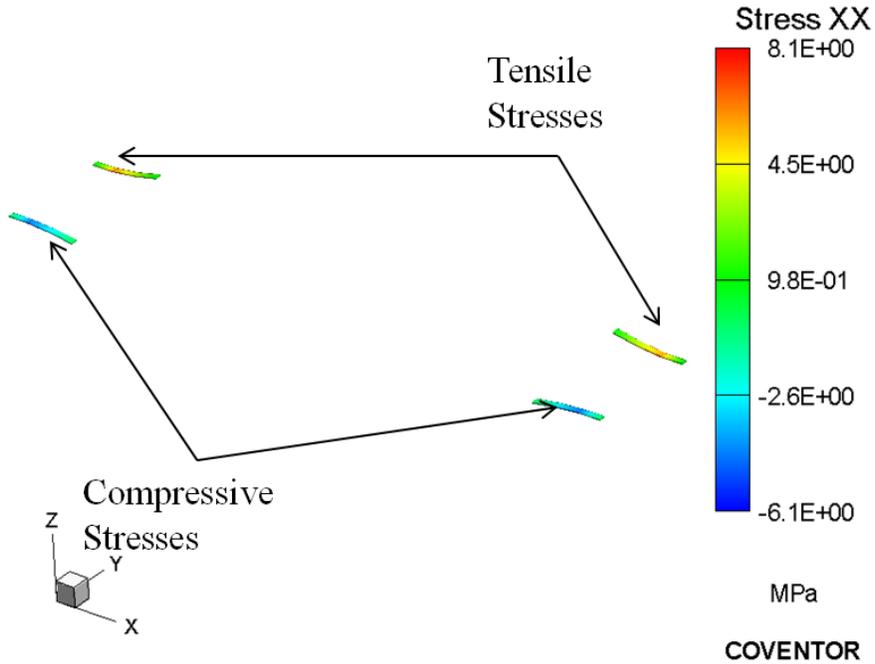


Figure 40: Piezoresistor stress of third proposed design

In this case, the spring constant increases to 10.98 N/m while the stress on the piezoresistors changes to a range of 14.2 MPa; 6.1 MPa of compressive stress, and 8.1 MPa of tensile stress. In this case, the spring constant is at a safe range to perform amplitude modulated KPFM, and at the same time, contains a large stress range.

Since two resistors undergo tensile stress, while the other two resistors undergo compressive stress, differential placement will aid in increasing the signal, seen in Figure 41. Since the cantilever beam is symmetric, it can be assumed that R_1 and R_3 will change in resistance at the same magnitude, while R_2 and R_4 will change in the resistance at the same magnitude, but in the opposite direction. This means that a fully differential bridge can be created.

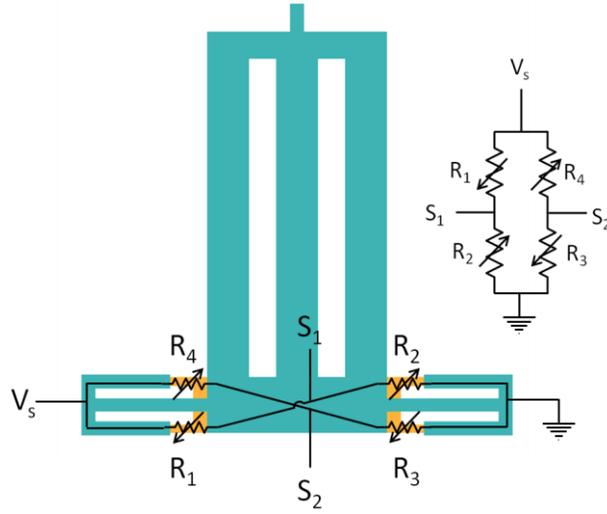


Figure 41: Differential Bridge of third proposed design

In this case,

$$V_{output} = S_1 - S_2 \quad (3.13)$$

$$V_{output} = V_s \left(\frac{R_2 + \Delta R_{tensile}}{R_1 - \Delta R_{compressive} + R_2 + \Delta R_{tensile}} \right) - V_s \left(\frac{R_3 + \Delta R_{compressive}}{R_3 - \Delta R_{compressive} + R_4 + \Delta R_{tensile}} \right) \quad (3.14)$$

Again, since all the resistances are the same,

$$V_{output} = V_s \left(\frac{\Delta R_{tensile} + \Delta R_{compressive}}{2R - \Delta R_{compressive} + \Delta R_{tensile}} \right) \quad (3.15)$$

Since the magnitude of change between $R_{compressive}$ and $R_{tensile}$ are similar, we can approximate that,

$$V_{output} = V_s \left(\frac{2\Delta R}{2R} \right) = V_s \frac{\Delta R}{R} \quad (3.16)$$

The differential voltage output from this design rises much more steeply with the change in resistance in comparison with the purely tensile design. The range of stresses experienced is also much higher. Internal electrical systems, including the bridge circuit is built within the device. The addition of the central beam brings the AC signal to the tip. To improve the scan resolution, the coupling between the cantilever beam to the sample must be minimized. The only effects the cantilever should have on the surface are through the tip signal. Hence, the rest of the cantilever must be grounded.

It should be noted that this also causes coupling in the MEMS device, between the signal line and the shielding [33]. The shielding layer is directed to an external pad for biasing, but the control of the biasing is beyond the scope of the current work.

3.5. Beam Optimization

Many iterations of the KPFBM have been designed through the five design tape outs, and are outlined in Appendix A. From this generation of device, many logistical shortcomings have needed fixing. Firstly, the beams delivering the signal to the cantilever must be moved further from the piezoresistors. The proximity of the lines causes a coupling effect between the AC signal and the piezoresistors. This is investigated in Chapter 5. Nevertheless, the routing must be changed to reduce the amount of coupling between the elements. In addition to additional metal shielding between the signal line and the piezoresistors, physical distance is increased to reduce the amount of coupling.

Secondly, the previous design only focused on the basic placement of the piezoresistors. The actual geometry and size of the beam and other features are not thoroughly investigated. Simulations are performed with changing geometries to find a certain dimension which reflects a high spring constant, and at the same time, a high maximum range of stress.

Thirdly, the cantilever shape must be redesigned slightly to incorporate structures with thinner beams. In the previous design, the cantilever consists of three 15 μm beams in parallel. This is found to be relatively large, and causes the release time of the silicon etch to be extended. The consequences of long release times are damage to the top layer of the device, as well as the possibility of cracking in the structural layer due to repeated exposure to high temperatures. Cracking in the piezoresistor region causes the silicon etch to remove the strain sensor.

However, it is also imperative that the mass of the device is high, thus raising the Q of the device, as described:

$$Q = \frac{\sqrt{mk}}{D} \quad (3.17)$$

where m is the mass, k is the spring constant, and D is the damping factor. Raising the Q improves the oscillation amplitude while the mechanical beam is resonating. A larger amount of material at the end of the cantilever raises the effective mass of the device. Raising the k constant is already a previous requirement of the KPFBM device. The damping factor heavily depends on the air resistance when the

beam is oscillating. The viscous damping of the air causes the energy held in the device to be dissipated as it drags in the medium. This can be alleviated with holes in the device or operation of the device in vacuum.

Cantilever beams are designed by cascading $8\ \mu\text{m}$ beams together, with $8\ \mu\text{m}$ separation. This is chosen to minimize the etching time by approximately one half. At the same time, large stiff structures with over $10\ \text{N/m}$ can be realized. At the same time, it is necessary to place the central beam that delivers the signal far from the piezoresistors. To match the characteristics of this cantilever, it is important that the signal line be placed on the axis of rotation. Allowing this central beam to rotate along this axis will preserve the ability for the piezoresistors to exhibit opposite stresses upon deformation, as well as retaining the points of highest stress on the beam. Placing the signal beam before or after all of the piezoresistors will cause the signal beam to exhibit the highest stress since it is the point furthest from the axis of rotation connecting the cantilever and the base.

As such, Figure 42 shows the next iteration of design. In this case, the signal line does not come close to the piezoresistor. The simulated stiffness is roughly $10\ \text{N/m}$, and the stresses on the piezoresistors are near that of the previous design.

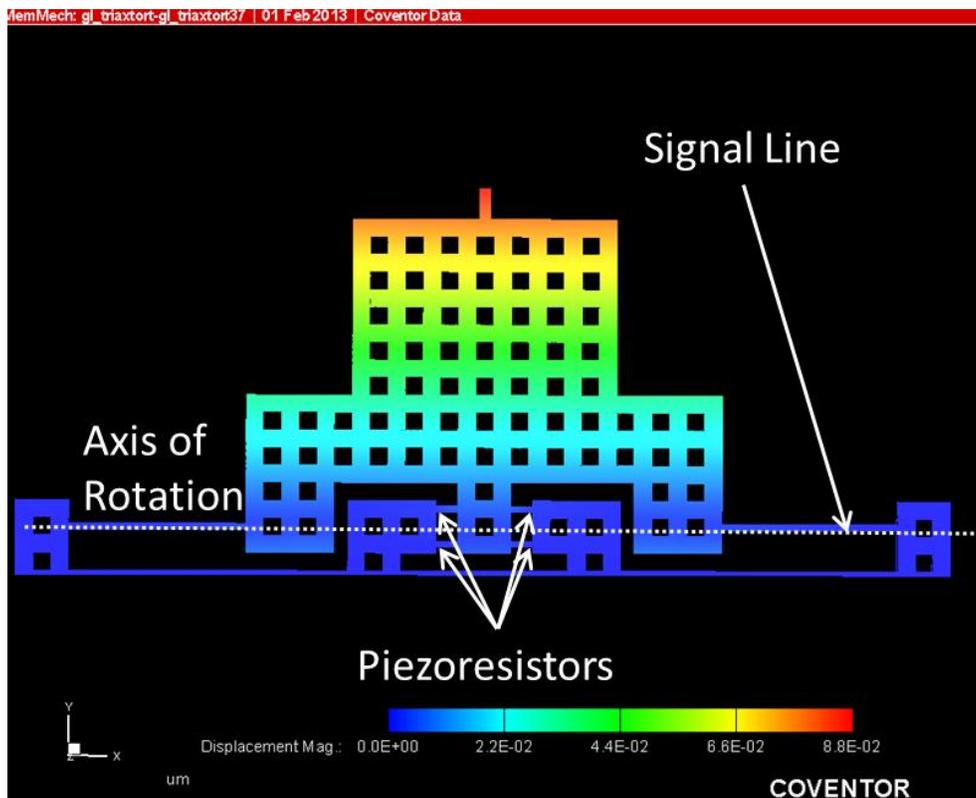


Figure 42: Proposed fourth iteration of KPFM design

Next, the geometry of the device must be optimized. Figure 43 shows the parameters that can be changed to affect the overall outcome of stiffness and stresses associated. Parameter d represents the distance between the axis of rotation and the tip of the device. Parameter s represents the separation between the piezoresistors. Parameter x is the length of the signal line. Parameter y represents the length of the metal covering the piezoresistor. The width of the metal area over the piezoresistor is determined to be $3\ \mu\text{m}$. This generates the highest stress while being conservative with the design rules – the $1\ \mu\text{m}$ wide piezoresistor is at least $1\ \mu\text{m}$ away from all edges of the masking metal. These dimensions are chosen for optimization as the rate of change in the lengths is much more sensitive than the widths, as seen in equation (3.9). Small changes in length can quickly impact the stiffness and sensitivity.

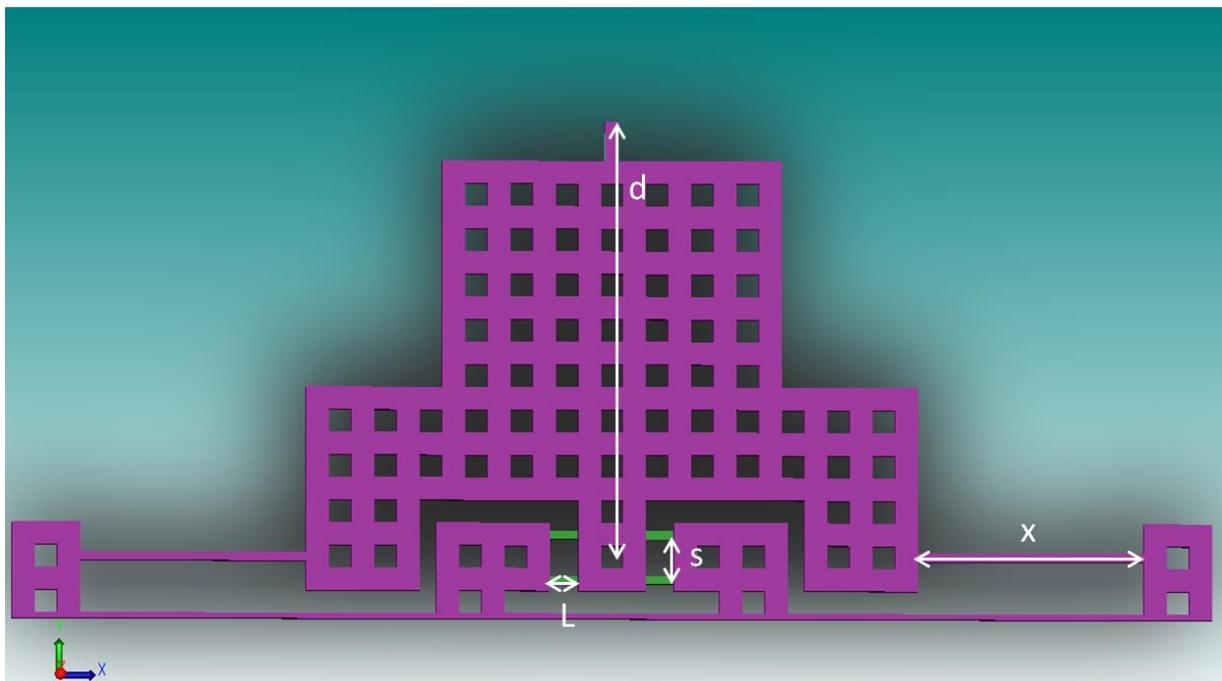


Figure 43: Dimensions to change for optimization

Simulations are performed varying these parameters. Figure 44 shows the effects of changing L with respect to spring constant and maximum stress. At a certain point between 10 and $15\ \mu\text{m}$, we see a maximum point. There are probably combating variables in terms of stress. A longer beam produces less stiffness, which in turn, raises the maximum stress, but the long length of the beam causes the stress to be dissipated throughout the beam. On the other hand, a shorter beam will increase the stress, lowering the amount of deflection, and hence, the maximum observable stress. Since optimization, it is important to choose the value with highest stress values, which is taken at $12\ \mu\text{m}$.

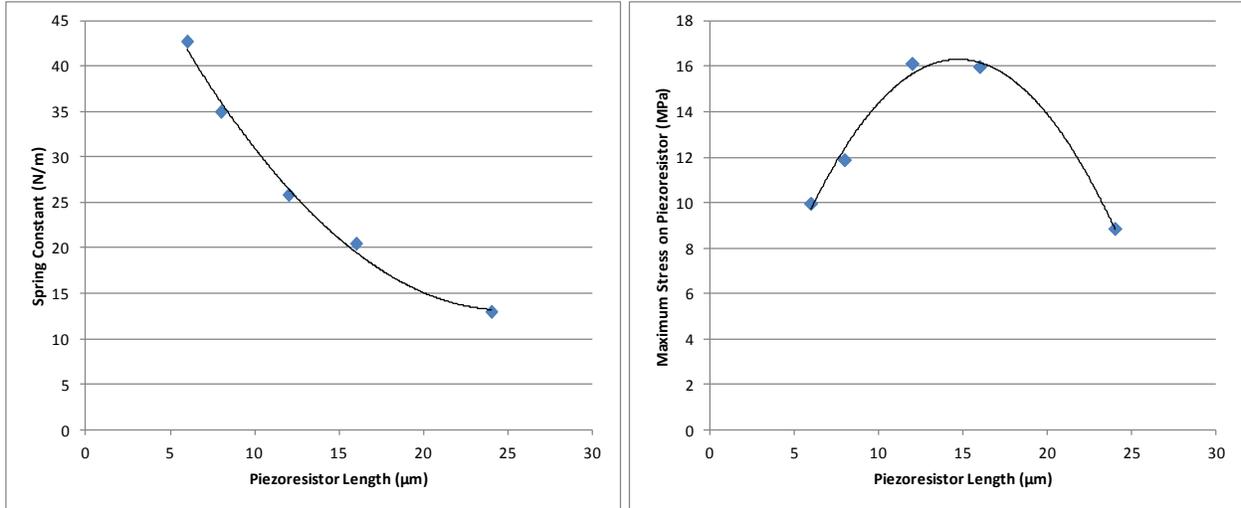


Figure 44: Effects of piezoresistor length with (Left) spring constant and (Right) stress

Figure 45 shows the effects of parameter s , or the piezoresistor separation. In this case, a larger separation increases the spring constant, but lowers the stress of the beam quickly. Increasing the separation reduces the effective length of the cantilever beam as well as increases the maximum stress. This parameter does not change the overall efficacy of the beam by a large amount.

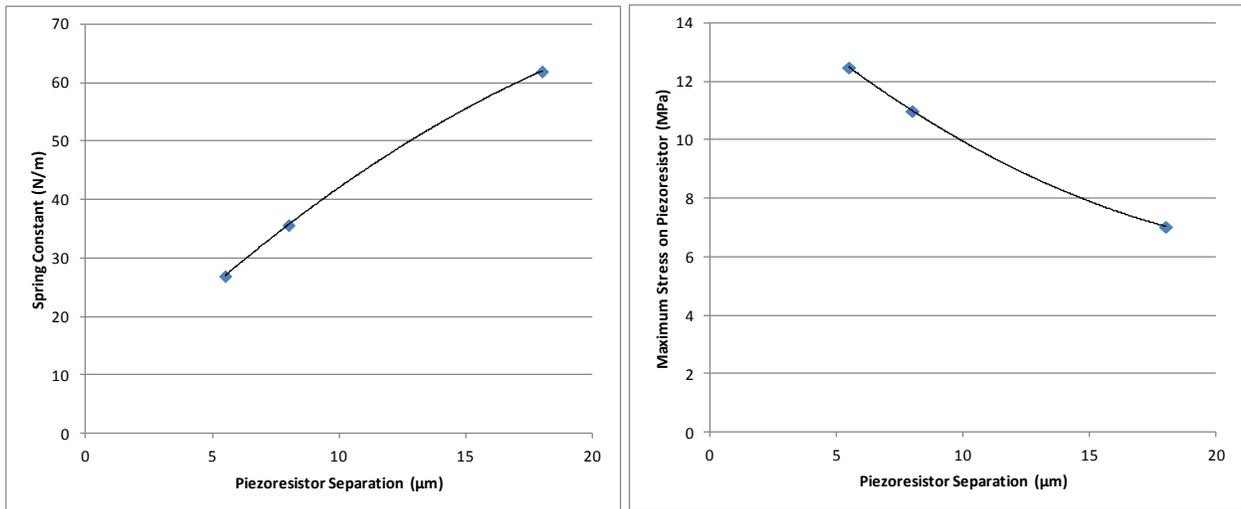


Figure 45: Effects of piezoresistor separation with (Left) spring constant and (Right) stress

Figure 46 shows the effects of parameter x , or the signal beam length. One can see that the beam length is not significant in terms of changing the maximum stress on the piezoresistor, while longer length causes a drop in the spring constant. The beam is kept short to reduce the unnecessary losses.

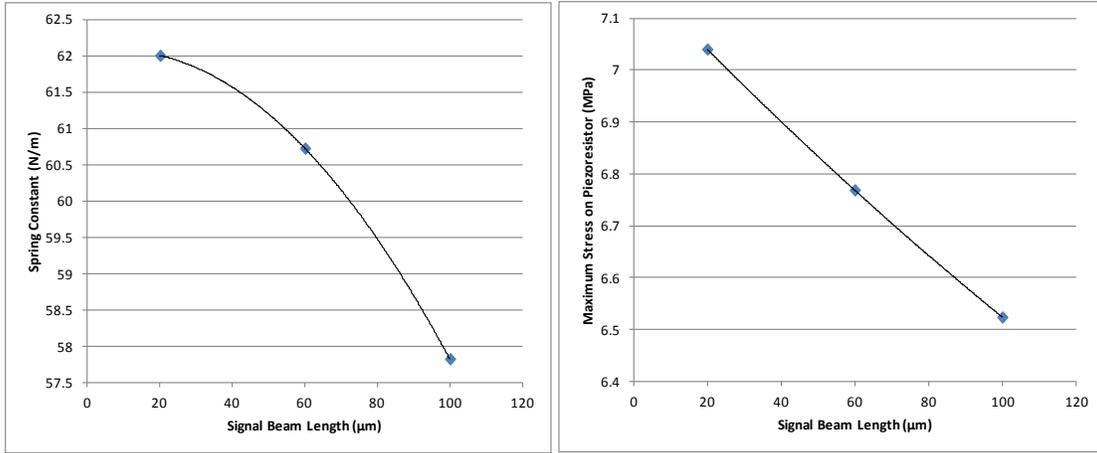


Figure 46: Effects of signal beam length with (Left) spring constant and (Right) stress

Figure shows the effects of changing parameter d , or the cantilever beam length. It is important to note that a longer beam is necessary for the logistics of the device, described later in Chapter 5. The stress placed on the piezoresistors is marginally sensitive to the length of the beam, but the spring constant vastly drops off steeply. It is important to keep in mind the length for the logistics, without trading too much of the spring constant away.

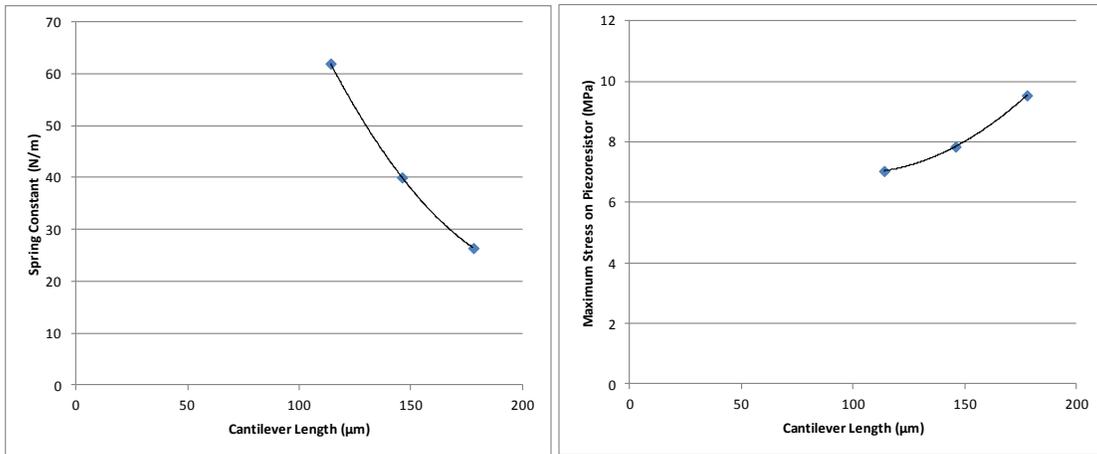


Figure 47: Effects of cantilever beam length with (Left) spring constant and (Right) stress

The final dimensions chosen from these set of simulations are shown in Table 2. These optimal values are found through constant parametric analysis for a spring constant of approximately 10 N/m with the highest possible maximum stress differential.

Table 2: Dimensions of Final Device Design

d (μm)	s (μm)	L (μm)	x (μm)	Spring Constant (N/m)	Maximum Stress (MPa)
186	12	10	20	13.1766	20.21183

A conservative spring constant of 13.176 N/m is chosen. After the application of an XYZ stage, the spring constant will probably fall, this is used as a buffer to make sure that the cantilever will not stick to the sample during operation. In this case, a maximum stress range of 20.211 MPa is observed, which is larger than the previous design.

3.6. Actuator Simulation

A secondary requirement of this work is to build an XYZ stage to support the KPFM device. A bimorph actuator is chosen to operate the XYZ stage. The CMOS process involves the combination of 4 aluminum layers and insulative oxide layers in between. Since the aluminum and the oxide have a thermal expansion constant that is one order of magnitude in difference, the application of heat causes the device to expand disproportionately.

The XY actuator and Z actuator use different bimorph schemes to move. The XY actuator will use a lateral bimorph arm, as large displacements with relatively low power dissipation can be observed. In bimorph actuators, a large set of parallel beams contain offset layers of metal. Upon application of heat, the actuator moves without pivoting around a point. This can be seen in Figure 48. The device is anchored at the left side, and the right side is free to move. The offset layers in the metal allow the devices to move without any rotation. In addition, out of plane movement due to parasitic stresses are cancelled due to a U-arm, which applies the same parasitic movements, but in the opposite direction [7, 65]. Heating the arm may cause unwanted parasitic out of plane Z directional movement, but will be severely negated.

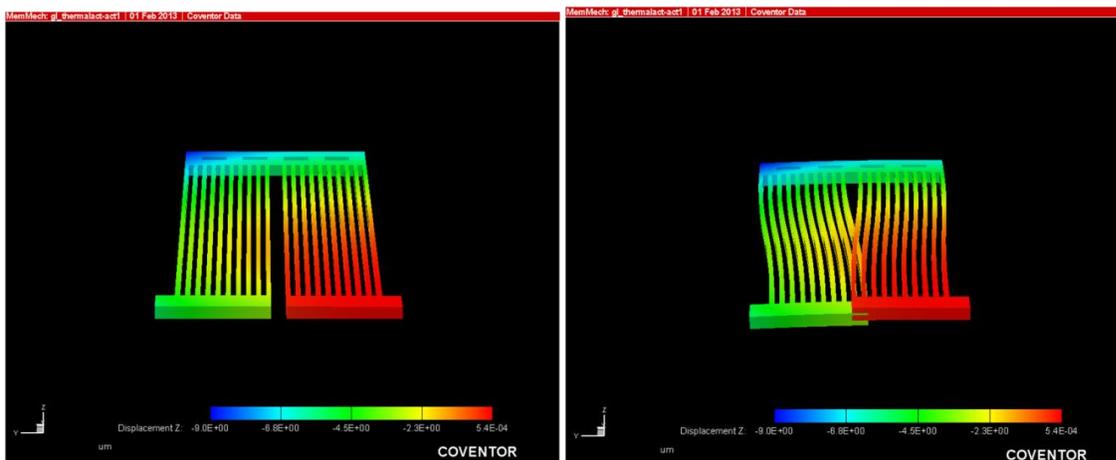


Figure 48: The effects of heating a bimorph arm (Left) without deformations and (Right) with deformations

While heating the actuator to 200 °C, the back portion of the arm moves 9 μm. The U arm negates 4.5 μm of the Z displacement. The resultant beams are also fairly parallel.

The heat is applied through a concept of Joule heating, where the current through a resistor causes a heating due to electrons hitting obstacles in the way, releasing heat. The polysilicon layer has a large resistance in comparison with the aluminum routing layer, and is able to efficiently heat up over small amounts of current. The polyresistor is placed at the turn in the U shaped bimorph actuator to deliver heat equally to the bimorph actuator. Simulations show that 100 °C moves the device approximately 5.5 μm.

The bimorph actuator only move in one direction, hence two lateral actuators must be placed in order for the actuator to move over the entire plane. There are two methods for bimorph actuator placement, and are seen in Figures 49a and 49b.

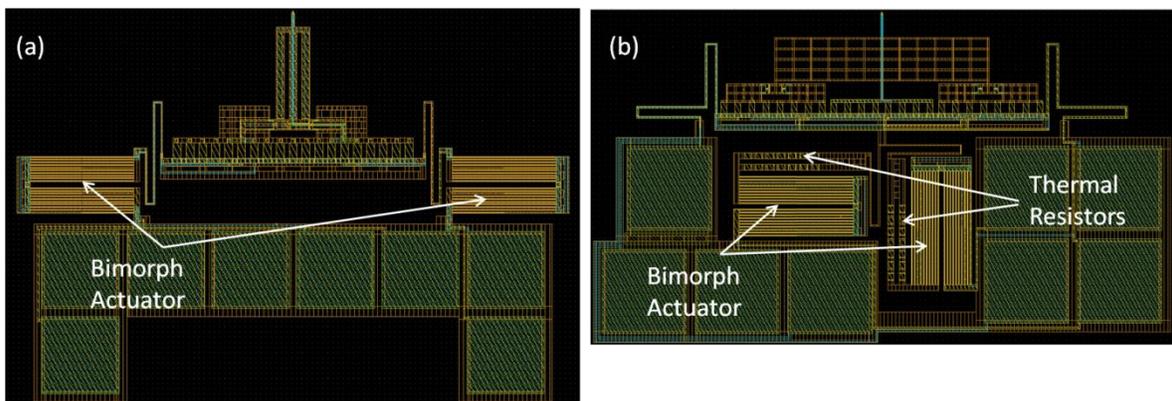


Figure 49: (a) Pivoting XY-stage and (b) Decoupled XY-stage

The design in Figure 49a shows two separate lateral actuators. The left actuator and right actuators can be actuated separately, causing the cantilever to pivot from the left to right. Applying equal voltage to both of the actuators causes the device to move back and forth. Significant challenges come from the coupling of the heat from the lateral actuators to the cantilever. The heat may cause the piezoresistive sensors to expand, causing unwanted signals. Later designs of the XYZ stage present thermal paths, metal lines, that are placed after the actuators that provide a path for the heat to go back to the substrate, limiting the amount of heat that enter the main KPFM device.

The design shown in Figure 49b shows two lateral actuators that are placed orthogonal to each other. One thermal actuator causes X movement, while the other causes Y movement. Again, design considerations are taken into consideration to limit the amount of heat that travels from the device into the KPFM cantilever. Large thermal blocks of insulating oxide and alternating aluminum layers without via holes are used to limit the thermal conduction. Figure 50 shows relative success of the thermal resistors while

displacing the rest of the device. The thermally resistive path reduces the temperature from 500 K (red) generated at the piezoresistor located in the right bimorph to approximately 350 K (light blue) at the device; and 310 K (dark blue) at the other actuator. The heat does not couple largely into the unpowered bimorph.

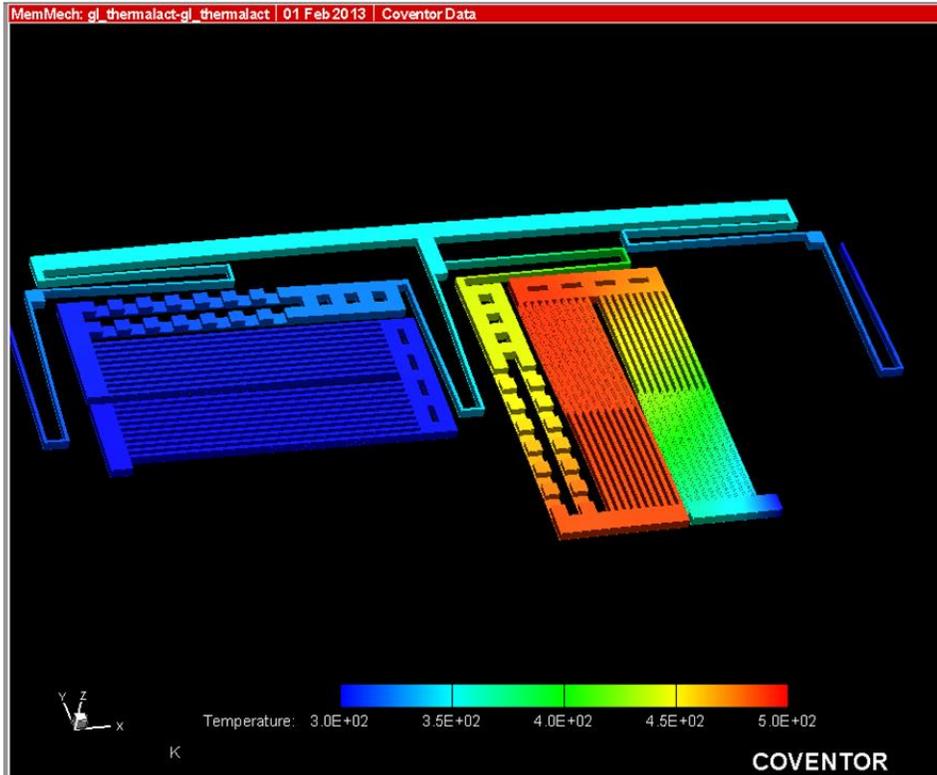


Figure 50: Effects of thermal resistors on XY-stage

The Z actuator must move out of plane – up and down. Special considerations must be made while creating the Z-actuator. Since it is out of plane, only one metal layer is considered. If two metal layers are cascaded on each other, heat will cause expansion of both, but due to the additional thickness, will result in less bending. In fact, to provide the largest amount of Z-directional deflection, the M1 metal should be used. The problem with using only the lowest layer on the beam is the reduced stiffness. The designs require the Z-actuator to be directly behind the cantilever beams. A low overall stiffness will affect the stiffness of the entire structure, allowing possible sticking of the structure to the sample during the scan. Two springs added in series are calculated accordingly:

$$\frac{l}{k_1} + \frac{l}{k_2} = \frac{l}{k_T} \quad (3.18)$$

where k_1 and k_2 are the spring constants of the Z-actuator and the cantilever, and k_T is the effective overall spring constant. Since the equation is heavily weighted towards the lower spring constant, it is important to match the stiffness of the Z-actuator to the device to prevent more loss.

There are a few ways to accomplish this task. The length of the beam must be shortened to prevent lowering the spring constant. Secondly, spring constants are added in parallel, hence, a cascade of beams are used to create the Z-actuator. Springs in series add directly to the stiffness. However, too many parallel beams will take up a large amount of space. Thicker bars are placed into the Z-actuator as well to increase the stiffness. Due to the large amount of highly deflective beams thin beams, the thicker bars will deflect alongside since all beams are in parallel. While this may lower the amount of deflection, Z-actuation is still expected to be in the micron region, and can be tuned with voltage. Figure 51, shows a cantilever and Z-actuator with a final stiffness of 7.69 N/m.

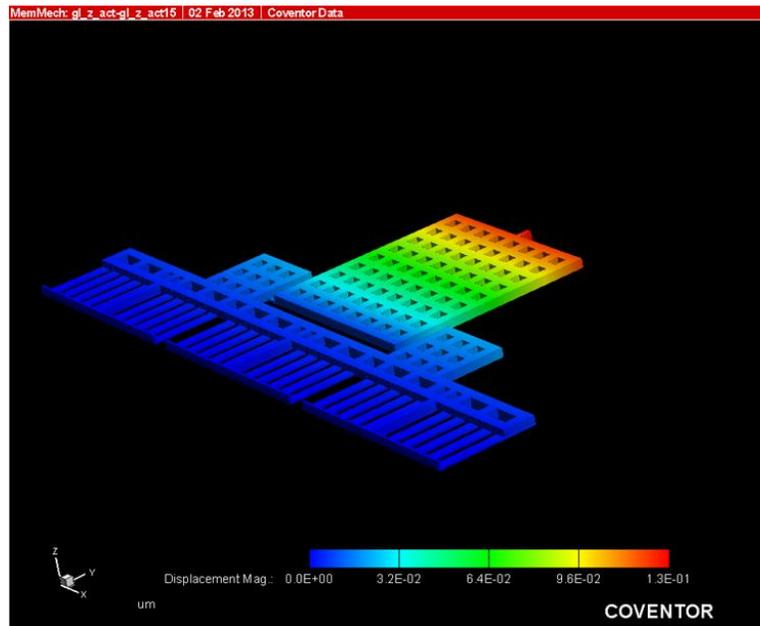


Figure 51: Final cantilever with stiff Z-actuator

3.7. Summary

This chapter discussed the basics of the KPFM and the medium in which it will be fabricated. The CMOS-MEMS process is an important emerging technology for MEMS devices due to its consistency and relatively cheap cost. Through the use of simulation, a cantilever beam resembling the properties of a conventional KPFM can be realized. Properties such as a conductive tip, piezoresistive strain gauges, a spring constant from 1-10 N/m are all necessary to create a working KPFM.

Further considerations are taken when the devices are optimized for maximum sensitivity by altering beam geometry. Problems such as electrostatic coupling between the KPFM signal line and the piezoresistors are discussed, and initiatives are taken to lower the amount of coupling through the use of strategic placing of signal lines.

Finally, considerations and initial designs for an XYZ stage are considered. Many of the problems such as thermal coupling between the thermal actuators during operation are discussed, and concepts such as large thermal resistances are introduced and incorporated into the devices. Basic simulations show that these concepts are effective at decoupling the heat between the actuators. Concepts such as Z-actuator stiffness are considered and solutions are made to incorporate the final cantilever while limiting the decrease in spring constant.

The next section assumes that the cantilevers have been correctly fabricated. Tip sharpening and modification techniques are applied to determine their effectiveness within the system that has been designed.

4. Tip Modification and Sharpening

Tip modification is an important aspect of any SPM tool. In all cases, the SPM tip must be extremely sharp in order to resolve any sort of atomic imaging. In other cases, the tip must be conductive such that the KPFM is operable. While the fabrication processes of conventional tips and cantilevers are quite simple and standardized [34-37], the integration of tips on a released CMOS-MEMS SPM device are a different challenge.

The two main commercially available cantilevers are fabricated using the underetching or mould method. This ensures wafer wide mass production and that fine atomic scale tips are fabricated from a precise atomic plane silicon etching step. While CMOS devices contain silicon, the process does not involve initial silicon etching during the processing steps. Hence, a tip cannot be created from the substrate material. Instead, the tip may only be fabricated from the aluminum layer of the process.

Two main approaches can be used to create the tip: creating a triangular tip that extends from the cantilever, as seen in Figure 52, or placing a minimum feature size square of the top metal layer over the cantilever, as seen in Figure 53. Both methods have been fabricated and show approximately a radius of curvature of approximately 500 nm.



Figure 52: Lateral 4-layer tip



Figure 53: Orthogonal tip stack

The post-processing of the CMOS-MEMS device results in a top device layer consisting of aluminum. This is the layer that is in contact with the sample. This presents a wide range of problems. Firstly, the aluminum layer readily oxidizes when exposed to the atmosphere. This insulative layer prevents contact between the aluminum and the sample, which is important for future work in passing current from the probe into a surface. Physically piercing through the oxide layer involves contact forces of up to the range of approximately 30-100 mN, which is unattainable via device actuation [69]. Methods such as additional RIE etching to remove the oxide layer is detrimental, as it may cause device damage, and the oxide layer will shortly reform after exposure to the atmosphere. The second problem involves post-processing deposition of polymers onto the device. The oxide etch in the RIE, which consists of a reaction between CHF_3 and SiO_2 , causes Teflon based polymers to redeposit within the chamber. This insulative polymer also prevents contact between the tip and the sample. A quick ashing process may help to remove the polymers.

The problems with CMOS-MEMS device tips are addressed in this section. Methods such as gallium-aluminum alloyed tips are investigated to increase tip sharpness. A new method of electroless plating MEMS devices with other materials is also investigated.

4.1. Gallium Tips

Gallium is known to alloy with other metals that it contacts, creating an extremely brittle material. In contact, the gallium penetrates through the aluminum metal lattice, and continues to form structures until the limited reaction depletes of the precursor materials [70]. By dipping the aluminum surface of the CMOS-MEMS device into a ball of gallium, a reaction will occur at the interface. The gallium penetrates through the grain boundaries of the aluminum, altering the chemical nature of the metal. A stress is applied during this process, causing the grain boundaries to slip, creating a new geometry with the alloyed materials.

The experiment will begin by depositing small droplets of gallium onto a substrate. A MEMS device attached to a XYZ-micromanipulator will be lowered into the gallium droplet. The MEMS device will remain in the gallium droplet for 5 minutes before being pulled out.

4.1.1. Experimental

A glass substrate is cleaned with acetone and isopropyl alcohol. Gallium is spread onto the glass substrate. Gallium does not wet the surface of the glass well, as tiny gallium droplets are formed on the glass. Epoxy is used to bond a released CMOS-MEMS SPM. The tip is observed in a scanning electron microscope, as seen in Figure 54. The flat edge of the cantilever is 5 μm . This is mounted onto a long cantilever with micromanipulator control. Observed from underneath a microscope, the device is lowered into the gallium droplet until a contact is created between the tip and the gallium ball. This can take a multitude of tries, as the gallium does not immediately wet the oxide surface.

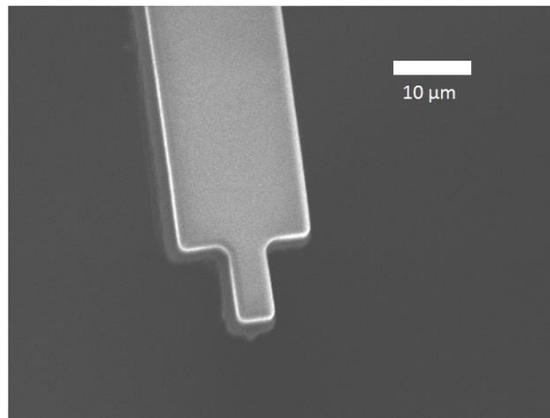


Figure 54: Pre-sharpened cantilever

Once a small amount of gallium sticks onto the surface, the CMOS-MEMS device is quickly removed from the droplet of gallium to form a gallium/aluminum tip. The rate of tip removal is difficult to track, as the micromanipulator is controlled by physically turning knobs by hand. While literature has controlled methods of tip removal [49], this kind of precision is unattainable with the tools used in this experiment. The integrated MEMS device contains a XYZ stage meant for cantilever displacement to drive upwards of 10 μm in displacement, however, gallium that has wet the surface of the aluminum creates a suction force that is not possible to overcome except through the use of the micromanipulator.

This procedure is performed on 5 separate CMOS-MEMS devices. The resultant tip formation can be seen in Figures 55a-e. The radius of curvature ranges from approximately 100 nm to 1 μm .

After imaging, the devices are electrically connected to the PCB with wirebonds. Within the MEMS device, there is an electrical path connecting the tip to one of the probing pads. The wirebond to the PCB allows a bias to be applied to the tip, or a resistance to be measured. A commercially purchased DC tungsten probe is lowered onto the gallium tips with the use of a micromanipulator. The resistance is

measured between the probe and the cantilever tips. No observable resistance is noted in any of the cantilevers.

The tungsten probes are removed from the cantilever tips. It is noticed that the gallium tips no longer exist, or are deformed beyond initial recognition. Further investigation shows that the gallium has migrated to the tungsten probe instead.

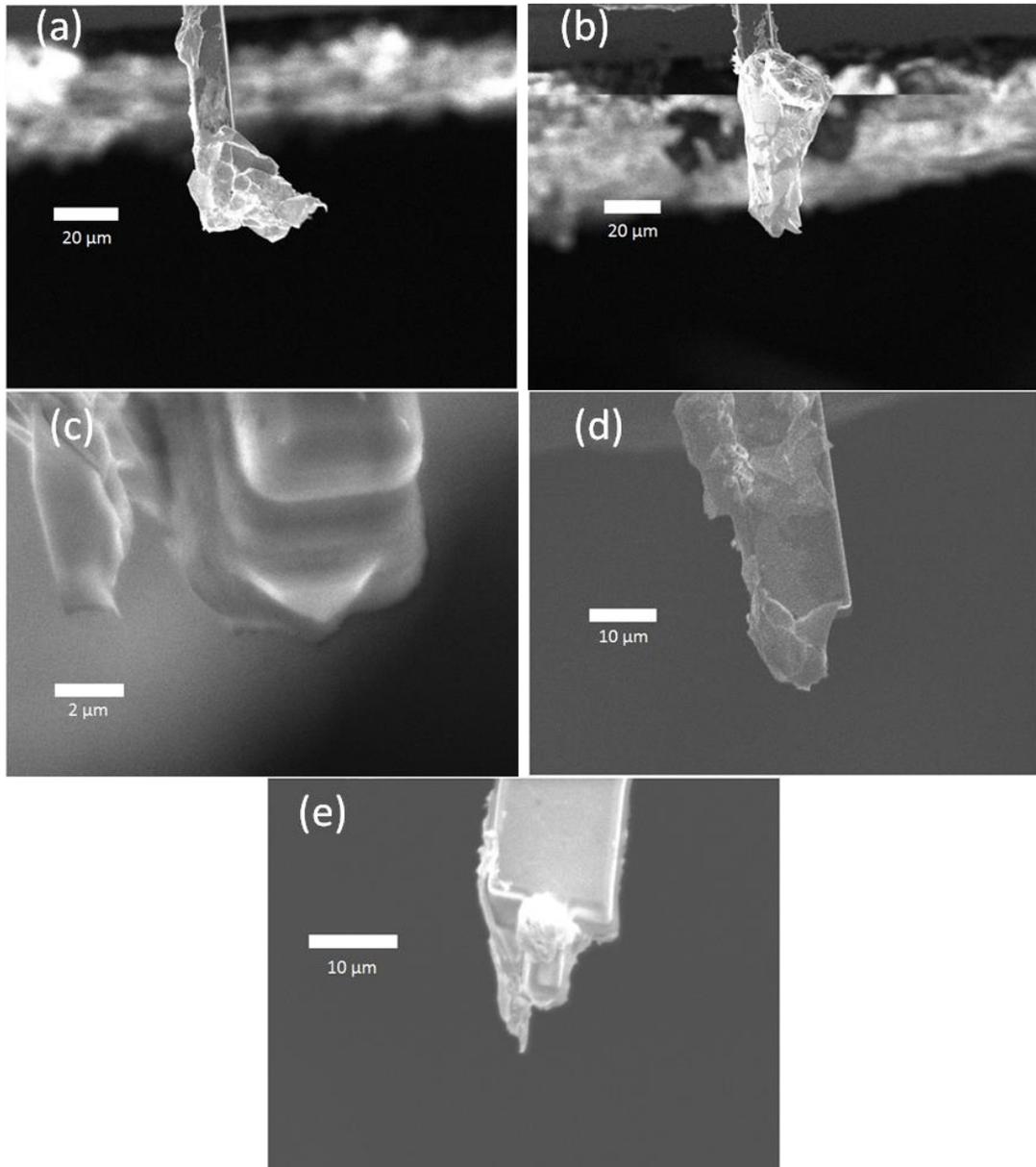


Figure 55: Tip formation post gallium dip of 5 separate devices

4.1.2. Analysis

While it has been shown that gallium can possibly create sharp tips, the lack of control makes this process undesirable. As observed from the Figures 55a-e, the wetting of the surface is extremely hard to control. Blobs of gallium wet the surface at different volumes. In cases such as Figure 55a, the tip is created far from the actual tip area. Figure 54c shows a sharp gallium tip that runs parallel, but not past the flat tip. This means that the sharp portion cannot be utilized. In cases such as Figure 54e, the gallium tip does not extend from the aluminum top layer, but is connected to the oxide layer underneath the metal layer. Without more control, this method fails to provide sharp tips. A coarse approach mechanism has been designed, using piezoelectric elements for movement, but has not been implemented for gallium tip creation.

The lack of electrical contact between the tungsten probe and the MEMS device shows that there is a high possibility of an insulative layer that exists between the aluminum and gallium. While the aluminum and the gallium are supposed to form a brittle alloy, the tungsten probe that destroys the tip also contains a smear of gallium. If a brittle alloy was formed, the tip would break off as a solid. This shows that the tip is made of a large portion of gallium with no reflows of the aluminum lattice. This suggests two possible outcomes. The first possible conclusion is that a longer time is needed in order for the limited gallium interfacing with the aluminum to create the alloy.

As such, the gallium tips are allowed a day of stagnation for alloying and solidification. This never occurs. A probing experiment one day later shows similar results. A large amount of gallium on the surface of the cantilever prevents a full reaction between the gallium and the aluminum lattice. The gallium is never properly mixed with the aluminum. Limiting the amount of gallium on the cantilever may allow more migration of the material to the tip, and depleting the amount of pure liquid gallium.

The second and more probable conclusion is that the gallium never breaks through the oxide layer of the aluminum in the first place. The lack of conductive contact shows that an insulative layer exists. The lack of brittle material at the tip also shows that the aluminum never actually alloys with the gallium. In order to create a good tip, this insulative layer must be removed. It may be formed from the oxide layer that naturally grows on the aluminum, or from the residual polymer from the fabrication process.

4.1.3. Future Work

The lack of controllable, sharp and hard tips shows that this process may not be optimal as it stands. Additional steps such as a well controlled piezoelectric stage must be utilized. This will control the amount of gallium that gets onto the tip through submersion. The oxide or polymer should be removed in a plasma before the gallium deposition or else the reaction may not occur. Gallium droplets should be limited in size to reduce the amount of gallium past the interface of the tip. Limiting this amount of gallium reduces the diffusion time allowed for the reaction between the two materials. This allows the formation of a brittle tip without residual liquid gallium.

4.2. Electroless Plating of CMOS-MEMS

Electroless plating is a method to deposit a material onto a surface without the introduction of an applied voltage. The first step often involves cleaning the surface of a CMOS-MEMS device. Without any processing, the oxide that forms over the aluminum layer fully insulates the surface, as seen in Figure 56a. This is followed by a chemical dip, which is used to remove the native oxide layer of the aluminum, thereby, readying the surface for a reaction; this is seen in Figure 56b. The last step involves the plating of the new material. A variety of materials can be placed onto the surface to provide new properties for the devices. Figure 56c shows a non-corroding surface, such as palladium that allows for an electrical contact. Figure 56d shows a magnetic coating that can induce movement of the device under a magnetic field. Figure 56e shows the application of a gold layer, which can be used to form a self-assembled monolayer surface used in sensing applications.

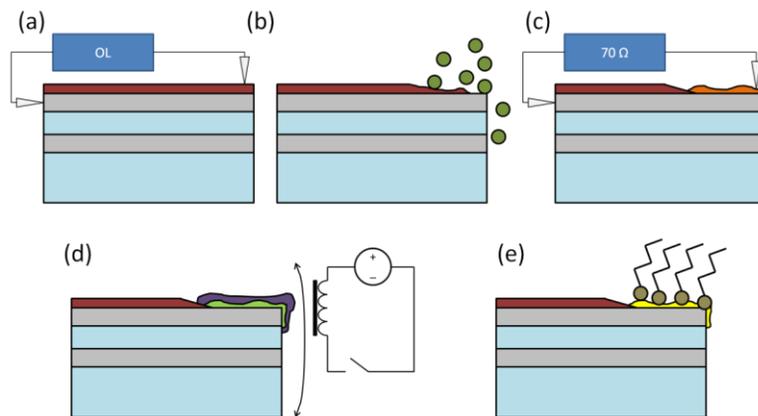


Figure 56: Electroless deposition of materials onto a device surface

Two commonly used electroless deposition processes involve palladium plating [71] and nickel plating [72]. In the case of both processes, the final product, the finished film will carry characteristics of the overlying material, namely, a hard, conductive, corrosion-proof surface. This is especially useful in CMOS-MEMS SPM devices, as the corrosion prevents oxidation reactions on the surface, improving the efficacy of using the SPM devices in the future for direct probing, voltage biasing and current carrying applications. An addition layer of hardness on the material prevents a sharp tip from dulling. While this is often performed on a macroscopic level, electroless plating has been shown to work on CMOS devices [71, 72]. This section presents a method to selectively plate a material onto a released CMOS-MEMS device.

The final solution for developing a working mechanism for electroless plating is as follows: a MEMS device with dice lines is lowered into a wire loop of electroless plating solution. The wire loop is used to limit the amount of liquid that can destructively interfere with the device. The device is allowed to plate for 5 minutes before removal.

4.2.1. Implementation Considerations

In the case of MEMS devices, where the four layers of aluminum form not only the structural beam, but the electrical routing, a pre-release electroless plating process will cause shorting between the layers. It may also affect the silicon etching process during the release, causing possible damage to the piezoresistors and the structural integrity of the device. There are various unknowns while etching a new material in the RIE without first optimizing the process. There is a possibility that the materials will also be etched. Hence, conducting the electroless plating process after the beam has been released will reduce the amount of possible damage to the device. It is also important to have the ability to selectively plate certain areas.

Performing electroless plating on the MEMS device after the release also presents new problems, as later described in this section. Once liquids enter the area beneath the device, it becomes permanently damaged. The capillary forces between the MEMS device and the substrate exceed the restoring spring force of the cantilever beam. This results in a non-functioning MEMS device. It is possible to place the liquid covered device into a supercritical CO₂ chamber, but the extraneous electroless plating solution must be removed from the chip first to prevent contamination of the chamber. This also fails to address the selective plating process. A nanoneedle with a nanopositioner can selectively place a specific volume onto a cantilever. However, upon drying of the plating solution, a large uncontrolled chunk of material

will be left behind due to extraneous nucleation. In addition, an extremely specialized set of tools are needed.

For this section, plating of the cantilever with palladium and nickel is presented. Palladium plating is important as it is a material that does not readily oxidize. While gold may be a much more common candidate, certain characteristics important to SPM techniques hold palladium in higher regard. Palladium is much harder than gold, such that if the tip accidentally crashes into the surface, it will not become chipped, nor will material be removed from the tip edge, keeping a hard conductive layer. Nickel is used due to the fact that it is a magnetic material, and can be used in other applications such as Magnetic Force Microscopy (MFM). In addition, the solution is a proprietary blend, and has been shown to be constant in its efficacy.

4.2.2. Results

The palladium electroless solution is first presented. Using a similar plating solution found in [71], a palladium plating solution is created. This one dip solution contains an acid used to dissolve the aluminum oxide, activating the bare aluminum surface underneath to the electroless plating reaction. The combination of all the other reactants causes the palladium to nucleate onto the surface of the MEMS device, and continue to grow the film until it is displaced from the solution. A CMOS-MEMS chip is attached to a micromanipulator arm as seen in Figure 57. Viewing from underneath a microscope, the chip is lowered into the solution until the tip of the cantilever is submerged into the liquid.

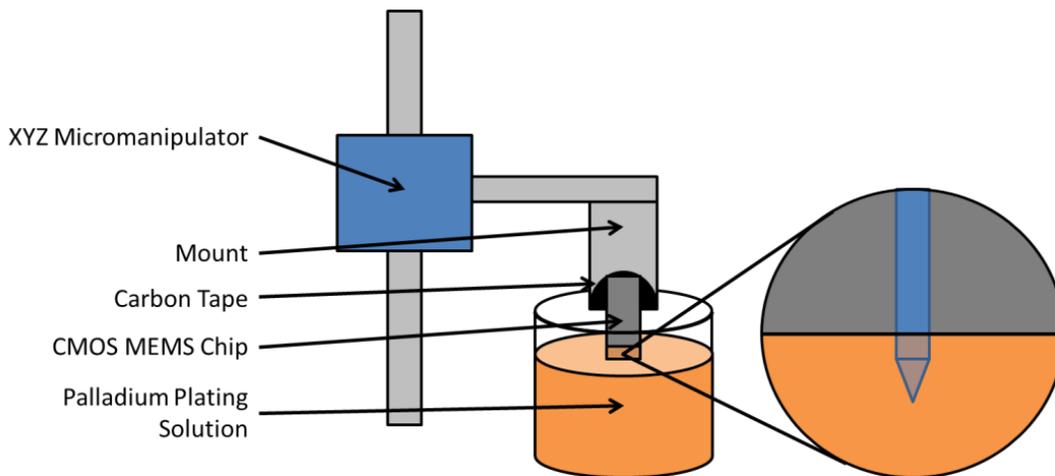


Figure 57: Set up of electroless plating system

When the chip is placed near the solution, capillary forces cause the liquid to quickly ride up the surface of the CMOS-MEMS chip. A lot of focus and attention is needed to adjust the micromanipulator up and down to keep the tip submerged. In fact it is generally too difficult to control this action, as the bubbles rising from the reaction of the chemicals, influences the level of the solution on the cantilever tip. The chip is submerged for 1 minute.

Once raised from the solution, it is observed that the cantilever tip is coated with a different material. The sheen of the material is orange/red instead of the conventional shiny white aluminum, presumably palladium. However, plating occurs at a point further than the intended plating area. The moving meniscus on the chip from the capillary forces occasionally covered entire devices. In addition, the violent bubble popping of the palladium plating solution caused splashing of the solution to the surrounding area. It can be seen that unintentional dots of palladium plating occurs over the non-plated portions of the chip.

This process also allowed liquid to flow between the cantilever and the substrate, causing the devices to be stuck down. The chip is placed into a 100 °C oven and allowed to dry. Upon observation, the dried cantilever was still stuck down to the substrate surface. The chip was not placed into a supercritical dryer due to the risk of contamination.

Two challenges can be identified; stopping the bubbling, and preventing the liquid from wicking past the intended plating portion. In order to stop the bubbling, the plating solution is further diluted with water. At a ratio of 1:1 water to plating solution, the bubble problem still occurs. At a 3:1 water to plating solution, the resultant solution becomes too diluted to form any significant plating within a 5 minute dip. A final ratio of 2:1 water to plating solution is used. The trade off of longer plating time is balanced with the detrimental bubble popping. While bubbles still exist, the pops are not violent, and no observed dots of plating appear on the chip thereafter.

To address the wicking, a chip splitting solution is utilized. In this process, the CMOS-MEMS device is diced half way before the post-processing etches are applied, as seen in Figure 58. Upon release, the cantilever is no longer stuck down to the substrate. At this point, dental picks are used to split the chips by placing pressure on the diced fissure. Since the device was suspended in air, the cantilever is not damaged, but hanging over the side of the substrate.

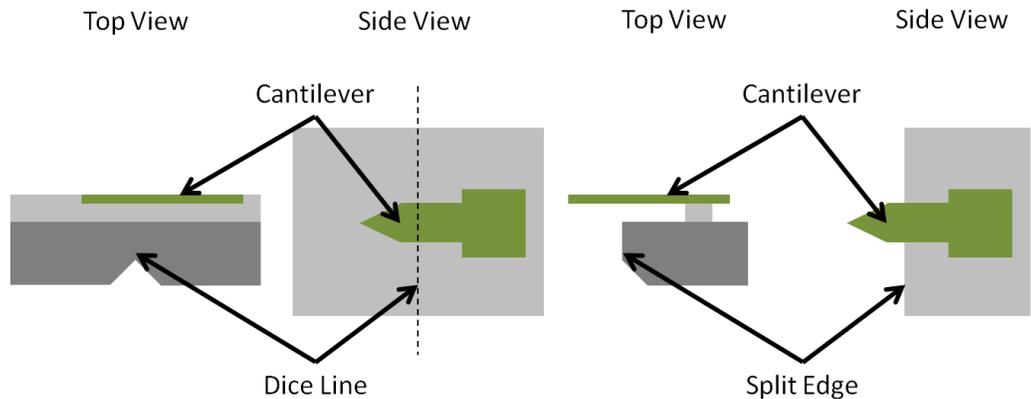


Figure 58: Snapping chip to have overhanging cantilever (Left) unreleased (Right) released and snapped

In this case, since the liquid does not have the large surface area of the 5 mm chip, and instead, a cantilever with a width of 15 μm , the amount of wicking should be minimized. In addition, since the edge of the cantilever is hanging over the substrate, a larger leeway is given to liquid being sucked up underneath the cantilever, thereby eliminating the stiction problem.

The same experimental set up is used to plate the devices. The bubbling is minimized, as stated before, but the amount of wicking is enough to cause the liquid to completely coat the edge of the substrate. Again, the stiction remains a problem in the device, and the tip is not controllably plated.

To prevent the wicking of the solution onto the device, the amount of plating solution was minimized. A 20-gauge syringe needle is purchased and the plating solution is placed the syringe. The syringe is held up by a mount, and a small amount of plating solution is forced out of the syringe, allowing only a small droplet at the tip of the syringe to interact with the device. The device is lowered into the droplet. Similar problems occur in this method as with the previously mentioned methods. In addition, the liquid often flows back down the needle of the syringe, causing problems for the plating process.

Finally, a method adopted by STM tip fabrication is used [73]. A wire loop is created from a tin wire. Placing the wire in the solution induces no reaction – no bubbles are formed. After a day of submersion in the plating solution, to reduce any chance that an unobservable reaction is occurring, the wire is dipped into a fresh solution of the palladium plating solution. This creates an extremely thin film of the plating solution. This film severely limits the amount of liquid that can wick up onto the device. The thickness of the film also allows a lifetime of at least 10 minutes, which allows for the quick 5 minute process.

During observation of the device underneath a microscope, the MEMS device is lowered into the wire loop with the thin film. The experimental set up is seen in Figure 59a. Under the microscope, the MEMS device can be seen and be manipulated towards the film, as seen in Figure 59b. Under the microscope

light, the film clearly reflects the surface of the MEMS device, and the proximity of the device can be estimated by the points of the two tips; one from the MEMS device, and the other from the reflection. Upon contact, the film deforms slightly, and the film does not suck in any more than 5 μm . The MEMS device can be pushed further into the film using the micromanipulators if it is necessary. The film is submerged in the film for 5 minutes.

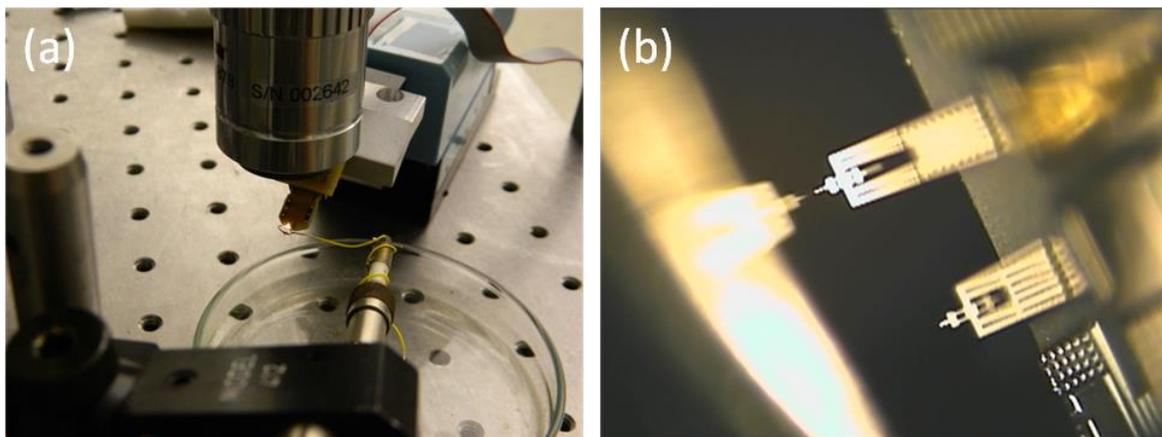


Figure 59: Electroless plating set up with wire loop

The devices are retracted after the plating process. It is observed that an orange material has formed on the tip of the device through investigations in an optical microscope. Further investigation is performed under the SEM. Figure 60a and Figure 60b shows the resultant samples before and after plating, respectively, under the SEM. Figure 60c shows the effects of film popping if the MEMS device is still located within the wire loop. Occasionally, when the film pops with the device within the loop, a residue forms and dries into a film, as seen in Figure 60c.

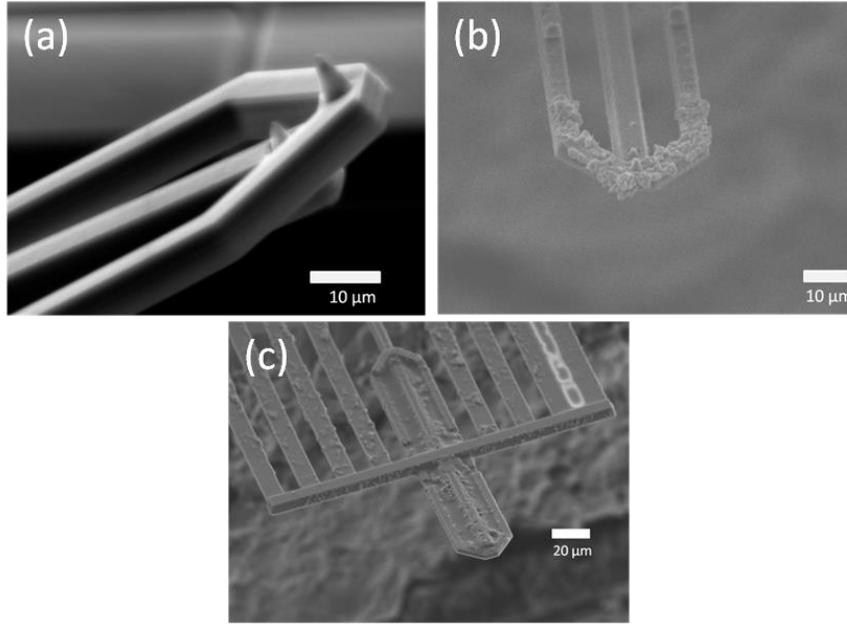


Figure 60: Effects of electroless plating using a wire loop on CMOS-MEMS devices

The palladium films forming on the MEMS device are tested for their conductivity and their lifetime. Firstly, an unplated CMOS-MEMS device with a spring constant of approximately 1 N/m is wirebonded to a PCB. The very tip of the cantilever is probed by an extremely sharp DC tungsten probe, as seen in Figure 61.

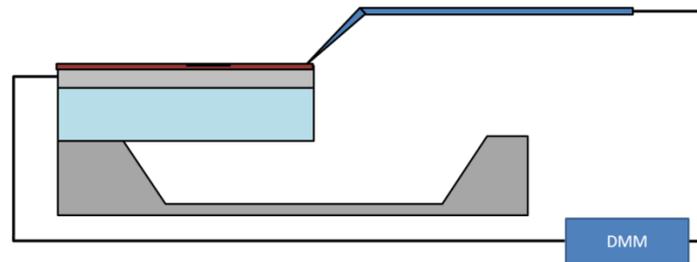


Figure 61: Testing conductivity of the surface of a CMOS-MEMS device

The resistance is measured. At first, no resistance is observed; however repeated scratching of the aluminum breaks through the oxide layer, showing a resistance of approximately 2-4 Ω . On the other hand, if a dull probe is used to probe the cantilever surface, no resistance can be measured on any device. This shows that a sharp DC probe tip is able to break through the aluminum oxide layer. However, in an application where the cantilever probe must be probed against a flat surface, no electrical contact can be made since the low spring constant cantilever is not stiff enough to generate enough forces to break through the oxide layer.

On the other hand, three of the six plated devices show a resistance between the tip and a dull probe. The resistance is measured every day for three days to determine the change in resistance. This is shown in Figure 62.

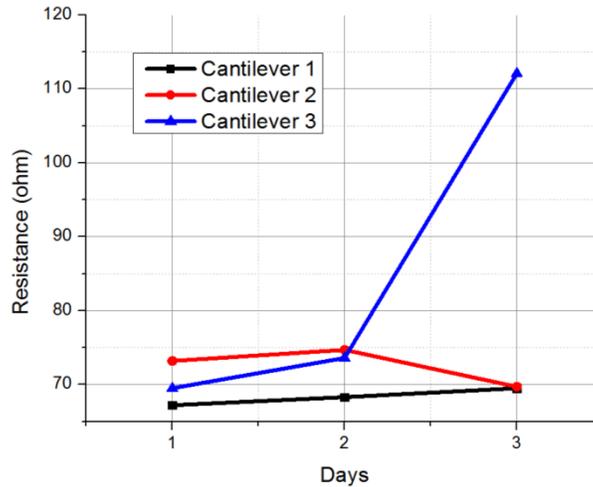


Figure 62: Resistance measurements of plated device surfaces

The resistance changes marginally throughout the three days of testing, showing that oxidation does not inhibit the conductivity of the surface. A sharp DC probe is used to measure the three devices that did not provide a contact resistance. No resistances are observed.

The palladium plated devices, while showing a contact resistance of approximately 71 Ω , is much higher than the 2-4 Ω shown on regular aluminum cantilevers. However, the palladium plated devices will be able to provide an electrical contact without a large applied force, which is impossible for an unplated MEMS cantilever.

The higher resistance can be attributed to a variety of reasons. Figure 60b shows the palladium coated device. It is extremely rough compared to the unplated portions. It is likely that the nucleation sites on the aluminum are from point areas where the activation solution penetrates through the oxide layer. Since the solution is diluted to reduce bubbling, the dissolution of the oxide layer also reduces. The palladium then grows outward from the one point, creating small particulates, blocking any of the underlying oxide from being etched away from the acid due to steric hindrance. The low contact area between the palladium and aluminum raise the overall contact resistance between the palladium and aluminum. However, this interface does not oxidize, and the palladium surface does not readily oxidize in three days. The palladium also forms large particulates. The boundaries between these particulates may also cause an increase in contact resistance. Further lifetime experiments are necessary to gauge the corrosion resistance of the palladium film.

The yield of this process in fabricating conductive cantilevers is 50%. A variety of reasons can attribute to this low yield. CMOS-MEMS devices are subject to a post-processing method which causes polymer to form from the reaction of CHF_3 and silicon dioxide. This Teflon based polymer coats the entire device, and while it does preserve the device during the silicon etch, the polymer remains on the device after the release process. If the polymer is not completely removed, the plating process may not make an electrical contact with the aluminum as the plating may occur on the polymer instead. It is suggested that a mixture of EKC 653 is used to eliminate the polymer on the surface of the device using the same wire loop process before beginning the electroless plating process.

If the contact area between the nucleation site and the aluminum is extremely tiny and near the surface, oxygen migration may occur. A reaction with the migrating oxygen and the aluminum causes oxide formation. This process produces an insulative layer between the palladium and the aluminum, stopping electrical contact through the junction. At this time, further investigation is needed to determine the optimal cleaning process and plating process.

Using the same procedure, nickel is also plated onto devices as well. A proprietary electroless nickel is used for the process. This involves first plating a layer of zincate onto the device, followed by the layer of nickel. The zincate is used to displace the aluminum oxide layer, and plate it with zincate, which oxidizes at a slower rate, and allows a reaction with the second plating solution. Again, the solutions are further diluted down at a ratio of 2:1 to prevent the bubbling from destroying the device. The devices are also allowed to dry in a 100 °C oven between the plating steps to prevent cross contamination of the two plating solutions.

In addition, the nickel plating involves heating the solution up to at least 70 °C to induce a reaction. A MEMS device is specifically chosen contains has a Z-stage bimorph beam, which actuate based on the principals of Joule heating. 0.5 V is placed through the 700 Ω polysilicon resistor, creating a >0.5 mA, which is used to heat the device to a temperature over 70 °C. This displaces the beam a few observable microns underneath the microscope. The heat at the surface of the tip approaches this temperature. The heat capacity of the film is not enough to dissipate heat. While the rate of evaporation would increase for the film, it shows no significant decrease in film lifetime.

Figure 63a shows a plain MEMS device before plating, Figure 63b shows the addition of zincate, and finally, Figures 63c and 63d show the nickel plating at two different zooms.

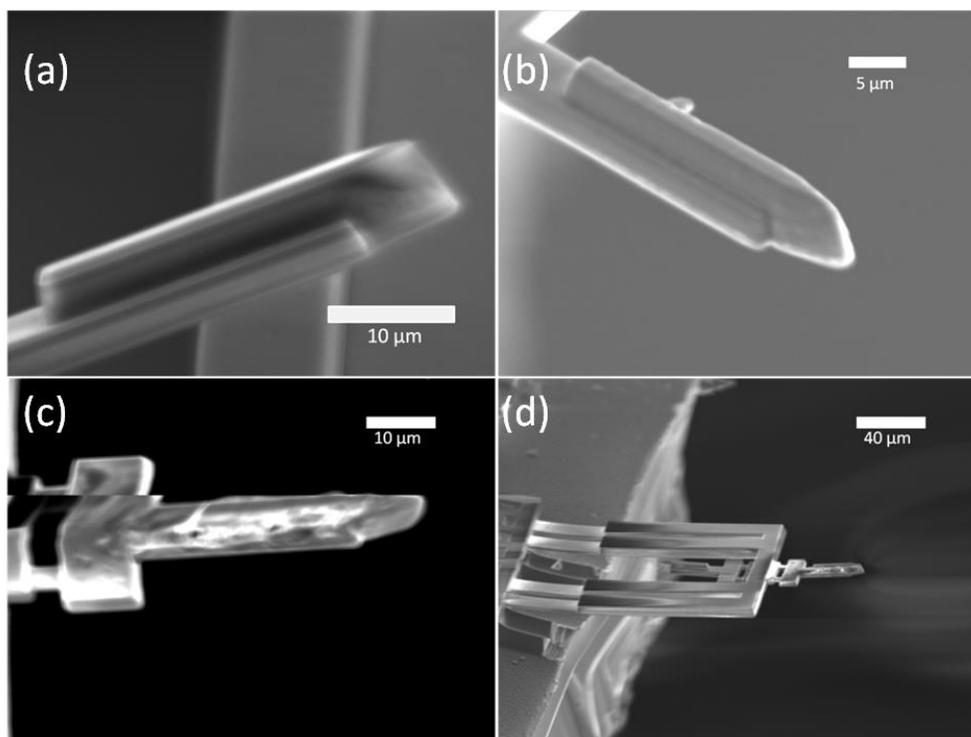


Figure 63: Scanning electron micrograph of CMOS-MEMS device throughout various stages of electroless plating

Firstly, a large difference in tip sharpness can be seen between the unplated device, and the zincate plated device. The very edge begins to dull after the implementation of the zincate. It is highly possible that the zincate begins to dissolve the submerged aluminum layer in order to provide a surface for activation.

The nickel plated MEMS device in Figure 63c is heavily distorted in the picture. This is due to the magnetic field influence during a high resolution, low speed scan in the SEM. A high speed scan at a reduced zoom is shown in Figure 63d. Distortions can be seen around the tip of the device. This implies that the material that has been electrolessly deposited onto the surface of the MEMS device is indeed nickel, as it produces its own magnetic field, interfering with SEM operation [74]. However, it can be noted that the finished product does not contain particulates like the palladium devices. This may be attributed to the fact that this plating process adheres to many materials. The tip is never cleaned, and the consistent smooth surface suggests that the plated zincate may coat the Teflon polymer as well. However, since the geometry of the tip has changed after the introduction of the zincate solution, may suggest that it dissolves the polymer film. Further investigation is needed to clarify the effectiveness of this process, and the conductivity of the tip. To this date, the electrical contact between the tip and a probe has not been measured.

As a next step, unplated devices and nickel plated devices will be subject to a magnetic field, as the piezoresistive sensors will be monitored for deflections, quantitatively validating the nickel surface.

4.3. Summary

Two new topics are introduced for tip modification of CMOS-MEMS SPM devices. The first method shows that gallium can be utilized to create a tip off of an existing cantilever. However, the tip fails to survive any sort of testing other than showing an initially sharp radius of curvature. The lack of stability in the tip and the liquid-like properties insists that a brittle gallium aluminum alloy tip has not been made. Instead, the large amount of gallium on the tip does not migrate into the aluminum lattice of the device. Reducing the amount of gallium, and applying higher resolution micromanipulation is necessary to produce consistent, hard tips.

The second topic of tip modification involves the electroless plating of a released CMOS-MEMS device. A new process, mimicking a STM tip fabrication process using a wire loop is utilized and made to function for a CMOS-MEMS process. This method is used to selectively plate many materials at the very tip of a CMOS-MEMS device with relative ease. In this work, a palladium and nickel surface is deposited onto a CMOS-MEMS device and qualitative tests have been performed on both types of plating to ensure that the material plated on the device matches the expected outcome. A quantitative test has shown that resistive contact can be made between the device and a probe tip. The success of each film is yet to be fully characterized. Work must be done to further refine this plating process to produce a higher yield of devices.

5. Experimental Validation

Following the design considerations, simulations and the fabrication process, a variety of CMOS-MEMS KPFM cantilever are fabricated. The optimized device designs have been submitted for fabrication, but to this date, have not been fully processed yet. The first design seen in Chapter 3, however, has been fully released and characterized. An SEM micrograph of the device is seen in Figure 64. Through vigorous testing, it is the goal of this section to demonstrate the validity of the CMOS-MEMS KPFM.

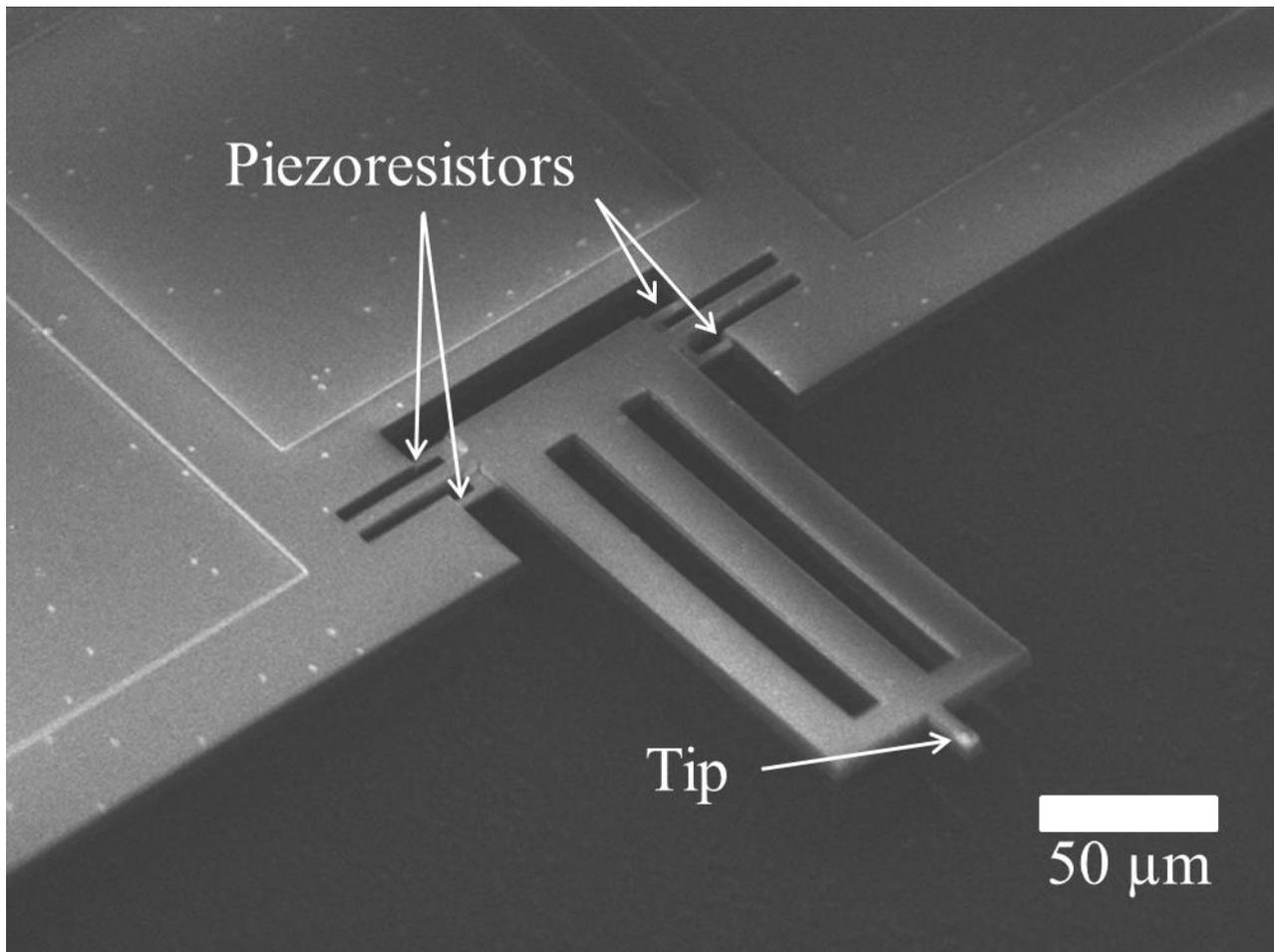


Figure 64: Released CMOS-MEMS KPFM cantilever

There are five $140\ \mu\text{m} \times 140\ \mu\text{m}$ pads on this device. Two of the pads are used to deliver the bias voltages to the bridge circuit; two pads are used to detect the output voltage signals from the bridge. The final pad is used to deliver the KPFM signal to the tip of the device. The signal is contained in a fully grounded shielded path all the way to the tip. The entire front plate of the cantilever is grounded with the exception

of the tip. To prevent outside interference with the inner circuitry, grounded aluminum is placed all around the pads.

To obtain characteristics from the device, two methods can be used. The five pads can be probed with DC tungsten probes. However, this creates additional noise paths. For this reason, wirebonds are used instead. The chip is mounted to a dip package with silver epoxy and allowed to bake at approximately 120 °C for an hour. Wirebonds are made to connect the device to the pins of the dip package. The package is placed on a breadboard.

The resistance is measured between the piezoresistors to make sure that there are no design flaws within the inner circuitry. Since all four resistors are equal in physical size, the resistances are roughly similar. According to the sheet resistances from the design rules document, the supposed resistances should be approaching 50 Ω /square with a range of 9.24 Ω /square. The resistance for each via hole connecting the aluminum to the polysilicon resistors are 26.3 Ω . Since the resistors are 7 μm long, from via to via, with a width of 1 μm , the expected resistance is roughly $402 \pm 32 \Omega$. The resistors are placed into a fully integrated differential bridge configuration, which means that the individual resistances cannot be measured – the one resistor will be measured in parallel with the three other resistors. It is however assumed that since all four resistors are relatively equal, measuring across the bias pads or the sense pads should give a rough sense of the resistance.

Roughly fifteen devices have been wirebonded and tested. Approximately 80% of the devices give measurements of $475 \Omega \pm 25 \Omega$. This is much more than the expected resistance, but the resistances of the aluminum routing lines, aluminum via holes, and wirebonding were not considered in the calculation. The other 20% of the devices exhibited short circuits of one or more resistor. Upon closer inspection, it is seen that poor wirebonding, connecting the pad and the upper grounded shield layer caused short circuiting. Removal of the poor wirebonds and rebonding occasionally produced the correct measurements, whereas other times, permanent deformations ultimately rendered the device unusable.

A voltage of 0.5 V is applied to the bridge as an initial test of the strain sensor. The voltage difference between the two sensor pads are measured to be on the order of 10 mV. This mismatch in voltage is due to the variation in resistors. Possible initial deformations in the tensile and compressive direction may have led to mismatching as well. A probe is lowered onto the cantilever, where a voltage change of up to 20 mV is observed. Since the force exerted by the probe cannot be measured, only a qualitative assumption that the strain gauge is functional can be made.

5.1. Implementation

The breadboard is taped to an optical bench. A Zurich Instruments lock-in amplifier (LIA) is used in the experiment. The instrument provides DC and AC outputs, as well as differential inputs. The LIA allows filtering of the noise outside of the frequency bandwidth being observed. The device is connected to the LIA as shown in Figure 65. The differential outputs measure the difference between two voltages. The voltages being measured are between the sensor pads and ground. A larger DC voltage allows for higher sensitivity, but at the same time, the higher current may cause damage to the bridge circuit. A DC voltage of 0.5 V is applied to the bridge to produce approximately 1 mA of current. The signal from the KPFM tip travels from the base through the cantilever to the tip, where it forms a capacitor with a grounded probe near the tip surface.

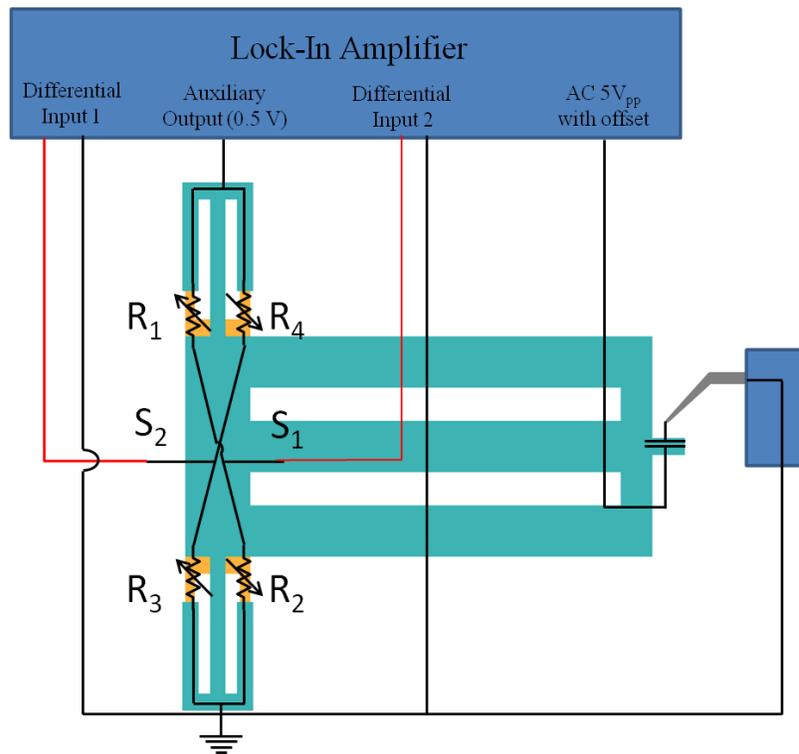


Figure 65: Experimental set up of the KPFM

A large amount of problems occurred during testing, which led to a reduction in the amount of devices. Testing the device with an unstable DC probe approach mechanism causes the probe to deeply contact the cantilever. Since the device is stiffly attached to the base, the probe pins the cantilever to the substrate, often causing catastrophic failure. This can be rectified in future designs by developing a more controlled

coarse approach mechanism. Secondly, snapping of the substrate, as demonstrated in Figure 58 disallows the pinning of the cantilever during the probe approach.

Secondly, it is found that the device often fails from electrostatic discharge. Two via holes in series connect the piezoresistor to an aluminum track. A large voltage difference may occur between the two via holes less than 1 μm apart, causing electrostatic discharge upon initial powering. This will destroy the circuit. Upon powering off, isolated charges may build up causing electrostatic discharge as well. The resistors are measured again after this occurs. This is the probable explanation after working devices are retested, only to see an open circuit. To mitigate this effect in the future, only one via hole is used per end of the resistor. It is also important to turn off the power supplies in a specific order. The circuits should be disconnected before turning on or off any power supply. The sudden impulse may cause electrostatic discharge, destroying the device.

Once the device is properly operating, the tungsten DC probe approaches the aluminum cantilever. A frequency sweep is performed between 10 kHz to 400 kHz with AC coupling; as this eliminates the initial DC mismatch from the difference in resistors. However, it is found that an extremely large, noisy signal throughput is shown; in fact, moving the probe far from the cantilever surface did not noticeably change the results. It is also noticed that the beam did not visibly oscillate. Powering down the 5 V_{p-p} signal to the tip resulted in no signal. A DC probe is brought into contact with the cantilever, visibly showing a deformation in the beam, yet shows a smaller change in signal than when the signal to the tip was applied. Since the oscillation of the beam is unnoticeable under the microscope during the signal input to the tip, there is strong evidence that the signal is coming from the coupling between the signal and the piezoresistors. After this investigation, it is necessary to revisit the design and evaluate a new method of placing the signal to the tip. To mitigate this effect, it is important to place the signal line far from the piezoresistor path, and encasing the structure in an external shielding.

In order to test the validity of the CMOS-MEMS KPFM with the device, a new method is considered, where the signal is instead applied to the tungsten DC probe. The tip is grounded instead, such that the grounded signal path does not interfere with the piezoresistors. This set up can be observed in Figure 66. This presents other problems, since the cantilever is also shielded. The signal may become stronger since the area for a capacitor is much larger, increasing fringe fields. However, due to the lack of a tip, the device can no longer operate in a high resolution regime. Changing the signal path in the future will help to resolve high resolution imaging. However, for the purposes of this thesis, this method can be used to validate the CMOS-MEMS KPFM.

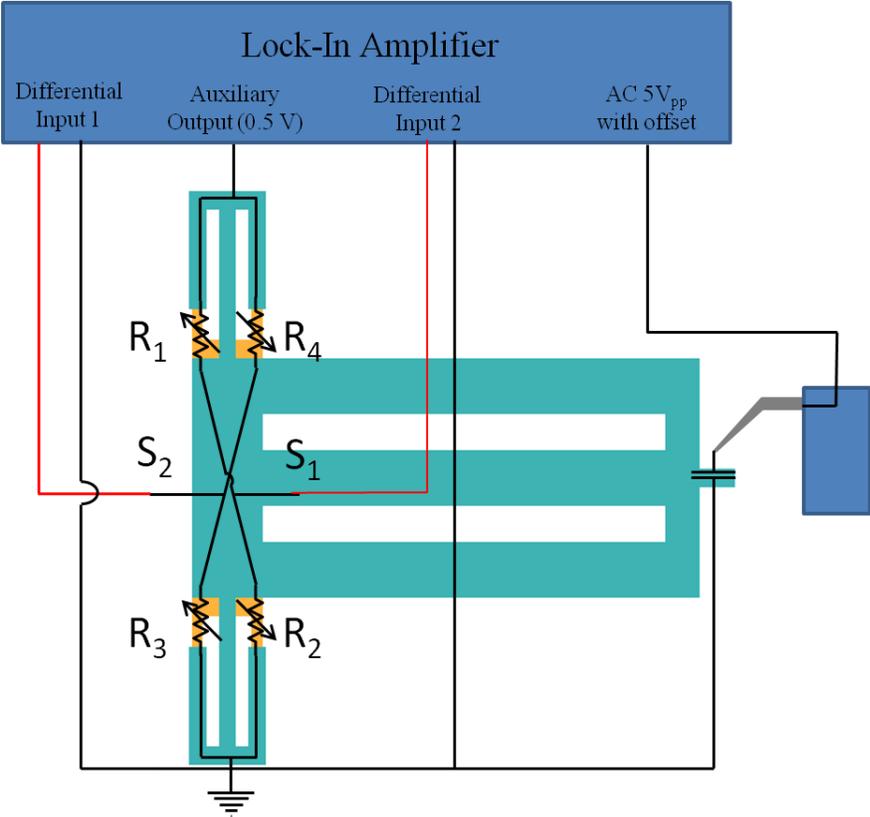


Figure 66: Experimental set of KPFM with no noise coupling

5.2. Results

The DC probe with the AC signal is placed in proximity with the device. A frequency sweep is run from 10 kHz to 400 kHz. The amplitude and phase with respect to the frequency is seen in Figures 67 and 68 respectively. Figure 67 shows increasing amplitude with frequency. This is due to high frequency parasitic capacitive coupling. The signal does not come from the deflection of the cantilever beam due to deflections, but actually resultant of the noise caused by coupling.

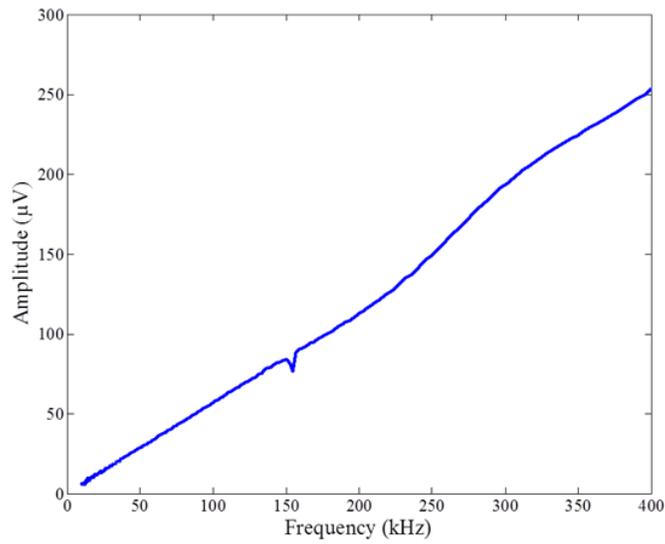


Figure 67: Amplitude of frequency sweep for a KPFM under electrostatic influence

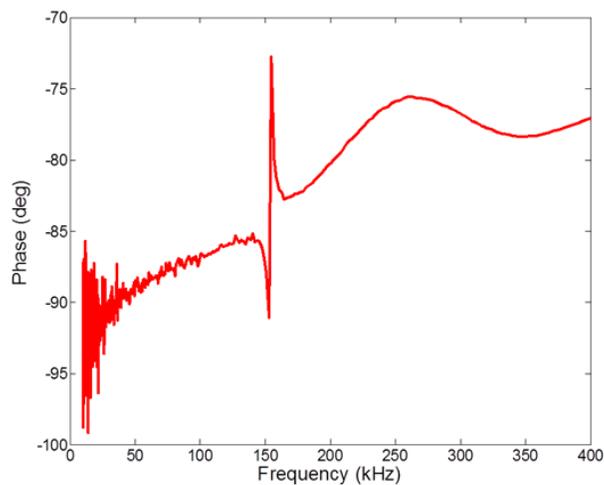


Figure 68: Phase of frequency sweep for a KPFM under electrostatic influence

At approximately 150 kHz, a resonant frequency is observed. A close scan reveals the resonant frequency to be at around 153.5 kHz. All the frequency sweeps are henceforth performed at a frequency between 148 kHz and 158 kHz. The operation of the amplitude modulated KPFM is performed at the resonant frequency, as the increased Q helps to improve the signal to noise ratio. A DC offset, V_{DC} , is placed on the AC signal. The V_{DC} offset is changed every frequency sweep, varying between -2.5 V to 2.5 V. Once the work functions align, and the contact potential difference, V_{CPD} , becomes zero, the amplitude of the signal will flat line. The amplitude of the signal is plotted against the frequency, and is shown in Figure 69.

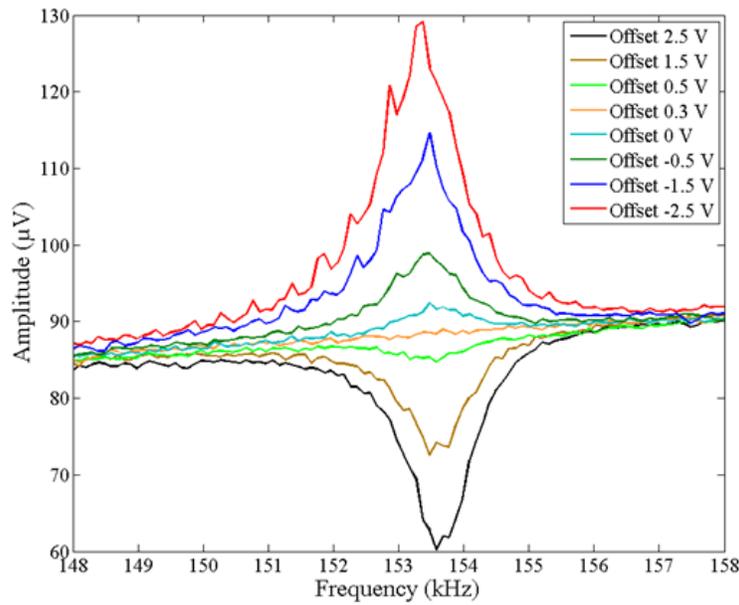


Figure 69: Frequency sweep of the device while varying V_{DC}

It can be seen that at a V_{DC} of 0.3 V, the amplitude peak of the resonant signal is minimized. However, it can be noted that between 0.3 V to 2.5 V, the amplitude of the signal goes beyond the baseline signal in a negative direction. The lowering of the signal means that the amplitude of the device becomes smaller. This is counterintuitive, as this suggests that the beam amplitude will reach a minimum voltage of 0 at some point while increasing the V_{DC} . However, this does not suggest that the V_{CPD} between the two materials occurs at this high voltage offset.

As the device is in operation, a sinusoidal signal is applied to cause deflection in the beam via electrostatic forces. This will cause the beam to move with a certain amplitude throughout a frequency sweep with a certain phase. At the resonant frequency, the amplitude of the signal rises. However, once the V_{DC} is applied such that it matches the V_{CPD} , equation (3.7) will tend towards zero, eliminating the amplitude. Once V_{DC} passes the contact potential difference, the sign of equation (3.6) switches, causing

the amplitude of the signal to flip. This changes the resonant peak into a resonant valley. Changing the amplitude of a sinusoidal waveform from a positive value to a negative value can be resolved as a 180° phase shift. With a Fast Fourier Transform, this corresponds to a resonant valley with respect to the original phase. Hence in this case, the force is not minimized as the amplitude continually decreases, but grows in the negative direction. The only point at which neither a peak nor a valley forms is when the DC offset bias is equal to the contact potential difference. The residual signal from the baseline results from the mismatch in the bridge circuit.

This is proven further by changing the direction of the bridge voltage. Changing the bridge bias voltage from $+0.5\text{ V}$ to -0.5 V causes values between 0.3 V and 2.5 V to form a resonant peak, whereas any offsets below 0.3 V forms a resonant valley. The swapping of the bridge bias voltage changes the beam the oscillation by a 180° phase shift. Initially, if a beam is deflected to give a positive voltage, swapping the bridge bias will cause the same deflection to give a negative voltage. Regardless, the 0.3 V offset causes the signal to stay constant, eliminating any amplitude. This can be seen in Figure 70.

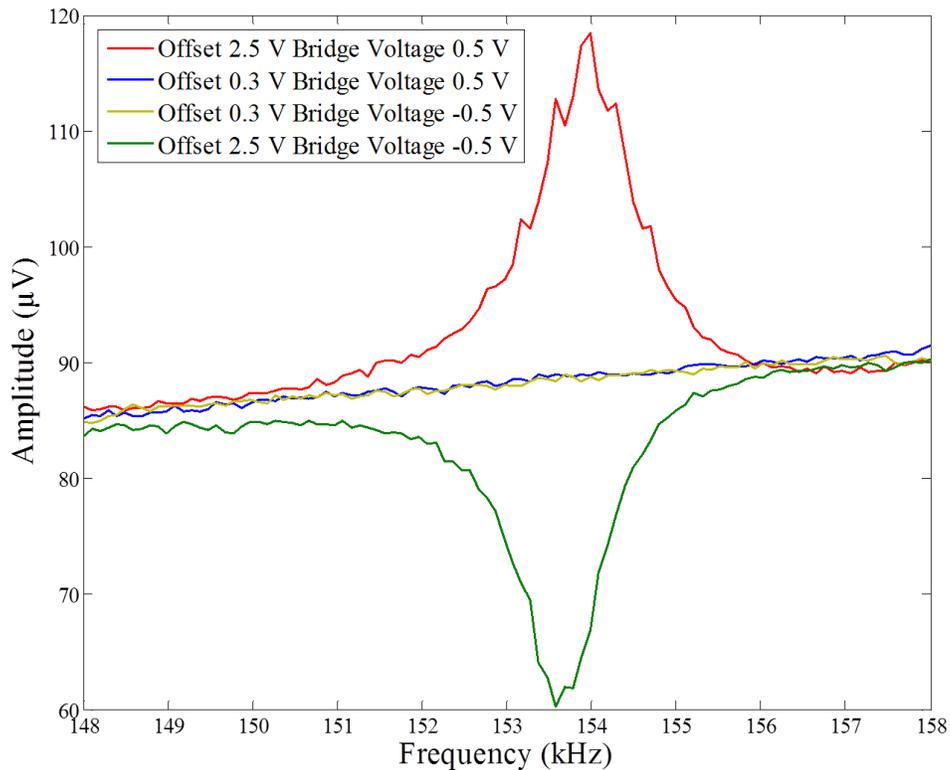


Figure 70: Effects of slipping bridge voltage with signal output

At 0.3 V, it can be seen that the V_{CPD} is equal to the V_{DC} . Since the signal goes through the tungsten DC probe, it can be said that the tip is tungsten, and the sample is the aluminum. Following equation (3.1), the work function of tungsten is shown to be 0.3 eV less than that of aluminum. From literature, the work function of tungsten and aluminum are 4.32-5.22 eV and 4.06-4.26 eV, respectively [75]. From the results, it can be seen that the results are opposite of the literature results. These results, however, are heavily dependent on the cleanliness of the surface being measured. Any particulates on the surface of the material will directly influence the surface charge measurement. Especially in the case of this fabrication process, the CHF_3 causes polymer to be deposited around the device, as discussed in Section 3.3. This polymer is not cleaned prior to the measurement. It is entirely possible that the polymer affects the surface charge in such a way that the true quantitative difference between aluminum and tungsten is not seen.

In addition, the tungsten work functions are based off of measurements from very specific crystal planes. Changing the crystal plane orientation can change the work function by almost 1 eV [75]. While the work function of any of the previously measured crystal plane does not go below 4.32 eV, the tungsten DC probe has been used thoroughly through different experiments previously. This increases the chance that the DC probe has already been oxidized previously. Also, as the tungsten probe was previously used in other probing experiments, residues from previous experiments may have reacted with the tungsten probe.

An important aspect of the verification includes the need to test for any coupling between the signal line and the piezoresistors. As seen in the earlier experiment, the signal in the line can couple to the piezoresistors; hence it is not entirely impossible for the signal from the probe to couple with the piezoresistors.

In this case, a bias voltage of 2.5 V is set on top of the AC signal to the tungsten DC probe. A frequency sweep is performed over the same range in order to capture the resonant frequency peak. On a second pass, the bridge is unpowered. This means that any coupling from the tungsten probe will show up in a voltage read out, caused by the current coupling from the signal line into the resistors. Figure 71 shows the amplitude of the frequency sweep when the bridge is powered and unpowered. It can be visually determined that the unpowered bridge does not show signs of coupling, as the signal amplitude does not change. The majority of the signal comes from cantilever deflection when electrostatic forces move it mechanically.

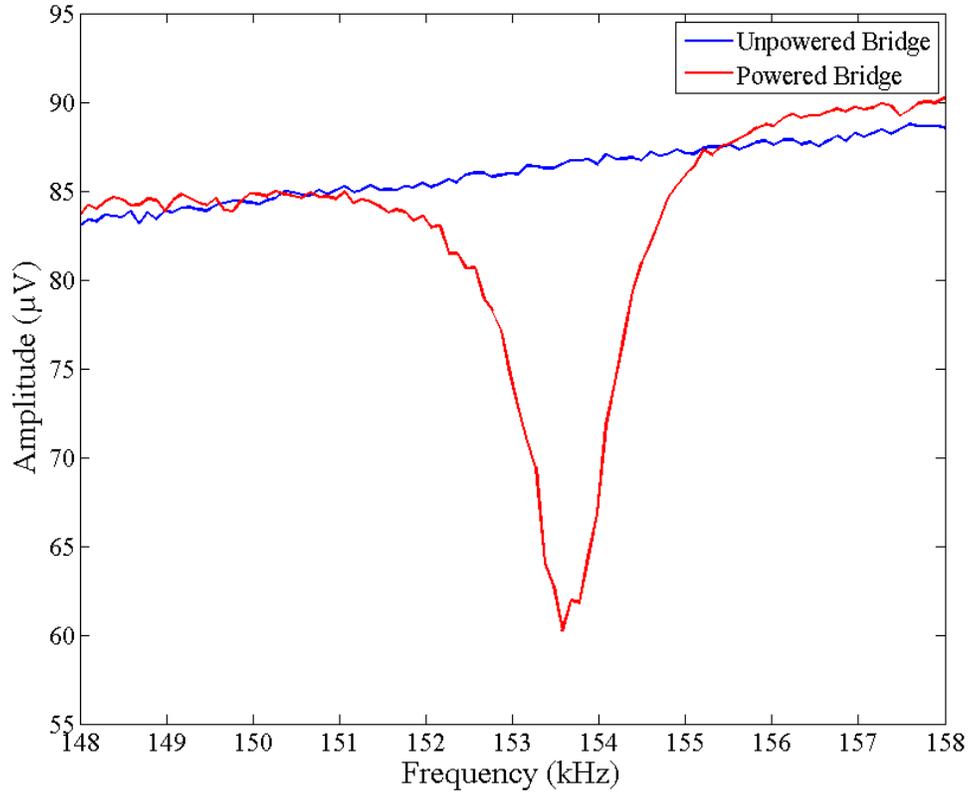


Figure 71: Frequency sweeps of a powered and unpowered bridge

Equation (3.8) shows that the second harmonic is independent of V_{DC} and V_{CPD} . Initially, the 2nd harmonic is monitored during a frequency sweep between 148 kHz and 158 kHz. However, the Q of the 2nd harmonic is extremely low, and a visible signal is not observed. However, by reducing the frequency parameters by a half – sweeping between 75 kHz and 80 kHz – while monitoring the second harmonic, approximately 153.5 kHz, the amplitude of the signal can be easily observed. While the bridge is powered, the frequency is swept when the applied V_{DC} is 2.5 V and 0 V. Figure 72 shows that the two signals directly over top each other, indicating that the change in these values do not offset the signals, thus verifying that the forces observed are indeed based on Kelvin Force Microscopy.

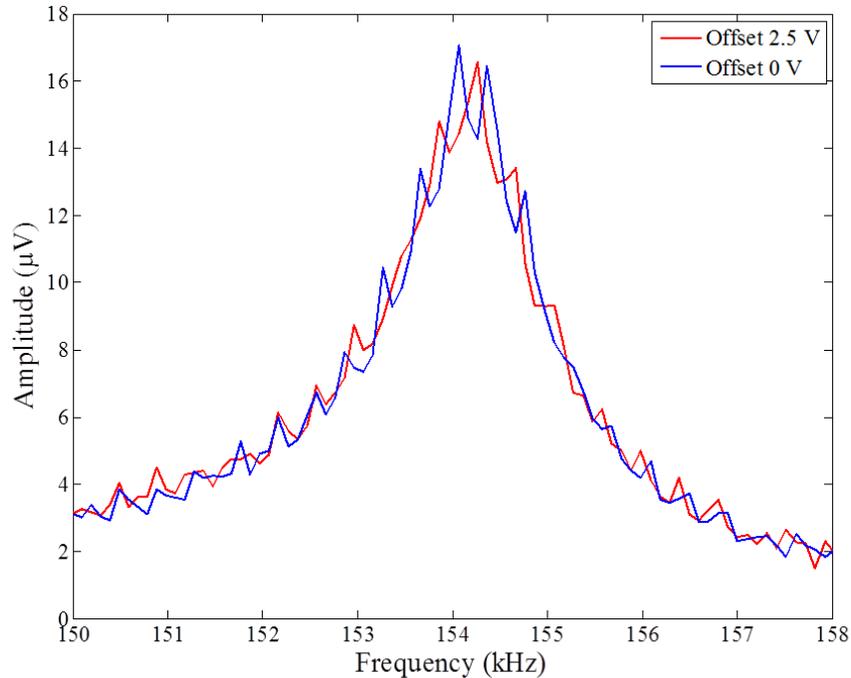


Figure 72: Frequency sweep of the 2nd harmonic with different V_{DC}

It can be seen that a large amount of noise is observed from the persistent peaks in the data. This is caused primarily by the DC probe, which was connected to the micromanipulator by a long cantilever. This long mechanical path allows small vibrations at the base to grow in amplitude at the tip of the DC probe located the opposite end. From equations (3.6-3.8), it can be seen that the changes in capacitance with respect to the distance between the two materials effects the electrostatic forces that the cantilever experiences. The experiments in both the first and second harmonic regime experience this noise factor. To reduce the noise an anti-vibrational table was used to acquire further results.

The SNR of the resonant signal is calculated at the signal given at -2.5 V. The standard deviation of the noise is calculated to be approximately 1.256 μV . The normalized signal from the baseline to the signal generated at -2.5 V has a signal amplitude of 40 μV . SNR can be taken as $20\log_{10}(40/1.256)$, which is equal to 30.05. Given that we wish to have an SNR of at least 4, the minimum detectable signal should be at least 2 μV . This is equal to approximately 140 mV of resolution, or a work function resolution of 140 meV.

A second, similar device is tested in an anti-vibrational SUSS probing system. Similarly, the set up observed in Figure 66 is maintained within this system. The frequency is swept, however, the resonant frequency was found to be 205.5 kHz, which is much higher than the resonant frequency of the previous device. This can be associated with damages that occurred during the system set up. Visible obstructions

were seen on the device after a DC probe made physical contact with the device. At the same time, due to the damages, and higher resonant frequency, the amplitude of the Q will also be lower. Again, the frequency is swept while varying the offset voltage. This is seen in Figure 73. The signal noise is considerably smaller, and the amplitude of the signal is reduced by more than $\frac{1}{2}$. Again, it can be seen that a V_{DC} of approximately 0.3 V reduces the amplitude of the signal to the baseline. Again, resonant peaks and valleys can be seen by varying the V_{DC} past the V_{CPD} .

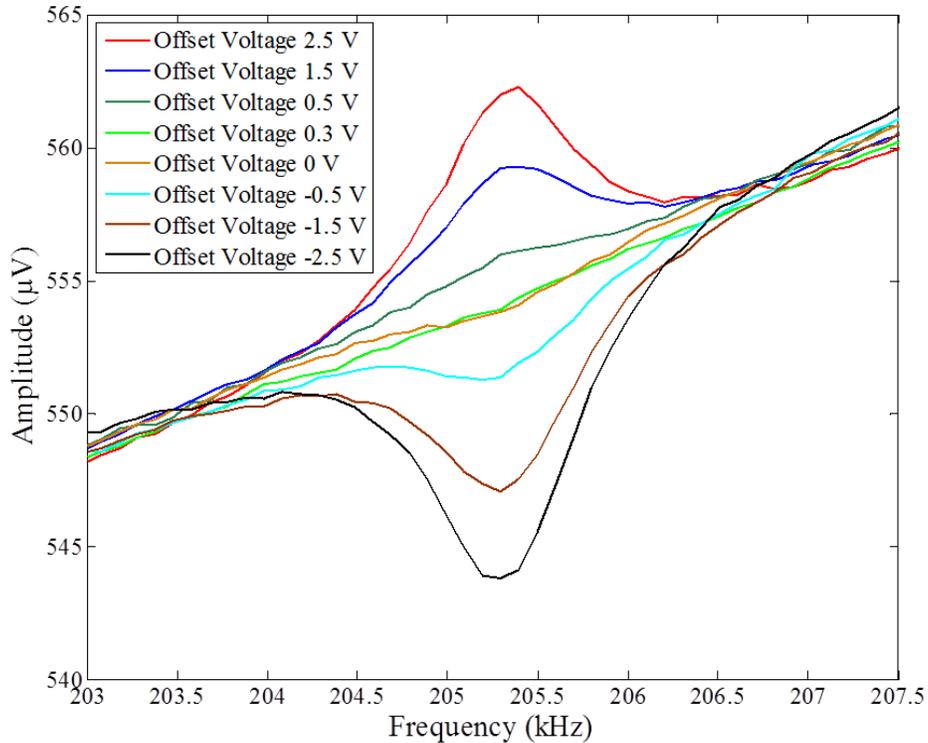


Figure 73: Frequency sweep of KPFM device in anti-vibration system

Similar tests are performed to verify the validity of the device. Again, Figure 74 shows that the signal does not couple directly with the piezoresistors. The second harmonic also directly overlaps again, as seen in Figure 75. This shows that the devices with different resonant frequencies show similar results in determining the V_{CPD} .

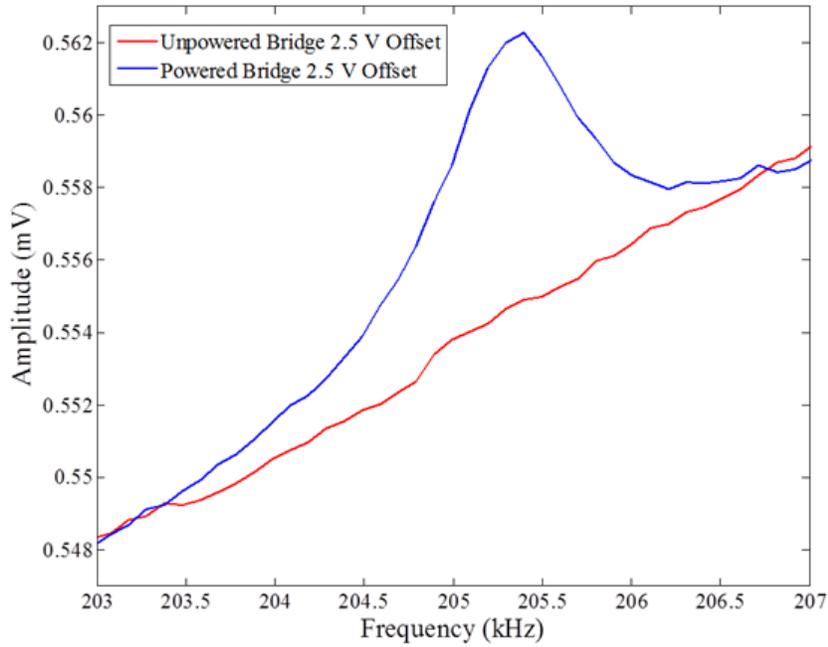


Figure 74: Frequency sweeps of a powered and unpowered bridge in an anti-vibration system

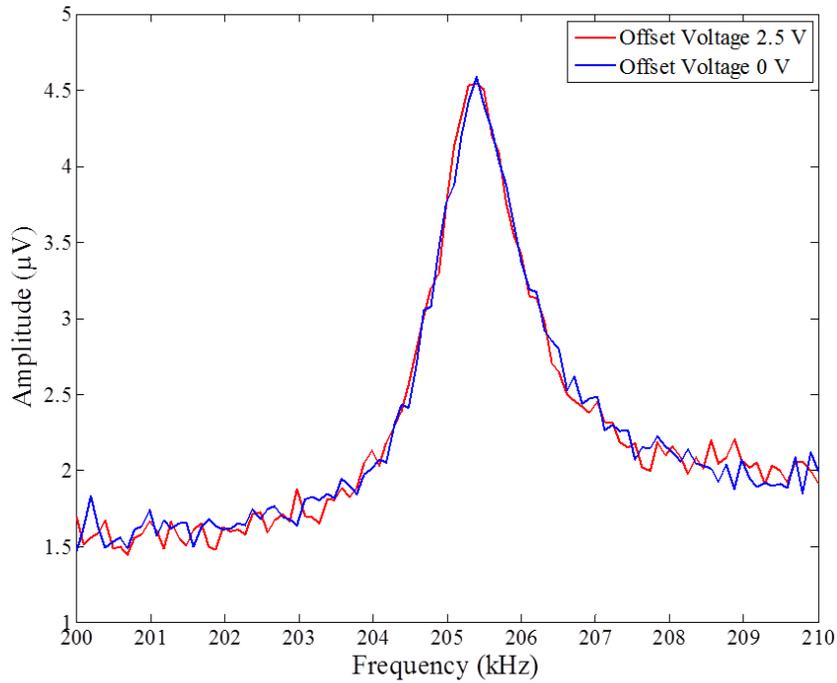


Figure 75: Frequency sweep of the 2nd harmonic with different V_{DC} in anti-vibration system

Similarly, the SNR can be calculated for this system. The standard deviation of noise is calculated to be approximately 0.1376 μV . The normalized signal from the baseline to the signal generated at -2.5 V has a

signal amplitude of 12.2 μV . SNR can be taken as $20\log_{10}(12.2/0.1376)$, which is equal to 38. Given that we wish to have an SNR of at least 4, the minimum detectable signal should be at least 0.218 μV . This is equal to approximately 50 mV of resolution, or a work function resolution of 50 meV.

However, this device was damaged and operating at a higher than expected resonant frequency. Due to the higher resonant frequency, the Q will be much lower, reducing the amplitude. If the noise factor of the anti-vibration system operates with the amplitude of the undamaged, lower resonant frequency device, an SNR ratio of 50 can be expected. The minimum detectable signal with an SNR of 4 will be 15 mV. To further increase the resolution, the device can take measurements in vacuum, which will increase the Q, and hence, the SNR ratio.

Next, to determine that the device is able to discern different materials, gold is used as a sample. In order to apply the gold, the tungsten probe is scratched across the surface of the gold until a large appreciable chunk is seen clinging onto the tip. Again, the same procedure is used to obtain measurements. Three sets of frequency sweeps are taken. It can be seen that at approximately -1.5 V, the sweep becomes fairly linear, indicating that the V_{CPD} and V_{DC} are similar. The application of a -1.5 V DC offset equates to a work function difference of -1.5 eV. The aluminum CMOS-MEMS KPFM can discern different work function from different materials.

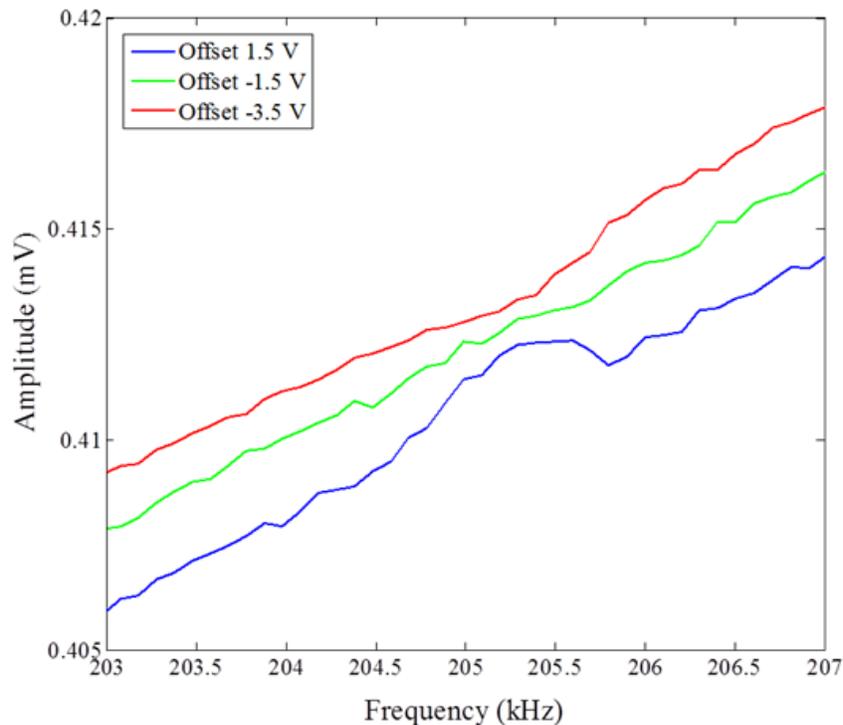


Figure 76: Frequency sweeps with gold as a tip

The amplitude of the signal seems weak. This is due to the fact that the gold rubbed onto the tungsten probe is not stable. To prevent collisions, the probe is lifted from the surface, minimizing the capacitance. The data can be normalized, and is seen in Figure 77.

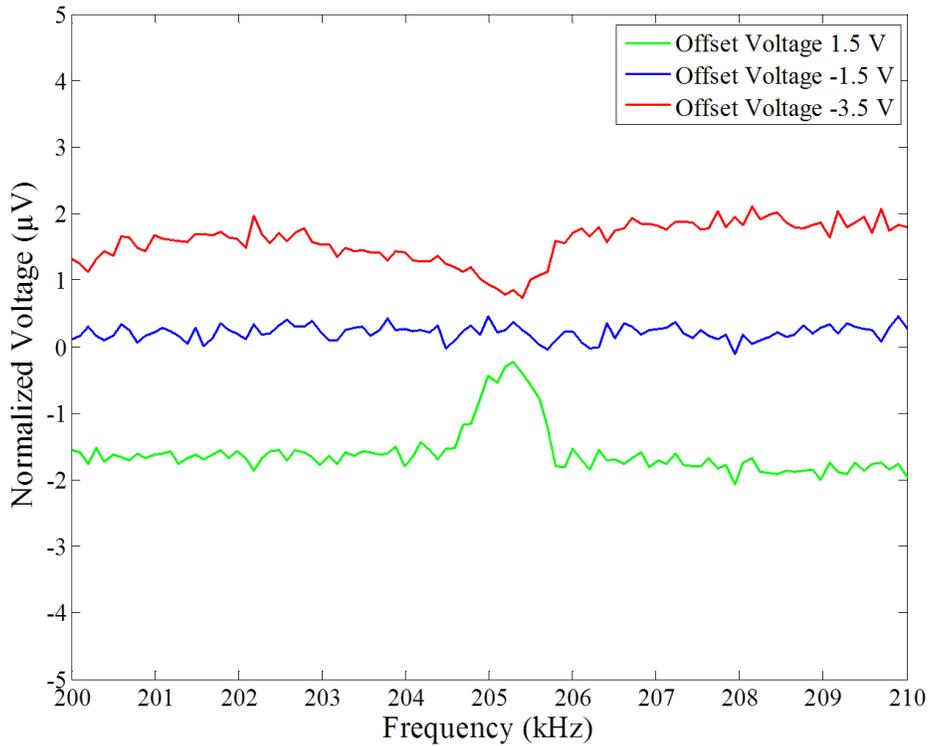


Figure 77: Normalized frequency sweeps with gold as a tip

The work function of gold is approximately 5.1 eV to 5.47 eV [75]. The difference between the aluminum sample and gold tip work function is approximately -0.84 eV to -1.41 eV. Again, the changes in the surface alter the results of the work function quite intensively. Removing a film of gold from a wafer with a DC probe guarantees no specific configuration of gold particles; hence the work function can vividly change. Other impurities heavily alter the work functions observed. The important factor of this experiment is that different work functions are present when changing from sample to sample. In order to obtain a proper KPFM image, it is necessary to discern relative work functions, not the absolute work function.

Finally, in order to create a proper KPFM image, an integrated stage must be utilized to scan a surface. The next section shows the integrated CMOS-MEMS XYZ-stage.

5.3. XYZ-Stage Implementation

Two methods of XY-stage implementation was presented in Section 3.6. These were designed and fabricated. The decoupled XY-stage can be seen in Figure 78a, and the rotational XY-stage can be seen in Figure 78b.

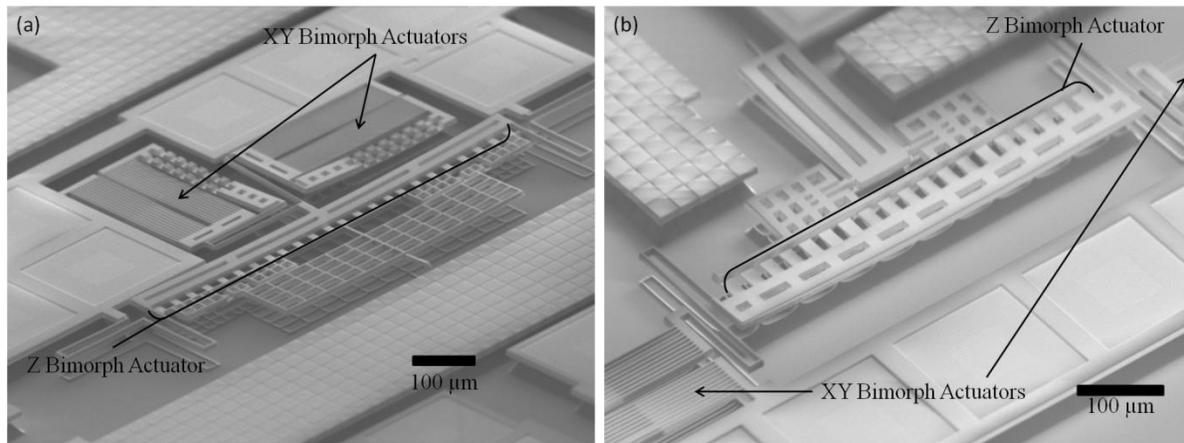


Figure 78: (a) Decoupled bimorph XY-stage and (b) Rotational bimorph XY-stage

Following the same scheme as shown in Figure 58, where the cantilevers are positioned over pre-diced edges such that upon snapping, the tips hang over the edge. Once flipped upside down, the approach of the tip to the surface can be seen. The XY-actuators can move the tip across the surface; the Z-actuator is used for fine positioning, as well as determining the height profile of the surface. These are wirebonded to a PCB board and wirebonded. The final product is shown in Figure 79.



Figure 79: Packaged KPFM device

As described earlier, the XY-actuators presented in Figure 77a shows decoupled X- and Y-bimorph actuators; where each actuator acts to move the stage in one dimension. Large stubs are put into place to add thermal isolation between the two actuators in order to limit the thermal transfer between the two actuators. Heating one actuator causes a small amount of heating of the second actuator, causing unwanted movement in the other dimension. The two actuators are attached together at the stage, which contains the Z-actuator and the KPFM cantilever. Upon release of the decoupled XY-actuator stage, the bimorphs deform slightly to relieve stress. The devices take a large amount of time to release due to the size of the stage; this may cause possible damage to the stage. Future iterations reduce the size of the stage from 15 μm beams to 8 μm beams. Figure 80 shows the results of a 21 minute release – generally, the cantilever beams with the thin piezoresistor portions are released within 15 minutes.

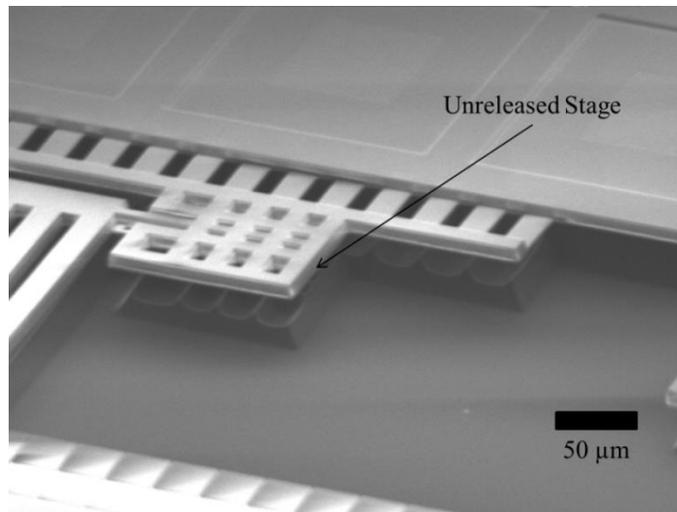


Figure 80: Unreleased stage after 21 minutes of silicon etching

Unreleased structures are located underneath the thick beams with tiny release holes. Once the stages are fully released, the residual stresses of the beams can be released. 24 minutes of silicon etch are required to release the stages such that the XY-actuator stage deforms. No observable damage is seen. A voltage is applied to heat the beams up such that the XY-actuators deform. At approximately 8 V, the actuators melt. Since the resistors are approximately 660 Ω , 12 mA pass through the device, massively heating the device. Since the layer of polysilicon is so thin, it is unsurprising that the heat generated from the polysilicon will melt the thin devices. Less than 10 μm of distance is observed in both the X and Y direction, following simulations. The displacement upon actuation is parabolic, as seen in Figure 81.

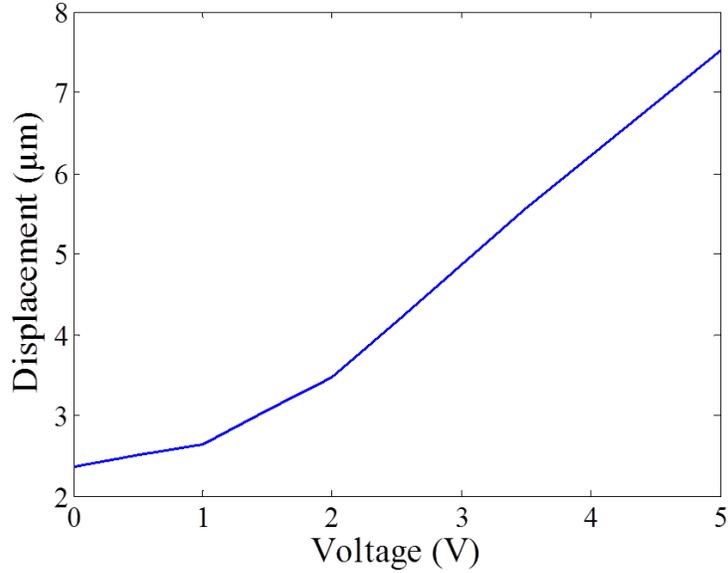


Figure 81: Bimorph actuator displacement during actuation

The current is linear with respect to the voltage, but the conversion to heat is dependent on the current squared. This means that increasing voltage linearly will increase the temperature in a parabolic fashion. Since the thermal expansion is linearly dependent on temperature, the displacement should increase in a parabolic fashion. This can be made linear by applying calibration to the software side.

Figure 82 shows the displacement of the tip upon actuation of the bimorphs. Figure 82a shows x-directional movement upon actuation of the x-axis thermal bimorph beam. Figure 82b shows the y-directional movement upon actuation of the y-axis thermal bimorph beam. The displacement is approximately $2 \mu\text{m} \times 2.5 \mu\text{m}$.

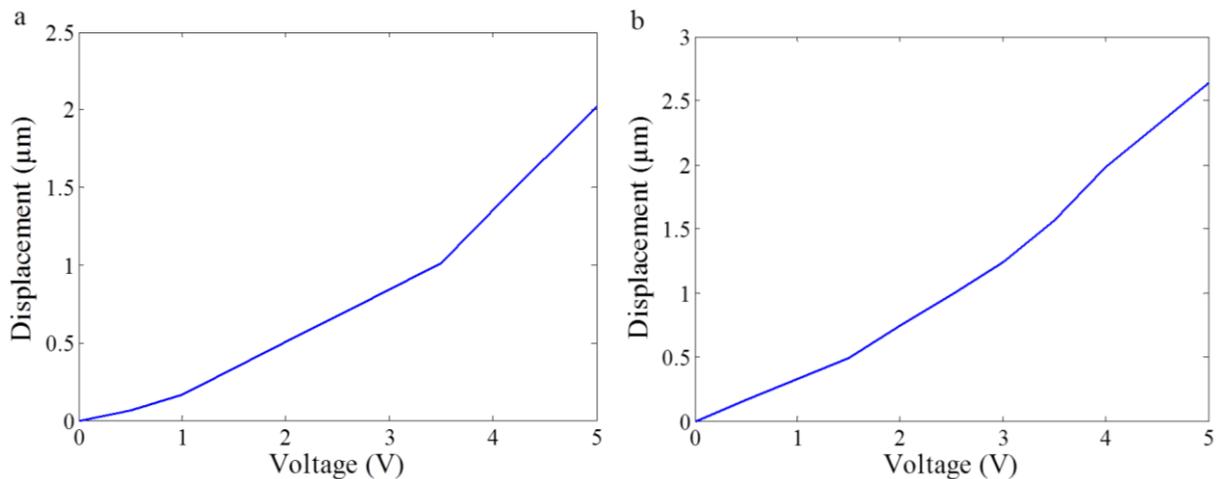


Figure 82: (a) X-displacement of tip upon x-actuation, (b) Y-displacement of tip upon y-actuation

The activation of one bimorph actuator does not heavily perturb the bimorph actuator of the opposing axis through thermal coupling. However, slight flexural coupling of the displacement occurs at the stage upon the activation of one actuator; a slight torque is seen on the stage during movement. The amount of movement in the X-axis upon activation of the Y-axis is much less than the movement in the Y-axis upon activation in the X-axis. Figure 83 shows the flexural coupling between the beams. Figure 83a shows x-directional movement upon actuation of the y-axis thermal bimorph beam. Figure 83b shows the y-directional movement upon actuation of the x-axis thermal bimorph beam. The intense coupling of the y-axis during x-actuation should be fixed within the actual MEMS design instead of using software correction, as the coupled movement is within the same magnitude as the wanted displacement. To correct for this, the x-actuator should be placed in the middle of the y-axis of the stage to limit the rotation. The y-actuator is placed in the middle of the x-axis of the stage, and can be seen to limit the flexural coupling in the x-axis upon actuation.

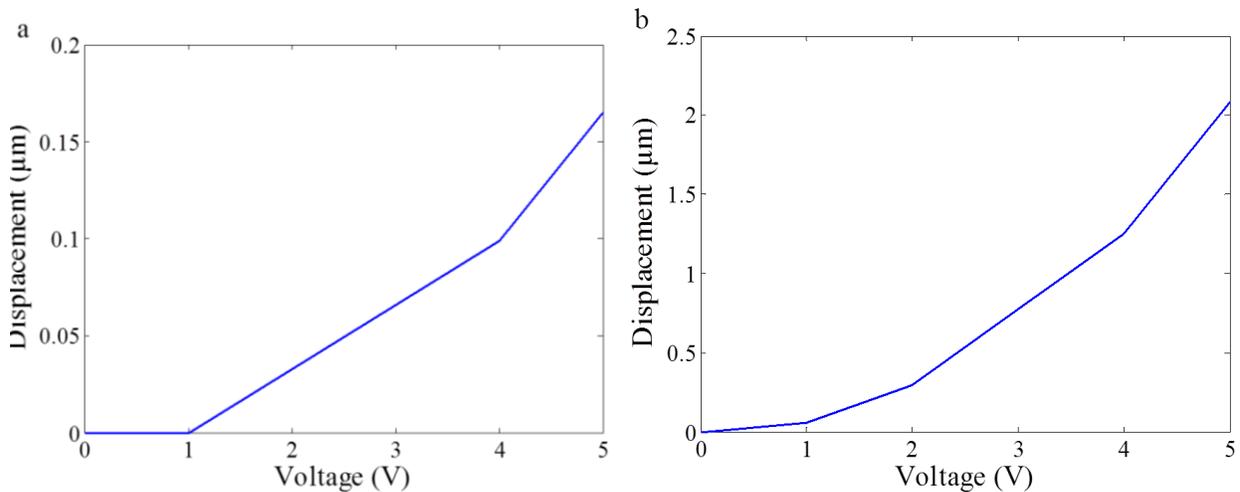


Figure 83: (a) X-displacement of tip upon y-actuation, (b) Y-displacement of tip upon x-actuation

Figure 77b shows two XY-actuators that are facing the same direction. The actuators are able to move individually, thus giving it angular and unidirectional movement. The actuators are attached to the main stage with extremely thin arms to allow the stage to bend and move without fracturing the device. The XY-actuators of the rotational stage also move less than 5 μm each. Thermal coupling can also be seen from one actuator to the other. In addition, the thin arms allowing the movement are extremely low in stiffness, and slight perturbations cause high amounts of physical deflection. Redesigns must be utilized to increase the spring constant.

The Z-actuators of both designs are similar. The stage is formed with a cascade of short M1 beams, also seen in Figures 77a and 77b. The M1 beam allows for ease in the bending moment from the heat.

However, at the same time, to increase the stiffness of the beam, a large number are needed, as the stiffness scales cubically to the length, and only linearly to the width. Upon release, a small amount of deflection from the residual stress can be seen. No visual deflection can be seen as a voltage is passed through the polysilicon.

An AC voltage is applied to the Z-actuator to allow oscillations in the Z-dimension. The vibrations should cause the cantilever tip to vibrate up and down as well. Once a bridge voltage is applied, the vibrations cause a small increase in amplitude during a frequency sweep compared to a frequency sweep with no actuation amplitude. This concludes that the Z-actuator is functioning, albeit a low amplitude. The next iteration of devices will include longer Z-actuators to allow for a larger deflection due to the initial residual stress of the system, such that the heating of the bimorphs allow for a wider swing. However, the use of longer M1 beams causes a reduction in the stiffness. Methods can be employed, such as the addition of thick M3 beams within the cascade of M1 beams to increase the stiffness of the Z-actuator.

5.4. Summary

This section outlined the implementation and testing of the devices. A basic cantilever beam with piezoresistive sensors placed in a Wheatstone bridge configuration, simulated in Coventorware are tested. The initial test of placing a signal through the tip, and placing it in close proximity with a tungsten DC probe did not produce results that show a functioning KPFM. To compensate for this, the signal is placed through the sample DC probe, and the KPFM cantilever becomes the grounded sample instead. The AC voltage through the DC probe allows the KPFM to oscillate due to electrostatic forces. The AC signal does not noticeably couple into the piezoresistors.

Applying a DC offset on top of the AC signal, allows the device to experience electrostatic KPFM forces. Varying the DC offset allows the amplitude of the cantilever oscillation to change, and at one point, causing a minimum oscillation. Beyond this point, either a resonant peak or valley will form. This is shown in two different sets of data with two separate devices.

In addition, to verify that KPFM is being observed, the second harmonic is monitored during frequency sweeps. Changing the DC offset does not change the amplitude of the signal, as suggested by the equations governing the KPFM. Frequency sweeps involving different offset voltages show direct overlap

in the observed signal. Results also show that scanning different materials result in different work functions; 0.3 eV between tungsten and aluminum, and -1.5 eV between gold and aluminum.

Finally, the XYZ stage is characterized. The bimorph actuators are able to move in their predefined paths. While thermal coupling remains an issue, additional thermal isolation, or software implementation can be used to reduce or compensate for the coupling. Small movements in all three dimensions are shown.

6. Conclusion

This section summarizes the research contributions. Outlines of future possible work are also discussed in this section.

6.1. Summary of Research

This thesis outlined three main topics, and as follows:

1. Methods to create CMOS-MEMS based KPFM devices are realized. Careful simulation allowed for the development of a new sensing geometry that increases the spring constant of the device without decreasing the overall stress of the system. FEA and simulations are performed to optimize the resulting geometry in order to achieve a spring constant that is able to function with AM-KPFM measurements. Basic XYZ-actuator schemes are realized in order to allow 3-dimensional cantilever tip movement, integrated within a MEMS device.
2. A method of electrolessly depositing a film onto a released CMOS-MEMS device is explored. At this time, two materials, nickel and palladium, have been plated onto a device. Qualitative results show that both materials have plated the device.
3. As far as the author knows, the first CMOS-MEMS KPFM has been validated using the equations that define a conventional KPFM. The work functions of different materials have been discerned using the CMOS-MEMS device. Additional validation from 2nd harmonic actuation and coupling between the signal line and the piezoresistors has also been explored. A 3-dimensional stage has been fabricated, and shows basic movement in all three directions.

6.2. List of Publications

The following is a list of academic publications related to this thesis.

Journal Publications

G. Lee, N. Sarkar, R. R. Mansour, “Design and Fabrication of a CMOS-MEMS KPFM.” (Pending)

Conference Publications

N. Sarkar, **G. Lee**, R. R. Mansour, “CMOS-MEMS DYNAMIC ATOMIC FORCE MICROSCOPE,” Transducers '13 (Pending)

6.3. Future Work

The following outlines the future work for this outlined research:

1. The electroless deposition of nickel has not been quantified. Submission of the device under strong magnetic fields should induce movement. Testing performed in proximity to an electromagnetic switching on and off will show in the piezoresistive sensors.
2. A new method of sharpening based on plasma fields is proposed. A high powered DC plasma is utilized between two electrodes within an argon environment. A MEMS device is placed in proximity with the field as the tip is positively biased. The positively charged argon ions race towards the negative electrodes. The high electric field of the tip allows repulsion of the ions; more from the tip point, where the field is the highest. Hence, overtime, a tip sharper tip can be milled from a dull tip.
3. Testing of the optimized KPFM device will allow for higher sensitivity measurements. The movement of the signal line further from the piezoresistors will limit the coupling that exists between the structures.
4. Further development of the XYZ-stage is needed. Labview code can be written to allow for 3-dimensional image scans of a sample while compensating for the thermal coupling. Further code is needed in order to track the decaying amplitude of the KPFM device as it is scanned across the surface, thus, creating an image.

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Appendices

Appendix A – Unmentioned Devices

The following are designs that have been fabricated, but are not included within the thesis due to lack of testing or awaiting return from fabrication.

Figure 84 shows the KPFM based on capacitive sensing. Figure 80a shows the basic design, with the interdigitated array functioning as the capacitive sensor. Figure 80b shows a device with an integrated Z-actuator, allowing for line scans.

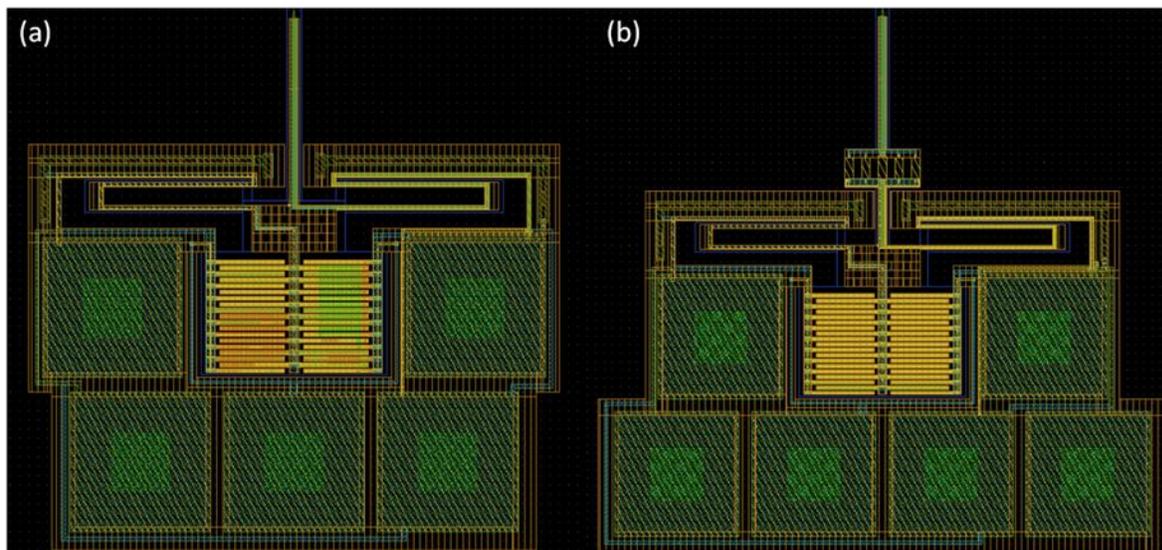


Figure 84: KPFM based on capacitive sensors

Figure 85 shows a device with large holes. This is meant to decrease the damping factor. The spring constant is relatively high with a double torsion plate. This results in a high Q device with the ability to resonate in air at large amplitudes.

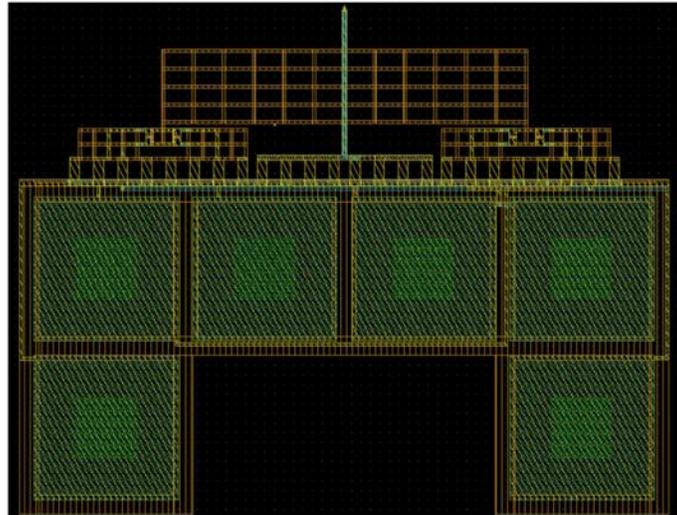


Figure 85: KPFM with low damping factor

Figure 86 shows a device optimized for stiffness and sensitivity. However, this device does not include moving the the signal line far from the piezoresistors.

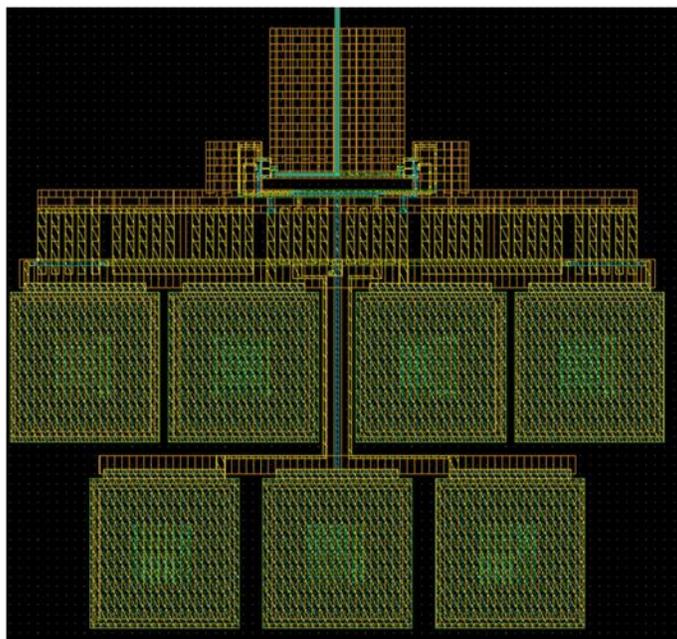


Figure 86: High stiffness, high sensitivity KPFM

Figure 87 shows devices that have been optimized for both high stiffness and sensitivity. It also includes the movement of the piezoresistor far from the signal line. Figure 87a shows an extremely large plate. This is to raise the spring constant of the device while extending the length of the device far from the anchor to allow for ease in assembly and use. Figure 87b shows a chevron based actuation system. This allows high stiffness in the XY-stage, allowing for highly stiff Z-actuation.

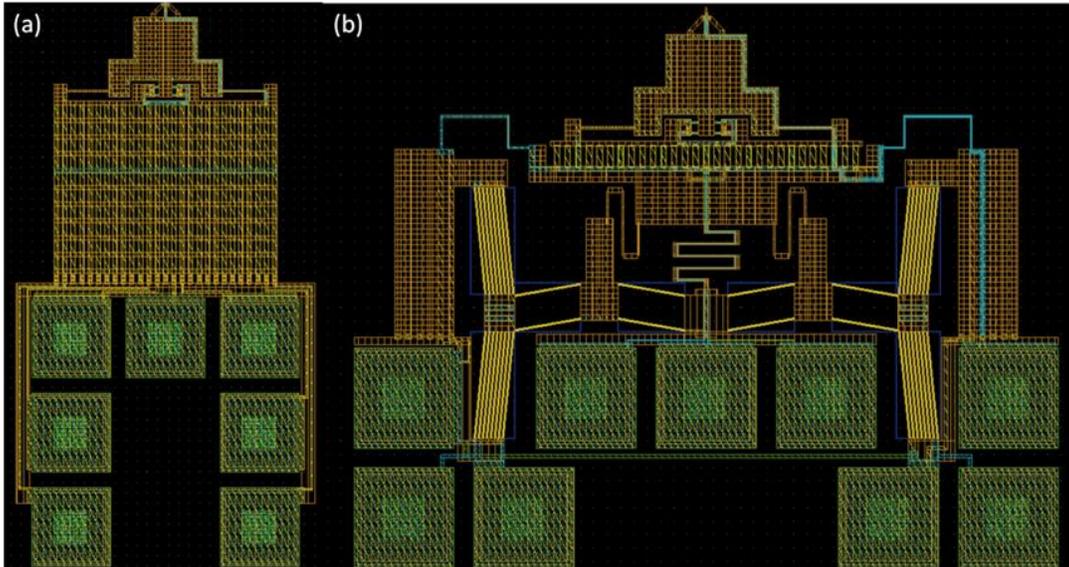


Figure 87: High stiffness, high sensitivity KPFM devices with piezoresistors far from the signal line

Figure 88 shows sensors based on capacitors, but based on the design ideas outlined for Figure 87.

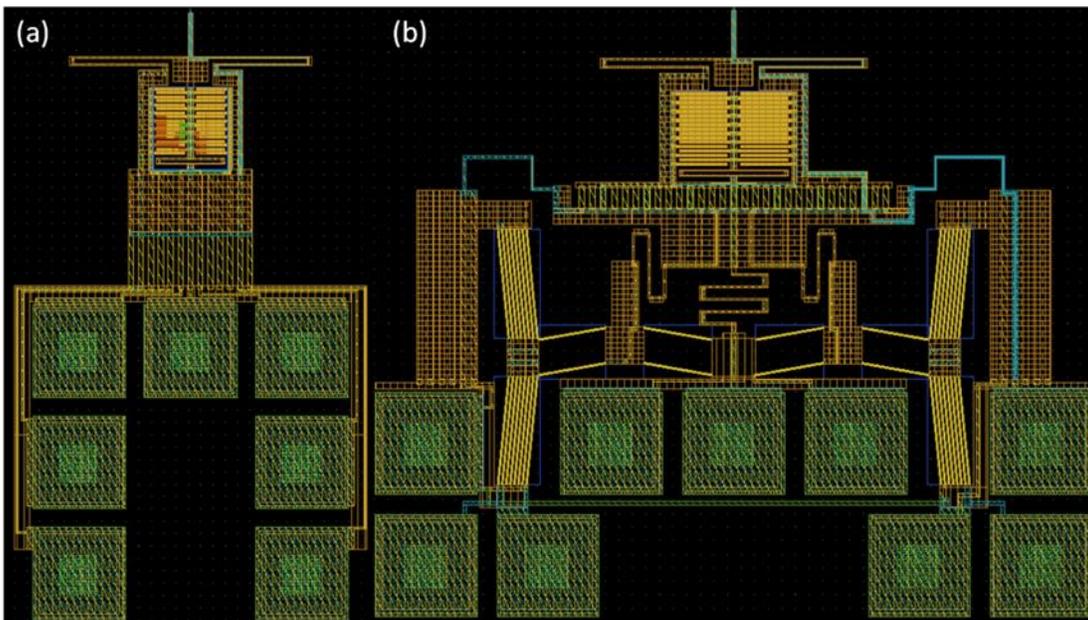


Figure 88: KPFM with capacitive sensors with various integrated stages

Figure 89 shows a device used for plasma sputtering. High plasma fields can be generated between two of the electrodes. A test cantilever can be actuated and thrown into the middle of the plasma to observe tip sharpening, as outlined in Section 6.3.

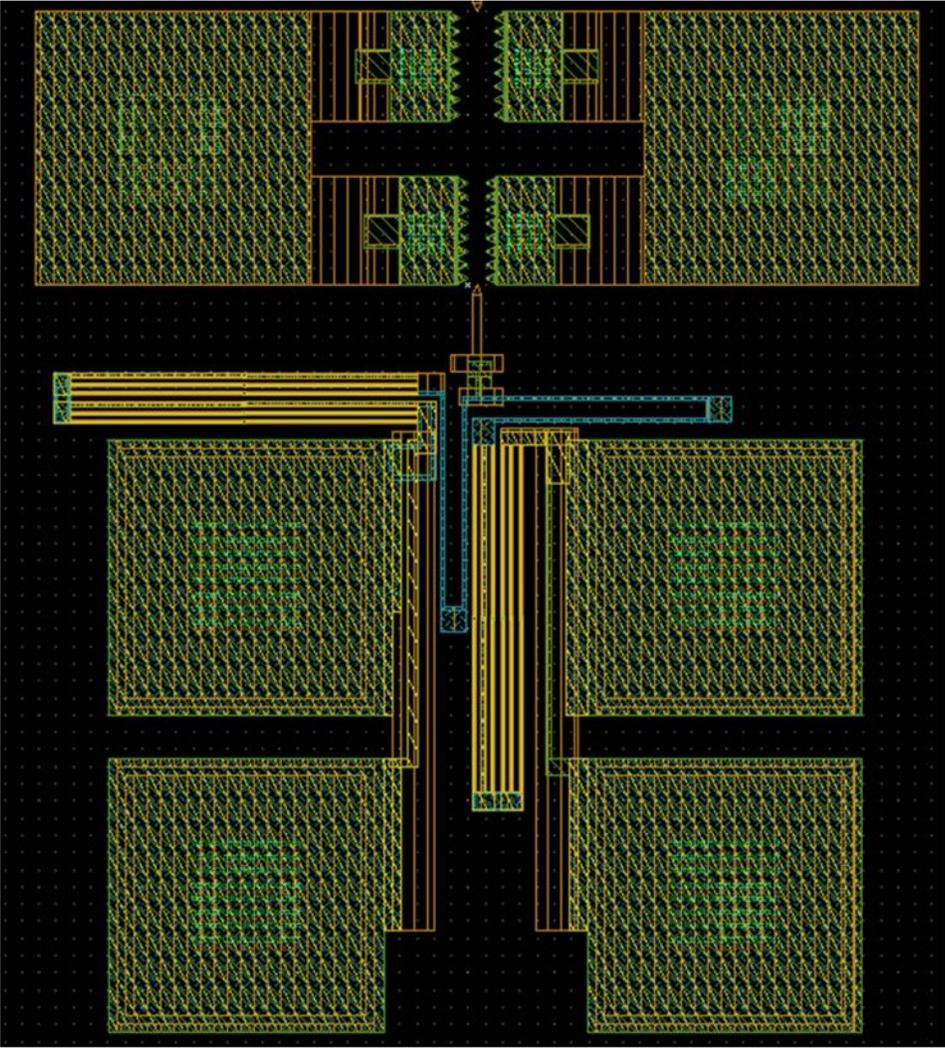


Figure 89: Device for experimentation in plasma sharpening of released CMOS-MEMS