Improved Overlay Alignment of Thin-film Transistors and their Electrical Behaviour for Flexible Display Technology

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

The integration of hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) with plastic substrates enables emerging technologies such as flexible organic light emitting diode (OLED) displays. Current a-Si fabrication processes, however, create residual thin film stress that affects the underlying flexible substrate due to its high mismatch in the coefficient of thermal expansion resulting in a dimensional instability for fabricating TFTs on large area flexible substrates. The motivation of this thesis is to reduce this non-uniformity and improve fabrication throughput of bottom-gated inverted-staggered a-Si:H TFTs on flexible substrates. This thesis therefore encompasses the study of overlay misalignment on TFTs over 3 inch flexible substrates and investigates the electrical characteristics of the TFTs fabricated on plastic platforms.

To reduce overlay misalignment of TFTs fabricated on flexible substrates, a plastic-on-carrier lamination process has been developed. The technique comprises of a polyimide tape to attach a 125 μm-thick poly-ethylene-napthalate (PEN) flexible substrate to a rigid carrier. This process has been used to minimize stress induced strain of the PEN substrate during the fabrication process; strain, which has been observed after processing a-Si:H TFTs on free-standing substrates. This technique would in turn assist in fabricating uniform stacked-layers as required for a-Si:H TFT fabrication on the PEN substrates. Overlay misalignment is measured after each of the 5 consecutive lithographic steps at 4 corner-most edges of the PEN substrates using a standard optical microscope. Results have shown an overlay misalignment reduction from 21 μm to 2 μm on average based on the TFTs fabricated on free-standing flexible substrates while ensuring a centre alignment accuracy of +/- 0.5 μm. Post fabrication adhesive removal to separate the PEN substrate from the rigid carrier has been accomplished by sample immersion in acetone. The results present a significant increase in fabrication throughput by reducing lithographic overlay misalignment such that the resolution of large-area flexible electronics would be enhanced. Electrical characteristics show the average performance of a-Si:H TFTs with an ON/OFF current ratio of 10^8, field effect mobility of $\sim$0.8 cm^2/Vs, and gate leakage current of 10^{-13} A.

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Lastly, I am grateful and forever indebted to my family for your unconditional love and support; I am nothing without you.

Dedication

This thesis is dedicated to my beloved Mama and Dada.

Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Flexible flat panel displays

The recent advancements in flat panel displays, particularly the transition from rigid to flexible displays opens a plethora of new possibilities for disseminating information to the end user. What used to be magical concepts in electronic paper and foldable displays are now becoming reality. Display companies around the globe have been advancing the technology to produce viable flexible displays. The major differences arise from the base substrates used. Glass, silicon, and other rigid substrates have been used as the staple material for manufacturing display screens. However, moving from rigid substrates to more flexible platforms forces researchers to reinvent the wheel in the advent of fabricating flexible displays. From process temperatures to new substrate-handling methods, each fabrication step must now be redefined for the emerging flexible flat panel display technology.

Flexible flat panel displays have been defined as follows:

"A flat panel display constructed of thin substrates that can be bent, flexed,

conformed, or rolled to a radius of curvature of a few centimeters without losing functionality" [1].

To enable the concept of flexibility in flat panel displays, a substrate consisting of a polymer or thin glass is typically employed. Thin glass can be manufactured to thicknesses of $\approx$50 μm and thus, is light-weight with excellent barrier properties but is fragile, costly, and has insufficient mechanical flexibility [2]. Due to the restrictions in mechanical flexibility, electronic devices fabricated on these substrates are batch-produced and thus, lacks the ability to be integrated with roll-to-roll technology. Therefore, polymeric or plastic substrates are used for this purpose as such materials meet the required demands of flexible electronics.

The availability of high quality flexible electronic display technology such as, rollable displays and electronic paper are highly anticipated to appear on the market with great interest and resources devoted by manufacturers and researchers to make this a reality [3]. Some examples of new concepts include a portable rollable display, a display that spans the entire dashboard of a vehicle, and applications that can be worn on the arm similar to a wrist-watch. Flexible electronics would allow for devices that are thinner, lightweight, robust, conformable, and rollable based on current technologies in liquid crystal displays (LCD) [4], organic light emitting diode (OLED) displays [5], [6], electrophoretic displays [7], as well as radio frequency identification (RF-ID) tags [3]. Such advantages in flexible electronics would allow for easy portability, high-throughput manufacturing, displays integrated in clothing, and other extreme engineering designs [3], [6]. To extract such modern concepts, well thought-out and -engineered novel device circuitry for display screens on flexible media is critical.

1.1.1 Roll-to-roll technology

In addition to the sleek features that flexible substrates offer, the prospects of transferring entire manufacturing processes of displays to roll-to-roll technology can eliminate many issues related to batch processing of large surface areas approximately up to 3 m^2. These issues include labour intensive and time consuming processing of large area electronics, one-component supply chains, and high manufacturing costs [8]. Currently, batch processing on glass occurs in manufacturing large-area electronics such as television (TV) screens where active matrix (AM) backplanes are fabricated on glass. Roll-to-roll technology is similar to that of producing newspapers - printing the film on rolls to the desired patterns. For this approach, the film can be deposited followed by a photolithography step for patterning. Since the substrate is now flexible, all process steps can be done on a roll-to-roll web feed, allowing for fully automated sequences with no human involvement. The challenging task here is patterning and defining device features on the AM backplane with high precision, accuracy, and yield. Figure 1.1 shows the process steps of a roll-to-roll stream line for flexible electronics. Transferring the devices to a roll-to-roll web after manufacturing the backplanes on glass has also been under investigation [3] but, its effectiveness is debatable since more wastage in process materials is involved, leading to an increase in manufacturing costs.

Other issues with web processing that are yet to be overcome include the winding tension that may lead to scratches on the substrate and deformation if not handled properly. Thus, best practices for substrate handling during the fabrication of devices must be considered to ensure the uniformity of the substrate surface area is protected. Creativity along with innovation are needed to share advantages of

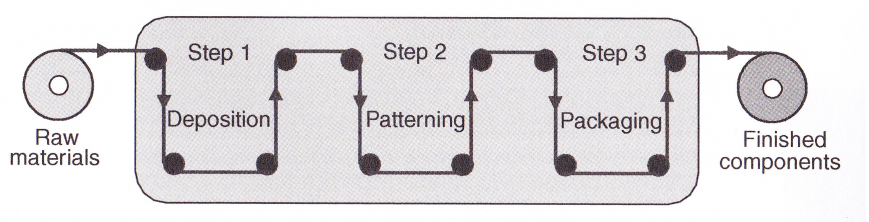


Figure 1.1: Roll-to-roll manufacturing process steps for electronics [3].

some of the substrate handling techniques followed in batch processing, including the attachment of the substrate to a rigid carrier during web processing to ensure the substrate surface is unhindered during fabrication. The ultimate goal of roll-to-roll technology is to create innovative equipment, process recipes and designs, and system integration with other tools involved in the fabrication of electronics on flexible substrates in order to produce high resolution and high throughput electronics that meet the tolerances achievable on rigid substrates.

1.1.2 Active Matrix Arrays

Figure 1.2a) shows a schematic of an active matrix (AM) display on a plastic substrate [4]. AM backplanes are used in LCDs and OLEDs for today's display screens. Contrary to its older alternative passive matrix arrays, AM arrays now control each pixel on its own, through the use of a thin-film transistor. As shown in Figure 1.2b) [9], information can be transferred to pixel circuits one row at a time using column drivers. Pixel circuits are application specific and thus, possess different circuitry. For example, LCD pixel circuitry uses thin-film transistors (TFT) to switch each pixel on and off at appropriate times. OLEDs on the other hand can use multiple TFTs to ensure pixel switching and necessary voltage are applied to the specific

pixel. This is shown in Figure 1.3.

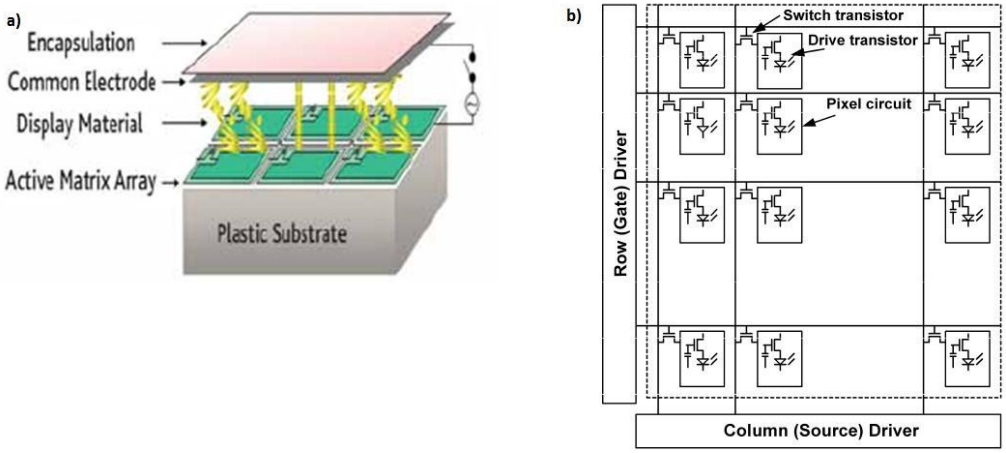


Figure 1.2: a) Schematic of an AM display fabricated on a plastic substrate [4] and b) schematic of an AM TFT array [9].

LCDs are voltage driven displays. Each pixel can be thought of as a capacitor since the liquid crystal itself sits between two transparent electrodes. When a row voltage turns on, the TFT switches on, which in turn allows for the data of the picture or video that must be displayed to be transferred. An additional capacitor helps in ensuring that the pixel stays in a stable voltage condition. The liquid crystal molecules can thus modulate the intensity of light entering from the backlight proportional to its voltage.

OLEDs on the other hand possess current driven pixel circuitry. Due to this factor, the voltage must be first converted into a current signal. An additional TFT can be used, as shown in Figure 1.3, for this purpose. In this case, when the row signal turns on, the switch TFT would also turn on as in the LCD, allowing the voltage of the data to be transferred to the capacitor, C_s. The data TFT would

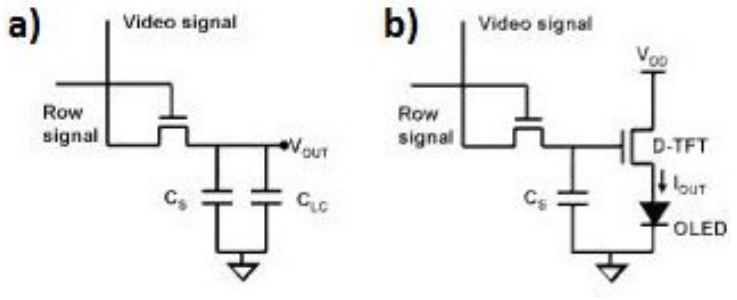


Figure 1.3: a) Pixel circuitry of LCDs and b) OLEDs [10].

convert the data voltage to an equivalent current, I_{out}. This current is proportional to the applied data, and consequently, to the generated light by the OLED pixel, which is what the end user views on the screen.

Figure 1.2a) shows a pixel depicting the concept of fill factor, displayed in green, within an AM array. The greater this fill factor becomes, the more visible would the displayed image be; in other words, the resolution of the display would increase. Increasing the fill factor in pixels for displays calls for the degradation of the space allocated for pixel circuitry. To do so, each component of the circuits shown in Figure 1.3 should decrease in size without compromising performance. This becomes particularly important to keep in mind when moving to flexible displays where TFTs with smaller dimensions must still be patterned accurately to form functional circuits.

The next section will discuss the type of low temperature TFTs that have been considered for flexible flat panel displays. Out of these, the section will provide details of the structure and type of TFT chosen to conduct our experiments.

1.1.3 Thin-film transistors (TFTs)

A vital component to enable flexible flat-panel displays in technologies such as OLEDs is the success in fabricating functional TFTs consisting of a high fill factor on plastic substrates. TFTs allow for both switching control of pixels and the appropriate voltage conversion to a current signal for technologies like OLED to provide the necessary intensity of the resultant colour displayed. Flexible electronics is a disruptive technology; its impact to society would become more apparent once it becomes pervasive [11]. Already composition of TFTs with different materials for their channel layers exist for flexible electronics. Table 1.1 below categorically illustrates four different types of materials used to fabricate TFTs and their attributes, which determine the characteristics of TFTs that are composed of them [12]. TFTs using a-Si and low temperature poly-Si on rigid silicon and glass substrates are mature technologies, primarily used for AM-LCDs but, also for image sensors and photovoltaics to power remote or portable electronics [11]. In addition, TFTs made of semiconducting organic materials are in various phases of development. The synergy between materials and device technologes will be a key driver in pushing flexible electronics into small and large scale applications with bright commercial prospects. This thesis will work with bottom-gated inverted-staggered lateral a-Si:H TFTs fabricated at low temperature (less than 150^0C). A schematic representation of the TFTs examined in this thesis is shown in Figure 1.4 (adopted from [13]).

A typical bottom-gated a-Si:H TFT would comprise of 5 masking steps stacked one on top of each other with each mask lending itself for pattern establishment on the film. In bottom-gated TFTs, the gate electrode is first direct-current (DC) sputter deposited and subsequently patterned (mask 1) following a trilayer deposition

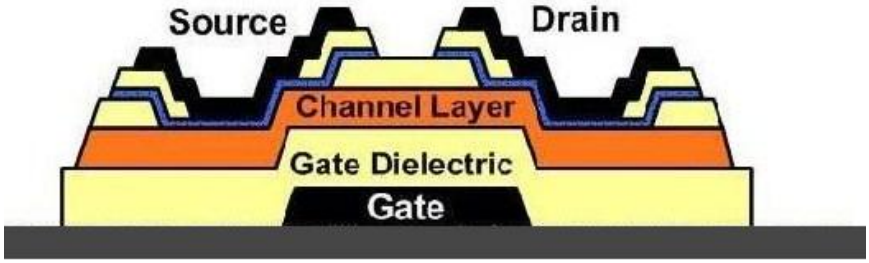


Figure 1.4: Cross-section of a lateral a-Si:H TFT. Adopted from [13].

of SiNx gate dielectric, a-Si:H channel region, and a SiNx passivation layer. The trilayer is deposited using a chemical vapour deposition (CVD) system such as the plasma enhanced chemical vapour deposition (PECVD) system. After source and drain contact regions are opened using the second mask, n^+ doped Si and SiNx thin-film are deposited using a PECVD. The n^+ regions are required to lower contact resistance between electrode and channel regions as well as provide a source of charge carriers for transport across the active region. SiNx regions are then isolated with another mask step (mask 3). Once vias of the source and drain regions are opened (mask 4), the last deposition and patterning (mask 5) of metal are completed for the source, drain, and gate contact pads. A source-drain overlap of approximately 10 μm is used in the fabrication of TFTs to ensure good transconductance and low resistance would affect TFT behaviour.

As listed in Table 1.1, a wide variety of TFTs can be fabricated based on different materials for their active channel regions. Amorphous (a-Si:H), nanocrystaline (nc-Si:H), and polycrystalline silicon (poly-Si) stem from silicon (Si), element #14 on the periodic table; it allows for already existing manufacturing infrastructure to be used and thus, eases the integration and interface quality of these materials with Si

Table 1.1: Materials that can be used to compose the active layer of TFTs [12].

Attribute	**a-Si:H**	nc-Si:H	poly-Si	organic
Mobility (μ)	**low**	greater than a-Si:H	high	low
Stability	**issue**	stable	stable	improving
V_t uniformity	**high**	high	improving	improving
Mobility uniformity	**high**	potentially high	improving	improving
Manufacturability	**mature**	new	new	has potential
Cost	**low**	low	high	potentially low
Flexible substrate	**promising**	uncertain	uncertain	promising

passivation and dielectric materials (eg. SiO_x and SiN_x) [14], [15]. A-Si:H possesses short range order. The range of order in the materials increases from nc-Si:H to poly-Si:H. Due to the high defect density and lack of long range order in a-Si:H, the material is considered of very poor quality, often trapping charge carriers and thus, degrading the overall mobility in devices while increasing the threshold voltage and subthreshold slopes in TFTs. From Table 1.1 we see that although nc-Si:H and poly-Si:H consist of higher mobility values and are more stable materials than a-Si:H, the latter has a mature manufacture life, which brings its associated costs also much lower than the former materials. Although a-Si:H is of poor quality, the quality stays uniform for large-area device fabrication, allowing for even 60 inch TV screens to appear on the market. Since high-uniformity a-Si:H materials can be fabricated, expected device performance of a-Si:H TFTs can be achieved based on modeling and simulations of such TFTs. These are the main reasons why a-Si:H materials are still used for large-area fabrication.

However, transferring the fabrication of TFTs onto flexible substrates is an in-

volving task comprising of several obstacles. Some of these obstacles include, dimensional instability of the flexible substrates during processing, proper substrate handling techniques that are required to minimize contamination of substrates as well as mechanical stress of films that would comply with the flexible materials used as they did with glass and silicon. These issues negatively contribute to the overlay alignment between successive mask layers in fabricating TFTs. Increasing the misalignment from one mask to another during the fabrication of TFTs could lead to high overlap capacitance in the devices. If this misalignment is large, non-functional TFTs can result. Thus, reducing the overlay misalignment during each fabrication step of TFTs is critical to ultimately produce well functioning devices. Reduction and better control of misalignment can also result in smaller feature sizes of TFTs, leading to a greater fill factor for each pixel of a display such as an AM-OLED. This control leads to higher resolution for pixels of AM-OLEDs and similar displays. Since the substrates are of flexible material, their built-in strain must be properly controlled from going inward (contracting) and outward (expanding) to reduce any overlay misalignment.

1.2 Research Motivation and Objective

The integration of electronic devices on flexible substrates lead to various new applications as well as the improvement of existing ones. Yet, flexible substrates can be easily distorted, which requires greater care to produce functioning electronics, increased functionality, and higher densities in multilayer devices and electronic systems. Additionally, the drive to lower costs has continued to place pressure on device fabrication for higher process yields. Improved layer-to-layer alignment has

been noted as a top priority requirement in industry [16]. Due to the significant number of advantages that flexible displays offer, a method of efficiently patterning and fabricating a-Si:H TFTs on flexible substrates is described in this thesis. More specifically, the focus will be on the accuracy of overlay alignment between successive mask layers during photolithography in fabricating a-Si:H TFTs on flexible substrates. Major challenges must be overcome in substrate handling as well as in the alignment and patterning process [17]. The process of precisely aligning multilayered electronic device structures and circuits on polymeric substrates for large-area electronics has been a daunting one due to the sensitive handling and processing of the flexible substrate compared to glass or silicon [4], [18]. For example, plastic substrates are more sensitive to thermal stress and are more likely to deform during thermal cycling. The purpose of this study is to understand these issues in order to obtain accurate overlay alignment of TFTs and bring about a more controlled, novel and robust technique to overcome these issues in fabricating a-Si:H TFTs on flexible substrates.

1.3 Structure of Thesis

Background information regarding the study of interest in this thesis is addressed in Chapter 2. The chapter looks at the properties of flexible substrates that have been considered in research for TFT fabrication such as dimensional stability as well as properties of the other materials used to reduce overlay misalignment on flexible substrates in this thesis project. The chapter also summarizes previous work in reducing the misalignment of TFTs on flexible substrates. Chapter 3 details the experimental work carried out in fabricating TFTs on flexible substrates. Fabrication

of the TFTs and processing done to attach and detach the laminated substrates before and after fabrication, respectively, are described. Chapter 4 discusses the results obtained for overlay misalignment and the final TFT characteristics. Misalignment has been compared with results obtained for previously fabricated batches of TFTs on free-standing substrates. Final analyses in terms of uniformity, effectiveness in reducing misalignment, increasing throughput, and ease of wafer handling of each method are provided in this chapter. TFT characteristics further show the uniformity and stability of the TFTs on laminated substrates. Chapter 5 concludes this thesis by summarizing the research contribution with the proposal of future work related to the topic considered herein.

Chapter 2

Materials limitations and challenges in existing technologies

2.1 Introduction

This chapter provides an overview of the materials that have been used for the implementation of a low-overlay misalignment fabrication process of a-Si:H TFTs in this thesis and the analysis of their properties. Following substrate analysis, a literature review of misalignment reduction techniques that have been developed will also be discussed.

2.2 Substrate analysis

Plastic substrates that are used to fabricate AM backplanes of flat panel displays ideally offer the properties of glass substrates [19]. Choosing the most suitable sub-

strate is heavily dependent on the thin-film deposited and process conditions. This is to ensure that the substrate can withstand process conditions as well as retain its composition without contaminating external surfaces. Some critical properties include transparency, chemical and moisture resistance, dimensional and thermal stability, a low coefficient of thermal expansion (CTE) coupled with a smooth surface. Cost-effective processing in high volumes to allow for the emergence of roll-to-roll technology is another criterion. However, no plastic has been able to provide all these properties and criteria for large-area display fabrication. In the meantime, alternate methods and processes can be used to make up for some of these missing properties to fabricate efficient and effective AM displays.

The plastic substrate used for backplane fabrication in this thesis is 125 μm thick, thermally-treated poly(ethylene naphthalene 2,6 dicarboxylate) (PEN), which is bi-axially oriented and semi-crystalline in nature. PEN is prepared by a process whereby the amorphous cast is drawn in the machine direction and the transverse direction of the substrate, which is then heat set to crystallize the film [3]. The polyester material provides high dimensional stability minimizing substrate warpage with a CTE of approximately 27 ppm/^{O}C [1] at 150^{O}C, a moisture pickup of 0.15%, good solvent resistance, a total light transmittance or clarity of 87% [20] through its entire sheet thickness, and a surface roughness of 0.8 nm, lending a smooth surface for TFT fabrication. As such, PEN is an attractive candidate for flexible AM displays [21]. Furthermore, moisture absorption is detrimental to dimensional stability since it can further distort the film leading to uneven shrinkage or expansion on some areas of the material, and thus require special adaptations for overlay alignment. PEN however, possesses a high hydrolysis resistance; for example, in a

[1] A 20 ppm error corresponds to a 2 μm shift over 100 nm [16].

recent study, 90% of its tensile strength had been retained after placing the PEN in a 90^{O}C bath for 1680 hours [21].

Figure 2.1 shows the molecular structure of PEN and polyethylene terephthalate (PET) [22]. Comparing PEN with its sister polyester film PET, PET consists of 1 phenyl ring as opposed to 2 as in PEN. The phenyl ring of PEN has little effect on its melting point (T_m), which is 263 ^{O}C but, increases the glass transition temperature (T_g) of PEN by several degrees Centigrade, making it more temperature resistant; by comparison, the T_g of PET is 80^{O}C while T_g of PEN is 155^{O}C [21]. T_g is the highest continuous temperature at which the polymer would survive under without changing from a rigid glass to a rubber melt. PEN comprises of almost 50 wt% of mosaic crystallites. Because of this semicrystalline nature, PEN consists of both T_m and T_g, affecting its crystalline and amorphous sectors, respectively. The increase in T_g allows for TFT processing to occur relatively close to such elevated temperatures where chemical reactions at the molecular level could occur with thermal assistance without having adverse effects such as melting of the substrate. This can assist together with RF power to lower the stress in a film deposited, for example, by a PECVD [23]. In addition, a-Si:H TFTs fabricated at elevated temperatures demonstrate increased stability possessing a decreased threshold voltage shift [15]. In contrast, several other materials that have been used in industry, such as PET, are composed of oligomers, which tend to surface quickly closer to its T_g, making it difficult to fabricate devices on such substrates. In addition, thin-film possessing a CTE $\leq$ 20 ppm/^{O}C is desirable to ensure low thermal mismatch such that the film attached to the PEN undegoes low strain and cracking under thermal cycling [19].

Dimensional stability is another critical feature to ensure accurate registration of the multi-layered TFTs and a high throughput of uniform and functional de-

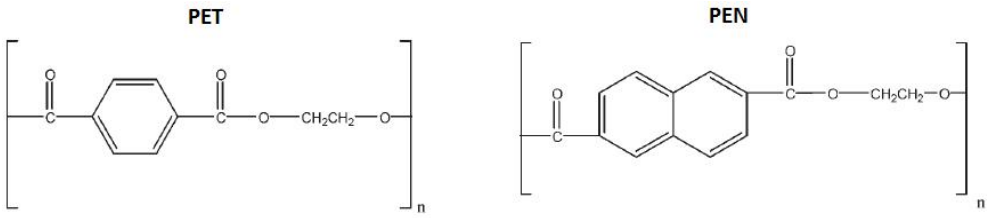


Figure 2.1: Molecular structure of PET and PEN [22].

vices are fabricated on the PEN substrate. This feature depends on two factors - the CTE and the residual stresses during processing [24]. Due to film manufacturing conditions, the substrate undergoes undesirable change in its dimensions at elevated temperatures, from mechanical stresses during handling, and changes in surface material compositions [21], [16]. At temperatures close to T_g, mobility of the PEN's polymer chains increase, allowing for shrinkage or expansion of the substrate to occur. The shrinkage of a film is measured by the change of direction in a given axis before and after the thermal cycle. Therefore, processing temperatures must retreat to at least a few Centigrade below the substrate's T_g to reduce the impact of molecular relaxation, which occurs mainly in noncrystalline regions of the substrate [25]. Running a thermal pretreatment prior to fabrication has shown to reduce the dimensional change on the substrate as shown in Figure 2.2 [21]. This method is now used as an additional processing step for PEN [3]. Here, the internal strain of the film is relaxed by exposure to elevated temperatures all under minimum line tension. Thermally treated PEN shrinks in the order of $\leq 0.1\%$ at high temperatures, lending good dimensional stability and reproducibility characteristics up to 200^{O}C [3]. Thus, PEN substrates are considered dimensionally predictable substrates below the temperatures at which they have been heat stabilised.

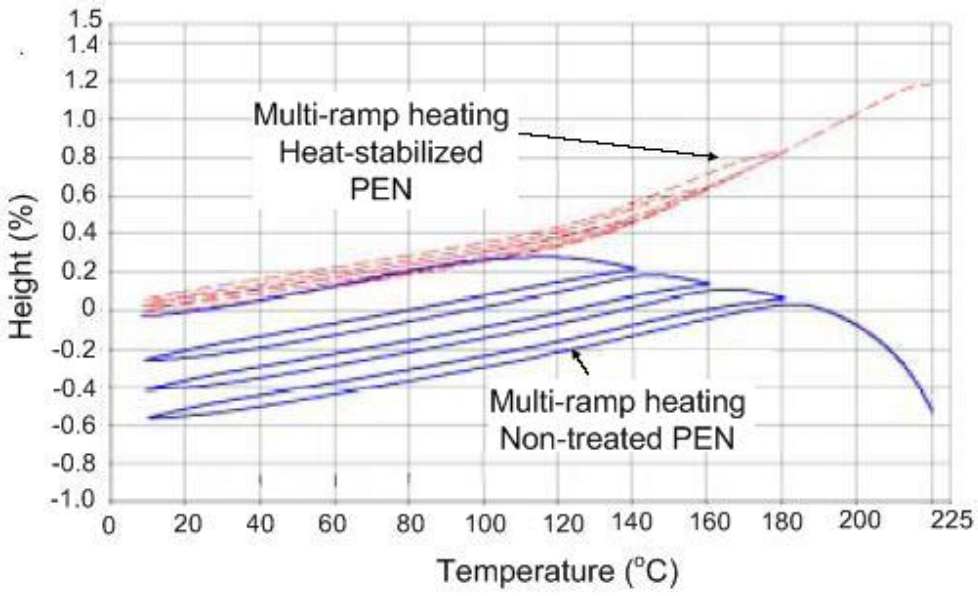


Figure 2.2: Dimensional stability of pretreated vs. non-treated PEN films. Adopted from [21].

At elevated temperatures, PEN decreases in stiffness. Thus, any small amount of stress applied to the substrate at higher temperatures can strain the substrate, causing dimensional instability upon reheating. Thermal mismatch strain is given by the CTE mismatch between substrate and film. Rigidity can be exploited to reduce the stress in the material as shown in Equation 2.1, where rigidity, R, is proportional to the thickness, t, of the substrate. Here, ν is Poisson's ratio, and E is the elastic modulus ($\sim$6.1 GPa for PEN), amounting to a rigidity of 15x10^{-4} Nm. Comparatively, E of the thin-film structure is $\sim$200 GPa [26] but, because the thin-film TFT structure is much thinner than the substrate thickness, the mechanical strengths are comparable, affecting each other's strain and thereby, resulting in the substrate to curve if processed free-standing. The naphthalene group in PEN is what

contributes to rigid macromolecular chains and thus, superior mechanical properties than phenylene groups, as seen in PET [27]. Rigidity has also been used to reduce distortion in the substrate [25]. This property becomes particularly important in the delamination step after device processing when the PEN is removed from its rigid carrier. Ensuring removal from the rigid carrier without stressing the fabricated TFTs on PEN is critical. The development of debondable adhesives are currently being researched for this purpose [25].

$$R = \frac{Et^3}{12(1-\nu)} \tag{2.1}$$

It has been suggested that the PEN film should be equilibrated prior to establishing registration of alignment in subsequent layers [25]. However, the definition of equilibrium in a processed PEN and when this is reached are factors that are currently unknown. In the meantime, thicker substrates are being exploited due to easier handling using equipment designed for glass substrates.

Several alternative plastics ranging from amorphous solvents cast to thermoplastic crystalline exist for the production of electronic devices. A detailed study of each of these materials is out of the scope of this thesis. However, it is noted that from recent literature, one of the more popular materials used for the backplanes of AM circuitry is polyimide film. Properties of this film is exceptional with T_g ranging from -269^{O}C to 400^{O}C, a Poisson's ratio of 0.34, and a CTE of 35 ppm/^{O}C at 150^{O}C [24]. However, the leading issue is that the film is yellow in colour, which leads to clarity issues and in general, a yellow display. To exploite the advantages of polyimide film without the yellow colour of the film affecting our work, the underlayer used in the lamination process is polyimide while the TFTs have been fabricated

Table 2.1: Properties of materials used for lamination process

Properties	**PDMS**	**PEN**	**Polyimide**	**Glass**
Thickness	1.5 mils	125 um	1 mils	2mm
Elastic modulus (Pa)	3.00E+08	6.10E+09	3.20E+09	7.20E+10
CTE	300	25	5.5E-5	31.8E-7
Glass transition temperature (^{O}C)	-125	155	$\geq$400	600

on the overlying PEN.

It is noteworthy to understand the properties of polydimethylsiloxane (PDMS or silicone) and Kapton at this moment. Both of these materials are used as our mechanism of attaching the PEN susbtrate to its rigid carrier. Table 2.1 shows the properties of all materials used in the lamination process. Silicone is used in several lithography techniques such as for phase-shift masks in creating 3D patterns and as the mold in nano-imprint lithography [28]. Soft PDMS, which is what has been used in lamination techniques, contains a soft nanostructure and is more likely to deform under thermal pressure, which is evident by its large CTE. However, the polyimide film that carries the silicone adhesive on its two sides as mentioned earlier in this chapter, possesses a high T_g and other glass-like properties. Therefore, the polyimide's influence on the PEN to deformation is minimal, similar to that of glass.

One of the key advantages of implementing this attachment scheme is that a curing step can be avoided during lamination and subsequent cross-linking during delamination, thereby reducing the thermal change that the substrates experience. Maintaining low thermal cycles in this regard can significantly reduce the amount of cracks and strain induced to the substrate and thin-film.

2.3 Overlay Registration and Misalignment

One of the biggest and most difficult issues in fabricating devices of stacked layers is having proper film registration or overlay alignment between successive mask layers [23]. The issue is seen in more compliant plastic substrates since they possess a higher dimensional change occurring at elevated temperatures, an increased CTE, and lower elastic moduli than conventional glass substrates. Thus, when a stiff thin film is deposited on a compliant plastic like PEN, the dimensions of the PEN tend to change. The impact of this issue is so serious that it can make or break the device i.e. allow for a functional or non-functional devices to be made. Furthermore, it can lead to device irregularities such as overlap capacitance at the source-gate and drain-gate regions of the channel and a shift in threshold voltage, resulting in early device breakdown. Therefore, it is imperative that the issue pertaining to overlay registration gets addressed. A technique that uses existing processing infrastructure to automatically identify the misalignment between each mask layer and thereby, adjust it accordingly without hindering the device, its electrical characteristics, or the substrate is ideal. Currently, such a system does not exist. Nevertheless, several techniques have been implemented to satisfy overlay alignment between successive mask layers of devices. Of them, the most popular ones are discussed in the next section of this chapter.

2.3.1 Existing techniques for overlay alignment

Self alignment

Self-alignment of TFTs existed since the early 80s [29] yet, the TFTs experimented with were fabricated on rigid substrates like glass. Partially self-aligned TFTs are achieved by defining the top nitride by back ultra-violet (UV) exposure. To produce low contact resistance glass, source, and drain contacts have been formed by ion implantation and silicidation [30]. However, the gate electrode along with source and drain contacts would still be defined using a total of 5 photolithography masks (or 4 with a liftoff step in place of the last metal contact formation [31]) with 1 self-alignment step, making the fabrication only a partial self-alignment process to date. This self-alignment process nevertheless, reduces the parasitic capacitance by decreasing the required source-gate and drain-gate overlaps to some extent with the hopes of eliminating this issue with a fully self-aligned process [30]. Output characteristics with no current crowding have been achieved, suggesting a good contact with low field injection using ion implantation through silicidation [30]. In addition, the mobility and threshold voltage show low distribution over a large glass substrate area. Self-aligned TFTs may be produced on glass substrates where shrinkage and alignment problems are minimum [30]. To produce high performance self-aligned TFTs, an ion shower doping step and an extra data-alignment photolithography step have been incorporated. Although a minimum channel length can be determined using the ion shower doping step, such technologies have not been used in AM-LCD or AM-OLED manufacturing and is not commercially available for very large area fabrication [32]. The extra data-alignment photolithography step avoids the ion-shower doping step while increasing performance of a tri-layer device; how-

ever, it involves an additional step to define the contact regions of the TFT. This results in the minimum channel length to be a factor of the gate dimension, the contact region alignment tolerance (overlap), and the minimum spacing of the contact photolithography [32].

Exposing the backside of the glass substrate in 2 separate occasions to UV light has been discussed to create self-aligned bottom-gated TFTs [32]. In addition to the top SiN passivation layer being patterned using the bottom-gate as the mask, the second UV exposure is used to define the contact regions while a mask is used in the same exposure to define the channel. Contact overlaps less than 1 μm can be obtained using this method while ohmic contacts and output currents of $\sim 10^{-5}$A have been achieved [32]. This procedure is yet to be researched on flexible substrates.

Fully self-aligned TFTs are yet to be proven for flexible substrates although, partial self-alignment on flexible substrates has been demonstrated with satisfactory TFT behaviour only by bonding the plastic substrate to a rigid glass plate during photolithography [33]. Here too, the process still depends on approximately 4 masks and 1 self-alignment step to function [34]. The advantage of self-aligned bottom-gated TFTs is that the source and drain electrodes minimize feedthrough capacitance to the gate by not requiring any overlap between the electrodes with the gate. This inherently facilitates the fabrication of short channel TFTs [35] that are used in high performance circuits [31]. Low and uniform capacitance in an AM-pixel array also helps in minimizing the kick-back voltage of the TFT while reducing image retention, which would undoubtedly improve display quality.

However, many limitations exist in this patterning process. The fabrication process is complex, requiring new and additional processing techniques than the standard back-channel etch process [31], [33], [30], [36]. Another key concern in

implementing this technique is that self-alignment still depends on standard photolithography infrastructure to function; thus, it makes little sense to completely invest and incorporate on such a new technology that requires already established techniques in addition to know-how of successfully implementing the technique. In addition, not using tapered film for the SiN_x passivation layer can result in stability issues overtime as well as requiring better techniques in etching the film when creating source and drain regions [37]. Because the use of masks are still a requirement for patterning in self-alignment, the throughput on flexible substrates is of concern and to date, have not been confirmed. This key concern stems from the fact that due to the nature of the substrate under thermal deposition, it is likely to deform resulting in varying channel length TFTs. In such a scenario, it would be difficult, if not impossible, to determine the actual channel dimensions and device feature size. Due to substrate distortions, varying dimensions of TFTs can result in the fabrication process of an AM display.

Digital lithography

Digital lithography is another technique that has risen for thin-film patterning [38]. The first demonstration of printed etch masks for a-Si:H TFTs presented feature sizes of $\approx$100 μm [39]. From thereon, the technique has been enhanced to allow for fine feature sized device fabrication to cater to display and imager arrays. This technique uses ink-jet printing in place of photolithography to achieve pattern generation and layer to layer registration of device features. An advantage of digital lithography is that alignment of the mask layer can be corrected through image processing prior to patterning the substrate [40]. First, the substrate is aligned in approximately the same orientation of the previously patterned layer. With the help

of alignment marks, the mask layer is digitally repositioned and aligned to fit the substrate prior to printing the device. This technique minimizes the need for special optics, back-exposures of the substrate, or physical adjustments to the fabrication of the TFTs. The real-time digital compensation of the mask for substrate distortion in this way is especially handy for flexible substrates. Figure 2.3 illustrates an array of digitally aligned TFTs with jet-printed etch resist [40]. Three masks were used to pattern the gate electrode, active device island, and source-drain metal electrodes.

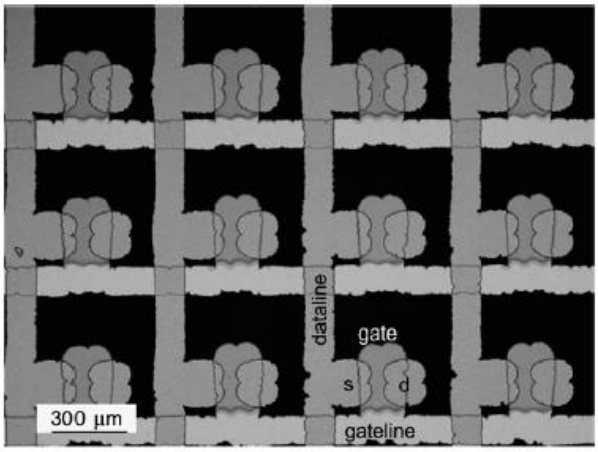


Figure 2.3: Array of TFTs fabricated by digital lithography [40].

Electrical characteristics have shown satisfactory results yet, several shortcomings exist. One of the biggest bottlenecks of digital lithography is that it requires much time to ensure alignment between the mask and substrate is satisfied. Assessing devices for alignment one at a time is not economically feasible and is cumbersome for backplane array processing of displays. Furthermore, since pattern generation and layer registration is achieved through digital ink-jet printing, the speed of processing substrates are limited by the effectiveness of the nozzlehead used, num-

ber of nozzleheads used, and their efficiency. In addition, although fine features of ≈20 μm have been reported [39], the ejection of small drop volumes must be well controlled to ensure proper volumes and drop diameters can be formed. Nevertheless, the process is still too novel, requiring industries to acquire new infrastructure and know-how in processing the substrates. Notwithstanding these issues, results of digitally aligned devices show a layer-to-layer registration of ≈5 μm over 4 inch substrates [40]. Others have shown alignment ensuring overlay accuracy of +/-2.5 μm [16].

Stress compensation

This technique identifies the built-in stress during fabrication of a-Si:H TFTs to ensure reduced overlay misalignment between successive thin-film layers. Built-in stress occurs from deposited atoms lying in non-equilibrium positions, leading to a dependency between the interacting material and deposition conditions [26]. The easiest and most effective method to obtain a change in stress for the entire bottom-gated TFT structure has been by changing the RF power of the SiNx gate dielectric, although a high power for the gate dielectric ensures electrical stability [23], [6], [41]. Thus, it has been customary to tweak, control, and monitor dielectric behaviour to engineer stability of the device and excessive stress for peel-off and film fracture prevention to the thin-film layers of the TFT. The goal in stress compensation is to maintain the size of the circuit on substrate at a constant value by compensating stress of the SiNx gate dielectric and keeping the substrate flat [26]. Built-in strain has been able to change the substrate orientation from tensile to compressive by increasing the RF power of the SiNx gate dielectric. Although the exact value in misalignment reduction was not published, Cheng et. al have been able to minimize

overlay misalignment in structures where the RF power was maintained at 12 W and 20 W [26]. Using a buffer layer on both sides of the flexible substrate can also help act as a mechanism to compensate for stress by adding more of the opposite stress requirement. For example, if the structure generates more tension to the substrate, a buffer SiNx layer can be added under the TFT to generate a compressive device structure. By adjusting the stress in the thin-film accordingly, the curvature of the substrate is minimized, thus resulting in less overlay misalignment between successive layers.

This technique also consists of several limitations. Although stress compensation works for standard device fabrication, changing recipes for specific demands or device fabrication requirements can make the stress in each layer vary and thereby, create devices with high overlay misalignment. Thus, the solution to misalignment does not terminate for all device-specific fabrication processes but, only a small window of device fabrication processes that can follow such thin-film recipes. The technique is limited in effectiveness given that the substrate changes may not be symmetric and can result in both tensile and compressive orientations. Additionally, by compensating for stress by adding more thin-film to the stacked layers increases the total thickness of the sample, making the sample less flexible for rollable applications. Furthermore, maintaining a free-standing substrate at a constant orientation throughout all photolithographic stages with no physical assistance such as a tape or lamination process is difficult with the possibility of producing creases and cracks in the layers during the fabrication process. Thus, due to excessive care required during fabrication, this process would be difficult to control for large-area a-Si:H TFT fabrication.

Lamination

To solve the physical dimension issues related to fabrication of TFTs on flexible substrates, a solution must arise at the physical level. Previously, critical feature sizes of TFTs fabricated on PEN have been limited by the dimensional stability of the substrate during device fabrication [5]. Lamination entails the bonding of flexible substrates to rigid carriers throughout the fabrication of devices to improve dimensional stability [26]. However, an adhesive would need to: (1) sufficiently bond substrate and the rigid carrier together throughout the process, (2) minimize outgasing of adhesives inside vacuum chambers, (3) resist process chemicals from entering the laminated sample, (4) prevent substrate curvature due to thermal and humidity exposure, and (5) be easily delaminated at the end of the process in order for this technique to be labelled as successful. It has also been noted that the adhesive(s) used can impose a ceiling on the maximum temperature for processing, which is lower than the highest working temperature of the chosen substrate material [42]. This requirement can severely degrade processing as well as ultimate device performance. In one process that used lamination, the fabrication had been kept at 105^{O}C in order to maintain adhesion [43]. Here, laser crystallization was used to recrystallize poly-Si thin-films on the flexible substrate. To protect the substrate from laser processing, a quarter-wavelength stack layer had been deposited between the laser processed film and the substrate. Delamination has been successful only in a remote forming gas plasma at 320^{O}C [43]. To withstand the high temperature, polyimide flexible substrates have been used in this process resulting in devices with good electrical characteristics. Another lamination process used temperatures up to 180^{O}C while limiting the distortion of its flexible substrates during processing in order to alleviate misalignment [5].

To solve the issues discussed, lamination has been considered for sometime [3], [25], [18], primarily because, the mechanical issues dominating flexible substrate device processing can be directly addressed at the physical level. In fact, the distortion of the substrate has been reduced to the point where the same design rules can now be used regardless of the chosen substrate material. Rather than reinventing the wheel for thin-film device fabrication on flexible substrates like in previously mentioned techniques, lamination can tackle dimensional stability, uniformity, and reproducibility while using standard photolithography to produce fine feature sizes and resolution for TFT fabrication on flexible substrates. This approach provides a solution to each of the above described issues using a novel yet, simple and cost effective manner that can be integrated with current and future roll-to-roll technologies.

Chapter 3

Experimental setup and Fabrication of TFTs

3.1 Introduction

This chapter discusses the process steps taken to fabricate bottom-gated inverted-staggered a-Si:H TFTs. The underlayers and mechanism used to prepare the substrate for the low temperature fabrication process are discussed. The fabrication of TFTs have been monitored closely to evaluate the overlay misalignment caused between successive mask layers and processing steps in the fabrication of the devices. Lastly, delamination of the substrate from the underlayers used during the fabrication process is discussed in this chapter.

3.2 Laminated TFT fabrication

To reduce misalignment that occurs between successive mask layers that are used for TFT fabrication, a lamination process has been established. Lamination is not a novel method. However, an important criteria requires the materials used, to ensure proper lamination for dimensional stability and reproducibility, be commercial products that can be readily obtained. The novelty of this process is in choosing such products to ensure misalignment is minimized while reducing outgassing, contamination during thin-film deposition, residual stress to deposited thin-film and strain to the substrate, and delamination of the substrate with a process below the materials' maximum workable temperature (T_g).

3.2.1 Sample preparation

Each substrate had been prepared in order to withstand thermal stress as well as air bubble formation under the PEN flexible substrate while ensuring minimized residue contamination from each of the processing steps. It has been hypothesized that implementing a lamination technique would overcome such issues to the PEN substrate and thereby reduce the overlay misalignment achieved between successive mask layers upon TFT fabrication. This lamination technique attaches the PEN flexible substrate to a rigid glass carrier of the same shape and size. Movement of the PEN substrate becomes restricted due to the attachment to the glass carrier and thereby, reduce the natural deformation that may otherwise occur during processing.

The lamination process that we have proposed uses a heat resistant silicone adhesive to paste the PEN substrate to the rigid carrier. This material was chosen as

the laminator since it is a commercially available double-sided Kapton/polyimide tape, where both sides of the polyimide film possess the silicone adhesive. Only about 1.5 mils of silicone is attached to the polyimide film, thus making the delamination process, which will be discussed later in this chapter, much faster and easier. Nevertheless, careful attention must be placed into attaching each of the materials. Air bubbles under the PEN substrate and polyimide tape must be nonexistant since they can reduce the bonding strength of the interface. Bubbles that exist under microstructures will cause failures of the device functionality [44]. This problem would be more severe for large area fabrication of devices. A mechanism was tested to reduce such air bubbles that could appear when attaching the materials together. Samples that were placed in a vacuum chamber at approximately 145^0C for approximately 48 hours had a decrease in air bubbles. After 2 weeks, all air bubbles that once existed under the PEN and polyimide tape had vacated. The drop in air bubbles is most likely a consequence of the increased temperature and high vacuum environment, whereby the suction of air was large enough to remove the air bubbles from the samples while the interactions between film materials were large enough to form well-laminated samples. Another factor that must be considered in attaching PEN to polyimide and polyimide to the rigid glass carrier is surface cleanliness. This clean surface is an essential requirement for obtaining reliable bonding of films [45]. The surfaces of each material can collect residue and other contaminants due to poor wafer handling techniques employed. Such contaminants would hinder bonding interactions at areas surrounding the particles. As a result, thin films that are later deposited to form TFTs would detach more easily from the substrate since there is no mechanical support to hold them to the substrate. This would degrade final yield of functional devices. Thus, surfaces have

been thoroughly cleansened using an RCA I bath to remove organic contaminants on both glass carriers and PEN substrates. Final blow drying was used to remove dust particles and any other macroscopic particles on the substrate surface.

Since the chosen tape is of polyimide material, the lamination process can withstand upto approximately 400^0C without any adverse effects [24]. The polyimide would shrink only upto 1.25% when kept for 2 hours at this temperature; after 30 minutes at 150^0C, the shrinkage is no more than 0.03% [24], making the polyimide tape a suitable candidate for attaching onto the PEN substrate. Figure 3.1 illustrates the procedure of lamination that has been implemented.

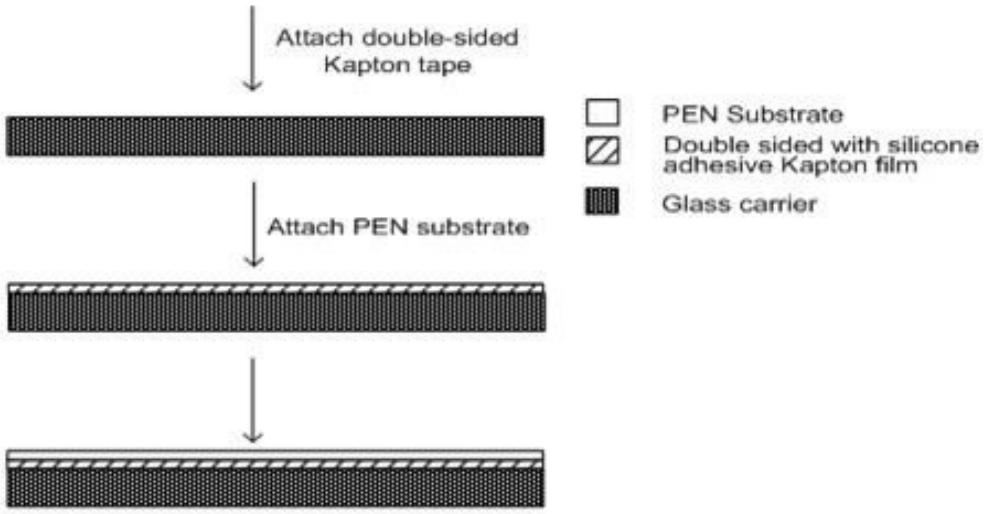


Figure 3.1: Procedure to attach plastic on rigid carrier.

Since this adhesive comes as a roll of tape, the technique can be easily incorporated to roll-to-roll technology. Roll-to-roll technology shows significant manufacturing advantages, of which some are high throughput and reduced turnaround time of very large area fabrication of devices. Figure 3.2 shows a schematic of a

roll-to-roll technology that uses UV exposure for lithography. This figure depicts the system type that can be integrated with TFT processing using the proposed lamination technique to ensure layer-to-layer alignment of the TFTs.

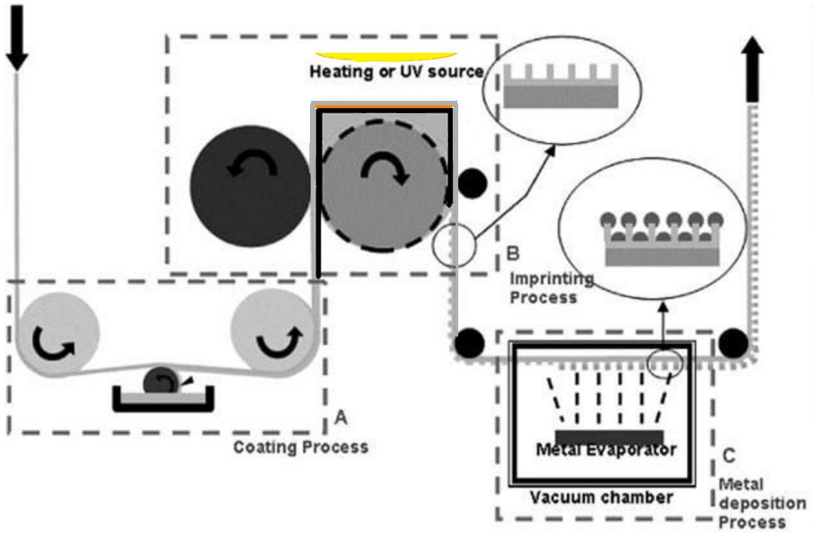


Figure 3.2: Schematic of a roll-to-roll processor that uses UV exposure for mask patterning onto the substrate [28].

Attention should be paid at the centre of the system where the substrate sits flat on the stage under the UV lamp ready for photolithography. To determine the difference that the laminated substrates would yield in overlay misalignment, a batch of TFTs on flexible substrates that were not laminated and instead free-standing have been fabricated using the same fabrication scheme. The free-standing batch of substrates are to act as a reference for further analysis of the effectiveness of our proposed lamination technique. The rigid carriers used have been Corning glass silica; this substrate would ensure consistency between both experiments with the only varying parameter being the lamination versus free-standing processes. Free-standing substrates have been temporarily attached to oxidized rigid carriers using

water as the acting element between the two materials only for each photolithography step involved in fabricating the TFTs. This oxidation process improves the hydrophilic behaviour of the glass surfaces [46], allowing water to be used to temporarily bond the substrates to the rigid carriers. The substrate stays attached for the duration of the lithography step.

A 300 nm thick a-SiN_x:H layer has been deposited via a PECVD at a RF of 13.56 MHz to the top surface of the PEN substrate. This buffer layer serves for multiple purposes:

- Strong barrier against moisture absorption and particle adsorption
- Substrate protection against process chemicals
- Substrate degassing protection to vacuum and chamber walls
- Provide reliable adhesion for subsequent thin-film deposition
- Reduction of thermally induced strain

The above bulleted items are some of the main advantages of using a buffer layer between the PEN substrate and the TFT comprised thin-film. In practice, the mismatch strain due to moisture can be minimized by depositing an inorganic barrier such as SiNx on both faces of the organic polymer substrate [6]. This is to dramatically slow down moisture uptake by the polymer substrate. Here, only the front surface of the PEN substrate had been treated with a SiNx layer as the bottom surface is attached to the polyimide tape and thereby, is protected against foreign particles and degassing to ambient surfaces. Moisture to the substrate surfaces occurs during RCA 1 cleaning, photoresist spin-cast, developing and stripping,

acetone and isopropyl (IPA) cleaning as well as toluene cleaning. Sealing the substrate against contamination from moisture absorption, chemicals, and other foreign agents as well as preventing degassing of the substrate itself allow for the separation of the substrate constituents from other particles. The contaminant- and moisture-free surface allows for the thin-film deposition to be less prone to cracking, which is essential for a high yield of devices. In addition, the a-SiN_x:H buffer layer has been used to control and thereby compensate for the stress exerted from each thin-film of the TFT during film growth [42]. This would effectively keep the strain of the substrate below a critical value (1% for TFT materials) and also reduce the mismatch strain caused by moisture [41]. Such advantages allow for more reliable and high throughput fabrication processes of a-Si:H TFTs to occur. Protection of this kind is particularly important for OLED devices. Oxygen and water penetration can result in having functional issues with such devices that depend on the charge movement and recombination for photon generation. Furthermore, when the substrate is in tension, the films tend to degenerate by crack propagation from pre-existing defects. In compression, a-Si:H degrades by delamination and buckling and fracture. To reduce these issues, the film must be made to adhere well. Additionally, the CTE of PEN is about 1 order of magnitude higher than that of the nitride, which can in turn assist in reducing the thermally induced strain in the film. Therefore, since SiNx forms a better interface with the subsequently deposited molybdenum than the polyimide film, SiNx has been utilised to support all these needs.

3.2.2 Fabrication process

All sputtering and deposition steps must occur below 150^0C, which is approximately the glass transistion temperature of PEN foils. This temperature was chosen as the highest process temperature, which is a compromise between obtaining satisfactory device performance and minimising excessive CTE mismatch between the TFT thin-film stack and PEN substrate. To ensure satisfactory material quality would be granted at this temperature, material characterization was carried out on silicon and glass 'dummy' substrates prior to fabrication using a PECVD system. The colour of the deposition and texture can be observed to determine expected and consistent quality of a-Si:H and SiNx thin-film. A light yellow colour of a-Si:H was uniformly deposited over the glass substrate while a blue thin-film was deposited for SiNx. This colour of SiNx varies depending on its thickness deposited and thus, a standard chart has been used as reference [47] to verify correct thickness deposition of the thin-film. A more comprehensive study of the built-in stress of the films are discussed in Chapter 4 of this thesis. Furthermore, the SiNx thin-film were also evaluated for strain induced to the substrates and weight of the thin-film. For this purpose, strain of the silicon substrate was measured before and after deposition with the difference taken as the additional strain caused by the thin-film. The Ionic Systems stress-gauge used in this process measures the deflection of the substrate using the distance travelled by a ray of light from a light source to the substrate and back to the light source. The ray of light approaches the substrate from the back-side of the wafer (i.e. side with no thin-film) as shown in the schematic in Figure 3.3. The smaller the distance, the higher the deflection towards a tensile film stress would be; by using this information, the strain on the substrate can be calculated. No optimizations were carried out in our analysis

but, measurements were taken to ensure that the thin-film used would produce acceptable and repeatable characteristics on the deposited substrates. To ensure consistency of deposited thin-film, the weight of the 300 nm film were also taken, before and after deposition. Before deposition, the glass substrates amounted to an average of 5.777886 g; after deposition, this measurement resulted in 5.780587. From this, the actual SiNx thin-film weight is on average 2.7 mg.

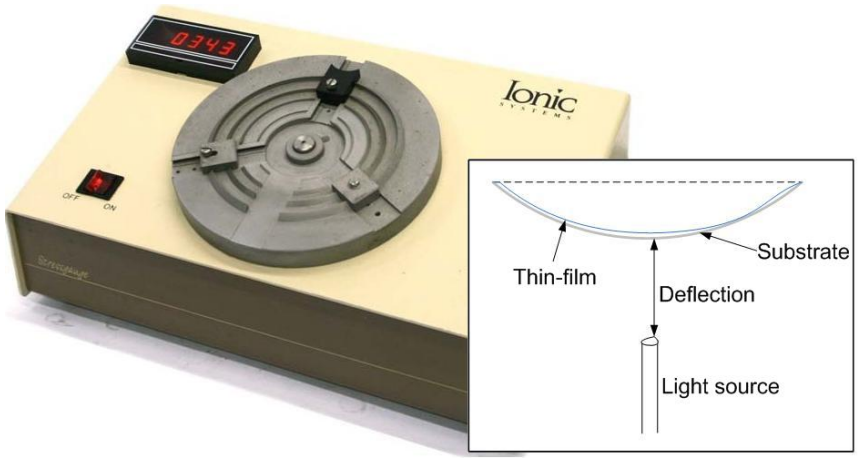


Figure 3.3: Stress-gauge and measurement schematic.

After preparing the substrate as discussed in Section 3.2.2 of this thesis, fabrication of a-Si:H TFTs on the prepared substrates commenced. Figure 3.4 shows the process steps taken for a-Si:H TFT fabrication. The fabrication process incorporates careful attention to wafer handling to ensure minimum contamination from residue on the samples. It was noted that handling the laminated samples was much easier than the free-standing ones. This was because, the rigid sample would disallow itself from being subject to bending during the processing steps while 100 nm of Molybdenum (Mo) metal is sputtered onto the a-SiN$_x$ buffer layer as the bottom gate metal for the TFT. It was noticed that the sputtered Mo can consist

of pinholes if the substrate contains residue on its surface [48]. Proper cleaning of the substrate surface can mitigate these issues. However, if the problem persists, then the Mo target in the sputtering system must be replaced as this may suggest a low amount of target material. The substrates complete a spin-coating of hexa-methyl-di-siloxane (HMDS) followed by positive photoresist (PR), which are uniformly applied on the sample surface for optical lithography under UV exposure. Subsequently, a-Si:H TFT fabrication occurs as described in Chapter 1.1.3 of this thesis. The source-drain to gate electrode overlap has been set to 10 μm to provide tolerance against change in substrate dimensions between patterning of the gate metal and the source-drain contacts. The UV exposure during lithographic patterning is instrumental in cross-linking chemical bonds in the long chain molecules of PR to ensure that the exposed areas of thin-film remain on the surface while the rest are removed [16].

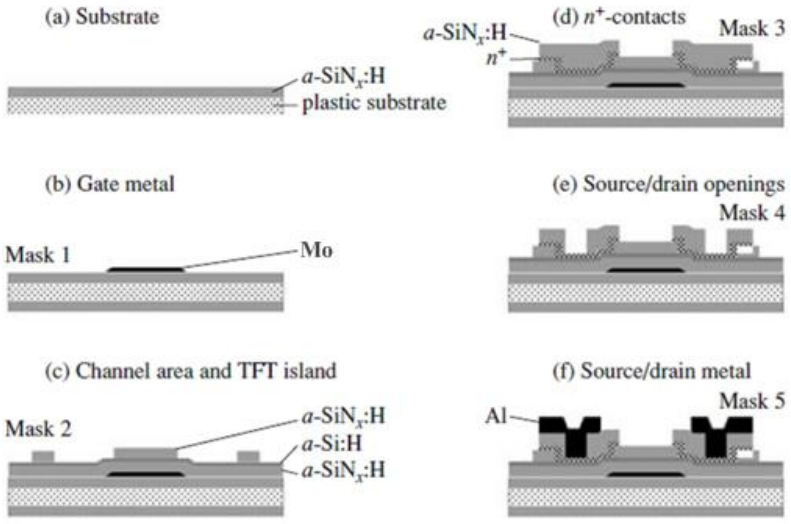


Figure 3.4: Fabrication process used for a-Si:H TFTs on PEN substrates. Adopted from [6].

During the processing of mask layer 3, we found the SiNx:H and n^+ Si layers to have been over-etched during source and drain definition using a phosphoric, acetic, and nitric (PAN) etchant solution. This over etch had exposed too much of the active channel region to air while shortening the source and drain electrode regions. If processing continued, the Al layer on top of the source and drain regions could have touched the surface of the active region. This contact could lead the entire device to short circuit during electrical operation. Therefore, the processing halted for the substrates that were in this condition. To reduce this effect from occuring, it is best to etch the thin-film slowly, by taking multiple mini-steps in etching and inspecting the etched regions with an optical microscope to effectively reduce the effects of over-etching the a-SiN_x passivation layer. Nonetheless, another effective method would be to use a liftoff process for this fabrication step. In this case, PR can be coated under the n^+ and a-SiN_x thin-film. After patterning the PR and depositing the n^+ and a-SiN_x thin-film, the PR would be lifted-off. This would result in sharp-edges of source and drain contact regions. A drawback of this lift-off process would be that residue may stick onto the active channel region; near the interface is where the back-channel of charge is formed during electrical conduction. This residue can cause contamination in the charge path, and thereby lead to open circuited or non-functional devices. Thus, care is needed in both cases to minimize contamination into the active region of the TFTs.

After fabrication, the TFTs are placed in a vacuum oven and annealed at 150^0C to improve the electrode contact over n^+ regions. This processing step would help reduce contact resistance at the electrodes. It can also assist in dopant activation by allowing interstitial charge carriers to move into vacancies of the lattice structure and thus, lead to 4-fold coordination bonds to activate the existing dopant ions in

the n^+-Si [15]. This processing step could greatly influence the functional behaviour of the devices fabricated.

3.2.3 Delamination process

Following successful completion of TFT fabrication as discussed in the previous section of this thesis, delamination of the substrate from the rigid carrier would occur to obtain the desired flexible circuitry. Delamination is a crucial step that must proceed with care to ensure that none of the fabricated devices nor the substrate itself would be damaged by the process. As suggested by Wagner et. al, the detachment should ensure that only the melting of the adhesive occurs, without melting the substrate [41]. For this reason, the process involves the submersion of the sample in an acetone-filled enclosure. An enclosure should be used to prevent the acetone solvent from evaporating. Acetone was selected to be the solvent here as the silicone readily dissolves, allowing for the PEN substrate and Kapton film to detach from the rigid carrier. The process would last for approximately 48 hours with a natural cross-linking of the adhesive occuring from the Kapton, PEN, and glass surfaces. Because of this natural delamination process, minimum strain to the devices on PEN would result through this chemically induced process. The substrates must be subsequently annealed at 150^0C to ensure no moisture would linger on the PEN substrate and thereby, affect device performance and lifetime characteristics. Figure 3.5 shows an image of a sample undergoing delamination.

Some methods of speeding the delamination process include heating the solvent and manually assisting delamination. When heating the acetone solvent, the volume in the acetone bath must be rigorously controlled as the bath could easily evaporate.

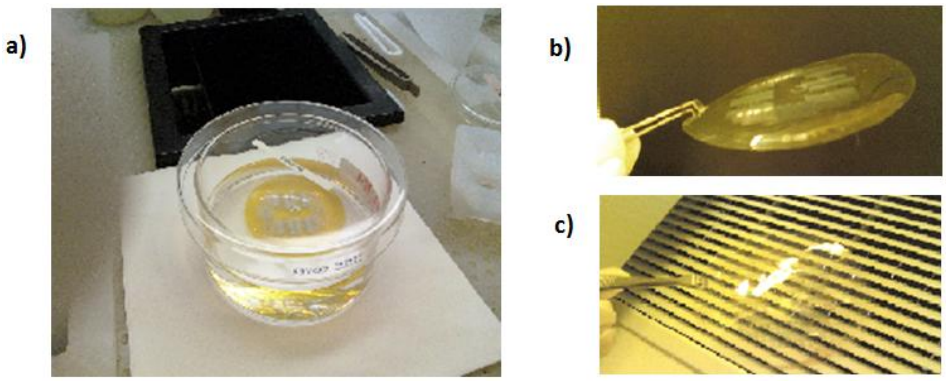


Figure 3.5: a) Delamination of a substrate in acetone, b) delaminated substrate, and c) optically transparent substrate post-fabrication and delamination.

While this may speed-up delamination, the process may lead to substrate warpage and deformation if proper steps are not taken afterwards to remove the moisture from the substrates. Optimizing these techniques as well as finding more innovative techniques of delamination to minimize deformation to the samples and cracking of thin-film are areas that should be further investigated.

3.3 Overlay misalignment measurement techniques

To measure the misalignment of mask layers between each processing step, alignment marks are placed within the layout of each mask layer itself. Thus, during exposure of a mask, the alignment marks would be transferred onto the PEN substrate. Using this method, deformation of the PEN substrate in the form of expansion or contraction can be quantitatively noted between successive overlay mask layers during the fabrication process of a-Si:H TFTs. Overlay alignment marks are placed at multiple locations of the PEN substrate for comparison against those of

mask layer 1, in which the gate metal electrode has been patterned. Mask layer 1 is used as the basis to measure the misalignment of all other process steps since it is patterned first. In addition, a set of overlay alignment marks are positioned at the centre of the PEN substrate; alignment at other positions of the substrate are measured and evaluated with respect to the centre of the PEN substrate. The centre alignment marks are therefore used as a lateral basis for all other locations of the PEN substrate. Thus, keeping the centre of the substrate well-aligned, the amount of misalignment in all other locations of the PEN substrate are measured. Figure 3.6 displays the alignment marks that have been used to measure misalignment on the PEN substrates. A set of horizontal and vertical vernier marks for each mask layer as well as a cross and a group of concentric squares are illustrated in the figure. The verniers provide information about the amount of overlay misalignment and orientation of the misalignment while the cross and concentric squares assist in the alignment process prior to patterning. Each vernier is 1 μm in width and separation to each other. Alignment begins at the centre where the tallest vernier exists. Such a set of alignment marks are positioned in multiple areas of the 3 inch PEN substrate, including the substrates' edges. The misalignment at such distances away from the centre of the PEN substrate would provide a clearer view as to the degree of deformation of the substrate. This information would assist in transferring device fabrication onto larger areas.

Prior to measuring misalignment, the mask must be aligned as much as possible to the substrate in two ways. The first is a centre alignment of aligning the mask to the PEN substrate. This occurs by ensuring that the smallest square in the centre of the bigger ones is at the centre of the cross. As a rule of thumb, the vernier marks beside the cross and squares must be observed; the centre long vernier mark

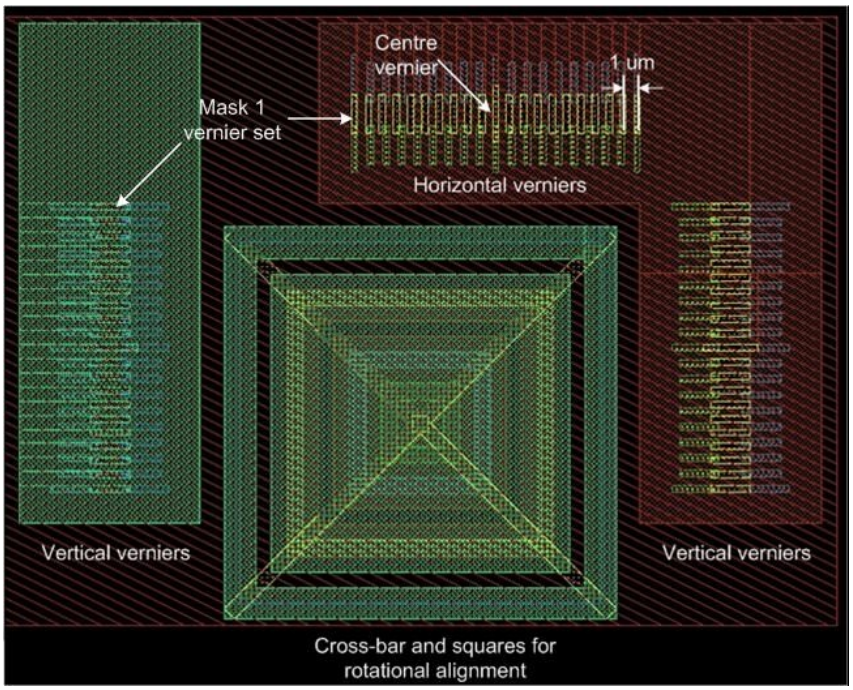


Figure 3.6: Alignment marks used to measure overlay misalignment between mask layer 1 and successive mask layers on the PEN substrate.

of the mask for both horizontal and vertical axes must also be well aligned with that of the PEN substrate. To measure the overlay misalignment of a specific mask against mask layer 1, vernier sets are further separated into the mask layer that they represent. Figure 3.7 shows an example of such a vernier set. The next mechanism of alignment is rotational, which consists of aligning the substrate to the mask by ensuring the lateral mismatch angle of the two substrates are 0^0 (well-aligned). The cross and the square alignment marks shown in Figures 3.6 and 3.7 are helpful in this task of aligning the mask and PEN substrate for rotational alignment.

Figure 3.7 shows a set of verniers for the horizontal dimension as well as those for the vertical dimension. As discussed before, these verniers provide a numerical

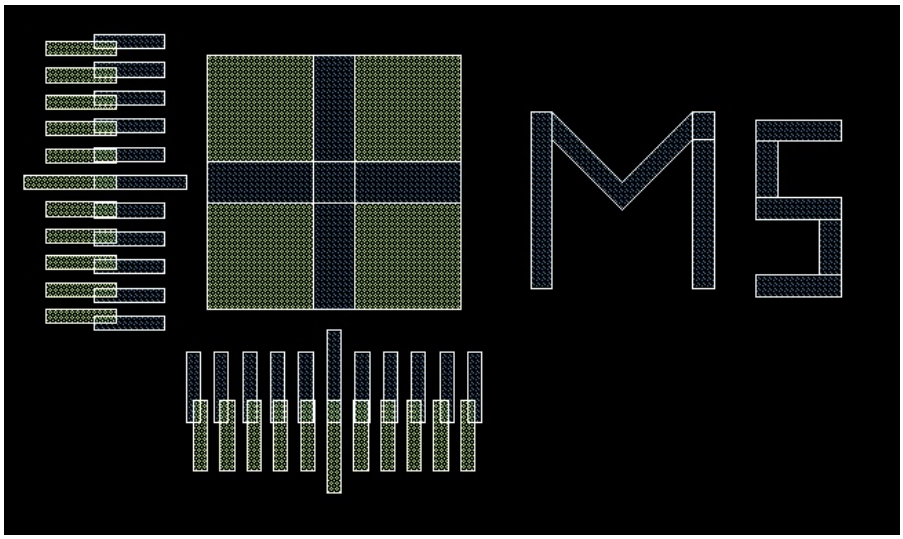


Figure 3.7: Example of a set of verniers for mask layer 5.

measurement for overlay misalignment. The cross that lies in between the four small squares composes a bigger square altogether. The squares and cross are used for rotational alignment while the small square that lies at the centre of this composition is used for centre alignment. Each mask has its own set of alignment marks in this manner at a number of positions on the substrate. Using such tools, the overlay misalignment between successive mask layers can be measured accordingly. From this, we can observe the effectiveness of the entire fabrication process used to reduce the overlay misalignment seen in a-Si:H TFTs on flexible substrates.

The misalignment marks described above are not the only means available to monitor the degree of misalignment between gate layer and source/drain photolithography regions. The channel overlap region of a fabricated TFT has also been used to measure overlay misalignment of successive mask layers. This has been completed by using a calibrated ruler in a standard optical microscope. Since

the lithographic channel overlap region is known to be 10 μm, TFT misalignment has been recorded against any deviation from this amount.

With the recorded data of measurements of overlay misalignment from the PEN substrates that have been laminated and free-standing, a comparison should be conducted between the two methods to analyze the significance of the lamination technique presented in this thesis. The results would suggest how susceptible the deposited thin-film are to cracking during each of the fabrication processes. The TFT layers must adhere well because, they can break easily during delamination [41]. To account for this, the forces of stress of the thin-film and substrate that are acting per unit length of the cross-sectional areas during the fabrication process must be opposite in direction (i.e. tensile versus compressive stresses) but equal in magnitude to provide no strain to the PEN substrate. Since the lamination technique comes with a delamination processing step after fabrication of the devices, electrical characteristics have been presented to test if TFTs fabricated under such conditions can withstand the stress incurred and produce uniformly functional electrical behaviour even after delamination.

Chapter 4

Overlay Alignment of Free-Standing and Laminated Substrates

4.1 Introduction

The overlay registration between successive mask layers in fabricating a-Si:H TFTs are assessed in this chapter to determine overall overlay misalignment with respect to the devices' locations on the PEN substrate. Free-standing substrates have been assessed followed by laminated substrates with a comparison of the methods and the overlay misalignment extracted from each. From such results, we shall recommend more appropriate design rules that may be used for future TFT designs on PEN substrates. The chapter ends with a look at the devices' performance in separate areas of the substrate to analyse electrical uniformity that can be obtained.

4.2 Overlay Misalignment

4.2.1 Free-standing samples

Initial lab work have been conducted with no adhesion of the PEN substrates to rigid carriers, for which we call free-standing samples, for the fabrication of a-Si:H TFTs. During photolithography however, the flexible substrates were attached to oxidised glass substrates. The batch of substrates went through the same conditions for the fabrication of a-Si:H TFTs as described in Chapter 3 to ensure that the only dynamic output is overlay misalignment between successive mask layers while the only dynamic parameter remains as free-standing versus laminated substrates.

An observation made during the fabrication of bottom-gated a-Si:H TFTs was the amount of random cracks on the plastic wafers. The number of cracks increased with each additional mask layer. Although processing was maintained at 150^{O}C, it is believed that some reasons exist for cracking of thin-film on the substrate:

- Substrate handling
- Device processing

Ambient humidity and contaminants on surfaces where the samples lay could lead to the penetration and ultimately, breakdown of the passivation layers. In such a case, the substrate can absorb these particles to its lattice structure, resulting in a non-uniform expansion of the substrate, which can lead to process variations and overlay registration misalignment. Due to substrate variations, cracking would occur due to the stress laid on the substrate. Improper substrate handling mechanisms

can facilitate thin-film cracking. This includes, dropping the substrate on hard surfaces and carelessly mounting substrate to carriers, heavy agitation of substrate during PR developing and stripping as well as during wet chemical etching, and negligence during substrate cleaning processes. Lastly, the a-SiNx gate dielectric stress built up during device processing can lead to further tension or compression to the substrate [41], which can cause random cracking of deposited thin-film. The intensity of such cracking is unknown but, to prevent cracking of the thin-film and substrate, the pressure during deposition of the a-SiNx has been reduced to ≈120 Pa.

Overlay misalignment have been obtained after each mask layer process except that of the gate metal layer (first mask). All layers have been aligned and analysed with respect to the gate metal as it is the first mask layer deposited on the substrate. Appendix A.1 shows overlay misalignment values obtained in both horizontal (x) and vertical (y) directions for each free-standing substrate at each mask layer. Four substrates have been used as samples to obtain a more accurate measure of overlay misalignment. The measured values correspond to specific areas that locate alignment marks on the substrate for overlay misalignment. For free-standing samples, the values obtained are assigned in each table in Appendix A.1 according to their position on the substrate; columns and rows relate to these positions on the substrate based on the design layout used. The magnitude and direction of the values obtained have been considered independently in the analysis of substrate deformation. Average and standard deviation values of the substrate topography based on the values obtained for overlay misalignment have also been recorded and shown in Appendix A.1. All samples are aligned with respect to the centre of their substrates. Thus, the closer the TFT is to the centre of the substrate, the higher

Table 4.1: Misalignment of mask layers on free-standing substrates.

Distance from center [μm]	Misalignment [μm]			
	Horizontal	Vertical	Hypotenuse	Average
0			0.4	0.4
11884			1.9	1.9
13928			4.9	4.9
14160.3	9.25	11.5	14.76	10.38
14941.6	8.25	8	11.49	8.13
15087	11.5	15.5	19.3	13.5
15556.5	11.75	8.13	14.29	9.94
16001			26.1	26.1
16350	12	13.75	18.25	12.88
16824			24.7	24.7
18984			28.1	28.1
19014.4	8.88	13.5	16.16	11.19
19912.7	8	12.88	15.16	10.44
20173.7	14	15	20.52	14.5
21540.7			24.7	24.7
25197.6	18	19	26.17	18.5
25451.3	14.25	17.13	22.28	15.69
29782.4	16.25	23.25	28.37	19.75
30606	13.75	21.5	25.52	17.63
30646.8	21.33	19.75	29.07	20.54
30825.4	20.5	16	26.01	18.25

the alignment of one mask layer to another is likely to be, thereby producing well-aligned TFT structures. However, the goal is to produce well-aligned TFTs and other device structures further away from the centre of the substrate as well such that even 60 inch arrays of TFTs can be produced. Table 4.1 shows the average overlay misalignment observed with distance to the centre of the substrate for the free-standing samples.

The values shown in Table 4.1 have been obtained from all 4 substrates that

used the same design layout for fabrication. Overlay misalignment significantly increases past 0.5 inches of the substrate, from 4.9 μm to as high as 20.5 μm. Aditionally, the misalignment is not a gradual increase with respect to distance from the centre of the substrate but, rather a non-uniform rise, showing deformation at specific areas being significant compared to other areas of the substrate. The average and hypotenuse values that do not possess horizontal and vertical values have been obtained from device structures directly where no vernier marks specifically for horizontal and vertical directions exist. Such areas have been considered to produce a more comprehensive study of the overlay misalignment on free-standing substrates. Although average overlay misalignment relates to the mean distribution of misalignment based on the values obtained in the horizontal and vertical directions, taking the hypotenuse provides a more accurate representation of the total deformation of the substrate. Figure 4.1 shows the gate, source, and drain electrodes of two TFTs patterned on the free-standing substrates. The TFTs shown here have been located near the edges of the 3 inch substrates. This figure facilitates in visually understanding the significance of the values shown in Table 4.1. The sudden increase in overlay misalignment, severely degrades the TFT structure as shown in Figure 4.1, which can in turn lead to non-functional devices.

From the values obtained, it can be concluded that overlay misalignment on free-standing flexible substrates increases with no apparant set relation as the edges of the substrate are approached. Both expansion and shrinkage, which are denoted by a plus (+) sign and a minus (-) sign near the values, respectively, have been detected in several areas on the substrate with shrinkage being the more dominant feature as a consequence of the stress of the deposited thin-film along with frequent moisture to the substrate. By inspection during fabrication, samples had not maintained their

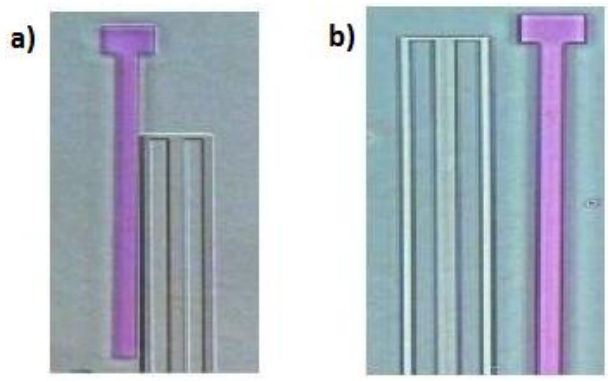


Figure 4.1: Images obtained of bottom-gated a-Si:H TFTs fabricated on free-standing substrates. TFTs are located on the a) left corner-most edge and b) right corner-most edge of a 3 inch substrate.

surface flatness but instead, deformed by swelling in some areas and shrivelling in others, further explaining the dimensional instability and variation of the free-standing substrates. In addition, it is clear that considerable overlay misalignment has been obtained at the second mask layer more than the other mask layers, relative to the location of misalignment on the substrate. Due to the trilayer deposition, the siginificant increase in stress to the substrate most likely strained the substrate to different orientations to alleviate the stress exerted, which consequently caused the increase in overlay misalignment in this mask layer. Thus, stress exerted to the substrate must be considered in optimizing fabrication processes of thin-film. Such research is underway by primarily reducing the stress in the SiNx [26]. Although it is reasonable to further such studies, the substrate where fabrication would occur must be considered and studied to cooperate with the tensile and compressive stresses attained. Merely adjusting for one of these stresses is futile as the substrate becomes exposed to both stresses as noticed in this fabrication process.

4.2.2 Laminated samples

Overlay misalignment values on laminated substrates have been analysed for mask 2 only since experiments based on free-standing substrates have shown a need for improvement in overlay alignment at this mask layer compared to the other layers. Nonetheless, Appendix A.2 shows overlay misalignment values obtained with respect to the gate for all other mask layers for subsequent mask designing in Section 4.2.3. Appendix A.2 comprises of the data sets obtained for overlay misalignment on laminated samples. Average and standard deviation of the samples have also been recorded. Due to the different design layout used for these samples, only verniers representing the horizontal and vertical directions in movement at the corner-most edges of the substrates have been recorded. All other values for overlay misalignment have been taken from device structures itself thus, corresponding to no values for strictly horizontal and vertical directions but rather, average and hypotenuse values. The average overlay misalignment with respect to distance from the centre of the substrate of laminated substrates after mask layer 2 deposition is shown in Table 4.2.

Here too, overlay misalignment values obtained for the hypotenuse based on horizontal and vertical directions are considered more accurate measures of registration misalignment than the average values obtained at vernier locations. Based on values obtained from the hypotenuse of horizontal and vertical vernier marks, the average overlay misalignment obtained is 2.1 μm with the maximum value obtained being 5.57 μm, occuring at 2.6 cm (1.02 inches) away from the substrate, which comprises of a diameter of $\approx$3.8 cm (3 inches). Figure 4.2 shows the overlay alignment of the TFTs that are located near the edges of the substrate that have been fabricated on

Table 4.2: Misalignment from laminated samples.

Distance from center [μm]	Misalignment [μm]			
	Horizontal	Vertical	Hypotenuse	Average
0			0	0
8190			0.5	0.5
8947			0.5	0.5
9837			0.8	0.8
14180			1.5	1.5
14920			1.9	1.9
17850			2.4	2.4
19843			2.6	2.6
23947.66	2	2	2.83	2
24040.3	1	1	1.41	1
26343.48	3.5	4.33	5.57	3.92
26350.69	1	3.17	3.32	2.08

laminated substrates.

From Figure 4.2, significant improvement can be noticed in overlay registration between successive mask layers. Substrates that were laminated throughout the fabrication of a-Si:H TFTs encountered much less movement and dimensional variation, which resulted in high overlay alignment between mask layers. It has been hypothesised prior to the fabrication of TFTs on laminated substrates that the process of lamination would add more changes to alignment due to the bonding of the substrate to a rigid carrier through another plastic. However, the Kapton tape, which comprises of the uniform layer of silicone adhesive, does not seem to negatively affect the bonding of the PEN substrate to the rigid carrier. Due to the strong bonding of the lamination process, the samples experienced very little deformation shown in the values obtained in Table 2.

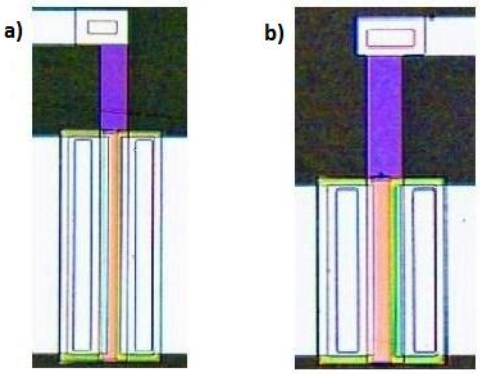


Figure 4.2: Images obtained of bottom-gated a-Si:H TFTs fabricated on laminated substrates. TFTs are located on the a) left corner-most edge and b) right corner-most edge of a 3 inch substrate.

4.2.3 Impact from substrate centre

All samples have been aligned with respect to the centre of the substrate with a rotational alignment to ensure both sides of the substrate are equally aligned prior to lithographic patterning. Figure 4.3 illustrates the average overlay misalignment of the two differently processed sample sets plotted for comparison.

Here, it is clear that a degradation in overlay misalignment and standard deviation exists in the laminated samples compared to the free-standing ones. The significant improvement in overlay alignment can be attributed to the attachment process of the laminated samples; by mitigating air bubbles, moisture, and other contaminant particles into the plastic-on-carrier stack, the substrates have been well intack with the rigid carriers. The standard deviation can be correlated to the dimensional stability of the substrate, suggesting that a higher standard deviation amounts to more deformation experienced to the substrate's dimensions. Taking distance into consideration, a linear best fit has been observed for the first inch

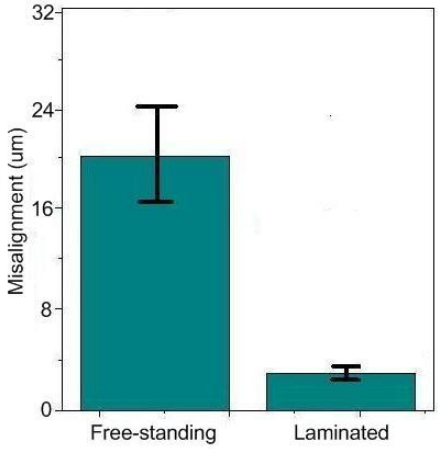


Figure 4.3: Average overlay misalignment in free-standing and laminated substrates.

radially from the centre of the substrates. To compare the difference between the two different batch of samples, the data has been plotted with their respective lines of best fit as shown in Figure 4.4.

Figure 4.4 shows the standard deviation in the two different sample sets. The standard deviation has been obtained from the values shown in Appendix A for each processed set. Here, the laminated substrates show a lower deviation from their average overlay misalignment. Yet, as the distance from the centre of the substrate increases, the overlay misalignment also increases gradually, as hypothesized at the beginning of the fabrication process. The line of best fit shown in Figure 4.4 for each curve can be used to extrapolate the average overlay misalignment for a substrate above 3 inches. Such a method can be used to predict the outcome of devices fabricated at specific distances from the center of the substrate, and thereby, compensate for this error in TFTs at the mask design stage accordingly. The line of best fit for the laminated substrates would follow,

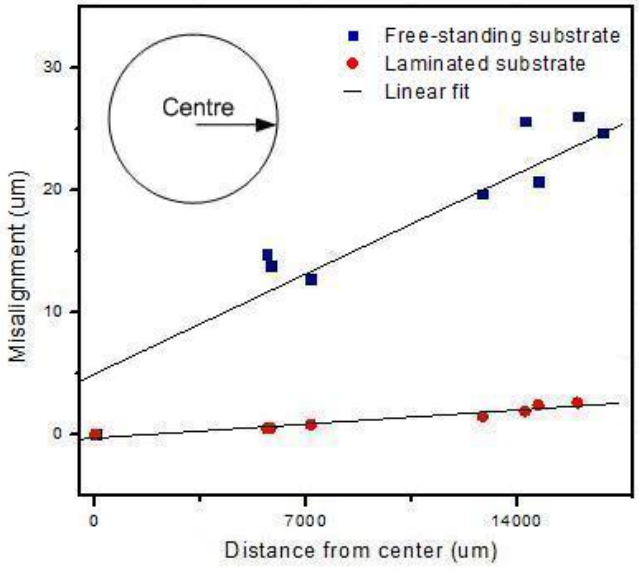


Figure 4.4: Misalignment in free-standing and laminated substrates.

$$y = 0.0001x - 0.433 \tag{4.1}$$

where x and y denote the distance of the device from the center in microns and corresponding average misalignment in microns, respectively. The line of best fit for a free-standing substrate follows,

$$y = 0.0012x + 4.989. \tag{4.2}$$

Equation 4.1 depicts a y-axis intercept of 0.433 μm while Equation 4.2 depicts a y-axis intercept of 4.989 μm, suggesting the alignment precision at the centre of both laminated and free-standing substrates requiring adjustments. To compensate

for this change in the substrates and to ensure all values are with respect to the centre, which we would like to assume as posing no misalignment, the values in all other areas of the substrates have been adjusted accordingly and shown in Appendix A.1. These equations would pose particularly useful in determining the extent of adjustments needed to the source-drain to gate overlap and aperture ratio of the a-Si:H TFTs so as to buffer the misalignment observed here. For this reason, the slopes of the above said equations are used. The slope here depicts the average misalignment noticed per micron away from the centre of the substrate. Based on this value, we can approximate the amount of overlap required at the mask layout to ensure well-aligned structures would form on the substrate. Figure 4.5 shows the overlap between masks 1 and 2 (OL_{21}) and aperture ratio of the a-Si:H TFT. For example, since the maximum overlay misalignment has been observed at 2.6 cm away from the centre of the substrate, the buffer length added to the gate electrode would be 2.6E4 μm x 1E-4 = 2.6 μm. This buffer value would be added to the gate length of the TFT structure. Thus, in a 100/25 (W/L) aperture ratio TFT, the gate length should change from 45 μm to 47.6μm. All other parameters such as source and drain openings as well as a-SiNx separation widths are part of mask layer 2 and thus, do not require buffer adjustments to their design values. This would result in OL_{21} to increase from 10 μm to 12.6 μm. However, after fabrication, due to shrinkage of the PEN substrate, the OL_{21} would decrease, resulting in a final OL_{21} of 10 μm.

Nonetheless, the upper mask layers must also be considered to fabricate a well-aligned TFT structure. Although the average change in overlay alignment is $\approx$1.3 μm between mask layers 1 and 3, the change per micron away from the substrate centre must be added to the gate length. The graph that illustrates the linear fit of

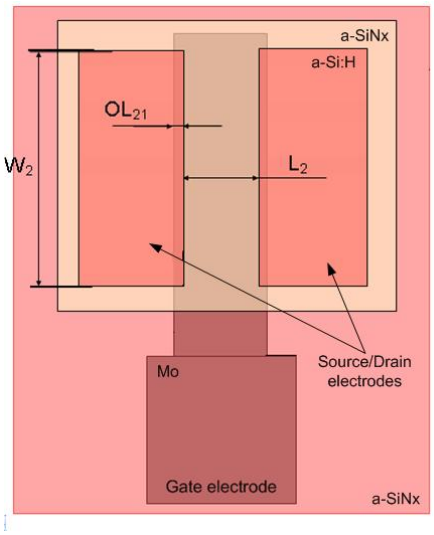


Figure 4.5: A-Si:H TFT design parameter adjustments between mask layers 1 and 2. Based on [49].

mask 3 in Appendix A.1 is helpful to determine the amount that must be added to the gate length and width. However, it is noted from Figure 4.6 that masks 4 and 5 do not overlap the gate metal and thus, do not require further adjustments to the gate dimensions. However, an average overlay misalignment of ≈0.4 μm shrinkage has been obtained through measurements at OL_{54} as illustrated in Figure 4.6. To prevent overlay misalignment here, OL_{54} must be increased by a buffer amount of 0.4 μm, and thereby enlarging the via opening. An overlay misalignment between the n^+ doped silicon and aluminum metal contacts would not pose a great issue due to their high electro-conductivity. The end result of overlay alignment between successive mask layers is illustrated in Figure 4.6 with a gate length of 48.64 μm and channel width of 103.64 μm. Note the actual channel L/W of 25/100 would result after the entire fabrication process of the a-Si:H TFT due to substrate contraction. Although the mask layout has been adjusted to a TFT structure 2.6 cm away from

the centre of the substrate, this procedure must continue for all device structures such that, particularly those further away from the centre, possess improved overlay alignment.

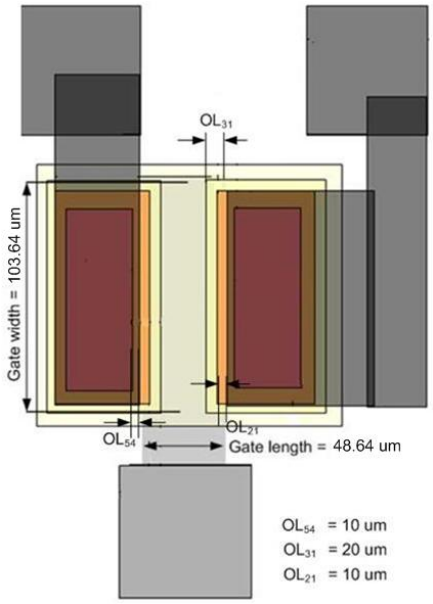


Figure 4.6: Final a-Si:H TFT mask layout adjustments with the overlay of all mask layers. Based on [49].

Since the proximity to the centre of the substrate from the alignment marks must be taken into consideration due to the approach in aligning the substrates taken in patterning structures, the percentage of strain detected has been obtained to eliminate location of its occurance with respect to its proximity to the centre of the substrate. This is to further determine the dimensional stability of the substrate after the fabrication of devices. Figure 4.7 shows the plot of percentage of strain for both sets of samples obtained.

The percentage of strain shown in Figure 4.7 has been obtained by taking the

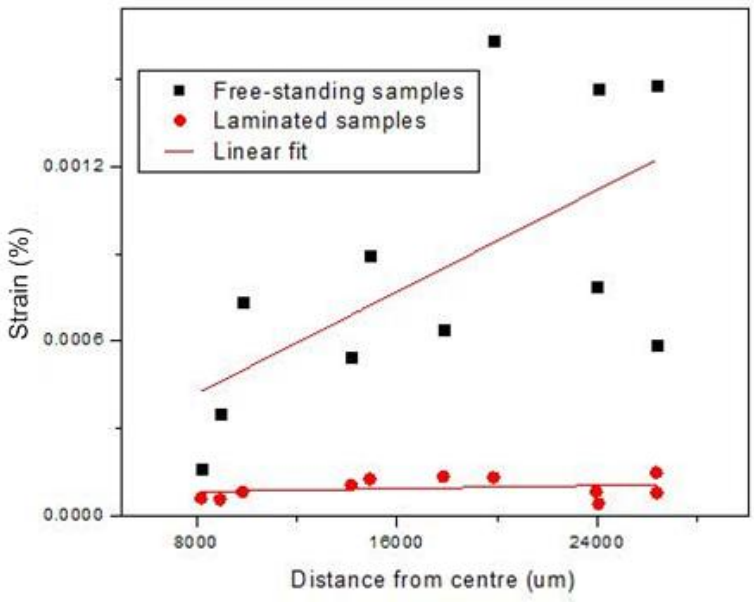


Figure 4.7: Percentage of strain in free-standing and laminated samples.

ratio of misalignment to distance and presenting the calculated value in percent form. Ideally, a constant zero-sloped linear (i.e. flat line) fit would be obtained for a fully dimensionally stable substrate. Although the linear fit for laminated substrates in Figure 4.7 is much lower in value and shallow in slope, indicating a lower overlay misalignment and more dimensionally stable substrate, respectively, the slope indicates that deformation in the substrates occur and have not been fully eliminated. Micro-deformation of the substrate has been attributed to the behaviour of overlay misalignment experienced this way in laminated substrates [18]. Despite the improved dimensional stability of laminated samples, the substrates still exhibit an inplane micro-deformation during fabrication due to the solvents and high temperature-to-RT exposure. This micro-deformation is the reason for overlay mismatch, although small, to exist in patterned TFTs on laminated sam-

ples. According to previous lamination experiments conducted with PEN substrates and Si rigid carriers, an initial in-plane strain of 13 +/- 33 ppm has been reported [18], corresponding to ≈1.3 μm of misalignment with a post-fabrication in-plane micro-deformation of 1758 +/- 199 ppm. Studies here confirmed that this deformation stemmed thermally at the final adhesive curing step of lamination, which occurred at 160^{O}C. The thermal exposure during the final curing step introduced micro-strains, which caused thermal expansion mismatches between substrate, adhesive, and rigid carriers. In our lamination process too, samples had undergone exposure to thermal cycles during thin-film fabrication. Alternative processes such as use of sub-100^{O}C for TFT fabrication have been explored to reduce strain in devices on flexible substrates [50]. Due to the use of a double-sided tape as our adhesive mechanism to attach PEN to the rigid glass substrates, curing steps have not been required. In addition, the elastic modulus and thermal expansion coefficients of polyimide and PEN are similar, suggesting low effects of distortion from these materials. Nonetheless, the use of solvents as suggested earlier can lead to deformation of the PEN substrate; use of them during processing of TFTs can not be eliminated but, must be reduced to further alleviate deformation seen in laminated samples.

4.2.4 Stress effects to overlay misalignment of TFTs

To further determine the strain induced during thin-film layer deposition for TFT fabrication, we have studied the effects of built-in stress from the trilayer deposition (mask 2) since the main source of overlay misalignment and thereby strain induced to the PEN substrate has been noticed in mask 2. We believe knowledge

garnered from this study can be used to understand the amount of stress handled and compensated by the polyimide tape via correlation of stress values obtained to strain on the substrate. During processing, deposited film tend to form a tensile or compressive stress, which subsequently distortes the substrate. When deposition occurs at elevated temperatures, as in a PECVD, the CTE mismatch of the thin-film and substrate is reason for generating this stress. Tensile stress is where the film is seen to relax by contracting, as shown in Figure 4.8, while compressive stress occurs when the film expands over the substrate. Minimization of stress is critical to ensure prevention of thin-film peel-off, which occurs when the stress in the film exceeds its maximum handling capacity. It can also lead to void formation upon subsequent thermal heating. Both characteristics are detrimental for the electrical properties of TFTs.

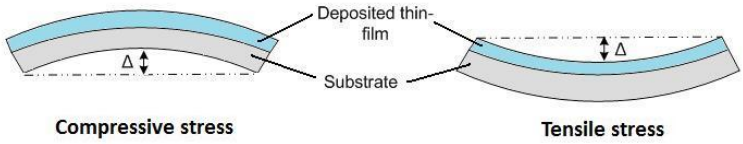


Figure 4.8: Change in deflection, Δ, is used to measure thin-film stress.

To measure the in-built thin-film stress, the bow of the underlying substrate before and after film deposition is used. For this experiment, all measurements have been obtained using an Ionic Systems stress-gauge system. A tri-layer comprising 300 nm a-SiN_x/50 nm a-Si:H/300 nm a-SiN_x has been deposited in a PECVD on Si. Two p-type Si substrates have been used here to ensure deflection from the light source of the stress-gauge would occur for usage of film stress extraction. Table 4.3 depicts the stress values obtained in both substrates from the stress-gauge after each thin-film layer deposition. Three values for each substrate have been collected

Table 4.3: Built-in stress of the trilayer thin-film.

Substrate Number	Stress (dynes/cm^2)		
	After 1st a-SiN$_x$	After a-Si:H	After 2nd a-SiN$_x$
1	3.74E+09	-7.63E+08	-7.73E+08
	4.10E+09	-6.02E+08	-6.38E+08
	3.58E+09	-8.01E+08	-7.57E+08
Average:	3.81E+09	-7.22E+08	-7.23E+08
2	4.28E+09	-4.89E+08	-4.90E+08
	4.17E+09	-5.84E+08	-5.82E+08
	4.31E+09	-5.17E+08	-4.75E+08
Average:	4.25E+09	-5.30E+08	-5.15E+08

to obtain an accurate view of the average stress of the thin-film. Appendix B contains a more comprehensive table with each of the deflection values obtained in the experiment as well as the calculations made in each step. To calculate the built-in stress of the tri-layer, the following equation has been used:

$$\gamma = \frac{\Delta Y_s T_s^2}{(D/2)^2 3(1-\nu)T_f} \tag{4.3}$$

where wafer deflection (Δ), knife edge diameter (D = 76.2E-3), Young's modulus of substrate (Y_s = 1.055 x 10^{12} dynes/cm^2), $\nu = 0.446$, thickness of substrate (T_s = 450E-6 m), and film thickness (T_f) are used as input parameters with the intrinsic thin-film stack stress (γ) presented as the output parameter. Here Y_s and ν are considered temperature independent and thus, do not contribute to stress variations at elevated temperatures [48].

Although the input parameters to Equation 4.3 have been used with respect to the properties of Si, a qualitative understanding of the built-in stress of the thin-film deposited can be gained. As noted in Table 4.3, after the first a-SiN$_x$ deposition,

a compressive stress is achieved from both substrates as all stress values in both substrates are positive, describing a greater deflection reached by the light ray after the deposition. An average of 0.4 GPa is achieved from the 2 substrates for the first a-SiN_x deposition. However, a tensile force is exerted after the 50 nm a-Si:H deposition, bringing the substrate closer towards its original shape. The final a-SiN_x deposition further pushes the substrate to its original place with a tensile force of 61.9 MPa. Observations indicate that initial atomic layers of deposition requires significant relaxation compared to subsequent layers deposited. The average stress obtained can be used to correlate the strain observed through overlay misalignment in the fabricated samples. Thus, 61.9 MPa of tensile stress of the trilayer film corresponds to an average strain of 2.1 μm to the substrate. This preliminary analysis can be used to further explore and optimize thin-film fabrication conditions for stress compensation on laminated substrates, in which it is believed that further reduction in strain to the PEN samples can be obtained and thus, significantly reduce overlay misalignment on a-Si:H TFTs in large area.

4.3 Performance

The performance of a-Si:H TFTs on the laminated substrates is studied here. Figure 4.9 shows the transfer characteristics of a well-aligned TFT on PEN substrate in enhancement mode. The overlay misalignment observed in this TFT at the overlap region is $\approx$2 μm; in par with the average overlay misalignment noticed in the TFTs fabricated on the laminated substrates. The TFT of L/W being 25/100 shows current-voltage measurements that were performed at RT using a Keithley 4200 semiconductor characterization system. The devices possess an ON/OFF ratio of

10^8, field-effect mobility of 0.8 cm^2/Vs, subthreshold slope of less than 0.29 V/dec, and gate-leakage current less than 0.1 pA within the bias window. These characteristics are consistent with state-of-the-art a-Si:H TFTs fabricated on plastic [1], [4], [13], [14].

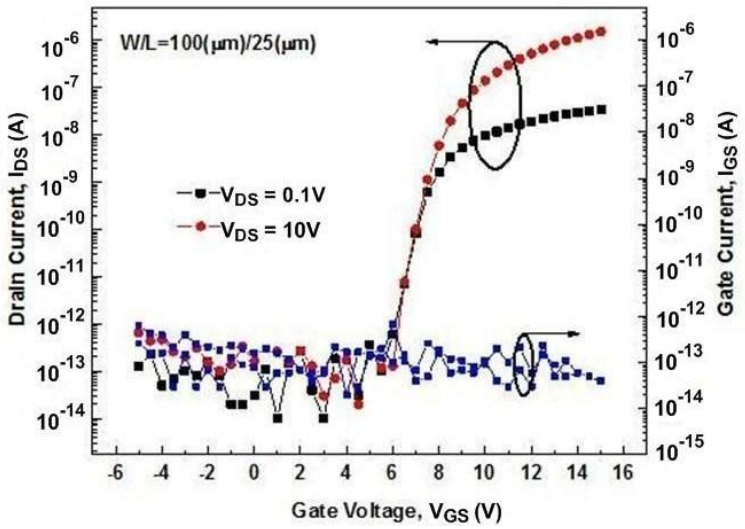


Figure 4.9: I_{ds}-V_{gs} at V_{ds} = 0.1 V and 10 V with I_{gs}-V_{gs} of an a-Si:H TFT on PEN substrate. Adopted from [52].

Generally, a-Si:H TFTs possessing overlap regions constitute for greater subthreshold slopes and off-currents [51]. However, from Figure 4.9, it can be noticed that the Pool-Frenkel region saturates at $\sim 10^{-13}$ A, with a very low reverse subthreshold region. In addition, Pool-Frenkel and gate leakage measurements match at achieving very low current levels. These are desirable features; for Pool-Frenkel this dictates that the positive charge injected at the drain overlap vicinity at negative bias is negligible while for gate leakage, the distribution of charge through the gate dielectric at a given electric-field is low and thus, can be neglected. If such characteristics are negligible at the gate-drain overlap, this could relate to a decrease in

overlap at the region of the a-Si:H TFT due to a contraction to the PEN substrate, and thus, possessing a lower degradation in the TFT behaviour while maintaining gate control over the active region. Although, the off-current should increase considerably at higher V_{ds} in these TFTs on plastic by comparison to those fabricated on glass [51], this has not been the case, as can be seen in Figure 4.9, suggesting satisfactory off-current stability and low defect state creation at the front interface in the fabricated TFTs. This is also dictated by the relatively high (on-current) field effect mobility achieved, also indicating the density of charge carriers trapped in the tail states is low while maintaining a high density of free electrons in the conduction band-edge of the a-Si:H.

To further demonstrate the dimensional stability of substrates laminated through this process, the output (I_{ds}-V_{ds}) characteristics of a-Si:H TFTs fabricated on them are illustrated. Figure 4.10 shows the range of the obtained output characteristics of 5 sampled TFTs that have been taken from separate locations on each substrate as shown in the inset of Figure 4.10 (adopted from [52]). Overlap has ranged between 0 μm - 4 μm in the tested TFTs. This range of variation for I_{ds} at several V_{gs} can be used to realise the uniformity in electrical characteristics of the a-Si:H TFTs fabricated over laminated substrates. As the gate voltage is increased here, saturation of drain current requires higher drain voltage. This can be attributed to an increase in parasitic resistance to intrinsic channel resistance.

Furthermore, several interesting changes to the behaviour in the a-Si:H TFTs on PEN substrates have been observed. After months ($\approx$7 months) of storage at RT, a significant change to the electrical characteristics of the a-Si:H TFTs were found as shown in Figure 4.11. I_{ds}-V_{gs} shows very similar ON/OFF current ratio to Figure 4.9 but, with a V_t shift; at V_{ds} = 10 V, V_t $\approx$10 V as opposed to $\approx$5 V from

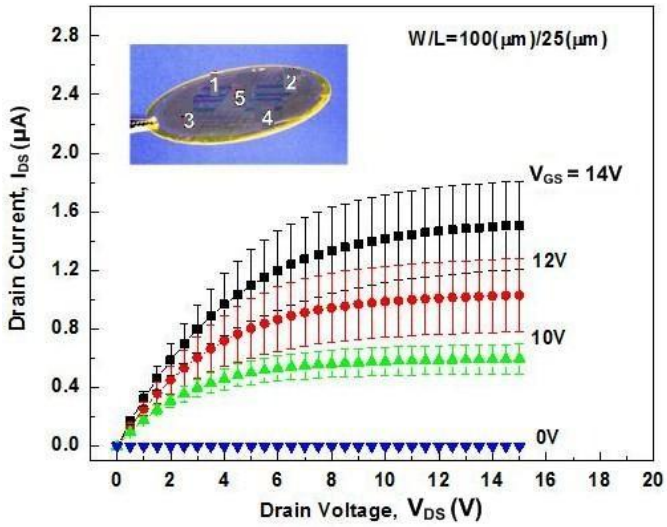


Figure 4.10: Average and standard deviation of V_{ds}-I_{ds} for a TFT on laminated substrates showing their uniformity. Ids reaches saturation at a small drain potential (5 V). Inset shows the location of the sampled TFTs on a laminated substrate. Adopted from [52].

Figure 4.9. The parasitic resistance at the ohmic source/drain contact influences the threshold voltage increase, by which the field effect mobility would in turn decrease in a-Si:H TFTs [51], [53] and has been the case here with ∼0.5 cm^2/Vs. The increase in overlay misalignment noticed in these TFTs can be a reason for the increased parasitic resistance along with the low temperature fabrication process, producing an increased series resistance of contacts as a result of a decrease in the doping efficiency. In addition, we had earlier related overlay misalignment to strain to the PEN substrate, which act together with the stress relaxation from the upper TFT layers in crack propagation in the thin-film. With an increase in strain, the intrinsic defect-state density would further increase due to the breaking of weak bonds in the thin-film. The result of this action would inherently increase the subthreshold

slope of the TFT due to its direct relation to defect density at the front interface of the TFT. The increase in subthreshold slope is partially due to the low temperature fabrication process consequentely, degrading device transconductance. Additionally, it is anticipated that the off-current would increase at greater gate currents as the band-tail at the front interface experiences extended band-bending. Due to the increased overlap capacitance of hole carriers at the gate-drain region residing at the front interface, a dynamic current source can be modeled at this region. Overtime, this characteristic can also affect gate leakage with the trapping of charge carriers in the gate nitride. Since threshold voltage is influenced by charge trapping at the front interface and increased built-in charge in the insulator at increased V_{gs} along with defect state creation in the channel at low V_{gs}, V_t is likely to increase overtime, degrading field-effect mobility. The analysis explains the behaviour observed from the following figures.

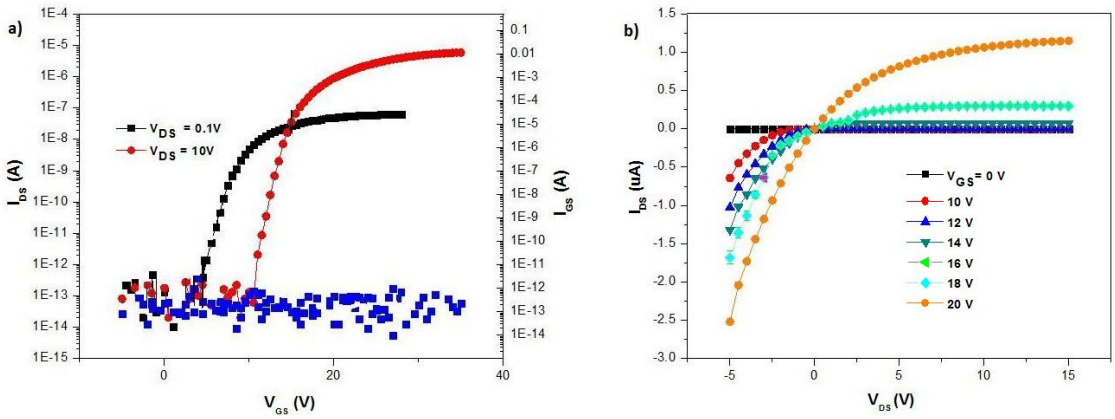


Figure 4.11: a) I_{ds}-V_{gs} and b) I_{ds}-V_{ds} of a corner-most a-Si:H TFT on PEN substrate.

In addition, the output-current at saturation, as shown by I_{ds}-V_{ds}, has severely degraded by comparison to Figure 4.10. Due to the long period of storage of the

TFTs at RT, it is assumed that the penetration of contaminants into the deep channel and gate dielectric has affected the TFTs here.

Chapter 5

Conclusions

To conclude, the contributions made in this thesis has been summarised. Additionally, areas that can be further studied based on our research conducted are presented below.

5.1 Contributions

Incorporating an adhesive to the plastic-on-carrier lamination process throughout the fabrication process of a-Si:H TFTs at low temperatures can assist in drastically reducing the overlay misalignment noticed in devices. This misalignment can be reduced by using the double-sided polyimide tape roll, allowing for standard lithographic and processing infrastructure to be used while complementing future roll-to-roll technology demands. The proposed lamination process effectively reduces the overlay misalignment by almost 10 times to $\sim$2.1 μm. Since the delamination process entails a wet chemical submerging of the samples, the lamination process

is quick and effective in granting a low overlay misalignment fabrication process using already existing infrastructure for a-Si:H TFTs. Additionally, the electrical performance of the fabricated TFTs and their uniformity have further proven that the fabrication process does not degrade the devices fabricated on such substrates.

5.2 Future work

Further improvement to eliminate the overlay misalignment seen in flexible substrates for TFT fabrication is imperative to increase size of flexible display screens. This would also increase the fill-factor, resulting in a higher resolution of displays. For this purpose, more work on substrates larger than 3 inches in diameter would complement feasibility studies of this lamination process. In addition, the design adjustments made in this thesis to the mask layout of TFTs should be emperically tested to determine if changes made to the mask layout would contribute to further aligned TFT stuctures. Moreover, the gradual increase in strain experienced by the laminated samples must be further studied with optimization of the built-in stress of TFT layers. Although laminated, prevention of micro-deformation to the PEN substrates in this kind must be researched at the manufacturing level. Such studies can lead to furthering the high yield of a-Si:H TFTs on large area.

APPENDICES

Appendix A

Overlay Misalignment data sets

A.1 Free-standing samples

Table A.1: Misalignment between Mask 1 and Mask 2 in um for Wafer 1

Column 1				Column 2			Column 3			Column 4				Column 5	
x	y			x	y		x	y		x	y			x	y
24	10			12	17									11	12
-	-			-	-		7	13	,-,-,	6.5	22			+	+
							1	1		-	-				
17	20		16	12			-	-			15	18		10	23
-	-		-	+							-	-		-	-
				13	14		6	11		10	14				
23	16			-	-		+	-		-	-			17	21
+	-													-	-

Table A.2: Misalignment between Mask 1 and Mask 2 in um for Wafer 2

Column 1				Column 2			Column 3			Column 4				Column 5	
x	y			x	y		x	y		x	y			x	y
18	20			15	17									12	26
-	-			-	-		13	8	,-,-,	8	12			-	-
							1	1		-	-				
15	16.5		13	8			-	+			13	19		24	22
-	-		-	+							-	-		-	+
				12	13		15	12		16	12				
21	18			-	-		-	+						18	32
-	-														

Table A.3: Misalignment between Mask 1 and Mask 2 in um for Wafer 3

Column 1				Column 2			Column 3			Column 4				Column 5	
x	y			x	y		x	y		x	y			x	y
17	14	6		10	12.5									16	24
-	-			-	+		9	7	,-,+	12	12			+	-
							0.5	0.5		+	-				
2	13	18	14	12							9	14		14	10
-	-		-	-							-	-		-	-
				10	13		5	9		17	19				
	20	13		+	-		+	-		-	-			16	16
														-	-

Table A.4: Misalignment between Mask 1 and Mask 2 in um for Wafer 4

Column 1				Column 2			Column 3			Column 4				Column 5	
x	y			x	y		x	y		x	y			x	y
23	20			19	5									16	24
-	-			-			4	4	,+,-,	9	8			-	-
							1	-0.5		-	-				
23	19		4	0.5							9	11		24	21
			-	-							-	-		-	-
				13	15		11	14		13	15				
20	25			-	-			-		-	-			14	24
-														-	-

Table A.5: Standard deviation of Misalignment between Mask 1 and Mask 2 in um

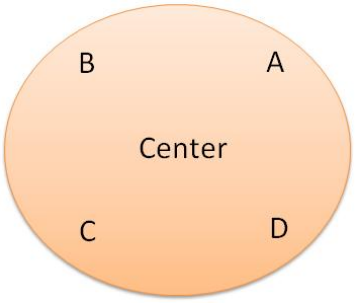
Column 1				Column 2			Column 3			Column 4				Column 5	
x	y			x	y		x	y		x	y			x	y
3.51	4.90			3.92	5.66									2.63	6.40
							3.77	3.74		2.32	5.97				
							0.25	0.71							
8.85	3.12		5.32	5.42							3	3.70		7.12	6.06
				1.41	0.96		4.65	2.08		3.16	2.94				
1.53	3.86													1.71	6.70

Table A.6: Average Misalignment between Mask 1 and Mask 2 in um

Column 1				Column 2			Column 3			Column 4				Column 5	
x	y			x	y		x	y		x	y			x	y
20.5	16			8	12.88									13.75	21.5
-	-			-	+		8.25	8	,+,-,	8.88	13.5			-	-
							0.88	0.5		-	-				
14.25	17.13		11.75	8.13			+	+			11.5	15.5		18	19
-	+		-	-							-	-		-	-
				12	13.75		9.25	11.5		14	15				
21.33	19.75			-	-		+	-		-	-			16.25	23.25
-	-													-	-

A.2 Laminated samples

Locations where misalignment data have been obtained from are shown in the following figure:



ND: No Data available

Table A.7: Misalignment between Mask 1 and Mask 2 in um for Wafer 1

	Center	A	B	C	D
Horizontal	0	0	1	ND	ND
			+	+	+
Vertical	0	1	2	5	5
		-	+	+	+

Table A.8: Misalignment between Mask 1 and Mask 2 in um for Wafer 2

	Center	A	B	C	D
Horizontal	0	ND	1	ND	2
			-		-
Vertical	0	ND	0	0.5	5
				+	+

Due to issues during the fabrication process, use of Wafer 4 had been halted.

Table A.9: Misalignment between Mask 1 and Mask 2 in um for Wafer 3

	Center	A	B	C	D
Horizontal	0	4	ND	1	5
		+		-	-
Verical	0	3	ND	4	3
		+		-	+

Table A.10: Standard deviation of Misalignment between Mask 1 and Mask 2 in um

	Center	A	B	C	D
Horizontal	0	2.828427	0	0	2.12132
Vertical	0	1.414214	1.414214	2.362908	1.154701

A.2.1 Overlay misalignment measurements between Masks 1 and 3

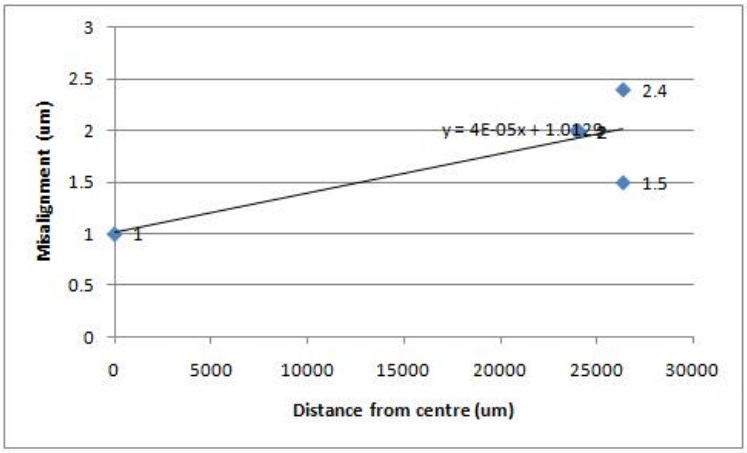


Figure A.1: Distance versus overlay misalignment between Masks 1 and 3

Table A.11: Average Misalignment between Mask 1 and Mask 2 in um

	Center	A	B	C	D		AVG
Horizontal	0	2	1	1	3.5		1.5
Vertical	0	2	1	3.166667	4.333333		2.1

Table A.12: Misalignment between Mask 1 and Mask 3 in um for Wafer 1

	Center	A	B	C	D
Horizontal	1	2	3	ND	3
		-	-		-
Vertical	1	2	2	ND	3
		-	-	-	-

Table A.13: Misalignment between Mask 1 and Mask 3 in um for Wafer 2

	Center	A	B	C	D
Horizontal	1	3	2	3	3
		-	-	-	-
Vertical	1	1	3	2	2
				+	-

Table A.14: Average misalignment between Mask 1 and Mask 3 in um

	Center	A	B	C	D	AVG
Horizontal	1	2.5	2.5	3	3	2.8
				-	-	
Vertical	1	1.5	2.5	2	2.5	2.1
				+	-	

A.2.2 Overlay misalignment measurements between Masks 1 and 4

Table A.15: Misalignment between Mask 1 and Mask 4 in um for Wafer 1

	Center	A	B	C	D
Horizontal	1	2	3	ND	2
			-		-
Vertical	1	3	2	ND	3
		-	-		+

Table A.16: Misalignment between Mask 1 and Mask 4 in um for Wafer 2

	Center	A	B	C	D
Horizontal	1	4	3	3	4
					-
Vertical	1	4	3	4	4
		-		-	-

Table A.17: Average misalignment between Mask 1 and Mask 4 in um

	Center	A	B	C	D	AVG	AVG2
Horizontal	1	3	3	3	3	3	
					-		2.15
Vertical	1	3.5	2.5	4	3.5	3.38	

A.2.3 Overlay misalignment measurements between Masks 1 and 5

Table A.18: Overlay misalignment between Mask 1 and Mask 5 in um for Wafer 1

	Center	A	B	C	D
Horizontal	1	3	4	3	3
			-	-	-
Vertical	1	4	3	3	4
		-		-	-

Table A.19: Overlay misalignment between Mask 1 and Mask 5 in um for Wafer 2

	Center	A	B	C	D
Horizontal	1	4	4	3	3
			-	-	
Vertical	1	3	4	4	5
		-	-	-	-

Table A.20: Average misalignment between Mask 1 and Mask 5 in um

	Center	A	B	C	D	AVG
Horizontal	1	3.5	4	3	3	3.4
			-	-		
Vertical	1	3.5	3.5	3.5	4.5	3.8

Appendix B

Stress analysis of deposited trilayer film

SiNx/a-Si/SiNx tri-layer:

Table B.1: Deflection values and corresponding stress

Subs. Num.	Deflection (uinches)				Stress (dynes/cm^2)		
	Initial reading	After 1st a-SiNx	After a-Si:H	After 2nd a-SiNx	After 1st a-SiNx	After a-Si:H	After 2nd a-SiNx
1	2460	4087	2073	1732	3.74E+09	-7.63E+08	-7.73E+08
	2330	4110	2025	1729	4.10E+09	-6.02E+08	-6.38E+08
	2445	4001	2039	1732	3.58E+09	-8.01E+08	-7.57E+08
Avg:	2411.67	4066.00	2045.67	1731.00	3.81E+09	-7.22E+08	-7.23E+08
2	2192	4050	1944	1731	4.28E+09	-4.89E+08	-4.90E+08
	2289	4102	1993	1741	4.17E+09	-5.84E+08	-5.82E+08
	2187	4060	1925	1740	4.31E+09	-5.17E+08	-4.75E+08
Avg:	2222.67	4070.67	1954.00	1737.33	4.25E+09	-5.30E+08	-5.15E+08
				AVG:	4.03E+09	-6.26E+08	-6.19E+08

Calculations

Input parameters:

Δ: See in tables for deflection

D: 7.62E-2

Es: 1.06E+12

v: 0.446

Ts: 4.50E-4

Tf: Substrate 0

After 1st a-SiNx (1st) 3.00E-7

After a-Si:H (2nd) 3.50E-7

After 2nd a-SiNx (3rd) 6.50E-7

Table B.2: Deflection conversion for Substrate 1

Substrate 1					
d2-d1 (uinches)			d2-d1 (m)		
After 1st	After 2nd	After 3rd	After 1st	After 2nd	After 3rd
1627	-387	-728	4.13E-5	-9.838E-6	-1.85E-5
1780	-305	-601	4.52E-5	-7.75E-6	-1.53E-5
1556	-406	-713	3.95224E-5	-1.03E-5	-1.81E-5
1654.33	-366	-680.67	4.20E-5	-9.29E-06	-1.73E-5

Table B.3: First parameter calculations for Substrate 1

After 1st a-SiNx		
$d/(D/2)^2$	$Es/3(1-\nu)$	Ts^2/Tf
2.85E-02	1.94823E+11	6.75E-01
3.11E-02		
2.72E-02		
2.89E-02		

Table B.4: Second parameter calculations for Substrate 1

After a-Si:H		
$d/(D/2)^2$	Es/3(1-v)	Ts^2/Tf
-6.77E-03	1.94823E+11	5.79E-01
-5.34E-03		
-7.10E-03		
-6.40E-03		

Table B.5: Third parameter calculations for Substrate 1

After 2nd a-SiNx		
$d/(D/2)^2$	Es/3(1-v)	Ts^2/Tf
-1.27E-02	1.94823E+11	3.12E-01
-1.05E-02		
-1.25E-02		
-1.19E-02		

Calculations for Substrate 2

Table B.6: Deflection conversion for Substrate 2

Substrate 2					
d2-d1 (uinches)			d2-d1 (m)		
After 1st	After 2nd	After 3rd	After 1st	After 2nd	After 3rd
1858	-248	-461	4.72E-05	-6.3E-06	-1.2E-05
1813	-296	-548	4.61E-05	-7.5E-06	-1.4E-05
1873	-262	-447	4.76E-05	-6.7E-06	-1.1E-05
1848.00	-268.67	-485.33	4.69E-05	-6.8E-06	-1.2E-05

Table B.7: First parameter calculations for Substrate 2

After 1st a-SiNx		
$d/(D/2)^2$	Es/3(1-v)	Ts^2/Tf
3.25E-02	1.95E+11	6.75E-01
3.17E-02		
3.28E-02		
3.23E-02		

Table B.8: Second parameter calculations for Substrate 2

After a-Si:H		
$d/(D/2)^2$	Es/3(1-v)	Ts^2/Tf
-4.34E-03	1.95E+11	5.79E-01
-5.18E-03		
-4.58E-03		
-4.70E-03		

Table B.9: Third parameter calculations for Substrate 2

After 2nd a-SiNx		
$d/(D/2)^2$	Es/3(1-v)	Ts^2/Tf
-8.07E-03	1.95E+11	3.12E-01
-9.59E-03		
-7.82E-03		
-8.49E-03		

Appendix C

Publications and Reported Conferences

- **TFTs with High Overlay Alignment for the Fabrication of Flexible Display Backplanes**
  Journal of Display Technology, IEEE, In progress
- **A-Si:H TFT backplanes with reduced overlay misalignment on flexible substrates at low temperatures**
  Engineering Conferences International, Spring 2010
- **Lithographic misalignment reduction for TFT backplane fabrication on transparent plastic substrates**
  Materials Research Society, Spring 2010

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