ITO/a-Si:H Photodiode and Thin Film Transistor for Optical Imaging

by

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Abstract

This dissertation deals with an a-Si:H photodiode (ITO/a-Si:H) and an a-Si:H thin film transistor which are pixel components in a large area imaging array. A low temperature process to deposit polycrystalline ITO has been developed. ITO films were characterized in terms of their degree of crystallinity, transmittance, and resistivity. The ITO/a-Si:H interface integrity was studied by measurements of oxygen and indium distributions.

An ITO/a-Si:H Schottky photodiode was designed and fabricated with low leakage current and high stability. The photosensitivity was improved by optimizing the a-Si:H thickness and the geometry of collection electrode. The mechanism underlying the leakage current was studied. It was concluded that the increase in the leakage current was due to oxgyen diffusion rather than indium if the ITO was annealed at high temperature (260 °C). X-ray detection was achieved by coupling a phosphor film with the photodiode.

The stability and the leakage current of the a-Si:H TFT are two issues for large area imaging or display applications. In this dissertation, the effects of passivation a-SiN$_x$:H on TFT performance was studied by the variation of a-SiN$_x$:H composition. a-SiN$_x$:H was deposited to yield either silicon- rich or nitrogen- rich film by varying the deposition gas ratio of NH_3/SiH_4. The measurements indicated that the shift in V_T and the leakage current were minimal with nitrogen- rich a-SiN$_x$:H films.

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Chapter 1

Introduction

Digital imaging technology is experiencing strong growth for both optical and X-ray signals. Two groups of system are currently available for large area imaging applications. The first group comprises linear imaging systems. such as photocopiers. fax machines. and scanners. These systems implement linear sensor arrays to image the object of interest. The other group comprises two dimensional (2-D) systems. such as optical/video cameras for optical imaging and imaging intensifier tubes (IITs) for X-ray imaging. These systems are built up by CCD or CMOS imaging chips coupled with the optical lens. to transfer the large-area information to the small sensitive area.

In both linear and 2-D systems. the basic imaging unit is called a pixel which consists of an image sensor and a switch. One of the basic and most widely used pixel configurations is shown in Fig. 1.1. Here. each pixel consists of a field effect transistor (FET). in metal oxide field effect transistor (MOSFET) technology or thin film transistor (TFT) technology. which is connected to an optical sensor (photodiode here) and to the matrix of gate and data lines. In this scheme. the

Bias

Photodiode

D **Storage node**

G **Switch**

Gate line

S

Output, to data line
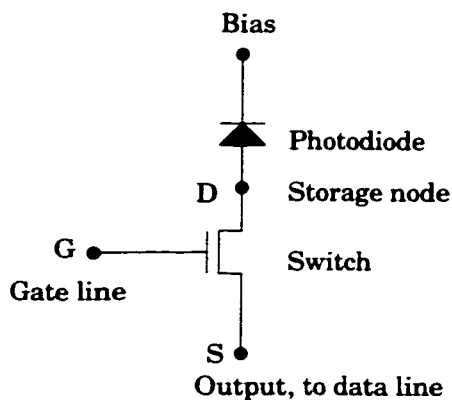
Figure 1.1: The pixel schematic where storage mode is employed.

small amount of photogenerated charges in the photodiode can be integrated over a long time interval to yield a large signal. When a voltage pulse is applied to the gate line. the charges in the photodiode are transferred to the data line where they are detected by a charge sensitive amplifier. This readout mode is called storage or integration mode [1].

Imaging array architectures based on crystalline silicon technology are introduced in Section 1.1. a-Si:H imaging technology is discussed in Section 1.2 to compare with the crystalline counterpart. Motivation of this research is given in Section 1.3 in terms of development of large area imaging systems. Section 1.4 describes the organization of this dissertation.

1.1 Imaging Array Architectures

Linear Imaging System

The configuration for a linear imaging array is shown in Fig. 1.2 [2]. Each block has only one readout line but a high density of pixels. The source electrodes of

all FETs in each block are connected to a single readout line. However, only one FET in each block is switched on at a time. The FET in one block is switched sequentially with the corresponding FETs in the other blocks. The output data of the blocks are scanned by a multiplexing chip. In this structure, there are no crossovers between signal lines due to the sequential scanning and therefore a much better performance can be achieved.
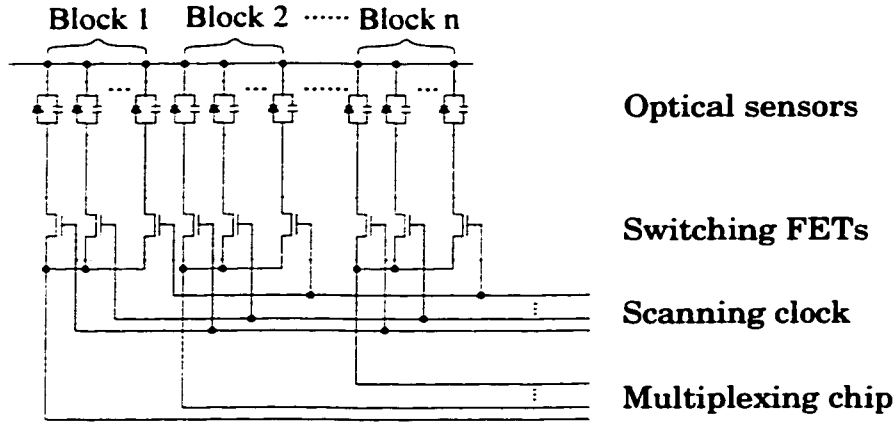
Figure 1.2: Architecture of linear imaging array.

Two-dimensional Imaging System

A 2-D imaging array with an active matrix readout is shown in Fig. 1.3 [3] [4] [5]. The FET in each pixel acts as an electronic switch with three electrical connections - drain, source, and gate. The drain is connected to the photodiode, the source is connected to a data line which is routed to an external charge sensitive amplifier, and the gate is connected to the scanning clock generator to control the charge transfer from the drain to the source. The gates for all the pixels in the same row are connected to a common scanning control line. All the pixels of the same column share a common data line and an amplifier. The readout of the entire detector can

be performed in real-time. thus permitting the creation of 2-D images.
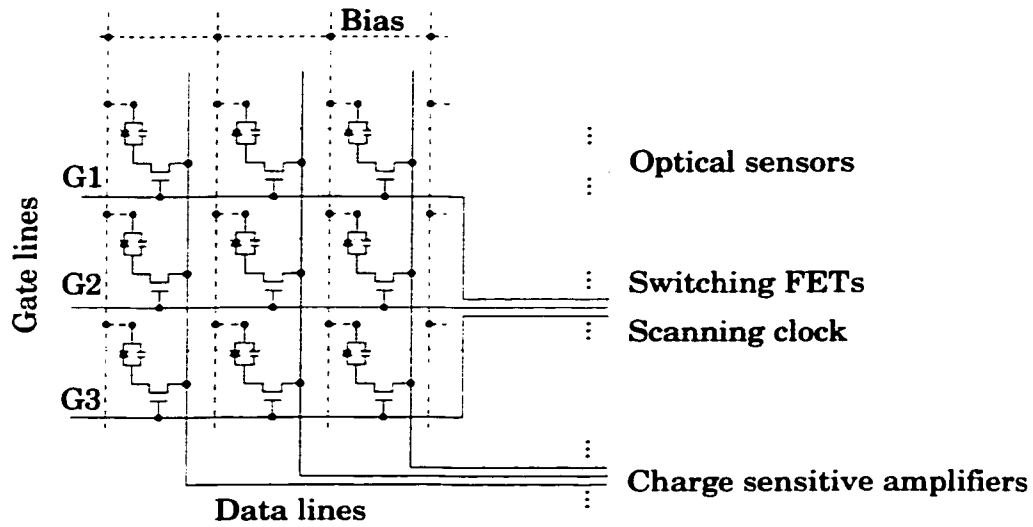
Figure 1.3: Architecture of 2-D imaging array.

The 2-D imaging process is described as follows:

- The scanning clock selects one row of **FET** switches and turns on all the switches in this row.

- The charges on each photodiode are discharged from the photodiode to the input of (external) amplifier through the **FET** switch.

- The clock trailing edge turns off the switch.

- The signal at the amplifier input is transferred to the amplifier output.

- The reset signal resets the amplifier input to zero.

- The above procedure is repeated for the next row until all rows are scanned.

The signal readout is then transmitted to the image processor for data analysis and video display.

1.2 a-Si:H Imaging Technology

Recently. optical and X-ray imaging using hydrogenated amorphous silicon (a-Si:H) technology have gained great promise. Here. the a-Si:H photodiode is used as the image sensor and the a-Si:H TFT as the switch. a-Si:H technology enables the easy manufacture of large-area electronics at low temperatures ($\sim$250 °C) [6] in contrast to the single-crystal (CCD or CMOS) technology. which imposes restrictions in terms of either higher cost or limited detectable area. The a-Si:H fabrication process is borrowed from IC technology. Moreover. since a-Si:H is in a state of greater disorder. it could be expected to be considerably less sensitive to radiation damage than its single-crystal counterpart. and induced radiation damage can be annealed at low temperature (for example. 150 °C) as well. Image sensor technologies of c-Si and a-Si:H are compared in Table 1.1. For example. a 19.5×24.4 cm^2 a-Si:H two-dimensional (2-D) imaging system with a pixel size of 127 μm has been recently demonstrated [7]. with a clear potential for higher quality. speed. and resolution.

Table 1.1: Image sensor technologies.

	c-Si	a-Si:H
Sensitivity to visible light	Yes	Yes
Response time	10 to 100 ps	500 to 1 μs
Homogeneity	Crystalline	Amorphous
Radiation resistivity	No	Yes
Large area compatibility	No	Yes (Linear/2D)
Maximum area (cm^2)	5.5×5.5	40×40

1.3 Motivation

1.3.1 Development of Optical Sensors

The ultimate goal of this research is to achieve large area imaging system using a-Si:H technology. Because of the low photosensitivity. the storage mode must be used. Therefore. the leakage current of the detector is required to be as low as possible to decrease the background signal and to increase the dynamic range. There are typically three types of optical sensors: photoconductor. photodiode. and photo TFT. As listed in Table 1.2. the leakage current of the diode structures is lower than those of the conductor and photo-TFT structures. In diode structures. the leakage current is higher in a Schottky structure than in a pin structure. However. in many applications. a leakage current of 10^{-10} A/cm^2 is low enough [8] to achieve an imaging system with 30 frame per second (fps). Therefore. the Schottky structure can still be a candidate if its leakage current can be further reduced. Table 1.3 shows the progress in development of Schottky photodiodes. In this work. we adopt the Schottky photodiode as the image sensor structure following our in-house fabrication infrastructure.

As the a-Si:H Schottky photodiode is operated under reverse bias. the shift in leakage current with time can be a major concern. In this work. the mechanisms underlying the leakage current and the interface integrity are examined.

The a-Si:H photodiode has higher photosensitivity compared to the c-Si photodiode because of its high absorption efficiency for visible light with the wavelength less than 700 nm. When used in X-ray imaging. however. the optical irradiation level is low and the photosensitivity still needs to be improved. In this work. the change in photosensitivity with the active layer and the geometry of collection

Table 1.2: Performance comparison of various a-Si:H image sensors.

	Photo conductor	Schottky diode	pin diode	photo TFT
Photo sensitivity	High	Low	Low	High
Response time (μs)	Slow ~ 500	Fast ~ 50	Fast < 5	Slow ~ 500
Dark current (A/cm^2)	~ 10^{-6}	10^{-7} to 10^{-9}	10^{-10} to 10^{-12}	10^{-7} to 10^{-8}
Stability	Good	Good	Good	Acceptable
Large area compatibility	Yes	Yes	Yes	Yes

Table 1.3: Progress in development of ITO/a-Si:H Schottky photodiodes.

Year	I_{photo} (A/cm^2)	I_{dark} (A/cm^2)	$\frac{I_{photo}}{I_{dark}}$	Stability	Response time (μs)	Quantum efficiency	Ref.
1981	10^{-5}	$(2\sim6)\times10^{-9}$	> 3000	N/A	< 500	0.7	[9]
1985	N/A	$10^{-7} \sim 10^{-8}$	1000	Very good	< 2	N/A	[10] [11]
1986	$(0.6\sim1)$ $\times10^{-5}$	5×10^{-9}	3000 ~ 10000	N/A	< 50	N/A	[12]
1992	N/A	1×10^{-9}	N/A	N/A	N/A	N/A	[4]

electrode is considered.

1.3.2 Study of Stability and Leakage Current of Thin Film Transistors

The other element in large area detection is the switch. which is used to control the signal readout from the detector to the data line. Currently both diode and TFT are used. A switch diode is a two-terminal device which can be fabricated simultaneously with a detector with fewer mask steps and a simpler connection technology. The problems associated with this element are the higher capacitance and nonlinear current-voltage characteristics. In order to overcome these obstacles. advanced addressing schemes are introduced but with more diodes [13]. The other switching element is the thin film transistor. Thin film transistors are more widely used because they provide low capacitance. linear switching characteristics. and low leakage current [14]. However. the shift in V_T in an a-Si:H TFT is the key challenge

and the study of the underlying mechanisms is one of the subjects of this research.

TFTs are used as analog switches to transfer the photogenerated signals to the data lines. Therefore. the instability of TFTs (the shift in threshold voltage with bias) must be reduced to the minimum. This instability has been attributed to the bulk defect generation in the active a-Si:H layer and charge injection into the gate insulator layer. In this research. we focus on the effects of top (passivation) a-SiN$_x$:H on the shift in V$_T$ with time.

1.3.3 Integration of Photodiode and Thin Film Transistor

In this research. the integration of the a-Si:H detector (Schottky photodiode) and TFT for large area imaging applications is one of the intended goals. In fabricating photodiodes and TFTs. some steps are common. for example. the bottom electrode for photodiodes and gate electrode for TFTs. and the aluminium layers for the wire bonding. However. there are some different steps. For example. although both of the active layers for photodiodes and TFTs are a-Si:H but their thicknesses are different (about 1 μm for a photodiode and 500 $\mathring{A}$ for a TFT). In this work. the fabrication feasibility is demonstrated.

1.4 Organization of Dissertation

Chapter 2 addresses various material issues with the perspective of achieving optimum performance of ITO/a-Si:H Schottky photodiodes and TFTs. For the Schottky photodiode. the optimization of the transparent material. which is used as metal contact and light window. in terms of structure. transmittance. and resistivity. needs to be considered. In this work. indium tin oxide (ITO) with polycrystalline

structure was deposited at low temperature to improve the quality of the interface between the ITO and the a-Si:H. The effects of deposition conditions on ITO film quality are discussed in Chapter 3. Development of the ITO/a-Si:H Schottky photodiode is presented in Chapter 4 based on the ITO material described in Chapter 3. The device is characterized in terms of the leakage current (and its variation with time). photosensitivity. and spectral response. The interface integrity is characterized in terms of diffusion profiles of oxygen and indium by SIMS measurements and correlated with leakage current measurements. to gain insight into the mechanisms underlying leakage current. The X-ray sensitivity with various X-ray source voltages is measured for a photodiode coupled with a phosphor layer. A study of thin film transistors is given in Chapter 5. where we focus on the effects of the passivation layer on the TFT performance. in particular. its stability and leakage current. In Chapter 6. the integration of the photodiode and TFT is considered. The contributions of this research are presented in Chapter 7.

Chapter 2

Summary of Materials and Properties Relevant to a-Si:H Imaging Technology

The performance of both optical sensors and TFTs is determined by material properties and the associated interface integrity. In order to provide a basis for the optimization of the device characteristics. we will first review relevant materials in a-Si:H imaging technology. These materials include a-Si:H. a-SiN$_x$:H. n$^+$ a-Si:H. metals. and phosphor.

2.1 a-Si:H

Hydrogenated amorphous silicon is a silicon network with long range disorder. The preservation of short range order results in a similar overall electronic structure of the amorphous material compared to the crystalline silicon (c-Si). The comparison

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of electrical properties for c-Si and a-Si:H is summarized in Table 2.1.

Table 2.1: Characteristics comparison of c-Si and a-Si:H

	c-Si	a-Si:H
Bandwidth (eV)	1.1	1.6-2.0
Conductivity (S cm^{-1})	4×10^{-6}	10^{-8} - 10^{-12}
Electron mobility (cm^{2}V^{-1}s^{-1})	10^3	1.0
Hole mobility (cm^{2}V^{-1}s^{-1})	10^2	10^{-3}-10^{-2}
Permittivity	11.9	~11.9
Diffusion length of electron (μm)	300	< 10
Diffusion length of hole (μm)	200	~ 0.1
Average lifetime of electrons (s)	2.5×10^{-3}	10^{-6}
Average lifetime of holes (s)	2.5×10^{-3}	10^{-6}

In this section. the deposition of a-Si:H films is discussed in terms of growth mechanism and the effects of process conditions on the film quality. a-Si:H properties including optical. transport. and metastability are summarized. The effects of material properties on the performance of photodiodes and TFTs will be discussed in Chapter 4 and Chapter 5. respectively.

2.1.1 PECVD Deposition

The a-Si:H can be prepared using conventional low pressure chemical vapor deposition (LPCVD). photo CVD. and plasma enhanced CVD (PECVD). PECVD yields low defect density and has evolved to become the industrial standard. Our PECVD is a capacitively coupled electrode system (see Fig. 2.1. Model: Plasma-therm 790).
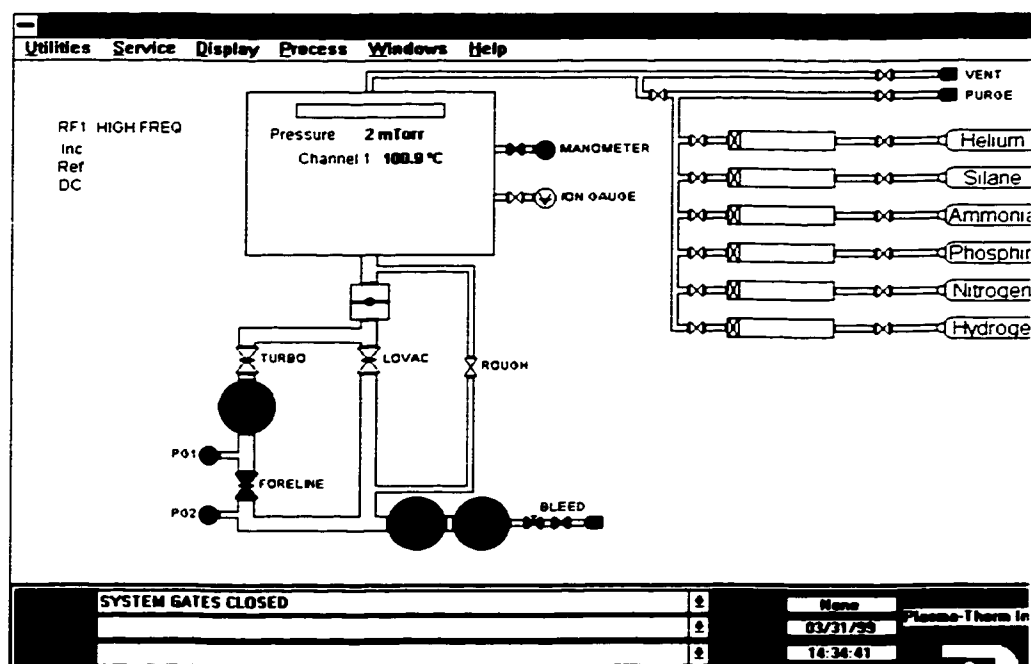
Figure 2.1: PECVD of a-Si:H and a-SiN$_x$:H schematic.

Silane (SiH$_4$) is decomposed in the chamber in the presence of a plasma. The process pressure is set by a control system to maintain the plasma. Ions and other reactive species in the plasma condense on a heated substrate (200-300°C) to form an amorphous film with incorporation of hydrogen in the film. A high concentration of Si-H bonds can be formed to passivate dangling bonds, which in turn, reduce the density of defect states.

The growth of a-Si:H can be classified as follows [15]:

1. Gas-phase processes: they involve radicals in the glow-discharge plasma and radicals to the film-growing surface. The gas-phase processes determine the arriving species on the film-growth surface, and can be controlled by many external parameters such as the type of source gas, gas pressure, gas flow rate, power frequency, and power density.

2. Surface reactions on growing surface: they are controlled by temperature and the arriving species. which determine the resulting micro-structure of the films.

The main reactions associated with film growth are:

$$SiH_4 = SiH_3 + H. \tag{2.1}$$

$$SiH_3 = SiH_2 + H. \tag{2.2}$$

$$SiH_2 = SiH + H. \tag{2.3}$$

$$SiH = Si + H. \tag{2.4}$$

Undoped a-Si:H is. however. not an "ideal" intrinsic semiconductor. Its dark conductivity activation energy is less than half of the optical gap and it shows a slightly n-type electrical behavior due to the smaller density of tail states near the conduction band and more electrons available as a result.

The effect of deposition parameters on i-a-Si:H quality is given in Table 2.2. Here. Ar dilution is also included (with low concentration). In a-Si:H deposition. the temperature is the most important parameter responsible for high quality. The low temperature (< 350 °C) prevents film from forming silicon crystal grains and maintains necessary hydrogen content. The deposition temperature is about 250 °C and an rf power density is about 10 mW/cm^2 for low defect density and high hydrogen concentration in our process. The deposition pressure is about 0.1 to 1 torr to minimize the voltage necessary to sustain the plasma. The concentration of hydrogen was measured to be 15% and the defect density was measured to be 10^{16} cm^{-3} [16].

Table 2.2: The effect of deposition parameters on the quality of a-Si·H.

	Defect density	Hydrogen concentration	Deposition rate
Temperature ↑ (200 - 400 °C)	Minimum at 250 °C	↓	↑
rf power density ↑	↑	Maximum at about 10 mW/cm² *	↑ (high gas concentration)
Gas concentration ↑ (SiH₄+Ar)/SiH₄	↓	↑	↑
Process pressure ↑ (0.1 to 0.5 torr)	↓	↑	↓

*Depending on the geometry of the electrodes and the size of the chamber [17].

2.1.2 Optical Properties

When a-Si:H is used in an optical sensor. its optical properties are of main interest. Fig. 2.2 shows the optical absorption spectrum. which can be roughly divided into three regions [18]: the high absorption region A ($\alpha > 10^3$ cm^{-1}). the exponential edge B ($10^1 < \alpha < 10^3$ cm^{-1}). and the weak absorption tail C ($\alpha < 10^1$ cm^{-1}).

The optical transition region A corresponds to electron excitation from the valence to conduction band mobility edge. This region is usually described by the Tauc expression:

$$(\alpha h \gamma)^{1/2} = B_0 (h\gamma - E_{0T}).$$ (2.5)

where B_0 is the constant containing an average matrix element. E_{0T} is the constant

energy. h is Planck's constant ($= 6.63 \times 10^{34}$ Nms). and γ is the optical frequency.

The region B shows an exponential variation of α with hγ:

$$\alpha = \alpha_0 e^{(h\gamma/E_c)}. \qquad (2.6)$$

where α_0 is the constant and E_c is the characteristic energy which represents the slope of the exponential tail. The exponential tail of the valence or conduction band reflects the randomness of the amorphous network.

The weak absorption tail of region C is attributed to the deep states in the mid-gap. mostly originating from the presence of defects and impurities.
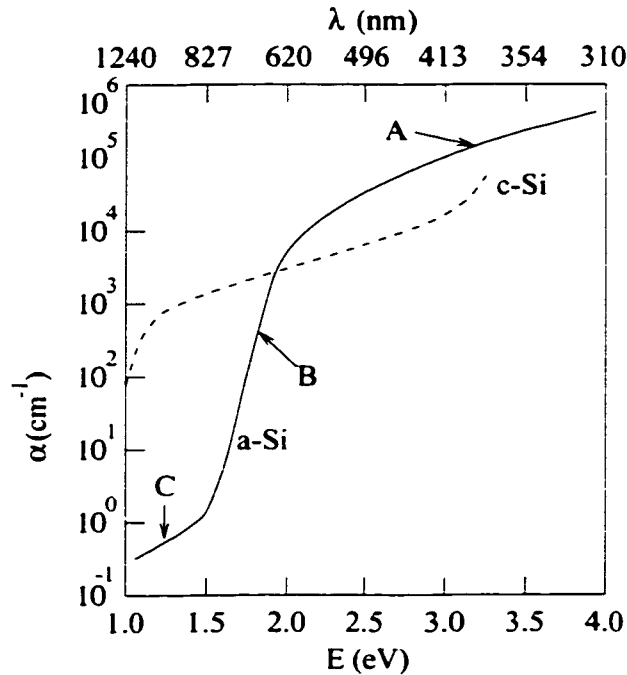
Figure 2.2: Optical absorption spectra of c-Si and undoped a-Si:H films (regions A. B. and C are described in text). Adapted from [18].

In a-Si:H. the abrupt band edges of a crystal are replaced by a broadened tail of states extending into the forbidden gap due to the deviations of the bond length

and angle arising from the long range structural disorder. Essentially the localized states in the amorphous silicon can be divided into two types: tail states and deep states. The tail states are formed by strained Si-Si bonds near the conduction or valence bands. They are localized by the disorder to form a "tail" of localized states just below the conduction band mobility edge and above the valence band mobility edge. The deep states originate from defects in the amorphous silicon network. These defects are considered to consist mostly of silicon dangling bonds. which have a wide range of energy because of the variations in the local environment. The schematic density of states distribution for a-Si:H is shown in Fig. 2.3.
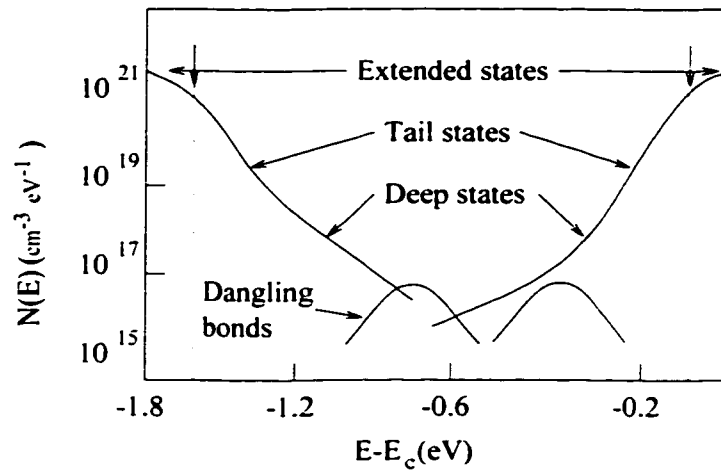
Figure 2.3: Density of states in a-Si:H.

Photoconductivity occurs when carriers are optically excited from the non-conducting to conducting states. The illumination excites electrons and holes to the band edges where they are drifted towards the electrodes by the applied electric fields. This phenomenon can be described by the following three processes:

- Generation of electron-hole pairs by an external source.

- Transport of mobile carriers by either extended or localized states.

• Recombination of the excited electron and hole.

The signal resulting from optical excitation in a semiconductor is proportional to the absorbed energy [19]:

$$Q = Eq/\varepsilon. \tag{2.7}$$

where Q is the charge produced (Coulomb). E is the absorbed energy (eV). q is the electronic charge (= 1.6×10^{-19} Coulomb). and ε is the average energy required to produce a hole-electron pair (eV/hole-electron pair). The value of ε (which represents the effective conversion efficiency) depends on the details of the interaction mechanism in the detector material. Not all the incident energy is used to produce ionization (to give a signal) – some is wasted in producing vibrations in the atoms and cannot be recovered. Therefore ε depends on the material and temperature.

2.1.3 Transport Properties

In the amorphous silicon. carriers transport in several processes (see Fig. 2.4). which can be summarized as the following conduction mechanisms [20]:
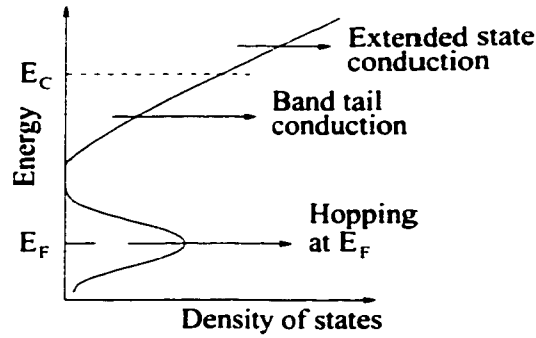
Figure 2.4: Three main conduction mechanisms expected in an amorphous semiconductor.

- **Extended state conduction**

Conduction is by thermal activation of carriers from E_F to above the mobility edge and follows the relation.

$$\sigma_{ext} = \sigma_{oc} e^{\frac{-(E_C - E_F)}{kT}} \tag{2.8}$$

where σ_{oc} is the average conductivity above the mobility edge (about 1000 $\Omega^{-1} cm^{-1}$). The activation energy is the separation of mobility edge from the Fermi energy. and varies from nearly 1 eV in undoped a-Si:H to 0.1 eV in n-type material.

- **Band tail conduction**

Although carriers cannot conduct in localized states at zero temperature. conduction by hopping from site to site is possible at elevated temperatures. Hopping conduction in the band tail is given by.

$$\sigma_{tail} = \sigma_{ot} e^{\frac{-(E_{CT} - E_F)}{kT}} \tag{2.9}$$

where E_{CT} is the average energy of the band tail conduction path. The prefactor σ_{ot} depends on the density of states and on the overlap of the wavefunction and is smaller than σ_{oc}. On the other hand. E_{CT} is closer to E_F than is E_C. so that the exponential term offsets the smaller prefactor. particularly at low temperature.

- **Hopping conduction at the Fermi energy**

Conduction at the Fermi energy occurs when the density of states is large enough for significant tunneling of electrons. The conductivity is small but weakly temperature-dependent and consequently this mechanism tends to dominate at the lowest temperature. The states at E_F usually originate from

defects and so the conductivity varies greatly with the defect density. For example. the addition of hydrogen to amorphous silicon reduces the defect density and almost completely suppresses the Fermi energy hopping conduction.

2.1.4 Metastability

The phenomenon of metastability. in which an external electronic excitation. such as light illumination. charge. current flow. and energetic particles. causes a reversible change in the density of electronic states. In the imaging application. the a-Si:H degradation from optical irradiation. which is called Staebler-Wronski effect [21]. is of main concern.

Long time exposure to light decreases the photoconductivity and increases dark conductivity of undoped and lightly doped n-type a-Si:H materials. Annealing at temperatures above 150 °C recovers the material characteristics. These observations have been explained by Staebler and Wronski that the additional localized gap states are created by light irradiation. These states can be eliminated by annealing because annealing can restore thermal equilibrium which is disturbed by the external excitation.

The bias effect also needs to be considered because an optical sensor is operated under reverse bias. The bias voltage causes the shift in quasi Fermi level and modifies the density of interface states. Both photocurrent and dark current which can be affected by interface states would change accordingly.

2.2 a-SiN$_x$:H

Silicon nitride (a-SiN$_x$:H) is an amorphous 4:3-coordinated random network which also contains hydrogen as an important impurity. Its bandgap is about 5.3 eV if prepared by PECVD with a mixture of SiH$_4$ and NH$_3$ during deposition. The Si dangling bond gives a state near midgap while a Si-Si bond and the negative N$^-$ center introduce gap states just above the valence band edge. The band structure of a-SiN$_x$:H is shown in Fig. 2.5.

Density of states
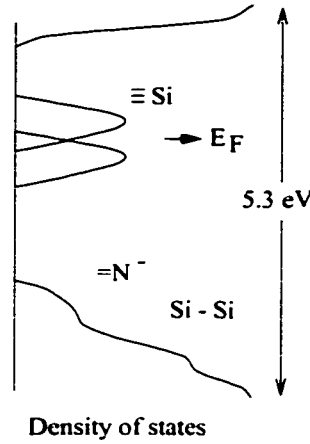
Figure 2.5: a-SiN$_x$:H band structure indicating the states within the band gap ($\equiv$Si: dangling bonds. =N$^-$: negative N dangling bond. Si-Si: silicon silicon weak bond). Adapted from [22].

a-SiN$_x$:H is used in TFTs as a gate insulator and a passivation layer due to its good interface with a-Si:H. The a-SiN$_x$:H with wide band gap is required in TFTs. The band gap can be controlled by deposition conditions. For example. the band gap is large if the a-SiN$_x$:H is nitrogen rich while the band gap is small if the a-SiN$_x$:H is silicon rich. The content of nitrogen and silicon in the a-Si:H film can be changed by varying deposition gas ratio of NH$_3$/SiH$_4$. As reported [23]. nitrogen to

silicon ratio (x) in a-SiN$_x$:H changes with deposition gas ratio from 0.9 to 1.6. and the a-SiN$_x$:H bandgap changes from 1.7 to 5.6 eV when NH$_3$/SiH$_4$ gas ratio changes with H$_2$ dilution. When the a-SiN$_x$:H changes from Si-rich to N-rich. the density of defect states decreases due to the reduced number of dangling bonds in the N-rich film. Therefore. nitrogen-rich a-SiN$_x$:H is preferred for both gate insulator and top passivation layers.

In this section. the deposition of a-SiN$_x$:H is discussed in terms of growth mechanism and the effects of process conditions on the film quality. The process optimization of the a-SiN$_x$:H and its effects on the TFT performance will be discussed in Chapter 5.

a-SiN$_x$:H is also prepared using PECVD with the supply of SiH$_4$ and NH$_3$ gases. SiH$_4$ and NH$_3$ react in the chamber in the presence of plasma. In order to decompose the NH$_3$ gas. a high plasma power is required compared to the deposition of a-Si:H. In our process. the deposition power with one order of magnitude higher is used.

The effect of process parameters on a-SiN$_x$:H quality is given in Table 2.3. Here. a high temperature process is preferred for a high quality film. However. the other processes and substrate constraint allow a-SiN$_x$:H to be deposited below 350 °C. The optimal deposition conditions in our process are as follows: rf power density at 100 mW/cm^2. process pressure at 400 mtorr. temperatures at 320 °C for TFT gate insulator and at 260 °C for TFT passivation or etch protection layers. The gas ratio is varied to yield either silicon- or nitrogen- rich a-SiN$_x$:H films. When NH$_3$/SiH$_4$ gas ratio is 20. the defect density is 10^{17} cm^{-3} at the deposition temperature of 260 °C) and 10^{16} cm^{-3} at 320 °C.

Table 2.3: The effect of deposition parameters on the quality of a-SiN$_x$:H.

	Defect density	Hydrogen concentration	Deposition rate
Temperature ↑	↓	↓	↑
rf power ↑	↑	↓	↑
Gas ratio of NH$_3$/SiH$_4$ ↑	↓	↑	Maximum at 10
Process pressure ↑	↓	↑	↓

2.3 n$^+$ a-Si:H

2.3.1 Doping Mechanism

Highly doped materials such as n$^+$ a-Si:H and n$^+$ μC-Si:H are used to establish ohmic contact between the intrinsic a-Si:H and the metal electrode in image sensors and TFTs. The addition of a small quantity of phosphine (up to a few percent) to the deposition gas results in a change in the room temperature conductivity. up to a factor of 10^8. Due to the low doping efficiency. the defect density in the a-Si:H increases significantly. The doping efficiency can be described as [20]

$$\eta = \frac{N_{BT} + N_{deep}}{N_{total}}. \tag{2.10}$$

where N$_{deep}$ is the density of states which can take an extra electron from the donor and N$_{BT}$ is the density of electrons occupying shallow states near the band edge.

The most popular method in preparing n$^+$ a-Si:H and n$^+$ μC-Si:H films is by mixing PH$_3$ with SiH$_4$ as feeding gases. Hydrogen dilution is also introduced in some cases to increase the film conductivity. especially for a low temperature process

[24]. The n^+ film contains a high hydrogen concentration (higher than 20 atomic percent) and high phosphorus concentration (higher than 10^{20} cm^{-3}). By varying the deposition conditions, such as the substrate temperature, hydrogen dilution, the rf power, and the process pressure, one can deposit high quality amorphous and microcrystalline n^+ layers with different conductivities and morphologies (see Tables 2.4 and 2.5). In our process, optimal n^+ a-Si:H is obtained with substrate temperature at 250 °C, rf power density at 10 mW/cm^2, and process pressure at 150 mtorr.

Table 2.4: The effect of deposition parameters on the quality of n^+ a-Si:H.

	Defect density	Hydrogen concentration	Conductivity (Ω^{-1}cm^{-1})
Temperature ↑	Minimum at 250 °C	↓	↑
rf power ↑	↑	Maximum at about 10 mW/cm^2	↑ then saturates
PH$_3$/SiH$_4$ ↑	↑	↑	↑ then saturated at 10^{-2}
Process pressure ↑	↓	↑	↓

2.3.2 Contact Properties

For n^+ a-Si:H layer there are two major characteristics to be considered: the bulk film resistivity and the contact resistance. Both should be as low as possible. The deposition temperature is required to be kept low enough to maintain compatibility

Table 2.5: The effect of deposition parameters on the quality of n^+ μc-Si:H.

	Defect density	Hydrogen concentration	Conductivity
Temperature ↑	Minimum at 200 °C	↓	Maximum at 200 °C
rf power ↑	↑	↓	↑
PH_3/SiH_4 ↑	↑	↑	Maximum at specific value then saturates
H_2 flow rate ↑	↓	↓	↑
Pressure ↑	↓	↑	↓

with other process temperatures. The n^+ a-Si:H layer usually has a film resistivity above 100 Ω-cm. In order to further improve the ohmic contact behavior. a low resistivity film (0.1 Ω-cm) of n^+ μc-Si is introduced. However. the n^+ μc-Si develops with the first thin layer of less than 10 nm of the film in amorphous phase and the crystalline structure appears and grows afterward. Therefore. its contact resistance should not be enhanced fully by the crystalline-phase part of the film. The removal of silicon oxide by hydrogen plasma at the interface of n^+ μc-Si/a-Si:H is also considered to be a contributor.

2.4 Metals

Cr. Al. and Mo are typical metals used as electrodes in photodiodes and TFTs. Mo is not widely used because of its poor selectivity with a-Si:H wet etch. high stress, and X-ray sensitivity. Cr is used as a bottom electrode for both photodiode

and TFT. Al is the final metal for contact and pad metalization. The deposition is taken using conventional DC sputtering. The process parameters are given in Table 2.6.

Table 2.6: Sputter deposition of Cr and Al in Ar gas.

Base pressure	2×10^{-7} torr
Process pressure	20 mtorr
rf power	400 W
Rotation	10 rpm

Both Cr (resistivity: 10^{-5} Ω-cm) and Al (resistivity: 10^{-6} Ω-cm) can be used as electrode materials. A good ohmic contact can be formed between Cr and n^+ a-Si:H layers. Cr is a heavy metal and forms a good interface with a-Si:H due to its low diffusion. In addition. Cr is stable at high temperature and is resistant to the a-Si:H etchant. Therefore, Cr is a good choice for the bottom electrode. With Al as a bottom electrode. the photodiode has a larger (dark) reverse current because of Al diffusion at the interface between Al and n^+ a-Si:H. Thus. Al is used either as a top electrode or pad metalization.

The thickness of the metal layer is an important process issue because of the trade-off between high conductivity and low stress. A thick film has low resistance but can have high stress. This is a very important issue for the sandwich photodiode structure or for stacked photodiode-TFT pixel structures.

ITO is another material used as a metal contact and light window in optical sensors (ITO/a-Si:H photodiodes). The deposition and optimization of this material will be discussed in details in Chapter 3.

2.5 Phosphor

When an optical sensor is coupled with a phosphour layer. an X-ray detector can be realized. A demonstration of X-ray detection will be presented in Section 4.5.5.

Phosphor materials convert X-rays to visible light. They absorb X-ray photons and generate high energy electrons. which in turn generate electron-hole pairs in the material. Visible light is emitted when electrons and holes recombine. Phosphors enable the use of X-rays to visualize objects in real time or to record a single image.

Many phosphors are available for this conversion purpose [25]. for example. Gd_2O_2S:Tb. CsI:Tl (Cesium Iodide with Thallium activated). ZnS (Ni doped). $CaWO_4$. $Zn_{0.68}Cd_{0.32}S$. LaOBr. $Bi_4Ge_3O_{12}$. Y_2O_2S:Tb. etc. [26] [27]. A proper phosphor material must match the illumination response of a-Si:H in the visible range. As shown in Fig. 2.6. both Gd_2O_2S:Tb and CsI:Tl are good candidates.
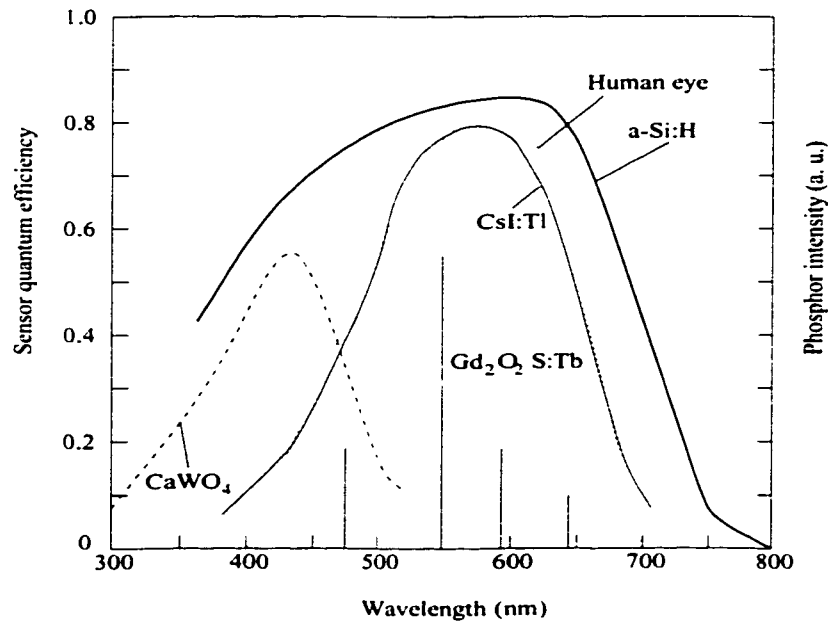
Figure 2.6: Spectral response for selected phosphor materials. Adapted from [28].

Gd_2O_2S:Tb has several characteristics convenient for X-ray imaging. One is that the X-ray attenuation coefficient is large because the effective atomic number is about 60. The X-ray-to-light conversion factor is also reasonable, up to 15 %. The light emission spectrum, which has its main peak at 550 nm, roughly conforms to the spectral sensitivity of an a-Si:H photodiode. This material is neither poisonous nor deliquescent and is chemically stable [29]. The thickness of the phosphor layer is determined by the trade-off between detection efficiency and spatial resolution [30].

2.6 Summary

In this chapter, various material issues associated with the performance of ITO/a-Si:H photodiodes and a-Si:H TFTs were addressed. Those issues include the film growth mechanisms, the effects of process conditions on the film quality, and the relevant film properties.

Chapter 3

Deposition of Polycrystalline Indium Tin Oxide at Low Temperature

Indium tin oxide (ITO) is a n-type semiconductor material with a direct band gap of about 3.7 eV [31]. Its high transmittance in the visible spectrum (400-800 nm) and low electrical resistivity (free electron density larger than 10^{20} cm^{-3} [32]) allow this material to be widely used in solar cells. flat panel displays. and image sensors as a conducting layer and a light window. In image sensor applications. an ITO film that is polycrystalline in structure is needed in order to ensure high transmittance and device stability. Such a material structure can be obtained at deposition temperatures above 150 °C. But. when it is used in an ITO/a-Si:H diode (usually referred as Schottky structure due to the high conductivity of the ITO film). high deposition temperature (> 200 °C) causes the diffusion of indium and oxygen from the ITO into the a-Si:H layer. thereby degrading device performance

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[33]. Thus deposition of ITO at non-elevated temperature is crucial. however. the deposited films tend to be amorphous in structure with very weak crystallinity. One method to increase the crystallinity of ITO at non-elevated temperature is to introduce O_2 or H_2O in the sputtering gas [34] [35]. But. because of partial pressure considerations. the control of film resistivity is very limited [36]. This leads to a narrow process tolerance. In addition. the presence of extra O_2 or H_2O causes the formation of high density of positively charged states at the Schottky interface [37] [38]. These states trap photogenerated electrons and holes. and result in an increase in both the dark current and photodiode instability. Therefore. an in-depth study on the growth of ITO is imperative for the optimization of ITO/a-Si:H Schottky photodiodes. This constitutes the focus of this chapter.

A standard rf sputtering system was used in the deposition (see Fig. 3.1) in this work. Before each sputtering cycle. the base pressure was set to be less than 2×10^{-6} torr and the (three-inch diameter) target was pre-sputtered for about 3 minutes. The ITO target (90 wt.% In_2O_3 and 10 wt.% SnO_2) was supplied by Cerac Inc.. USA. with a purity of 99.999%. Pure Ar with a purity of 99.999% was used as the sputtering gas. In order to study the spatial variation in film characteristics. the wafer was placed at different positions on the substrate holder: A. B. C. and D. Here. A was about 20 mm away from the center of the substrate holder and the positions were separated by 35 mm (see Fig. 3.1). The distance between the substrate and sputtering target was 15 cm. The process pressure was 15 mtorr and the rotation speed was 10 rpm. The substrate was not heated during the depositions and the substrate temperature associated with the heating by the plasma was measured to be less than 40 °C. The sputtering power was varied at 200 W. 300 W. and 400 W. The corresponding voltages were -717 V. -865 V. and -1026 V. respectively.
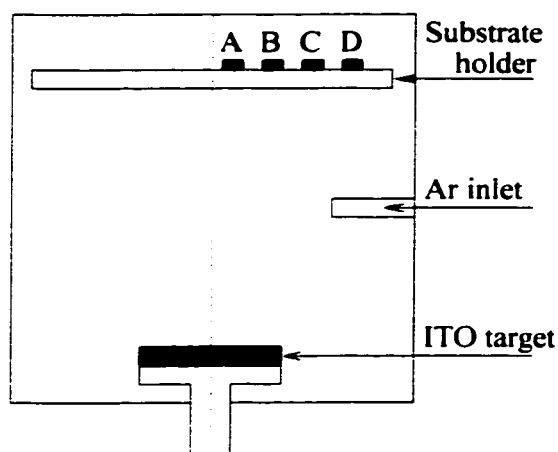
Figure 3.1: Schematic of a CVE system.

The ITO deposition rate varied with rf power due to the associated energy change of sputtering species. By measuring the film thickness using a Dektek profiler. the sputtering rate was calculated to be 55 $\mathring{A}$/min at 300 W and its linear dependence upon rf power is shown in Fig. 3.2.

The properties of ITO films are governed by the nano-structure of the film. which can be controlled by process parameters such as sample position. annealing temperature. sputtering power. and process pressure. In this chapter. we present a systematic characterization of the ITO in terms of its crystallinity in structure. optical transmittance. and electrical conductivity. Interface properties with a-Si:H will be discussed in Chapter 4.
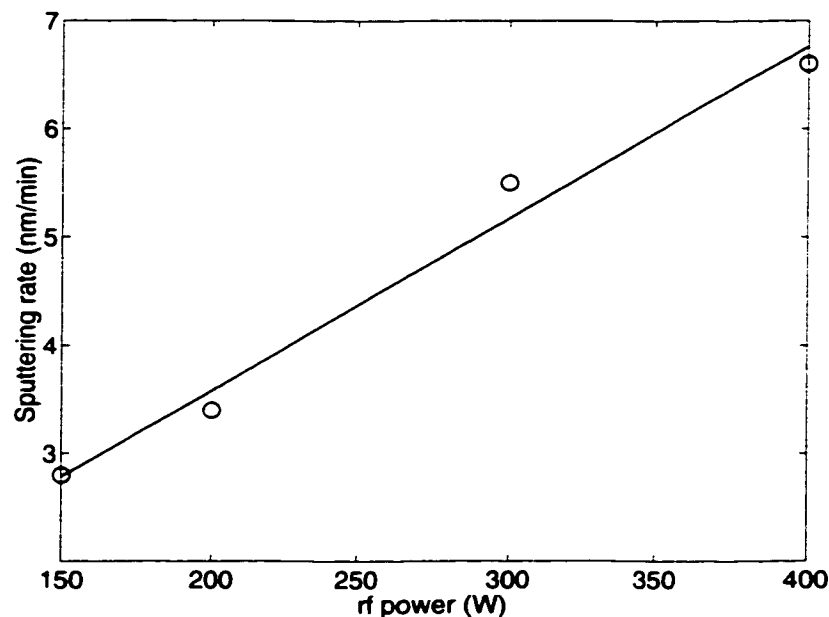
Figure 3.2: ITO deposition rate vs rf sputtering power.

3.1 Crystallinity

3.1.1 Low Temperature Crystallization

To determine the film nano-structure. X-ray Diffraction (XRD) measurements were performed with a Nicolet-12 diffractometer (Cu radiation. 30 kV. and 20 mA).

Fig. 3.3 shows the XRD measurement for ITO deposited at low temperature with the sputtering power at 300 W. The film features a strong <222> peak and confirms the polycrystalline structure [39].

Whether or not we can achieve a polycrystalline ITO depends on the growth mode in the film. A 2-D layer-to-layer growth mode (referred to as Frank-van de Merve mode) results in polycrystalline structure while a 3-D island growth mode (referred to as Volmer-Weber mode) results in amorphous structure. As previously
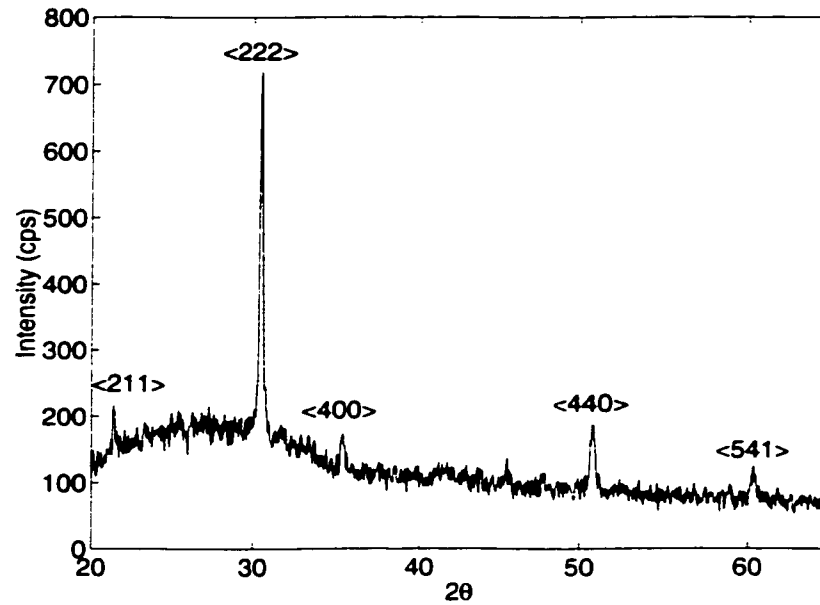
Figure 3.3: XRD pattern for ITO films deposited at low temperature (rf power: 300 W and film thickness: 220 nm).

reported [40] [41] [42]. the 3-D growth mode occurs at low temperature (below 100 °C) while the 2-D growth mode happens at high temperature (above 150 "C). The transition in growth modes has been reported to happen at around 150 °C. Our results show that this transition can also happen at a lower temperature. In order to gain the insight of underlying mechanism. the crystallinity of ITO placed at different positions is measured (see Fig. 3.4). We observed that. at positions A and B. there is a strong presence of <222> peaks. At position C. the film crystallinity is very weak and it is amorphous in structure at position D. The above results of XRD patterns for the samples at positions A and B indicate that an ITO film with polycrystalline structure can be deposited at low temperature. This change in structure can be attributed to the supply of sputtering species. Rutherford back scattering (RBS) experiments were used to measure the oxygen and indium-tin
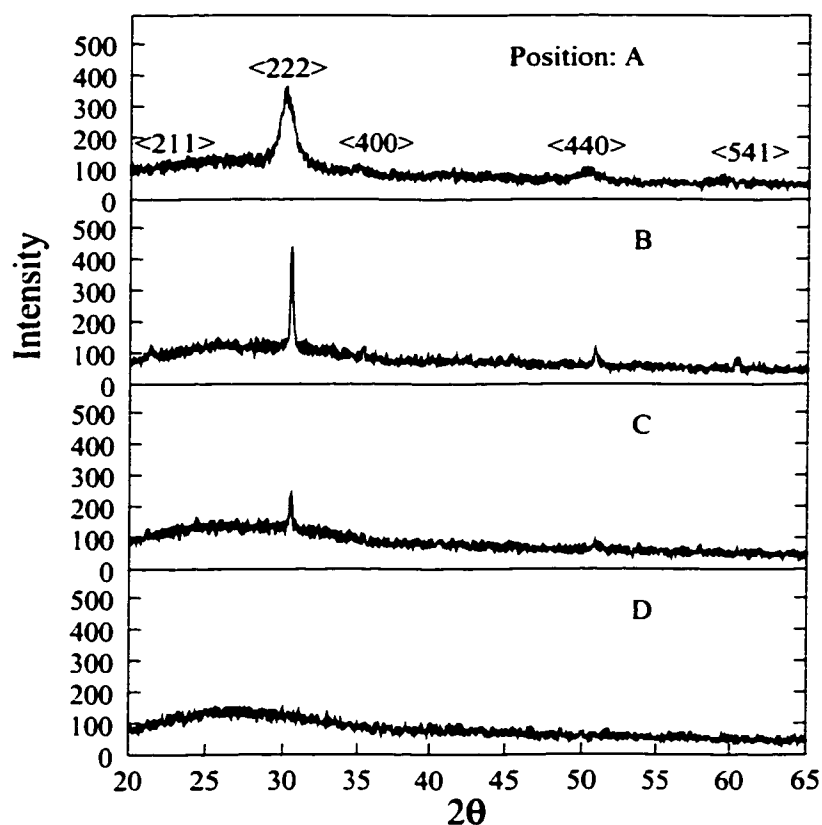
Figure 3.4: The change of film crystallinity for different positions. The sputtering power is 300 W.

distributions in the film (see Fig. 3.5). As observed. the oxygen and indium-tin have similar distributions independent of the substrate position. Near the middle (for example. at A). the contents are lower than those at position B. but higher than those at positions C or D. The distribution of sputtered elements (O. In-Sn) is consistent with the presence of the <222> peak with the substrate position in going from the middle to the edge.
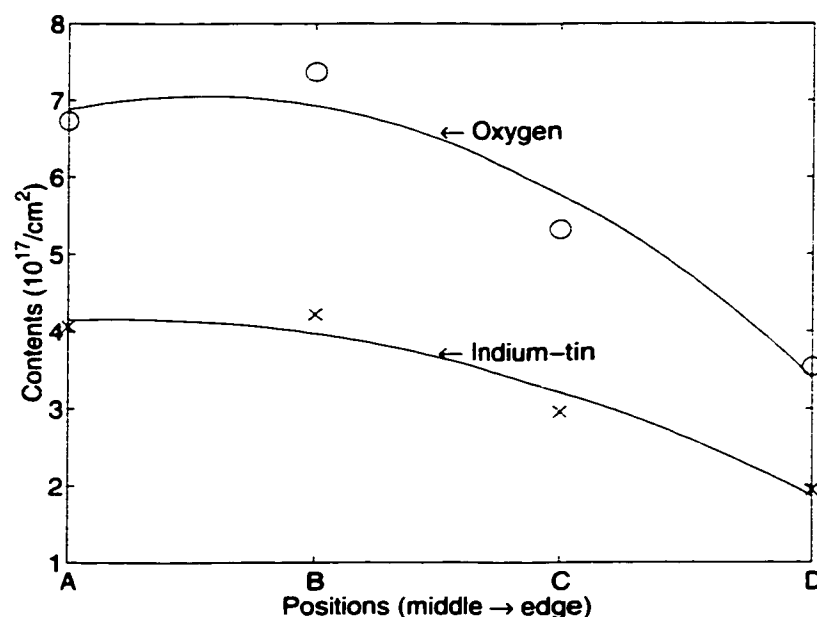
Figure 3.5: The change of content of oxygen and indium-tin in the film deposited at low temperature ITO for measured different positions.

3.1.2 Effects of Sputter Conditions on Film Structure

The variation in film structure with sputtering power was also investigated. From XRD measurements, we observed a weak <222> peak starting at an rf power of 150 W. For powers greater than 200 W, the peak becomes distinct if the wafers are placed near the center of the substrate holder. Fig. 3.6 shows XRD measurement results with the sample at position B when the rf sputtering power changes from 200 W to 400 W. The corresponding film thicknesses were 148 nm, 220 nm, and 292 nm, respectively. It is clear from the results that the crystallinity is affected by sputtering power. Here, the crystallinity first increases when the sputtering power changes from 200 W to 300 W, but it decreases from 300 W to 400 W. The SEM cross-section in Fig. 3.7 also shows a change in columnar structure, a feature which
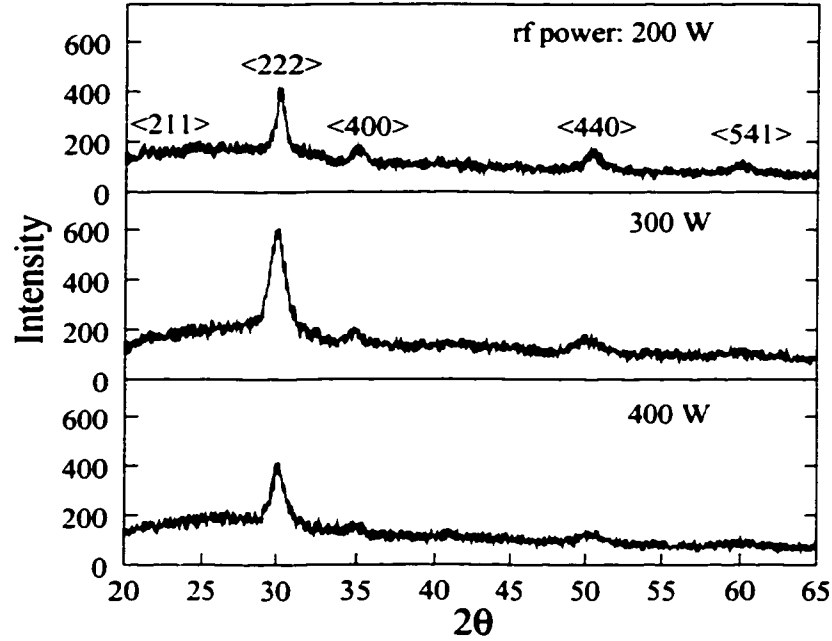
Figure 3.6: The change of film crystallinity for different sputtering powers.

is closely associated with polycrystalline materials. It is found that the trend in morphology shown by SEM is similar to that of XRD measurements. We conjecture that the ITO crystallizes to a high degree at some critical power. This is about 300 W in our process. For sputtering powers less than this value. the sputtered species have low surface mobility. However. at high powers. collisions between highly energetic incoming particles and the growing surface on the substrate undermine film crystallinity [43].

The change of film crystallinity with sputtering pressure is shown in Fig. 3.8. Here. the critical change can be seen when the sample is placed in position C. The XRD patterns indicate that the film crystallinity is weak at 5 mtorr but there is almost no peak at 15 mtorr.

Annealing will change the film structure and change film crystallinity. The
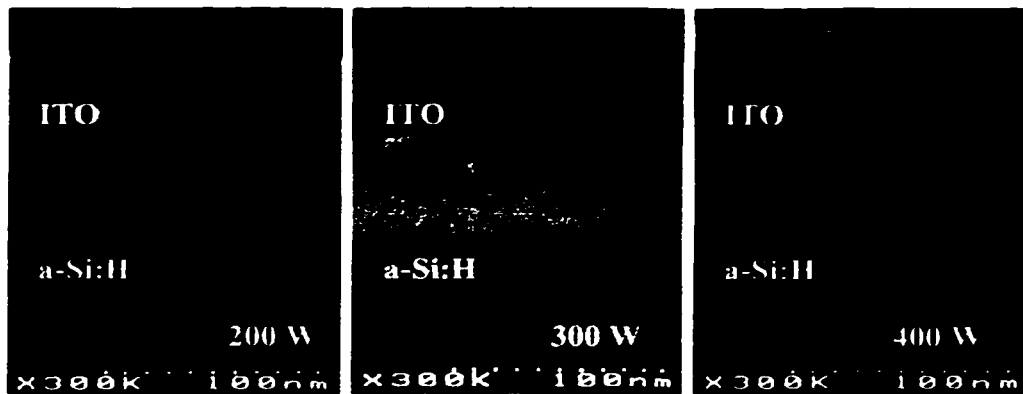
Figure 3.7: SEM cross-section for ITO deposited at different sputtering powers.
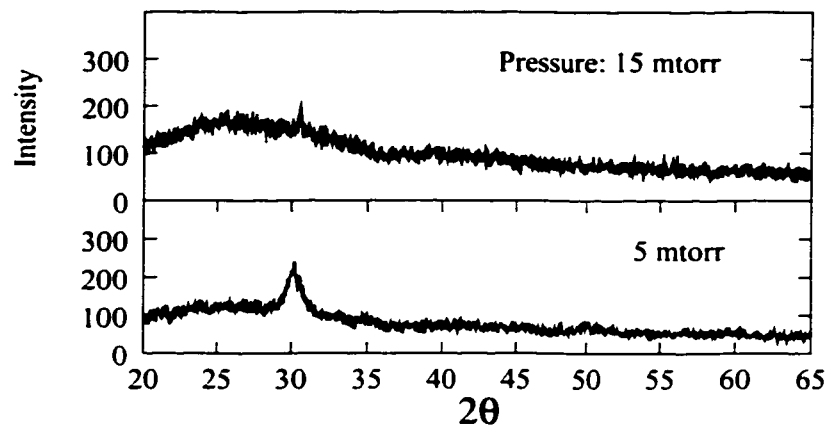
Figure 3.8: The change of film crystallinity for different sputtering pressures.

perspective changes for the samples at position B are shown in Fig. 3.9. The results indicate that the film at positions A and B becomes more crystalline after the film is annealed at higher temperature. However, there is no obvious change in crystallinity for the sample placed at positions C and D. The reason is that there is shortage of oxygen and indium at positions C and D. As a result, the film structure cannot change from the amorphous to the polycrystalline. However, there is enough oxygen at positions A and B and therefore the increase in temperature will improve

the structural order (crystallization) of films.
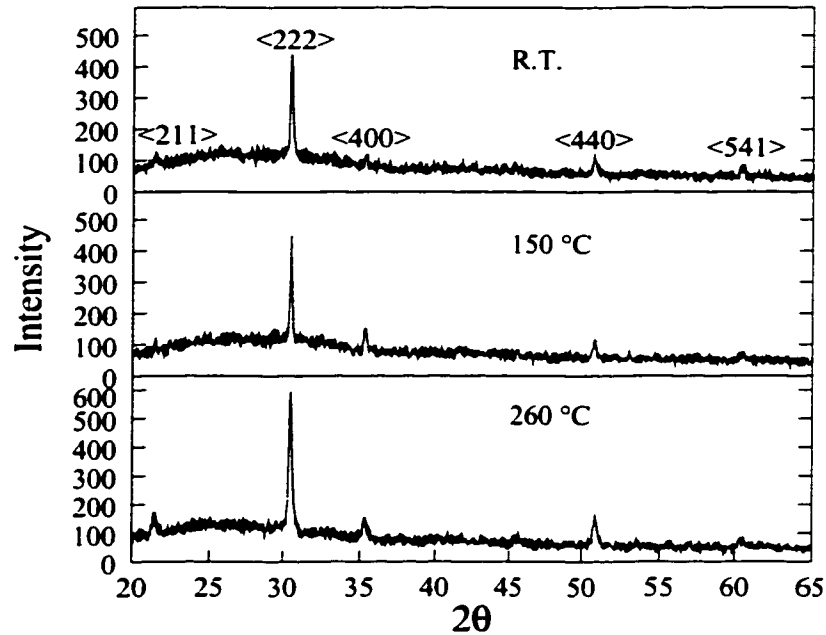
Figure 3.9: The change of film crystallinity for different annealing temperatures at position B.

Although the microstructure appears not to be influenced by the substrate when the ITO is deposited at elevated temperatures (> 150 °C). it plays a role when deposited at low temperatures [44]. X-ray diffraction (XRD) measurements have been performed to study the effect of two different substrates (a-Si:H and glass) on ITO crystallization. As indicated in Fig. 3.10. there is a strong presence of the <222> peak when deposited both on a-Si:H and on glass. However. the ITO film tends to be crystallized more easily on a-Si:H than on glass. Measurements carried out on one sample show that the degree of crystallinity is 60% or higher drawing from the height of <222> peak (see Fig. 3.10). The mechanism underlying the enhanced film crystallinity with the former is believed to be due to the reaction of the sputtered species with oxygen on the a-Si:H surface at the initial stages of film growth. With
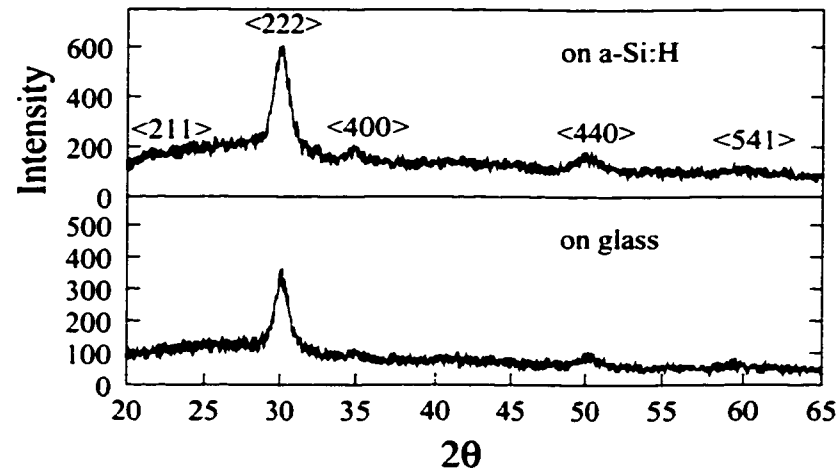
Figure 3.10: The change of film crystallinity for different substrates.

the glass substrate. however. and in contrast to the elevated temperature counter-part. the presence of the oxygen in the substrate does not contribute to the film crystallinity significantly because of the low processing temperature. which limits the diffusion of oxygen [45].

3.2 Transmittance

The film transmittance measurements were performed using an ORIEL optical system whose wavelength lies in the visible spectrum ranging from 400 nm to 900 nm. Here. glass was used as a reference and the transmittance was calculated based on the ratio of the output signal with and without the film. The film was deposited at 300 W unless otherwise specified.

3.2.1 Thickness

When ITO is used as a light window in optical sensors. the light absorption in ITO film and the light interference loss at the interface between ITO and other layers must be minimized. We performed the film transmittance measurements for different thicknesses of the ITO (see Fig. 3.11). It is observed that. in the visible range (400 - 700 nm). the films with thickness of 200 nm show higher transmittance and the transmittance decreases with increasing film thickness. Also. the interference occurs when the ITO layer is thicker than 400 nm.
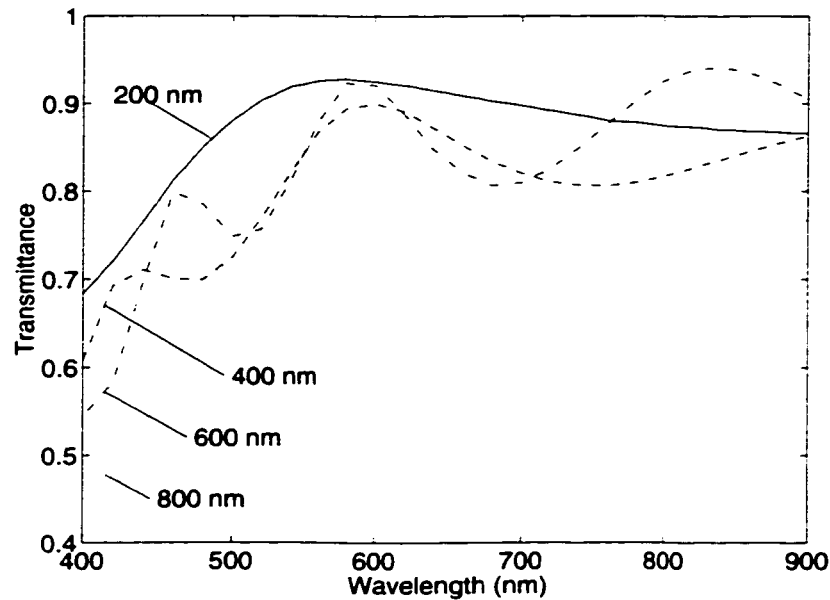
Figure 3.11: Transmittance spectra for different thicknesses of ITO films.

3.2.2 Effects of Sputter Conditions on Film Transmittance

The film transmittance at different positions is measured for 200 nm thick film and the results are plotted in Fig. 3.12. Here. film transmittance varies with position

of the substrate. It is observed. in the visible range. the transmittance is higher at positions A and B and decreases by moving the sample from the center to the edge of the substrate holder. This change in transmittance can be attributed to the change in film structure. as discussed in Section 3.1. At positions A and B. films are polycrystalline in structure while films are amorphous at positions C and D.
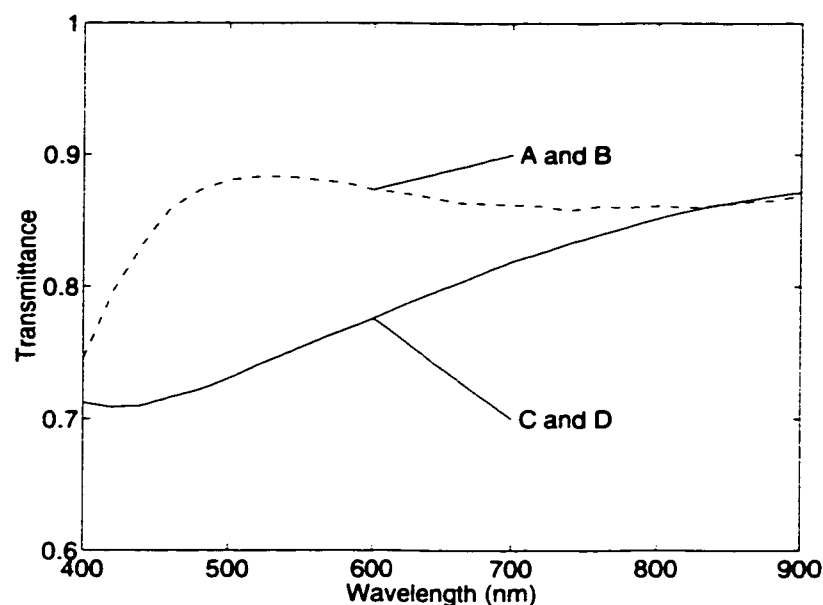
Figure 3.12: Transmittance spectra for different sample positions.

The film transmittance depends on the process power (see Fig. 3.13). It is observed that at lower powers (~ 200 W) the transmittance is very low. This could be due to the presence of voids and pinholes in the films. When the sputtered ion flux is high. the ions have a tendency to accommodate in these voids and pinholes. thereby improving the film quality. A high ion flux can be achieved by increasing the power. The improvement in transmittance is obtained when the film deposited at 300 W compared to the film deposition at 200 W. However. the decrease in the transmittance occurs at higher powers (400 W). This could be due to damage of
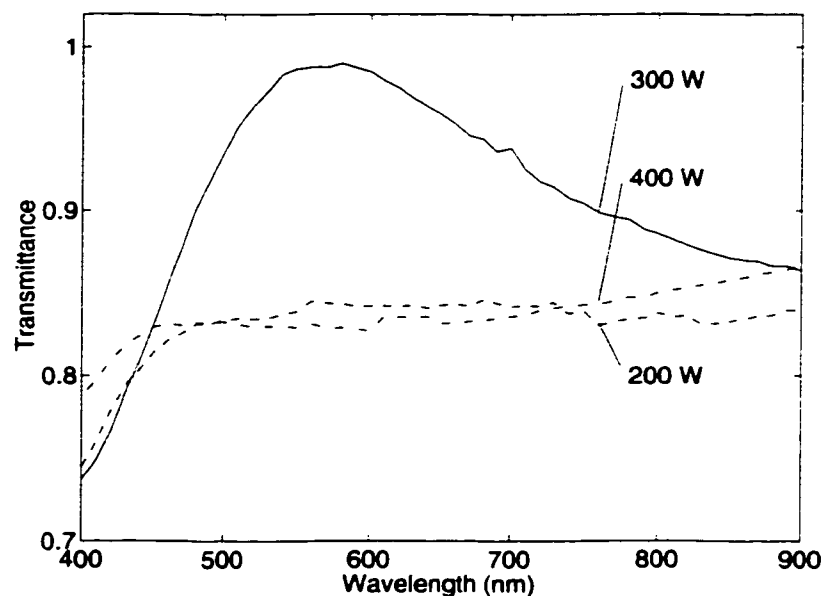
Figure 3.13: Transmittance spectra for different rf sputtering powers (film thickness: 220 nm).

film surface induced by energetic incoming ions.

The dependence of transmittance on sputtering pressure (5 and 15 mtorr) is shown in Fig. 3.14. Here. the deposition time is 20 minutes for both samples. Optical interference occurs for the sample deposited at 5 mtorr. which means that the thickness is higher than that deposited at 15 mtorr. The pressure is chosen to be high enough to maintain the presence of the plasma. In our process. a controllable and stable value of the sputtering pressure is 15 mtorr.

Annealing also improves the nano-structure of these films. The dependence of the transmittance of these films on annealing temperature is shown in Fig. 3.15 for the film deposited at Position *B*. As expected. the transmittance is increased all over the visible region in the annealed samples. due to improvement in the film structure. However. no obvious change in transmittance is observed for the
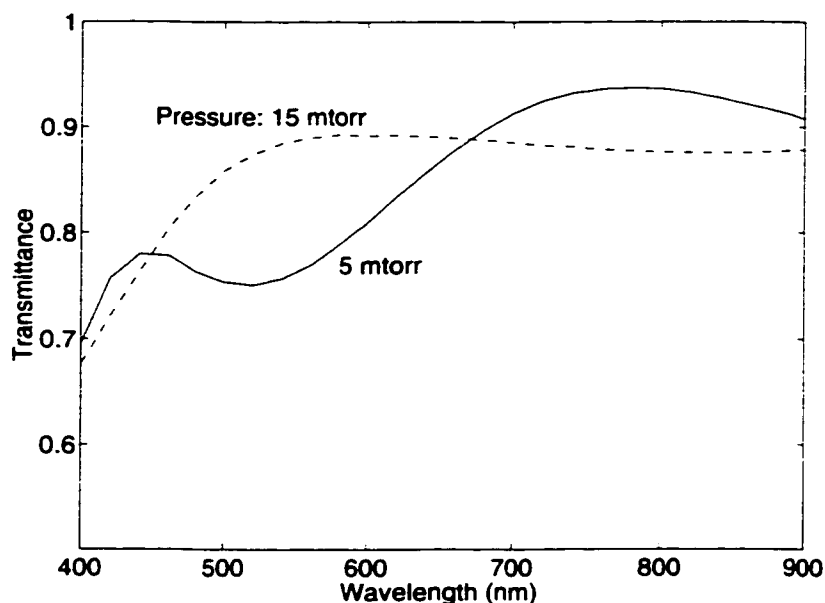
Figure 3.14: Transmittance spectra for different sputtering pressures.

film deposited at positions C and D. This result indicates the structure remains unchanged even after high temperature annealing.

3.3 Resistivity

A low resistivity is required when ITO is used as a conducting material in active matrix liquid crystal displays (AMLCDs) or as a contact metal material in Schottky photodiodes. The resistivity depends on the film nano-structure (i.e.. either polycrystalline or amorphous). the doping concentration of tin. and the content of oxygen in the film. For a polycrystalline ITO. the electron density is high (up to 10^{21} cm^{-3}) and the mobility is about 15 cm^{2}V^{-1}s^{-1}.

Fig. 3.16 shows the change of the resistivity with the sample position for the film thickness of 220 nm. The resistivity is measured by a four-point probe. The
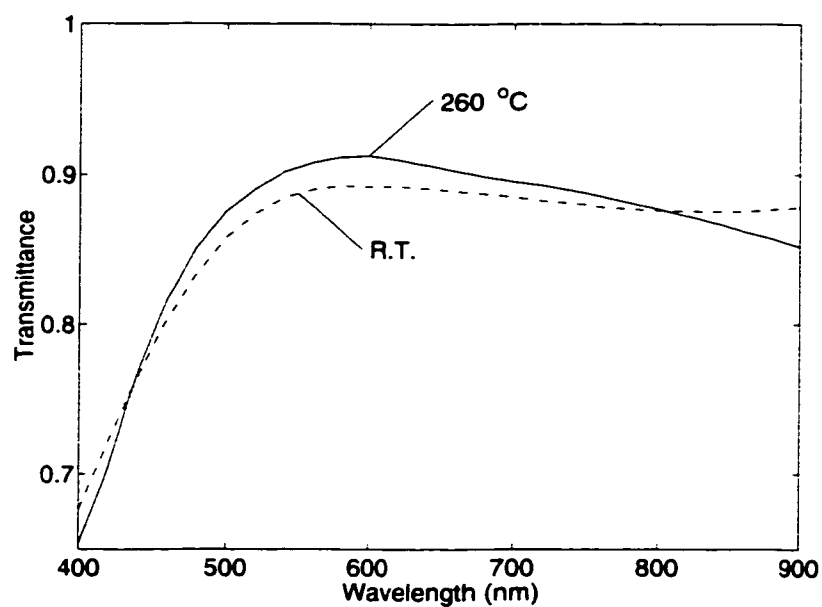
Figure 3.15: Transmittance spectra of ITO deposited with and without annealing.

film was deposited at 300 W with the process pressure of 15 mtorr. The resistivity reaches a minimum at position *B*. for a value of 4×10^{-4} Ω-cm. Values reported elsewhere are also plotted in the figure [46] [47] [48] [49] [50] [51].
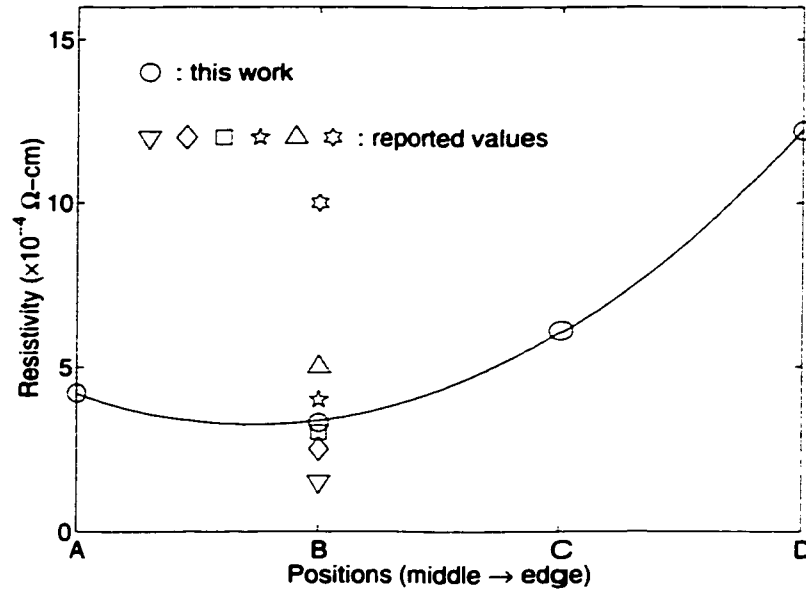
Figure 3.16: The change of film resistivity with sample positions.

3.4   Summary

In this chapter. we presented a deposition process of polycrystalline indium tin ox-ide (ITO) films at low temperature. The material characteristics in terms of optical transmittance. electrical resistivity. and the degree of crystallinity were optimized by controlling sample position. rf sputtering power. sputtering pressure. and sub-strate type. Optimal deposition condition for device grade material was obtained at an rf power of 300 W. a sputtering pressure of 15 mtorr. and with the substrate positioned near the center of the substrate holder.

Chapter 4

Characterization of ITO/a-Si:H Schottky Photodiodes

a-Si:H optical sensors are used to detect the visible light. Their suitability for large area imaging depends on many parameters:

- Photosensitivity: if it is high enough to meet the requirement of signal level.

- Leakage current: if it is low enough to reduce the background signal and to increase the dynamic range.

- Spectral response: if it is well matched to the spectrum of light out of phosphor and if it is large enough to achieve high sensitivity.

- Photo response: if it is fast enough to obtain high frame rate.

- Stability: if it is high enough to catch the original information and to decrease the image lag.

- Process simplicity for low cost and fabrication reproducibility for high yield.

In this work. Schottky photodiode was used as a detection element. The device operation is given in Section 4.1. Design details are examined in Section 4.2. Process considerations are discussed in Section 4.3. The fabrication issues are described in Section 4.4. In Section 4.5. the device is characterized in terms of photosensitivity. leakage current. stability. spectral response. and X-ray sensitivity.

4.1 Device Structure

When a metal contacts with a crystalline silicon (c-Si). the Fermi levels in the two materials must coincide at thermal equilibrium. As a result. a Schottky barrier is formed at the interface. The barrier height is determined by the metal work function. the Fermi level in Si. and the interface properties. The device performance is therefore subject to the quality of metal layer. interface features. and the characteristics of silicon [52].

When a metal contacts with an amorphous silicon. a Schottky barrier is established as in the crystalline case. However. there is an important difference. In the crystalline case. the charge density in the depletion region is generally determined by shallow donors or acceptors. so that the potential is parabolic in shape if the doping concentration is uniform. In amorphous semiconductors. however. the charge density is determined by the charge associated with the localized states in the gap. Since the electron population in these states is determined by the position of the Fermi level in the gap. the charge density due to the localized states is far from uniform and the potential shape is therefore not parabolic [53].

The photodiode is based on ITO/a-Si:H Schottky structure (see Fig. 4.1). ITO is used as a metal contact to form a Schottky barrier as well as a light window which allows the light to go to the a-Si:H layer. The intrinsic a-Si:H serves as an

active layer where electron-hole pairs are generated. n^+ a-Si:H acts as an ohmic contact between the a-Si:H and the bottom electrode. Cr is a metal layer where the photogenerated electrons are collected. When light (with a wavelength shorter than 1000 nm) enters a-Si:H it creates electron-hole pairs, which are collected at the opposite contacts and detected as a photocurrent when ITO/a-Si:H Schottky photodiode is held under the reverse bias.
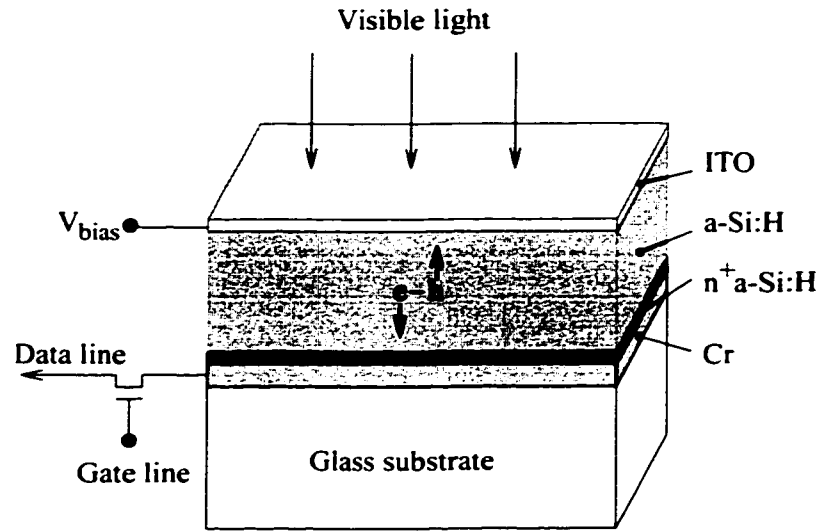
Figure 4.1: Schematic of photodiode.

The intrinsic a-Si:H has sufficient carrier lifetime (see Table 2.1) to enable the separation of photogenerated carrier pairs even without an external bias [54]. At reverse bias, the intrinsic a-Si:H can sustain a fairly wide depletion region on contact with a metal forming a Schottky barrier, or in contact with a p-type region of a-Si:H forming a p-n junction. For a Schottky diode, the Schottky barrier serves as electron blocking. Therefore, the electron injection from the electrode is negligible. Moreover, photogenerated carriers will be captured in traps, and hence will build up a space charge region which perturbs the applied field to low values in this region.

Blocking contacts allow high fields to be retained so that carriers can travel across the a-Si:H active layer [55].

There are two types of Schottky-barrier photodiodes. One relies on absorbing the photons in the semiconductor of an MS structure and the other relies on absorbing the photons in the metal of an MS structure. In this work. the former device is employed and it is designed to detect wavelengths shorter than [56]

$$\lambda \leq 1.24/E_g.$$ (4.1)

where E_g is the bandgap in electron volts.

An ITO/i a-Si:H/n^+ a-Si:H/Cr band structure is shown in Fig. 4.2. In undoped a-Si:H devices. the photocurrent is mainly contributed by electrons because of their higher mobility (~ 1 cm2/Vs) than holes' (~ 0.01 cm2/Vs). Therefore. the electron current is the main component of interest.

4.2 Design Considerations

Based on the operating principle described in Section 4.1. device design is discussed in this section.

4.2.1 Capacitance

The design of a photodiode reduces primarily to tailoring its capacitance since the diode capacitance determines to a large extent the detection sensitivity. dynamic range. readout speed. and noise. The capacitance in a c-Si Schottky diode stems from the depletion layer and can be expressed as [57].

$$C_{photo} = \sqrt{\frac{qN_D\epsilon_0\epsilon_s}{2(V_b + V_a)}}A.$$ (4.2)
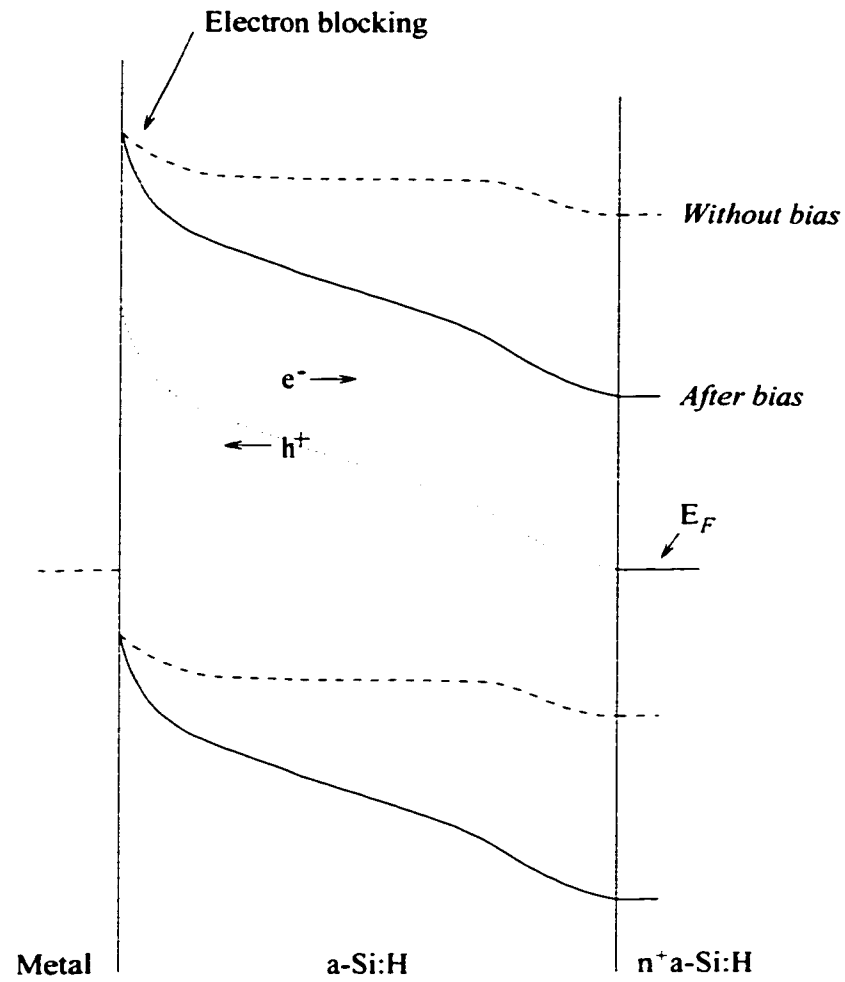
Figure 4.2: Schematic of an ITO/a-Si:H/n$^+$ a-Si:H/Cr Schottky photodiode at zero bias and under reverse bias.

where ϵ_0 is permittivity of free space (8.85×10^{-12} F/m). ϵ_s is dielectric constant of semiconductor($\sim$ 12 for a-Si:H). q is elementary charge (1.6×10^{-19} Coulomb). A is the sensor area (W×L). V_b is the built-in potential. V_a is the bias voltage. and N_D is the doping concentration. Here. the capacitance is dopant level dependence. In the a-Si:H Schottky diode. N_D is the defect density. For an area of 100×100 μm^2. N_D of 5×10^{15}/cm^3. V_b of 0.8 V. and V_a of 5 V. the capacitance is calculated to be 1.1 pF.

When an a-Si:H Schottky diode is used to detect the optical signal. the reverse bias voltage is applied to fully deplete the active layer. The capacitance of a full depletion layer in a sandwich structure is

$$C_{photo} = \frac{\epsilon_0 \epsilon_s A}{d}.$$ (4.3)

where d is the a-Si:H thickness and A is the sensor area. For the thickness of 1 μm. the area of 100×100 μm^2. the capacitance is calculated to be 1.1 pF.

4.2.2   Film Thickness

As discussed in Section 3.2.1. the thin ITO layer has higher light transmittance. Also. the thickness is required to be less than 400 nm in order to avoid the light loss due to light interference at the interface. However. the film needs to be thick enough to achieve the low resistance. In our device. the thickness of the ITO film is 110 nm.

As discussed in Section 2.1.2. high light absorption of a-Si:H will give rise to high photosensitivity. The thickness of the a-Si:H is therefore needed to be optimized. In terms of high storage capabiltiy of photogenerated charges. however. the a-Si:H thickness is required to be small to have a large capacitance. Fast optical response

is required to reduce image blurring in large area imaging. The transit time T_{tr}. defined as the time taken to traverse the entire fully depleted a-Si:H layer. is given by [58]

$$T_{tr} = \frac{d^2}{V\mu}. \tag{4.4}$$

where d is the transit length which corresponds to the thickness of the a-Si:H film. μ is the mobility of the photocarrier. and V is the applied voltage. The electron mobility in a-Si:H is about 1 $cm^2V^{-1}s^{-1}$. Therefore. a-Si:H thickness is required to be small in order to obtain a short transit time. For example. for an a-Si:H thickness of 1 μm at an applied voltage of 5 V. the maximum transit time for the electron is calculated to be 2×10^{-9} s and that for the hole 2×10^{-7} s. Those short times allow both electron and hole to be collected before their recominations (lifetime for electron and hole: 1×10^{-6} s. see Table 2.1).

n^+ a-Si:H is required to be as thin as possible due to the presence of high density of defect states. which act as recombination centers. In our device. the n^+ a-Si:H thickness is 50 nm.

Cr thickness is also needed to be optimized in terms of high stress and low conductivity. When Cr is very thick. the film might break. which in turn leads the photoresist to stick inside the Cr film. On the other hand. the Cr has a low conductivity. which will introduce high resistance if the film is too thin. In our design. the Cr thickness is chosen to be 100 nm.

The ITO/a-Si:H Schottky photodiode is designed with geometry parameters listed in Table 4.1.

Table 4.1: Photodiode geometry design parameters.

a-Si:H thickness	0.25. 0.5. 1.0. 1.25. 1.5	μm
n$^+$ a-Si:H thickness	50	nm
ITO thickness	110	nm
Cr thickness	100	nm
Al thickness	1	μm

4.2.3 Geometry of Collection Electrode

In this work. the effects of different collection electrodes on the device performance were studied. The structures of grided. slot. and conventional electrodes were compared in terms of photosensitivity. which will be presented in Section 4.5.1.

4.2.4 Breakdown

The Schottky photodiode based on thin film structure does not have a conductive substrate. The static charges can be easily accumulated as a result and undermines the device performance. In some situations. those charges can be large enough to break down a working device. The breakdown electric field of amorphous silicon diodes was found to be around 6×10^5 V/cm [59]. Care must be taken to avoid electrical charging of the sensor units during handling and technological processes. for example. during the wire-bonding.

4.3 Process Considerations

ITO is characterized in terms of its structure. transmittance. and resistivity in Chapter 3. In this section. we shall study its interface properties with a-Si:H in order to provide the information for the improvement in the characteristics of photodiodes.

The leakage current of the sensor is a source of noise and limits the integration time in large area arrays. The leakage current is determined by a-Si:H material characteristics and the features of the ITO/a-Si:H Schottky interface. The defect density in the a-Si:H depends on the film preparation processes. post annealing. thickness of active layer. light soaking. and bias. The density of interface states depends on the ITO and a-Si:H materials. preparation method. and device structures (e. g.. a-Si:H on ITO or ITO on a-Si:H). The elements which might be responsible for the leakage current and the shift in leakage with time are indium. tin. and oxygen.

In order to improve device performance. the interface characteristics must be optimized with respect to device structure and fabrication processes. During the formation of Schottky contact. chemical reaction and atomic interdiffusion can happen at the interface. As shown in Fig. 4.3. it is possible for indium. tin. and oxygen to interact with the silicon and hydrogen at the interface during or after ITO deposition. leading to a compositional change at the interface. Oxidation of the surface is observed to increase the density of interface states by one order of magnitude or more and also to change the defect energy level by 0.2 eV [60]. On the other hand. the hydrogen concentration is also different near the interface. The change in oxygen. hydrogen. and the disorder or bonding structure at the interface modifies the density of interface states. hence the Fermi energy. the slope of the band
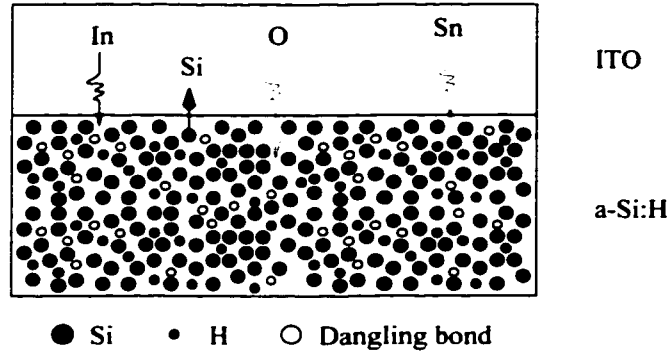
Figure 4.3: ITO/a-Si:H interface schematic.

tail. and the position of the defect states in the gap. The distribution of oxygen. indium. and hydrogen at the vicinity of the interface depends on the preparation condition. such as deposition temperature. annealing. and sputtering power. How to control this interface structure and to reduce the density of interface states is a major endeavor in this research.

The elemental and compositional analyses and their diffusion profiles in our samples were characterized using secondary ion mass spectroscopy (SIMS). The SIMS measurements were performed with a CAMECA 3F mass spectrometer system. The secondary ions were analyzed as a function of sputter time through the sample and stylus profilometry was used to determine the depth scale.

4.3.1 Test Structures

There are two typical structures. as shown in Fig. 4.4. One arrangement is based on ITO deposited on glass with the a-Si:H active layer deposited on the top of this transparent material. The other is a reverse arrangement whereby the ITO is deposited on the top of the active a-Si:H layer. For the former structure $(Cr/n^+$ a-Si:H/a-Si:H/ITO/glass). during the glow-discharge deposition of a-Si:H layers.
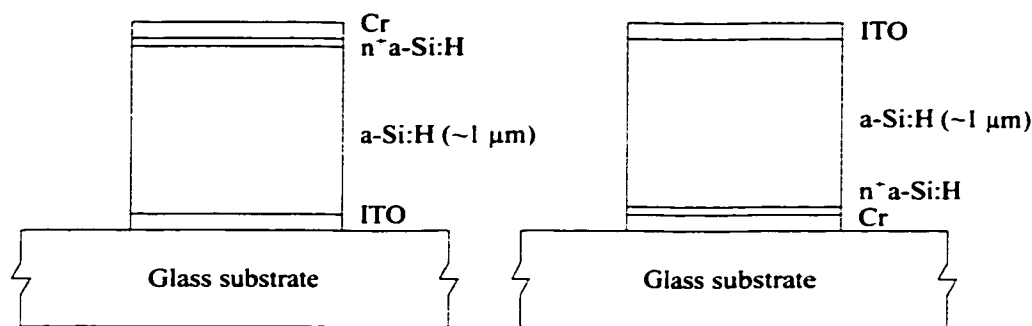
Figure 4.4: Optical sensor structures.

however, the interaction of the ITO with activated species (radicals, electrons, ions) present in the plasma can lead to chemical reaction at the ITO/a-Si:H interface. Chemical reaction and interdiffusion may result, with subsequent deterioration of device characteristics. In this research, we employed the ITO/a-Si:H/n^+ a-Si:H/Cr/glass one, which is ITO-sputtered after a-Si:H deposition, to make ITO low temperature process possible. In this process, ITO does not need to withstand high temperature. Also, there is no light loss in glass and at ITO/glass interface. Furthermore, the phosphor can be coupled directly on the surface of optical sensor when used for X-ray detection, thereby the detection resolution can be enhanced and lateral crosstalk can be reduced. As reported, the initial deposition of a-Si:H yields material with a high defect density so that the Schottky barrier between a-Si:H and bottom electrode is screened out over a short distance [61] [62].

We fabricated the above two structures: Process I for a-Si:H on the top of ITO and Process II for ITO on the top of a-Si:H. Figs. 4.5 and 4.6 show the SIMS depth profiles of oxygen and indium diffusion in a 750 nm thick a-Si:H layer. Here, it is observed that the oxygen diffuses deeply by about 150 nm into the a-Si:H in both cases. The oxygen concentration in the ITO is less in the case of process I due to the interaction of the oxygen with the hydrogen in the plasma. In contrast, the oxygen
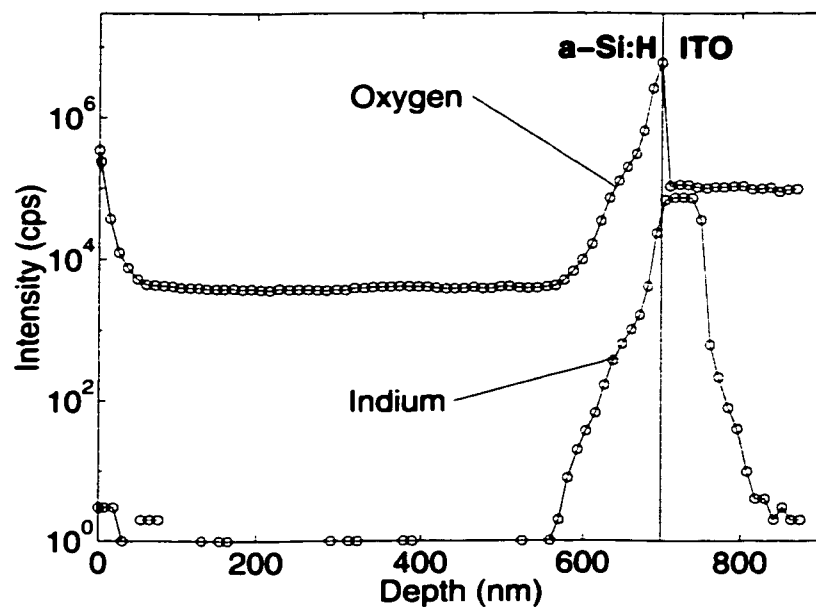
Figure 4.5: SIMS measurements for a-Si:H/ITO/glass structure.
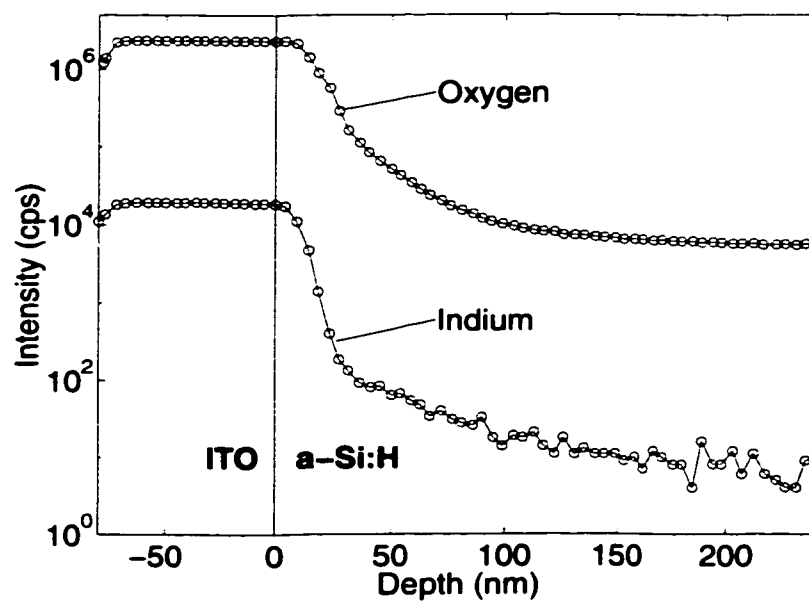
Figure 4.6: SIMS measurements for ITO/a-Si:H/glass structure.

concentration in ITO films remains unchanged in process II. As observed. there are no peaks for either oxygen or indium at ITO/a-Si:H interface in process II. while there is a peak for oxygen in process I. This indicates that the ITO composition was affected by the plasma reaction in process I. In terms of fabrication. we adopted process II in view of the higher conductivity. which increases in ITO films with higher oxygen content. This also yields a smoother interface. which is useful for reducing the leakage current. Furthermore. the oxygen deficit in the ITO film leads to reduced transmittance. which is usually referred as blacking of ITO. The study of the substrate effect on ITO crystallinity is also favorable in process II. as shown in Fig. 3.10. The distribution of indium and oxygen for process II is focused on in the following discussion.

4.3.2 Sputtering Power

The diffusion of oxygen and indium from ITO to a-Si:H increases with the increasing of rf sputtering power. as shown in Figs. 4.7 and 4.8. respectively. The lower sputtering power is preferred from the standpoint of interface integrity. In terms of ITO nano-structure discussed in Section 3.1. rf power of 300 W was chosen for a film with high degree of crystallinity.

4.3.3 Annealing Temperature

In terms of ITO crystallinity and transmittance. high temperature (260 °C) is preferred. as discussed in Sections 3.1 and 3.2. In a Schottky photodiode structure. however. high temperature might introduce a high density of interface states between ITO and a-Si:H.
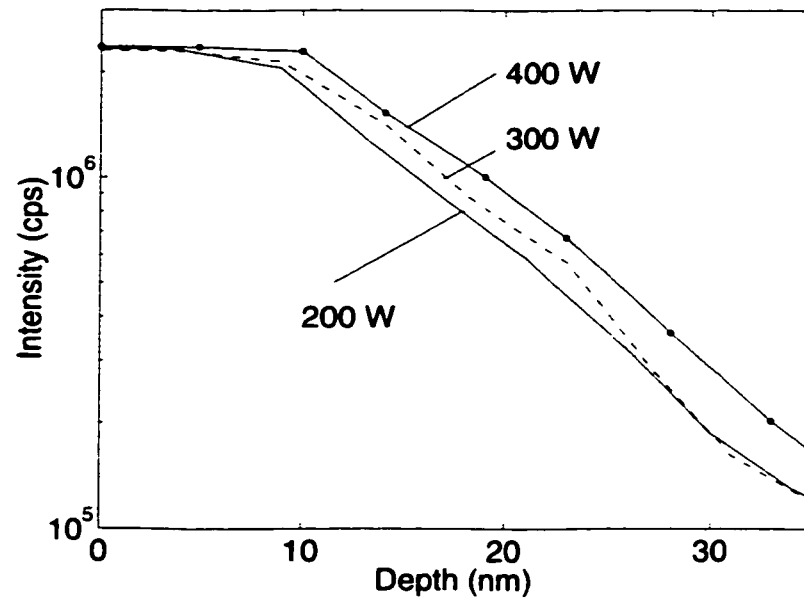
Figure 4.7: Oxygen profiles in a-Si:H with ITO sputtered at different powers.
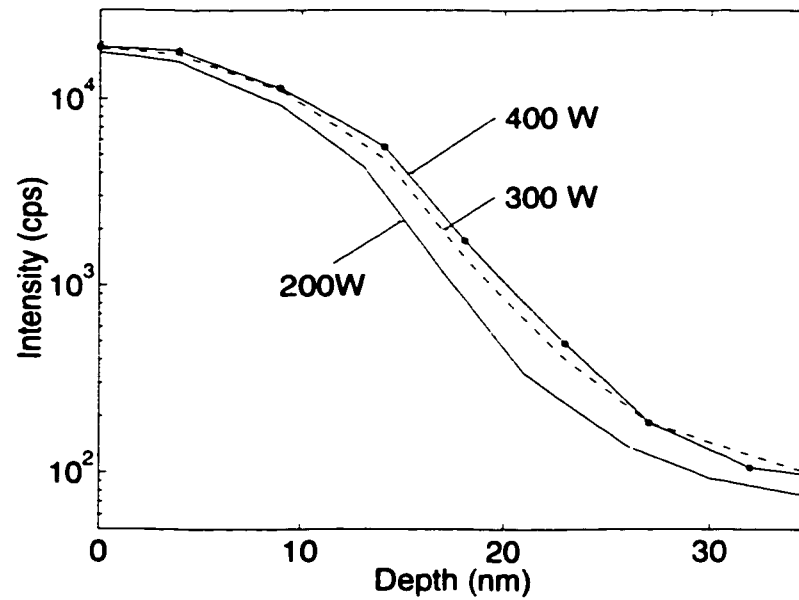
Figure 4.8: Indium profiles in a-Si:H with ITO sputtered at different power.

SIMS measurements for different annealing temperatures for oxygen and indium distributions are shown in Figs. 4.9 and 4.10. respectively. As observed. both
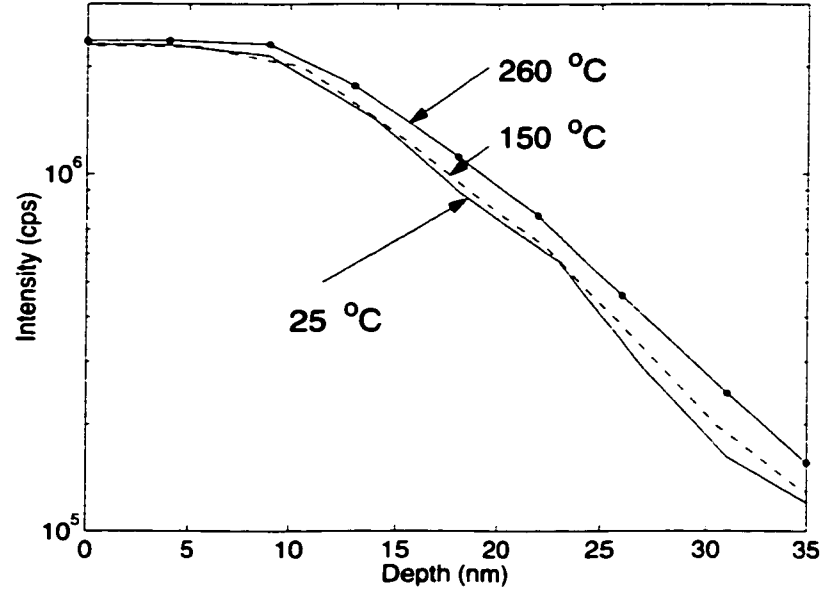
Figure 4.9: Oxygen profiles in a-Si:H with ITO annealed at different temperatures.

oxygen and indium diffuse more into the a-Si:H at 260 °C than at room temperature. the details are given in Table 4.2. However. the diffusion depth of oxygen is much higher than that of indium at 260 °C compared with at 25 °C. One very interesting result is that the diffusion of indium and oxygen at 150 °C is very close to that

Table 4.2: Indium and oxygen diffusion range (ITO film thickness: 80 nm).

	Indium (nm)	Oxygen (nm)
25 °C	80 to 130	82 to 231
150 °C	81 to 131	83 to 236
260 °C	82 to 135	84 to 260
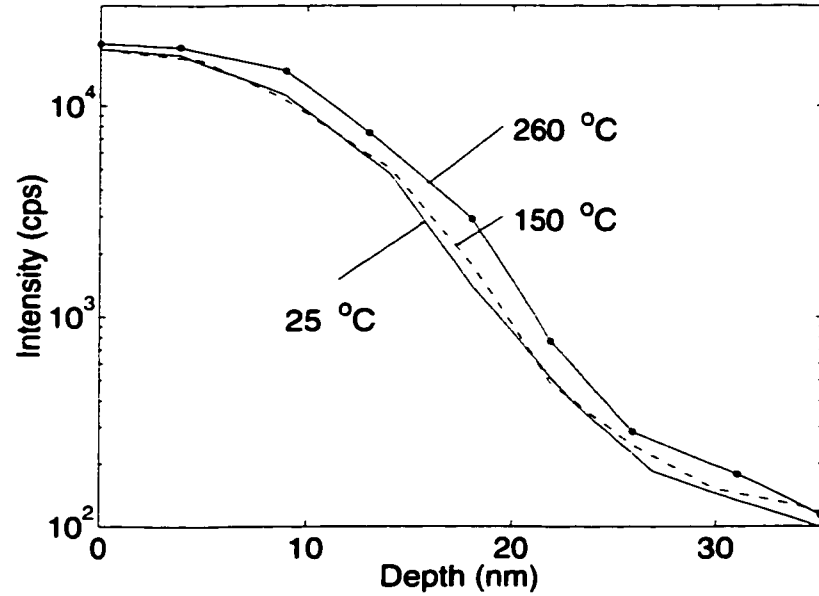
Figure 4.10: Indium profiles in a-Si:H with ITO annealed at different temperatures.

at room temperature. which means that the sample can be annealed at 150 °C for a long time to remove sputtering damage and light-generated defects without undermining the ITO/a-Si:H interface integrity.

4.4   Fabrication

4.4.1   Wet Etch Process

A fully wet etch process was used in patterning the various layers needed for the fabrications of the photodiodes and the TFTs as well as the integration of the photodiode and TFT. The etchants and etch conditions used are given in Table 4.3. Highly diluted buffered HF was used to provide a good etch control of the a-SiN$_x$:H. In etching a-Si:H. a high selectivity between a-Si:H and a-SiN$_x$:H was realized with

KOH at low concentration. In patterning polycrystalline ITO. a strong acid (HCl) with the addition of strong oxidant ($FeCl_3$) was used.

Table 4.3: Wet etchants for fabrication of photodiodes (and TFTs).

	Etchants	Temperature (°C)
Cr	$Ce(NH_4)_2(NO_3)_6$: CH_3COOH : H_2O = 120 g : 100 ml : 500 ml	25
a-Si:H n^+ a-Si:H n^+ μC-Si:H	KOH (10 wt.%)	40
a-SiN$_x$:H	BHF (NH_4F : HF=15:1)	25
Al	H_3PO_4 : CH_3COOH : HNO_3 : H_2O = 456 : 36 : 18 : 90 ml	40
ITO	HCl (18%) : $FeCl_3$ = 1 L : 5.6 g	50

4.4.2 Fabrication Sequence

The photodiode used in this work is based on the sandwich structure. We started with patterning Cr (the bottom electrode) on a glass substrate. n^+ a-Si:H. intrinsic a-Si:H. and a-SiN$_x$:H were deposited in one process run. Al layer was then sputtered and patterned. Passivation a-SiN$_x$:H layer was deposited all over the area. The contact window between the a-Si:H and the ITO was opened before the ITO film was sputtered. Process parameters are summarized in Table 4.4.

Figs. 4.11 and 4.12 show the top view and cross-section of photodiodes. taken by microscopy camera and SEM. respectively. The fabrication sequence is shown

Table 4.4: Deposition conditions of ITO/a-Si:H Schottky photodiodes.

Layer to deposit	Pressure (Torr)	Power (W)	Sub. temperature. (°C)	Gas
Cr (bottom metal)	5×10^{-3}	400	R.T.	Ar
n^+ a-Si:H (ohmic contact)	0.15	12	260	$\frac{PH_3}{SiH_4} = 1\ \%$
a-Si:H (active layer)	0.5	12	260	$SiH_4 = 50$ sccm
Al (final metal)	5×10^{-3}	400	R.T.	Ar
ITO (metal layer)	0.02	300	R.T.	Ar
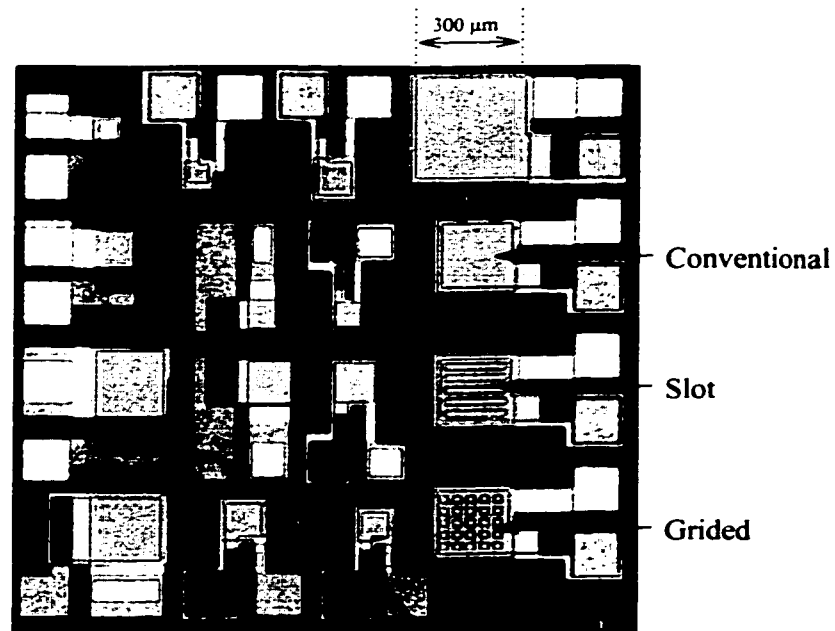
Figure 4.11: Photograph of fabricated die showing photodiodes with different areas and bottom electrode structures (conventional. slot. and grided).
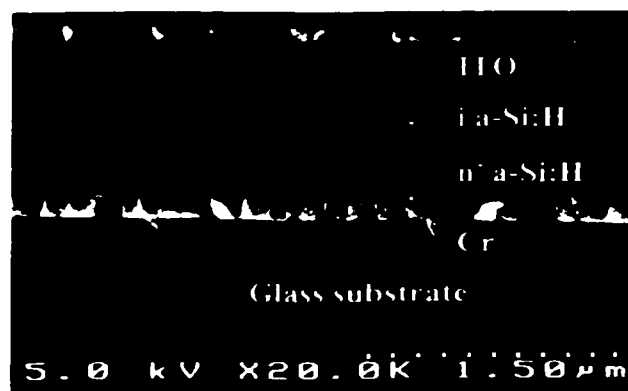
Figure 4.12: SEM cross-section of fabricated photodiode.

in Fig. 4.13. Due to the multilayer structures and complicated connections over the large area, the film continuity is also considered. For example. in one process of our photodiode fabrication, the step exists between the ITO and the bonding pad when the ITO was connected from the top of photodiode to the wire bonding pad. The other process without this step is also accomplished. as shown in Fig. 4.14. No obvious difference between those two processes was observed in the device performance, which indicates that different slope profiles do not affect the device characteristics. Therefore, the interconnection with a step in a large-area imaging system is feasible.

In order to eliminate the cross-talk between neighboring pixels in large area imaging, the active layer of the photodiode for each pixel is isolated from the surroundings. Both wet and dry etchings can be employed for this purpose. In our process for fabricating thin film transistors. KOH was used to etch a-Si:H because of the easy handling and simple control. However, in photodiode fabrication. etching of very thick film requires a much longer time over a large area because of non-uniformity in etching process. As shown in Fig. 4.15, the a-Si:H was etched nicely but it was not clean in some areas. By rotating the samples in the solution. high-uniformity etching was achieved.

The a-SiN$_x$:H layer was used as an etch mask in the a-Si:H etching. A highly dense a-SiN$_x$:H film is therefore required to avoid etchants to go through. Also, the a-SiN$_x$:H is required to be of less stress. Otherwise, the built-in stress would lead to the film peel-off (see Fig. 4.16), especially when the etching is taken over a large protected area.

Process #1: Cr sputtering and bottom electrode formation (Mask #1)   Cr

Glass substrate

Process #2: n⁻a-Si:H/i a-Si:H/a-SiN$_x$:H deposition and PD area definition (Mask #2)

a-SiN$_x$:H

i a-Si:H

n⁻a-Si:H

Glass substrate

Process #3: Al sputtering and bonding pad formation (Mask #3)   Al

Glass substrate

Process #4: a-SiN$_x$:H deposition and PD window opening (Mask #4)

Glass substrate

Process #5: ITO sputtering, top electrode formation (Mask #5)
Pad opening (Mask #6), bonding, sawing and test

Bonding (top)   ITO   Bonding (bottom)

Glass substrate

Figure 4.13: Process sequence for optical sensors when there is a step between top ITO and metallization layers.

Process #1: Cr sputtering and bottom electrode formation (Mask #1)

Process #2: n⁻a-Si:H/i a-Si:H/SiN$_x$:H deposition and PD area definition (Mask #2)

Process #3: Al sputtering and bonding pad formation (Mask #3)

Process #4: a-SiN$_x$:H deposition and PD window opening (Mask #4)

Process #5: ITO sputtering and top electrode formation (Mask #5)
Pad opening (Mask #6), bonding, sawing and test
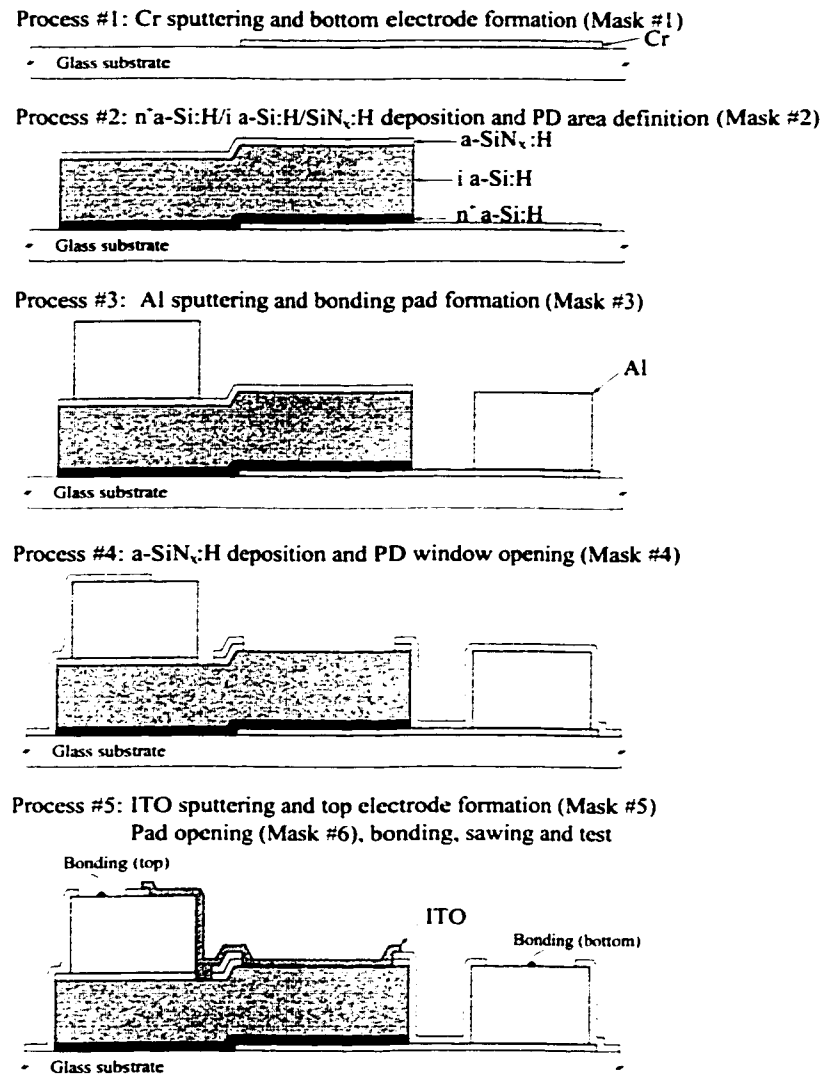
Figure 4.14: Process sequence for optical sensors without step between top ITO and metallization layers.

a-Si:H residue
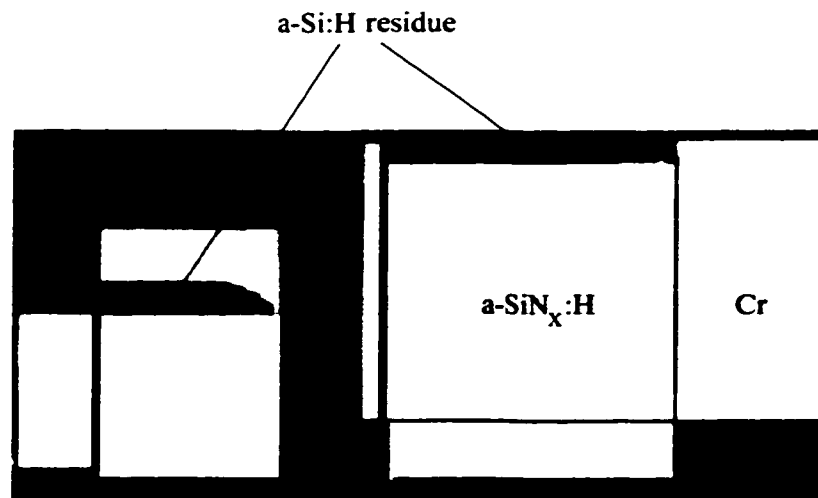
Figure 4.15: a-Si:H etch non-uniformity.
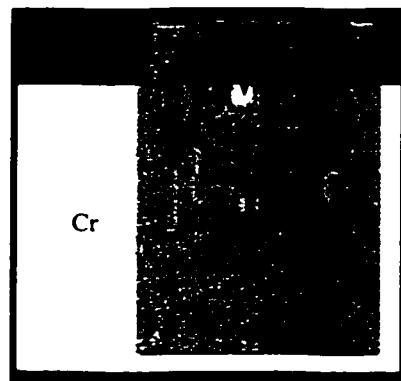
Figure 4.16: a-SiN$_x$:H as a protection layer in a-Si:H etching. A pinhole in a-SiN$_x$:H allows the KOH to penetrate into the a-Si:H layer.

4.5   Characterization of Photodiodes

The optical sensitivity of photodiodes was measured in terms of current-voltage (I-V) characteristics under optical illumination. The I-V measurements were performed using the Keithley 236 source measurement units (see Fig. 4.17).
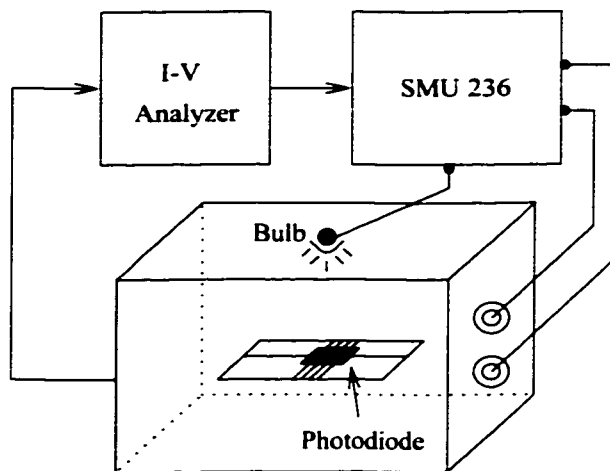
Figure 4.17: Sensitivity and leakage current measurement set-up.

4.5.1   Photosensitivity

The I-V characteristics for an ITO/a-Si:H Schottky photodiode in the presence and absence of optical illumination is shown in Fig. 4.18. At a bias voltage of -2 V. the photocurrent is 7×10^{-7} A/cm^2 and the dark current 7×10^{-10} A/cm^2. The ratio of photo to dark current is about 1000.

The photosensitivity, which is a key issue in imaging applications. depends on [63]:

• Light transmittance of the ITO film.
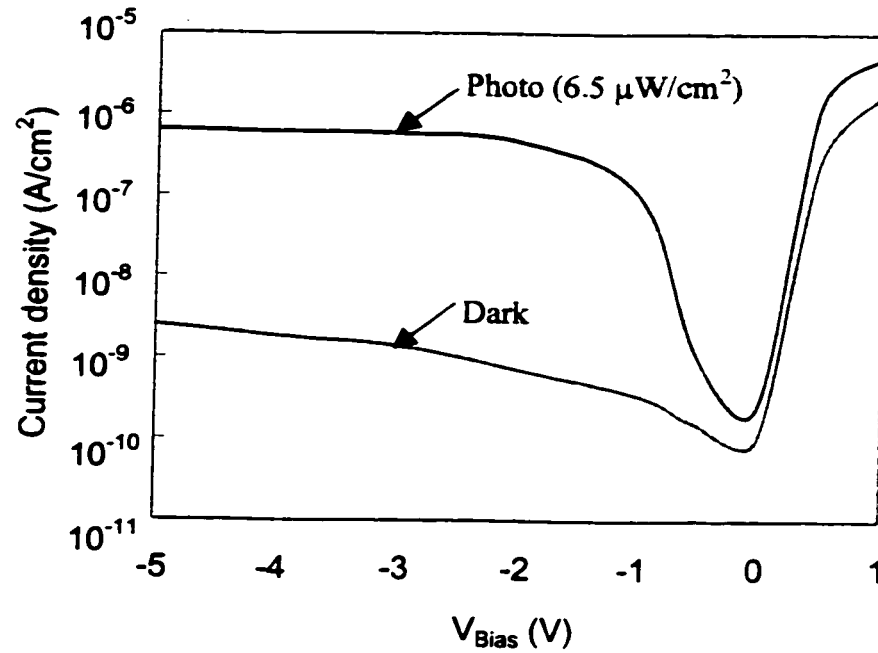
Figure 4.18: Characteristics of a Schottky photodiode based on an $ITO/a\text{-}Si{:}H/n^+$ $a\text{-}Si{:}H/Cr$ structure using ITO deposited at low temperature in the presence and absence of ambient light.

- Optical absorption of the a-Si:H.

- Recombination in the a-Si:H.

- Recombination in the n^+ a-Si:H.

- Light loss at interfaces.

- Reflection of back (bottom) electrode.

- Charge collection efficiency.

In this research. the dependence of photosensitivity on the a-Si:H thickness and the geometry of the collection electrode is considered.

The photosensitivity can be modified by the thickness of the a-Si:H active layer. Fig. 4.19 shows the ratio of photocurrent over dark current (biased at -2 V) in the presence of ambient light (intensity: 6.5 $\mu W/cm^2$). Here. we observe that the optical sensitivity reaches a maximum when the a-Si:H thickness is 1 μm. This dependence of photosensitivity on thickness can be explained by the light absorption and collection efficiency. When the thickness of the a-Si:H active layer is small. most of the light with long wavelength passes through. Therefore. the photosensitivity is small. On the other hand. when the thickness of a-Si:H is very large. the collection efficiency is small for the fixed bias. This can be attributed to the following: large bulk trapping of photogenerated carriers. reduced electric field in the active layer. and possible increase of the (diffusion-dominated) neutral region [64].

The geometry of collection electrodes also plays a role in the photosensitivity of the ITO/a-Si:H Schottky photodiode (see Fig. 4.20). Here. we observe no appreciable change in photosensitivity at low bias. When the bias is higher. the change is significant. For example. when the bias voltage is -2 V. the photocurrent
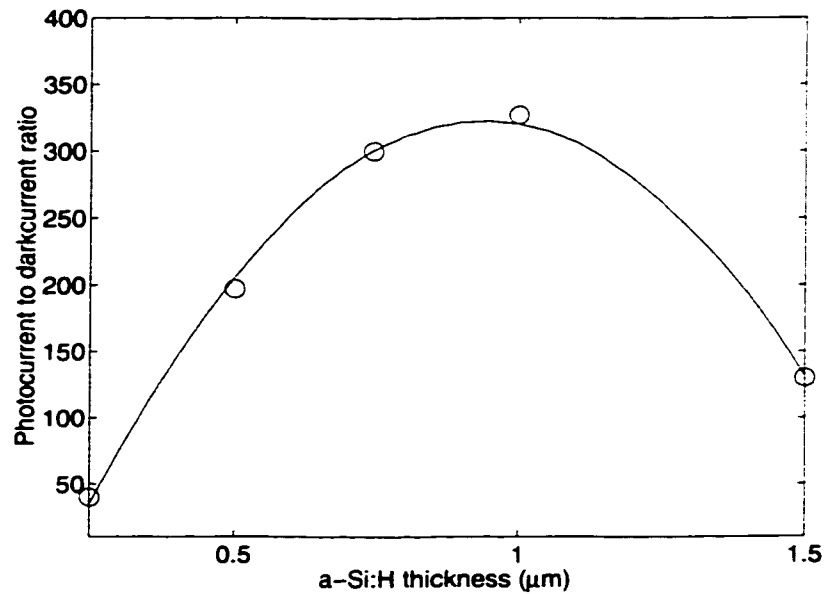
Figure 4.19: Optical response change with a-Si:H thickness.

with the slot structure is higher than that of the conventional structure, by a factor of 40 %. With the grided structure. the photocurrent is higher than the conventional counterpart. by a factor of 50 %. There are two possible processes responsible for this increase in photosensitivity: the increased light absorption (due to increased optical reflection off the non-uniform bottom electrode geometry) and the enhanced collection efficiency. as shown in Fig. 4.21. Due to low increase in photosensitivity at low bias and high increase under high bias. the enhancement in photosensitivity can be attributed to the enhanced collection efficiency.

4.5.2 Leakage Current

For a Schottky diode. the contributions to the leakage current come from thermionic emission. tunneling. bulk thermal generation. and edge effect. as illustrated in Fig. 4.22 [65]. The bulk thermal generation component arises from the excitation of
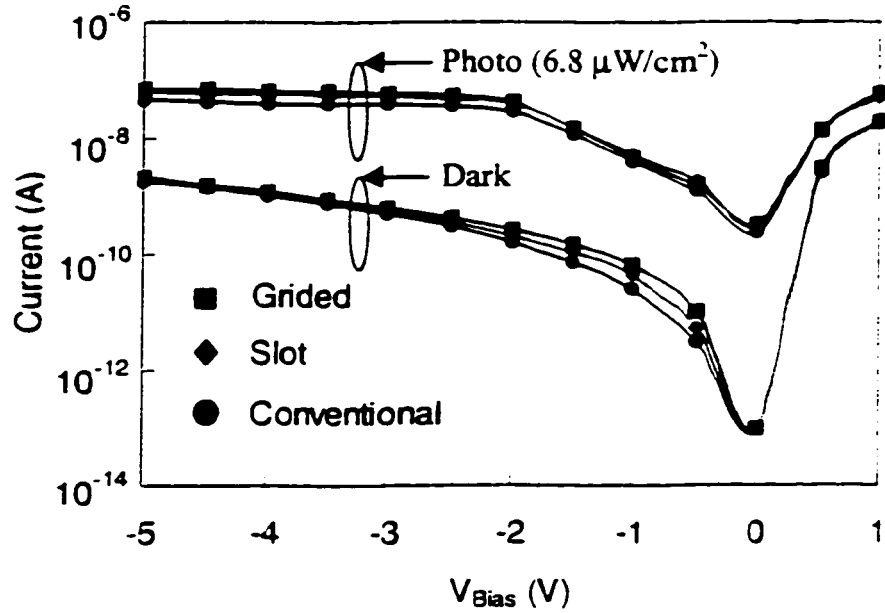
Figure 4.20: I-V characteristics for different structures of collection electrodes. The structure is shown in Fig. 4.11.

electrons from the valence band to the empty gap states, and from the filled states to the conduction band. It is a feature of the active layer and is generally in the low end of the leakage current. Edge effect usually contributes when the detection area is very small. Thermionic emission is due to the difference between the work function of metal and the Fermi energy level of a-Si:H. This is the main contributor to the leakage current for a Schottky diode. Tunneling occurs when there is a high density of defect states at the interface. This high density of interface states stems from the diffusion of oxygen and indium from the ITO into the a-Si:H, which is significant when the ITO is deposited at an elevated temperature [66]. It is generally accepted that the diffusion of indium and oxygen from the ITO into the a-Si:H leads to the increase in the density of interface states. In addition, there is instability in the leakage current, which arises not only from the generation of
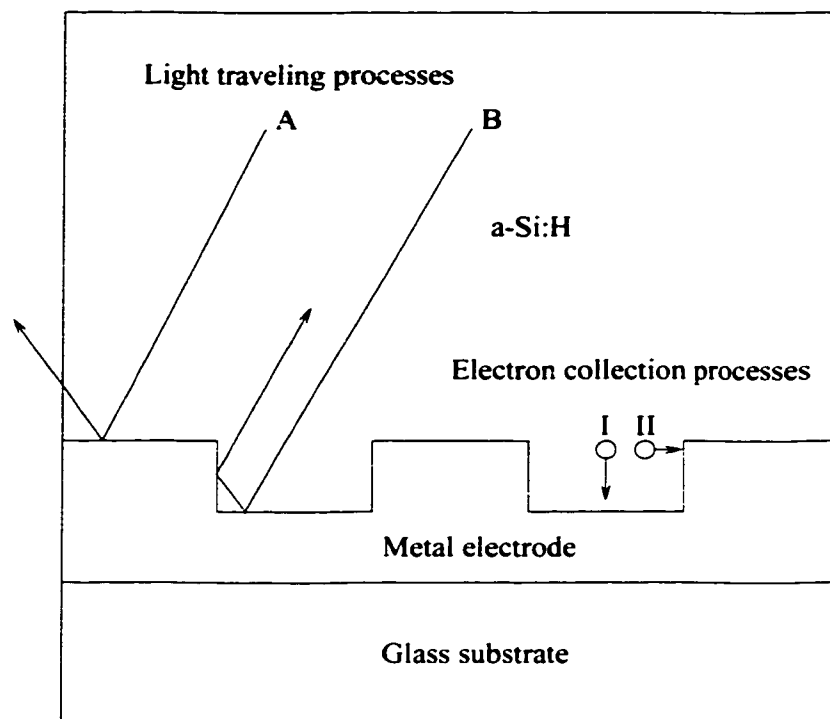
Figure 4.21: The schematic of possible processes responsible for the enhanced photosensitivity in the grided or slot structures.
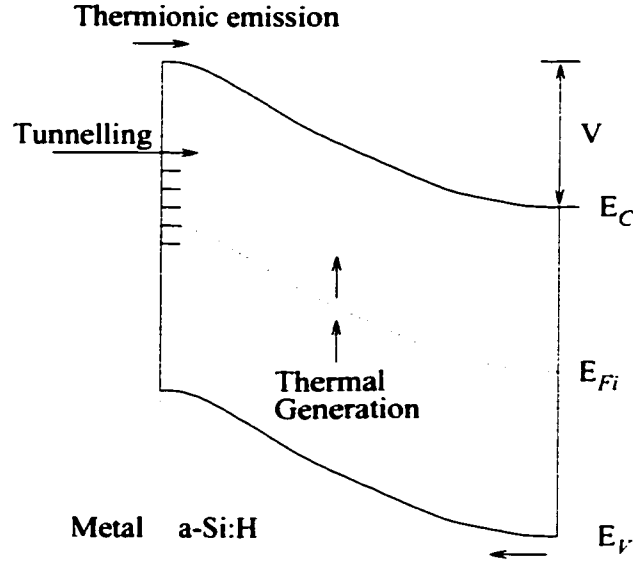
Figure 4.22: Schematic of a reverse bias Schottky sensor illustrating the possible leakage current mechanisms.

deep defect states in the intrinsic a-Si:H layer but also from the generation of defect states at the interface. This will be discussed in Section 4.5.3.

The most dominant mechanism in the Schottky barrier junction is thermionic emission and it can be written as [67].

$$J_0 = A^* T^2 e^{-q\Phi_B/kT}.$$ (4.5)

where A^* is Richardson's constant. T is temperature. q is elementary charge (1.6×10^{-19} Coulomb). k is Boltzman's constant. and Φ_B is the barrier height. If Richardson's constant of a-Si:H is 96 $Acm^{-2}k^{-2}$ and the modified barrier height is 0.97 eV. the leakage current caused by the thermionic emission at 300 K can be calculated to be 5.4×10^{-10} A/cm^2.

Bulk thermal generation also contributes to the leakage current. The capture and release of charges in the deep trapping states in the a-Si:H layer are well known.

The probability for trapping is proportional to the diode thickness and inversely proportional to the product of the carrer drift mobility. the carrier life time. and the electric field across the sensor [68]. The bulk states originate from charge generation through gap states. Electrons are excited by thermal generation. These excitations generate electron-hole pairs which are separated and collected by the internal field. The current is the product of the density of states and the excitation rate. It is given approximately by

$$J_{th} = qN(E_{qF})kT\omega_0 e^{[-(E_C-E_{qF})/kT]}d \qquad (4.6)$$

where q is elementary charge (1.6×10^{-19} Coulomb). $N(E_{qF})$ is density of states at E_{qF}. k is Boltzman's constant. T is temperature. ω_0 is excitation rate prefactor and d is the thickness of the a-Si:H film. Substituting $N(E_{qF}) = 10^{16}$ cm^{-3}eV^{-1}. and equating E_C-E_{qF} to half the mobility gap. E_{qF} is approximately at midgap. so that E_C-$E_{qF} = E_m/2 = 0.9$ eV. and $\omega_0 = 10^{13}$ s^{-1}. film thickness d is 1 μm. The thermal generation current is calculated to be 3.8×10^{-11} A/cm^2.

There is a larger thermal generation current when the voltage is first applied. This current can be described as

$$J_{th}(0) = J_{th}e^{(\Delta E_F/kT)}. \qquad (4.7)$$

where ΔE_F is the shift of Fermi level. Assuming the change of E_F is 0.1 eV. the thermal generation current can be calculated to be 1.8×10^{-9} A/cm^2.

A thin intermediate layer is formed at the interface because of surface reactions and inter-diffusion during processing. As a result. a high density of interface states is created. which can lead to tunneling conduction. The corresponding current tunneling across the barrier is approximately [69]

$$J_{leak} = J_0 e^{(E_t R_t/kT)}. \qquad (4.8)$$

where R_t is an effective tunneling length and E_t is the field at the contact. The origin of R_t is unclear hitherto and its magnitude depends strongly on deposition conditions. Assuming effective tunneling length R_t is 100 $\overset{\circ}{A}$ and the electric field E_t at the contact is 5×10^6 V/m (5 V applied to the device with 1 μm thick a-Si:H). the leakage current can be calculated to be 2.6×10^{-10} A/cm^2.

Annealing has been performed to study the mechanisms underlying the leakage current. A comparison of the leakage current characteristics is given in Fig. 4.23 for the photodiodes unannealed and annealed at 260 °C. The leakage current asso-
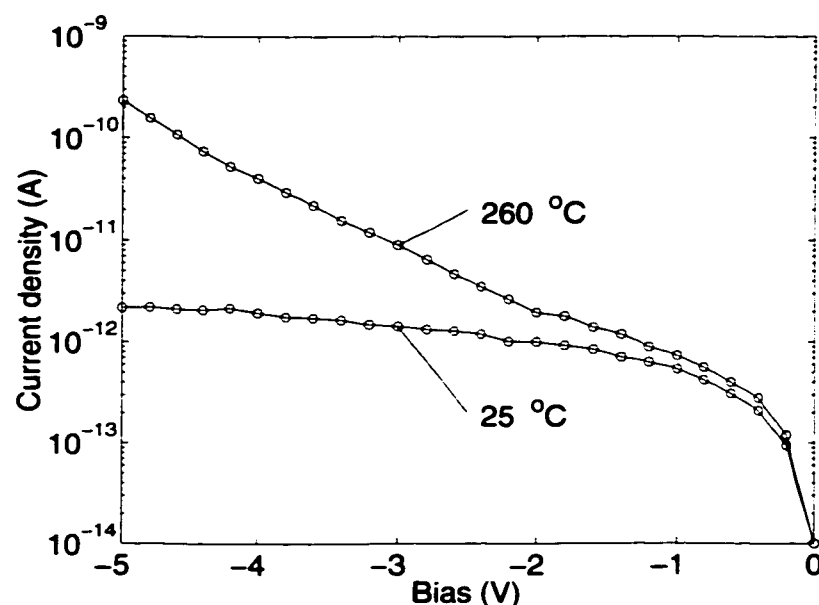
Figure 4.23: The leakage current for ITO deposited at room temperature (no annealing) and when subject to annealing at 260 °C. The diode area is 300×300 μm^2 and a-Si:H thickness 1 μm.

ciated with the ITO deposited at room temperature is about 1 pA at -2 V. This is a factor of 2 smaller than the corresponding current obtained with high temperature annealing. At high reverse voltages. the leakage current increases rapidly for the

annealed samples. The difference in leakage currents at -3.5 V is about one order of magnitude higher. This unusual voltage dependence of leakage current can be explained by examining the transport processes depicted in Fig. 4.24 [70]. As mentioned in Section 4.3.3. there is little difference in indium diffusion between low and high temperature processes. Therefore. the contribution to the increase in leakage current from indium diffusion is negligible [71]. However. there is increased oxygen diffusion into the a-Si:H layer after thermal annealing at 260 °C. The presence of oxygen creates positively charged defect states in the bulk a-Si:H layer near the interface. Therefore the increase in leakage current after high temperature annealing stems from the creation of these defect states which actively participate in tunneling. At high bias voltages. the increased band bending results in more interface states that contribute to tunneling. leading to the rapid increase in leakage current.
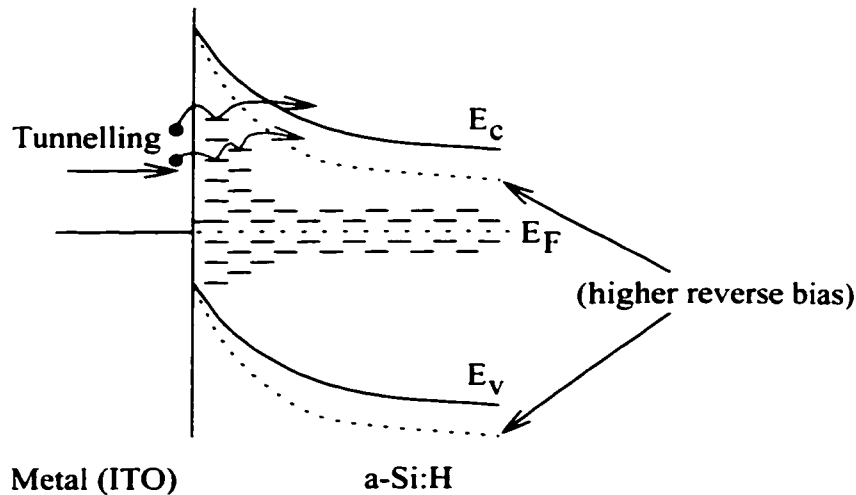
Figure 4.24: Possible tunneling processes due to the interface states and the states near the interface. The effect of bias is also indicated.

4.5.3 Instability

The shift in leakage current with time (referred as instability) for a photodiode must be as small as possible for improved imaging resolution and accuracy. In a-Si:H based devices, the leakage current is time dependent. This instability originates from a number of sources, such as the release of trapped charges, thermal generation, thermionic emission, and tunneling [20]. All these components are affected by the instabilities intrinsic to the a-Si:H material, causing large temporal variations of the reverse current [72].

Fig. 4.25 shows the shift in leakage current at a long time scale. At low reverse voltages, the shift in leakage current is insignificant, for example, the shift stabilizes to a value less than 9% when biased at -2 V. With increasing reverse voltage, the shift in leakage current increases but not dramatically. Even at high reverse voltages (V_{rev}=-10 V), the leakage current changes by a factor less than 3. This is much smaller than that observed in Mo/a-Si:H Schottky diodes [73].

An expanded view of the time-dependence leakage current behavior at the initial stages after the bias voltage is applied is plotted in Fig. 4.26. When the photodiode is biased at -10 V, an initial decay in the current for about 1.4 s is observed, followed by a slow increase. When biased at -5 V, the initial decay takes about 5 s. However, when biased at -2 V, the current decreases with time before reaching the steady state. Since the current is observed not to increase with time (as in the previous two reverse voltages), this implies that the contribution to the leakage from tunneling is smaller than that at high bias voltages.

These results can be explained as follows. At the initial stages, the decrease in leakage current can be attributed to charge depletion from active a-Si:H layer. However, in the a-Si:H layer, a prolonged bias induces metastable changes. This can
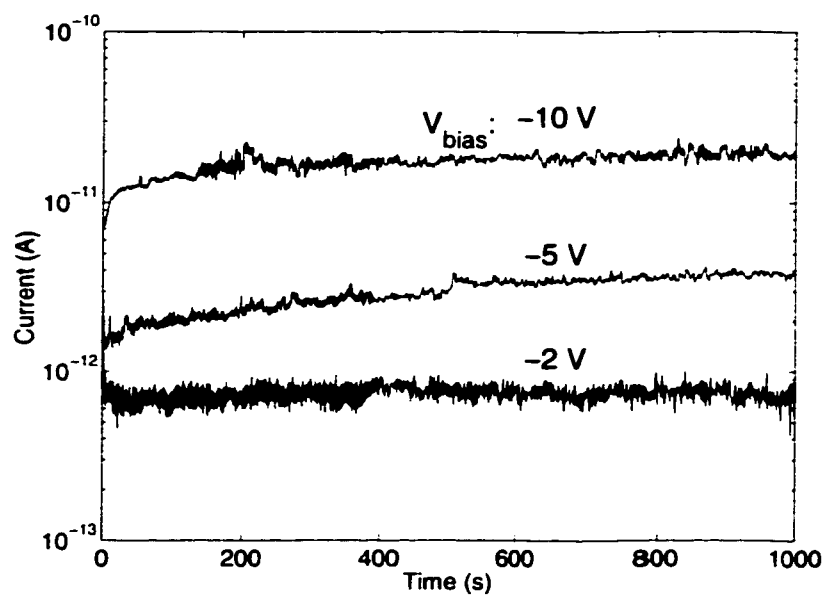
Figure 4.25: Leakage current shift: long time scale.
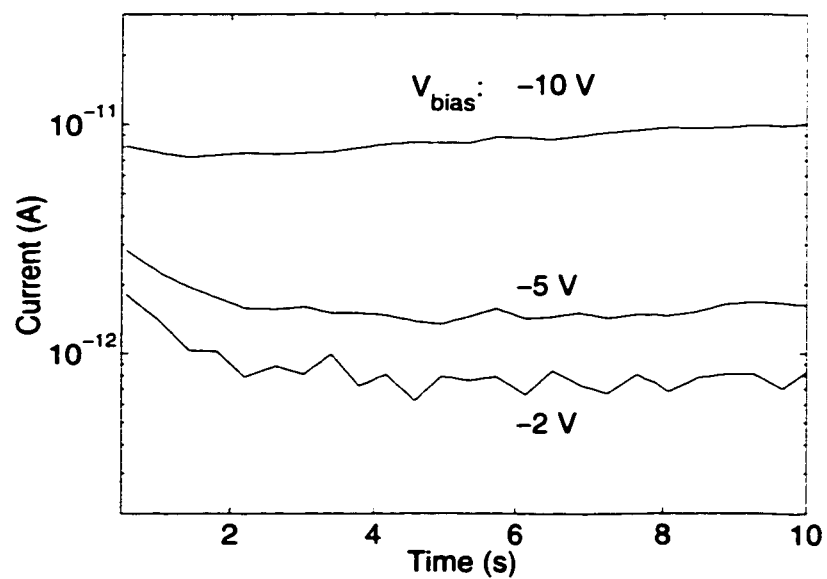
Figure 4.26: Leakage current shift: short time scale.

be attributed to the possibility of alternative bonding configurations of each atom. which leads to a strong interaction between the electronic and structural states and causes the phenomenon of metastability. As a result. the carrier transport in the a-Si:H layer would be time dependent. On one hand. the process of electron releases from traps and electron trapped in the shallow states occurs, leading to a dispersive transport (see Fig. 4.27). On the other hand. the change in trap density and interface states is significant when Schottky diode is reverse biased. At low biases. the shift is small because the change comes only from trap discharge. thermal generation. and thermionic emission. For high biases. however. the shift in leakage current increases greatly. This can be explained by the increased interface states due to the high electric field. which in turn enhances the tunneling.
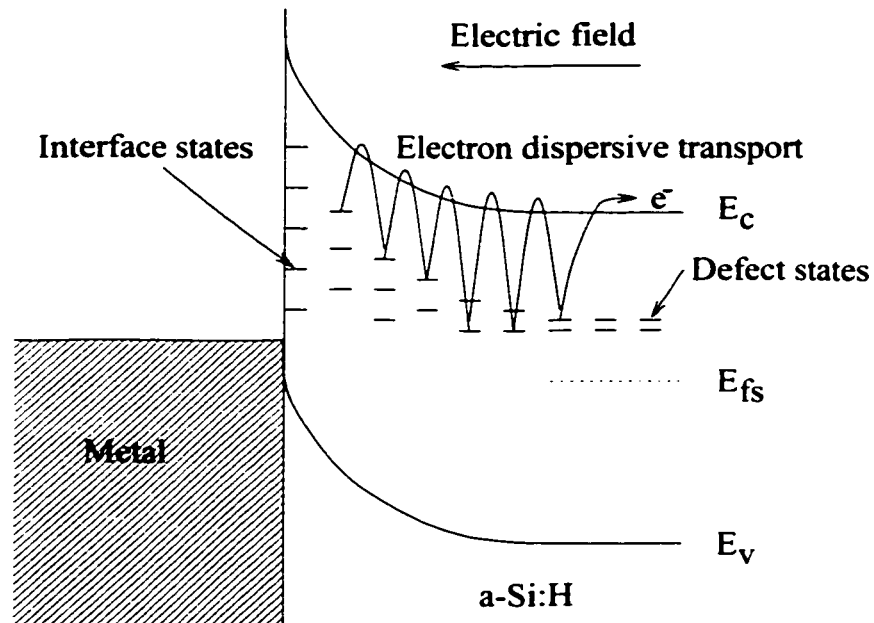
Figure 4.27: Electron transport in an a-Si:H Schottky diode at reverse bias.

4.5.4 Spectral Response

The spectral response was measured using the system shown in Fig. 4.28. The monochromatic light was generated with Sciencetech 150 W arc lamp system. A power meter was used to measure the light intensity before the photodiode was placed. The lens was used to increase the light uniformity at the measured area. Fig. 4.29 illustrates the variation of photocurrent with wavelength. It is observed that the maximum output response current occurs at around 600 nm.
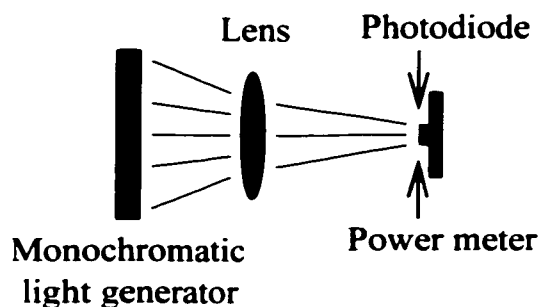
Figure 4.28: Spectral response measurement set-up.

Overall, the spectral sensitivity decreases as λ increases beyond 600 nm, due to the low optical absorption and hence increased penetration depth in the a-Si:H in the red region of the spectrum (see Table 4.5). For example, the penetration depth is 100 μm at a wavelength of 780 nm. At low wavelength, on the other hand, as λ decreases towards the blue region (e. g. 450 nm) of the spectrum, spectral sensitivity decreases. This can be attributed to: small transmittance through the ITO layer and reflection losses in the ITO, strong surface absorption leading to low collection efficiency since the penetration depth is merely within 0.03 μm of the active a-Si:H layer.

The spectral response can be quantified by the behavior of the extrinsic quantum efficiency (η) at the different wavelength. The quantum efficiency is defined as the
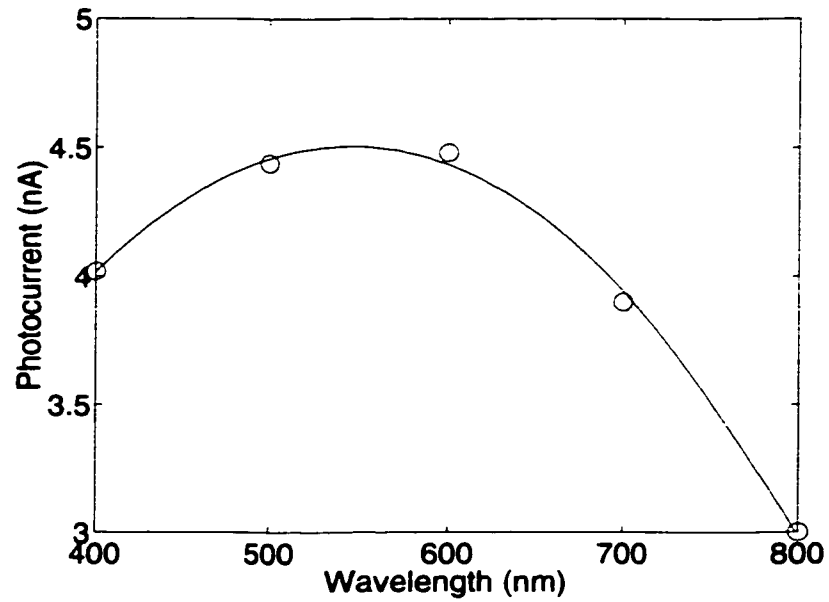
Figure 4.29: Spectral response of a Schottky photodiode under the bias of -5 V. The diode area is 300×300 μ^2 and a-Si:H thickness 1 μm.

Table 4.5: Light absorption in a-Si:H film. Adapted from [74] [75].

Wavelength (nm)	Penetration depth in a-Si:H (μm)
450	0.02 – 0.03
510	0.2
600	2
780	100

ratio of the number of collected photocarrier pairs to the number of incident photons and is limited by three factors: light losses through the ITO and at the ITO/a-Si:H interface. the limited light absorption in the a-Si:H layer. and the collection efficiency of photogenerated electrons. It is calculated as

$$\eta = \frac{No.\ of\ collected\ electrons}{No.\ of\ incident\ photons}$$
$$= \frac{I/q}{WA/E_{photon}}. \tag{4.9}$$

where I is the measured photocurrent. t the collected period. q the elementary charge. W the light intensity. A the sensor area. and E_{photon} the photon energy.

Fig. 4.30 shows the quantum efficiency as a function of wavelength retrieved from (4.9) using measured values of the photocurrent and the light intensity. The quantum efficiency reaches a maximum of 0.5 at a wavelength of 600 nm. which is consistent with the spectral response. as shown in Fig. 4.29.
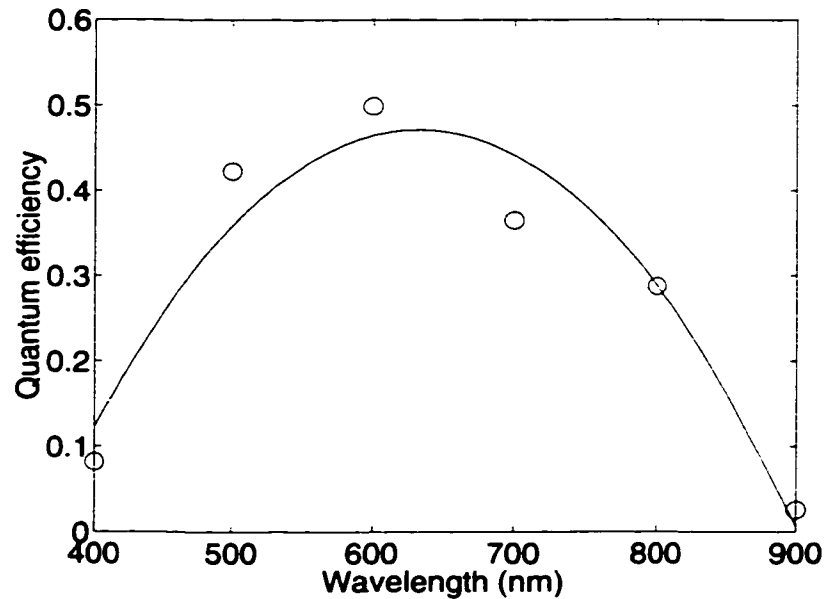
Figure 4.30: Quantum efficiency vs wavelength.

4.5.5 X-ray Sensitivity

Based on its optical response. the photodiode can be used as an X-ray detector if it is coupled with a phosphor layer. This phosphor layer can be a commercial film placed on the top of the photodiode or can be intimately coupled with a photodiode (see Fig. 4.31). We adopted the former one to demonstrate the detection feasibility using the above photodiode. The latter one is under development in order to improve the detection resolution when used in large-area imaging. In this work. the phosphor layer is commercial KODAK MIN-R screen (Gd_2O_2S).
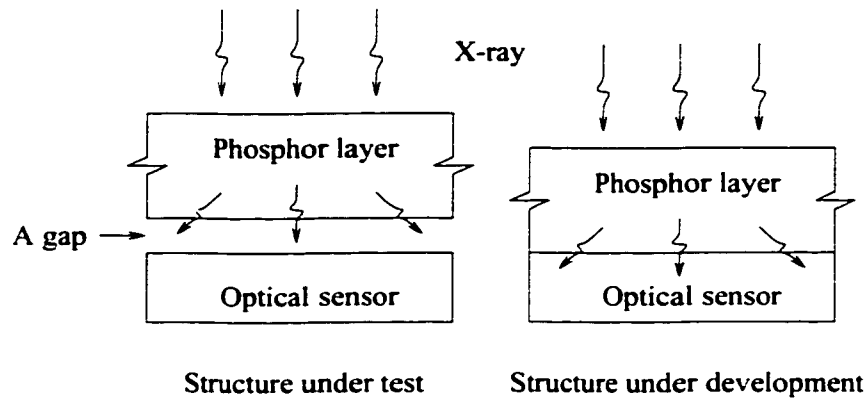
Figure 4.31: X-ray detection using a phosphor layer coupled with an optical sensor.

Fig. 4.32 shows the dependence of X-ray response with X-ray source voltage (kVp) for a detector with the area of 100×100 μm^2 and a-Si:H thickness of 0.5 μm. Here. bias voltage was chosen at -2 V due to its low shift in leakage current with time. The response is comparable with that observed for a Mo/a-Si:H detector [72]. However. we observe a slight nonlinearity with the detector-phosphor arrangement presented here. This nonlinearity is believed to be due to phosphor. which characteristically depicts an "S-type" response.
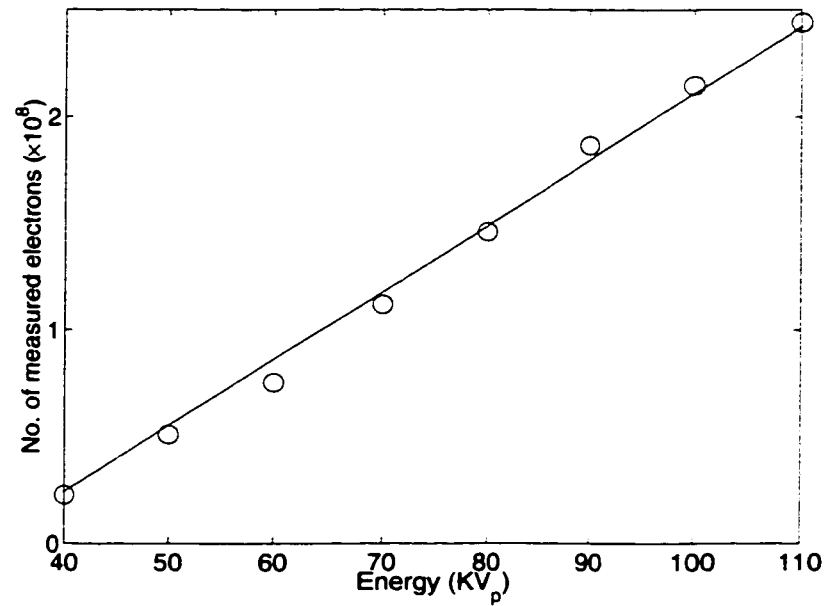
Figure 4.32: X-ray sensitivity of a $Gd_2O_2S/ITO/a$-Si:H detector for various X-ray source voltages (kVp) with 100 mAs. collected over a period of 500 ms. The detector area is 100×100 μm^2.

4.6 Summary

In this chapter. the operating principle of the ITO/a-Si:H Schottky photodiode was described. The device was designed based on the considerations of the capacitance. the thickness of relevant films. the geometry of collection electrode. and breakdown voltage. An optical sensor based on the Schottky barrier has been developed using polycrystalline ITO film deposited at low temperature. Photosensitivity was optimized by the change of the thickness of a-Si:H active layer and the geometry of the collection electrode. The interface integrity between the ITO and the a-Si:H was optimized using SIMS measurements for the profiles of oxygen and indium. The underlying mechanism of the generation of leakage current was studied by the performance of the effects of annealing. The spectral response was measured and the performance was discussed. Finally. X-ray sensitivity was measured for a photodiode coupled with a phosphor layer.

Chapter 5

Characterization of Thin Film Transistors

a-Si:H TFTs are widely used as switching elements in large area electronics such as liquid crystal displays, and more recently in optical and X-ray image sensor arrays. However, several issues still remain to be solved, such as stability and leakage, which limit their widespread use as commercial devices in large area electronics. The instability of a-Si:H TFTs, i.e. the variation in threshold voltage (ΔV_T) after prolonged gate bias (see Fig. 5.1), should be low to enable fast read out of the signal in large-area imaging arrays. Two models have been proposed to account for this threshold shift: charge trapping in the silicon nitride gate insulator and the metastable creation of new defect states in the amorphous silicon. The latter occurs when the TFT is biased into strong accumulation. The experimental results show that the state creation is the dominant mechanism at the lower voltage, but the charge trapping dominates at the higher voltage [76]. The leakage current in these TFTs has been identified to stem mainly from the injection of holes near the
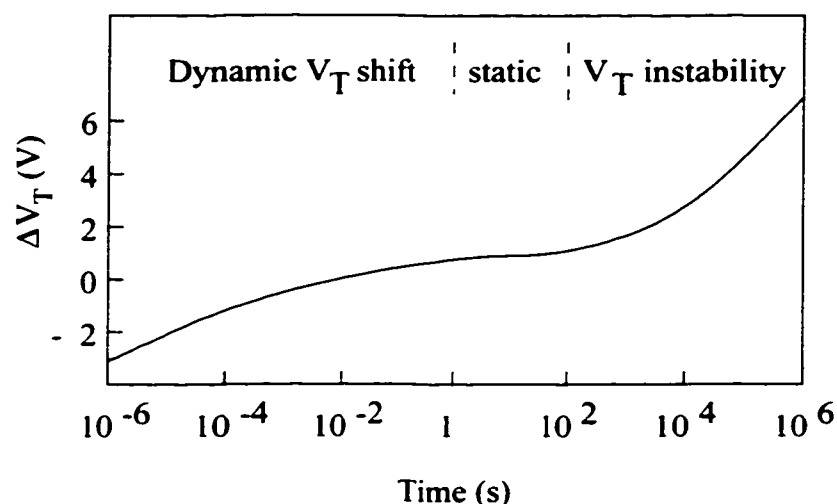
Figure 5.1: Time dependence of the threshold voltage shift after the application of a positive bias of 12 V [76].

drain region and from ohmic conduction associated with diffusion of phosphorous atoms into the a-Si:H layer from highly doped μc-Si:H (source and drain contact layers). The leakage current should be small enough for the retention of the charge on the pixel during the OFF-state of the TFT.

In inverted staggered TFT structures. since the top nitride layer is in direct contact with the active a-Si:H region. it can influence the performance of the TFT [77]. While there have been few reports relating the integrity of the top nitride on stability. its effect on the leakage current has hardly been broached. Nakamura et al. [78] have attributed the instability to electron injection from the a-Si:H into the nitride. However. the nitride layer in their samples was not varied in nitrogen content. In contrast. Choi et al. [79] have associated the instability in their TFTs with hole trapping at the top a-Si:H/a-SiN$_x$:H interface. and have proposed an

experimental procedure to separate the effects of the top and gate nitride on the instability. More importantly. Possin et al. [80] have reported that the effects of top nitride quality on the TFT stability are insignificant if the thickness of a-Si:H layer is greater than 100 nm. It is clear from the above studies that the top nitride affects TFT stability. However. the extent to which it influences the shift in threshold voltage and how this shift depends on nitride composition were not reported. In particular. in samples with a thin a-Si:H layer. the composition of the nitride determines. to a large extent. the degree of carrier injection. Following these considerations. a systematic characterization of the stability and leakage with respect to the composition of the top nitride layer was performed. In this research. gas ratios of NH_3 and SiH_4 were varied.

5.1 a-Si:H/a-SiN$_x$:H Interface

For an a-Si:H TFT. the most popular structure is inverted staggered (see Fig. 5.2) because the gate insulator a-SiN$_x$:H can be deposited at higher temperatures than the a-Si:H active layer. Therefore. an a-SiN$_x$:H layer with high quality can be obtained and a good interface can be achieved between the gate and the active layer. As compared to the staggered structure. the inverted staggered structure has smoother interface morphology and sharp transition of compositions between gate insulator and active layer.

TFTs have are two different interfaces between a-Si:H and a-SiN$_x$:H. One is between the a-Si:H and the a-SiN$_x$:H layer (where the a-SiN$_x$:H is the bottom or gate nitride in TFT) and the other is between the a-SiN$_x$:H and the a-Si:H layer (where the a-SiN$_x$:H is the top or passivation nitride in TFT). The difference between them can be explained by the observation that the bottom nitride interface
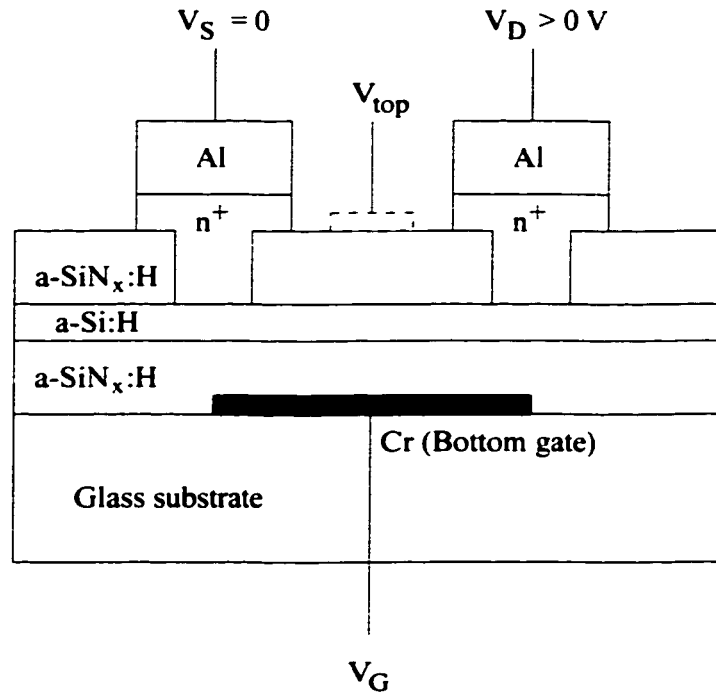
Figure 5.2: Thin film transistor structure.

forms when the NH_3 is pumped out of the deposition system in order to grow a-Si:H while top nitride interface forms with NH_3 exposure to the a-Si:H surface [81].

(A) a-Si:H on a-SiN_x:H

The interface width associated with this structure is determined to be of the order of 10 $\overset{\circ}{A}$. arising from the reactive nature of the plasma [82]. It is known that ammonia tends to linger in the reactor by sticking to the chamber wall and can significantly increase the nitrogen concentration by up to three orders of magnitude in a subsequently deposited bulk a-Si:H film. Once the NH_3 radical is trapped at the a-Si:H surface. it would be donor-like. acquiring a positive charge and liberating an electron. The presence of donors in bulk a-Si:H generates a large number of dangling bonds due to the shift of the Fermi energy. Hence the presence of positive

species at the a-Si:H surface might give rise to a large density of interface defects.

(B) a-SiN$_x$:H on a-Si:H

When a-SiN$_x$:H is deposited on a-Si:H. the a-Si:H surface is exposed to the SiH$_4$-NH$_3$-H$_2$ plasma. and some nitrogen atoms permeate and distort the network because of their small size. They break weak bonds to make Si-N bonds. thereby emitting electrons. A graded N-rich. maybe including H. region was observed in the a-SiN$_x$:H layer on a–Si:H (top nitride) interfaces. The fast electronic states at the interface are thought to be located in the a–Si:H layer. with a higher density in the top nitride than in the bottom nitride configuration [83].

5.2   The Basic Operation of Thin Film Transistor

The band bending and the occupancy of the electronic states with a simple density of states diagram can be used to describe the operation of TFT. (see Fig. 5.3) [76]. At zero gate voltage the energy bands are close to the flat-band condition. For a positive gate voltage. less than the threshold voltage. the energy band bends downward and the Fermi level moves through the deep states. which then get occupied. At the same time. some space charges are located in the band-tail states. but the occupancy of these states is low. This is because they are well above the Fermi level and so the total space charges are dominated by the deep states. The increase in the source-drain current is due to the small fraction of the band-tail electrons above the conduction band mobility edge. The space charges in the deep states increase proportionally to the increase in gate voltage. but the current increases exponentially. as the band-bending increases. If the density of the deep states between the Fermi level and the tail states was constant. then

the prethreshold slope in the logarithmic transfer characteristics would be roughly inversely proportional to the square root of the density of states.

Above the threshold voltage, the space charge in the band-tail states exceeds the space charge in the deep states, even though the Fermi level is still below the tail states. Both the total space charge and the source-drain current increase linearly with the applied gate voltage and we have a well defined field-effect mobility. The mobility is thermally activated with an activation energy given by the width of the tail states, and not by E_C-E_F.

$$V_G = V_T \qquad V_G < V_T \qquad V_G > V_T$$

Band bending profiles

$$n_{DEEP} > n_{BT} \qquad n_{DEEP} < n_{BT}$$

Occupancy of states
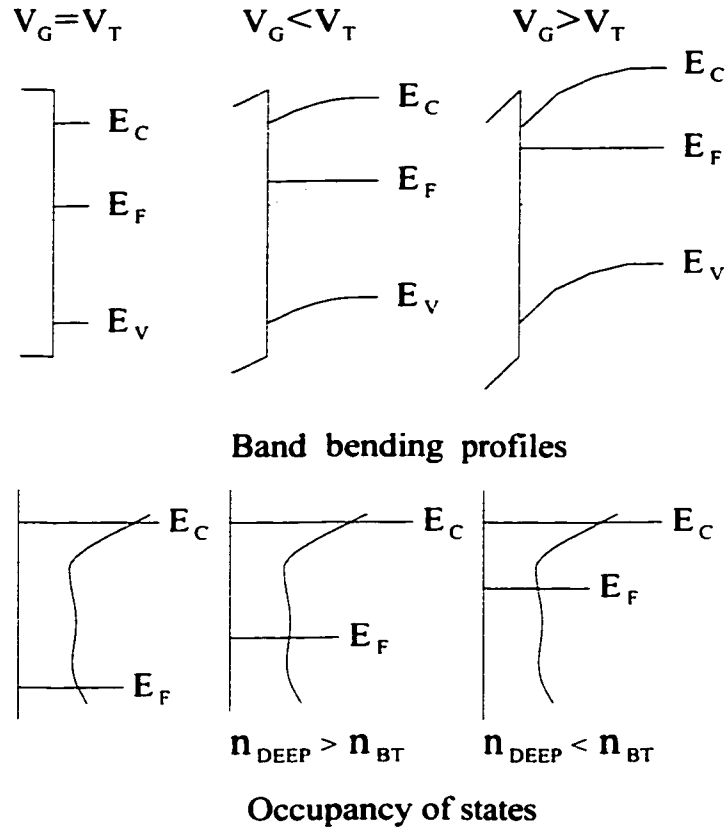
Figure 5.3: Basic operation of an a-Si:H TFT [76].

The description of the terminal behavior in TFTs is similar to that of c-Si

MOSFETs. The accumulation charge (per unit channel area) is given by [84]

$$Q(x) = C_G[V_G - V_T - V(x)]. \tag{5.1}$$

where C_G is the gate capacitance per unit area. V(x) is the voltage along the channel (x=0 @ source and x=L @ drain).

The drain current along x is then:

$$J_D(x) = wQ(x)\mu_{FET}E(x). \tag{5.2}$$

which can be expanded to read:

$$J_D(x) = W\mu_{FET}C_G[V_G - V_T - V(x)]\frac{dV(x)}{dx}. \tag{5.3}$$

Integrating from the source (x=0) to the drain (x=L) yields

$$J_D = \mu_{FET}C_G\frac{W}{L}[(V_G - V_T)V_D - \frac{1}{2}V_D^2]. \tag{5.4}$$

In the linear region.

$$J_D = \mu_{FET}C_G\frac{W}{L}(V_G - V_T)V_D. \tag{5.5}$$

and in saturation.

$$J_{DSAT} = \frac{1}{2}\mu_{FET}C_G\frac{W}{L}(V_G - V_T)^2. \tag{5.6}$$

5.3 Design

The TFT with the structure shown in Fig. 5.2 is designed with geometry parameters listed in Table 5.1. Due to the low electron mobility ($\sim$ 1 cm^{2}V^{-1}s^{-1}). the W/L ratio is required to be large in order to achieve the necessary on-current. The gate capacitance per area is

$$C_G = \epsilon\,\frac{1}{d} \tag{5.7}$$

where d is the gate insulator thickness and ϵ is the permittivity of the gate insulator. For a TFT with d = 250 nm. ϵ = $8.85 \times 10^{-14} \times 7.5351$. the capacitance per area is 2.667×10^{-8} F/cm^2.

Table 5.1: TFT geometry design parameters.

W/L (μm/μm)	200/20
a-Si:H thickness (nm)	50
n$^+$ μC-Si thickness (nm)	50
Gate a-SiN$_x$:H thickness (nm)	250
Top a-SiN$_x$:H thickness (nm)	200
Al thickness (μm)	1
Bottom electrode (Cr or Mo) thickness (nm)	100

5.3.1 On-Resistance

On-resistance reflects the drive-ability of the TFTs. It can be described as [85].

$$R_{on} = \frac{1}{\mu_{FET} C_G \frac{W}{L} (V_G - V_T)}.$$
(5.8)

where W is the gate width. L is the gate length. V_G is the gate voltage. and V_T is the threshold voltage. We use W/L = 200μm/20μm and the on-resistance biased at 5 V for V_T = 2 V is 1.2×10^6 Ω.

5.3.2 Time Delay

Time delay in a-Si:H TFTs is also a concern due to the low mobility ($\sim$ 1 cm^{2}V^{-1}s^{-1} for electrons) when used in the fluoroscopy imaging. It is found to be directly

proportional to the square of the channel length and inversely proportional to the effective drive voltage [86].

$$t_d \leq \frac{L^2}{\mu_{FET}(V_G - V_T)} \tag{5.9}$$

If the effective channel length L is 20 μm. the mobility μ_{FET} is 1 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$. the gate voltage is 5 V. and the threshold voltage V_T is 2 V. the transit time is 1.33×10^{-6} s. Therefore. the length is required to be as small as possible. In our process. the minimum lithographic accuracy is about 5 μm and the gate length is chosen to be 10 μm.

5.3.3 Overlap Capacitance

Overlap capacitance introduces the feed-through charges and degrades the TFT transit characteristics. To minimize its value is very important especially for large area arrays because the capacitance in each pixel would be added to a large value and consequently undermines the array performance. Based on our facility. we design overlap distance with 2 μm. 5 μm. and 10 μm. Its further discussion has been done elsewhere [87].

5.3.4 Photosensitivity

For TFTs which are used as switching elements. it is required to reduce or eliminate the photosensitivity. Currently the following practical schemes are used to achieve this goal [88]: a shield layer and thining the a-Si:H layer. Using a light shield is very simple and is commonly used without any extra masking steps in the fabrication. Thinning the a-Si:H to reduce the photosensitivity is feasible and depends on the TFT structure.

5.4 Fabrication

The TFTs used in this work are based on the conventional inverted staggered structure. Corning 7059 glass wafers were used as the substrate material. After depositing and patterning the Cr gate metal on these glass substrates. 250 nm of gate a-SiN$_x$:H. 50 nm of a-Si:H layer. and 250 nm of top a-SiN$_x$:H were deposited in a parallel-plate electrode plasma enhanced chemical vapor deposition (PECVD) system within one vacuum-pump-down cycle to minimize the density of defect states at the interfaces. The composition of the top nitride was varied in terms of the NH$_3$/SiH$_4$ gas ratios. At the source and drain regions. a highly doped microcrystalline (n$^+$ μc-Si:H) layer was employed to reduce the contact resistance. The overlap of the source and drain over the bottom gate was varied from 2 to 5 μm. For the source and drain contacts. we employed a 1 μm Al film. which also served as the interconnect and pad metalization. In some samples. we also deposited and patterned a thick 1 μm Al film to serve as a top gate (see Fig. 5.2). The deposition conditions are given in Table 5.2. The process sequence is shown in Fig. 5.4 and its top view of fabricated TFT is shown in Fig. 5.5.

5.5 Process Optimization of Passivation a-SiN$_x$:H

It has been reported that nitrogen to silicon ratio (x) in a-SiN$_x$:H affects the characteristics of the interface between the a-SiN$_x$:H and a-Si:H. Table 5.3 shows the surface density of charged defects (σ_D) for different nitrogen to silicon ratio (x) in the a-SiN$_x$:H [89]. It is observed that the surface density of charged defects depends strongly on the composition of x, with a maximum value near $x = 1.0$.

The active layer in TFTs is chosen to be thin (in the range of 100 to 1000$\overset{\circ}{A}$) to

1. Bottom (Gate) electrode formation (Mask #1)
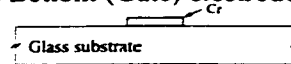
2. a-SiNx/a-Si:H/a-SiNx deposition and
   drain/source contact opening (Mask #2)
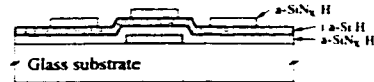
3. n+ μC-Si/SiN depositions and contact definition (Mask #3)

4. Contact area opening (Mask #4)
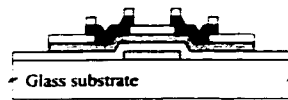
5. Al sputtering and wire bonding (Mask #5)
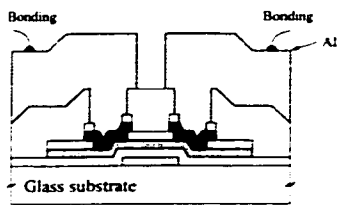
Figure 5.4: Process sequence for thin film transistor.
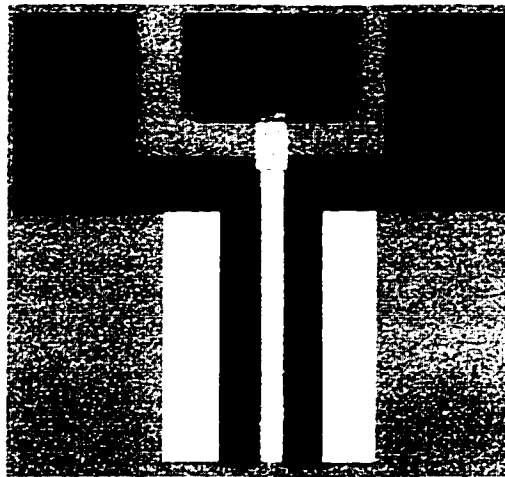
Figure 5.5: Top view of fabricated thin film transistor.

Table 5.2: Deposition conditions of a-Si:H TFTs.

Layer	Pressure (Torr)	Power (W)	Sub. temp. (°C)	Gas ratio
Mo (gate metal)	5×10^{-3}	400	RT	–
Gate a-SiN$_x$:H	0.5	110	260	$\frac{NH_3}{SiH_4} = 20$
a-Si:H	0.5	12	260	
Top a-SiN$_x$:H	0.5	110	260	$\frac{NH_3}{SiH_4} = 5. \ 10. \ 20. \ 25$
Al (final metal)	5×10^{-3}	400	RT	–

Table 5.3: The surface density of charged defects σ_D with respect to the nitrogen to silicon ratio (x) in a-SiN$_x$:H.

N/Si (x)	0.68	0.78	0.93	1.25	1.33
σ_D (cm^{-2}) $\times 10^{12}$	4.7	5.0	7.1	5.7	3.6

minimize the photosensitivity and also the leakage current due to thermal generation. As a result. the characteristics of the interface have a significant impact on the device characteristics. The presence of electron accumulation layers affects the electrical properties of TFTs. Depending on device structures the nitride can be deposited before or after the silicon layer (referred to as bottom and top nitride. respectively). An electron accumulation at the gate interface produces a negative shift in the device's threshold voltage V_T but no change in the mobility. An electron accumulation at the passivation layer interface shifts the V_T and increases the leakage current. as to be discussed in Sections 5.6.3 and 5.6.4.

Low leakage current and high stability are two key desired features in large area

imaging. The work undertaken in this project focused on the role of top nitride layer composition on stability and leakage. In this section. the characterization of a-SiN$_x$:H composition is discussed in terms of deposition process.

The composition of the top nitride layer in the fabricated samples was characterized using the measurements of Fourier Transform Infrared (FTIR) (see Fig. 5.6) and Rutherford Backscattering Spectroscopy (RBS). It is found that films de-
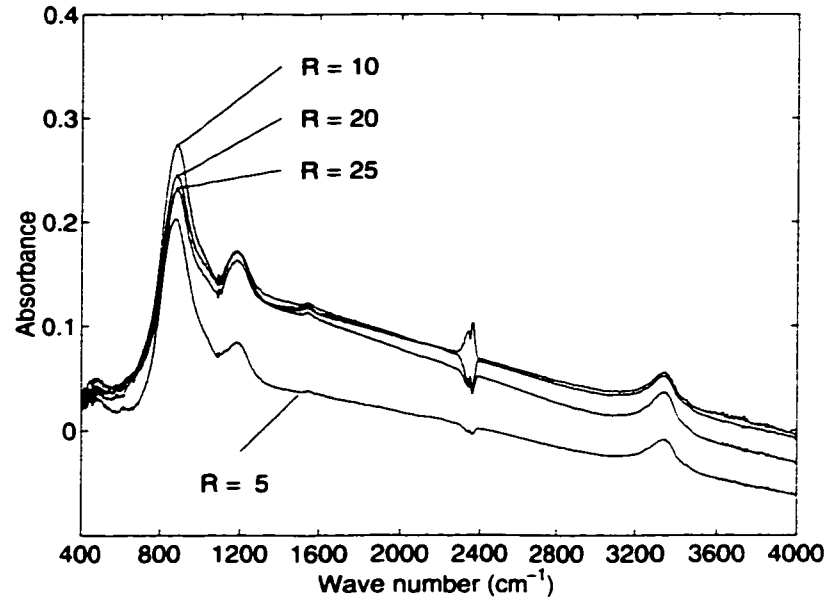
Figure 5.6: Top a-SiN$_x$:H FTIR measurements for different NH$_3$/SiH$_4$ gas ratios.

posited at high NH$_3$/SiH$_4$ gas ratios (R = 20 and 25) are nitrogen rich. Also. it is found that when R > 20. the nitride composition of the a-SiN$_x$:H saturates. i.e.. x goes up slowly to 1.52 (see Fig. 5.7). At this composition. the presence of NH groups is promoted thus reducing the coordination of Si atoms bonded to nitrogen and hydrogen. This is in contrast to films deposited at low gas ratios (R = 5). which are silicon rich ($x \sim 1.1$).
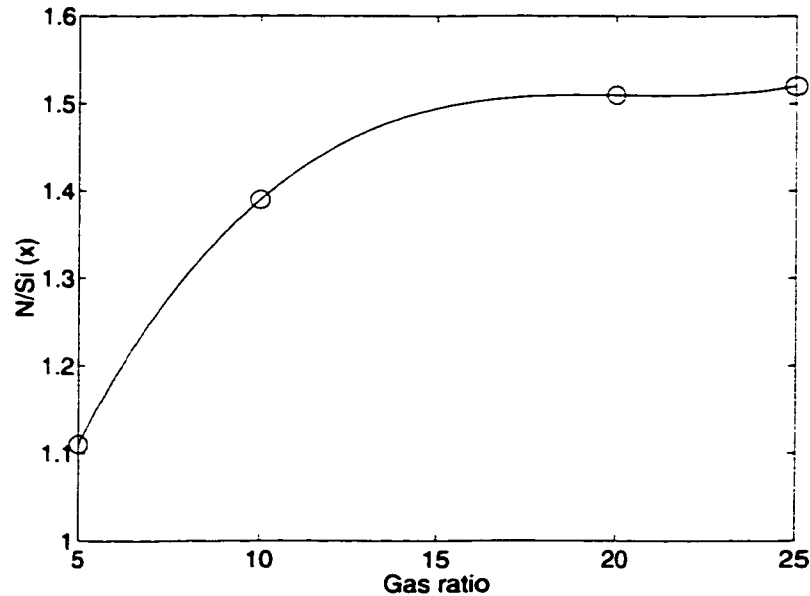
Figure 5.7: N/Si change with NH_3/SiH_4 gas ratio.

5.6   Characterization of TFTs

All measurements were performed using the Keithley 236 source measurement units. The variation in device characteristics, for a large variety of samples at each aspect ratio (W/L) was less than 5%. The threshold voltage was determined from the intercept of the $(I_D)^{1/2}$ vs V_G curves. The bias stress was applied on these TFTs in two different ways:

1. A positive voltage of 25 V was applied to the bottom gate for a duration of 5, 15, 30 and 60 minutes. Here, both the source and drain electrodes of the TFTs were grounded to preserve electrical field symmetry in the a-Si:H layer.

2. A positive voltage of 25 V was applied to the top gate electrode for the duration of 5,15, 30 and 60 minutes, also keeping the source and drain electrodes grounded.

To restore the initial transfer characteristics. the a-Si:H TFTs were annealed at 170 °C for 30 minutes before each bias stress measurements.

5.6.1   Current–Voltage Characteristics

The current-voltage (I–V) characteristics are shown in Fig. 5.8 for a TFT with the aspect ratio (W/L) of $200\mu m/20\mu m$ at different gate biases. The saturation drain current at $V_G = 10$ V reaches 10^{-5} A. which agrees very well with the value calculated by (5.4).
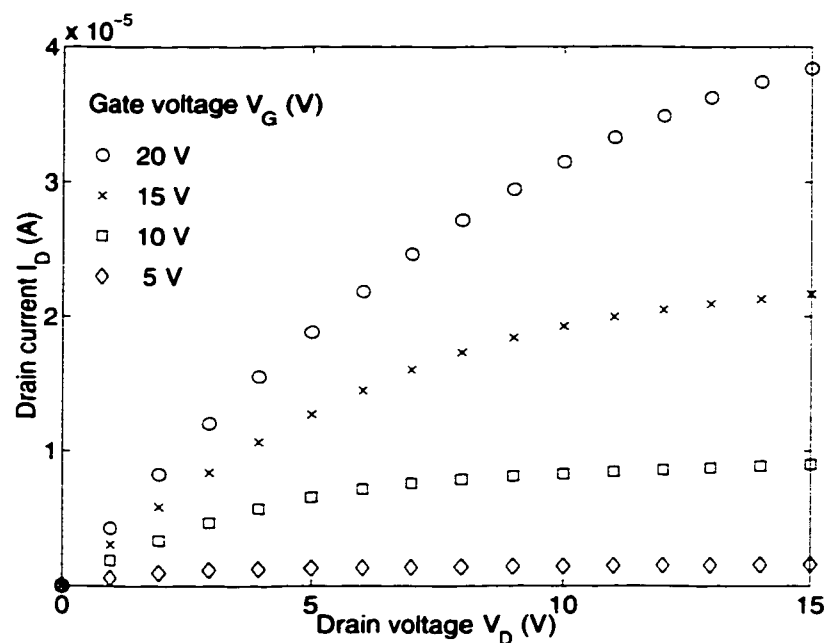
Figure 5.8: a-Si:H TFT I-V characteristics.

5.6.2   Transfer Characteristics

TFT transfer characteristics are shown in Fig. 5.9. When V_D is small (0.1, 1 V), the saturation current increases with V_D. However, when V_D is larger than a specific value, for example, 5 V, the saturation current tends to reach the same value even though V_D increases. Here, the on-current reaches 10^{-5} A when the drain voltage is 10 V. The leakage current at a gate voltage of -5 V is 2×10^{-13} A. The ON-OFF current ratio is 5×10^7 and the mobility is 1 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$.
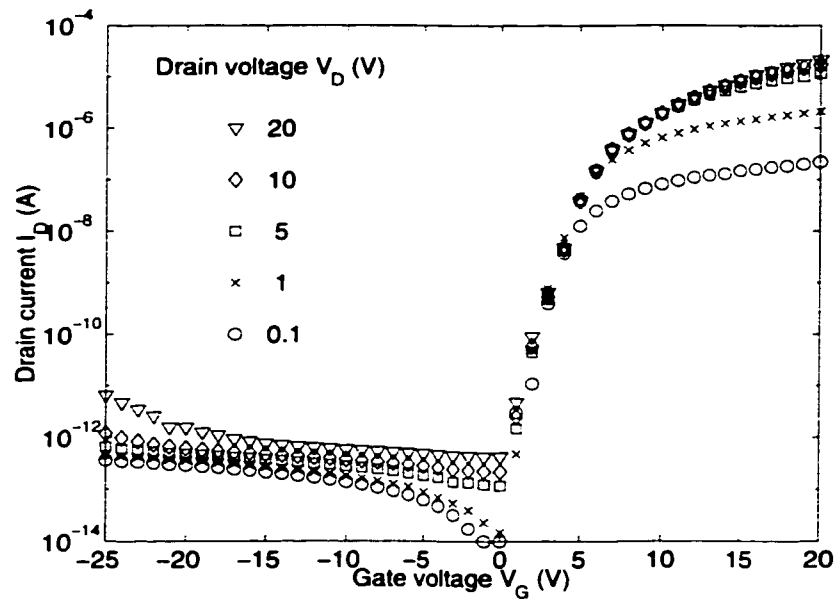
Figure 5.9: TFT transfer characteristics.

5.6.3   Stability

After a prolonged gate bias-stress, the threshold voltage (V_T) of a-Si:H TFTs undergoes a shift whose value and direction depend on the stress conditions [76]. There are two main mechanisms proposed to explain the bias-stress induced V_T

shift (ΔV_T). One is the charge trapping in the gate insulator and the other is the defect creation in the electronic band gap of a-Si:H near the a-Si:H/a-SiN$_x$:H (gate) interface.

Recently there have been reports discussing the effect of passivation layer on V_T shift [90]. The variation of threshold voltage with bias stress for the different nitrides is shown in Fig. 5.10. Here. the threshold voltage is measured after the application of a positive 25 V to the (bottom or top) gate for durations of 5. 15. 30 and 60 minutes. It is observed that when gas ratio is high. the shift in V_T is very small compared to that at low gas ratios.
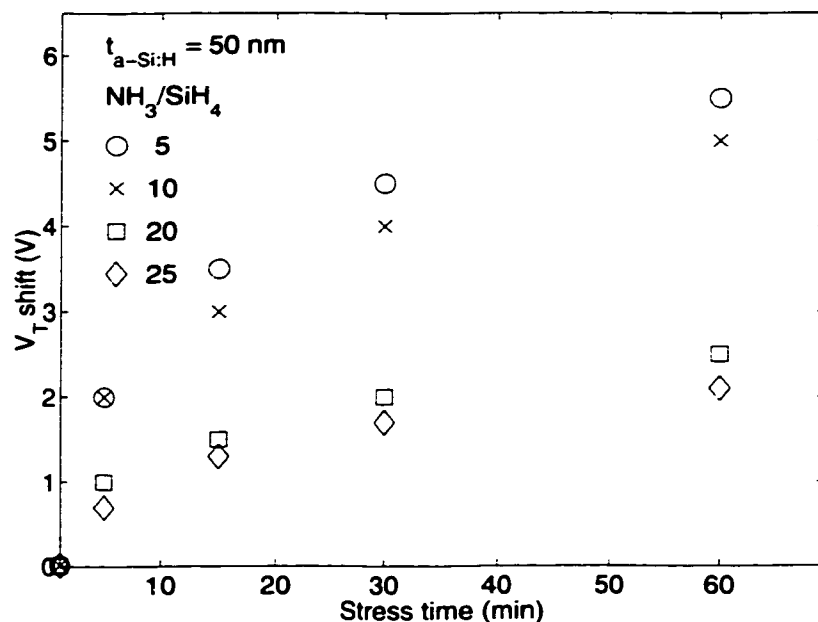
Figure 5.10: The shift in threshold voltage for different NH$_3$/SiH$_4$ gas ratios. V_{GS} = 25 V applied at the bottom gate.

Different bias schemes are also performed to study the shift in V_T. The bias voltage is applied either to the bottom or top gates. The results of V_T shift are

shown in Figs. 5.10 and 5.11, respectively. In both cases, we see that the shift in V_T is significant with respect to stress duration as well as nitride composition. The shift is far less pronounced in films deposited at high gas ratios. Here, the films are nitrogen-rich with less defect states in the bulk as well as at the a-Si:H/a-SiN$_x$:H interface. As a result, the degree of carrier injection is low.
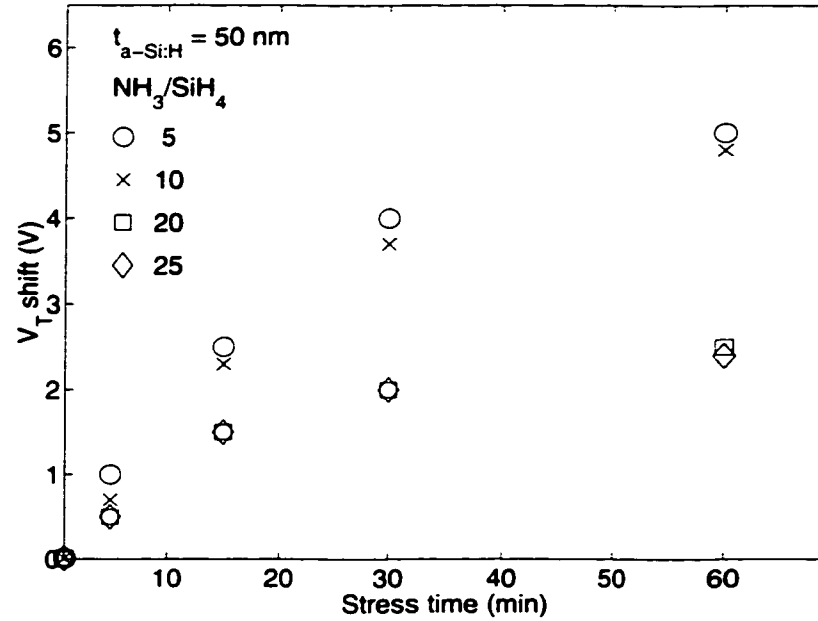
Figure 5.11: The shift in threshold voltage for different NH_3/SiH_4 gas ratios. V_{GS} = 25 V applied at the top gate.

5.6.4 Leakage Current

The transfer characteristics, including leakage current for the different bias stress durations, are shown in Figs. 5.12 and 5.13 for films deposited at high and low gas ratios, respectively. In both cases, we observe the usual increase in (reverse) leakage current with increasing (negative) gate voltage. In these measurements,
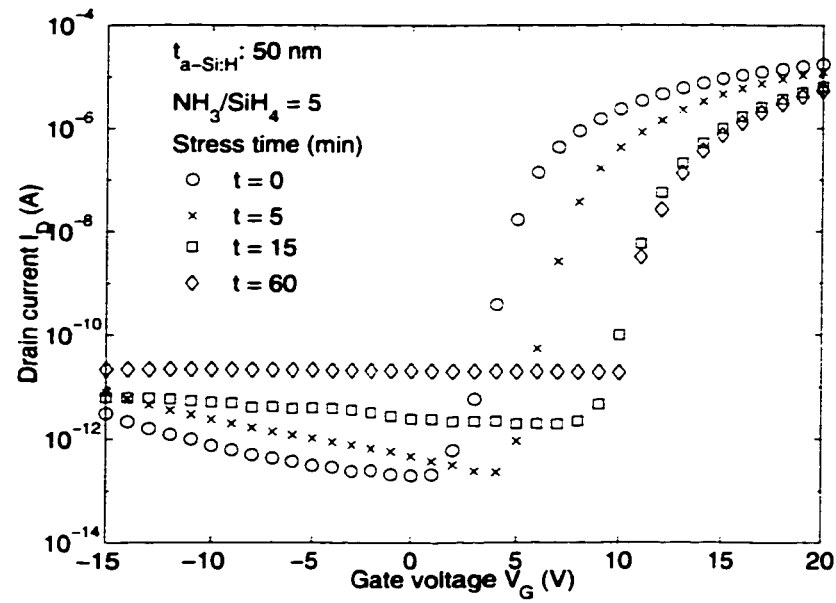
Figure 5.12: Leakage current change with gas ratio NH_3/SiH_4 at 5.
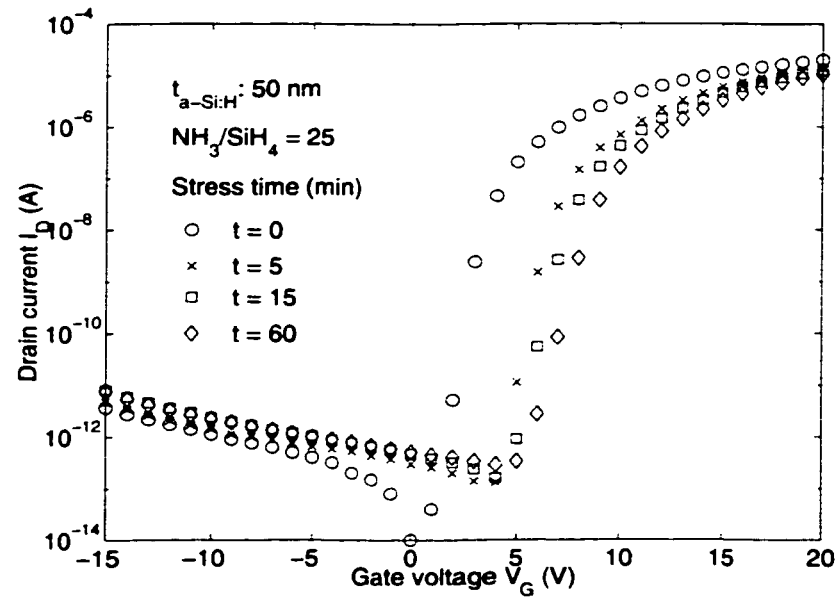
Figure 5.13: Leakage current change with gas ratio NH_3/SiH_4 at 25.

the drain-source voltage V_{DS} was 10 V. There is a pronounced variation in leakage current with bias stress in the case of nitride films deposited at small gas ratios. In fact, at elevated stress times, the leakage current becomes virtually independent of the gate voltage. We believe this may be attributed to hole trapping in the top nitride layer, which results in a pinning of the Fermi level [91] at the a-Si:H/a-SiN$_x$:H interface. Thus we have the formation of an electron back channel at the interface, giving rise to a steady leakage current that is V_G - independent. From the above observations we conjecture that the shift in V_T contributed by the top nitride is due to hole trapping. As seen from FTIR and RBS shown in Section 5.5, the films deposited at low gas ratios are Si-rich. In these films, there is a high density of Si dangling bonds, which acts as hole trapping centers. The density of Si dangling bonds decreases with increasing gas ratios, thus reducing the degree of hole trapping and hence the shift in V_T.

5.7 Summary

This chapter presented a systematic study of the behavior of the threshold voltage and leakage current with composition variation in the top (passivation) nitride in inverted staggered a-Si:H TFTs. Both the V_T shift and leakage current were influenced by the nitride composition. The composition was varied by using different NH_3/SiH_4 gas ratios during deposition, to yield either a silicon- or nitrogen- rich nitride at low or high gas ratios, respectively. With nitrogen- rich nitride films, the shift in V_T as well as leakage current was observed to be minimal.

Chapter 6

Pixel Integration

6.1 Structure Design

The pixel refers to the photodiode integrated with the TFT switch. Two pixel structures currently used are (1) the conventional structure (where TFT is adjacent to the photodiode) and (2) the stacked structure (where the photodiode is stacked on the top of TFT) (see Fig. 6.1). A comparison of two structures is shown in Table 6.1. In the stacked structure, an intermediate layer is required between the photodiode and TFT to reduce the leakage current and mechanical stress. In this work, we adopted the conventional structure, which quite comfortably meets the requirements of a large number of optical applications.

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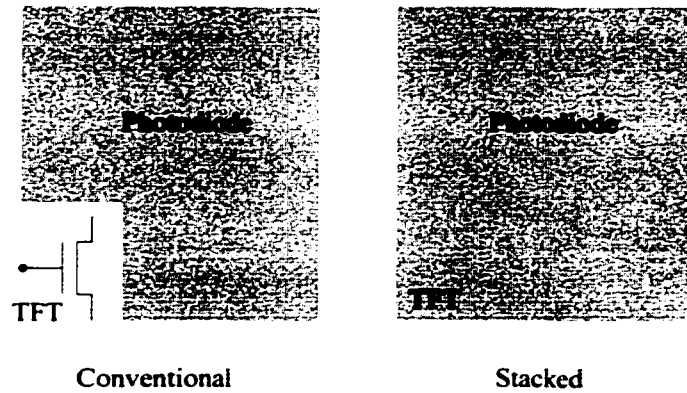
Figure 6.1: Top view of pixel structures (conventional and stacked).

Table 6.1: Differences between conventional and stacked structures.

	Conventional	Stacked
Fill factor	0.3 - 0.7	> 0.9
Intermediate layer between photodiode and TFT	Not required	Required
No. of total masks	11	11

6.2 Pixel Integration

6.2.1 Process Consideration

In the pixel integration, it is necessary to etch the very thick a-Si:H active layer of the photodiode. If the fabrication starts with the TFT, it is crucial to protect it during the etching of thick a-Si:H layer. For the protection layer, an optimized thickness must be considered for small built-in stress and to provide efficient etch protection. In our process, a 200 nm thick layer is necessary to achieve this purpose.

On the other hand. if fabrication starts with the photodiode. the considerations previously discussed are not of importance. However. gate insulator a-SiN$_x$:H cannot be deposited at 320 °C. All the PECVD processes must be undertaken less than 260 °C. Fig. 6.2 illustrates our FTIR measurements for a-SiN$_x$:H deposited at 320 °C and 260 °C with a gas ratio (NH$_3$/SiH$_4$) of 20. We observed no obvious difference between these two a-SiN$_x$:H films. Therefore. the TFT with the gate insulator a-SiN$_x$:H deposited at 260 °C in our process can also achieve comparable device characteristics as that deposited at 320 °C.
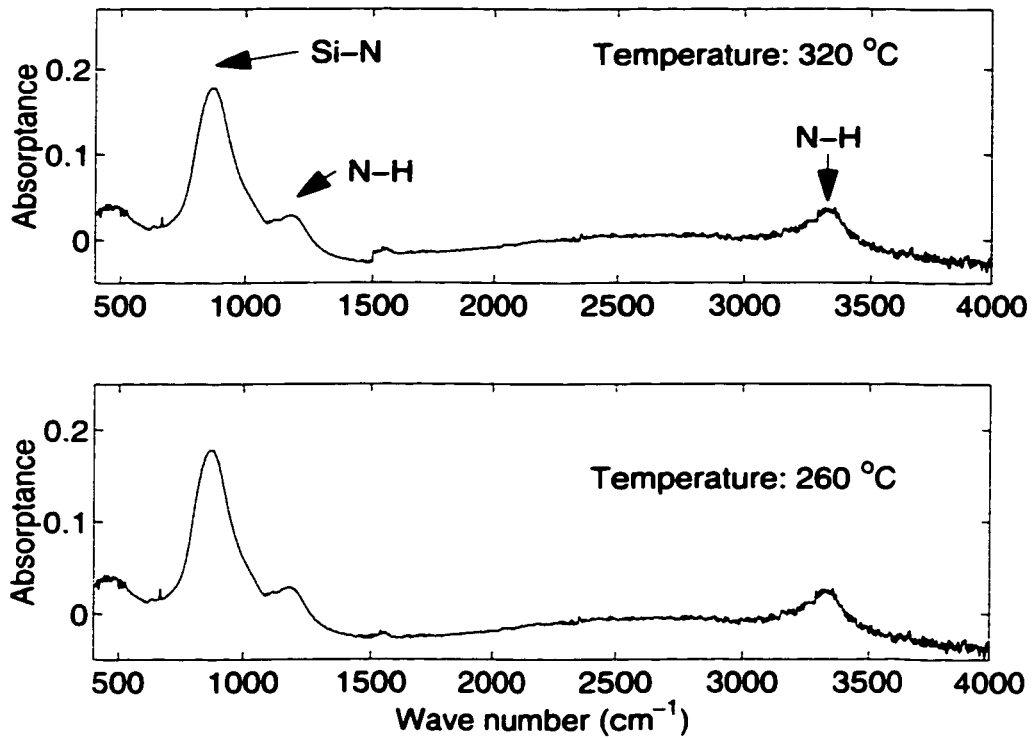
Figure 6.2: FTIR measurement for a-SiN$_x$:H deposited 320 °C and 260 °C with gas ratio of 20.

6.2.2   Fabrication Sequence

Integration of the photodiode and TFT is the ultimate goal of this work. As mentioned in Section 6.1, there are two different pixel structures: conventional and stacked. The fabrication sequences for both of them are shown in Figs. 6.3 and 6.4. respectively. The top views of the fabricated pixels are shown in Figs. 6.5 and 6.6. This research addresses preliminary work on the integration of the conventional structure, an in-depth study of stacked structures is currently under development in our group [92].

In pixel integration, one important process issue is ITO etching. The etching of polycrystalline ITO needs very strong acid solutions (see Table 4.3). In our fabrication, ITO deposition is the final process step. The protection of all the other metal films is crucial during the patterning of the ITO film. Fig. 6.7 shows the ITO pattern after samples were dipped for 20 seconds: only partly etching is observed. If overetched, the etchant may go through any imperfections to attack the bottom electrode metal. One example is given in Fig. 6.8. Here, the gate of the middle TFT was attacked by the etch solution. Thus, to minimize such occurrences, the thickness of a-SiN$_x$:H protection layer is required to be more than 200 nm.

Photodiode   TFT   VIA

1. TFT fabrication and protection

a-SiN$_x$:H
n$^+$μC-Si:H
i a-Si:H
a-SiN$_x$:H

Cr

Glass substrate

2. Photodiode fabrication

a-SiN$_x$:H

a-Si:H

n$^+$a-Si:H

Glass substrate

3. Opening of TFT source/drain contact and PD bottom electrode, Al sputtering and passivation

a-SiN$_x$:H
Al

Glass substrate

4. Opening of PD top electrode contact, ITO sputtering, opening of all electrodes contact, wire bonding

ITO to Al   Bonding   Bonding   Bonding

Glass substrate

Figure 6.3: Process sequence for a conventional structure pixel.

TFT and photodiode   TFT gate via   TFT source via

1. TFT fabrication, passivation, contact opening between TFT and photodiode

a-SiN$_x$:H
n$^+$µc-Si:H
i a-Si:H
a-SiN$_x$:H

Glass substrate   Cr

2. Photodiode fabrication, Al sputtering, and passivation

a-SiN$_x$:H
i a-Si:H
n$^-$a-Si:H
Al

Glass substrate

3. ITO sputtering, and top photodiode electrode formation,
Opening of all the electrode contacts, wire bonding

ITO to Al
Bonding (to gate line)
Bonding (to data line)

Glass substrate

Figure 6.4: Process sequence for a stacked structure pixel.

Photodiode
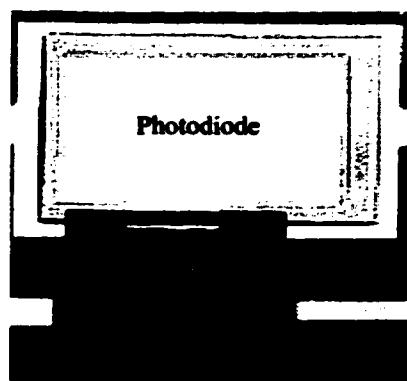
Figure 6.5: Top view of a conventional structure pixel.
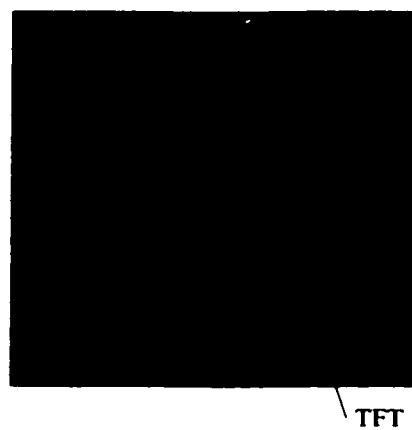
Figure 6.6: Top view of a stacked structure pixel.
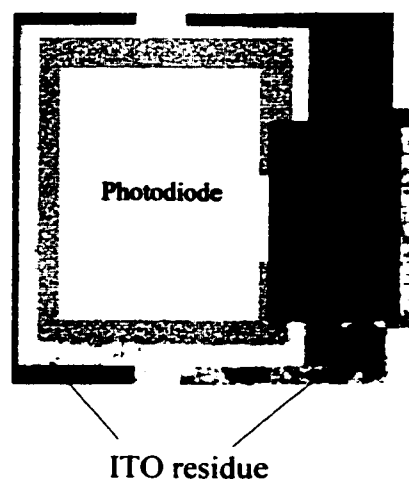
Figure 6.7: Nonuniformity of ITO etching.

Unattacked gate   Attacked gate
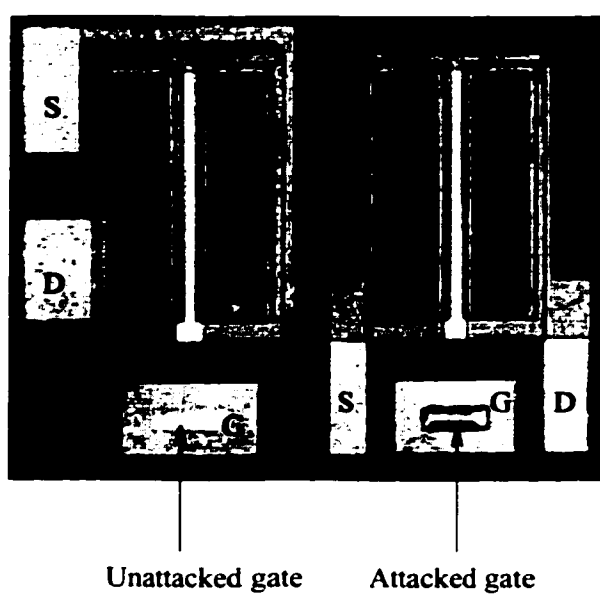
Figure 6.8: Possible attacks to metals by ITO etch solution.

Chapter 7

Conclusions

A process for polycrystalline ITO films deposited at low temperature has been developed for high performance Schottky photodiode image sensor. The degree of crystallinity, transmittance, and resistivity of the ITO films have been characterized in tems of sample position, rf sputtering power, annealing temperature, and sputtering pressure.

The profiles of oxygen and indium at the interface between the ITO and the a-Si:H are measured by secondary ion mass spectroscopy (SIMS) for different structures (ITO/a-Si:H and a-Si:H/ITO) and deposition parameters, such as rf power and annealing temperature. In terms of interface integrity, the ITO on top of the a-Si:H features a better interface compared with the a-Si:H on top of the ITO. It is found that annealing at high temperatures (for example, at 260 °C) results in high oxygen diffusion while indium distribution does not change significantly. When annealed at low temperature (150 °C), both oxygen and indium profiles are close to that of as-deposited films at room temperature, indicating that low temperature (150 °C) annealing is able to remove the interface damage caused by the plasma

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while not affecting the distributions of oxygen and indium at the interface.

A photodiode based on the ITO/a-Si:H Schottky structure has been developed. The ITO film was optimized and the associated photodiode features low leakage current (7×10^{-10} A/cm^2 at -2 V) and high stability (with a shift of less than 9% of the initial value when biased at -2 V). When co-integrated with a Gd_2O_2S:Tb phosphor film. X-ray detection was demonstrated. The corresponding X-ray sensitivity is comparable to that of the direct detection Mo/a-Si:H sensor.

The effect of annealing is studied and it is observed that high temperature (260 °C) annealing increases the leakage current of the photodiode while low temperature (150 °C) annealing yields superior device characteristics. SIMS measurements for profiles of oxygen and indium indicate that it is the oxygen diffusion. rather than indium diffusion. that contributes to the increase in the leakage current when processed at high temperatures (for example. 260 °C.)

The photosensitivity is optimized by the change of thickness of a-Si:H active layer and the geometry of the collection electrode. It is found that the device with the a-Si:H of 1 μm thick has the maximum photosensitivity as a consequence of the increased optical absorption in the a-Si:H layer. The increase in photosensitivity with the grided collection electrode can be attributed to the enhanced collection efficiency.

Our work on the a-Si:H TFT shows that both the shift in threshold voltage and change in leakage current are influenced by the compositions of the top (passivation) nitride layer. Here. the nitride composition is varied by using different NH_3/SiH_4 gas ratios (5. 10. 20. 25) during deposition. to yield either a silicon- or nitrogen-rich silicon nitride at low (5) or high (20. 25) gas ratios. respectively. It is observed that both V_T shift and leakage current are minimal in the case of nitrogen- rich

films.

A fabrication process for a pixel based on the conventional structure has been developed for the large area application. An alternative processing sequence which fabricates the photodiode first and the TFT subsequently has also been accomplished based on the same deposition temperature (260 °C) for a-Si:H and a-SiN$_x$:H. The process issues related to the fabrication have been addressed. These include ITO etching compatibility, a-SiN$_x$:H/a-Si:H etching compatibility, and a-SiN$_x$:H etching protection.

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