Mitigation of Memory Effects in High Power Microwave Amplifiers

by

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Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions as accepted by my examiners.

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Abstract

This thesis expounds on the application of Doherty Power Amplifiers (DPA) along with baseband Digital PreDistortion (DPD) techniques to tackle the antagonistic demands of high power efficiency and linearity imposed by modern communications.

Memoryless modeling is firstly introduced and its limitations when dealing with PAs driven with realistic devices. Therefore, electrical memory effects are explored in greater detail and a mathematical model showing the relation between the various harmonic components in the output and how they can re-mix back into the fundamental band is developed. The importance of the output bias network in the reduction of memory effects is highlighted. A memory polynomial (MP) based DPD is shown to be a good solution for the linearization of wideband DPA which exhibit strong memory effects. To further improve this solution, the complexity of the MP-DPD is reduced. For that, the even-order terms in the MP branches were first removed. Then, the PA memory effects theory was used to further reduce the number of coefficients of the MP-DPD by decreasing the nonlinearity orders in the different branches individually. These two steps allowed for a reduction of the number of coefficients to almost one-third and the conditioning number by three orders of magnitude while maintaining the same linearization capability. This substantially alleviates the requirements on the digital signal processors and the time needed to construct and implement the MP-DPD in real environment. Experimental validation carried out using a 400 Watt DPA, driven with 4-Carrier WCDMA signal, showed excellent linearization capability by achieving an ACPR of better than 50 dBc with a power efficiency of better than 42.4%. Despite this, the depth of the memory effects in the DPA was still significant.

While an effort was made to reduce further the memory effects, the discrepancy between the simulated behavior of the DPA and that observed in simulation was significant. In an attempt to rule out the DPA structure as the cause of the discrepancy between the measured results and the behavior predicted in simulation, a single branch class AB PA was designed using the transistor model. The PA behavior was well predicted when driven with a Continuous Wave (CW) signal, however the simulated and measured behavior differed greatly when the PA was driven by a two tone signal. This rendered the desired reduction of the memory effects impossible at the design stage.

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Introduction

RF Power Amplifiers (PA) are essential components in wireless communications systems. Designed to operate at a multitude of frequency bands, at various power levels using a variety of architectures, their role is generally the same: amplify and send a signal to one or multiple antennas to be transmitted. Two fundamental and antagonistic performance criteria are used to benchmark all PAs.

Linearity has risen in importance in the last decade. In previous generations of RF devices Frequency Modulated (FM) and Gaussian Minimum Shift Keying (GMSK) signals were used to avoid linearity constraints, as they are characterized by a constant envelope and therefore did not require linear amplification. However, driven by consumer demand for more real-time, high data density media content, there is an increasing demand for spectral efficiency in wireless technology. This demand has led to the use of increasingly complex modulation schemes (Quadrature Amplitude Modulation (QAM), Orthogonal Frequency Division Multiplexing (OFDM)) and access technologies (Wideband Code Division Multiple Access (WCDMA), Worldwide Interoperability for Microwave Access (WiMAX)), which use both phase and amplitude modulation. These modulation schemes are characterized by high to Peak to Average Power Ratio (PAPR) signals while the access technologies are characterized by stringent linearity requirements. Hence, modern PAs need to be extremely linear over a large power range.

Competing with the demand for high linearity is the antagonistic demand for high power efficiency in modern transmitters. In mobile devices, greater power efficiency translates into longer lifetime. In base stations, higher power efficiency also reduces the size of the necessary cooling system, translating into significantly lower operating and deployment costs for service providers. Furthermore, satellite communications applications have very tight weight and energy budgets, so any way to reduce the energy consumption without increasing the mass of the transmitter is of critical importance.

Being the largest source of distortion and the most power hungry block in the transmitter chain, the power amplifier is at the centre of these conflicting antagonistic demands. To meet the linearity requirements set by the regulatory bodies over the large dynamic range necessary for high PAPR signals, service providers often use Pas biased in very linear classes of operation, such as class A and AB, and operate them in back-off. However, these classes of operation are

characterized by very poor efficiency in back-off. Conversely, more efficient classes of PAs are extremely non-linear and thus not a suitable solution. Hence, recent research efforts have focused on designing linear and efficient PAs.

The Doherty PA (DPA) architecture is one of the most promising solutions that has started to be deployed in the field. This dual branch architecture uses active load modulation to optimize the load impedance seen by the transistor, which greatly improves the efficiency of the PA at back-off.

Linearization techniques have shown various degrees of improvement in the linearity performance when applied to class AB PAs. However, techniques based on feedback have limited linearization bandwidth capability and are thus unsuitable for wideband base station applications. Baseband Digital PreDistortion (DPD) is an ideal complement to the DPA as it allows for high linearization capability and bandwidth while conserving the high power efficiency of the DPA. Unfortunately DPD the advantages of using DPD come at the cost of high complexity.

The primary focus of this thesis is to examine ways of reducing the complexity of a DPD required to linearize a high power, wideband, commercial DPA. This will be done by finding new ways to simplify the DPD scheme itself as well as trying to improve the design of the DPA to reduce the requirements for the DPD.

The thesis is divided into four chapters. The first chapter will present a quick review on PA classes, the DPA architecture and the most common metrics used to measure PA linearity. Different linearization techniques are also reviewed and compared in this section

The second chapter explores memoryless modeling and introduces the concept of memory effects. A mathematical model showing how various output harmonics re-mix back into the fundamental band is developed.

In the third chapter, a brief outline of various Volterra based modeling schemes is given. A Memory Polynomial (MP) based DPD is developed and its complexity is reduced by eliminating even-order terms in the MP branches and reducing the order of the subsequent branches. An effort is made to further reduce the complexity of the DPA, however a significant discrepancy between the measured and simulated behavior of the transistor is observed.

The fourth chapter deals with a single branch class AB PA designed in order to eliminate the active load modulation of the DPA architecture as the source of the discrepancy between

predicted and measured transistor behavior. The single branch PA behavior continues to deviate significantly from the predicted model behavior when stimulated with a two-tone input. This leads to the conclusion that the transistor model is the source of the discrepancy, rendering further mitigation of the memory effects impossible.

Chapter 1: Background

1.1 Single Branch Power Amplifiers

Several different classes of PA exist, each having its own tradeoff between linearity and power efficiency depending on how the transistor used in the PA is biased. This tradeoff is illustrated in Figures 1.1 and 1.2. It can be seen that while moving from a linear class of operation (Class A) to more nonlinear classes of operation (Class AB and Class B) by reducing the conduction angle does offer interesting improvements in efficiency, this improvement comes at the cost of increased harmonic components at the output , and hence stronger nonlinearity [1].

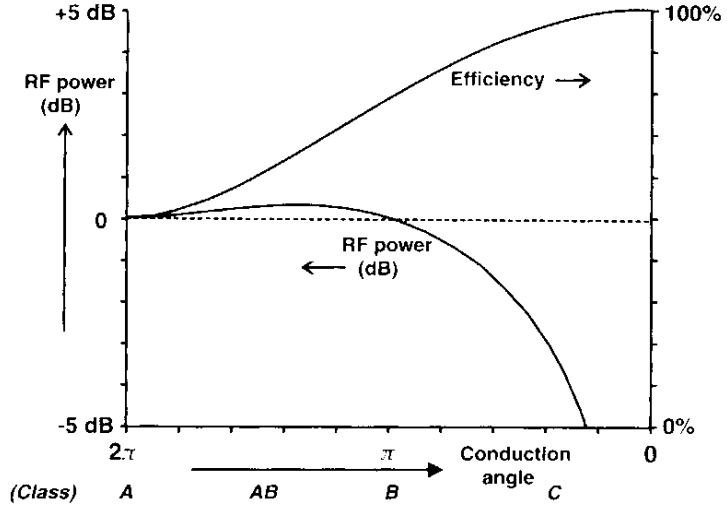


Figure 1.1: PA Efficiency as a Function of the PA's Class of Operation [1]

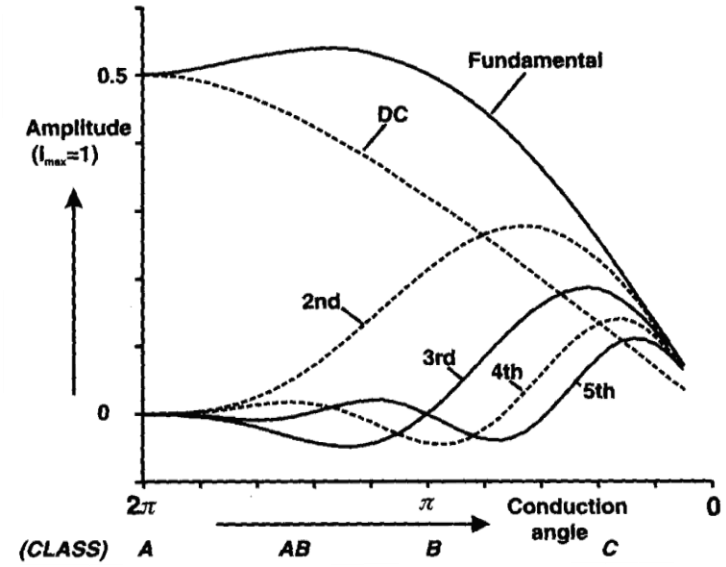


Figure 1.2: PA Nonlinearity as a Function of the PA's Class of Operation [1]

To ensure the linear behavior over a large dynamic range that is required by the high PAPR signals prevalent in modern communications, most commonly deployed PA architectures are biased in the quasi linear class AB and operated in deep back-off. While this class of operation does offer a good efficiency at peak output power, its efficiency decreases quickly in back-off, as shown by the linear region in Figure 1.3. One can see that the power efficiency of this PA drops from over 50% to around 20% when it is backed off 8 dB from peak output power. Furthermore, the region at which the PA achieves peak efficiency cannot be used due to the nonlinearity of the PA as shown by its gain compression. Hence, operating the PA in this manner leads to extremely poor average power efficiency (10 to 15%) when driven with modulated signals. Furthermore, operating the PA in class B or C, which offers significant efficiency improvement is not feasible due to the poor linearity of these classes of operation.

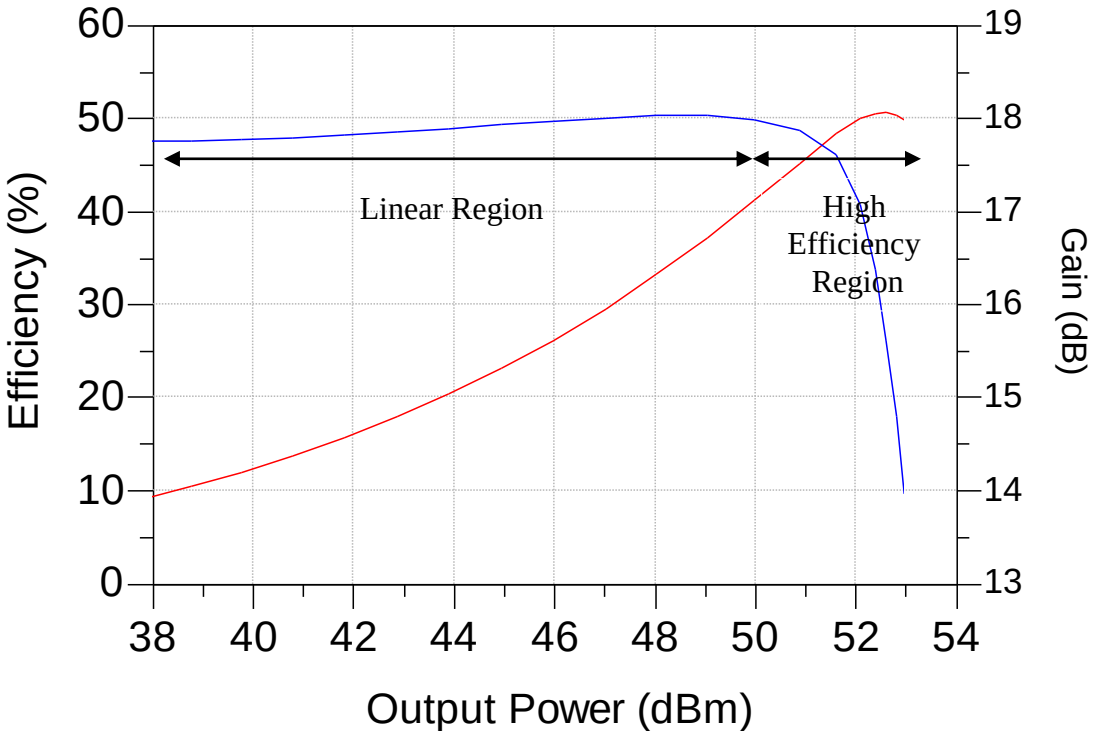


Figure1.3: Class AB Power Efficiency and Gain as a Function of Output Power

Thus, the efficiency of the PA needs to be improved in the back off without significantly compromising its linearity. Furthermore, the use of linearization techniques would allow the use of the "high efficiency region" highlighted in Figure 1.3. Currently, highly efficient PA architectures such as those based on the load modulation technique are used to improve the PA's

inherent power efficiency. These techniques dynamically vary the load impedance seen by the PA as a function of its input power so as to present the optimal load impedance to maximize the PAs efficiency. In the literature, the most commonly used load modulation based amplifiers are Doherty amplifiers [2]–[8] and LINC (LInear amplification using Nonlinear Components) architectures [9]–[11]. Among these two techniques, Doherty amplifiers are currently being considered for handset devices whereas the LINC architecture is still in the R&D stage. In fact, Doherty amplifiers achieve relatively high power efficiency with a moderate linearity and the use of linearization techniques makes it possible to meet the regulatory linearity requirements.

1.2 Doherty Power Amplifier

The original Doherty PA (or DPA) was proposed in 1936 by William H. Doherty [2]. The original design dealt with very high power tube amplifiers for an Amplitude Modulation applications. While modern systems have output powers that are several orders of magnitude less than the original design, the efficiency enhancement that this technique offers remains extremely relevant.

The Doherty PA is an architecture consisting of two parallel amplifiers, a main and peaking amplifier as shown in Figure 1.4, where Z_o is the characteristic impedance of the system and the load impedance.

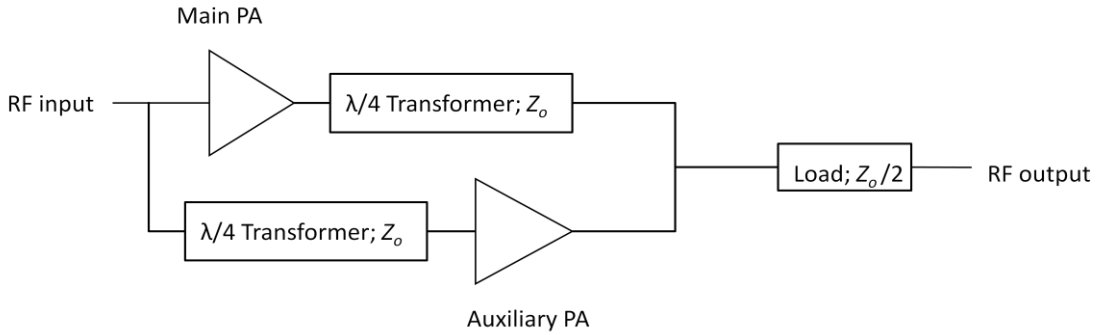


Figure 1.4: Typical Doherty Power Amplifier Topology

The main amplifier is usually biased in class AB or class B, while the peaking amplifier is biased in class C. The output load is connected to the main amplifier through a quarter wave transformer and directly into the peaking amplifier. The peaking amplifier is biased so as to turn on at half of the maximum input voltage. A simplified analysis can be performed by representing both PAs as current sources as shown in Figure 1.5.

The DPA has two operating modes. When the input power is below half the maximum input voltage, only the main PA is turned on. Since the auxiliary PA is biased in Class C, it consumes no Direct Current (DC) power when it is in cut-off. Through the quarter wave transformer, the load seen by the main amplifier (Z_{main}) is twice the load impedance. This increase in the impedance seen by the main amplifier allows it to reach saturation at half the maximum input voltage, achieving its peak efficiency much quicker.

At higher power levels, the peaking amplifier is turned on and delivers power to the load in phase with the main PA. This serves to actively modulate the load seen by the main PA, increasing the impedance of the load. However, when seen through the quarter wave transformer, the impedance seen by the main PA is gradually reduced as the input drive increases to keep the main PA in saturation. This active load modulation allows the DPA to maintain high efficiency over a 6 dB dynamic range as seen in Figure 1.6.

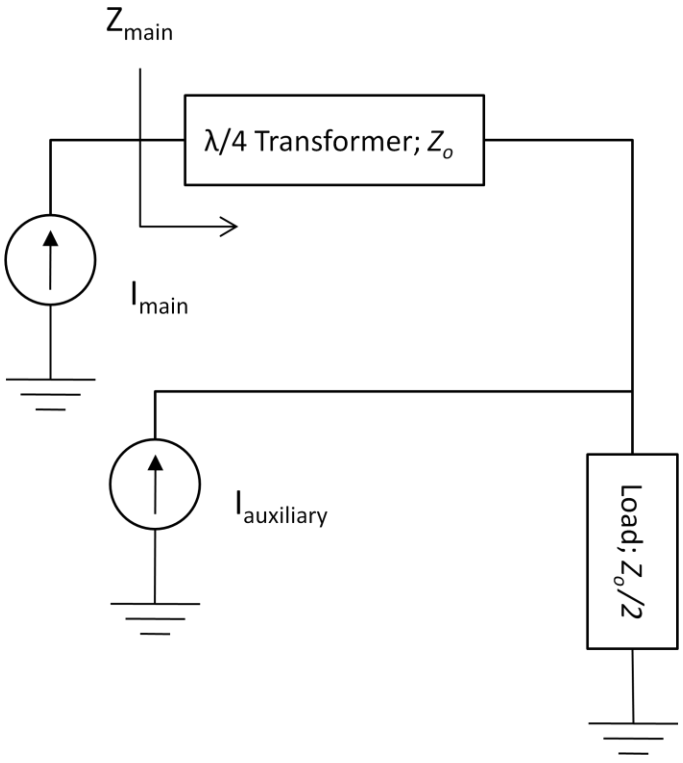


Figure 1.5: Simplified Doherty Power Amplifier Model

A more detailed mathematical analysis of the Doherty design can be found in a variety of references [1]-[3], [12].

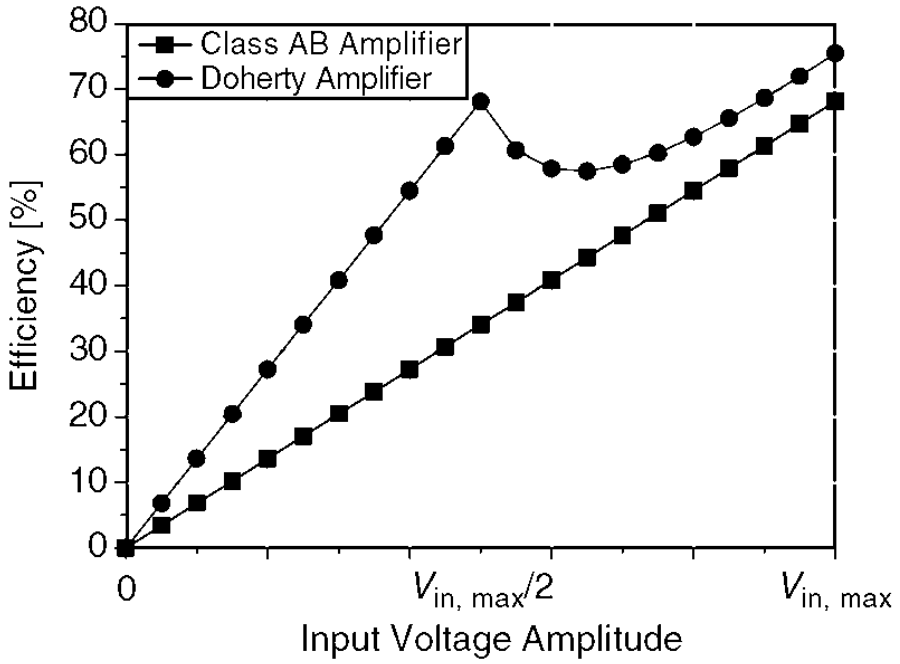


Figure 1.6: Doherty PA Efficiency Compared to a Class AB PA efficiency [12].

1.3 Metrics of Nonlinear Distortion

One of the drawbacks of the DPA, relative to single branch implementations, is further degradation in transmitter linearity. This increase in nonlinear behavior can be observed in a variety of ways, however, the most common tests to characterize nonlinear behavior are the one and two tone test. While the simplicity of these two tests is ideal for debugging PA design, ultimately the PA must be tested under realistic drive conditions using a modulated signal.

1.3.1 Single Tone Testing

The one tone test consists of stimulating the Device Under Test (DUT) with a single sinusoidal tone. This test uses an extremely simple input signal and hence is an extremely easy test to perform and interpret. The most important metrics that are extracted from this test are the AM-AM and AM-PM response of the DUT. The AM-AM characterization describes the relation between the output amplitude of the fundamental frequency with the amplitude of the input signal. Hence, it describes the gain compression or expansion of the DUT as a function of the input drive level. This allows for the evaluation of the 1 dB compression point (P_{1dB}), which is defined as the point at which the output is compressed by 1 dB as compared to an ideal linear

output. The AM-PM response of the DUT describes its phase deviation as a function of the input drive level. Typical AM-AM and AM-PM curves are shown in Figures 1.7 and 1.8.

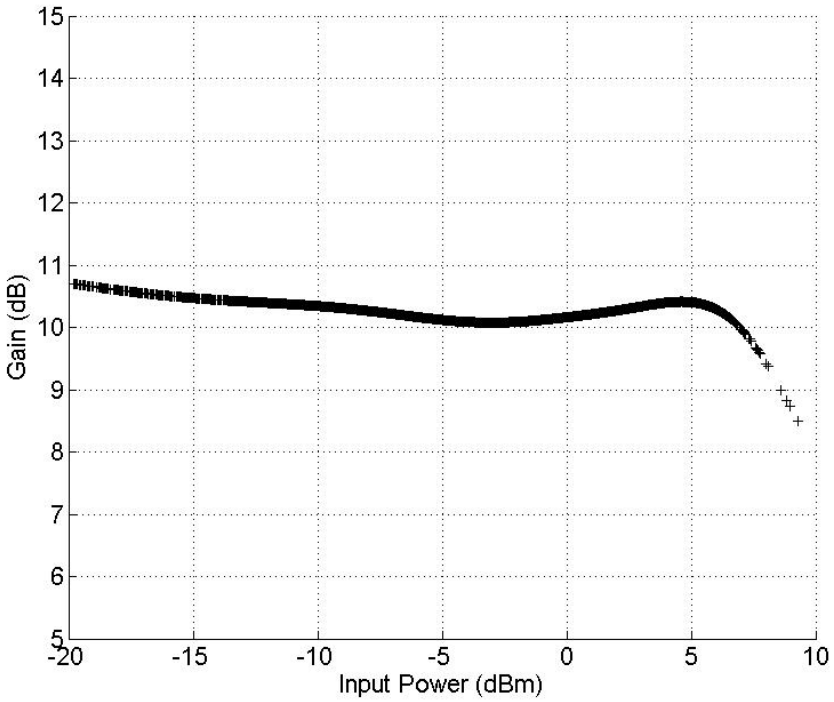


Figure 1.7: Typical AM-AM Characteristics of a Power Amplifier

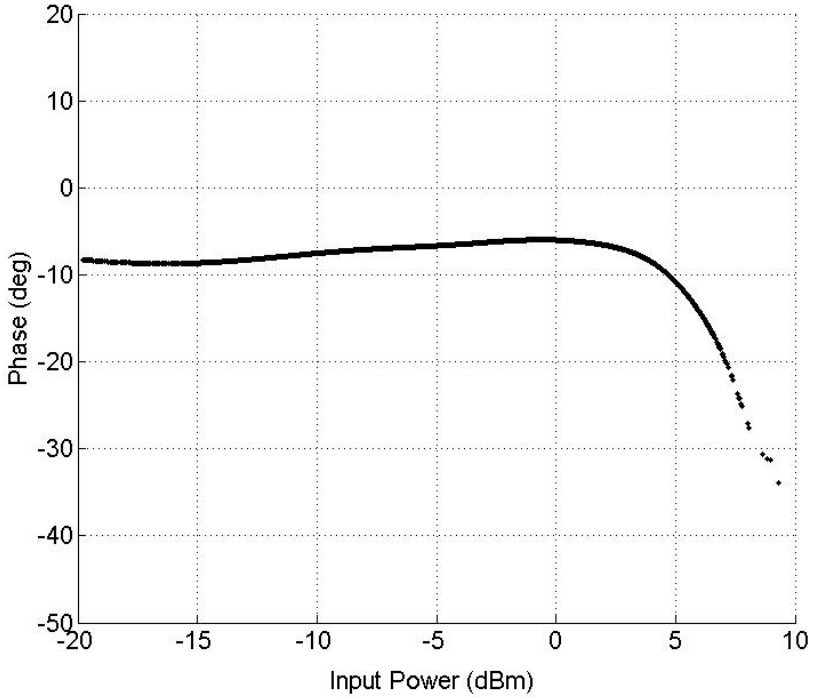


Figure 1.8: Typical AM-PM Characteristics of a Power Amplifier

1.3.2 Two-Tone Test

The two-tone is a better representation of true telecommunications signal excitation. The DUT is stimulated with two sinusoids with frequencies f_1 and f_2. This test allows for a better characterization of the DUT as the test signal used begins to resemble a realistic test signal, however, the results are simple enough to allow great insight into the source of the nonlinear behavior.

The spacing between the two tones, $\Delta f = f_2 - f_1$, is analogous to the bandwidth of a modulated signal used in modern communication systems. This test enables the characterization of generated harmonics, specifically the mixing components close to the fundamental. These mixing components are the dominant sources of nonlinear interference in bandpass systems as they are much harder to filter out. These mixing products are classified as third and fifth order intermodulation products or IMD3 and IMD5 respectively. The IMD3 products occur at $2f_1 - f_2$ and $2f_2 - f_1$ while the IMD5 products will occur at $3f_1 - 2f_2$ and $3f_2 - 2f_1$, as shown in Figure 1.9.

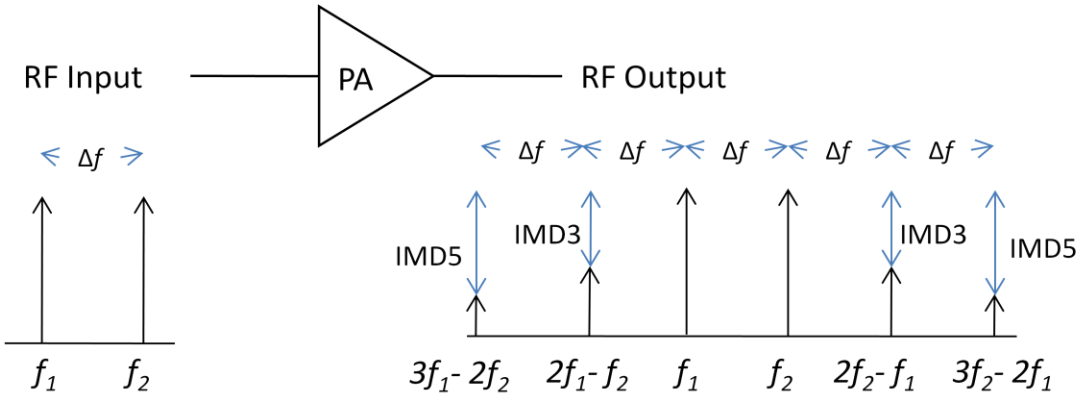


Figure 1.9: Input and Output Spectrum of a Typical PA

The IMD products are usually expressed as the power ratio of these mixing products to that of the fundamental tones. This ratio provides a good first guess to see if the DUT will meet the spectral mask requirements of the telecommunications regulatory body. These requirements usually specify the Adjacent Channel Power Ratio (ACPR) for several frequency bands around the transmit frequency. This metric is explained in further detail in the following section.

1.3.3 Modulated Signal Testing

The ACPR is a metric that can only be used when the DUT is being driven with a modulated input signal and is extremely useful for understanding the nonlinear behavior of the

DUT and how it can interfere with adjacent signals. ACPR is defined as the power ratio of the average power in the adjacent frequency channel to the average power in the transmit frequency channel, and is analogous to the IMD3 in the simple two tone case. Similarly, the alternate channel ratio, is defined as the power ratio of the power in a bandwidth two channels away from the main signal to the average power in the main signal bandwidth, and is analogous to IMD5. A typical ACPR measurement is shown in Figure 1.10

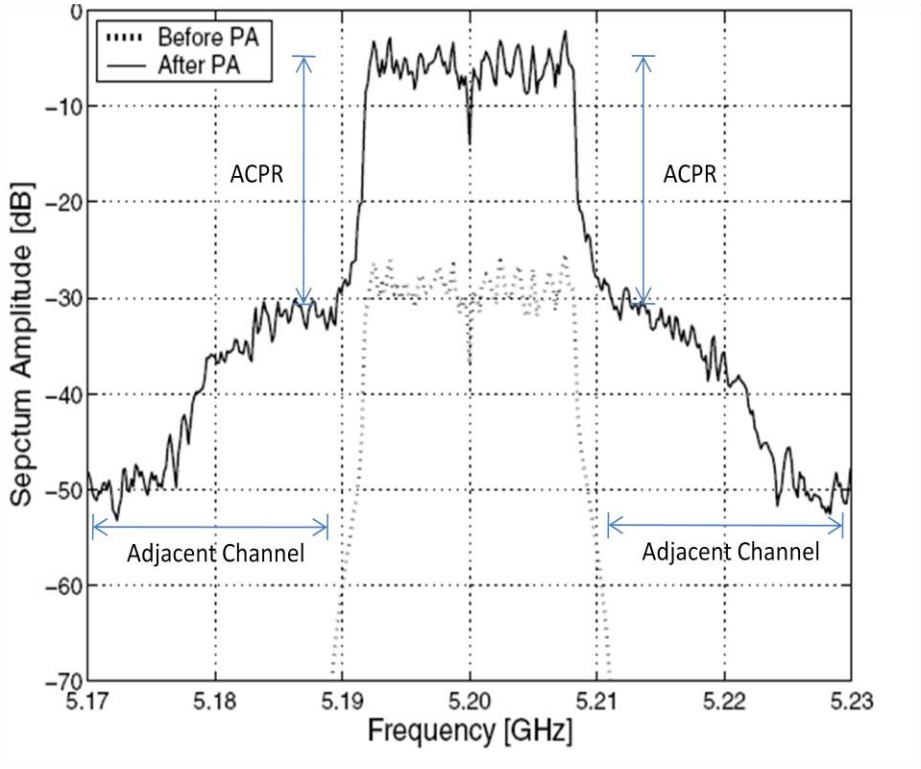


Figure1.10 Typical PA Input and Output Spectrum

However, the ACPR does not provide any information on how the transmitted signal is distorted within the transmission channel. For this, the Error Vector Magnitude (EVM) metric is needed. EVM is the most commonly used metric to measure how the transmitter distorts the desired output. An error vector is a vector in the I-Q plane between the ideal constellation point and the point received by the receiver as shown in Figure 1.11. The EVM is defined as the ratio of the power of the error vector to the Root Mean Square (RMS) power of the reference. It is described in dB as:

$$\mathrm{EVM(dB)} = 10\log_{10}\left(\frac{P_{error}}{P_{reference}}\right) \tag{1-1}$$

where P_{error} is the RMS power of the error vector, and $P_{reference}$ is the RMS power of ideal transmitted signal. EVM can be written as a percentage similarly:

$$\text{EVM}(\%) = \sqrt{\frac{P_{error}}{P_{reference}}} * 100\% \quad (1\text{-}2)$$

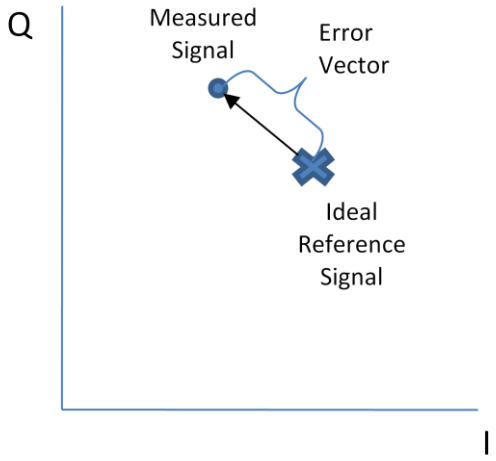


Figure 1.11: Graphical Representation of an Error Vector

1.4 Linearization techniques

Despite the interesting power efficiency gains that DPAs offer, this architecture usually presents a slight decrease in linearity from the previous generation of less efficient class AB amplifiers. To meet the stringent linearity requirement of modern communication standards, different linearization techniques are applied to Doherty PAs. Furthermore, linearization allows us to use the PA as its gain begins to compress allowing us to operate it in peak efficiency, despite the increase in nonlinearity in this region. This section describes the three most well established linearization techniques: feedback, feedforward, and predistortion.

1.4.1 Feedback Techniques

Feedback is a control technique that uses the current output of a system to adjust the future output of the system. Generally this is done by comparing the output signal to a desired output and generating an error signal. This error signal is then used to adjust the system parameters to generate the desired output signal. The signal path from the output of the system back to the system is referred to as the feedback loop [13].

A typical feedback loop is shown in Figure 1.12, where *x* and *z* are the time domain input and output of the system respectively. The general equation for this loop can be described as

$$\frac{Z(f)}{x(f)} = \frac{G(f)}{1+G(f)H(f)} \tag{1-3}$$

where *X(f)* and *Z(f)* are the Fourier transforms of the input and output of the system respectively

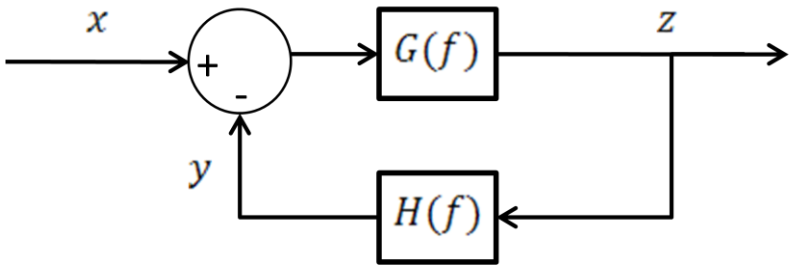


Figure 1.12: Typical Feedback Loop

This section presents 3 common applications of feedback to PA linearization.

1.4.1.1 Indirect Feedback

Feedback linearization can be distinguished into three commonly used techniques: indirect feedback, the Cartesian Loop, and Polar Loop. A basic indirect feedback is shown in Figure 1.13.

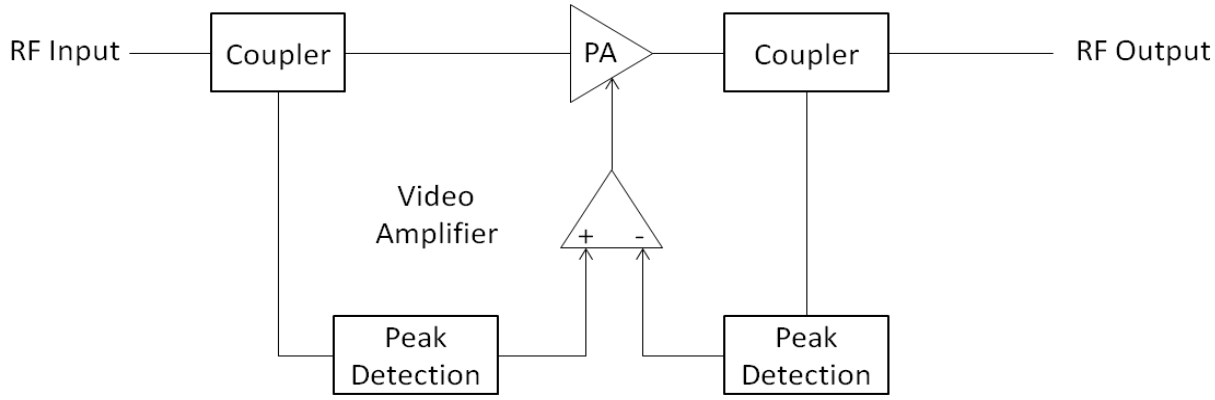


Figure 1.13: A Basic Indirect Feedback Linearization for an RFPA

A conventional RFPA has envelope detectors coupled to its input and output ports. These envelope detectors are used in conjunction with a differential video amplifier to form an error correction signal which is used to control the gain of the PA. This method only corrects for AM/AM distortion and cannot correct AM/PM effects.

1.4.1.2 Cartesian Loop Feedback System

Cartesian Correction is a transmitter rather than a PA linearization technique and requires the signal in its baseband form. The basic Cartesian Loop feedback system is shown in Figure 1.14. In this architecture, the I and Q signals are fed through differential correcting amplifiers. The output of these amplifiers is then fed into a vector modulator which feeds the RF PA. The PA output is sampled, downconverted back into separate I and Q signals. The sampled output I and Q signals are then compared with the original input baseband signals. The error signal is then re-injected at the input of the PA to yield linear output.

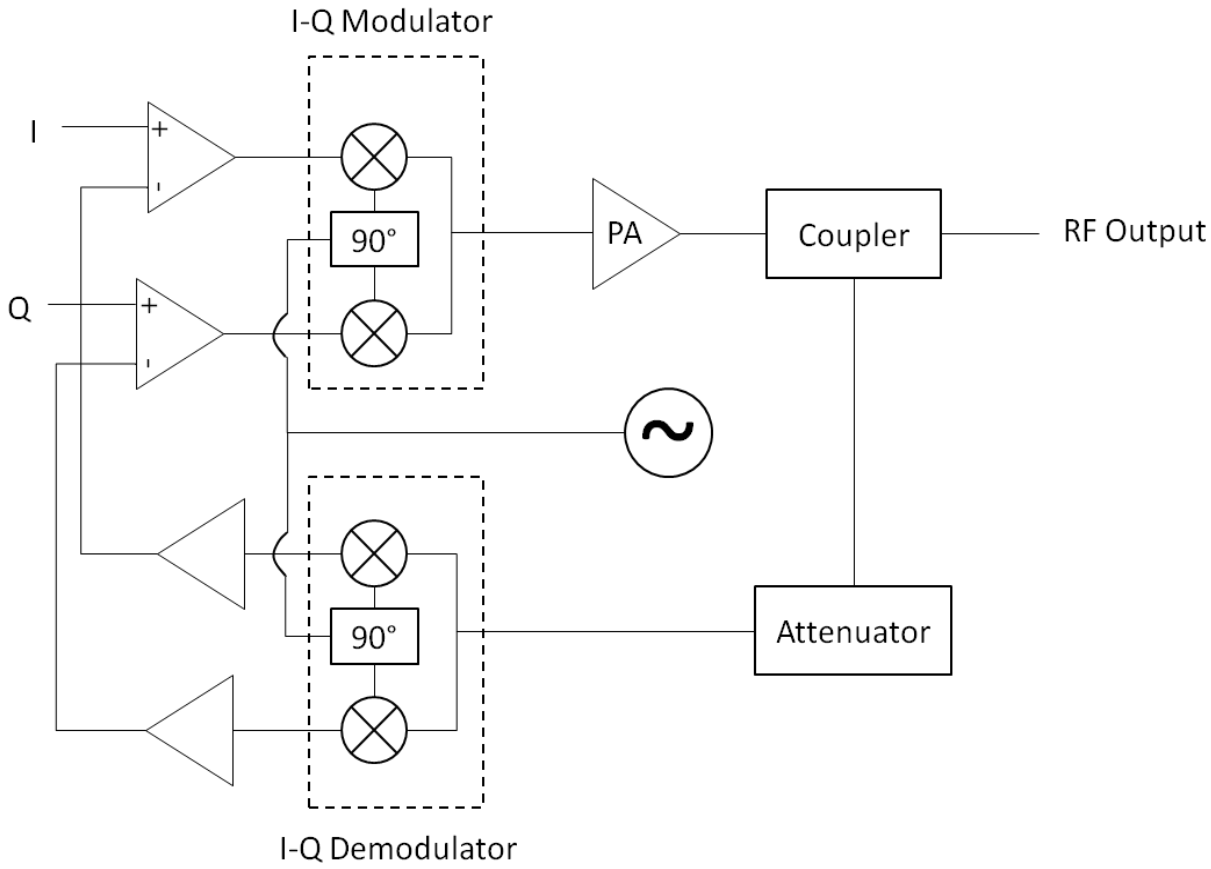


Figure1.14: A Cartesian Loop Feedback System

1.4.1.3 Polar Loop

The Polar Loop, as shown in Figure 1.15, would be better classified as a modulator rather than as a linearizer. The input to the modulator is a fully modulated IF signal. An RF PA in a supply modulated envelope restoration configuration creates the AM portion of the output RF signal, while a Voltage Controlled Oscillator (VCO) phase-locked to the IF input creates the PM

on the RF carrier. The PA output is sampled, down converted and then compared to the input to create an error signal. This error signal is used to adjust the gain of the envelope restoration RF PA.

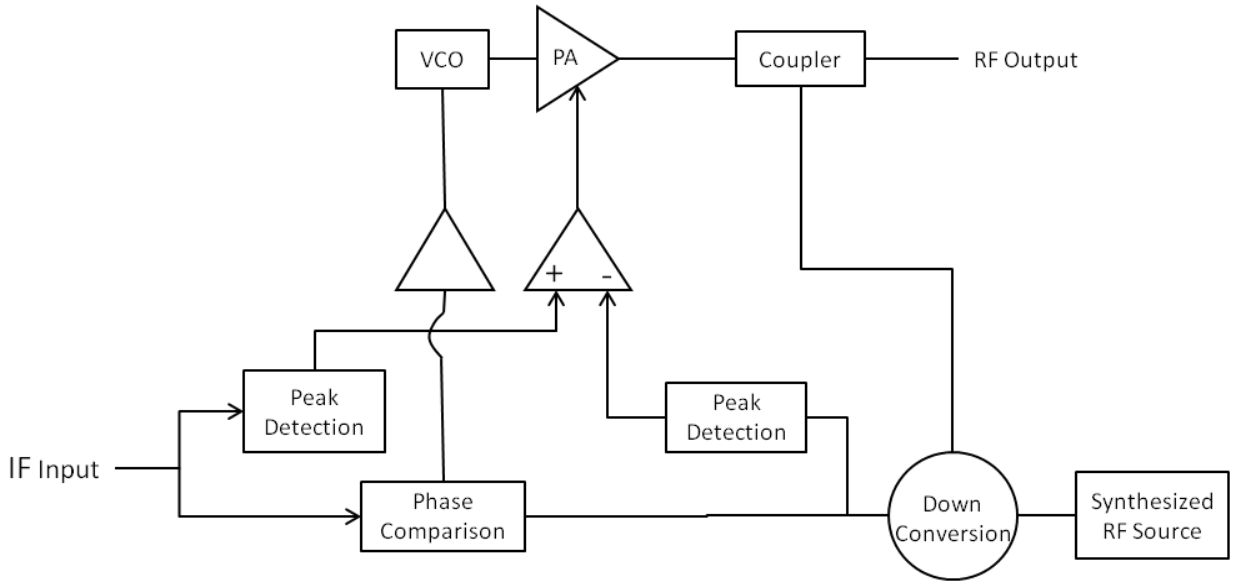


Figure 1.15: A Polar Loop Modulation System

1.4.1.4 Summary of Feedback Linearization

While all feedback techniques offer some improvement in the linearity of the RF output, they all face the bottleneck presented by BandWidth (BW) limitations in the feedback loop. Hence, they are more suitable to narrowband and single carrier applications.

1.4.2 Feedforward

Feedforward is a well established linearization technique that is used for wideband PA applications. The basic feedforward architecture, along with signal spectra at the input, main PA, error PA and output are shown in Figure 1.16. The feedforward architecture consists of two loops: a main signal loop and an error cancellation loop.

The input is divided into both signal paths. In the main path, the input is amplified by the main PA, generally a highly efficient but nonlinear PA that will generate harmonics and inter-modulation products. In the error cancellation path, the signal is delayed by an equal amount of time. The distortion generated by the main PA is extracted by subtracting the delayed version of the undistorted input from a sampled version of the main PA's output. If there is no error, then input to the error PA is zero. However, if there is any distortion, the error PA amplifies it back to the power level of the output. The output of the main PA is delayed to ensure that the delay in

the main path is equal to that in the error cancellation loop. The amplified distortion is then recombined with the PA output, cancelling out the inter-modulation products.

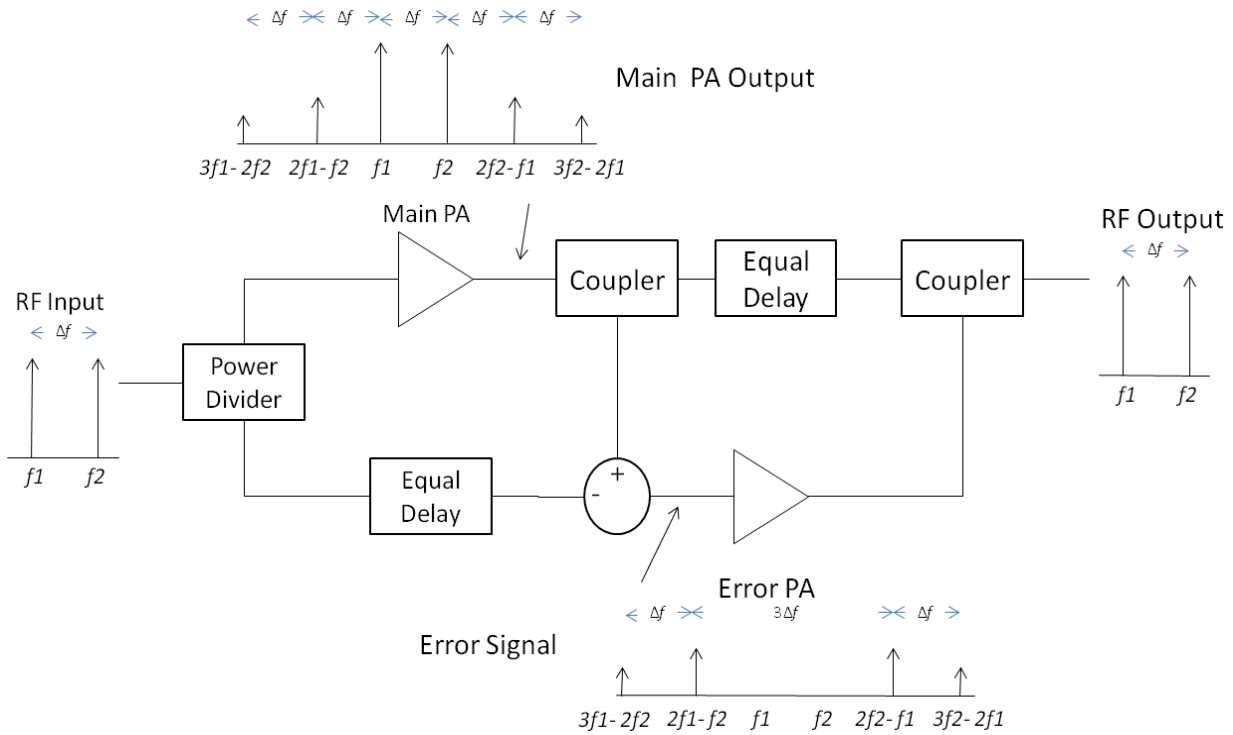


Figure 1.16: Basic Feedforward Error Correction Loop

1.4.3 Predistortion

Predistortion consists of adjusting the magnitude and phase of the input signal before the PA, such that the PA-predistorter (PD) pair appears as linear device. One aspect that is often overlooked is that the use of a PD will always create new distortion components not present in the original un-predistorted PA response. Thus, the output of the PD will display a spectrum of distortion products which exceed the spectral BW of the uncorrected PA. Analog predistorters are often crude and consist of using attenuators with an expansive insertion loss characteristic [1]. With the advent of Digital Signal Processing (DSP), analog predistortion has become a much more complex method of accomplishing what can be easily done using digital techniques.

Hence, this section focuses on the significantly more popular and useful Digital PreDistortion (DPD). Indeed, thanks to developments in high speed DSP, baseband DPD is the most actively researched area of linearization. The basic principle behind DPD consists of creating an inverse function for the PA and using this function in series with the PA as shown in

Figure 1.17. This means that an accurate behavioral model is crucial to the implementation of the DPD. The predistorter usually consists of a series of Look Up Tables (LUT).

Unfortunately, early versions of linearizers using this technique achieved very modest results (10 dB to15 dB reductions of ACPR). The reason for these poor results was found to be short-term variations in PA characteristics, called memory effects. This leads to more complicated DPD algorithms, which use previous signal values to determine the appropriate correction. Further improvement, can be achieved, by adding an adaptation loop in the DPD system.

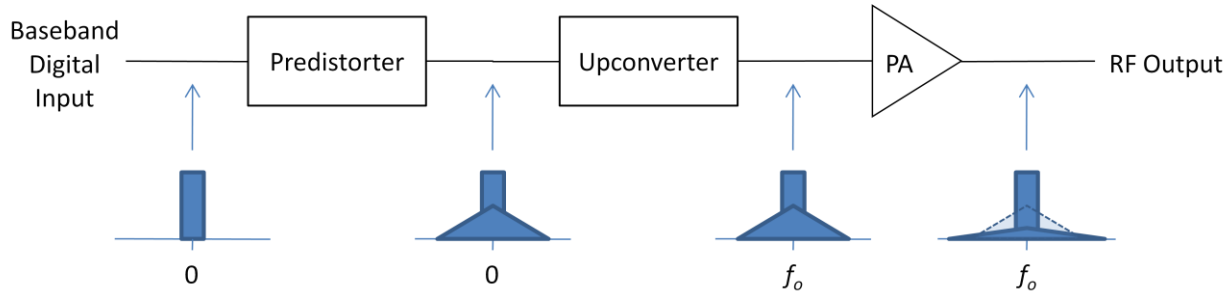


Figure 1.17: Digital Predistortion Linearizer Setup with Signal Spectrums

1.4.4 Performance Comparison

The indirect feedback linearization system has several limitations, notably it cannot increase the intrinsic power saturation of the device. Additionally, AM-PM effects are not corrected with this method. Furthermore, delays in the detection and signal processing become severe for stable operation when linearizing signals with large bandwidths.

The advantage of the Cartesian Loop method is that the symmetry of gain and bandwidth in the I and Q paths reduces the phase shifts between AM-AM and AM-PM processes which are principally responsible for asymmetrical inter-modulation products. Moreover, the use of a synthesized RF source enables the Cartesian Loop to be a frequency agile solution. While reductions of 30 dB in the IM products have been reported, the video bandwidth and stability of this architecture limit its use to signal modulation bandwidths under 100 KHz.

In the case of the Polar Loop modulator, while it has shown the ability to greatly improve lower inter-modulation products, such as IMD3 and IMD5, higher order products can be uncorrected or even increased. This is due to the limitations on video bandwidth and stability. Additionally, these limitations restrict the usefulness of this technique to single carrier

applications. Nevertheless, when limited to single carrier applications, average efficiencies of greater than 50% and IMD3 products of 50 dBc have been reported [14]. Although difficult to implement, this scheme is becoming more popular, especially in handset applications using challenging modulation schemes such as EDGE, which has taxing demands on the linearity-efficiency tradeoff in traditional Class AB architectures.

The key advantage in the feedforward process is that both amplitude and phase errors are corrected. The major drawback of this solution is that the Error PA needs to be extremely linear, which limits the overall power efficiency of the overall solution to 10% to 15%. Furthermore, variations in frequency and temperature cause gain and phase alignment errors in the error PA. Moreover, the gain and phase tracking requirements for the error PA to obtain significant linearity improvements are extremely stringent: less than 0.01 dB of Gain error and less than 1degree of phase error to obtain a reduction of 40 dB in the IMD3. Thus, while feedforward does offer some advantages, the power efficiency limitations do not make it an attractive solution for multi-carrier base station applications.

Modern DPD linearizers yield a 20 dB to 30 dB improvement in ACPR of the PA over a significant bandwidth. Additionally, due to the low power consumption of the DPD relative to the PA, there is no significant degradation in the transmitter's power efficiency. Furthermore, DPDs are extremely flexible. However, the DPD is the only system which requires thorough behavioral modeling of the PA, which can significantly increase its implementation complexity.

A summary of these results is shown in Table 1.1.

TABLE 1-1: COMPARISON OF LINEARIZATION TECHNIQUES

Linearization Technique	**Complexity**	**Power Efficiency**	**Bandwidth**	**Cancellation Performance**
Indirect Feedback	Low	Moderate	Low	Low
Cartesian Loop	Moderate	High	Low	High
Polar Loop	High	High	Low	High
Feed Forward	High	Moderate	High	High
DPD	High	High	High	High

1.5 Proposed Solution

Since the focus of this project is a base station application, the three most important criteria when evaluating the proposed solution are power efficiency, bandwidth and cancellation performance. The only linearization technique that can achieve high performance in all these criteria is the DPD. Thus, a DPA when coupled with a DPD should display good average efficiency over a large dynamic range while meeting the stringent linearity requirements for multiple carriers. In fact it has been shown in the literature that this is a promising solution for wideband multi-carrier applications.

Nevertheless, it is desirable to reduce the complexity of the algorithms necessary for DPDs to meet the linearity requirements. Thus, it is necessary to reduce memory effects through more careful design. Therefore, it becomes necessary to build a systematic design approach that can be used to minimize memory effects which is universally applicable.

Chapter 2:

Characterization of Power Amplifier Nonlinearity

This chapter reviews memory effects and where they originate from in power amplifiers. Section 2.1 examines some basic non-linear modeling of Power Amplifiers and how this can be used to gain a greater understanding of the motivation behind early DPD linearization attempts. Sections 2.2 and 2.3 examine memory effects, which have led to more complex models being used for state-of-the-art DPD linearizers with more success.

2.1 Memoryless Behavior

Traditionally, Power Amplifiers are modeled as nonlinear, memoryless devices, often using a polynomial model because it allows for easy calculation of spectral components. Assuming the use of a fifth order polynomial to model the PA's behavior, the PA output can be described by

$$y = a_1 x + a_2 x^2 + a_3 x^3 + a_4 x^4 + a_5 x^5 \tag{2-1}$$

where x and y are the PA input and output respectively, and a_1 to a_5 are the complex polynomial coefficients.

To quantify the undesired spectral component the PA will produce as a function of the instantaneous bandwidth of the input signal, x, a two tone input signal consisting of two pure sinusoids at f_1 and f_2 is used, where

$$x = A(\cos(f_1 t + \emptyset_1) + \cos(f_2 t + \emptyset_2)) \tag{2-2}$$

where A is the signal magnitude, $\emptyset_1$ and $\emptyset_2$ are the phase shifts of the first and second tone respectively.

While the input signal may be band-limited, the output of the PA will consist of numerous inter-modulation products in several frequency bands. Figure 2.1 shows some of the output frequency products at baseband, fundamental and second harmonic frequency bands.

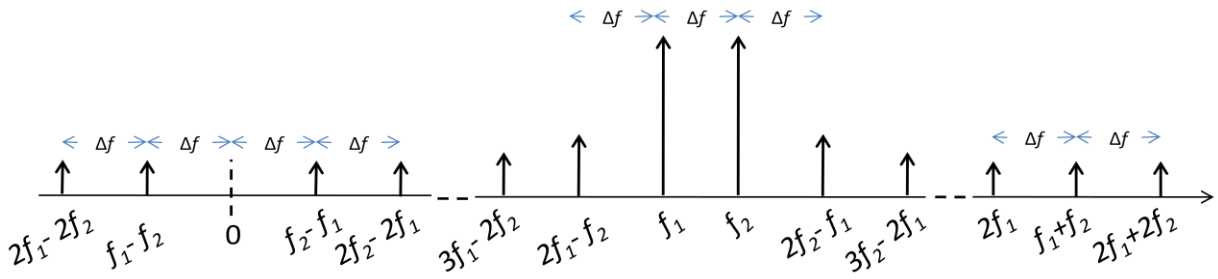


Figure 2.1: Output Spectrum of a Nonlinear System When Stimulated with a Two Tone Input

By expanding Equation (2-1) and simplifying for the spectral components, one can obtain the magnitude of all the spectral components. The results of this operation are shown in Table 2.1.

TABLE 2-1: MAGITUDE AND FREQUENCY OF THE POWER AMPLIFIER SPECTUM COMPONENTS

Frequency	Name	Magnitude
0	DC	$A^2a_2 + A^4a_4\frac{9}{4}$
$f_2 - f_1$	2nd Order Envelope	$A^2a_2 + A^4a_43$
$2f_2 - 2f_1$	4th Order Envelope	$A^4\left(a_4\frac{3}{4}\right)$
$3f_1 - 2f_2$	IMD5 Left	$\frac{5}{8}a_5A^5$
$2f_1 - f_2$	IMD3 Left	$\frac{3}{4}a_3A^3 + \frac{25}{8}a_5A^5$
f_1	Fundamental Left	$a_1A + \frac{9}{4}a_3A^3 + \frac{25}{4}a_5A^5$
f_2	Fundamental Right	$Aa_1 + A^3a_3\frac{9}{4} + A^5a_5\frac{25}{4}$
$2f_2 - f_1$	IMD3 Right	$A^3a_3\frac{3}{4} + A^5a_5\frac{25}{8}$
$3f_2 - 2f_2$	IMD5 Right	$A^5\left(a_5\frac{5}{8}\right)$
$3f_1 - f_2$	Second Harmonic Difference Left	$A^4\left(a_4\frac{1}{2}\right)$

$2f_1$	Second Harmonic Left	$A^2a_2\frac{1}{2}+A^4a_42$
f_1+f_2	Second Harmonic Sum	$A^2a_2+A^4a_43$
$2f_2$	Second Harmonic Right	$A^2a_2\frac{1}{2}+A^4a_42$
$3f_2-f_1$	Second Harmonic Difference Right	$A^4\left(a_4\frac{1}{2}\right)$
$4f_1-f_2$	Third Harmonic Difference Left	$A^5\left(a_5\frac{5}{16}\right)$
$3f_1$	Third Harmonic Left	$A^3a_3\frac{1}{4}+A^5a_5\frac{25}{16}$
$2f_1+f_2$	Third Harmonic Sum Left	$A^3a_3\frac{3}{4}+A^5a_5\frac{25}{8}$
$2f_2+f_1$	Third Harmonic Sum Right	$A^3a_3\frac{3}{4}+A^5a_5\frac{25}{8}$
$3f_2$	Third Harmonic Right	$A^3a_3\frac{1}{4}+A^5a_5\frac{25}{16}$
$4f_2-f_1$	Third Harmonic Difference Right	$A^5\left(a_5\frac{5}{16}\right)$
$4f_1$	Fourth Harmonic Left	$A^4\left(a_4\frac{1}{8}\right)$
$3f_1+f_2$	Fourth Harmonic Sum Left	$A^4\left(a_4\frac{1}{2}\right)$
$2f_1+2f_2$	Fourth Harmonic Sum Centre	$A^4\left(a_4\frac{1}{2}\right)$
$3f_2+f_1$	Fourth Harmonic Sum Right	$A^4\left(a_4\frac{1}{2}\right)$
$4f_2$	Fourth Harmonic Right	$A^4\left(a_4\frac{1}{8}\right)$
$5f_1$	Fifth Harmonic Left	$A^5\left(a_5\frac{1}{16}\right)$
$4f_1+f_2$	Fifth Harmonic Sum Outer Left	$A^5\left(a_5\frac{5}{16}\right)$
$3f_1+2f_2$	Fifth Harmonic Sum Inner Left	$A^5\left(a_5\frac{5}{8}\right)$

$3f_2 + 2f_1$	Fifth Harmonic Sum Inner Right	$A^5\left(a_5\frac{5}{8}\right)$
$4f_2 + f_1$	Fifth Harmonic Sum Outer Right	$A^5\left(a_5\frac{5}{16}\right)$
$5f_2$	Fifth Harmonic Right	$A^5\left(a_5\frac{1}{16}\right)$

This table shows that in a nonlinear, memoryless device, the magnitudes of the intermodulation components are not dependent on the instantaneous bandwidth of the signal. However, we know that in real devices, the magnitude of the third and fifth order intermodulation products exhibits a dependence on the instantaneous bandwidth of the signal. This indicates the presence of bandwidth dependent nonlinear effects with memory. These nonlinear effects are described as memory effects and are further classified into two distinct categories: thermal memory effects and electrical memory effects.

2.2 PA Behavior With Memory Effects

This section explores the two different sources of memory effects in PA behavior.

2.2.1 Thermal Memory Effects

A power amplifier's performance is affected by several factors. One of the factors that is sometimes overlooked is the dynamic temperature variation and its effect on the electrical properties of the transistor. While much effort is put into cooling systems for high power amplifiers, it is impossible to obtain a perfectly a constant temperature due to fluctuations in the drive level in the input signals. Figure 2.2 illustrates the IMD3 contribution of thermal memory effects as a function of tone spacing in a typical LDMOS amplifier. One can see that the contribution drops by almost 20 dB over 4 MHz

As discussed earlier, one of the simplest tests to detect memory effects is the two tone test. Examining the IMD3 of a PA as the tone spacing is varied in a two-tone test can help reveal the source of the memory effects. If the PA's IMD3 levels vary significantly when the tone spacing is 100 KHz to a few MHz, then thermal memory effects are the likely culprit.

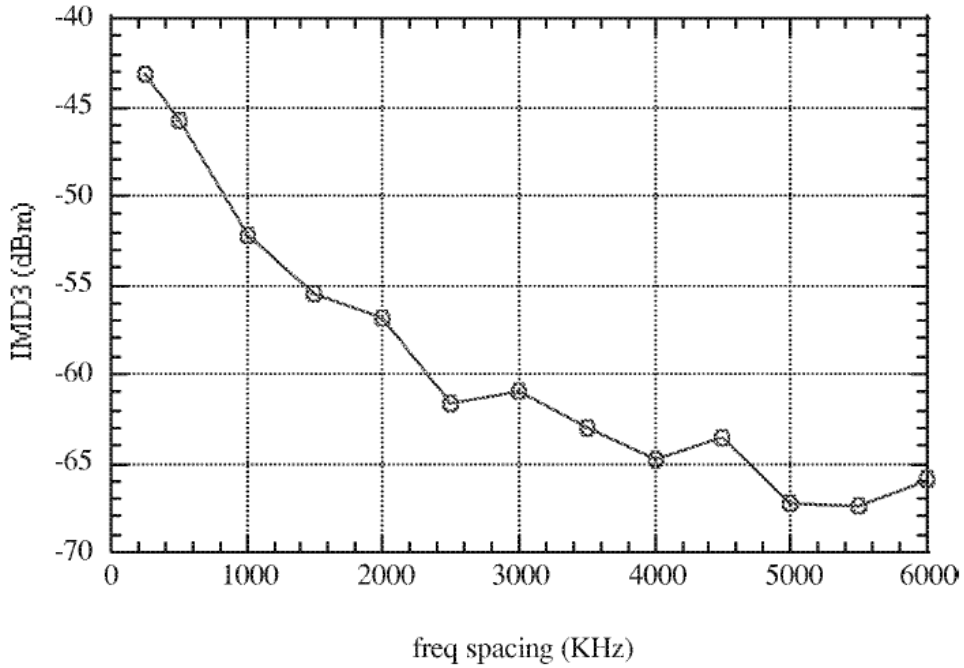


Figure 2.2: IMD3 Amplitude due to Thermal Memory Effects Versus Frequency Spacing

2.2.2 Electrical Memory Effects

To determine how electrical memory effects originate, it is crucial to understand how real power amplifiers differ from the memoryless polynomial model presented in the earlier section. This section explores the causes of electrical memory effects which are prevalent at modulation bandwidths of greater than 1 MHz. First, a qualitative understanding of the node impedances of power amplifiers is explored. The effect of these impedances on the distortion components is examined. Finally, the relation between the power amplifier design and memory effects is discussed.

Figure 2.3 shows a simplified block diagram of a power amplifier's output node. From this diagram, we can see that there are three factors that will determine the output node impedance:

- The transistor's bias dependent output impedance
- The Matching Network (MN) impedance
- The Bias Network (BN) impedance

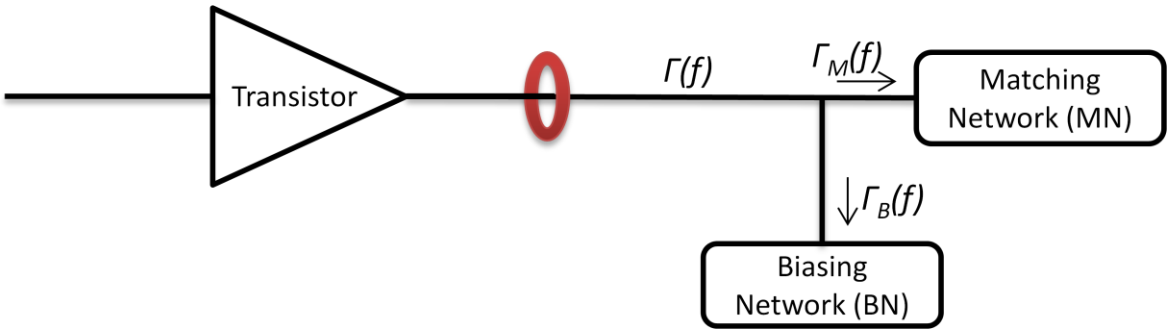


Figure 2.3: Output Node Impedance Block Diagram

The transistor's output impedance is generally fixed when the class of operation of the PA is decided. The Matching Network (MN) is generally designed as a band pass network and as such has the most impact on the fundamental band and will generally reflect all other harmonics back into the transistor. Similarly, the Biasing Network (BN) is designed as a lowpass filter to allow DC power to flow to the transistor while blocking all RF signals. As such, the BN has the most significant impact on intermodulation products in the baseband frequency range. As a note, the preferred bias topology in today's RF PA usually involves the use of a quarter wavelength transformer. This topology, which is usually designed to present an open circuit at the fundamental frequency, will present a short circuit at all even harmonics. Therefore, the bias network will influence the output node impedance at all even harmonics if this topology is used.

To understand how these impedances contribute to memory effects the PA can be modeled using the simplified block diagram shown in Figure 2.4, where $G(f)$ represents a memoryless nonlinearity produced by the power amplifier, $H(f)$ is a linear function representing the reflection coefficient of the output node, and x, y and z are the PA input, signal components re-injected into the PA, and the PA output respectively.

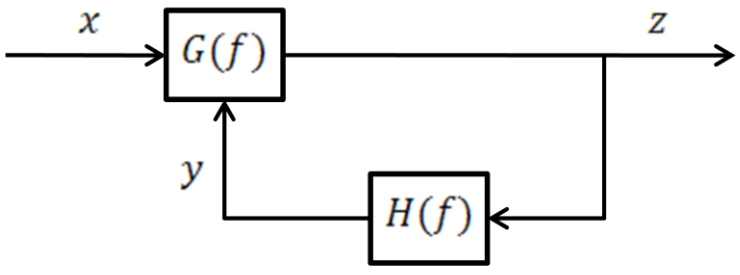


Figure 2.4: Simplified Block Diagram of the PA Nonlinearity Mechanism

The reflected signal components are remixed via the nonlinearity in the PA back into the fundamental frequency band. If we begin with an initial assumption that H is an all pass filter to simplify the analysis, the coefficients of these reflected components can be calculated using simple trigonometric identities. Table 2.2 illustrates all of the frequency combinations that will result in creating a product that is at the same frequency as the right IMD3 product. For example, the second harmonic left component ($2f_2$) will mix with the right fundamental (f_1) to produce an additional right IMD3 component via a 2nd order nonlinearity. Note here that some frequency components appear to be replicated, this is not the case. For example the second entry in Table 2-2 is a third order recombination product which can be obtained from developing the expression $\cos^2(f_2 - f_1)\cos(f_1)$ and separating it into its various frequency components. Conversely the third entry is obtained from developing the second order expression $cos(2f_2 - 2f_1)\cos(f_1)$.

TABLE 2-2: FREQUENCY COMPONENTS THAT WILL REMIX INTO THE RIGHT IMD3 PRODUCT

Frequency 1	Frequency 2	Nonlinearity Mixing Order	Coefficient
$f_2 - f_1$	f_2	2nd Order	$A^3 a_1 a_2^2$
$2(f_2 - f_1)$	f_1	3rd Order	$\frac{3}{4} A^5 a_1 a_2^2 a_3$
$2f_2 - 2f_1$	f_1	2nd Order	$\frac{3}{4} A^5 a_1 a_2 a_4$
$3f_1 - 2f_2$	$4(f_2 - f_1)$	5th Order	$\frac{25}{128} A^{13} a_2^4 a_5^2$
$3f_1 - 2f_2$	$2(2f_2 - 2f_1)$	3rd Order	$\frac{45}{128} A^{13} a_3\ a_4^2 a_5$
$2f_1 - f_2$	$3(f_2 - f_1)$	4th Order	$\frac{3}{8} A^9 a_2^3 a_3\ a_4$
$3f_2 - 2f_1$	$-(f_2 - f_1)$	2nd Order	$\frac{5}{8} A^7 a_2^2 a_5$
$-(3f_1 - f_2)$	$2f_1 + f_2$	2nd Order	$\frac{3}{8} A^7 a_2\ a_3\ a_4$
$-(2f_1)$	$2f_2 + f_1$	2nd Order	$\frac{3}{8} A^5 a_2^2 a_3$
$-2(f_1)$	$2f_2 + f_1$	3rd Order	$\frac{9}{16} A^5 a_2\ a_3^2$

$f_2 + f_1$	$-(2f_1 + f_2)$	2nd Order	$\frac{3}{4}A^5 a_2^2 a_3$
$2f_2$	$-f_1$	2nd Order	$\frac{1}{2}A^3 a_1\ a_2^2$
$2(f_2)$	$-f_1$	3rd Order	$\frac{3}{4}A^3 a_1^3 a_2$
$3f_2 - f_1$	$-f_2$	2nd Order	$\frac{1}{2}A^5 a_1\ a_2\ a_4$
$-(4f_1 - f_2)$	$3f_1 + f_2$	2nd Order	$\frac{5}{32}A^9 a_2 a_4 a_5$
$3f_1$	$-2(2f_1 - f_2)$	3rd Order	$\frac{27}{256}A^9 a_3^4$
$3(f_1)$	$-2(2f_1 - f_2)$	5th Order	$\frac{45}{128}A^9 a_1^3 a_3^2 a_5$
$3f_2$	$-(f_2 + f_1)$	2nd Order	$\frac{1}{4}A^5 a_2^2 a_3$
$3(f_2)$	$-(\omega_2 + f_1)$	4th Order	$\frac{1}{2}A^5 a_1^3 a_2\ a_4$
$4f_2 - f_1$	$-(2f_2)$	2nd Order	$\frac{5}{32}A^5 a_2^2 a_5$
$4f_2 - f_1$	$-2(f_2)$	3rd Order	$\frac{15}{64}A^5 a_1^2 a_3\ a_5$
$2f_1 + 2f_2$	$-(3f_1)$	2nd Order	$\frac{1}{8}A^7 a_2\ a_3\ a_4$
$2(f_1 + f_2)$	$-(3f_1)$	3rd Order	$\frac{3}{16}A^7 a_2^2 a_3^2$
$2(f_1 + f_2)$	$-3(f_1)$	5th Order	$\frac{5}{8}A^7 a_1^3 a_2^2 a_5$
$(2f_1 + 2f_2)$	$-3(f_1)$	4th Order	$\frac{5}{8}A^7 a_1^3 a_4^2$
$3f_2 + f_1$	$-(2f_1 + f_2)$	2nd Order	$\frac{3}{8}A^7 a_2\ a_3\ a_4$
$4f_2$	$-(2f_2 + f_1)$	2nd Order	$\frac{3}{32}A^7 a_2\ a_3\ a_4$
$2(2f_2)$	$-(2f_2 + f_1)$	3rd Order	$\frac{9}{64}A^7 a_2^2 a_3^2$

$4(f_2)$	$-(2f_2+f_1)$	5th Order	$\frac{15}{64}A^7a_1^4a_3\ a_5$
$5f_1$	$-2(3f_1+f_2)$	3rd Order	$\frac{3}{256}A^{13}a_3^3a_5$
$-(4f_1+f_2)$	$3(f_1+f_2)$	4th Order	$\frac{5}{32}A^{11}a_2^3a_4\ a_5$
$3f_1+2f_2$	$-(4f_1)$	2nd Order	$\frac{5}{64}A^9a_2\ a_4\ a_5$
$3f_1+2f_2$	$-2(2f_1)$	3rd Order	$\frac{15}{128}A^9a_2^2a_3\ a_5$
$3f_1+2f_2$	$-4(f_1)$	5th Order	$\frac{25}{128}A^9a_1^4a_5^2$
$3f_2+2f_1$	$-(3f_1+f_2)$	2nd Order	$\frac{25}{64}A^9a_2\ a_4\ a_5$
$4f_2+f_1$	$-(2f_1+2f_2)$	2nd Order	$\frac{5}{32}A^9a_2\ a_4\ a_5$
$4f_2+f_1$	$-2(f_1+f_2)$	3rd Order	$\frac{15}{64}A^9a_2^2a_3\ a_5$
$5f_2$	$-(3f_2+f_1)$	2nd Order	$\frac{1}{32}A^9a_2\ a_4\ a_5$

Similarly, Table 2-3 shows the frequency combinations that will produce distortion in the right IMD5 component.

TABLE 2-3: FREQUENCY COMPONENTS THAT WILL REMIX INTO THE RIGHT IMD5 PRODUCT

Frequency 1	Frequency 2	Nonlinearity Mixing Order	Coefficient
f_2-f_1	$2f_2-f_1$	2nd Order	$\frac{3}{4}A^5a_2^2a_3$
$2(f_2-f_1)$	f_2	3rd Order	$\frac{3}{4}A^5a_1\ a_2^3$
$2f_2-2f_1$	f_2	2nd Order	$\frac{3}{4}A^5a_1\ a_2\ a_4$
$-(3f_1-2f_2)$	f_1+f_2	2nd Order	$\frac{5}{8}A^7a_2^2a_5$
$2f_1-f_2$	$4(f_2-f_1)$	5th Order	$\frac{15}{64}A^{11}a_2^4a_3\ a_5$

$2f_1 - f_2$	$2(2f_2 - 2f_1)$	3rd Order	$\frac{81}{256}A^{11}a_3^2a_4^2$
f_1	$3(f_2 - f_1)$	4th Order	$\frac{1}{2}A^4a_1\ a_2\ a_4$
$-(3f_1 - f_2)$	$2f_2 + f_1$	2nd Order	$\frac{3}{8}A^7a_2\ a_3\ a_4$
$-(2f_1)$	$3f_2$	2nd Order	$\frac{1}{8}A^5a_2^2a_3$
$-2(f_1)$	$3f_2$	3rd Order	$\frac{3}{16}A^5a_1^2a_3^2$
$-2(f_1)$	$3(f_2)$	5th Order	$\frac{5}{8}A^5a_1^5a_5$
$-(2f_1)$	$3(f_2)$	4th Order	$\frac{1}{4}A^5a_1^3a_2\ a_4$
$2f_2$	$-(2f_1 - f_2)$	2nd Order	$\frac{3}{8}A^5a_2^2a_3$
$2(f_2)$	$-(2f_1 - f_2)$	3rd Order	$\frac{9}{16}A^5a_1^2a_3^2$
$3f_2 - f_1$	$-f_1$	2nd Order	$\frac{1}{2}A^5a_1\ a_2\ a_4$
$-(4f_1 - f_2)$	$2f_1 + 2f_2$	2nd Order	$\frac{15}{64}A^9a_2\ a_4\ a_5$
$-(4f_1 - f_2)$	$2(f_1 + f_2)$	3rd Order	$\frac{15}{64}A^7a_2^2a_3\ a_5$
$4f_1 - f_2$	$-2(3f_1 - 2f_2)$	3rd Order	$\frac{375}{4096}A^{15}a_3\ a_5^3$
$-3f_1$	$3f_2 + f_1$	2nd Order	$\frac{1}{8}A^7a_2^2a_3\ a_4$
$-3(f_1)$	$3f_2 + f_1$	4th Order	$\frac{1}{2}A^7a_1^3a_4^2$
$4f_2 - f_1$	$-(f_1 + f_2)$	2nd Order	$\frac{5}{16}A^7a_2^2a_5$
$4f_2$	$-(2f_1 + f_2)$	2nd Order	$\frac{3}{32}A^7a_2\ a_3\ a_4$
$2(2f_2)$	$-(2f_1 + f_2)$	3rd Order	$\frac{9}{128}A^7a_2^2a_3^3$

$4(f_2)$	$-(2f_1+f_2)$	5th Order	$\frac{15}{64}A^7a_1^4a_3\ a_5$
$-5f_1$	$3(f_1+f_2)$	4th Order	$\frac{1}{32}A^{11}a_2^3a_4\ a_5$
$-(4f_1+f_2)$	$2(2f_2+3f_1)$	3rd Order	$\frac{375}{4096}A^{15}a_3\ a_5^3$
$3f_2+2f_1$	$-(4f_1)$	2nd Order	$\frac{5}{64}A^9a_2\ a_4\ a_5$
$3f_2+2f_1$	$-2(2f_1)$	3rd Order	$\frac{15}{512}A^9a_2^2a_3\ a_5$
$3f_2+2f_1$	$-4(f_1)$	5th Order	$\frac{25}{128}A^9a_1^4a_5^2$
$4f_2+f_1$	$-(3f_1+f_2)$	2nd Order	$\frac{5}{32}A^9a_2\ a_4\ a_5$
$5f_2$	$-(2f_1+2f_2)$	2nd Order	$\frac{1}{32}A^9a_2\ a_4\ a_5$
$5f_2$	$-2(f_1+f_2)$	3rd Order	$\frac{3}{64}A^9a_2^2a_3\ a_5$

While there is a significant number of combinations that will result in unwanted distortion in the fundamental band, most of them play a minor role in the distortion due to the frequency response of the linear element *H(f)* shown in Figure 2.4. The variation of the output node impedance as a function of frequency, as represented by the frequency response of *H(f)* is the cause of the frequency dependent electrical memory effects. While the output node impedance does vary to some degree in the each of the frequency bands, the frequency bands that will display the most variation are the baseband, fundamental and second harmonic bands. Hence, the distortion elements generated using frequency components from the third and higher frequency bands can be dismissed as trivial.

Assuming a centre frequency of 2.14 GHz and a modulation bandwidth of 20 MHz, the baseband response is important up to 40 MHz or beyond because of the 4th order envelope harmonic component. An important difference between the baseband frequency band and all others is that it is dependent on the modulation bandwidth and independent of the centre frequency. The fundamental band will be a 100 MHz, between 2.09 GHz and 2.19 GHz due to

the importance of the IMD5 distortion products. This bandwidth is a fairly significant design constraint as it represents 4.67% of the centre frequency. The second harmonic band is defined between 4.24 GHz and 4.32 GHz. While keeping this bandwidth does not seem to represent a significant portion of its centre frequency, the prevalence of the use of a second harmonic trap in the RF choke of the BN of most modern PAs is something that has not been examined in great detail.

Minimizing the memory effect generated from the baseband frequency harmonics becomes of pivotal importance as the band of interest is not dependent on the centre frequency of the transmitted signal. Conversely, the band of interest around the fundamental and second harmonic frequency bands on the centre frequency, is significantly more challenging. Hence, ensuring that the output node impedance is either very low or constant over this region through careful design of the bias network will minimize memory effects regardless of the intended frequency of operation of the PA.

Chapter 3:

Linearization of Multicarrier DPA using a Memory Polynomial Digital Predistorter

Chapters one and two demonstrated the need for a solution to the power efficiency and linearity problem that plagues modern PA designers. A Doherty power amplifier with digital predistortion was proposed as a solution to this problem. However, one must explore how this solution can offer the promised high average while meeting communication standards linearity requirements when stimulated with realistic test signals.

This chapter explores the various modeling techniques used to model PA nonlinearity and construct the corresponding DPDs. After some comparisons, a memory polynomial is chosen as the technique used for this thesis. The computation complexity of Memory Polynomial (MP) DPD is examined as well as ways to reduce it. Despite reducing the complexity of the required MP DPD, the fact remains that the DPA has strong memory effects. Hence, the MP DPD required to linearize the DPA to meet linearity requirements will be expensive from a computational standpoint. Therefore it becomes necessary to minimize memory effects at the design stage of the PA to reduce the complexity of the MP DPD required. ADS simulations and measurements were used to quantify the strength of the memory effects of the DPA using the linearity benchmarks described in Chapter 2. The results of these simulations show that ADS simulation cannot adequately predict memory effects at the design stage in the PA.

3.1 Motivation

As discussed earlier, Doherty power amplifiers have shown significant power efficiency enhancements over the standard Class AB linear counterparts at the cost of slightly decreased linearity. For an RF transmitter which uses a DPA to meet communication standards' requirements, linearization techniques are required. Among these techniques, Baseband Digital Predistortion is currently the most suitable linearization scheme, as it preserves the overall efficiency of an RF system. Baseband DPD exploits the advances in Digital Signal Processors (DSP) and Field Programmable Gate Arrays (FPGA). However, the application of DPD poses some challenges attributed to significant memory effects especially when driven with wideband and multi-carrier signals.

To improve the quality of signals, the DPD has to compensate for both the nonlinearities and memory effects of the transmitter PA. Various comprehensive DPD schemes such as Volterra series and their derivations (memory polynomials, Hammerstein, Wiener) and Neural Networks [15] were introduced in the literature to linearize wideband PAs.

3.2 Modeling Techniques

This section examines the 3 most commonly used behavioral models used to model PAs or to construct DPDs.

3.2.1 Volterra Series

A linear, causal system with memory can be described by the following:

$$y(t) = \int_{-\infty}^{\infty} h(\sigma)x(t-\sigma)d\sigma \tag{3-1}$$

where *x(t)* is the system's input, *y(t)* is its output and *h(t)* is its impulse response. A nonlinear system without memory can be described with a Taylor seies:

$$y(t) = \sum_{n=1}^{\infty} a_n[x(t)]^n \tag{3-2}$$

where *x(t)* is the system's input, *y(t)* is its output and a_n are the Taylor series coefficients.

A Volterra series combines the above two representations to describe a nonlinear system with memory as follows:

$$y(t) = \sum_{n=1}^{\infty} \frac{1}{n!} \int_{-\infty}^{\infty} du_1 \dots \int_{-\infty}^{\infty} du_n g_n(u_1, \dots, u_n) \prod_{r=1}^{n} x(t-u_r) \tag{3-3}$$

$$= \frac{1}{1!} \int_{-\infty}^{\infty} du_1 g_1(u_1)\, x(t-u_1) \tag{3-4}$$

$$+ \frac{1}{2!} \int_{-\infty}^{\infty} du_1(u_1) \int_{-\infty}^{\infty} du_2 g_2(u_1, u_2) x(t-u_1)\, x(t-u_2) \tag{3-5}$$

$$+ \frac{1}{3!} \int_{-\infty}^{\infty} du_1(u_1) \int_{-\infty}^{\infty} du_2 \int_{-\infty}^{\infty} du_3 g_3(u_1, u_2, u_3)\, x(t-u_1)x(t-u_2)x(t-u_3) \tag{3-6}$$

where *x(t)* is the system's input, *y(t)* is its output and $g_n(u_1, \dots, u_n)$ are the Volterra kernels of the systems. u_i represent time variables used to distinguish them better from *t*. One will recognize Equation (3-4) to be the familiar convolution shown in Equation (3-1), with $g_1(u_1)$ as

the impulse response. Hence, the Volterra kernerls where $n > 1$ can be likened to "n^{th} order impulse responses". [16]

While the Volterra representation is very powerful, its complexity makes it extremely cumbersome when used to model higher order non-linearities. Hence a number of approximations of the Volterra series have been proposed.

3.2.2 Weiner and Hammerstein Models

Hammerstein and Weiner models are examples of Volterra approximation that use two separate blocks to account for the nonlinearities and the memory effects. Also known as two-box-based models [17]-[21], these models are essentially permutations of each other. The Hammerstein model consists of a nonlinear block followed by a linear block, generally a filter, as shown in Figure 3.1. In the Weiner model, the linear block precedes the nonlinear one.

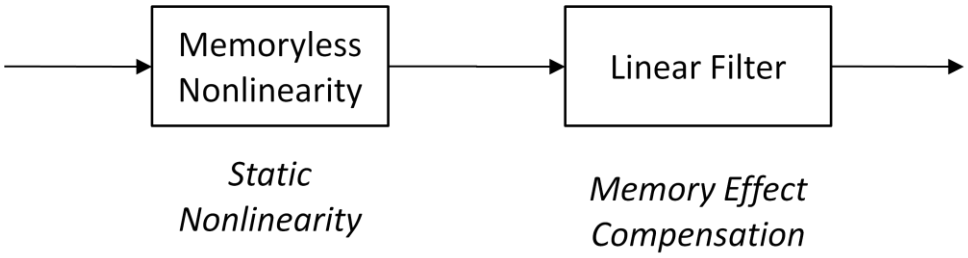


Figure 3.1: Typical Hammerstein PA Model

In the case of the PA, the first box of the Hammerstein scheme captures the static nonlinear behavior, while the second one is intended to account for the PA's memory effects. However, the limitations of conventional Hammerstein/Weiner schemes in mimicking wideband PA behavior have been demonstrated in [19]. While Parallel Hammerstein/Weiner models have been suggested [20] to address these limitations by stacking extra branches in parallel, parameter identification becomes extremely tedious.

3.2.3 Memory Polynomial Model

The memory polynomial is a comprehensive modeling scheme derived from the Volterra model. The multi-branch MP, as introduced by Kim et al. [21], requires less coefficients than the Volterra model while preserving its capability of accurately capturing memory and nonlinearity

effects. In fact the number of coefficients of a Volterra series of memory depth *K* and maximum polynomial order *P* can be written as:

$$number\ of\ coefficients = (K+1)^P \tag{3-7}$$

where as the coefficients of a memory polynomial of equal memory depth and maximum polynomial order is given by:

$$number\ of\ coefficients = P(K+1) \tag{3-8}$$

A typical memory polynomial structure is shown in Figure 3.2. Each branch is a polynomial Poly of degree *P* that can be expressed as:

$$Poly\ i = h_1\ x + h_2 x\ |x| + h_3 x\ |x|^2 + \cdots + h_P x\ |x|^{P-1} \tag{3-9}$$

The general model equation can be written as

$$y(n) = \sum_{k=0}^{K} \sum_{p=1}^{P} h_{p,k}\ |x(n-k)|^{p-1}\ x(n-k) \tag{3-10}$$

where *x(n)* and *y(n)* are the complex envelope signals at the predistorter input and output, respectively. *K* is the memory depth of the system, equivalent to the number of polynomial branches. *P* represents the polynomial order of the branches and $h_{p,k}$ designates the polynomial coefficients of the *k*th branch.

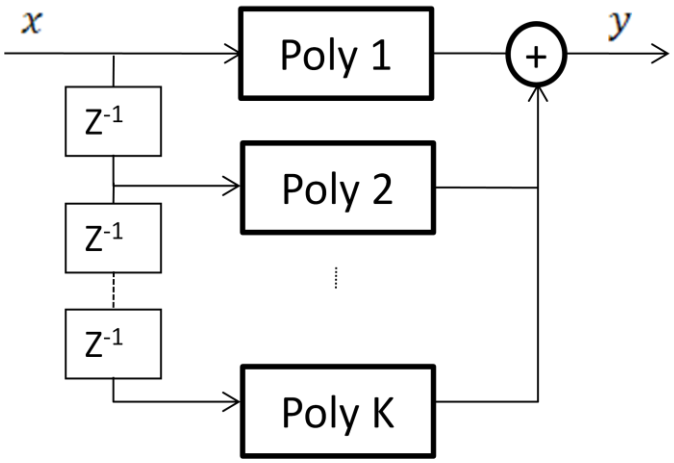


Figure 3.2: Typical Memory Polynomial Structure.

The identification of the DPD coefficients is done by solving the Least Squares Error problem formulated as $\boldsymbol{y} = \boldsymbol{A}\,\boldsymbol{B}$ and detailed in [22]; where

$$\boldsymbol{y} = [y(0) \quad \cdots \quad y(N)]^T \tag{3-11}$$

$$\boldsymbol{B} = [h_{1,0} \quad \cdots \quad h_{P,0} \quad h_{1K} \quad \cdots \quad h_{P,K}]^T \tag{3-12}$$

$$\boldsymbol{A} = [\boldsymbol{a}(0) \quad \cdots \quad \boldsymbol{a}(N)]^T \tag{3-13}$$

$$\boldsymbol{a}(n) = \big[\beta_1\big(x(n)\big) \quad \cdots \quad \beta_P\big(x(n)\big) \quad \beta_1\big(x(n-1)\big) \quad \cdots$$
$$\cdots \quad \beta_1(x(n-K)) \quad \cdots \quad \beta_P(x(n-K))] \tag{3-14}$$

where $\beta_p\big(x(n-k)\big) = |x^{p-1}(n-k)|x(n-k)$.

The coefficients of $\boldsymbol{B}$ are determined using LSE optimization and are calculated using the following:

$$\boldsymbol{B} = pinv(\boldsymbol{A})\boldsymbol{y} \tag{3-15}$$

where $pinv(\boldsymbol{A}) = (\boldsymbol{A^H A})^{-1}\boldsymbol{A^H}$ is the pseudo-inverse of the matrix $\boldsymbol{A}$.

The computational complexity of the DPD resides in the LSE algorithm's complexity being proportional to $(number\ of\ coefficients)^3$. Each reduction in the number of unknown coefficients significantly improves the realizability of the scheme. Moreover, the accuracy of the solution reached by such an algorithm depends directly on the conditioning of the matrix $\boldsymbol{A}$ [23]. Higher polynomial orders yield higher conditioning numbers, which in turn decreases the stability and accuracy of the DPD coefficient solution.

Henceforth, for both realizability and efficiency of DPD, the MP's number of branches and the polynomial orders of each branch must be carefully chosen to optimize the linearization outcome of the DPD and avoid the adverse effects of over or under-fitting of the problem.

The Memory Polynomial model is widely used to compensate for the RF PA behavior characteristics as it offers a good tradeoff between modeling accuracy and complexity of DSP

implementation. The complexity of the MP scheme is dependent on two parameters: (i) the order of the polynomial and (ii) the number of memory branches needed to compensate for both the nonlinearity and memory effects of the PA behavior. The values of these parameters required for an efficient DPD depend directly on the PA induced nonlinearities and memory effects.

3.3 Memory Polynomial Digital Predistortion Complexity Reduction

This section examines two different approaches to reducing the number of coefficients and hence decreases the computational complexity of the MP DPD.

3.3.1 Memory Polynomial Over and Under-Fitting

When evaluating a MP-DPD, it has been implied that increasing polynomial orders provides a better fit for the nonlinearities of the PA and improves the DPD's linearization capacity. This "over fitting" the PA behavior with higher orders of polynomials than are actually needed, not only decreases the stability of the DPD coefficient computations but also has no noticeable effect on the linearization outcome. Moreover, experimental results indicate that a MP having only odd orders can achieve similar linearization as a full odd and even order MP despite the reduced number of coefficients.

In this chapter, a Doherty power amplifier was used in conjunction with a complexity reduced MP-DPD to show the effects of over-fitting and under-fitting on a linearization capability when driven with a 4 carrier WCDMA test signal. Finding the lowest and satisfactory polynomial order is shown to be crucial in the system conditioning and thus the Least Square Error (LSE) solution accuracy, which in turn lowers the calculation and implementation requirements of the DPD.

3.3.2 Memory Polynomial Even Order Omission

In this section, the necessity of using the full even and odd orders in the MP-DPD is investigated. Experiments were performed to compare the linearization outcome of

- a MP-DPD using the full even and odd nonlinear terms
- a MP-DPD where the even-order terms are eliminated

The same polynomial orders and same number of branches were used in both cases. Even order terms, as shown in the experimental results of the next section, can be omitted from the

model used, achieving the same linearization results obtained using full odd and even order MP-DPD. The odd-order only MP-DPD model equation can be written as in (1), where *p* takes odd values only. Thus, the number of coefficients required by the DPD is reduced from $number\ of\ coefficients = P.(K+1)$ required by the full even and odd MP-DPD to $number\ of\ coefficients_{odd} = \frac{(P+1)}{2}(K+1)$; *P* is assumed to be odd. Eliminating the even order terms in the MP-DPD reduces the LSE algorithm order of complexity by a factor of 8 as compared to that of the full MP.

Another advantage of using odd-only complexity reduced MP resides in the drastic improvement of the conditioning number of matrix *A* described in the previous section. *A* is not as ill-conditioned as in the typical MP case, and *cond(**A**)* drops significantly implying a better DPD coefficient solution convergence and accuracy.

3.3.3 Unequal Order Memory Polynomial

The distortion introduced by the RF PA is generally due to a high order static nonlinearity when driven with narrowband signals. However, when stimulated with wideband input signals, the PA also exhibits lower order dynamic nonlinearities attributed to the memory effects. Hence, it is expected that one can use lower order polynomials in the subsequent branches of the MP without compromising the linearization performance.

By assigning a different polynomial order to every branch of the structure, the optimized MP [24] can be defined as:

$$y(n) = \sum_{k=0}^{K} \sum_{p=1}^{P_k} h_{p,k}\ |x(n-k)|^{p-1}\ x(n-k) \tag{3-9}$$

where P_k represents the polynomial order of each branch. The optimized MP has *K*+1 memory branches and requires $number\ of\ coefficients = \sum_{k=0}^{K} P_k$ number of coefficients.

If both above mentioned complexity reduction approaches are concurrently applied, a significant drop of the LSE algorithm complexity and a lower *cond(**A**)* can be obtained. The number of coefficients of the different MP configurations is summarized in Table 3-1.

TABLE 3-1: SUMMARY OF THE NUMBER OF MP COEFFICIENT

	Number of Coefficient
Full MP	$P.(K+1)$
Odd-order only MP	$\frac{(P+1)}{2}.(K+1)$
Optimized MP	$\sum_{k=0}^{K} P_k$
Odd-only optimized MP	$\sum_{k=0}^{K}(\frac{P_k+1}{2})$

3.3.4 Performance Evaluation

Both theoretical and experimental validations of the DPD were conducted to determine the effect of these complexity reduction techniques on its PA linearization capacity. The theoretical figures of merit used to evaluate both the stability of the LSE algorithm and the complexity of implementation of the DPD scheme are the conditioning of matrix A and the number of coefficients required as well as *coeff* respectively.

In the experimental results, the linearization capability of the MP-DPD is evaluated using the measured ACPR, as well as observing the PA output spectrum.

3.4 Experimental Results

This section details the experimental work done to test the complexity reduction techniques discussed previously.

3.4.1 Test Setup

A lineup of 3 amplifiers was used as the Device Under Test (DUT) for the experimental validations. The three PAs were:

- 5 Watt IC driver (Freescale MHV5IC2215N)
- 100 Watt class AB driver (Freescale MRF6S21100H)
- 400 Watt Doherty PA (2x Freescale MRF7S21170H)

The experiment setup is shown in Figure 3.3. A 4 carrier WCDMA test signal was synthesized using Agilent's Advanced Design System (ADS). The signal is then predistorted if need be using Agilent Ptolemy. The signal is then uploaded to the vector signal generator and used to drive the PA lineup. The output of the PA lineup is then captured with the vector spectrum analyzer through the Agilent Vector Spectrum Analyzer (VSA) software. The PA

output is compared to the input signal in MATLAB to generate the MP-DPD using the LSE algorithm.

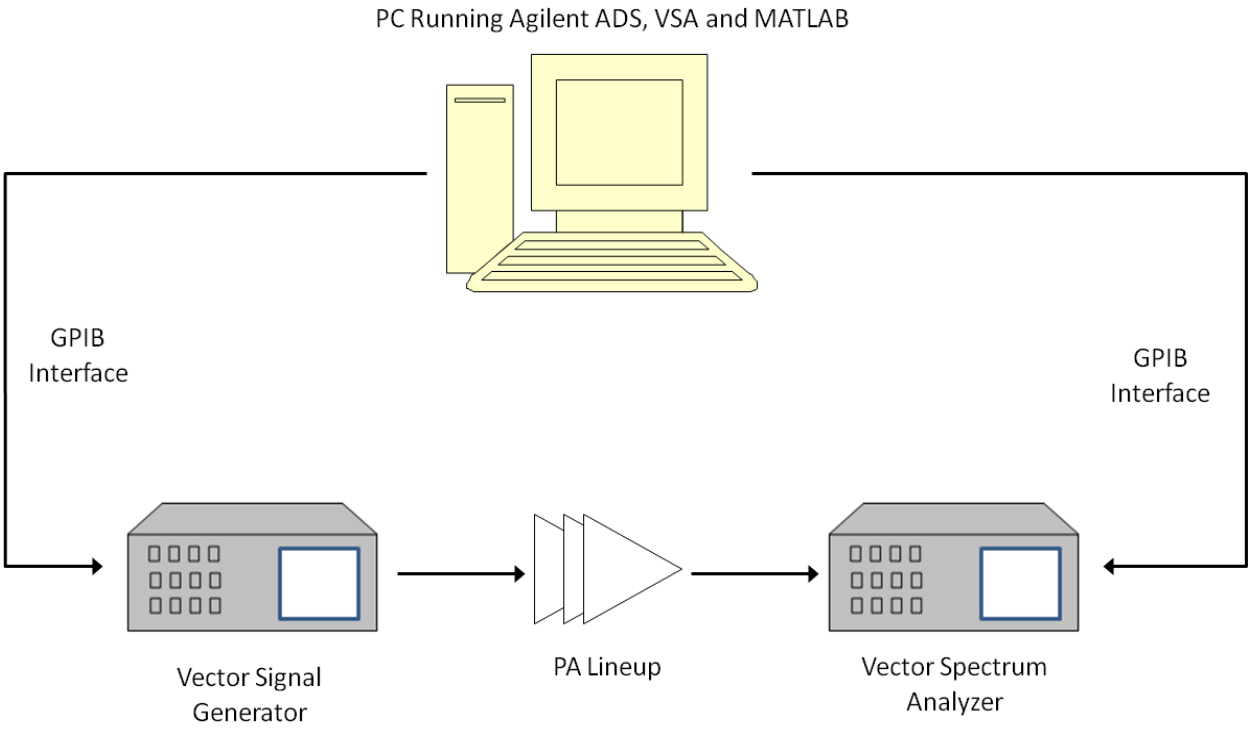


Figure 3.3: Experimental Setup

3.4.2 Under and Over-Fitting Memory Polynomial Digital Predistorters

Throughout the following sections, the DPD complexity reduction is evaluated against its linearization efficiency. Test cases were set up to determine appropriate MP orders and number of branches. These are compared in their relative context as shown in the following figures.

The first test scenario is to use the full MP with equal polynomial orders across its branches. A high order, large number of branches MP is used as a starting point. The complexity of this initial DPD is lowered by reducing the order of the MP and the number of branches used. The performance of these lower complexity DPDs is evaluated based on the different figures of merit summarized in Table 3-2.

Despite a significant reduction of the total number of coefficients using the 6x10 MP-DPD, the ACPR deteriorates. Furthermore, the matrix *A* is still ill conditioned using the 8x10 MP

DPD. Figure 3.4 shows the output spectrum of the signal using over and under-fitting DPD. One can observe the deterioration of the ACPR when the 6x10 DPD is used.

TABLE 3-2: MP ORDER REDUCTION

	ACPR (dBc) *Offset*			**Conditioning of *A***	**Total # of Coefficients**
DPD Used	5 MHz	10 MHz	15 MHz		
12x12	-50.45	-54.75	-57.6	1.97E+12	144
8x10	-50.3	-54.4	-57.3	1.33E+10	80
6x10	-49.15	-53.2	-57.5	1.27E+10	60

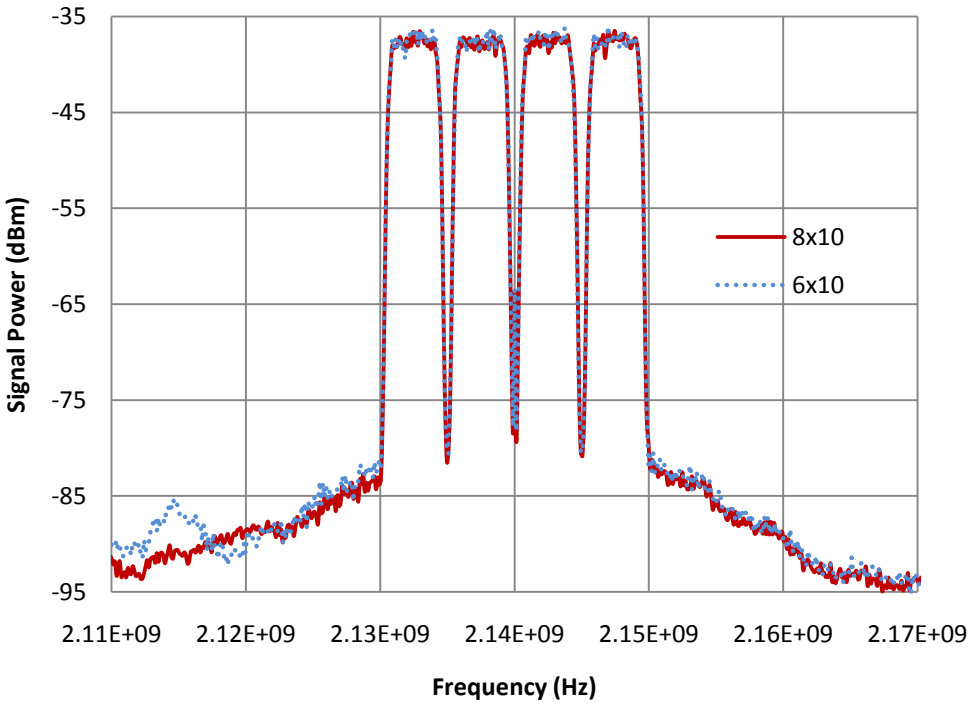


Figure 3.4: Linearized DPA Output Spectrum Using Under and Over-Fitted MP-DPD

3.4.3 Even and Odd Order Digital Predistorters

The next aspect of complexity reduction investigated is the elimination of the even order coefficients of the MP. This elimination maintains the linearity attained when using the full even and odd order MP-DPD as shown in Figure 3.5

Omitting the even order terms from the DPD maintains good linearity, as measured by the ACPR, while also improving on several other performance criteria. A significant improvement is achieved in the conditioning of matrix A (from 10^9 to 10^6), while reducing the total number of coefficients from 72 to 40. These results are summarized in Table 3-3.

TABLE 3-3: MP-DPD COMPLEXITY REDUCTION USING EVEN ORDER ELIMINATION

	ACPR (dBc) *Offset*			**Conditioning of *A***	**Total # of Coefficients**
DPD Used	5MHz	10MHz	15MHz		
8x9	-50.59	-55.08	-56.98	1.09E+09	72
8x9 Odd only	-49.7	-54.25	-55.99	1.46E+06	40

A MP-DPD of 8 branches each consisting of a 9th order polynomial with odd and even order terms is found to be the least complex full MP-DPD scheme that still achieves the desired -50 dBc ACPR (assessed with a bandwidth of 3.84 MHz). Hence, all MP-DPDs with further reductions in their complexity are evaluated against this "standard" MP-DPD.

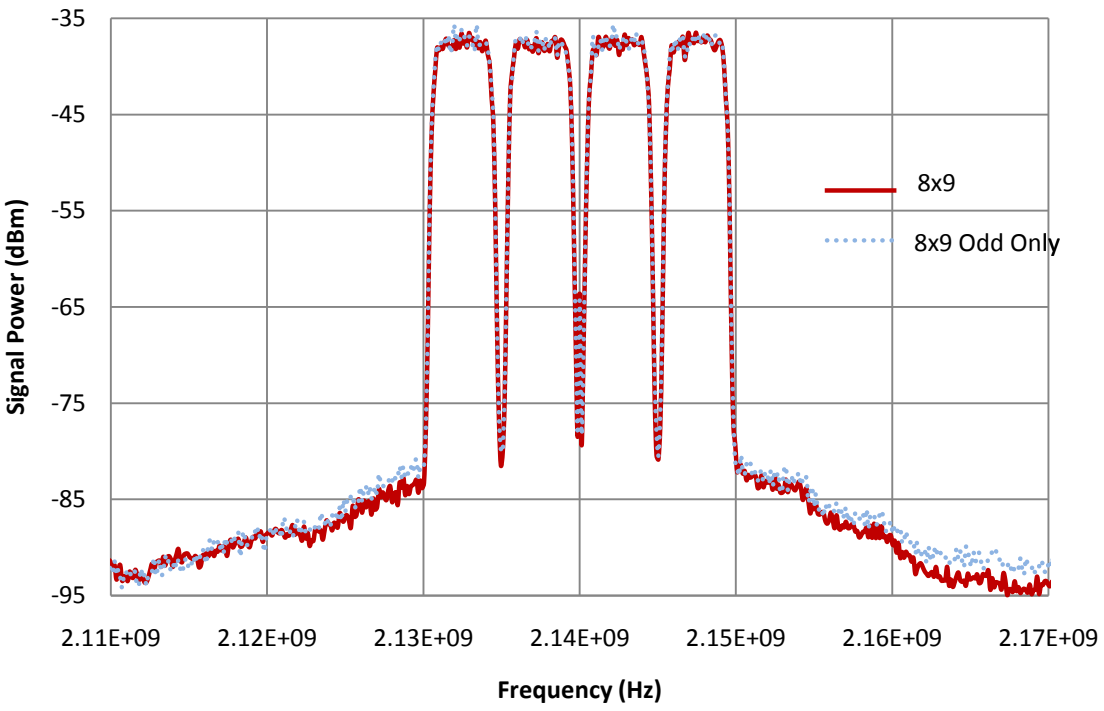


Figure 3.5: Linearized DPA Output Spectrum Using Odd Only Orders MP-DPD

3.4.4 Unequal MP Branch Orders DPD validation

The orders of the subsequent polynomial branches, in the odd-order MP, are now individually reduced as described in the second section. To clarify the notation, the 1st number refers to the number of branches and the second number refer to the polynomial order. For example, the 1x9_1x7_6x5 DPD has one branch of 9th order, one branch of 7th order and 6 branches of 5th order. The MP-DPD with the lowest number of coefficients that maintains the same linearity performance as obtained using the "standard" MP-DPD is shown in Figure 3.6.

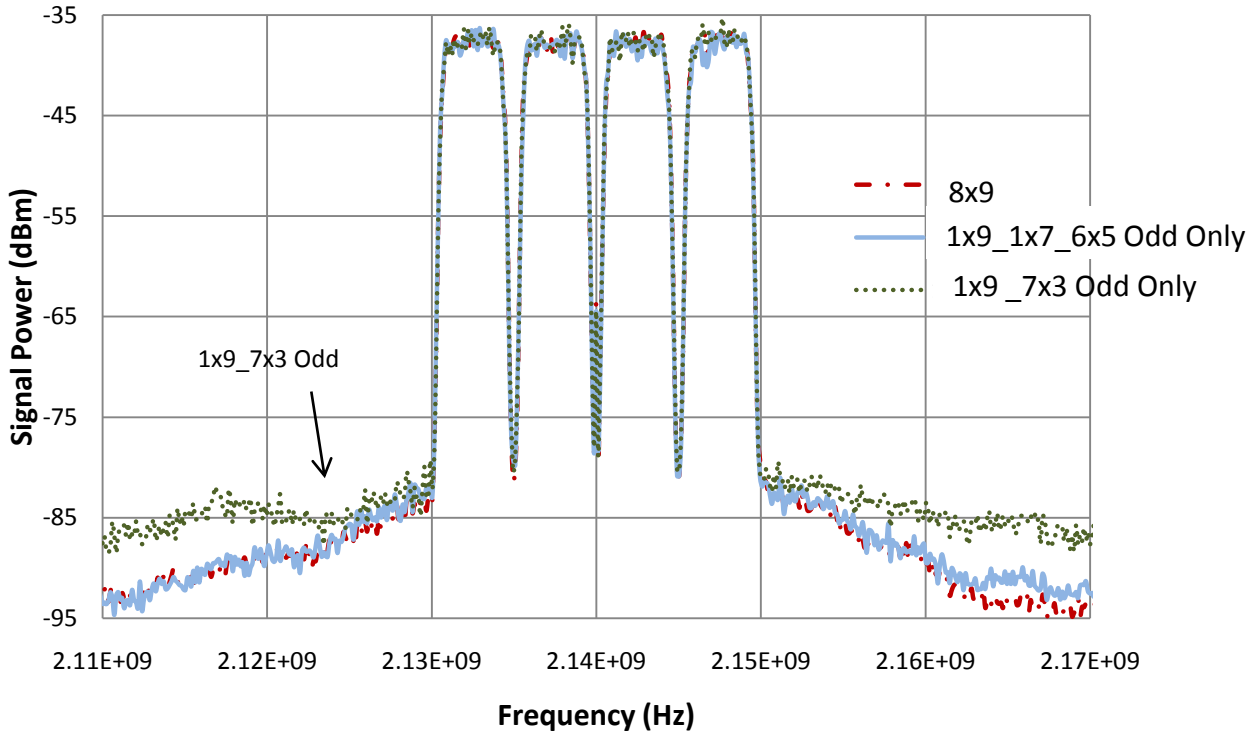


Figure 3.6: Linearized DPA Output Spectrum Using Reduced MP Branch Orders

The number of coefficients is reduced by a factor of 2.667 (72 as compared to 27) and the conditioning number is reduced by three orders of magnitude (from 10^9 to 10^6) compared to the "standard" MP scheme. Therefore, combining the even order elimination and the unequal MP-DPD approach greatly reduces the DPD complexity while maintaining good linearity performance as shown by the ACPR levels in Table 3-4.

The last DPD listed in the table demonstrates the important presence of 5th order distortions in the MP branches. The ACPR degrades significantly when the order of the

polynomials of the subsequent branches is reduced to less than 5. The deterioration of the ACPR can also be seen in Figure 3.6.

TABLE 3-4: UNEQUAL ODD ORDER ONLY MP

	ACPR (dBc) *Offset*			**Conditioning of *A***	**Total # of Coefficients**
DPD Used	5 MHz	10 MHz	15 MHz		
8x9	-50.59	-55.08	-56.9	1.09E+09	72
1x9_7x7 Odd Only	-50.45	-54.23	-56.3	1.05E+06	33
1x9_1x7_6x5 Odd Only	-50.3	-54.4	-57.3	1.05E+06	27
1x9_7x5Odd Only	-49.4	-53.6	-55.8	*1.05E+06*	26
1x9_7x3 Odd Only	-47.9	-50.9	-51.1	1.04E+06	19

3.4.5 Overall System Performance

Using the MP-DPD with the reduced number of coefficients (27), the Doherty power amplifier achieved 42.4% drain efficiency, with an average output power of 86.1 Watts. To achieve similar linearity without the use of such a DPD, the input power to the PA had to be reduced by 8 dB. At this point, the PA only achieved 17.0% efficiency with 12.74 Watt output power. Hence, the use of the odd only MP-DPD allows us to operate the DPA with over 25% better efficiency.

3.5 Comparison of Measured and Simulated Two Tone Testing Results

While one can compensate for the memory effects with MP-DPD, when the DPA is driven with wideband input signals such as four carriers WCDMA, the complexity of the DPD required is quite high, even with the aforementioned techniques. This complexity is required due to the strong memory effects in the design. Hence, it becomes desirable to minimize the memory effects exhibited by the DPA at the design level. This will enable the use of the DPA without a DPD in single carrier applications and reduce the overall complexity of the DPD required to meet spectral mask requirements for multi-carrier applications.

Before beginning to minimize the memory effects in the DPA, one must examine how they can be quantified at the design phase. As a first step, the accuracy of the prediction of the memory effects in simulation will be examined. If the memory effects can be quantified and predicted in simulation, then one can begin to minimize them at the design process level using a

design tool such as ADS. However, should the simulations fail to accurately predict the memory effects, measurements will be the only reliable design tool.

Figure 3.6 shows both the IMD 3 results from ADS simulations as well as measurements. Clearly there is a large discrepancy between the results as the simulations fail to accurately predict not only the correct levels of the IMD 3 products, it also does not come close to predicting the trends of the left and right IMD 3 products. While the left and right IMD 3 products diverge only slightly in simulation, they diverge significantly in measurement.

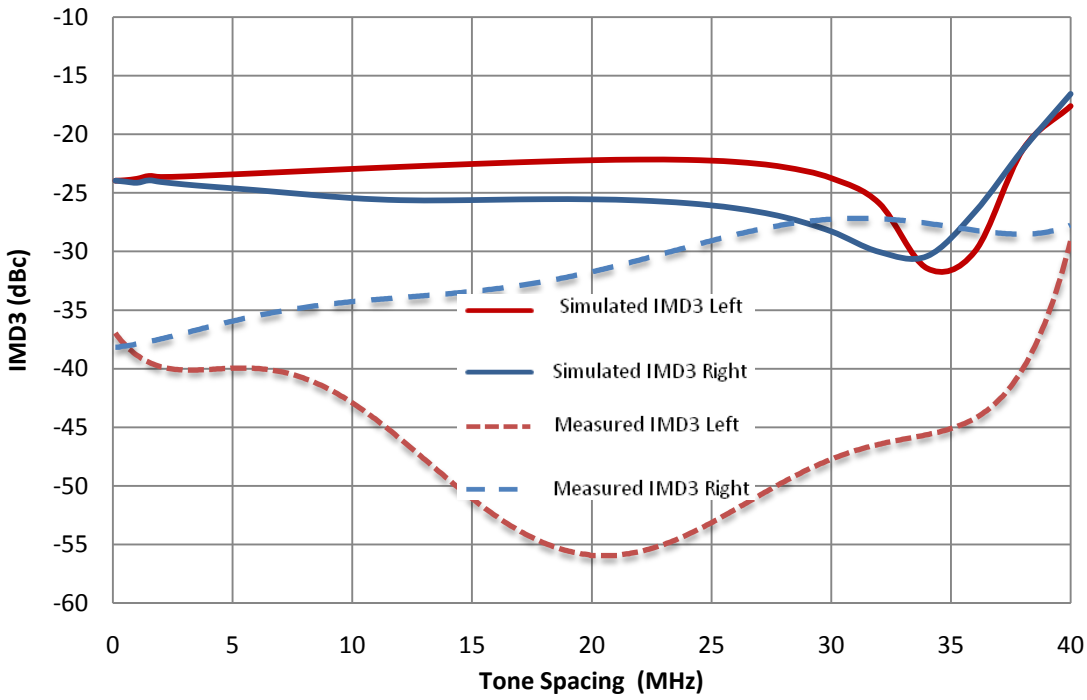


Figure 3.7: Simulated and Measured IMD3 Levels vs Tone Spacing

To eliminate the memory effects when the DPA is driven with extremely wideband signals such as 4C WCDMA, the IMD3 products will need to be relatively similar and constant. Clearly, the measured IMD 3 results of the DPA indicate that it has strong memory effects. Furthermore, the disparity between the measured and simulated results is significant. This indicates that the ADS transistor model is not capable of accurately predicting the behavior of the DPA accurately. This may be due to the active load modulation that the DPA structure uses. Another possible reason is that transistor models are notoriously bad at predicting Class C behavior, so the peaking amplifier in the DPA may also be causing the failure of the simulator to

accurately predict the DPA's behavior. To eliminate these possible sources of discrepancy between the predicted and measured PA behavior, as well as to better determine the source of the memory effects in the PA, a single branch class AB PA will need to be constructed.

Chapter 4:

Design and Validation of a Class AB Power Amplifier

In this chapter, the design of a single branch class AB PA is presented. First Agilent Advanced Design System (ADS) load-pull simulations are used to find the ideal input and output impedances for the transistor. The impedances obtained from the load-pull simulations are then used to design the input and output matching networks. The complete PA is then optimized in ADS and the layout is finalized. The final design is simulated to provide an estimate of the behavior of the predicted design.

4.1 Design of the Power Amplifier

Before fabrication, the class AB PA will be designed in ADS. This will allow a greater understanding of how the parameters in the matching networks affect the performance of the PA. For this PA, the MRF7S21170 transistor (the same transistor used in the previous chapter's DPA) was selected as it can provide the desired average output power (47 dBm) at the desired frequency of 2.14 GHz. Since an accurate model for the transistor has been developed by the manufacturer, Freescale, additional load-pull measurements to characterize the transistor were not necessary. This meant that the first design step was to perform ADS simulations to identify the optimal input and output impedances. The quiescent current of the transistor was set to 1.4 A so as to ensure the class AB operating mode specified in [25].

4.1.1 Source-Load-Pull Simulations

Source-Load-Pull simulation consists of using an impedance synthesizer to sweep the input and output impedance presented to the transistor. To ensure accurate results, the bias network should be included in the simulation as it will affect the optimal impedance. The DC blocking capacitors however should be omitted and ideal DC blocks should be used, because these capacitors are typically placed in the matching networks and will have a significant effect on impedance matching.

Since sweeping both the source and load impedance concurrently would create an impossibly large amount of data to interpret, load-pull simulations are done iteratively. Typically, the load impedance is swept while the source impedance is kept constant. Once the

optimal load impedance is located, the output impedance presented to the transistor is fixed at this point and the source impedance is swept. This process is repeated until the optimal source and load impedances converge. The ADS design used to perform the load-pull simulation is shown in Figure 3.1, where X16 and X19 represent the input and output bias networks respectively.

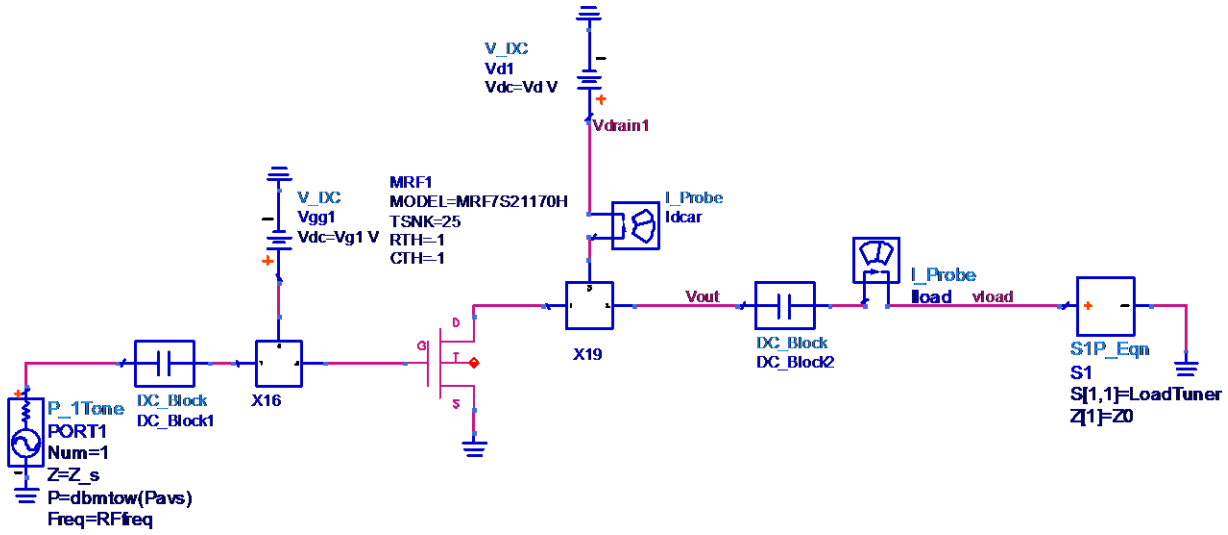


Figure 4.1: ADS Load Pull Simulation Schematic

The DC power can be calculated by measuring the drain voltage and current. Similarly, the output power is measured through probing the load current and voltage at the fundamental. This in turn allows the Power Added Efficiency (PAE) and gain to be calculated for each synthesized impedance. The optimal impedances for this PA were chosen to provide a PAE over 50% with at least 16 dB of gain at peak power. Using the impedances obtained from the source-load-pull, the input and output matching networks can be designed. The obtained optimal source impedance is $17.66 - 4.16j$ and the optimal load impedance is $1.42 - 4.16j$. This allowed the amplifier to achieve a peak PAE of 50.2% while generating 52.71 dBm of output power.

4.1.2 Input and Output Matching Network Design

A multi-section transformer architecture was chosen for the input and output matching networks to minimize their insertion loss and surface area. Figures 4.2 and 4.3 illustrate the schematic of the input matching network and its response simulated S parameter response, where

Z_o, the characteristic impedance of the Smith chart is 50 ohms. One can see that the input matching network achieves the desired optimal load impedance obtained through source-pull simulations. The dimensions for the transmission lines used in the input matching network are shown in Table 4-1.

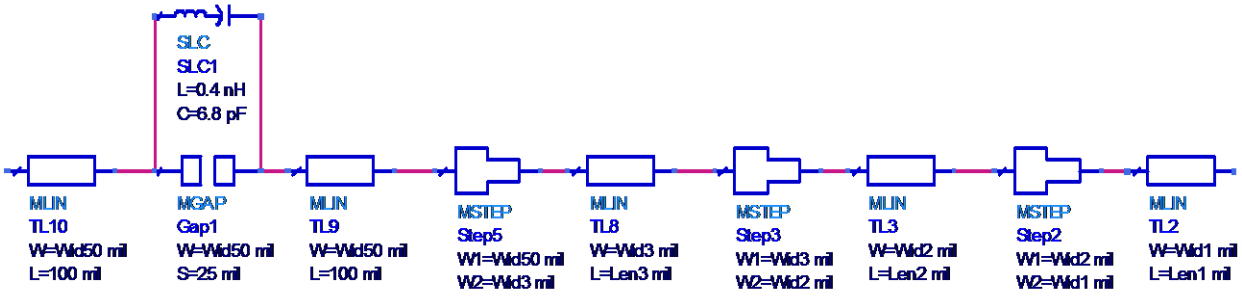


Figure 4.2: ADS Schematic of the Input Matching Network

TABLE 4-1: INPUT MATCHING NETWORK DIMENSIONS

	Wid50 (mil)	Wid3 (mil)	Wid2 (mil)	Wid1 (mil)	Len3 (mil)	Len2 (mil)	Len1 (mil)
Value	42.7	57	68	668.5	368	616	86

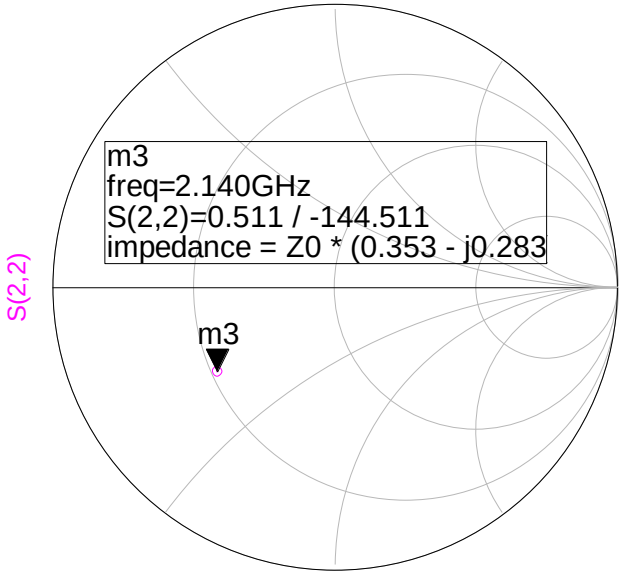


Figure 4.3: Simulated Response of the Input Matching Network

Similarly, figures 4.4 and 4.5 illustrate the schematic of the output matching network and its response simulated S parameter response, where Z_o is 50 ohms. One can see that the output

matching network also achieves the desired optimal load impedance obtained through load-pull simulations. The dimensions for the transmission lines used in the output matching network are shown in Table 4-2

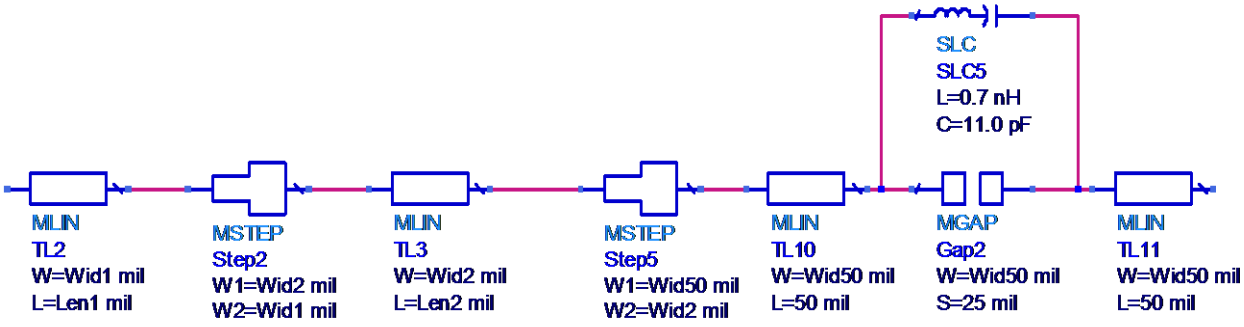


Figure 4.4: ADS Schematic of the Output Matching Network

TABLE 4-2: OUTPUT MATCHING NETWORK DIMENSIONS

	Wid50 (mil)	Wid2 (mil)	Wid1 (mil)	Len2 (mil)	Len1 (mil)
Value	42.7	236	1045	398	99

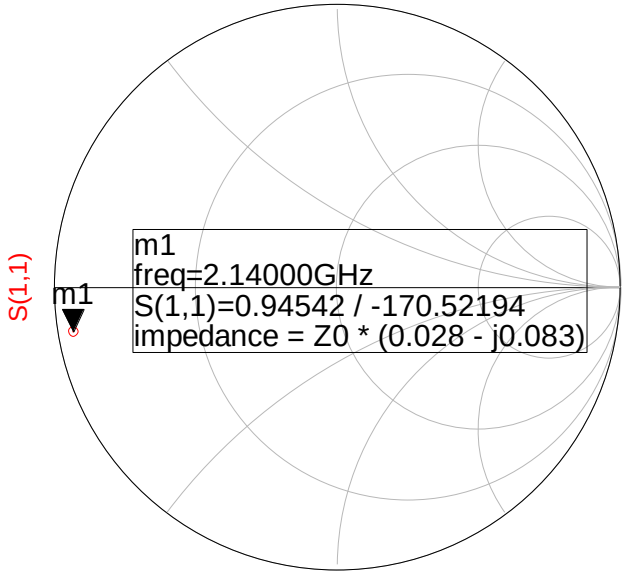


Figure 4.5: Simulated Response of the Output Matching Network

4.1.3 Class AB Power Amplifier Design and Simulation

Combining the input and output matching networks with the transistor in Agilent ADS, a single tone Harmonic Balance (HB) simulation was performed at the intended frequency of operation, 2.14 GHz, while the input power was swept. The PA was then tuned to optimize Input

Return Loss (IRL), gain and PAE. Figure 4.6 shows the ADS schematic of the simulated design. Component X16 contains the input matching network and the gate bias circuit, while X19 contains the output matching network and the drain bias circuit.

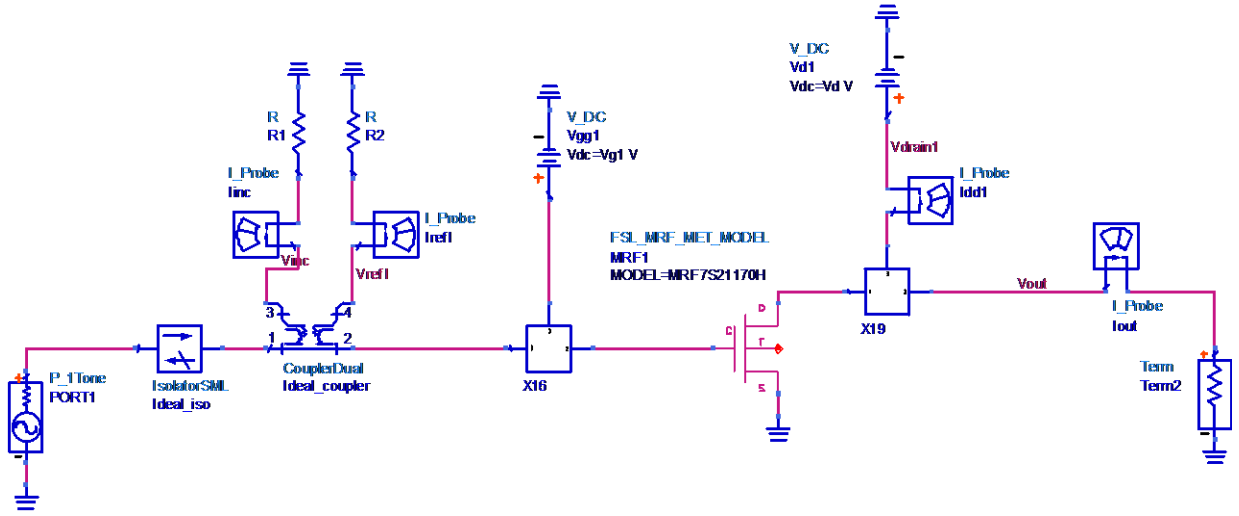


Figure 4.6: ADS Schematic of the Designed Class AB PA

The simulation results illustrating these figures of merit are shown in Figures 4.7 to 4.9 as a function of the output power of the PA. The PA achieves a PAE of 50.68%, a gain of 16.46 dB and a good input matching (IRL = -15.92 dB) at an output power 52.461 dBm. These values are in agreement with the performance benchmarks detailed in [25].

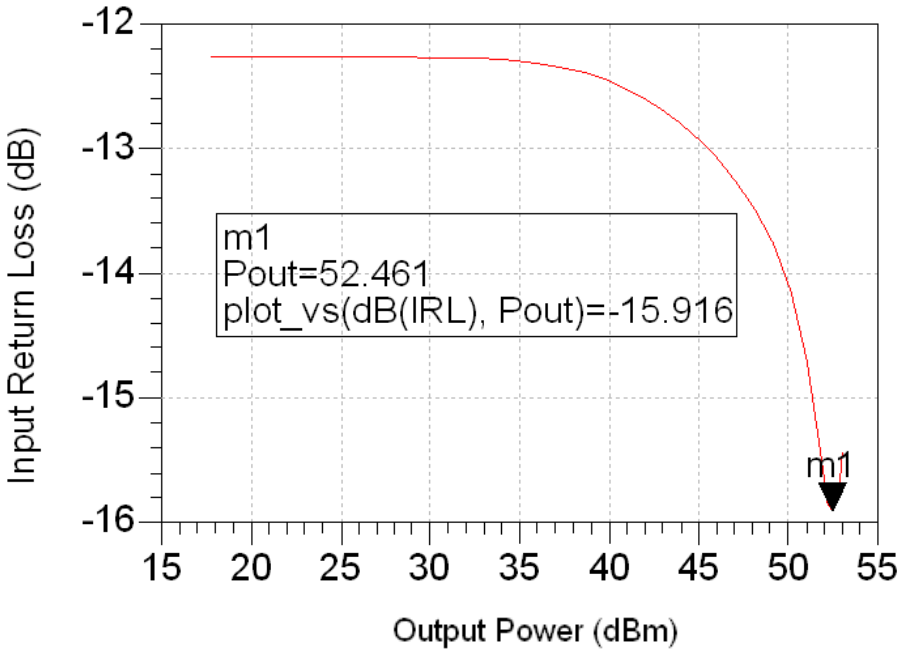


Figure 4.7: Simulated IRL of the PA as a Function of the Output Power

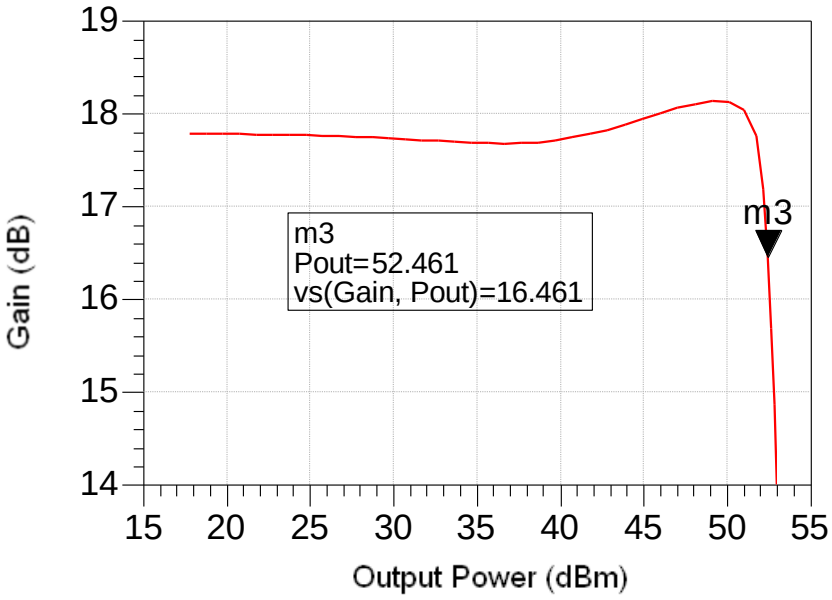


Figure 4.8: Simulated Gain of the PA as a Function of the Output Power

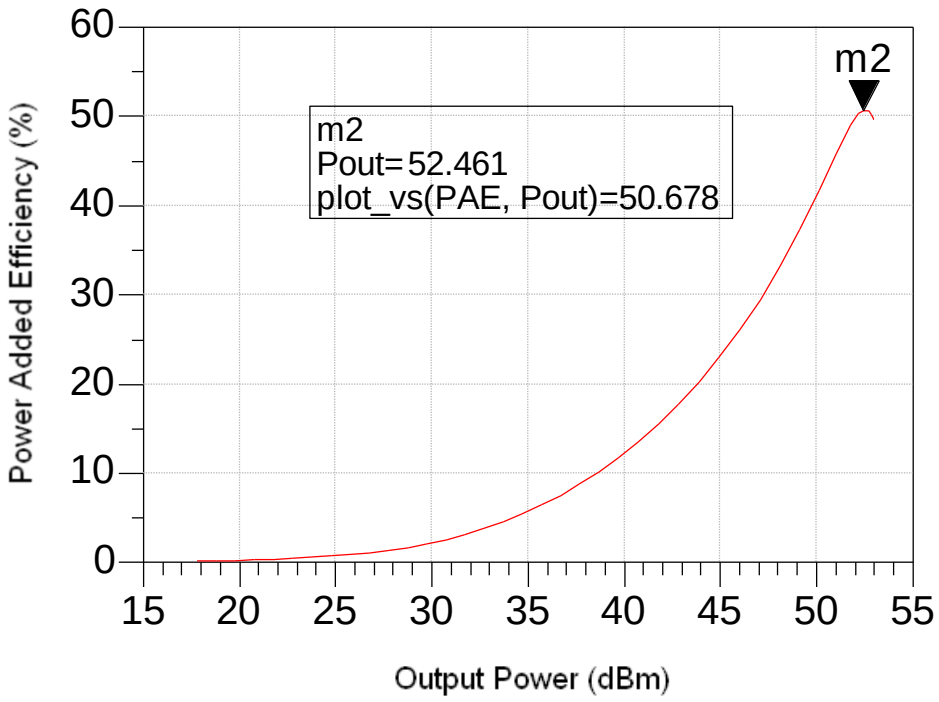
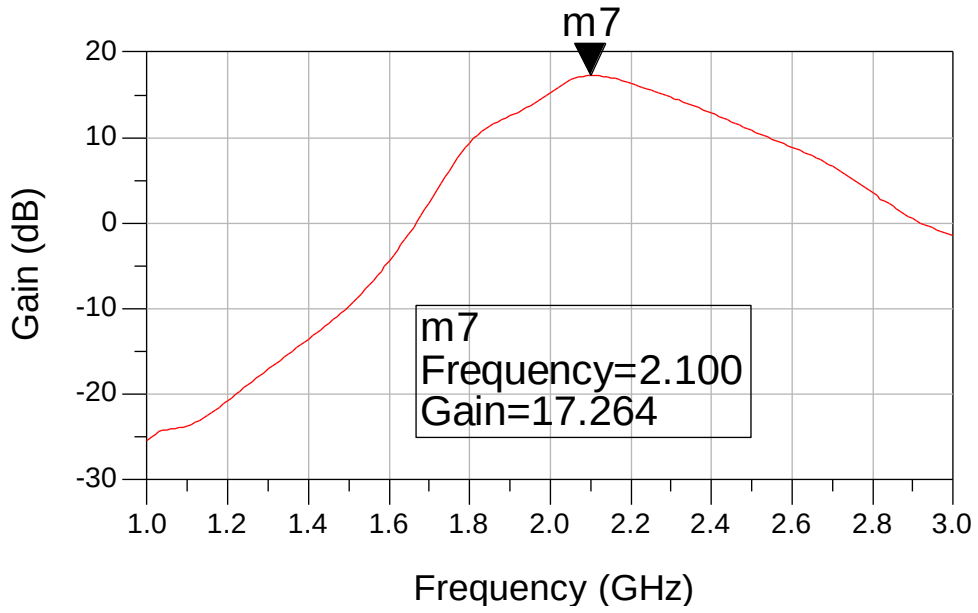
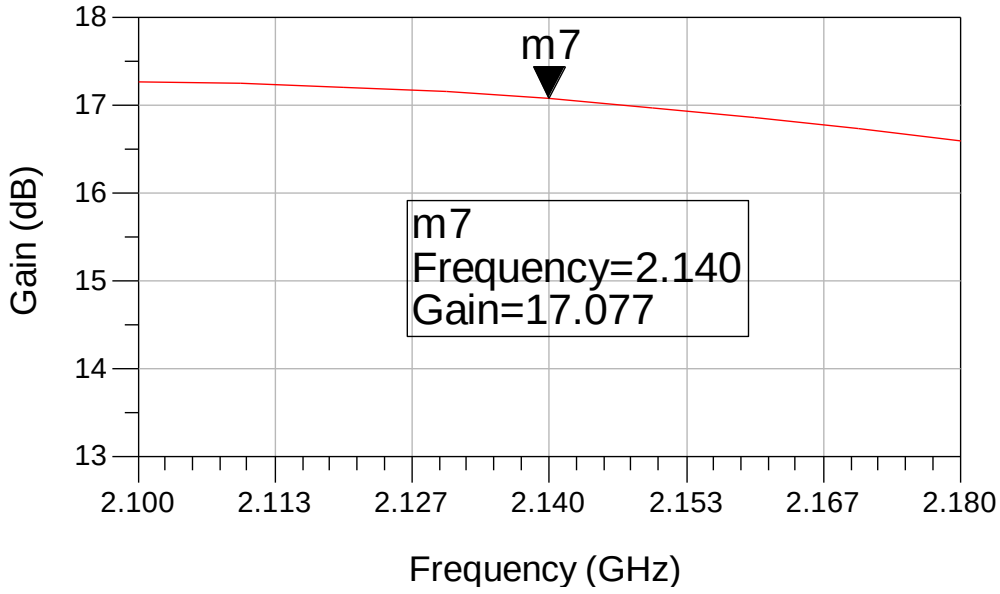


Figure 4.9: Simulated PAE of the PA as a Function of the Output Power

Further simulation was performed to ensure that the PA would have the expected BW detailed in the MRFS21170 data sheet [25]. For this, the input power of the PA was held constant while the frequency of the RF input was swept. Figures 3.10 and 3.11 show the gain and the IRL of the PA as a function of the RF input frequency respectively. One can see that gain does vary by about 0.6 dB and the IRL does not exceed -10 dB over an 80 MHz range.

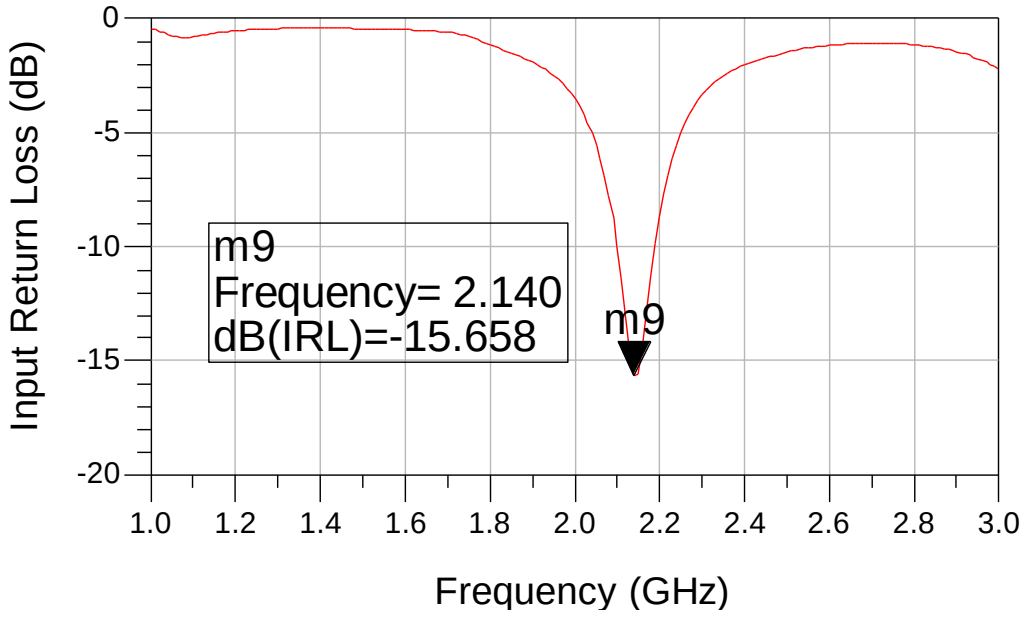


(a)

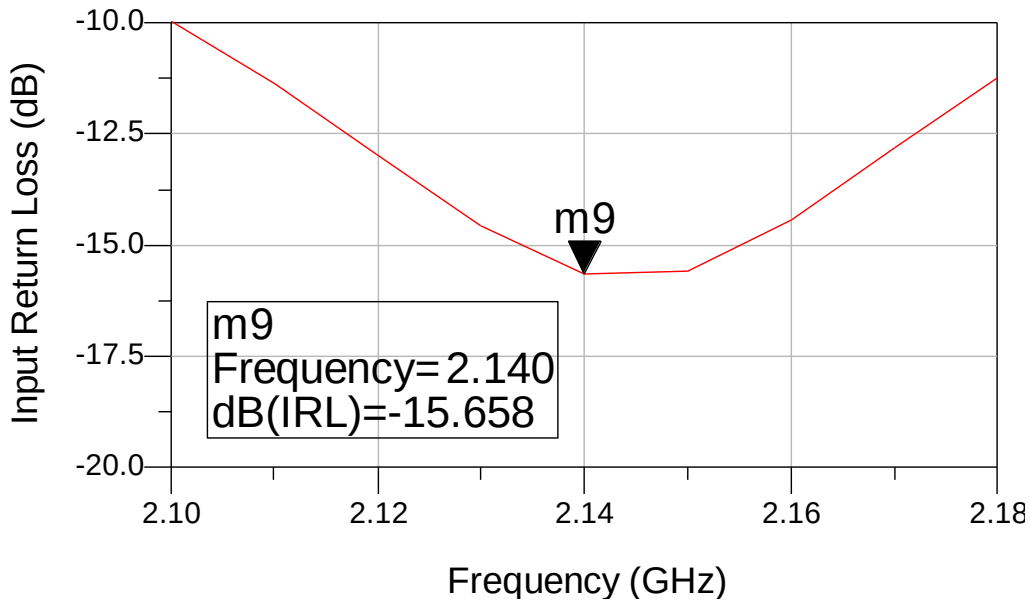


(b)

Figure 4.10: Simulated Gain of the PA as a Function of the RF Input Frequency: Between 1 and 3 GHz (a), and Centered on the Frequency of Interest (b)



(a)



(b)

Figure 4.11: Simulated IRL of the PA in dB as a Function of the RF Input Frequency: Between 1 and 3 GHz (a), and Centered on the Frequency of Interest (b)

4.2 Class AB Power Amplifier Layout and Fabrication

The substrate chosen for the PA was the RF-35 substrate from Taconic. This substrate was chosen as it offers a very high thermal reliability and an exceptionally low dissipation factor, which make it a great choice for high power base station applications.

ADS was used to convert the schematic to a micro-strip layout. A ground pad was added in the upper right corner. For the purpose of tuning, ground pads were added parallel to the input and output matching network. Mounting holes and alignment holes were also added at this point. Figure 3.12 shows the layout submitted for fabrication.

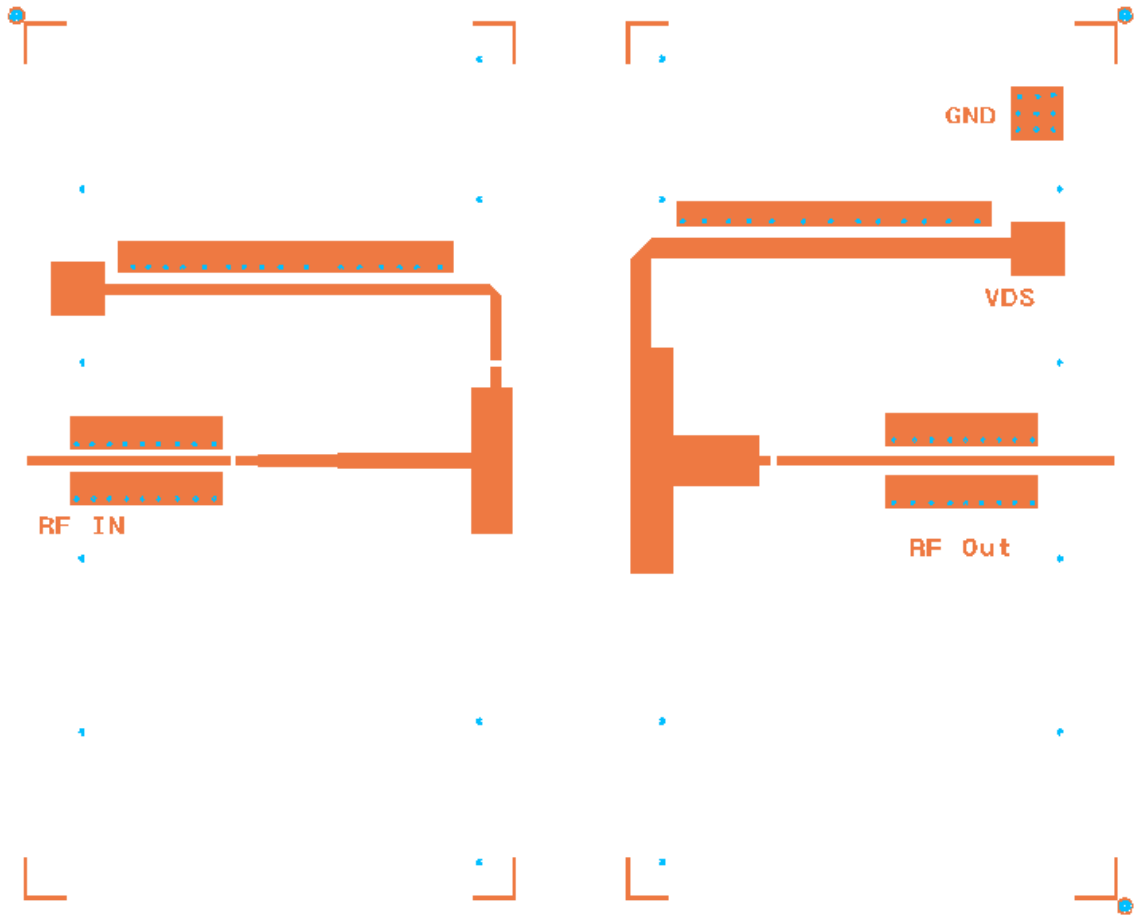


Figure 4.12: Layout of the Fabricated Class AB PA

The resulting PCB was then populated and mounted to a custom copper fixture. Figure 3.13 shows the fabricated Class AB PA.

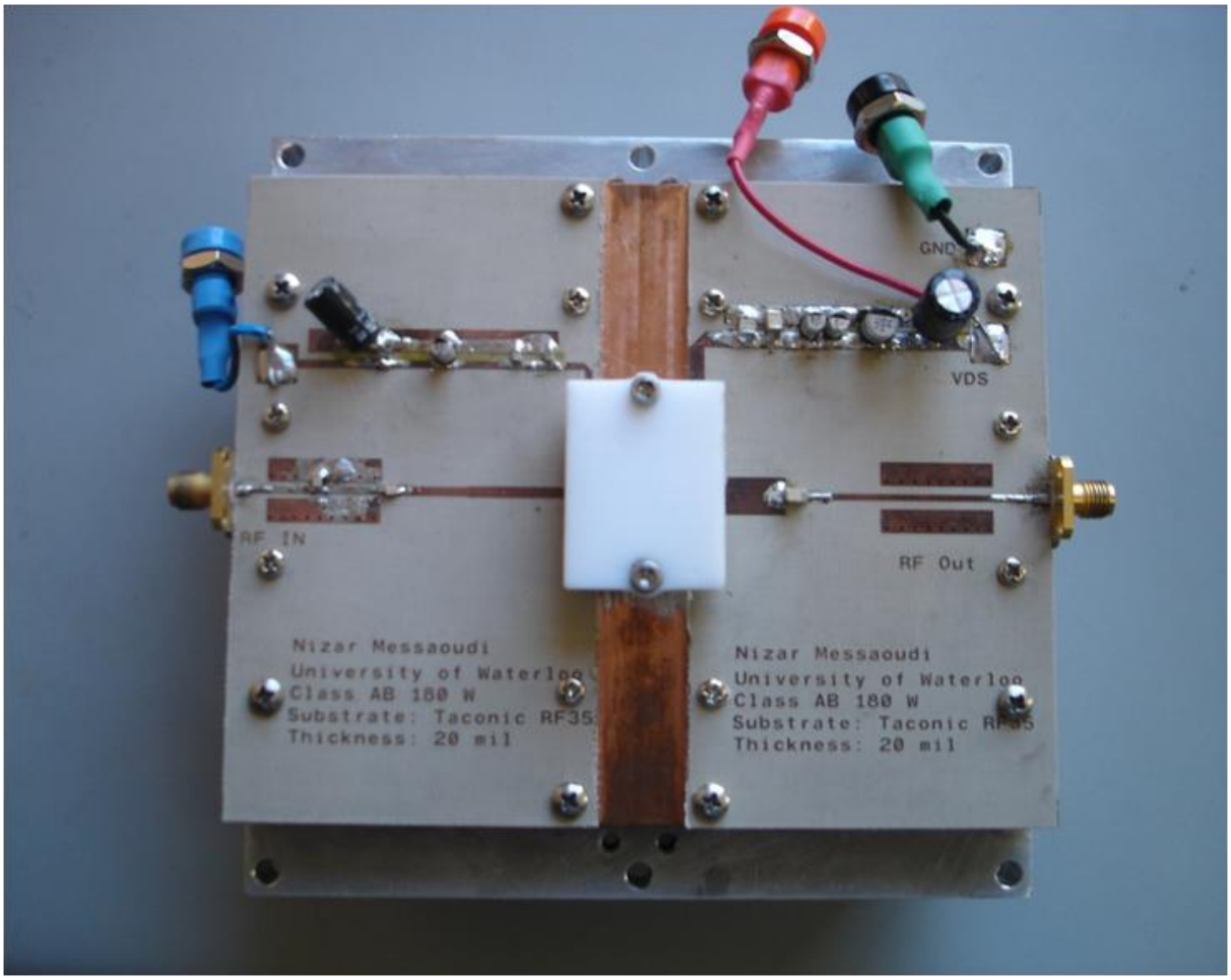


Figure 4.13: Fabricated Class AB PA

4.3 Class AB Power Amplifier Validation under CW Signal

The S parameters of the fabricated amplifier were measured to see if they corresponded with the values obtained in simulation. To ensure that the Vector Network Analyzer (VNA) used was protected, attenuators were used to ensure that the power at the input of the VNA never exceeded safe values. The S parameters were measured using a 0 dBm input signal. Figure 4.14 shows the experimental setup used to measure the PAs S parameters as a function of frequency.

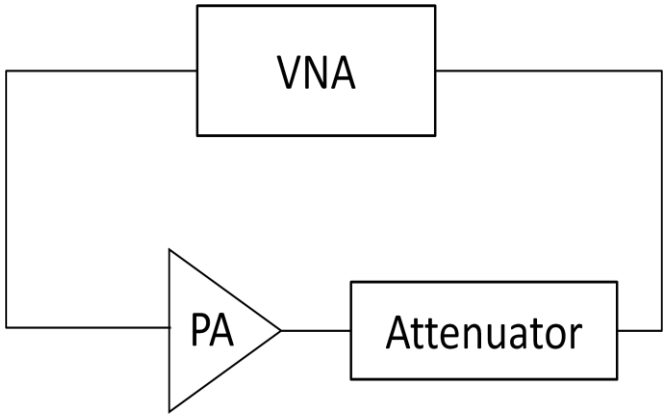


Figure 4.14: Setup Used to Measure the Small Signal Parameters of the Class AB PA

Initially the input matching network of the PA was detuned. However, with the addition of a shunt capacitor we were able to obtain the desired S11 or IRL. Figure 4.15 shows the S11 of the PA after the addition of the shunt capacitor in the input matching network.

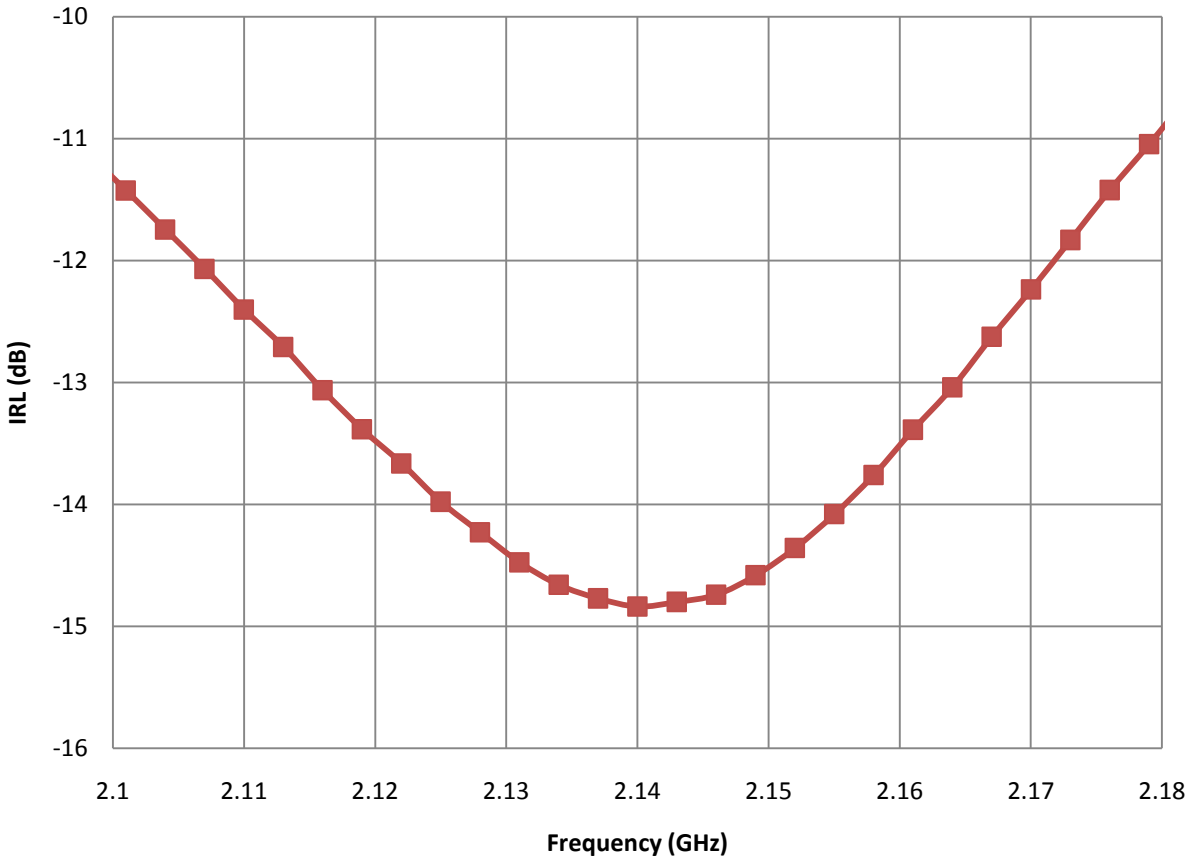


Figure 4.15: IRL of the Class AB PA as a Function of Input Frequency

Once the desired IRL was achieved, the power gain of the transistor was measured. Figure 4.16 shows the gain of the PA as a function of input signal frequency. While the gain is slightly higher than expected, it varies less than 0.5 dB over an 80 MHz BW.

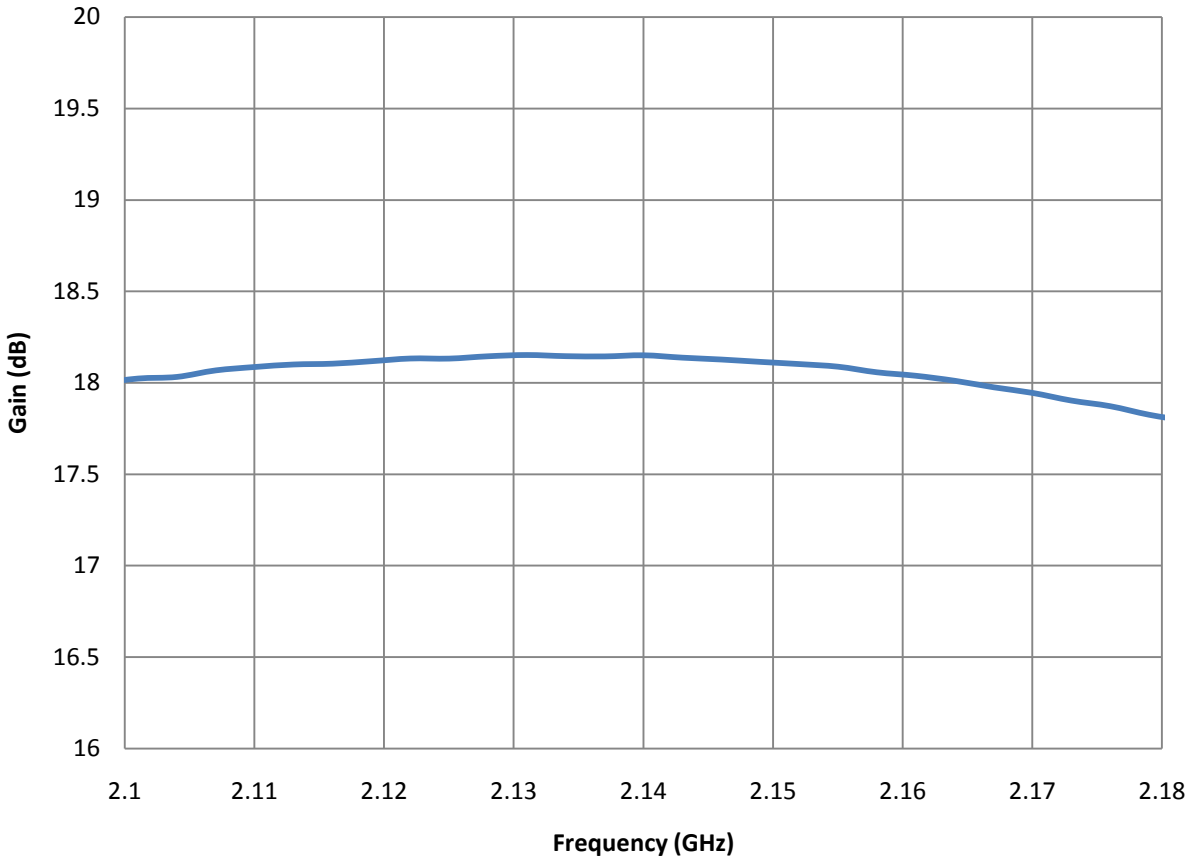


Figure 4.16: Gain of the Class AB PA as a Function of Input Frequency

Figure 4.17 shows the phase of the gain of the PA as a function of input signal frequency. The gain phase is linear with frequency, indicating that at this power level the device is linear.

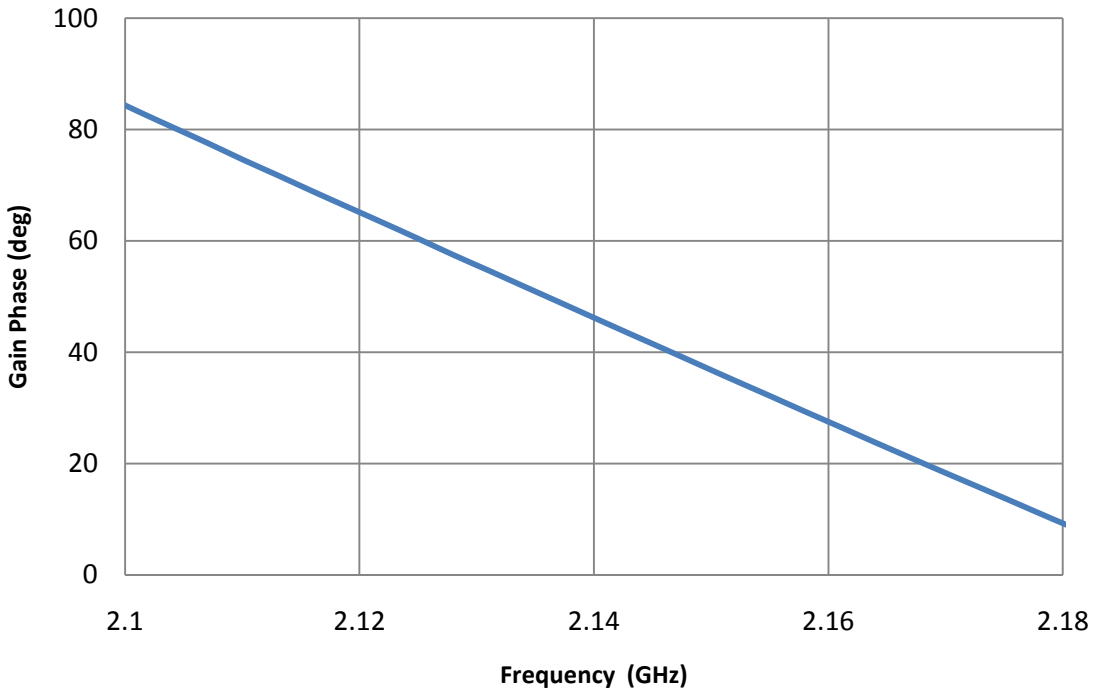


Figure 4.17 Gain Phase of the Class AB PA as a Function of Input Frequency

To measure the performance of the PA at higher input power levels, a driver PA must be used. The setup to measure the gain of the PA at higher input power levels is shown in Figure 4.18.

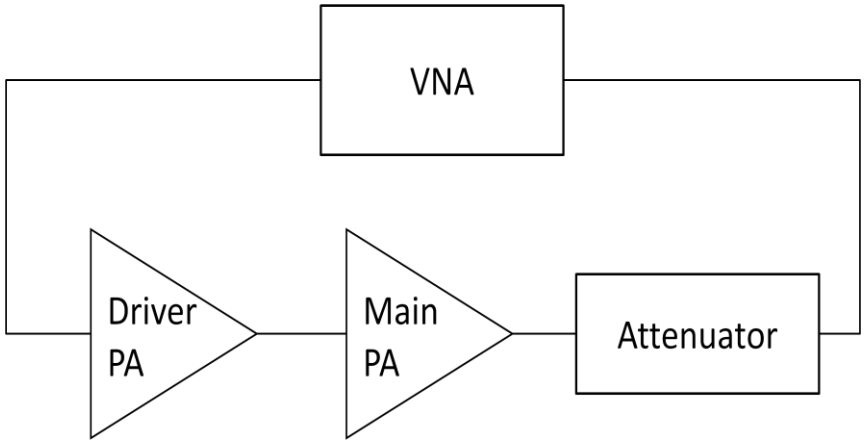


Figure 4.18 Setup Used to Measure the Gain Compression of the Class AB PA

Since the driver is connected to port 1 of the VNA, it is impossible to measure the IRL of the PA at higher power levels. However this setup is the only way to measure the gain accurately

at higher power levels, which is crucial for determining the 1 dB compression point of the PA. Figure 4.19 illustrates the gain of the PA as a function of input power at 2.14 GHz. The 1 dB compression point of the PA is 33.2 dBm.

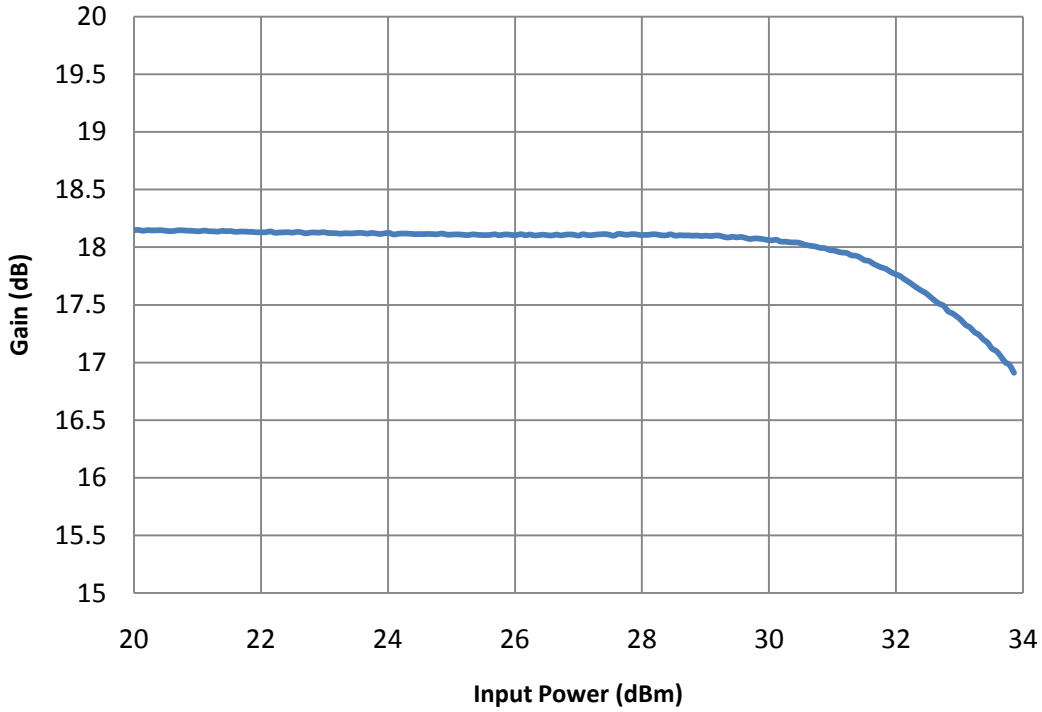


Figure 4.19: Gain of the Class AB PA as a Function of Input Power

4.4 Memory Effect Investigation

Now that the PA has been validated using CW stimulus, further testing using modulated input signals is necessary. As a first step we will begin by performing two-tone testing to measure the IMD3 and IMD5 levels of the PA as a function of tone spacing. As highlighted in Section 1.3.2, this test is a good indicator of the strength of the nonlinearity of the PA and the existence of memory effects.

4.4.1 Two Tone Measurements

The experimental setup used to test the PA is illustrated in Figure 4.20. To ensure a clean two tone signal was input to the PA, two signal sources and a combiner were used. A driver PA was necessary as the output signal of the signal sources deteriorates significantly in quality near

its peak output power. To ensure that the driver was not affecting our measurements, two-tone tests were performed on the driver.

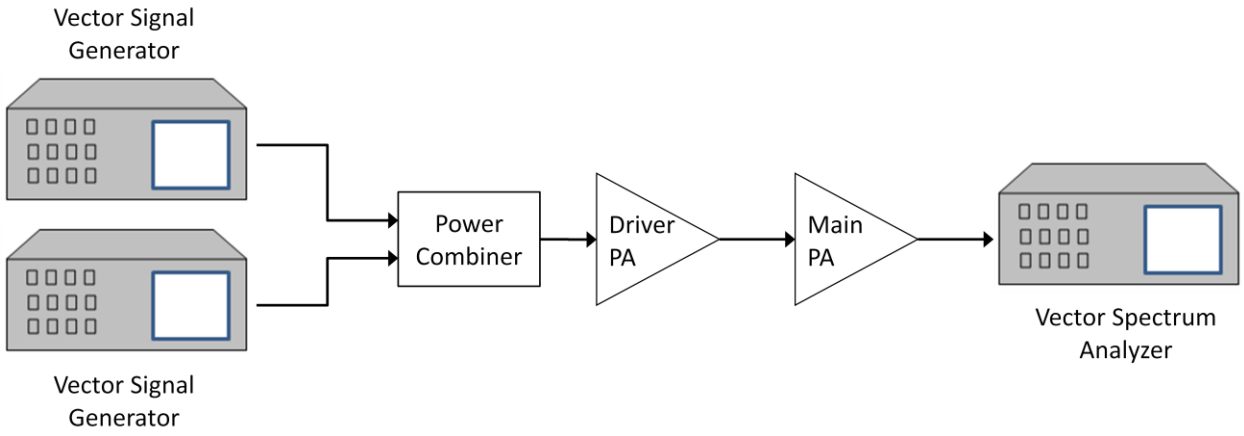


Figure 4.20: Experimental setup used for two tone testing

The measured IMD3 of the driver is shown in Figure 4.21. The lack of any significant intermod products indicates that the driver is extremely linear. Furthermore, since the left and right IMD products are identical and are almost independent of the tone spacing, the driver does not exhibit any memory effects.

Figure 4.22 shows the measured IMD3 of the designed class AB PA. The high level of IMD distortion indicates that the PA is quite nonlinear. Furthermore, while the left and right IMD3 products do not differ greatly (about 1 dB at the most over the 40 MHz tested), there is a strong correlation between the IMD3 levels and the frequency spacing (greater than 10 dB over the 40 MHz span). This indicates that there are strong memory effects in the PA.

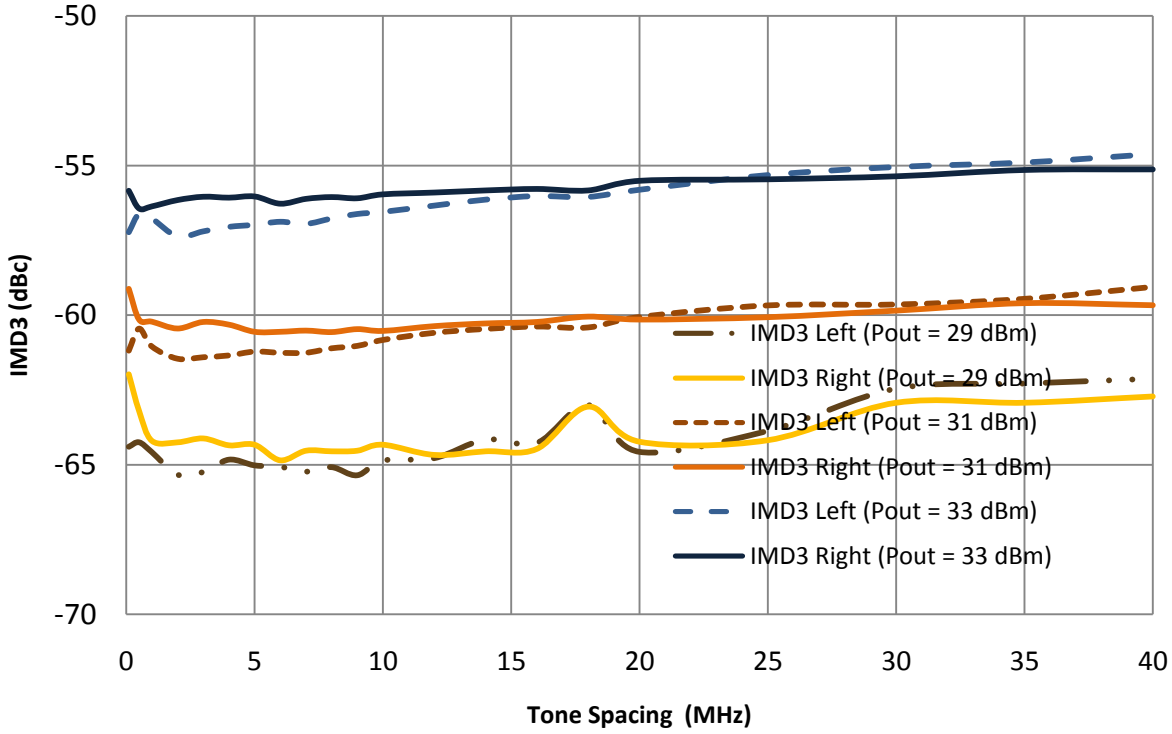


Figure 4.21: Measured IMD3 of the Driver PA as a Function of Tone Sspacing

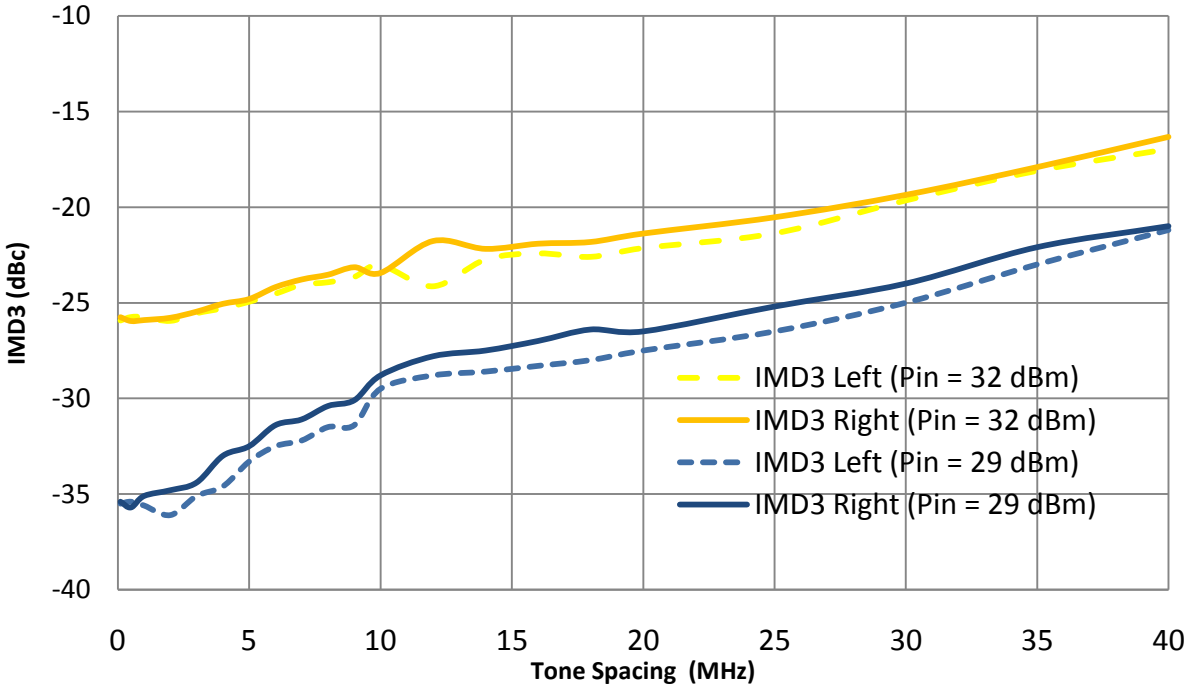


Figure 4.22: Measured IMD3 of the Class AB PA as a Function of Tone Spacing

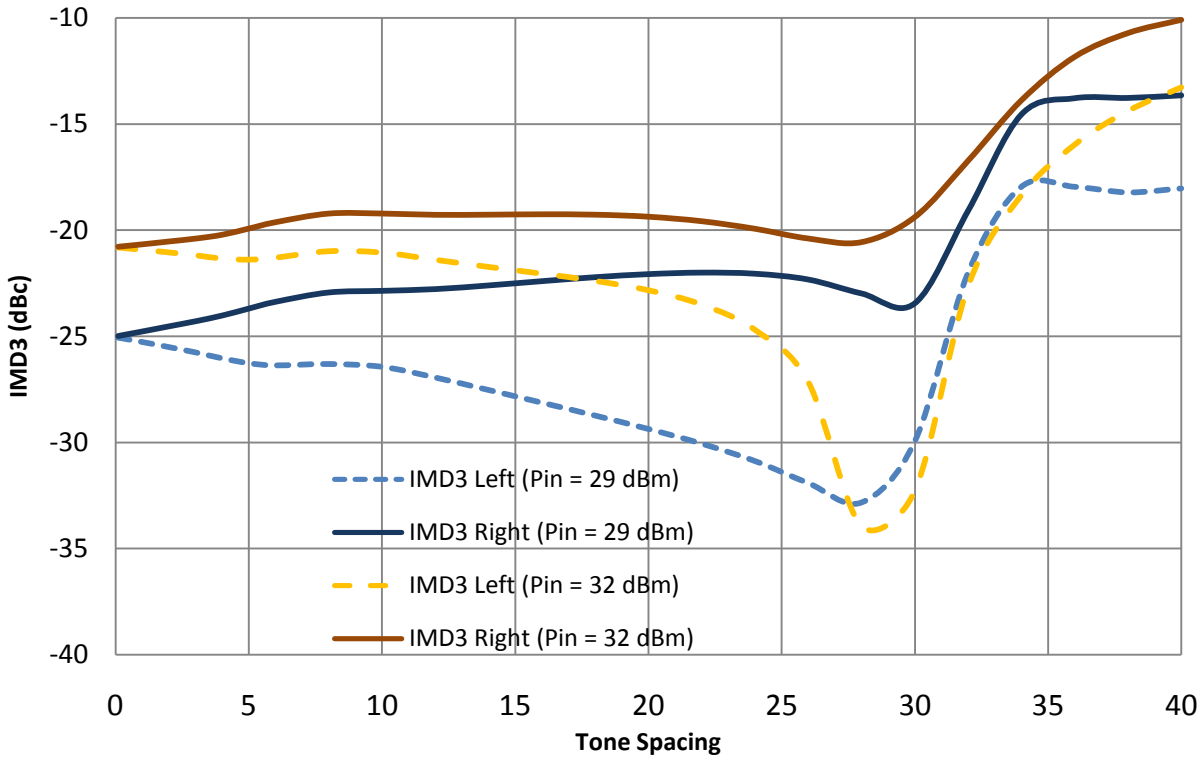


Figure 4.23: Simulated IMD3 of the Class AB PA as a Function of Tone Spacing

Figure 4.23 shows the simulated IMD3 of the designed class AB PA. These simulated results vary greatly from the measurements, with large variations between the left and right IMD3 product and a strong variation of the IMD3 levels of the PA with the tone spacing used. This deviation indicates that the discrepancies reported in the previous chapter between the measured and simulated IMD3 levels of the DPA is not due to the Doherty structure, but rather the result of poor device modeling. Therefore, the memory effects will not be well predicted, and hence impossible to reduce the memory effects in the design stage for this particular device using the current model.

4.4.2 Modulated Signal Testing

After the PA was tested using a two tone signal, a single carrier WCDMA signal was used to test the same lineup. The IMD3 results seem to indicate that the PA is not memoryless and modulated signal testing confirmed this result as shown in Figure 4.24.

When a memoryless 12^{th} order polynomial predistorter was applied to the input signal, the ACPR was still quite significant, as shown in Figure 4.24, indicating that the PA does indeed

have memory effects. The use of two and three branch memory polynomials of 12th order predistorters show significant improvement in the ACPR of the PA.

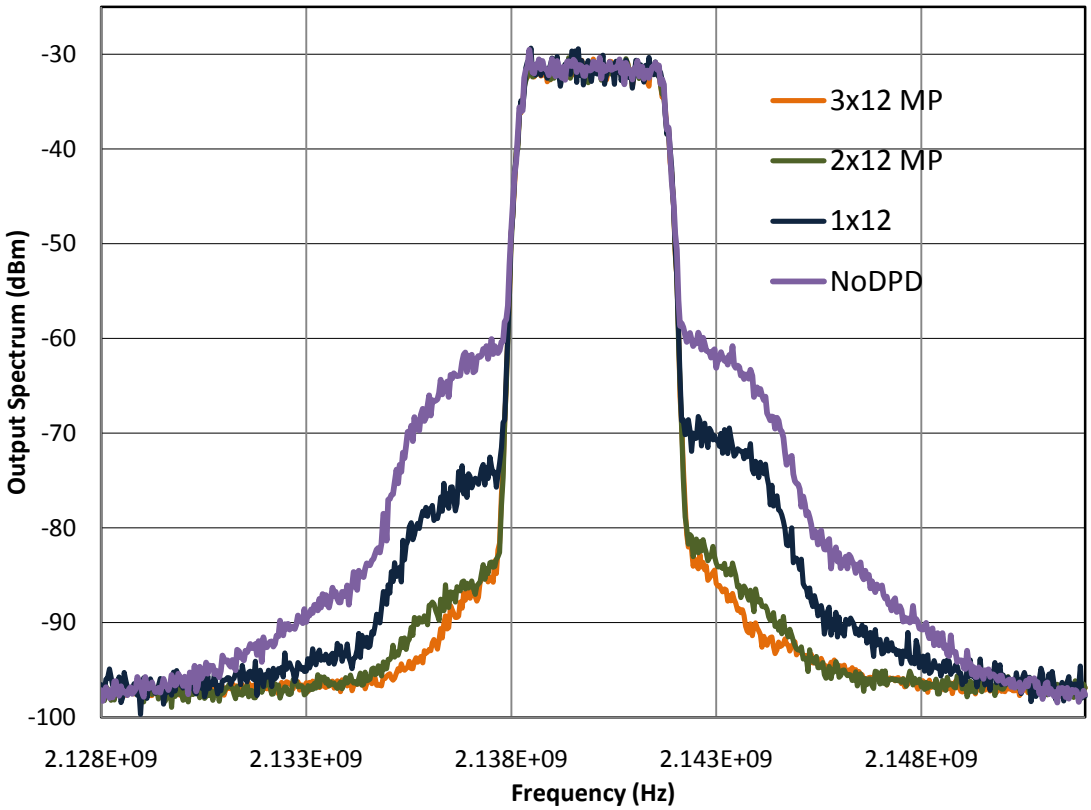


Figure 4.24: Frequency Spectrum of the PA Output with the Use of Various Predistorters

The ACPR of the PA output using the different DPDs is shown Table 4-3. The ACPR drops by around 10 dBc when going from the memoryless DPD to the use of 2 branches. The addition of a third branch further improved the ACPR by another 1.5 dB.

TABLE 4-3: SINGLE CARRIER WCDMA LINEARIZATION

	ACPR (dBc)					
	5 MHz Offset		10 MHz Offset		15 MHz Offset	
1x12	-48.13	-45.92	-65.77	-64.26	-65.85	-63.89
2x12	-57.68	-56.51	-64.54	-64.03	-65.12	-64.74
3x12	-58.79	-58.91	-64.15	-63.88	-65.3	-65.15

Conclusion

Over the course of this work, the antagonistic demands for power amplifier linearity and drain efficiency were explored. First, the tradeoff between these two figures of merit in single branch amplifiers was demonstrated. The Doherty PA structure was proposed as a structure that could achieve a strong efficiency enhancement over the dynamic range required by modern communication schemes. Next, the various methods of evaluating PA linearity (single tone, two tone and modulated signal testing) and the metrics used were reviewed. Subsequently, several linearization techniques, such as feedback, feedforward and predistortion were reviewed and compared. As a result, baseband digital predistortion was chosen as the most promising solution to improve the linearity of the Doherty PA while maintaining its strong average efficiency.

Chapter 2 explored the origin of memory effects within the PA. First, a memoryless behavioural model was developed. This model predicted the independence of the magnitude of the spectral components of the output with the frequency spacing of a two tone input. Memory effects were then separated into two categories: thermal memory effects and electrical memory effects. Since thermal memory effects are an intrinsic property of the transistor, there is little that can be done to minimize them. The focus then shifted to electrical memory effects and a mathematical formulation of all of the harmonic components using a simple 5^{th} order polynomial model that could affect the in band harmonics was developed. Finally the importance of the biasing network in the reduction of memory effects was highlighted.

In the third chapter, the various models used for PA digital predistortion were compared. A solution to the antagonistic demands for high power efficiency and good linearity in high power microwave amplifiers through the use of the Doherty power amplifier combined with memory polynomial digital predistortion was demonstrated. The use of the MP-DPD allowed for the PA to operate at over 40% average efficiency and produce over 86 Watts of output power while maintaining 50 dBc ACPR, using a 4 carrier WCDMA with 8.3 dB PAPR. To reduce the complexity of the DPD used and reduce the computational complexity required for the DPD, odd order only and uneven branches techniques were used. This allowed the number of coefficients required by the MP DPD to be reduced by 64% and the computational complexity of calculating the coefficients to be reduced by a factor of 19. Furthermore, the importance of the 5^{th} order

intermod products in memory effects was demonstrated. However, the memory effects in the DPA were significant and poorly predicted in simulation.

In an effort to better understand the source of the discrepancy between the memory effects predicted in the DPA through simulation and those observed in measurement, a single branch class AB PA using the same transistor as the DPA was designed and fabricated. Two tone testing revealed similar discrepancies between predicted memory effects and those observed through measurement. This indicated that the Doherty structure was not the cause of the difference between the measured and simulated results. Rather, this discrepancy is due to poor device modeling, rendering the reduction of memory effects at the design stage impossible with this device using two tone testing. Modulated signal testing confirmed the presence of significant memory effects in the PA.

There are many avenues in which this work may be continued. One could attempt to construct more accurate device models using two-tone stimulus combined with source-load-pull in order to more accurately predict the device behavior when driven with wideband signals. Other technologies such as Gallium Nitiride should be explored to see if there a correlation between device technology and the depth of memory effects in a PA. Finally, while there has been some work on memory effect reduction and linearity enhancement by adjusting the drain bias of the PA, there is no work that the author is aware of that does so systematically. A theory based methodology to tackle this problem would avoid the arbitrary trial and error approach that seems to be commonplace with this problem.

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