Nano-Crystalline &Amorphous Silicon PhotoTransistor Performance Analysis

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

In this thesis, we compared electrical performance and stability of a novel nanocrystalline Si (nc-Si) thin film phototransistor (TFT) phototransistor and a regular amorphous silicon (a-Si:H) TFT phototransistor for large area imaging applications. The electrical performance parameters of nc-Si TFT phototransistor were extracted from the electrical (current-voltage) testing in dark and under illumination. The field-effect mobility is found to be around 1.2 $cm^2V^{-1}s^{-1}$, the threshold voltage around 3.9V and the sub-threshold voltage slope around 0.47V/Dec. Optical properties of nc-Si TFT phototransistor have been evaluated under the green light illumination in the range of 10^{14} – 10^{17} lum, and the photocurrent gain and the external quantum efficiency were extracted from the experimental results. By comparing the results with those for a-Si:H TFTs measured under the same conditions, we found that nc-Si TFT has higher photo current gain under low illumination intensity, 5×10^{14} to 7×10^{15} lum. This thesis shows the relations bewteen the photo current gain, the external quantum efficiency, TFT drain and TFT gate bias; the photo current gain and the external quantum efficiency can be controlled by the Vds and the Vgs.

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Chapter 1
Introduction

1.1 Application Areas for Phototransistor Array

Large area thin film phototransistor arrays have been developed since the 1990s, for such applications as flat-bed (line) scanners or large area imagers. A flat-bed scanner can scan a two-dimensional image by carrying out line scanning (Y direction) with a line sensor (such as a CCD line sensor), having pixels aligned in a linear pattern (X direction). However, the scanning speed is limited by the mechanical components for scanning a two-dimensional image, which makes it hard to reduce the scanner thickness and weight. Therefore, in order to reduce the scanner thickness and weight, and increase it's scanning speed, a matrix-type two-dimensional image sensor is an option. A two-dimensional photosensor is also suited as the data reader of a personal computer, word processor, or work station. This two-dimensional photosensor array requirements are a large area, a high sensitivity, and a rapid-response. Most of these requirements can be fulfilled by use of amorphous silicon (a-Si:H) and its alloys used in large-area applications such as backplane electronics for photodectors [1-4]. The high photoconductivity and fairly low cost of a large-area deposition setup have made the hydrogenated a-Si:H an attractive materials in large area photodetector research and industry [5, 6].

1.2 Problems for Thin Film Imaging Pixels

A typical photo imaging pixel(The Active Pixel Sensor(APS)) consists of a photodiode and several transistors. In thin film electronics, p-i-n photodiodes are used as sensing elements, and thin film transistors as switching elements, hence the process to fabricate this type of pixel will require two-process sequences: the transistors will be fabricated first followed by the photodiode fabrication. Therefore, the cost of the process for a photo pixel array is much higher than the cost of the process of a TFT array. Moreover, most foundries are built to manufacture TFT backplanes for the flat panel displays (where only n+ doped films are used for TFT source/drain contacts) and simply do not have p+ layer deposition capabilities essential for thin film p-i-n photodiode fabrication. Furthermore, the photosensitivity of a photodiode is hard to adjust just electrically by adjusting its operation point- a device layout change or fabrication process has to be adjusted for that. To reduce the process cost and simplify photosensitivity control, thin film phototransistor can be used as a photo-sensor that can be fabricated within the same process sequence as switching TFTs. However, the low field effect mobility (0.1-1 $cm^2V^{-1}s^{-1}$) and the low stability of the amorphous phototransistor have prevented the applications from being used in industry[7]. Hence the quest for the large area thin film phototransistors, which have higher mobility and stability.

1.3 Nanocrystalline silicon thin film phototransistor

In order to compensate for low field effect mobility and get sufficient drain current, the typical solution would be increasing the ratio of TFT Width to Length(W/L) ratio. With the fixed length, the width will increase, which means the TFT footprint will increase. The

mobility of an amorphous TFT is 0.1-1 $cm^2V^{-1}s^{-1}$[7]; whereas the mobility of a nano-crystalline TFT is 0.5 -3 $cm^2V^{-1}s^{-1}$[8, 9] and has potential to be further improved [8, 9]. Furthermore, the use of nanocrystalline silicon as TFT active layer reduces threshold voltage shift, hence increasing TFT stability[10] compared to a-si:H counterpart. Therefore, the use of nc-Si active layer leads to smaller footprint and stable photo-TFTs.

1.4 Goal of the Research

In order to verify our idea, two types of phototransistors have been fabricated. One type of devices was amorphous silicon thin film phototransistor fabricated based on a previously published result [11, 12]. In the other process, a nano-crystalline phototransistor was fabricated using the same layout as that of amorphous counterpart [13]. The electrical and optical performances of these two thin-film phototransistors were examined, such as the field effect mobility, stability, photosensitivity, total quantum efficiency and dynamic range.

Chapter 2
Background Study

2.1 Imaging Application

Figure 1 shows a typical APS image sensor block diagram. Even though it is using Complementary Metal Oxide Semiconductor (CMOS) technology, the large area thin film Active Pixel Sensors (APS) is using the same layout. APSs are sensors that implement a buffer per pixel. APS image devices include an array of pixel cells that convert light energy into electrical signals. Each pixel includes a photo-detector and one or more active transistors. The transistors usually provide amplification, readout control and reset control, in along with producing the electrical signal output from the cell. An APS imager includes a pixel array and a readout electronics. The area of the APS sensor, that might consume a good amount of the chip area, is where the signal is generated[14].

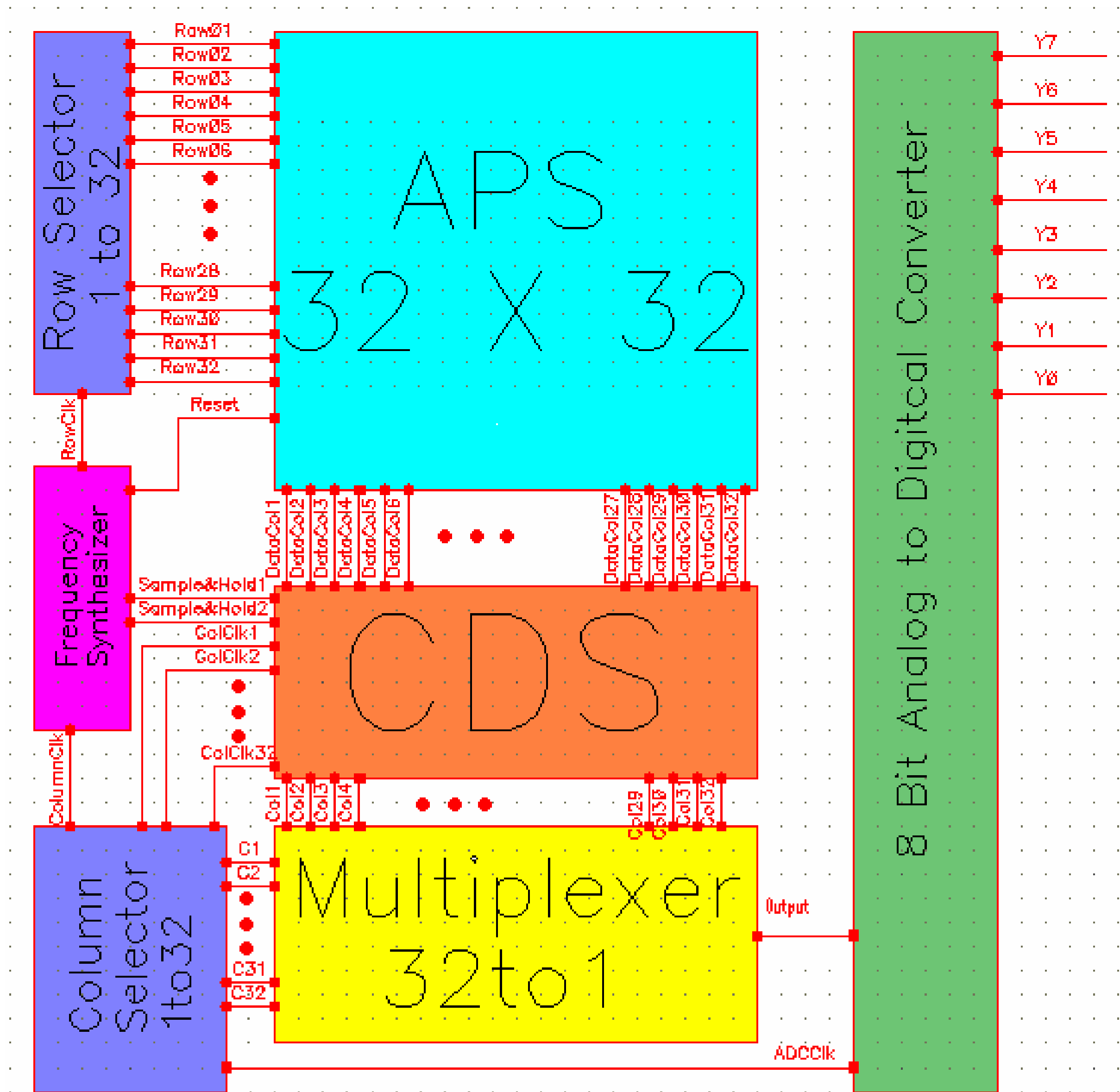


Figure 1: A typical image sensor diagram [14]

Figure 2 shows the schematic of a single APS pixel. From the schematic, one can see that one APS pixel consists of a photodiode and several transistors. In our case, a phototransistor is proposed to be used as a photosensor, and we will only concentrate on the comparison of

hydrogenated amorphous silicon (a-Si:H) and nanocrystalline silicon (nc-Si) TFT phototransistor devices under green light illumination without further conditioning the signal using on-pixel electronics.

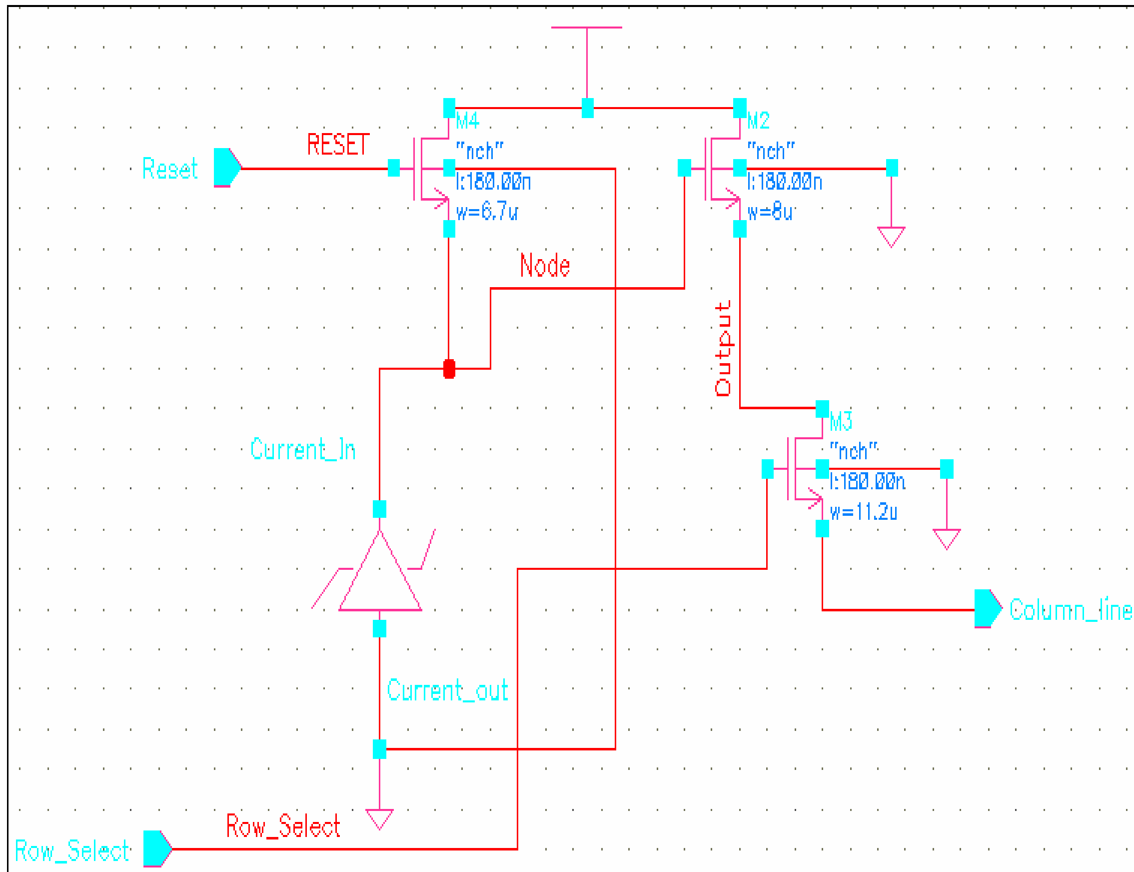


Figure 2: one APS pixel schematic [14]

2.2 Issues for Comparing Photo Transistor Performance

In our phototransistor design, we are restricted by a number of considerations. First, the structure of the photo transistor has to be determined before the fabrication to yield desired electrical performance. In this paper, the bottom gate structure has been used due to the low gate leakage current as compared to the top gate structure[15] and by the fact that most foundries have bottom gate structure as a standard. Second, the proper fabrication process needs to be designed. This is critical for the future industrial implementation. Third, the size/layout of the photo transistors is another important factor that determines the value of the photo current. For high resolution applications, photo transistors must be as small as possible. However, downscaling may reduce the drain current. To find a best structure of a photo transistor, five different channel lengths and three different channel widths have been made in our experiment. Fourth, since two different types of devices will be compared, the two devices have to be tested under the same conditions so that the test results are comparable. These conditions will include the same light illumination, the same temperature and the same test equipment. To reduce the effects of above three factors, the two devices were tested one after another without any break. Lastly, the operation conditions yielding the best performance will be different for each device. Therefore, a large range comparison is necessary to comprehensively evaluate the performance of the devices.

2.3 Amorphous Silicon & Nano-crystalline Silicon Photo Transistors

2.3.1 Amorphous Silicon Transistors

Amorphous silicon (a-Si:H) is a semiconductor material deposited by plasma enhanced chemical vapor deposition (PECVD), using silane (SiH_4) or a mixture of silane and hydrogen (H_2) source gases at temperatures of less than 300 ºC. This low temperature process along with the amorphous nature of used substrates, e.g. glass, lead to formation of amorphous materials lacking structural order like that of crystalline silicon [7]. A two dimensional structure of atomic bonding for the a-Si:H and the crystalline silicon is given in Figure 3.a and Figure 3.b [16]. The atoms take regular positions in the crystalline structure; whereas they are slightly varied in the amorphous structure, which cause the bond length and angle of atoms to vary. Since the amorphous silicon has this type of structural disorder, it brings out different electrical properties. For example, the missing atoms will create deep defect states in the

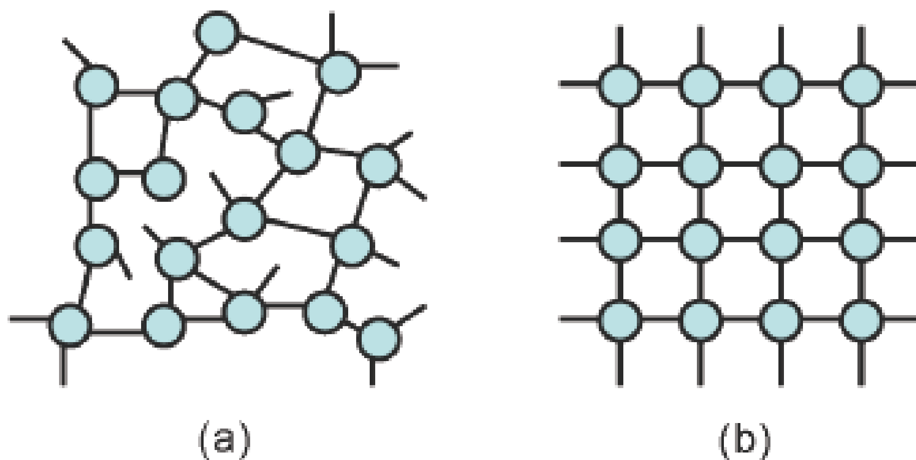


Figure 3: Two dimensional structure of atomic bonding in (a) a-Si:H and (b) crystalline silicon [16].

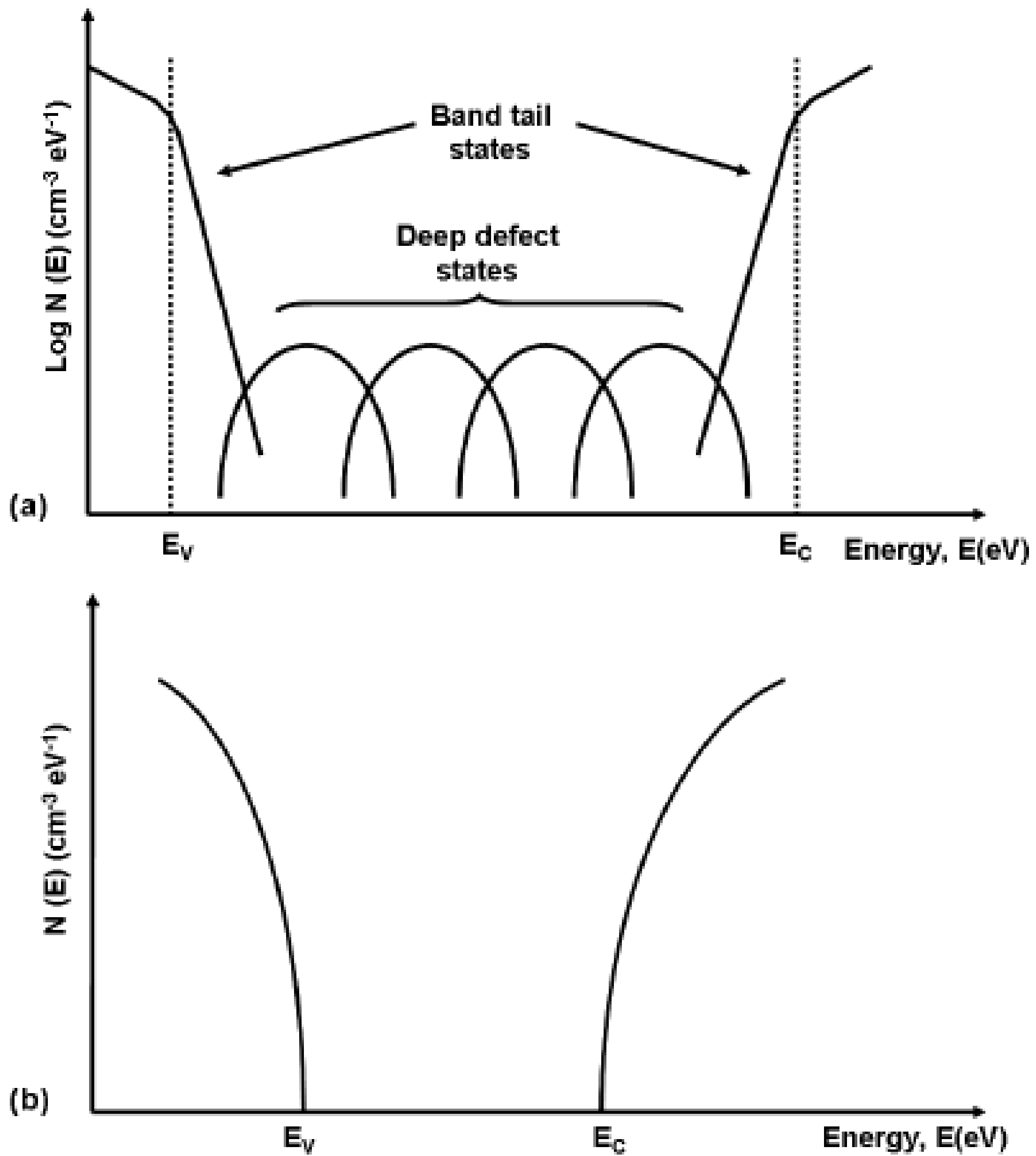


Figure 4: Distribution of density of states in (a) a-Si:H and (b) crystalline silicon. Adapted from[16, 17]**. N (E) is in log scale in (a).**

energy gap of a-Si:H, i.e. dangling bonds, and the deviation in bond length and angle causes in states below the conduction band, commonly known as band tail states. An example of the

distributed deep effect states of the amorphous silicon has been shown in Figure 4.a [7, 16] The density of deep defect states largely depend on PECVD conditions, generally being in the range 10^{15}–10^{18} $cm^{-3}eV^{-1}$[7, 16]. The field-effect mobility of amorphous silicon thin film transistors is in the range of 0.1-1 $cm^2V^{-1}s^{-1}$. The reason of this low mobility is because the electrons are trapped into and released from the band tail states [7]. The instability of the thin film transistor device is another issue to take care of. When TFT is subject to a prolonged gate voltage, the drain-source current (IDS) is observed to gradually decrease over time, associated with a shift in its threshold voltage (ΔVt) [18]. This instability is commonly attributed to two mechanisms: (1) defect state creation in the a-Si:H active layer and (2) charge trapping in the gate dielectric[18].

2.3.2 Nano-Crystalline Silicon Transistors

Due to high-performance and low-cost, nanocrystalline silicon (nc-Si:H) thin film transistor (TFT) have been drawn much attention recently as an alternative of amorphous silicon (a-Si:H) to improve the carrier mobility and the device stability[19]. With the benefit of sharing the same tools with the amorphous silicon technology processing, the nanocrystalline silicon TFT processing just needs the process parameters to be changed so that the material microstructure can be changed from the amorphous phase, without any structural order, to crystalline phase, with some degree of structural order. A two dimensional atomic bonding of the nanocrystalline silicon device has been shown in Figure 5. Although nc-Si contains amorphous phase, it was observed that its electrical stability was significantly improved when the volume fraction of crystalline grains exceeds 60% [20, 21].

Figure 6 has shown the physical structure of the nanocrystalline silicon device, which has indicated that at the beginning of the deposition process, the growth structure of the nanocrystalline silicon on the glass or other wafer is not the crystalline structure. It may be entirely amorphous or comprised of very small grains of just a few nanometers with dominant amorphous phase. When the film grows thicker, the grain size increases and the film becomes highly crystalline with very little of the amorphous phase [22].

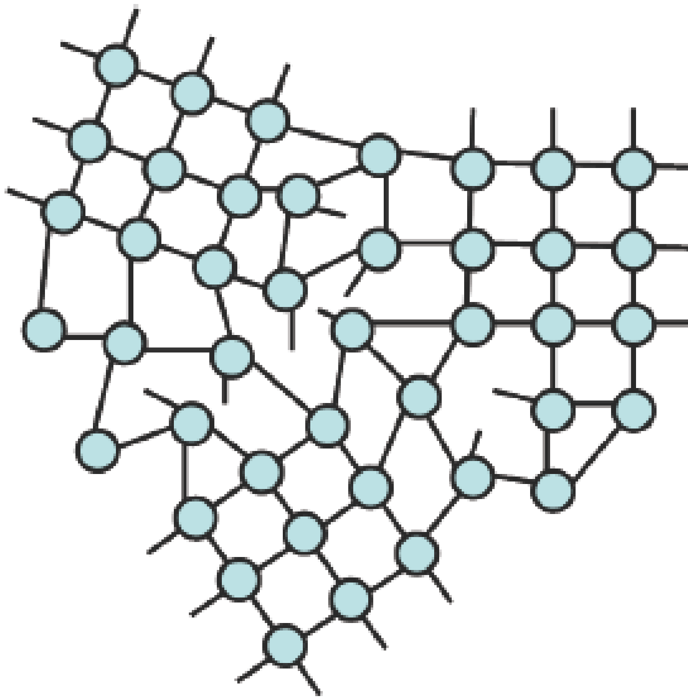


Figure 5: Two dimensional representation of atomic bonding in nc-Si (adapted from [23]**).**

Figure 7.a has shown the bottom gate TFT structure; while Figure 7.b has shown the top gate structure. It can be expected that the top gate nc-Si device, where the conduction channel will be formed in the highly crystalline part of the nc-Si film, has better performance than the bottom gate nc-Si device, where the device performance is determined

by the quality of bottom layers of nc-Si. However, most industrial facilities use bottom-gate process, hence, in order to comply with them, bottom-gate structure is commonly used for practical applications. Thin film phototransistors are operated in their off state region and active region. Electron-holes will be generated when the incident light hit the channel. The photo current will be generated to go through the source and the drain.

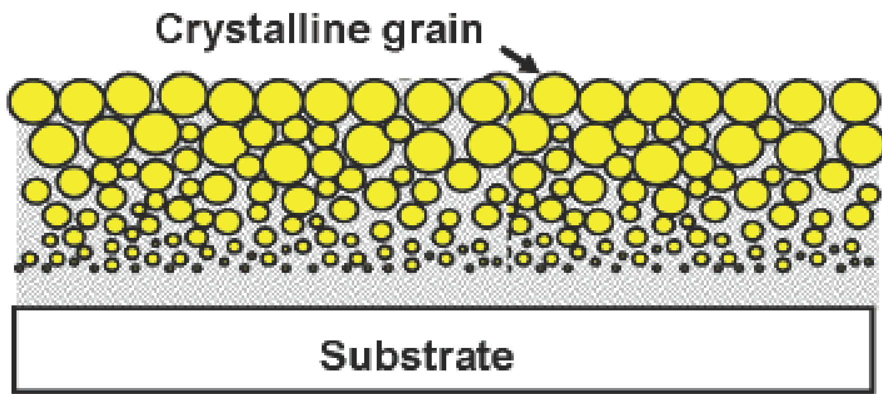


Figure 6: Material structure of nc-Si. It is inhomogeneous and comprises of smallgrains near the substrate and larger grains when thickness increases (adapted from[22]**).**

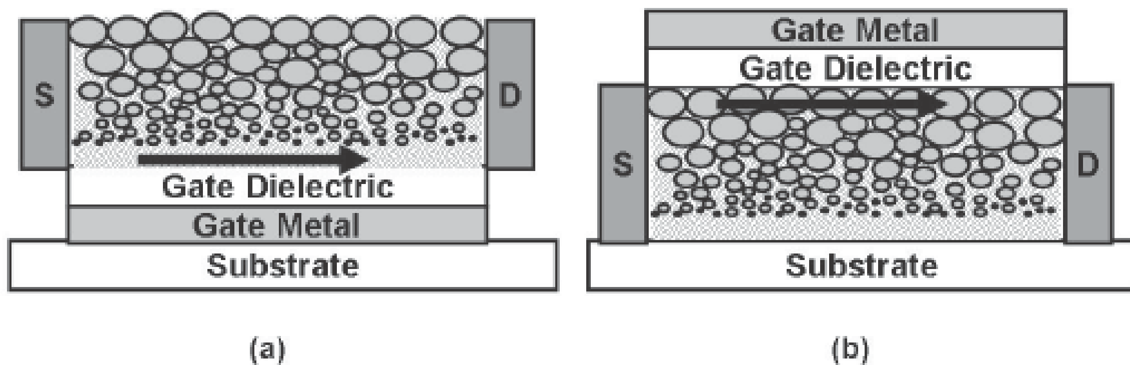


Figure 7: Two nc-Si TFT structures, (a) bottom-gate and (b) top-gate. The arrow represents the conduction path[18]**.**

Chapter 3
Experiments and Procedures

3.1 Introduction

The transfer characteristic is those intrinsic parameters of a system, subsystem, or equipment which, when applied to the input of the system, subsystem, or equipment, will fully describe its output. The mobility, threshold voltage are sub-threhold voltage are three key parameters for evaluating a thin-film phototransisor device. Parasitic resistance and stability are two key parameters for evaluating the performance of a nano-crystalline device. Therefore, these parameters were measured or extracted from the designed experiments.

3.2 Photo-TFT Fabrication Process

Photo-TFTs used in this study were fabricated using standard bottom-gate structure. The cross sections of the a-Si:H and the nc-Si TFT in the fabrication process are shown in Figure 8. The gate metal is below the active layer and source/drain contacts are on the top, which is the well known bottom-gate inverted-staggered structure [24]. Figure 9 shows the basic sequence of the fabrication process. Figure 9.1 and Figure 9.2 shows that a metal layer is deposited, by sputtering, on a substrate and patterned to define the gate area. After the gate has been deposited, in Figure 9.3, a trilayer comprising of hydrogenated amorphous silicon nitride as the gate dielectric, a-si:H or nc-Si as the active layer, and another a-SiNx:H as the passivation dielectric are deposited in one PECVD cycle.

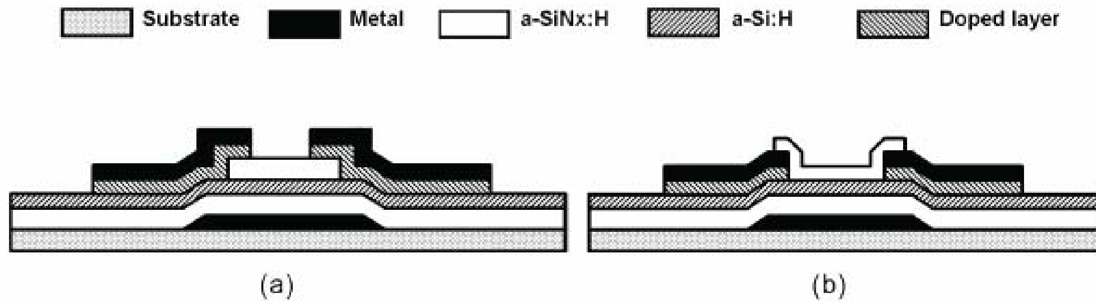


Figure 8: Bottom-gate inverted-staggered TFT structures, (a) trilayer and (b) back channel etched[16, 24]

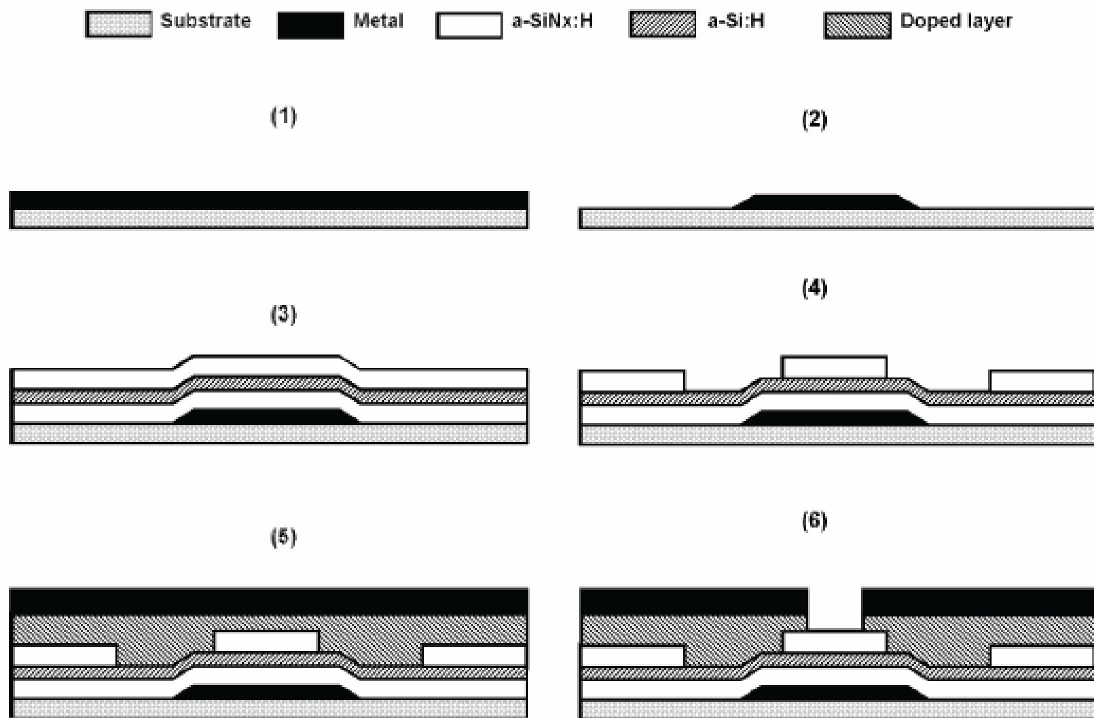


Figure 9: PECVD fabrication process[18, 25]

The passivation nitride is then patterned to expose selected regions of the active layer in Figure 9.4. Subsequently, n+ doped and metal layers are deposited and patterned to make source-drain contacts (Figure 9.5 and Figure 9.6)[16, 18, 24]. This structure is commonly

known as trilayer or etch stop, due to the fact that the passivation nitride protects the active layer, on top of the gate area, from being exposed to etchants and, thus, being damaged during etching processes [18].

An accumulation channel has been shown in Figure 10 when the bottom-gate TFT has its source connected to the ground and its drain to Vd. Considering an n-type device, a higher positive gate voltage will induce more electrons near the semiconductor and gate dielectric interface. Therefore, the accumulation channel will become wider so that the conductivity will increase, which indicates the electron mobility of the thin film transistor improves. Figure 11 shows the density of states in the energy gap of a-Si:H and is a simple one-dimensional model [7]. The band tail states degrade the electron mobility in the thin film transistor. As can be observed from Figure 11, the electron can be trapped or released into or out of different energy levels traps. The effective field-effect mobility μ_{FE} can be calculated as,

Equation 3-1: $\mu_{FE} = \mu_0 \frac{\tau_{free}}{\tau_{free} + \tau_{trapped}}$

where μ_0 is the band mobility of electrons without trapping, τ_{free} and $\tau_{trapped}$ are the time intervals that electrons are free and trapped[7].

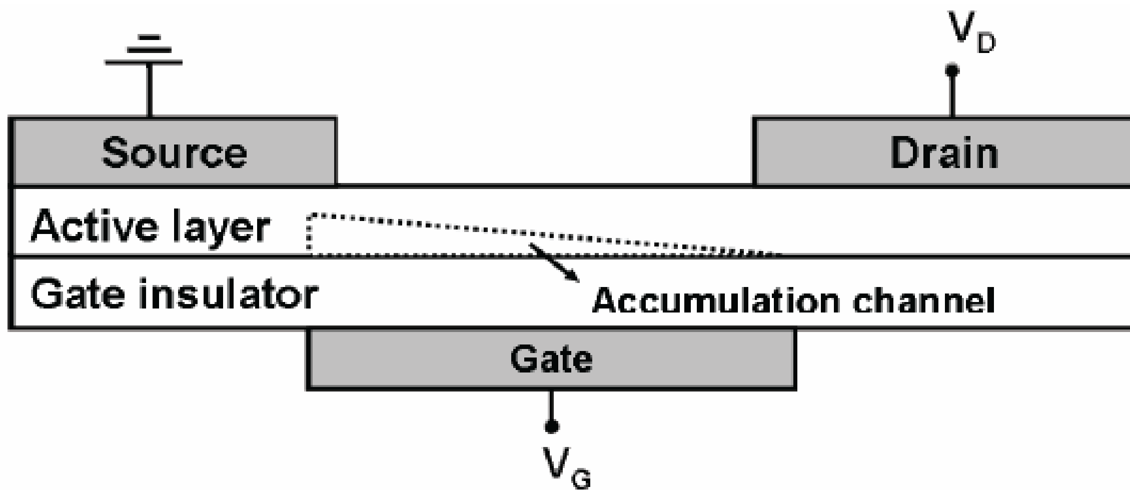


Figure 10: Illustration of operation of a bottom-gate TFT when gate and drain biases are applied [26]

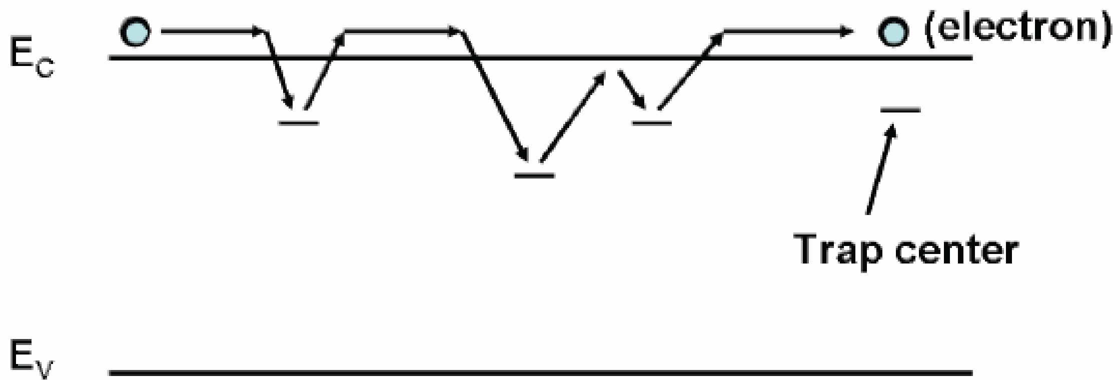


Figure 11: A one-dimensional model showing the motion of electrons that are frequently trapped in and released from band tail states [7]

A typical transfer characteristic of a bottom-gate nc-Si or amorphous silicon TFT has been shown in the Figure 12, which has been separated into three regions: off-state region, sub-threshold region and on-state region. The sub-threshold region refers to the region where most of the induced electrons are trapped in deep defect states until all deep defect states have been filled up by induced electrons, when the gate voltage increases from around zero

to positive voltage and the Fermi level E_F is in the band tail states [24, 27]. Therefore, the threshold voltage V_T can be expressed as,

Equation 3-2: $V_T = qN_T t_S (E_F - E_i) / C_{gate}$

where $E_F - E_i$ is the energy difference between the Fermi level and the intrinsic level at threshold, the C_{gate} is the gate capacitance per unit area, the t_S is the thickness of the channel layer[16].

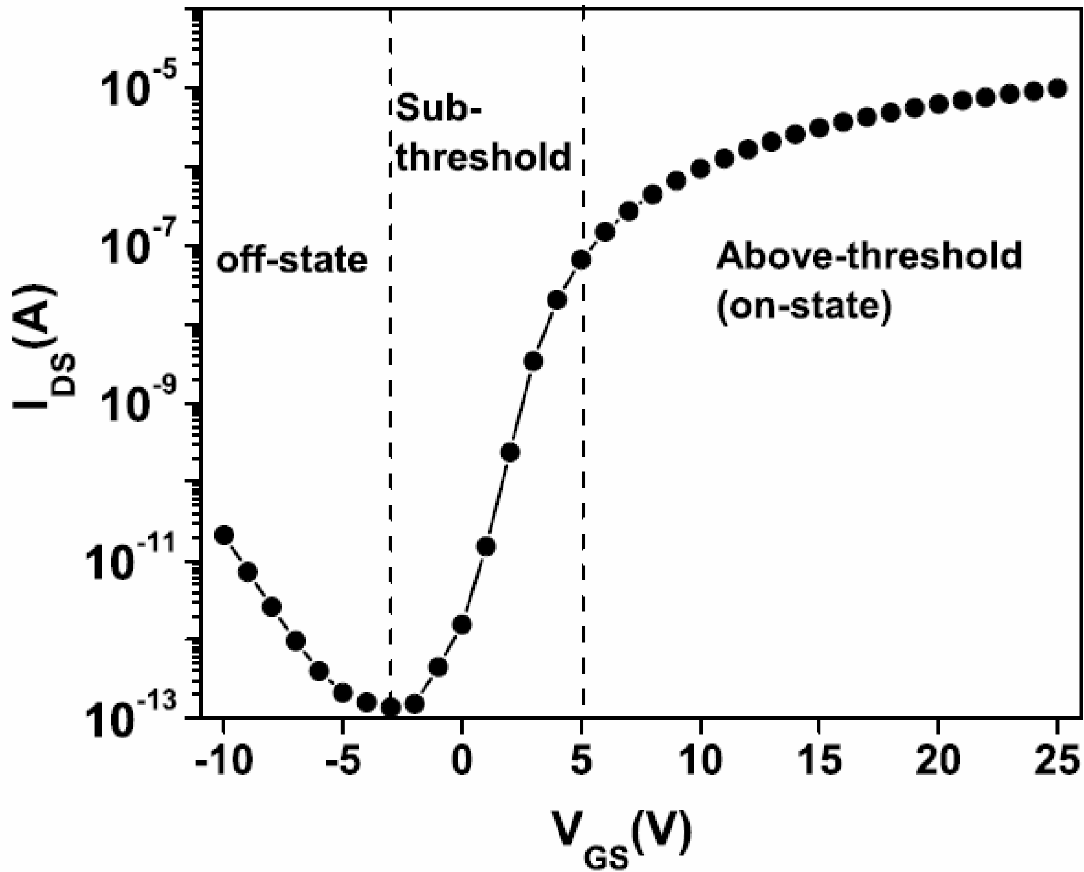


Figure 12: Typical I-V curve of a bottom-gate nc-Si or a-Si:H TFT [18]

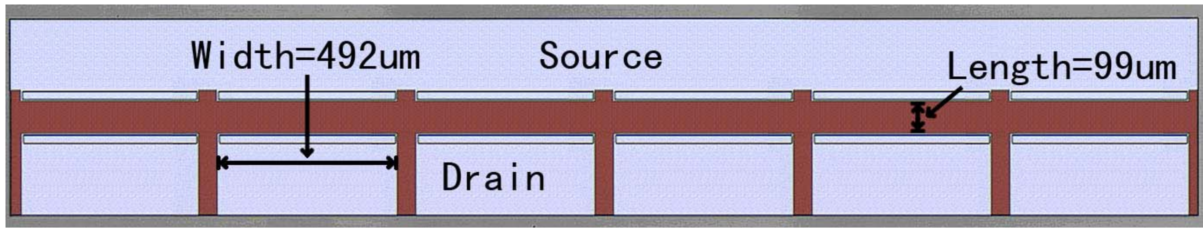


Figure 13 : Bottom Gate Photo Transistor Length=99um and Width=492 um

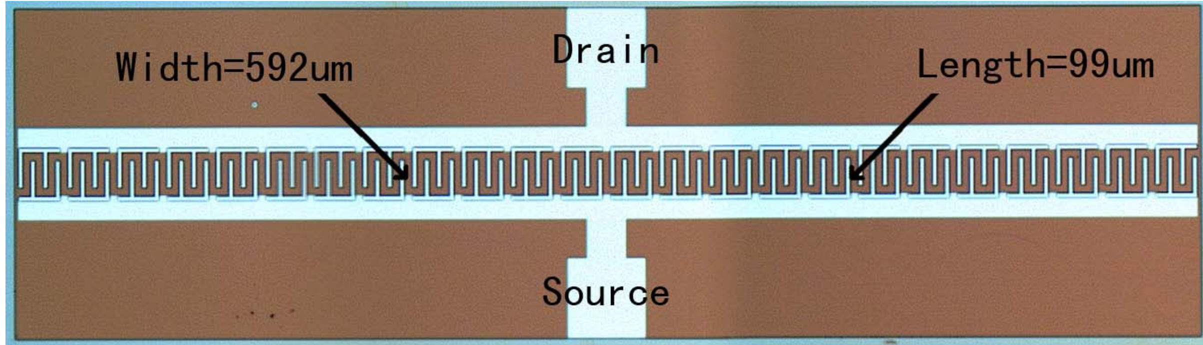


Figure 14: Bottom Gate Photo Transistor Length=99um and Width=592 um

Different physical structures of the photo transistors used in our testing are shown in Figure 13 and Figure 14. Different experimental measurements have been carried on these devices. The structure in Figure 13 was used for verifying the stability of the devices, whereas the structure in Figure 14 was selected for calculating the electrical and optical parameters. This was done due to limited number of large footprint TFTs on each wafer. Since phototransistor electrical performance after the stability stress test can only be reverted by high temperature annealing, we used small footprint TFTs for stability tests, and then used TFT in Figure 14 for electrical testing because it has larger W/L ratio than the structure in Figure 13. Note that TFT stability is independent on width to length ratio.

3.3 Measurements and Calculations

3.3.1 Electrical performance

3.3.1.1 Mobility Calculation

Figure 15 shows a typical field-effect mobility curve, which was obtained from TFT transfer characteristic.

Because the TFT is operating in the linear region, $V_{ds}>V_{gs}-V_t$; $V_{ds}=1V$. Following equations show how to calculate the field effect mobility.

Equation 3-3: $I_{DS} = \mu_{FE}\frac{C_i W}{L}((V_{GS}-V_T)V_{DS}-\frac{1}{2}V_{DS}^2)$

$\frac{\partial I_{DS}}{\partial V_{GS}}|_{V_{DS}=1V} = \mu_{FE}\frac{C_i W}{L}$;

Thickness: $t = 2.7\times10^{-5}cm; \varepsilon = 6.4; \varepsilon_0 = 8.854\times10^{-14}Fm^{-1}$

$C = \varepsilon * \varepsilon_0 / t = 2.1\times10^{-8}Fcm^2 = 21nFcm^2; W = 592um$

Sample calculations:

L=99um: $\frac{\partial I_{DS}}{\partial V_{GS}}|_{V_{DS}=1V} = \frac{C_i W\mu}{L} = 1.62\times10^{-7} \Rightarrow u = 1.26cm^2V^{-1}s^{-1}$

L=47um: $\frac{\partial I_{DS}}{\partial V_{GS}}|_{V_{DS}=1V} = \frac{C_i W\mu}{L} = 2.60\times10^{-7} \Rightarrow u = 0.96cm^2V^{-1}s^{-1}$

L=25um: $\frac{\partial I_{DS}}{\partial V_{GS}}|_{V_{DS}=1V} = \frac{C_i W\mu}{L} = 4.41\times10^{-7} \Rightarrow u = 0.866cm^2V^{-1}s^{-1}$

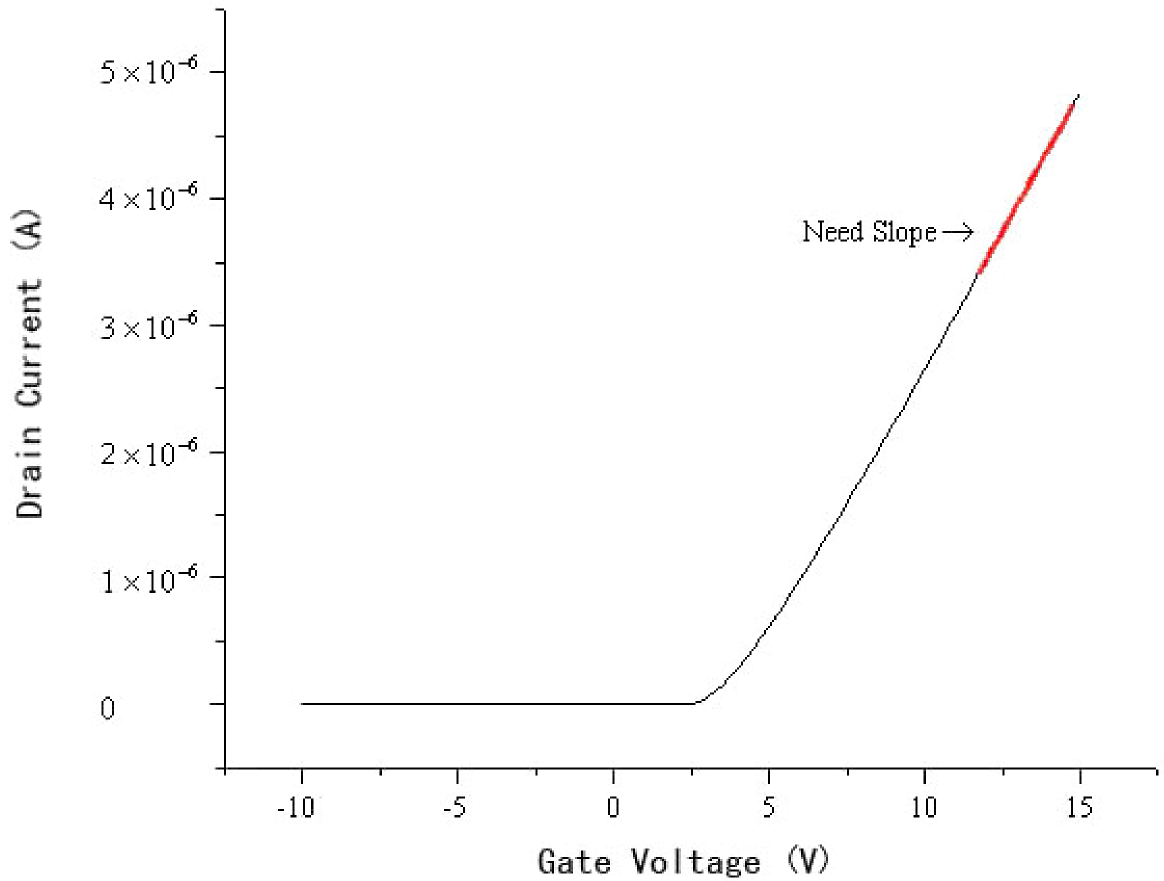


Figure 15: Field-Effect Mobility and Vt calculation Method

3.3.1.2 Threshold voltage (Vt) calculation

Figure 15 shows a typical threshold voltage calculation curve, which was obtained from TFT transfer characteristic using Orgin calculation software.

Because the TFT is working in the linear region, $V_{ds}>V_{gs}-V_t$; $V_{ds}=1V$;

Equation 3-4: $I_{DS} = \frac{C_i W \mu}{L}((V_{GS}-V_T)V_{DS} - \frac{1}{2}V_{DS}^2) = \frac{C_i W \mu}{L}(V_{GS} - (V_T + \frac{1}{2}))$

where $I_{ds}=0$.

Therefore $V_T=V_{gs}-0.5$.

From I-V curve, we can get an I-V relationship, which was represented as Y=kx+b, where x represents V_g(Gate Voltage), y represents I_d(drain current)

$$K = \frac{\partial I_{DS}}{\partial V_{GS}} |_{V_{DS}=1V} = \frac{C_i W \mu}{L}$$

Sample calculation:

L=99um : $y = 1.62 \times 10^{-7} x - 5.89 \times 10^{-7}$; V_g=4.39V, V_t=3.89V

L=47um : $y = 2.60 \times 10^{-7} x - 1.11 \times 10^{-6}$; V_g =4.27V, V_t =3.77V

L=25um : $y = 4.41 \times 10^{-7} x - 1.77 \times 10^{-6}$; V_g =4.01V, V_t =3.51V

3.3.1.3 Sub-Threshold slope calculation

Figure 16 has shown a typical sub-threshold slope calculation curve, which was obtained from the TFT transfer characteristic using Orgin calculation software. The sub-threshold voltage slope (S) is defined as, $1/S=d(\log(I_d))/d(V_g)$. The unit of S is V/Dec.

Because the TFT is working in linear region, $V_{ds}>V_{gs}-V_t$; V_{ds}=1V;

From I-V curve, we fit a linear relationship, which was represented as Y=kx+b, where x represents $\log(V_g)$(Gate Voltage), y represents $\log(I_d)$(Drain current), $K=d(\log(V_g))/d(\log(I_d))$

Sample Calculation:

L=99um: y=2.55429x-15.15577; 1/S=2.55429; S=0.3915 V/Dec

L=47um: y=2.40961x-14.406; 1/S=2.4096; S=0.415005 V/Dec

L=25um: y=2.34927x-14.03; 1/S=2.34927; S=0.425664 V/Dec

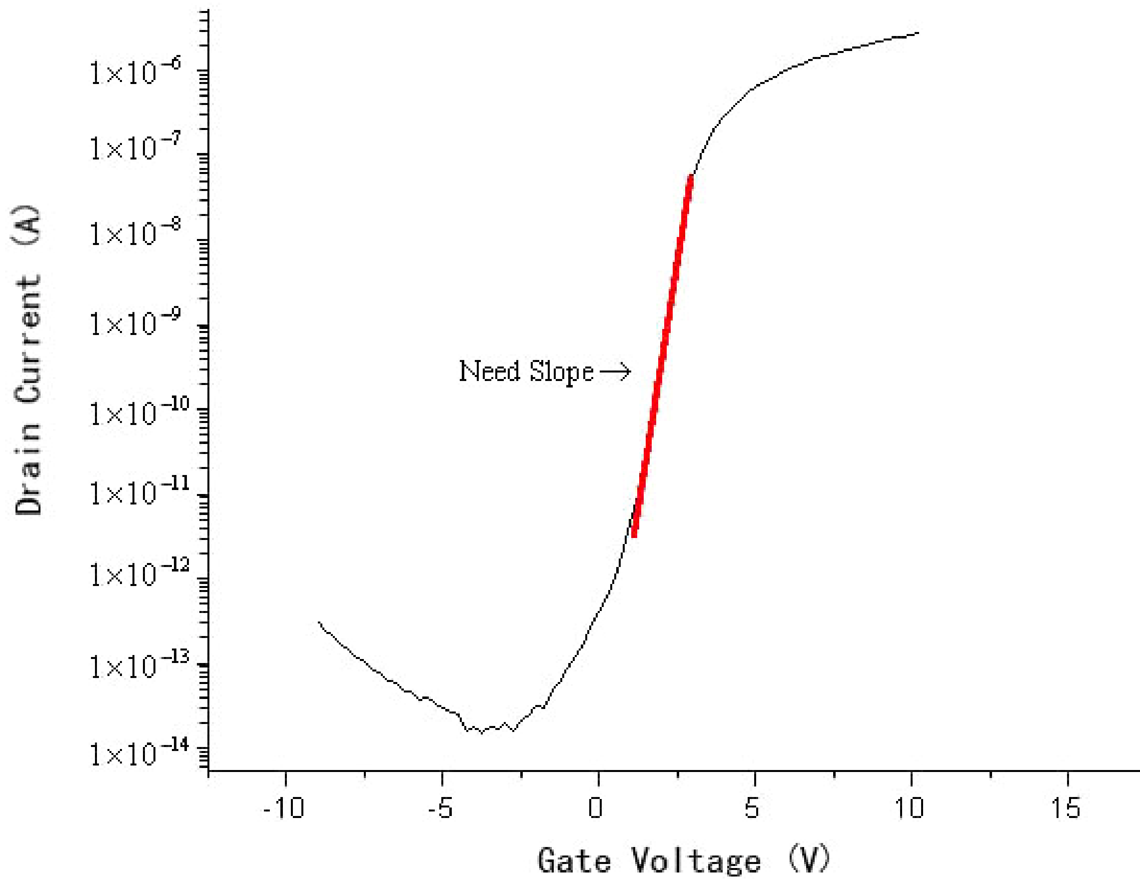
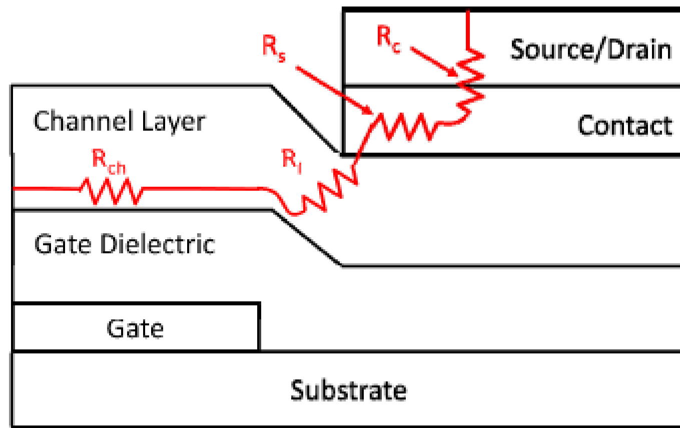


Figure 16: Sub-threshold Voltage Slope Calculation

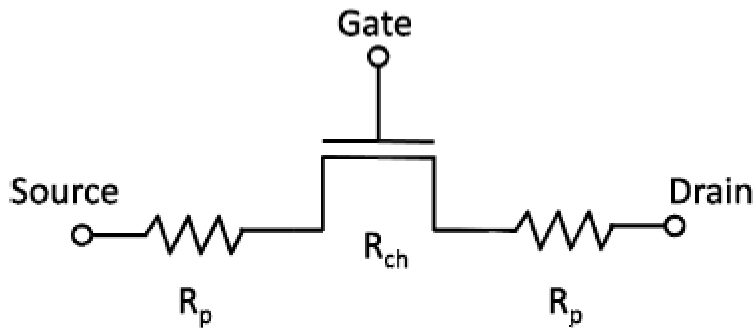
3.3.1.4 Parasitic Resistance

Figure 17.a shows the parasitic resistance in a typical TFT, which may affect TFT parameter extraction, especially for a short channel device. The total parasitic resistance is the sum of the interface resistance between the source/drain and the contact(R_c), the contact series resistance(R_s), the resistance between the contact and the channel(R_i) and the channel series resistance(R_{ch}). Figure 17.b shows a typical parasitic resistance model. The parasitic

resistance affects the experimental photo current result for some devices. In our experiments, the experimental results from the shortest channel length device, 14um, had to be abandoned due to the inconsistent data results.



(a)



(b)

Figure 17: (a) Parasitic components in staggered bottom gate nc-Si:H TFT and (b) equivalent circuit for parasitic resistance analysis[28]

3.3.2 Performance Measurement under illumination

Two important photo-TFT performance indicators are discussed in this research. One is the

photo current gain, which is defined as the ratio of the photo current over the dark current. Another is the external quantum efficiency. The external or overall quantum efficiency is defined as the number of photogenerated electron-hole pairs, which contribute to the photocurrent, divided by the number of the incident photons[29]. Following equations show how to calculate external quantum efficiency by using a photodiode, whose quantum efficiency was given.

$$E = \frac{hc}{\lambda}$$

where E is the energy, h is Plank's constant, c is the speed of light, λ is the incident light wave length

$$P_{opt} = E\Phi A \Leftrightarrow \Phi A = \frac{P_{opt}}{E} = \frac{P_{opt}\lambda}{hc}$$

where E is the energy, h is Plank's constant, c is the speed of light, λ is the incident light wave length, P_{opt} is the incident light power, Φ is the light flux density, A is the area

$$\frac{I_{ph}}{P_{opt}} = \frac{e_0\lambda_0}{hc}QE \Leftrightarrow I_{ph} = \frac{e_0\lambda_0 P_{opt}}{hc}QE = e_0 QE\Phi A$$

where h is Plank's constant, c is the speed of light, λ is the incident light wave length, P_{opt} is the incident light power, Φ is the light flux density, A is the area, e_0 is the charge of an electron, QE is the total quantum efficiency

Equation 3-5: $I_{DS-PD}(A) = \Phi \cdot e_0 \cdot A_{PD} \cdot QE_{PD}(\lambda)$.

Equation 3-6: $\Phi = \frac{I_{DS}(A)}{e_0 \cdot A_{PD} \cdot QE_{PD}(\lambda)}$

In this study, our extracting method has used two photo TFTs. One TFT is a calibrated stable photodiode. Another TFT is the tested transistor. First, after the light source was mounted, a calibrated stable photodiode was placed in a fixed position. Then, the photo current of the photo diode was measured. The quantum efficiency of the photo diode has already been measured previously and was found to be around 0.8. From Equation 3-6, the light illumination intensity of the position where the photodiode was placed can be calculated. Then we took out the photodiode and replaced it with our phototransistor at the position as close as possible the original position, After the photo current was measured, the quantum efficiency can be calculated from Equation 3-8. The illumination, the quantum efficiency and the photo current gain can all be calculated from the experimental procedures, and the graphs of the quantum efficiency vs the light illumination and the photo current gain vs the light illumination can be drawn. Hence, the optical properties of different devices under the same light illumination can be compared.

Equation 3-7: $I_{DS-PT}(A) = \Phi \cdot e_0 \cdot A_{PT} \cdot QE_{PT}(\lambda)$

Equation 3-8: $QE_{PT}(\lambda) = \frac{I_{DS-PT}(A) \cdot A_{PD} \cdot QE_{PD}(\lambda)}{I_{DS-PD}(A) \cdot A_{PT}}$

3.3.3 Stability Test

To evaluate the stability of the nc-Si TFT, a stability test has been performed using an automated test equipment. The drain voltage was set to 0.1V. The gate voltage was +10V. The source was connected to the ground. The transfer characteristics were measured every 30 minutes. Threshold

voltage was retrieved from the transfer characteristics, and threshold voltage shift was used as the stability measure. The test lasted six hours.

Chapter 4
Performance Analysis

4.1 Electrical Performance Analysis

4.1.1 Transfer Characteristic

Figure 18 shows typical transfer characteristics of the nc-Si TFT 'before annealing' in dark and 'after annealing' in dark and the a-Si:H TFT transfer characteristics 'before annealing' in dark. From these characteristics, we subtracted electrical properties of these two devices, including the mobility, threshold voltage, sub-threshold voltage slope, off current and the series resistance of the devices. One can see that annealing increases both off-current and on-current making nc-Si TFT comparable with a Si:H counterpart.

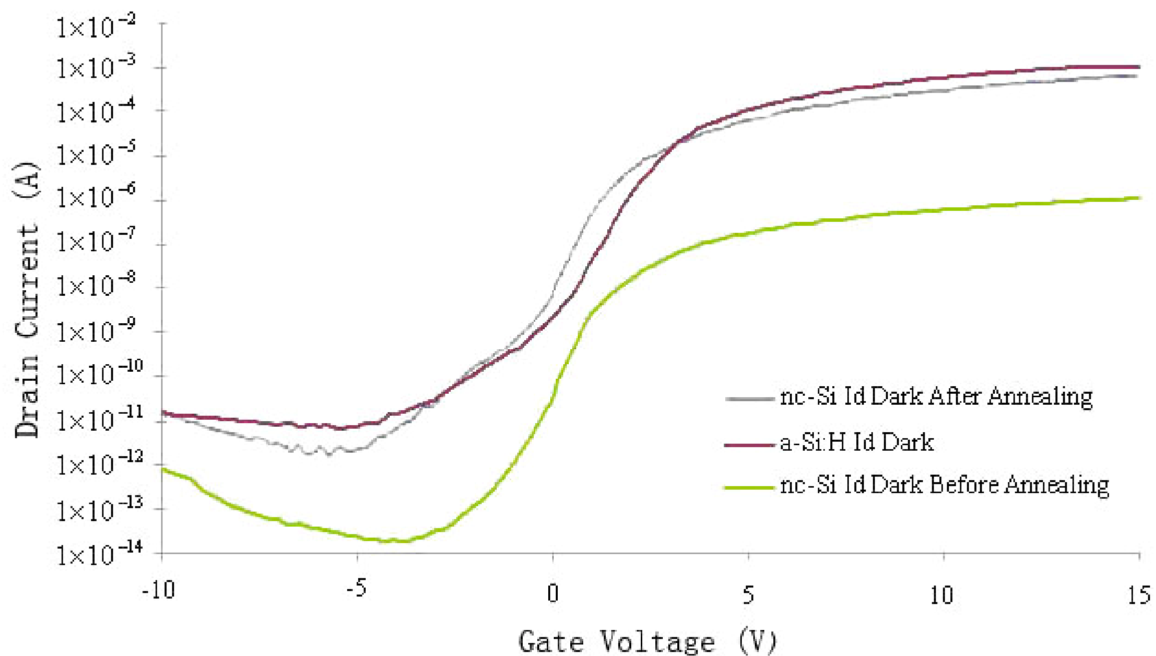


Figure 18: nc-Si Vs a-Si:H Transfer Characteristic

4.1.2 Mobility Analysis

Figure 19 shows the mobility vs TFT channel length varying from 20um to 100um for a-Si:H TFT. One can see that the mobility of the device increases when the channel increases. Because the device resistance can be modeled as the fixed source/drain resistance plus the channel resistance [30], when the channel length increases, the effect of the source/drain resistance will decrease. Therefore, the mobility of the device will be closer to the mobility of the channel.

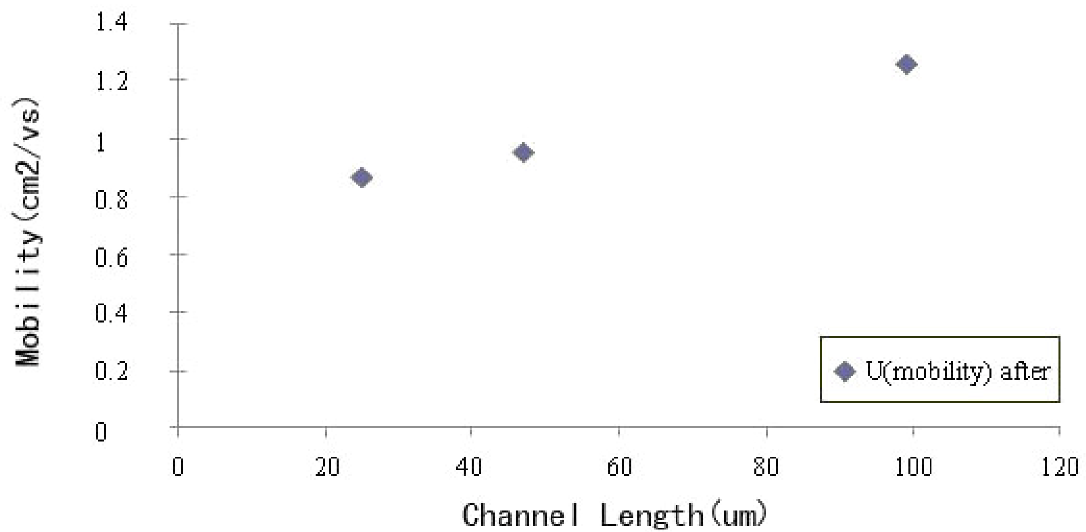


Figure 19: Mobility of a-Si:H TFT

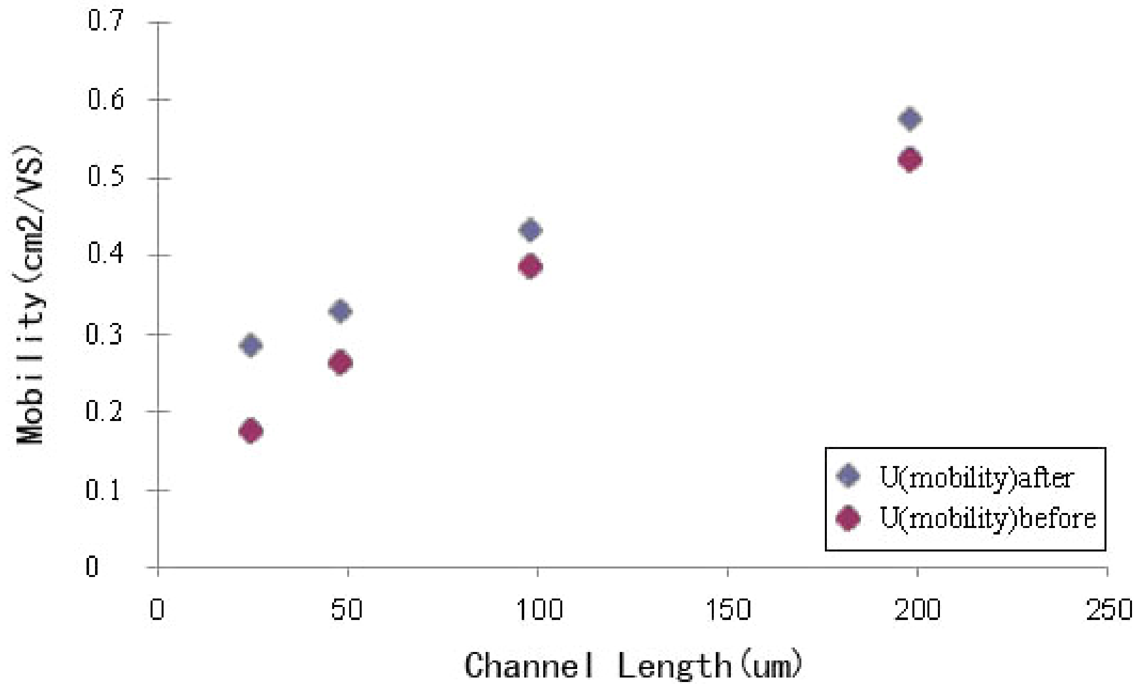


Figure 20: Mobility of nc-Si TFT

In Figure 20, the same trend was found as in a-Si:H photo-TFTs, i.e., field-effect mobility increases with channel length. This figure also shows the comparison the mobility of the device 'Before Annealing' and 'After Annealing', performed under 120ºC for 45 minutes with air supply. It is known that in nc-Si TFTs, an oxidation takes place, which may decrease open state TFT resistance, in particular, the source/drain resistance. One can see that after annealing, the mobility of our device has been slightly increased. This increase is more profound in short-channel device, which is attributed to the effect of source/drain resistance. Thus, the source/drain resistance in nc-Si photo-TFTs is affected by oxidation.

From the above analysis, we can conclude that both devices show the state-of-art performance because the mobility values of both devices agree with the best results previously published for such devices, around 1 $cm^2V^{-1}s^{-1}$[31]. In addition, they both fit the

series resistance model. Second, the nc-Si TFT has slightly lower mobility than the a-Si:H TFT. We can predict that the nc-Si TFT will have lower dark current than the a-Si:H TFT as shown in Figure 25 under certain condition, where we will have more analysis later. Lastly, to make sure the device performance is not affected by source/drain contact oxidation, we pick up the 99um channel length devices to make the comparison because of the limitation of the process of the a-Si:H TFT.

4.1.3 Threshold Voltage Analysis

The threshold voltage of the a-Si:H photo-TFT varies from 3.50 V to 3.90 V when the channel lengths vary from 25um to 99um (see Figure 21). This can be attributed to reduced gate control over the channel in short-channel TFTs similar to short-channel effect in MOSFETs as depletion layers in TFTs is wider than in MOSFETs. As we have mentioned, when the channel length equals 99um, the threshold voltage of the a-Si:H TFT is 3.89V.

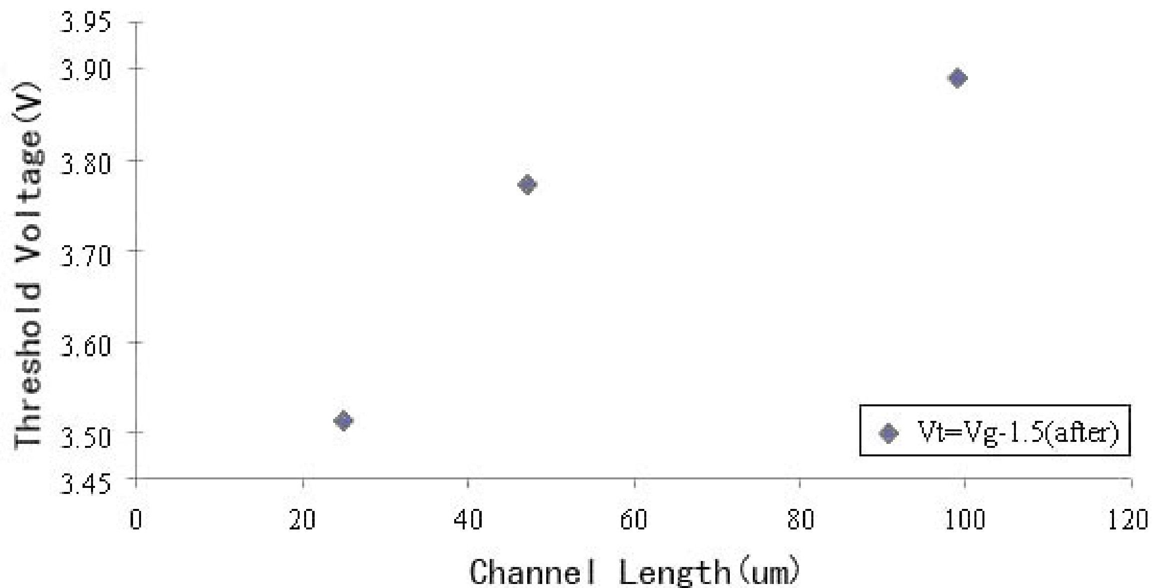


Figure 21: Threshold Voltage of a-Si:H TFT

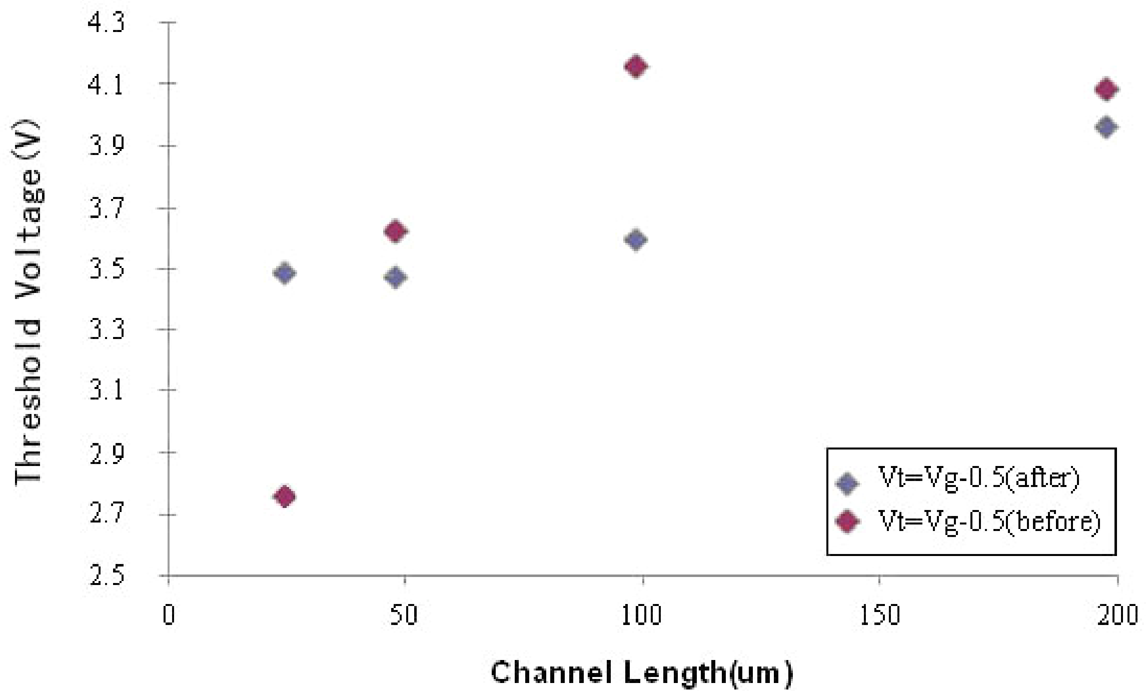


Figure 22: Threshold Voltage of nc-Si TFT

The threshold voltages of the nc-Si TFTs vary from 3.50 volt to 4.0 V for the 'after annealing' process and from 2.70 V to 4.2 V for the 'before annealing' process when the channel lengths vary from 25um to 198um . Because the annealing process helps to stabilize the source/drain contact layers and hence lower the contact resistance, the threshold voltage of 'after annealing' TFT shows lesser dependence on channel length than that for 'before annealing' TFT as shown in Figure 22. As we have mentioned, when the channel length equals 99um, the threshold voltage of the nc-Si TFT is 3.61V. Therefore, we can conclude that both devices have the similar turn-on voltage, around 4 V.

4.1.4 Sub-Threshold Slope Analysis

The sub-threshold slope of the a-Si:H TFT has the range from 0.43 V/Dec to 0.39 V/Dec when the channel length is changing from 25um to 99um in Figure 23. These values are in the normal range for common TFT devices, which is around 0.5V/Dec- 4.72V/Dec [19]. In other words, the a-Si:H TFT has the same turn-on speed as other TFTs.

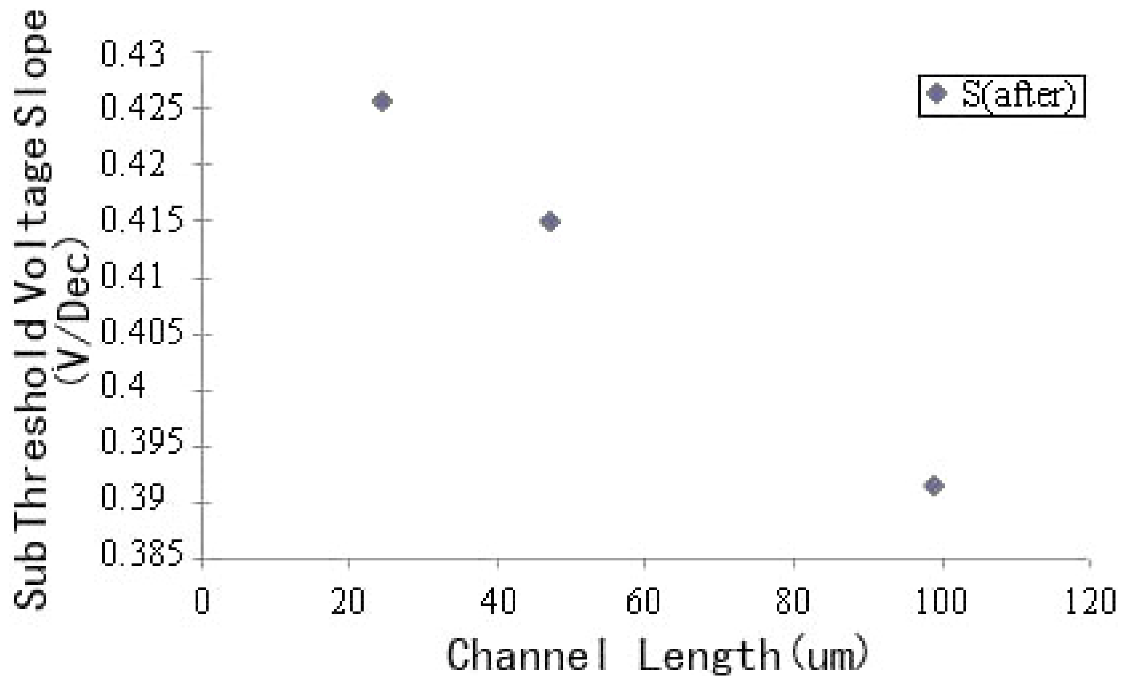


Figure 23: Sub-Threshold Slope of a-Si:H TFT

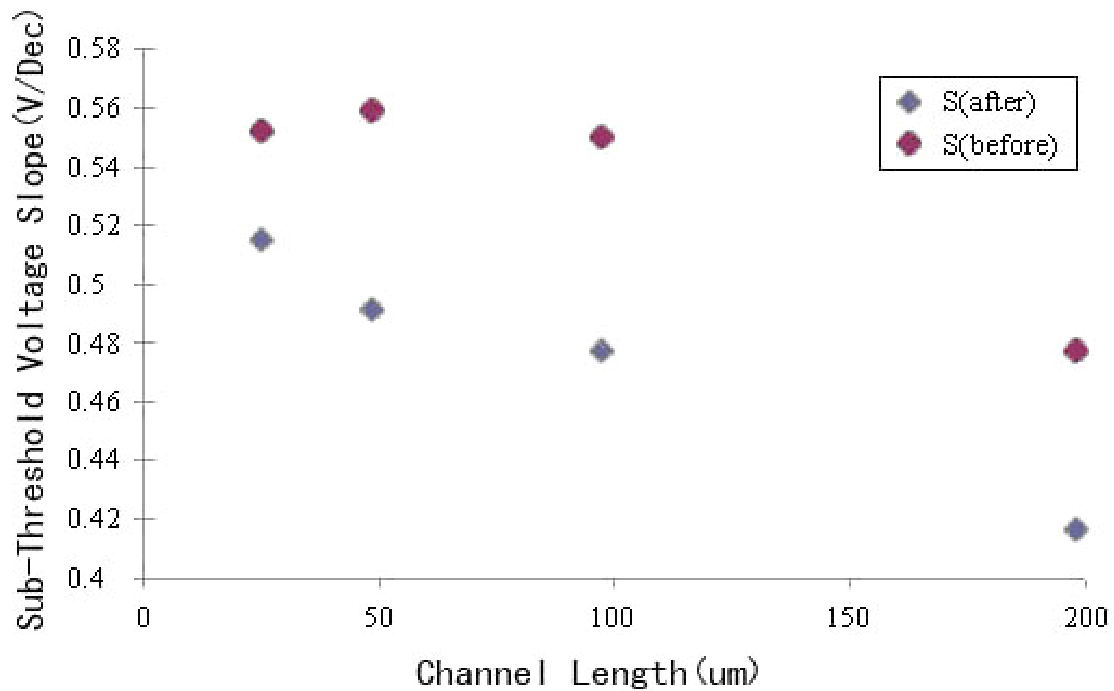


Figure 24: Sub-Threshold Slope of nc-Si TFT

The sub-threshold slope of the nc-Si TFT has a range from 0.6 V/Dec to 0.4 V/Dec when the channel length is changing from 25um to 198um in Figure 24. These values are in the normal range of common TFTs, which usually range from 0.1 V/Dec to 1 V/Dec. In other words, the nc-Si TFT has the same turn-on speed as other TFTs. As we can see, the values of the sub-threshold voltage slope of the device decreased after annealing. As we have discussed, when the device has been annealing, the mobility will increase. In other words, the corresponding drain current will increase. Because the value of the sub-threshold voltage slope equals $d(V_g)/d(\log(I_d))$ [30], the value of the sub-threshold slope will decrease after the device has been annealing.

We can observe that the nc-Si TFT has higher sub-threshold voltage slope than the a-Si:H TFT when the channel length equals 99um. Therefore, the nc-Si TFT has a lower transition

time than the a-Si:H TFT.

4.1.5 Off-current Analysis

The dark current of the a-Si:H TFT has the range from 1×10^{-11}A to 1×10^{-3}A when the gate voltage is changing from -12 V to 15 V in Figure 25. The dark current of the a-Si:H TFT range from 1×10^{-12}A to 1×10^{-3}A when the gate voltage is changing from -12 V to 15 V in Figure 25. We can observe that the nc-Si TFT has a lower dark current than the a-Si:H TFT when gate voltage is from -10V to -3V. We will have more discussion in this range later because the photo transistor basically works when the gain voltage is negative.

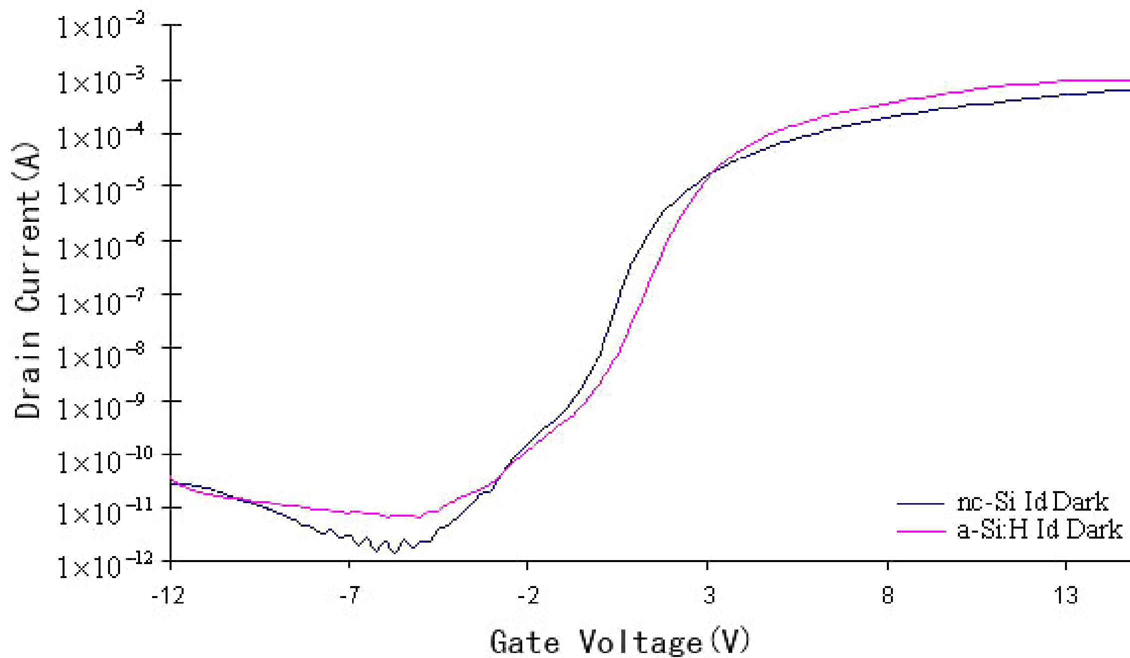


Figure 25: nc-Si Vs a-Si:H Dark Current (Id)

4.1.6 Channel Length Vs Series Resistance Analysis

In its ON state, a TFT can be represented by a series of the channel resistance(R_{ch}), and the

source/drain resistance (R_{ds})(channel length = 99um).

$V_{ds}=I_d(R_{ch}+R_{ds}) = I_d R_m$

$R_m|_{L=0} = R_{ds}$

Therefore, get I_{ds} when $V_g=0.5+V_t$.

For the nc-Si TFT, $V_g=0.5+3.61=4.11$ V.

From the nc-Si curve of Figure 26, when $V_g=4.11V$, we can read $I_d=3.8\times10^{-5}$ A.

Therefore $R_m=V_{ds}/I_{ds}=4.11/3.8\times10^{-5}=108$ KΩ.

$R_m\cdot W=108K\Omega * 592um=6.39$ KΩ-cm <25.0 KΩ-cm[32]

For the a-Si:H TFT, $V_g=0.5+3.89=4.39$ V .

From the a-Si:H curve of Figure 26, when $V_g=4.39V$, we can read $I_d=7.4\times10^{-5}$ A.

Therefore $R_m=V_{ds}/I_{ds}=4.39/7.9\times10^{-5}=60.1$ KΩ.

$R_m\cdot W=60.1K\Omega * 592um=3.56$ KΩ-cm <25.0 KΩ-cm[32]

25.0 KΩ-cm is the well accepted upper bound value for the resistance of TFTs[32]. Both experimental values are less than this value. Therefore, the values of the resistance of both devices are acceptable.

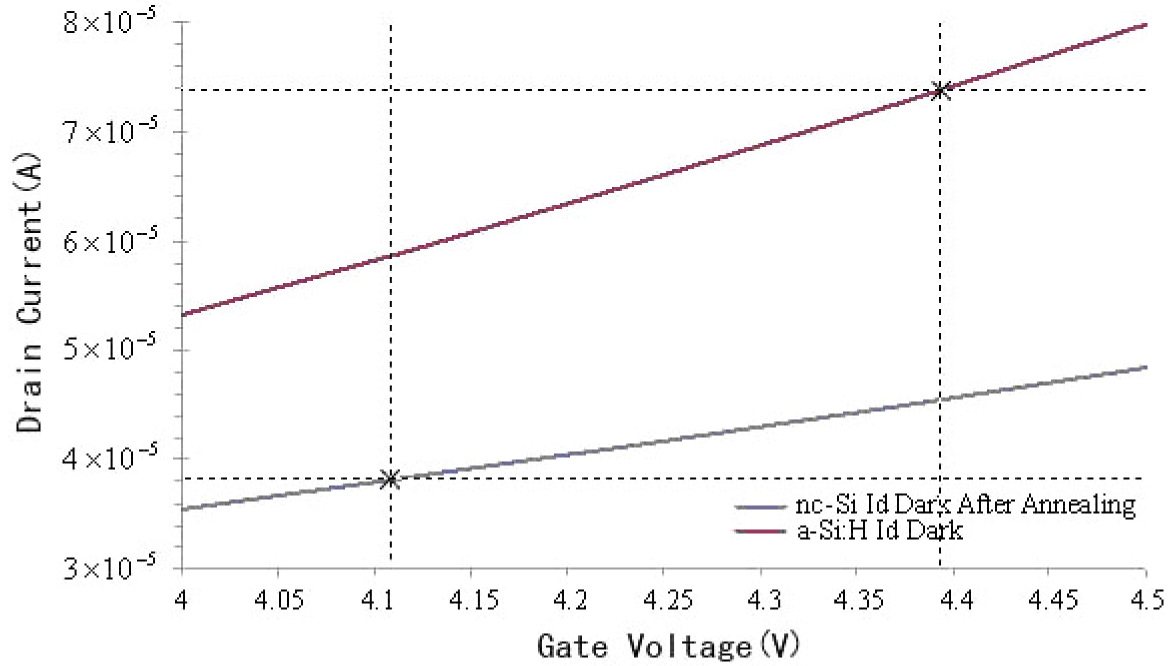


Figure 26: Drain current dependence on Vg of nc-Si and a-Si:H devices

4.2 Performance under Illumination Analysis

4.2.1 Characteristic Photocurrent

Figure 27 shows a-Si:H TFT transfer characteristics under various illumination intensity given in terms of LED current. Figure 28 shows the same characteristic for nc-Si TFT. Based on this information, the following sections give the detail analysis of the optical properties of these two devices, including the photo current, the photo current gain, the quantum efficiency, the effects of Vds and the effects of Vgs.

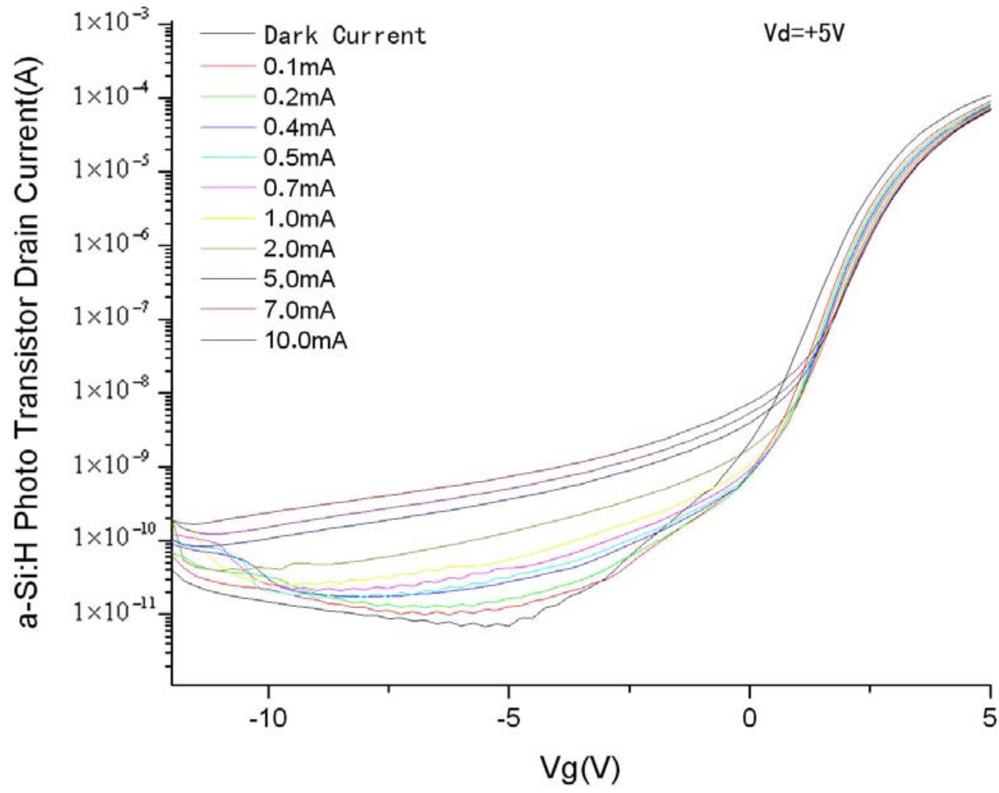


Figure 27: a-Si:H TFT Transfer Characteristic under various illumination intensity

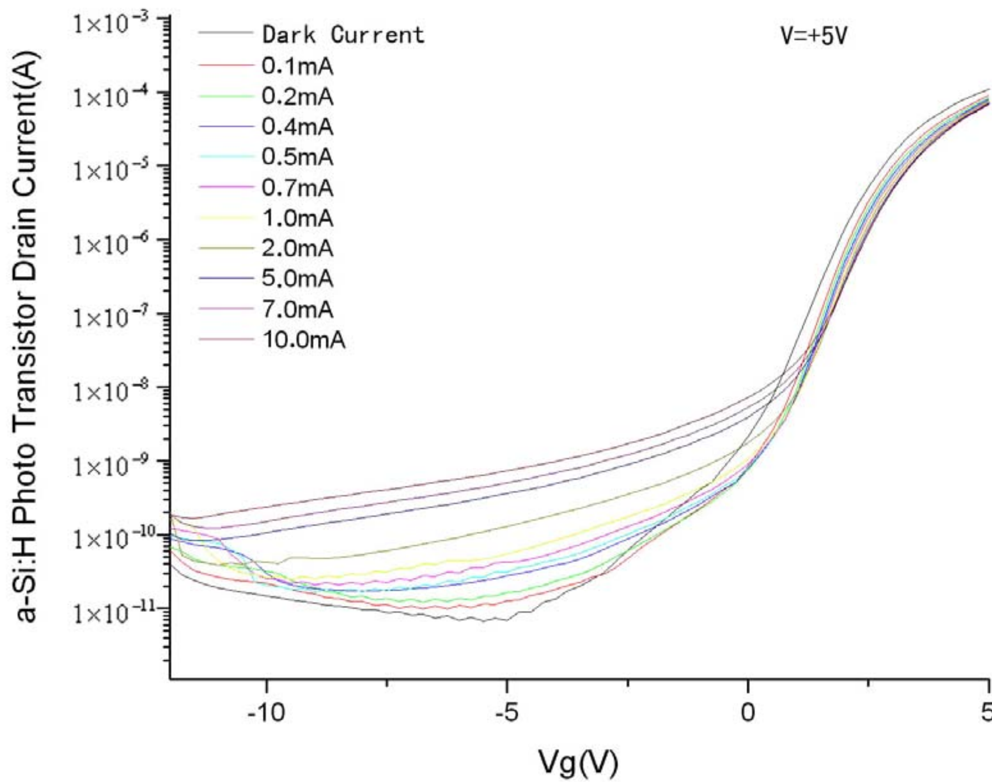


Figure 28: nc-Si TFT Transfer Characteristic under various illumination intensity

4.2.2 Photocurrent Analysis

We will list a group of photo current experimental data to perform detailed analysis in this section. When the gate voltage is less than -12 V or greater than +5 V, the photo current of these two devices are almost the same. In Figure 29, the nc-Si TFT has higher photocurrent than the a-Si:H TFT when the gate voltage is from -5V to +3V under the illumination equivalent to the LED with 0.1mA current supply. In Figure 30, the nc-Si TFT has higher photocurrent than the a-Si:H TFT when gate voltage is from -5V to +3V under the illumination equivalent to the LED with 0.2mA current supply. In Figure 31, The nc-Si TFT has higher photocurrent than the a-Si:H TFT when gate voltage is from -6V to +4V under the

illumination equivalent to the LED with 0.4mA current supply. In Figure 32, the nc-Si TFT has a higher photocurrent than the a-Si:H device when gate voltage is from -7V to +4V under the illumination equivalent to the LED with 0.5mA current supply. In Figure 33, the nc-Si TFT has a higher photocurrent than the a-Si:H TFT when gate voltage is from -6V to +4V under the illumination equivalent to the LED with 0.7mA current supply. In Figure 34, The nc-Si has a higher photo current than the a-Si:H when gate voltage is from -7V to +4V under the illumination equivalent to the LED with 1.0mA current supply.

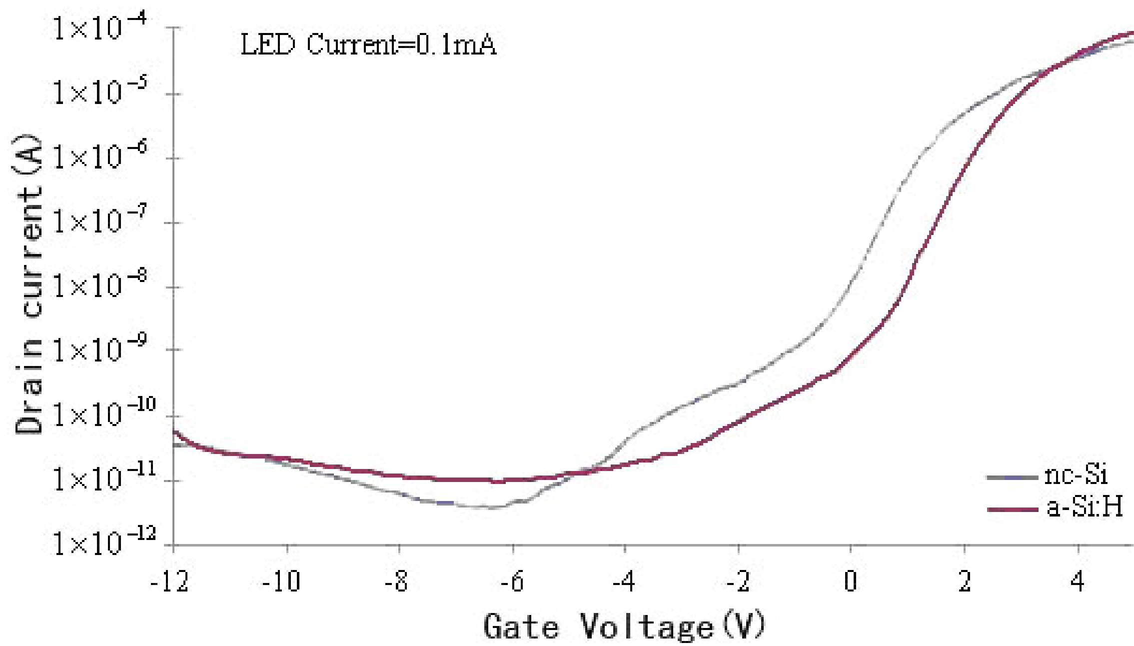


Figure 29: nc-Si Vs a-Si:H Id photo current at the LED current =0.1mA

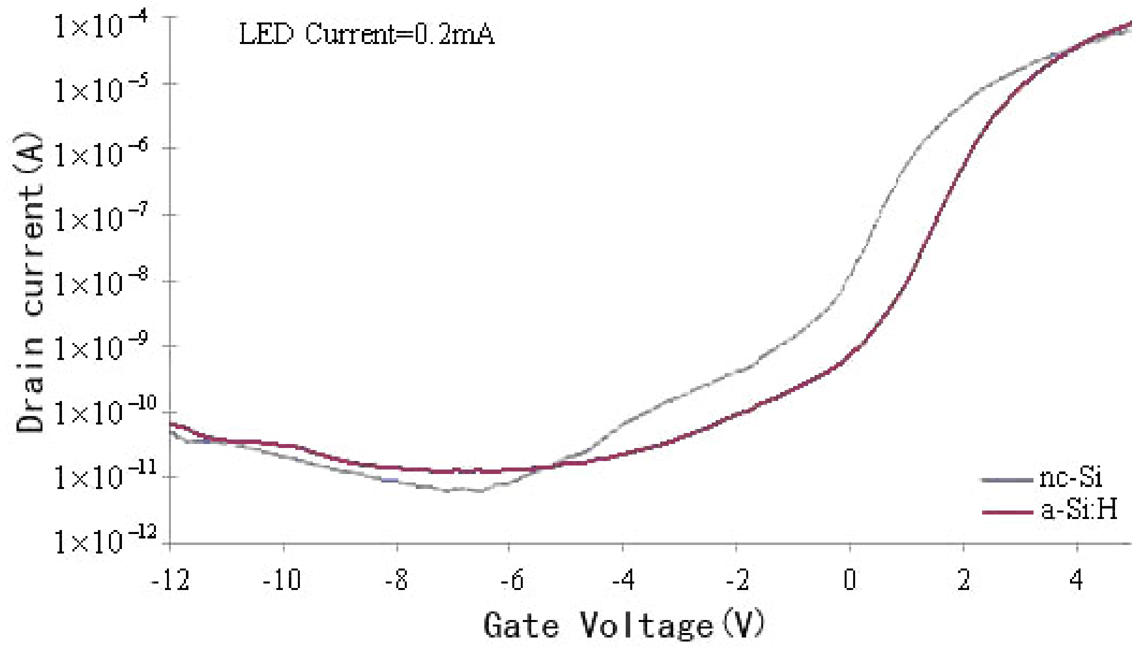


Figure 30: nc-Si Vs a-Si:H Id photo current at the LED current =0.2mA

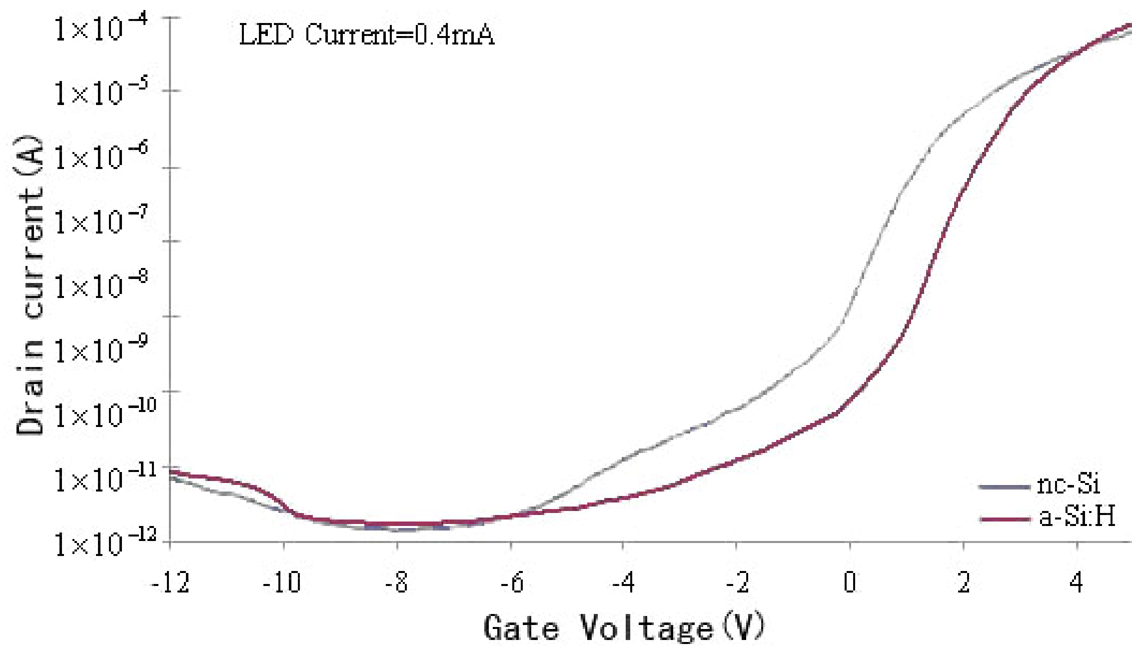


Figure 31: nc-Si Vs a-Si:H Id photo current at the LED current =0.4mA

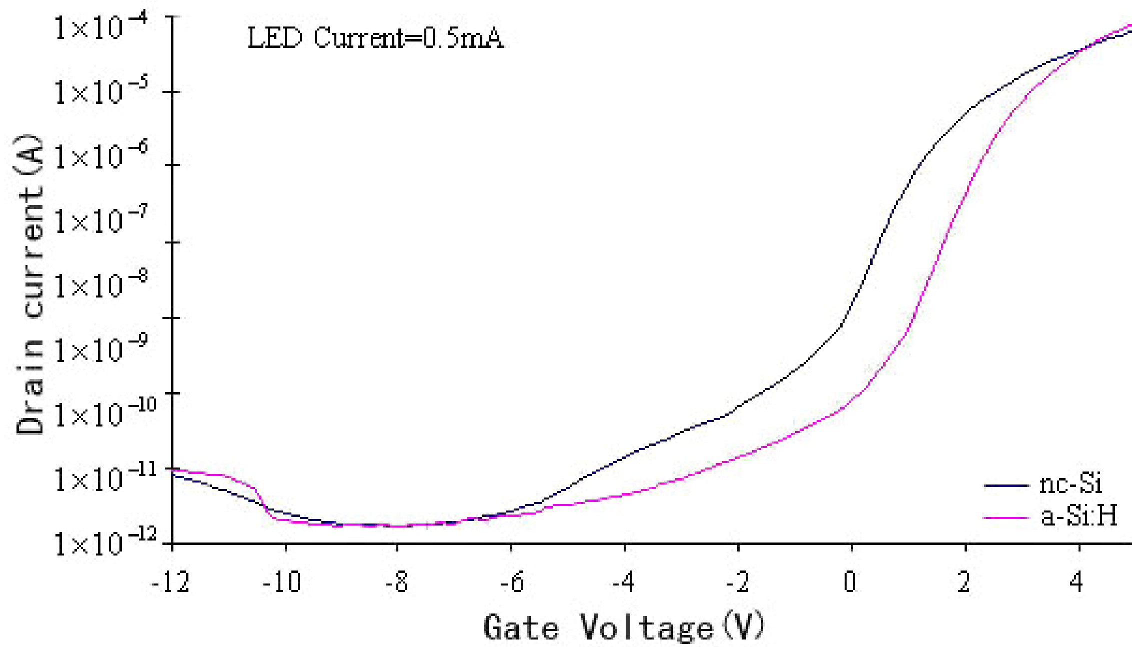


Figure 32: nc-Si Vs a-Si:H Id photo current at the LED current =0.5mA

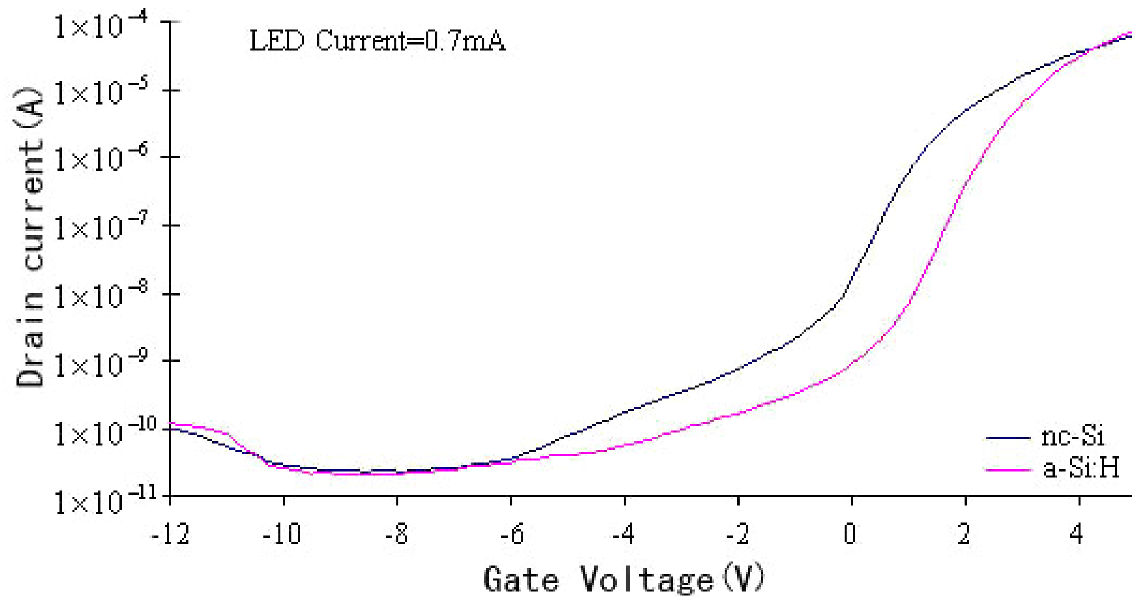


Figure 33: nc-Si Vs a-Si:H Id photo current at the LED current =0.7mA

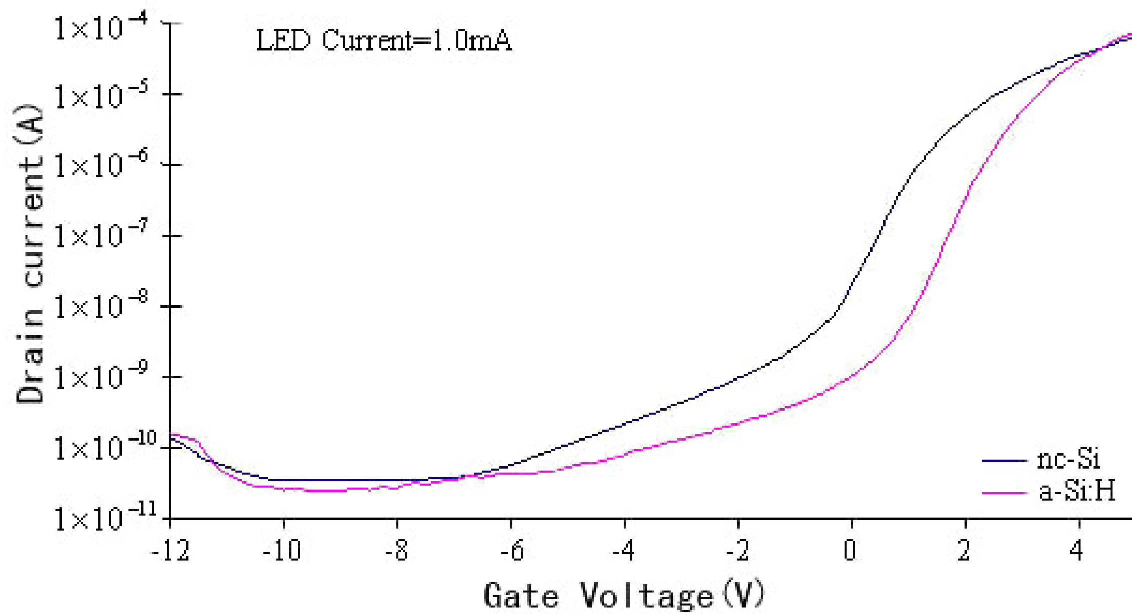


Figure 34: nc-Si Vs a-Si:H Id photo current at the LED current =1.0mA

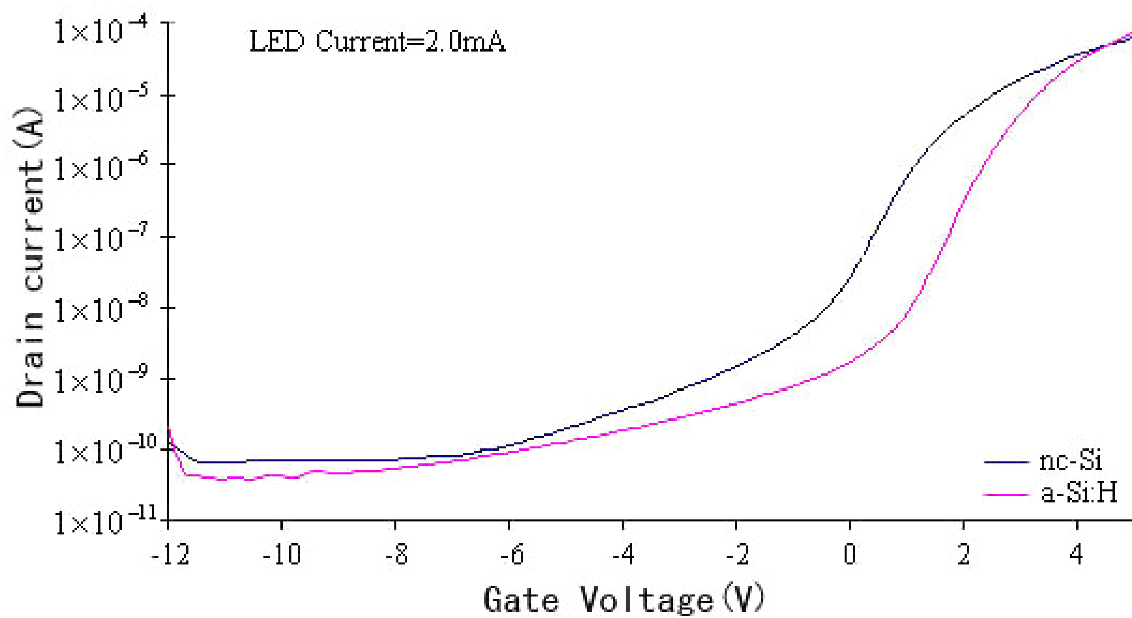


Figure 35: nc-Si Vs a-Si:H Id photo current at the LED current =2.0mA

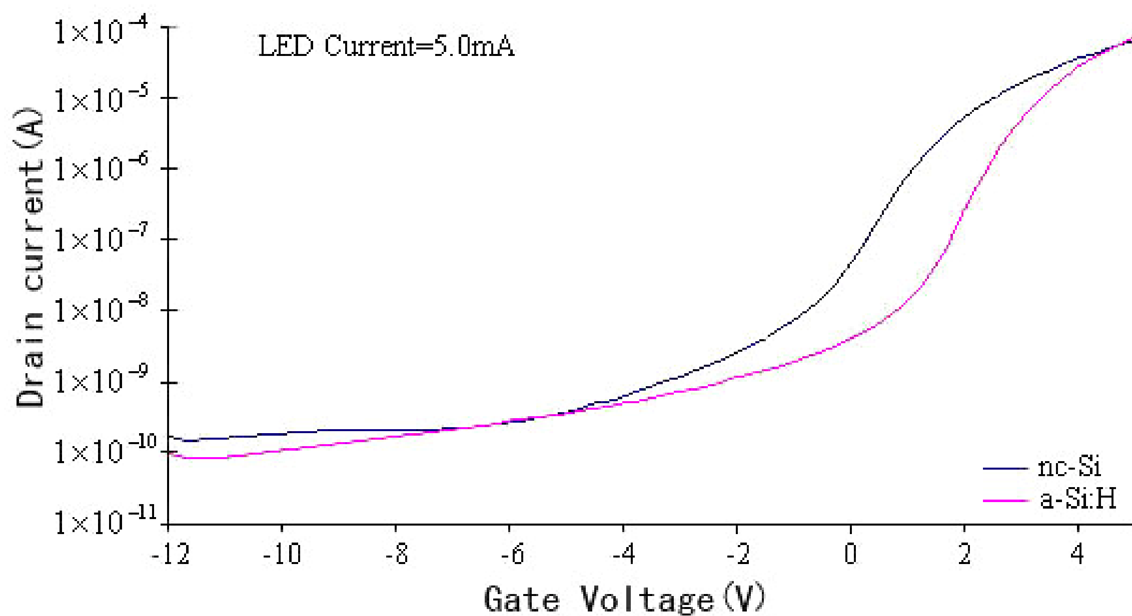


Figure 36: nc-Si Vs a-Si:H Id photo current at the LED current =5.0mA

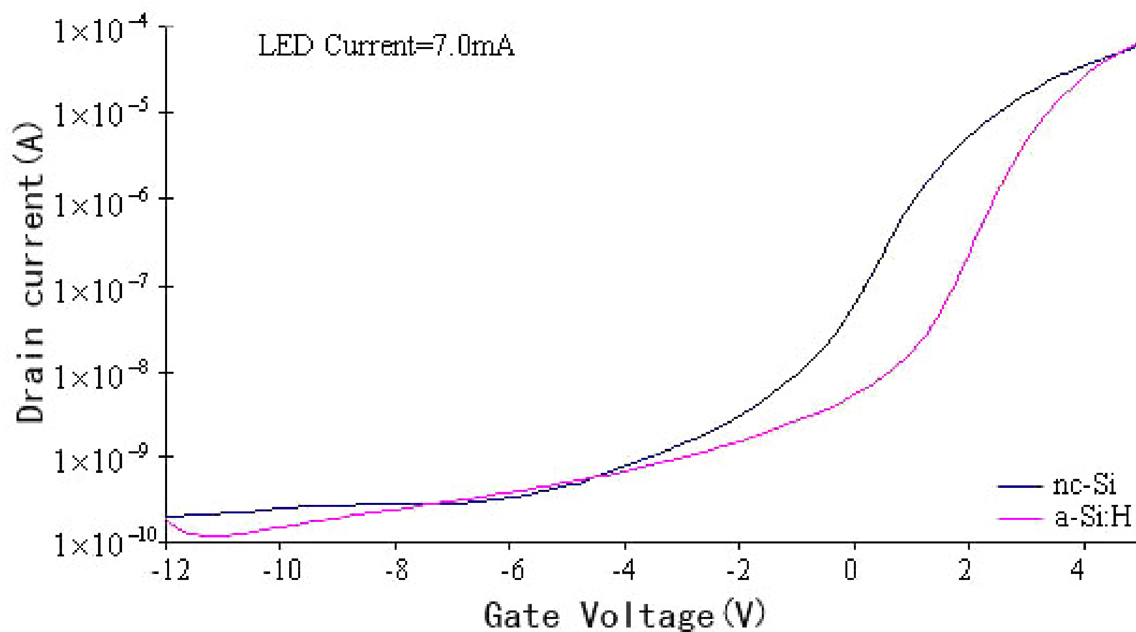


Figure 37: nc-Si Vs a-Si:H Id photo current at the LED current =7.0mA

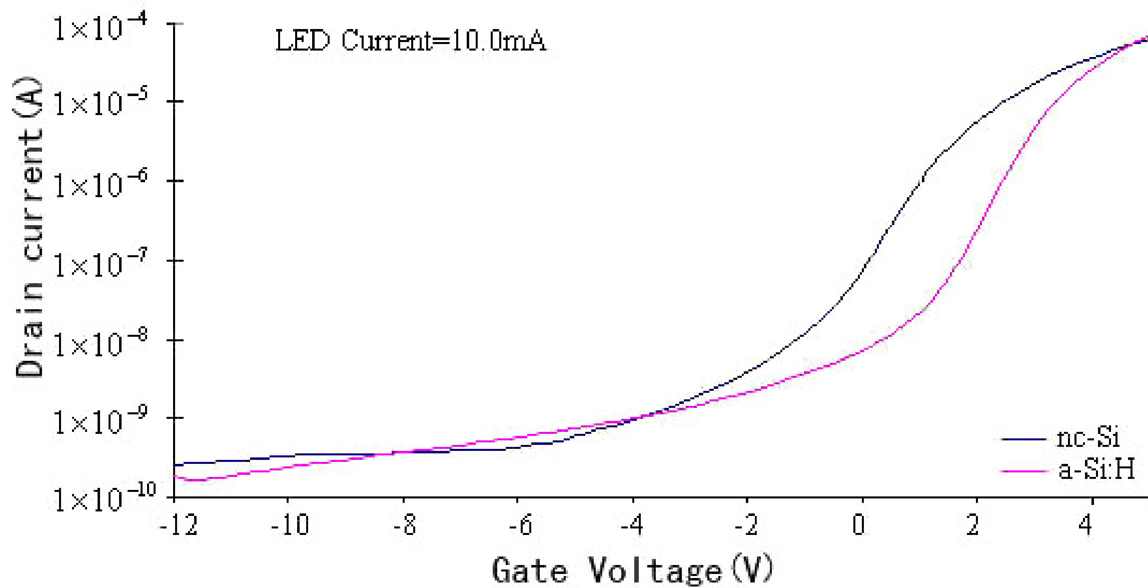


Figure 38: nc-Si Vs a-Si:H Id photo current at the LED current =10.0mA

In Figure 35, the nc-Si TFT has higher photocurrent than the a-Si:H TFT when gate voltage is from -12V to +4V under the illumination equivalent to the LED with 2.0mA current supply. In Figure 36, The nc-Si TFT has a higher photocurrent than the a-Si:H TFT when gate voltage is from -5V to +4V under the illumination equivalent to the LED with 5.0mA current supply. In Figure 37, the nc-Si TFT has higher photocurrent than the a-Si:H TFT when gate voltage is from -5V to +5V under the illumination equivalent to the LED with 7.0mA current supply. In Figure 38, the nc-Si TFT has a higher photocurrent than the a-Si:H TFT when the gate voltage is from -4V to +5V and from -12V to -8V under the illumination equivalent to the LED with 10.0mA current supply.

To get the best performance of the nc-Si TFT, from the intersection of the gate voltage range from Figure 29 to Figure 38, for the large range of illumination intensity, the nc-Si TFT only works on -4V to -3V. This section analysis only covers the photocurrent data,

which does not always reflect the highest gain and the highest quantum efficiency working ranges. However, the absolute values of the photocurrent are the important parameter for the measurement equipments. The lower current requires higher sensitivity probes, which will are probably expensive. Sometimes, if the photocurrent is too low, the practical measurement might not be possible. The following sections will discuss about the photo current gain and the quantum efficiency of the devices.

4.2.3 Analysis of the Effect of Light Intensity

Equation 4-1: $I_{DS-PD}(A) = \Phi \cdot e_0 \cdot A_{PD} \cdot QE_{PD}(\lambda)$.

Equation 4-2: $\Phi = \dfrac{I_{DS}(A)}{e_0 \cdot A_{PD} \cdot QE_{PD}(\lambda)}$,

where $e_0 = 1.6 \times 10^{-19} C$, $A_{PD} = 2 \times 2mm^2$, $QE_{PD}(\lambda) = 0.8$

Equation 4-1 is the basic equation for the diode photocurrent. The photo current is determined by the incident photo flux, the area of the contact, the quantum efficiency of the photo diode and the electron charge. The quantum efficiency of the photo diode for the experiments, which has already been measured previously, was found to be around 0.8. Use Equation 4-2, the photon flux can be calculated as shown in Figure 40 after Figure 39 has been generated. We can conclude that the light intensity linearly increases when the green LED input current increase. Therefore, the green LED input current represents the corresponding light intensity for the device.

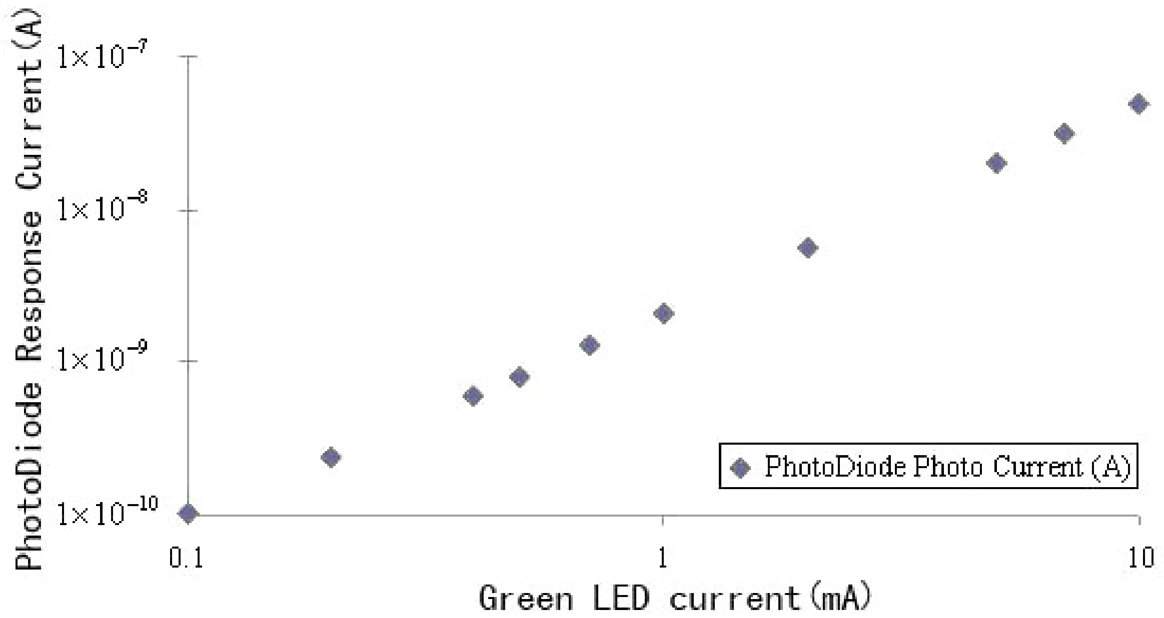


Figure 39: PhotoDiode photo current Vs Green LED current

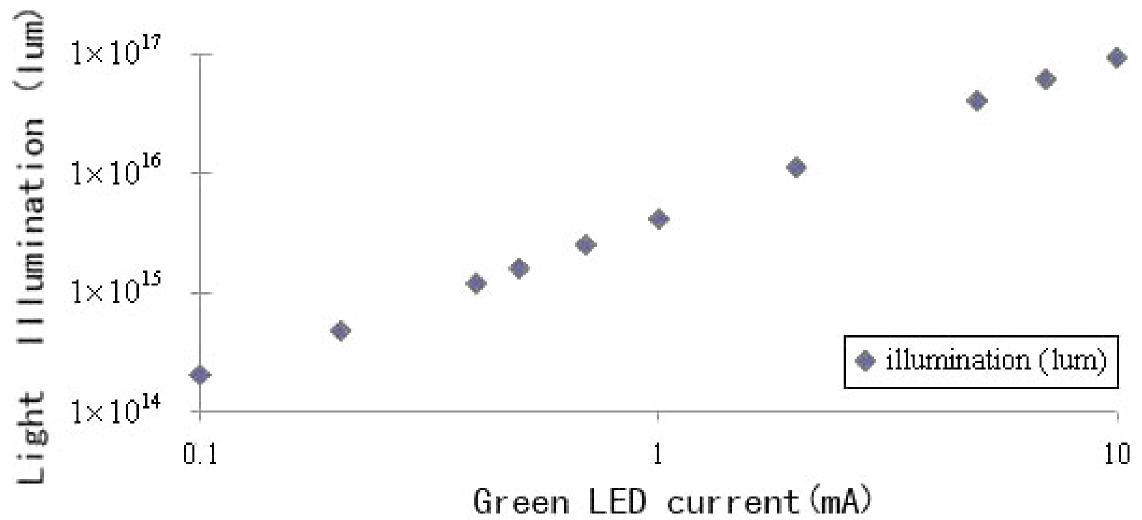


Figure 40: Light Illumination Vs Green LED current

4.2.4 Vgs Effect Analysis

In the 4.2.2, when Vg is in the range from -4 V to -3 V, the nc-Si TFT has a higher drain

current than the a-Si:H TFT for the full range of illumination of the green LED. Figure 41 has shown the a-Si:H photo transistor drain current with different Vgs. It can be concluded that the drain photo current under illumination increases when the Vg increases. With this positive correlation between the drain current and the Vg, it is easy to control the output current by adjusting the Vg.

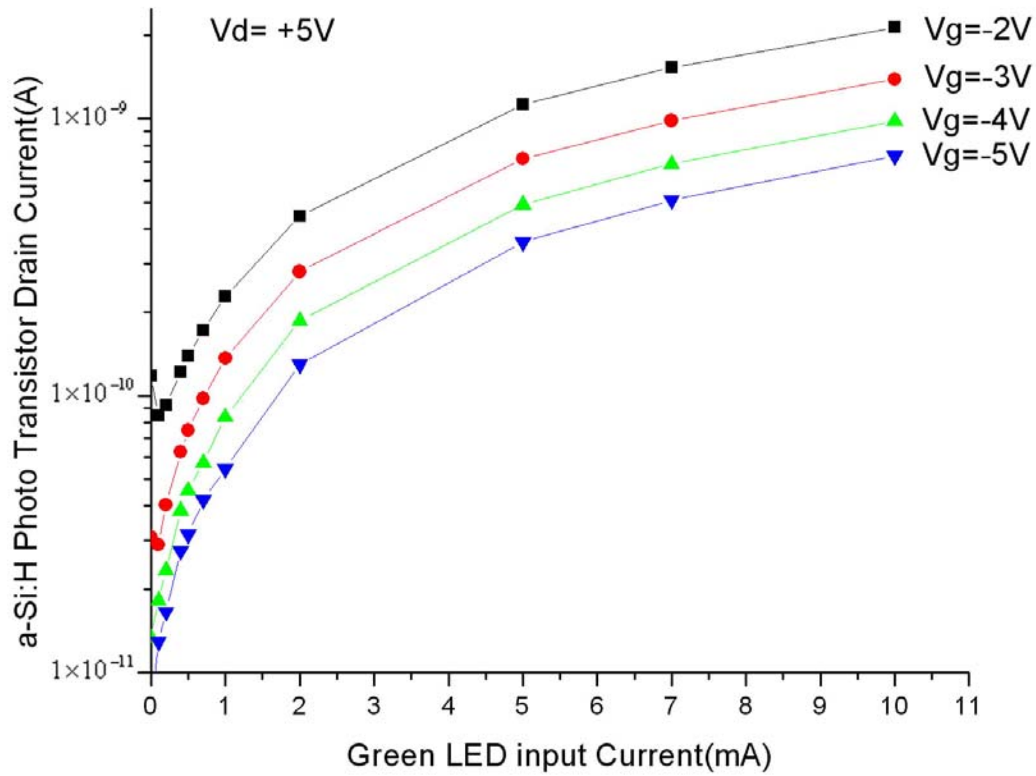


Figure 41: a-Si:H Photo Transistor Drain Current at Different Vgs

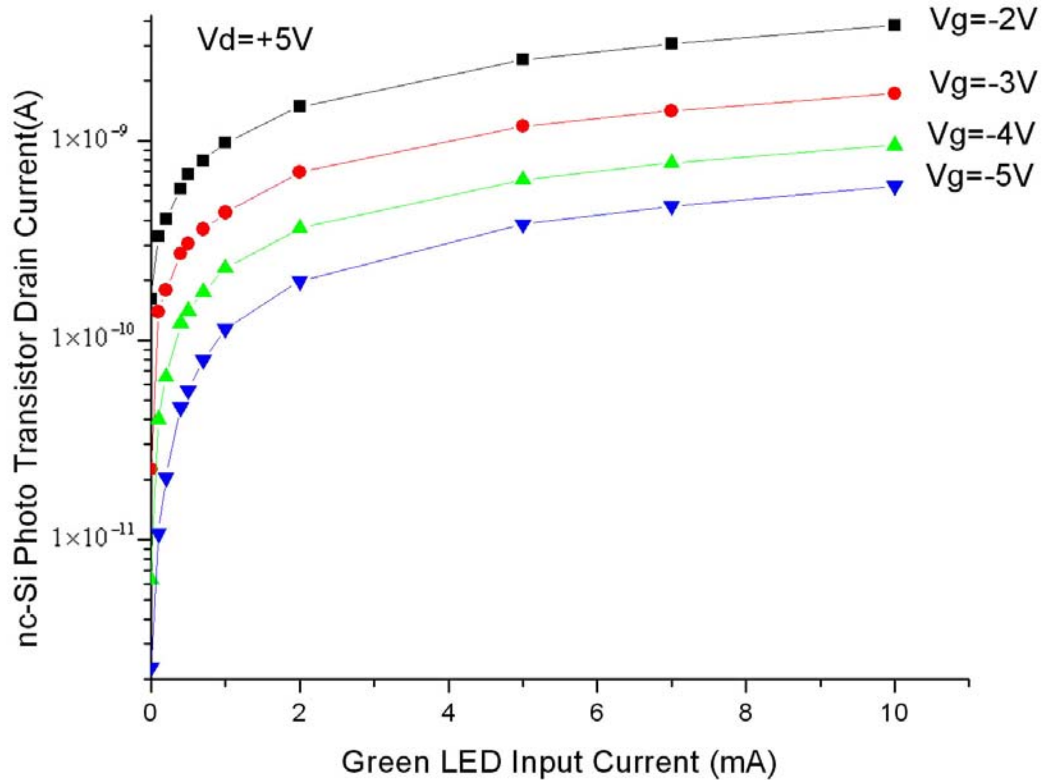


Figure 42: nc-Si Photo Transistor Drain Current at Different Vgs

Figure 42 has shown the nc-Si photo transistor drain current with different Vgs. It can be concluded that the drain photo current under illumination increases when the Vg increases. With this positive correlation between the nc-Si TFT drain current and the Vg, it is easy to control the output current by adjusting the Vg, depending on the external circuitry requirements.

4.2.5 Photo Current Gain Analysis

The photo current gain is calculated as the ratio of the photo current under illumination and the dark current of the same device. In Figure 43, to achieve the maximum photo current gain, the gain bias voltage of the a-Si:H has to be around -5 V. If we want to achieve the

photo current gain higher than 1, the gate bias voltage range must be in between -8 V and -3 V roughly. When the gate voltage is higher than -3 V, the output current becomes less than the input current. Therefore, the photo transistor gain is less than one when the gate voltage is greater than -3 V, which region was not adopted in our further measurement. Because in the subthreshold region, incident lights will create more defects close to the electronic tunnel which is created by Vg, the total current will be less than the dark current.

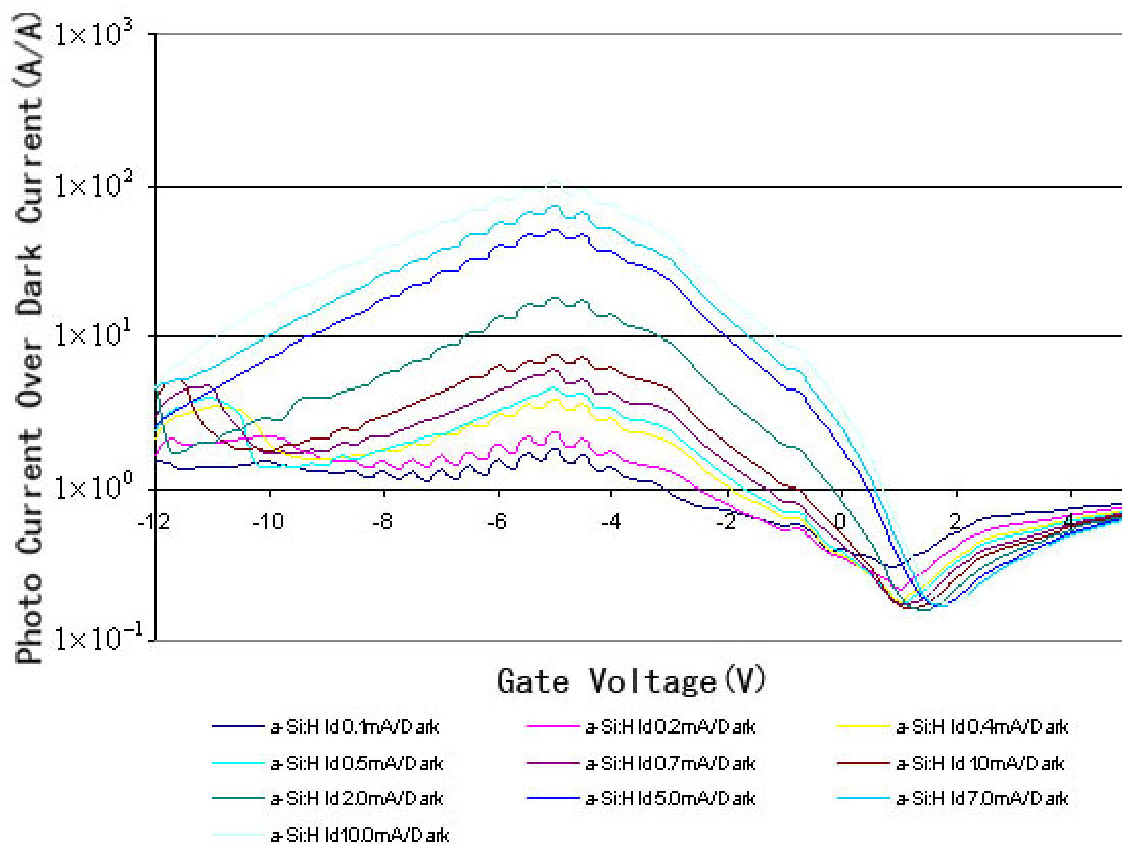


Figure 43: The a-Si:H Photo Current Gain

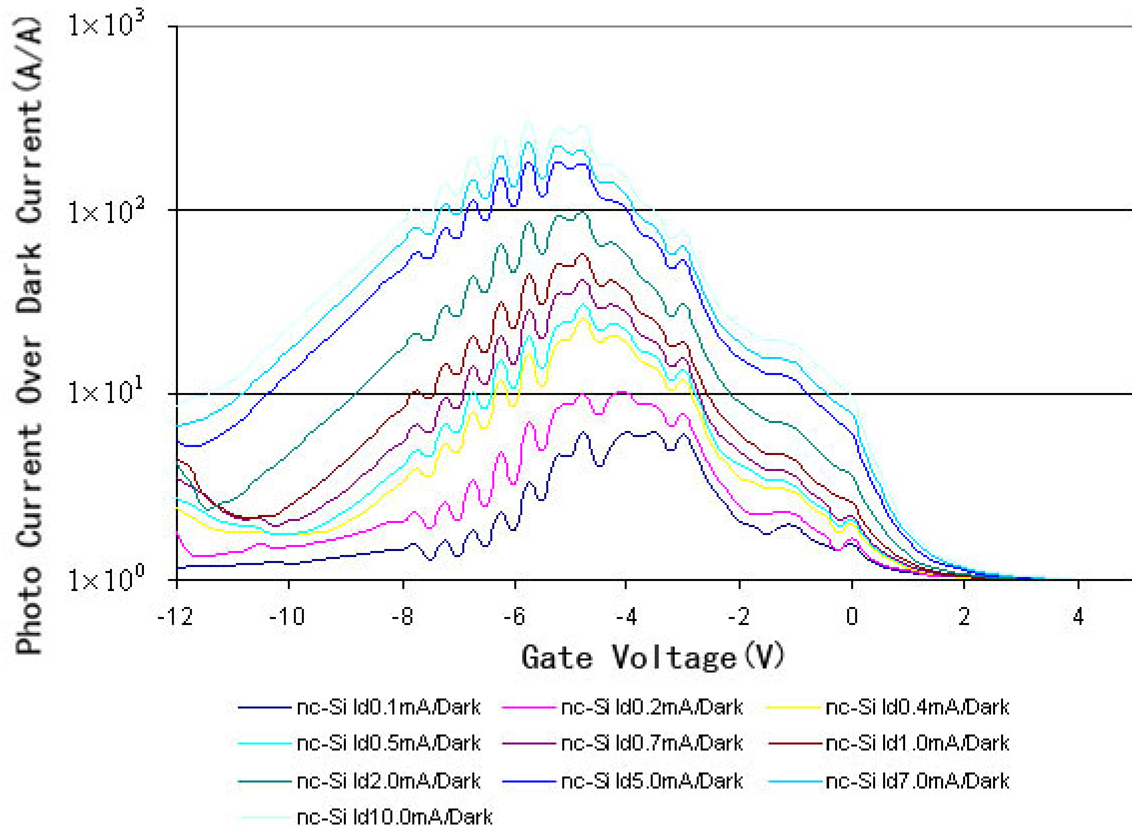


Figure 44: The nc-Si TFT Photo Current Gain

In Figure 44, to achieve the maximum photo current gain, the gate voltage of the nc-Si has to be around -5 V. If we want to achieve the photo current gain more than 1, the gate voltage range will be from -10 V to +3 V roughly. When the gate voltage is higher than +3 V, the output current becomes undistinguishable.

Because both devices have the maximum photo current gain when the gate voltage is around -5 V, using the ratio of the devices' gain will help to find the better device. As seen in Figure 45, the ratio is greater than 1 when the gate voltage is from -8 V to -2 V and from -2 V to 4 V. However, from Figure 43, when the gate voltage is greater -3 V, the a-Si:H TFT actually does not amplify the signal. Therefore, the range from -8 V to -2 V is where are

more reasonable. Figure 46 is the zoom-in graph of the photo current gain ratio. It can be seen that when the gate voltage is from -5.5V to -4.6, the nc-Si TFT has better performance than the a-Si:H TFT at least twice the magnitude for the full range 0-10mA LED current. Some ripples can also be observed when gate voltage is from -8 V to -4 V because the dark current measurement has stronger noise due the low value.

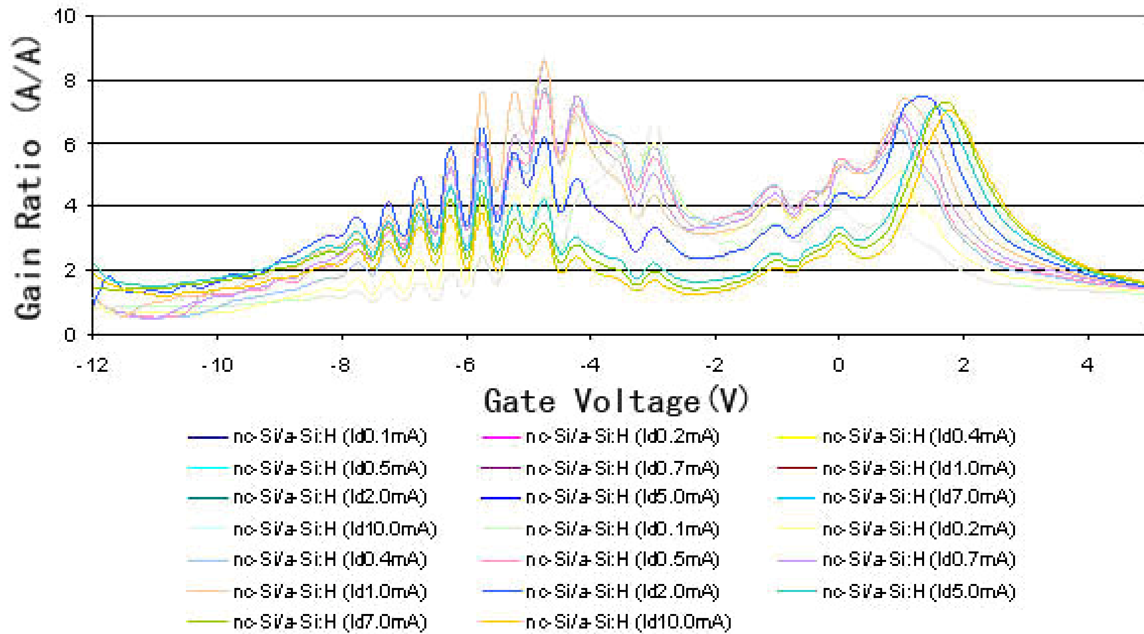


Figure 45: the ratio of the nc-Si device current gain over the a-Si:H device current gain

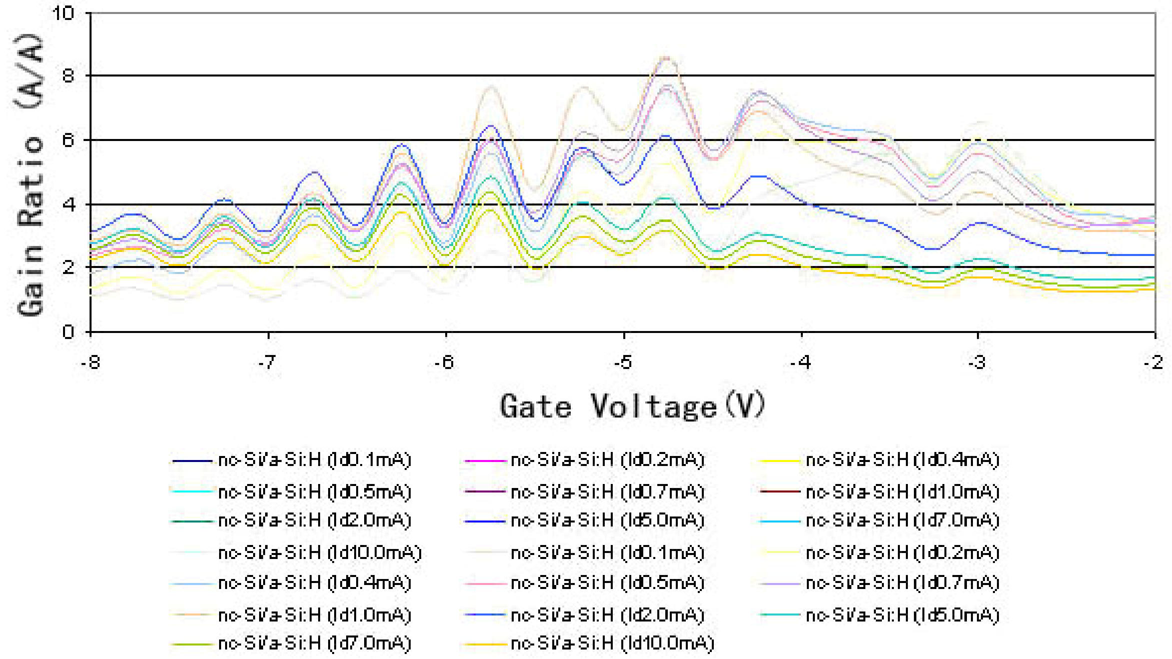


Figure 46: ratio of the nc-Si device current gain over the a-Si:H device current gain(Zoom in)

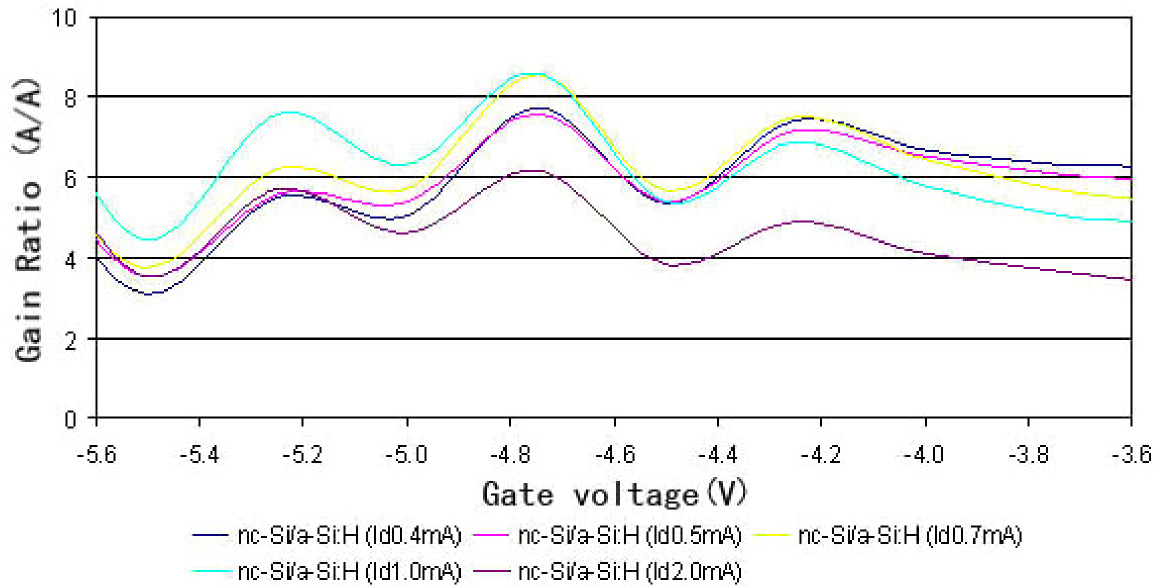


Figure 47: ratio of the nc-Si device current gain over the a-Si:H device current gain(Zoom in)

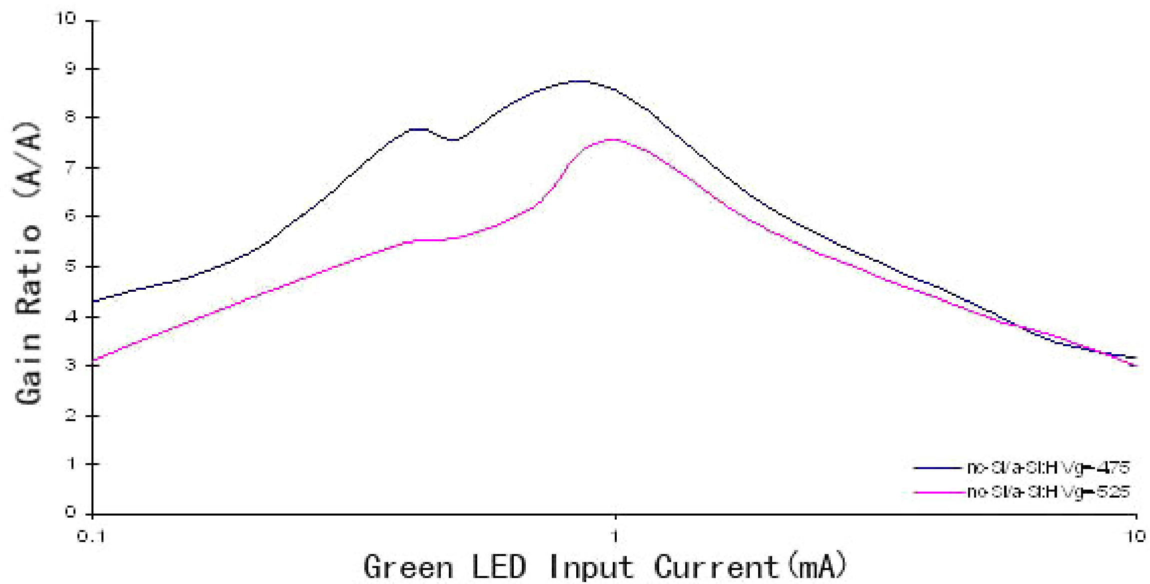


Figure 48: Photo Current Gain Ratio (nc-Si/a-Si:H) when Vg=-4.75V and Vg=-5.25V

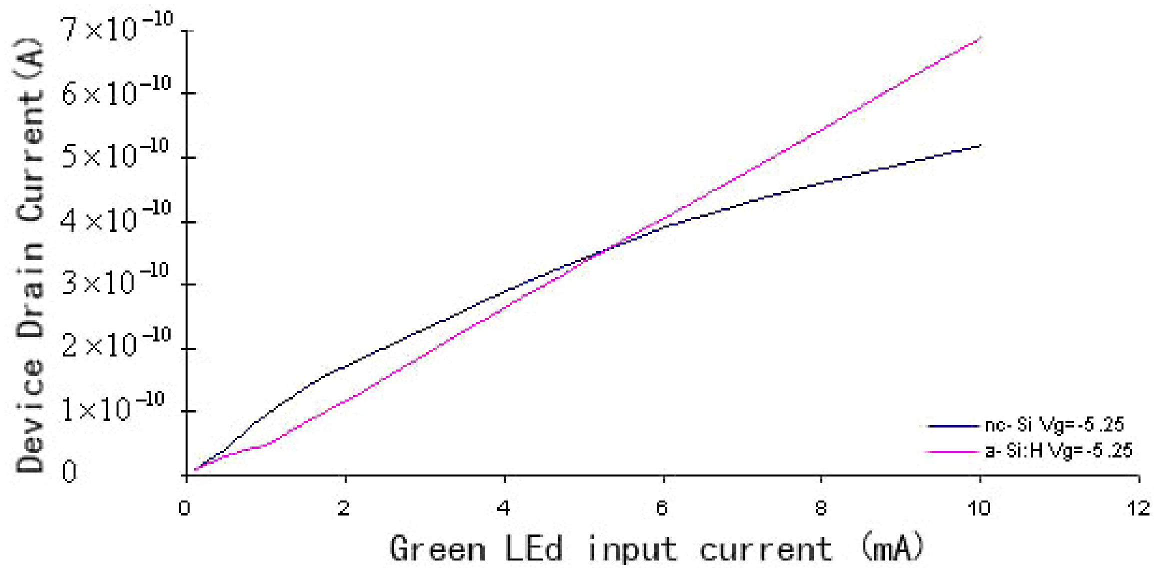


Figure 49: Comparison of the nc-Si TFT and the a-Si:H TFT drain current when Vg=-5.25V

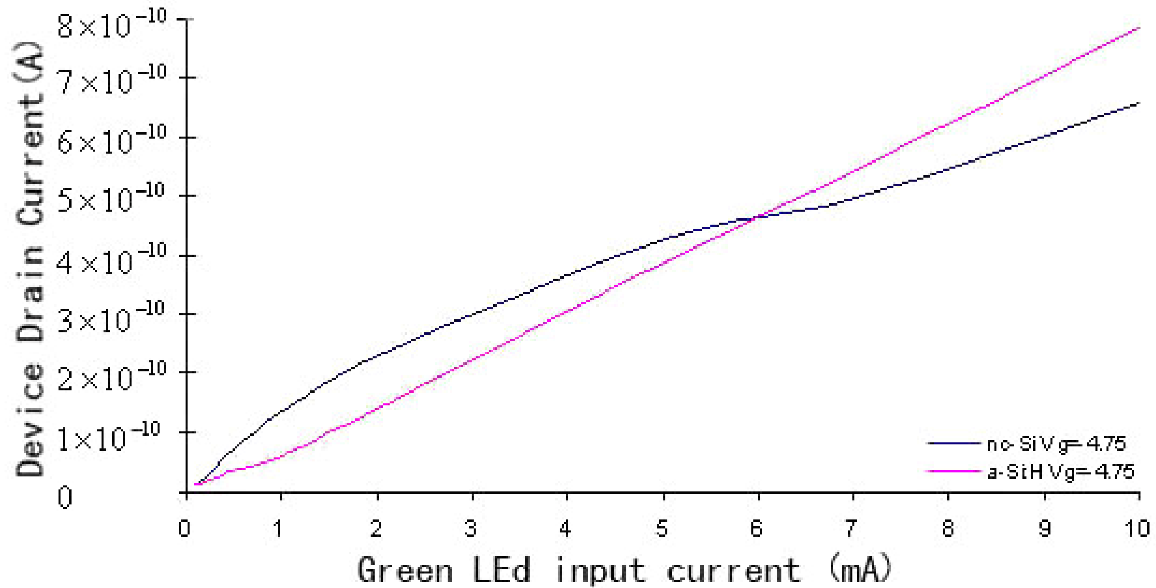


Figure 50: Comparison of the nc-Si TFT and the a-Si:H TFT drain current when Vg=-4.75V

In Figure 47, when the gate voltage is from -4.9V to -4.65V and -5.3V to -5.1V, the nc-Si TFT has better performance than the a-Si:H TFT by at least five times the magnitude when the LED current is in the range of 0.4mA to 2mA. In Figure 48, when the gate voltage is -4.75V to -5.25V, the nc-Si TFT has at least three times the magnitude as the a-Si:H TFT when the LED current is in the range of 0.1mA to 10mA. As shown in Figure 49 and Figure 50, the values of the photo current for both devices are very close when different light magnitudes have been applied. This indicates that the reason that the nc-Si TFT has better photo current gain is because the nc-Si TFT has lower dark current when the gate voltage is around -5 V.

We can conclude that the nc-Si TFT has better photo current gain only for the light magnitude equivalent to the source LED input current in the range of 0.4mA to 2mA. In other words, this device achieves better photo current gain than the a-Si:H device only for

low illumination light within a certain range, as we have discussed before.

4.2.6 Analysis of the Effect of Vds

Figure 51 has shown the relation between the nc-Si TFT dark current and the Vds. The correlation is not a simple positive or negative. The graph indicates that the correlation is positive when the Vd increases from 1 V to a certain voltage. Then the correlation becomes negative when the Vd decreases from that voltage to 10 V. From the practical method, the Vd is set to 5 V. The graph shows that when the Vd equals 5 V, the dark current is the highest.

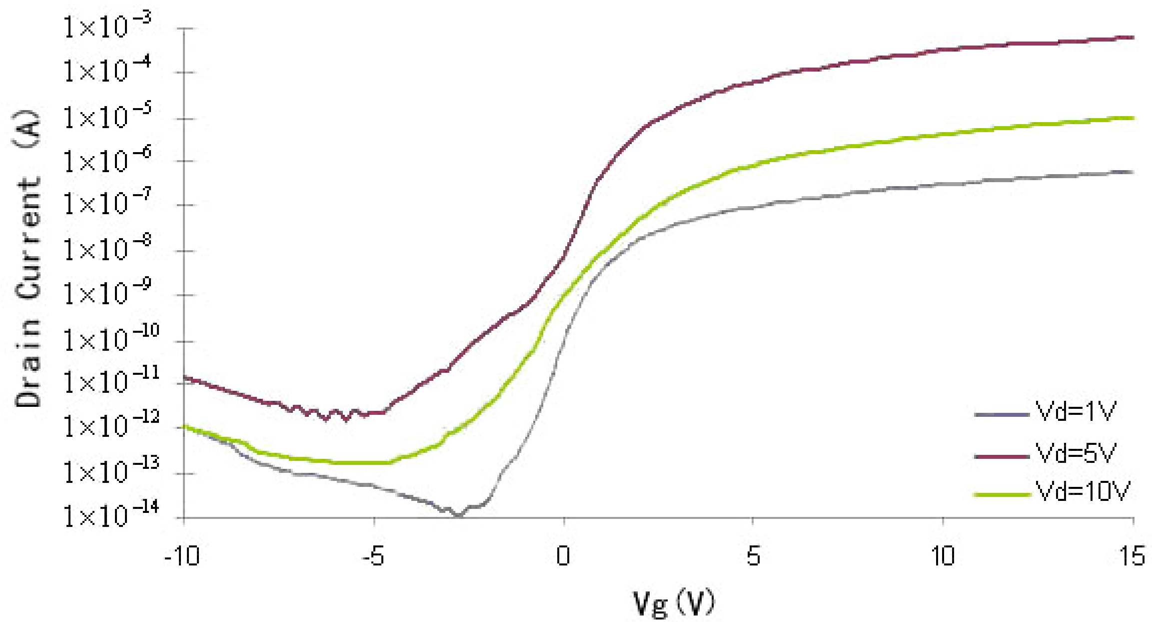


Figure 51: nc-Si TFT Dark Current with Different Vds

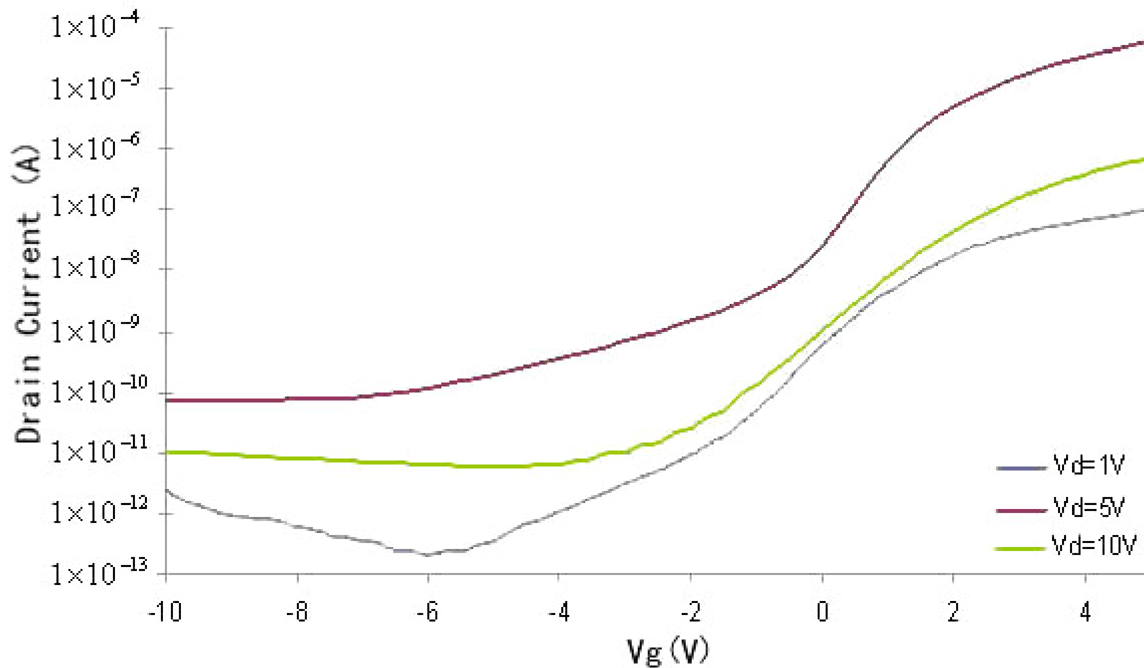


Figure 52: nc-Si TFT Current under Illumination with Different Vds

Figure 52 has shown the relation between the nc-Si TFT photo current under illumination and the Vds. Similar to what we saw for a-Si:H photo-TFTs, the graph indicates that the correlation is positive when the Vd increases from 1 V to a certain voltage. Then the correlation becomes negative when the Vd decreases from that voltage to 10 V. From the practical method, the Vd is set to 5 V. The graph shows that when the Vd equals 5 volt, the photo current is the highest. Based on these information, all other photo current data results were collected when the Vd was 5 V.

4.2.7 Quantum Efficiency Analysis

From 4.2.3, the light intensity can be calculated from the measured results. Equation 4-3 and Equation 4-4 are given as followings.

Equation 4-3: $I_{DS-PT}(A) = \Phi \cdot e_0 \cdot A_{PT} \cdot QE_{PT}(\lambda)$

Equation 4-4: $QE_{PT}(\lambda) = \dfrac{I_{DS-PT}(A) \cdot A_{PD} \cdot QE_{PD}(\lambda)}{I_{DS-PD}(A) \cdot A_{PT}}$

where $e_0 = 1.6 \times 10^{-19} C$, $A_{PD} = 2 \times 2mm^2, QE_{PD}(\lambda) = 0.8$, $A_{PT} = 592 \times 99um^2 = 0.0586mm^2$

From these two equations, the quantum efficiency of the nc-Si TFT and the a-Si:H TFT can be calculated for different Vgs, -5.25V, -4.75V, -4V, -3V, -2V, -1V, 0V, +1V and +1.5V.

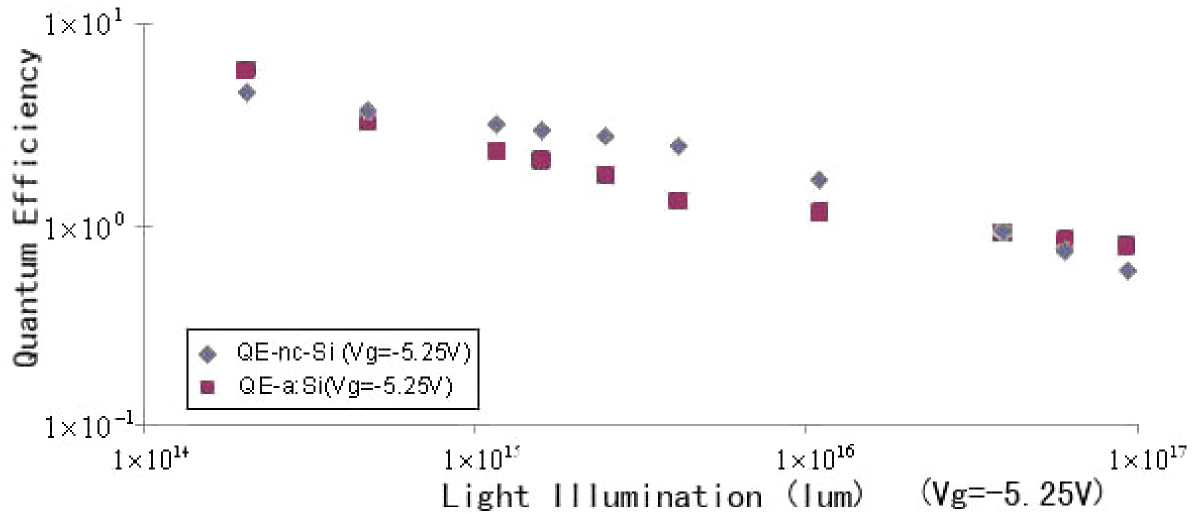


Figure 53: Light Illumination Vs Quantum Efficiency when Vg=-5.25V

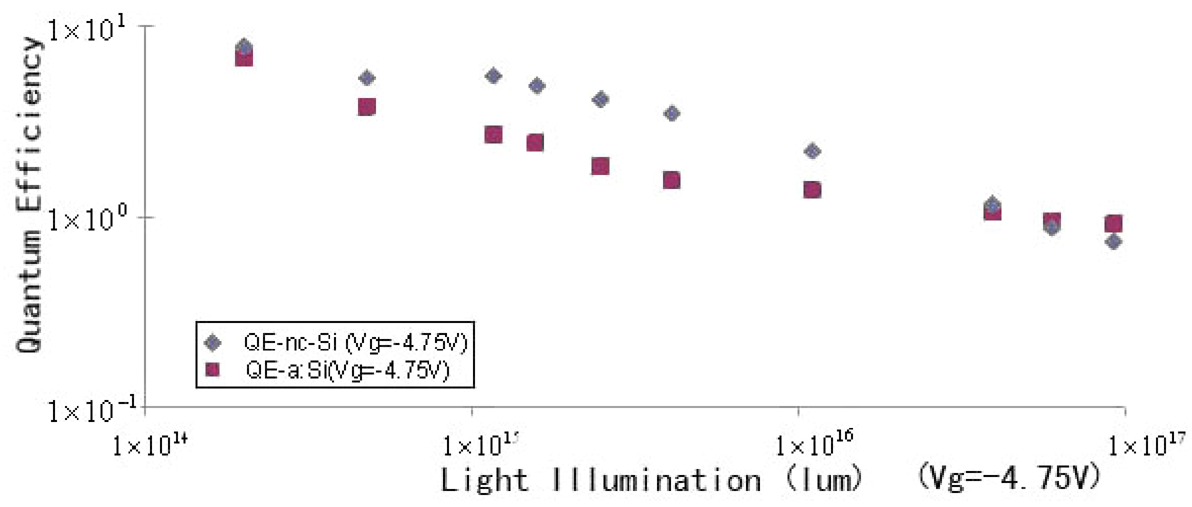


Figure 54: Light Illumination Vs Quantum Efficiency when Vg=-4.75V

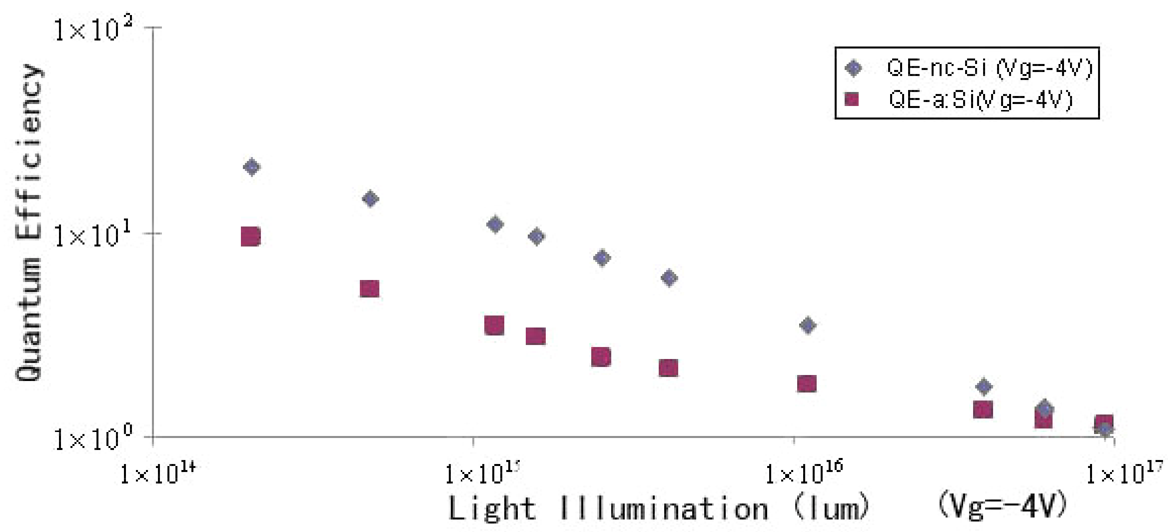


Figure 55: Light Illumination Vs Quantum Efficiency when Vg=-4V

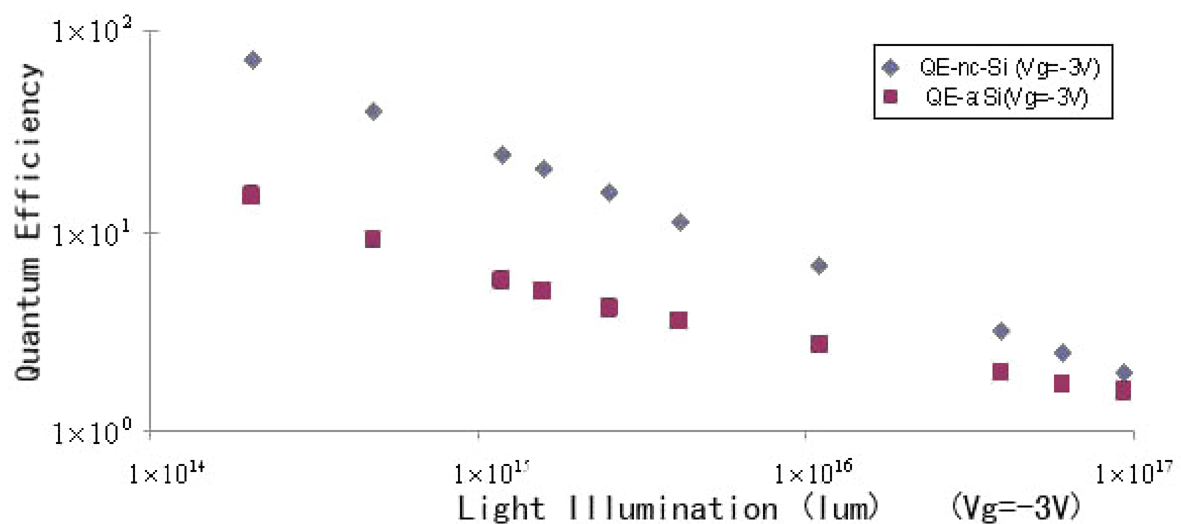


Figure 56: Light Illumination Vs Quantum Efficiency when Vg=-3V

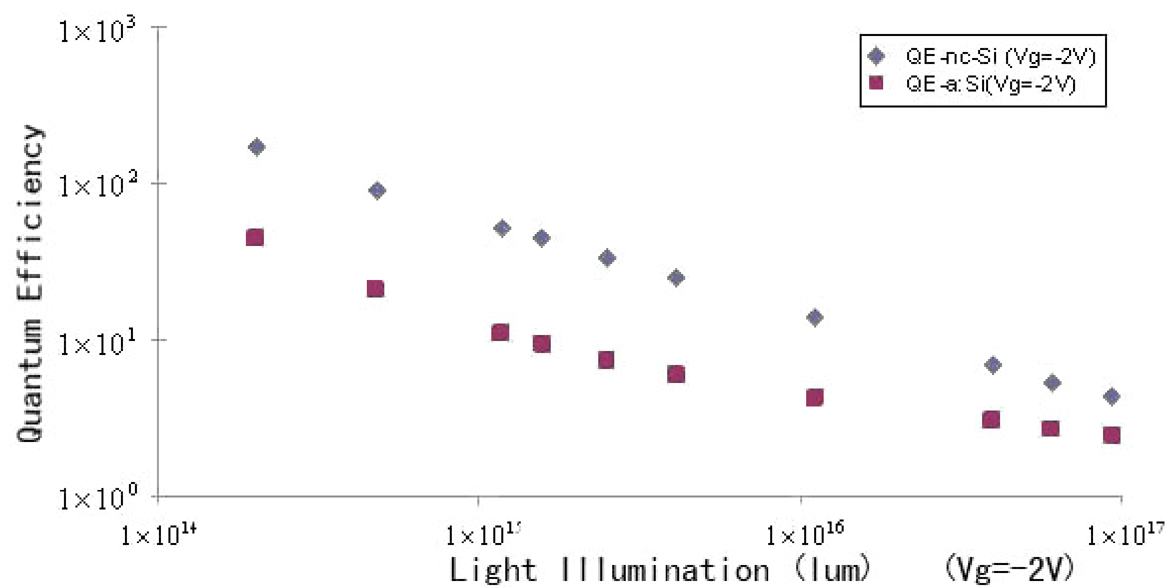


Figure 57: Light Illumination Vs Quantum Efficiency when Vg=-2V

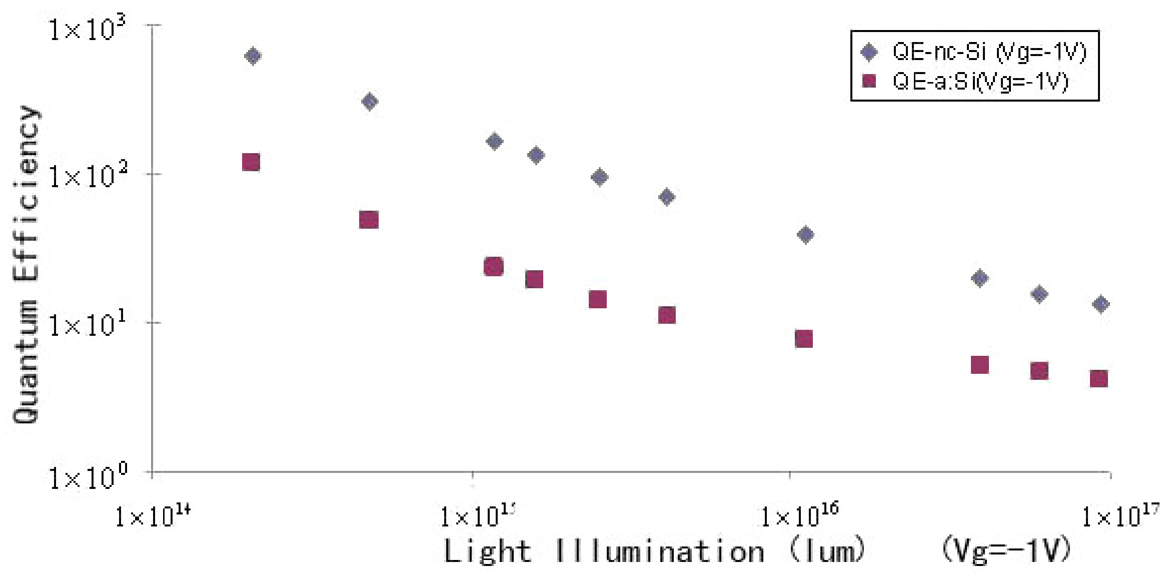


Figure 58: Light Illumination Vs Quantum Efficiency when Vg=-1V

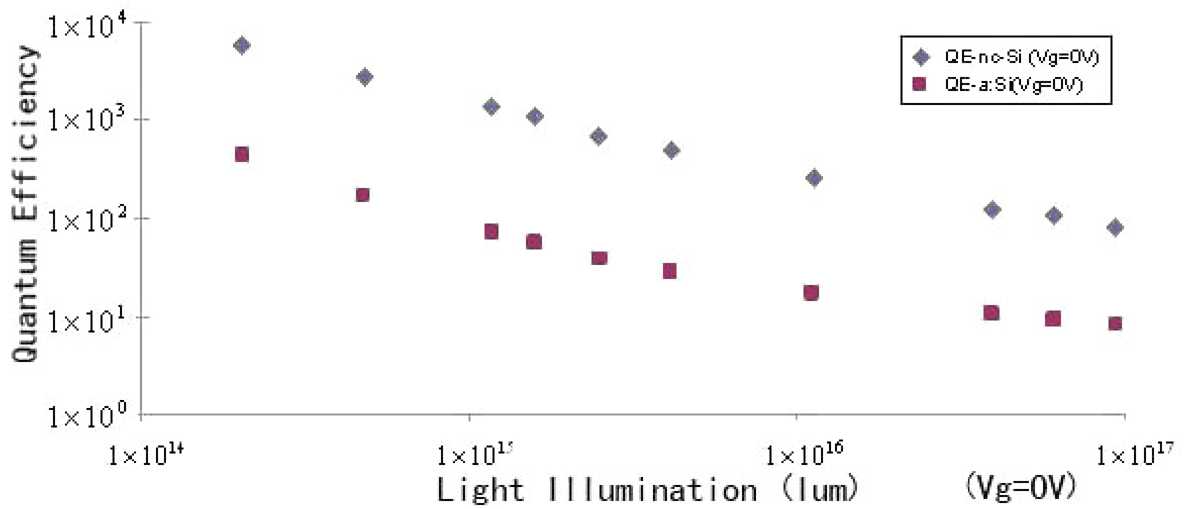


Figure 59: Light Illumination Vs Quantum Efficiency when Vg=0V

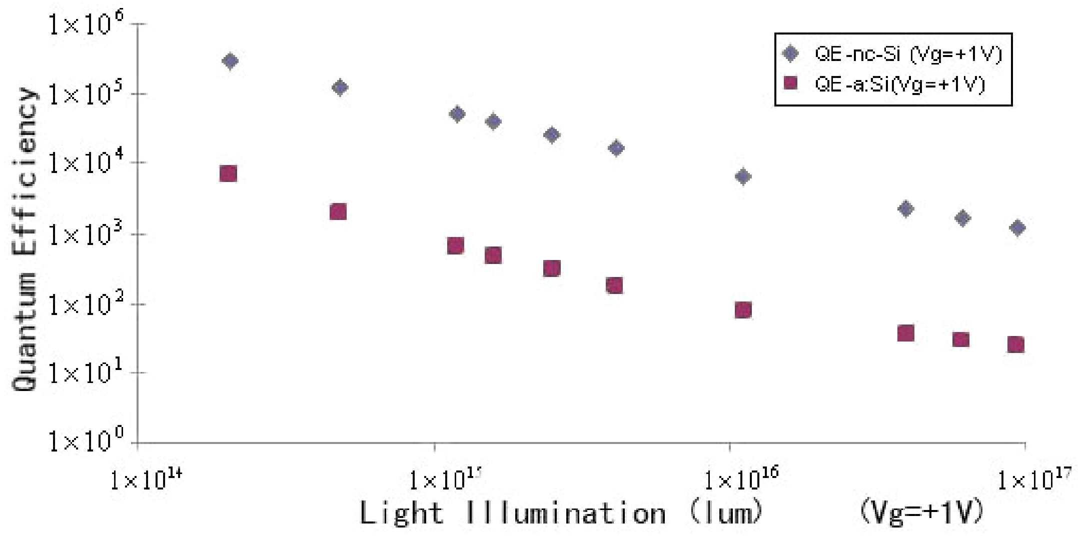


Figure 60: Light Illumination Vs Quantum Efficiency when Vg=+1V

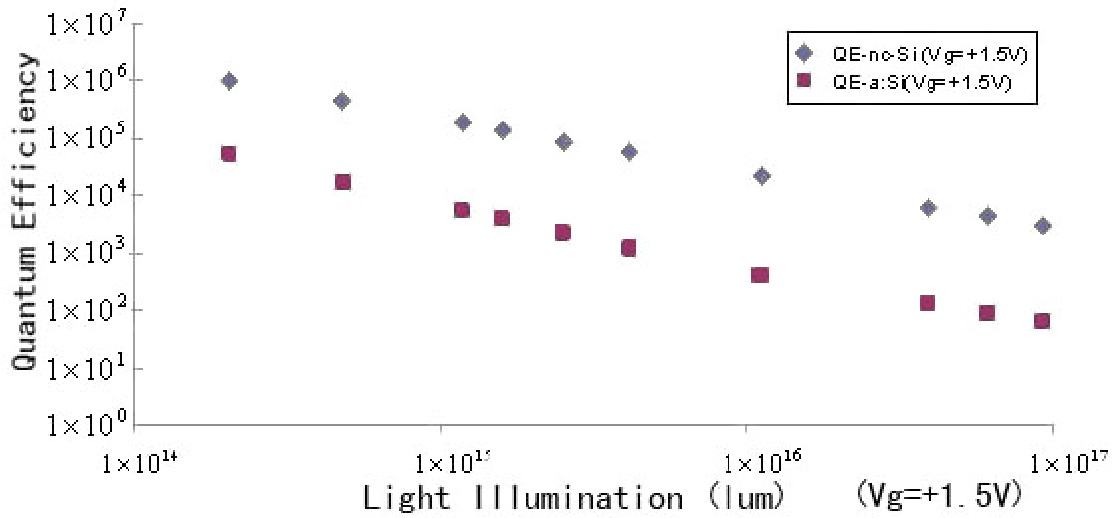


Figure 61: Light Illumination Vs Quantum Efficiency when Vg=+1.5V

With these calculations, from Figure 55 to Figure 61, the results have shown that the nc-Si TFT always has higher quantum efficiency than the a-Si:H TFT. As we have discussed, since the nc-Si TFT always works on the negative bias gate voltage, as discussed in section 3.1, the summary of the quantum efficiency of the nc-Si TFT is shown in Figure 63. The summary of

the quantum efficiency of the a-Si:H TFT is shown in Figure 62. When the Vg equals 0 V, the nc-Si TFT gets its best quantum efficiency. This value is better than the value of the a-Si:H TFT when the Vg equals 1 V. But it is worse than the one of the a-Si:H TFT when the Vg equals 1.5 V. In section 4.2.8, the relation of the quantum efficiency, the photo current gain, the Vg and the Vd will be discussed more.

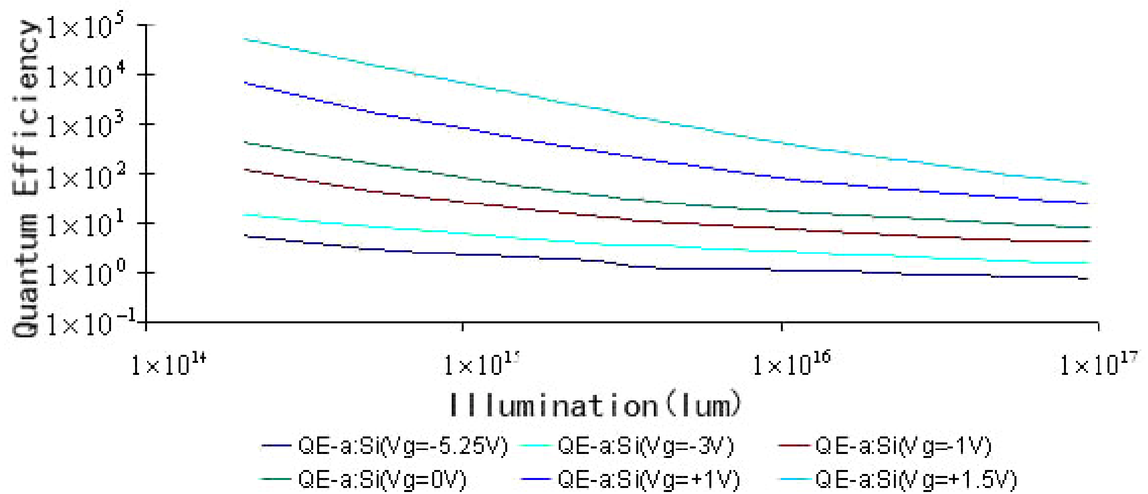


Figure 62: a-Si:H Quantum Efficiency with different gate voltages

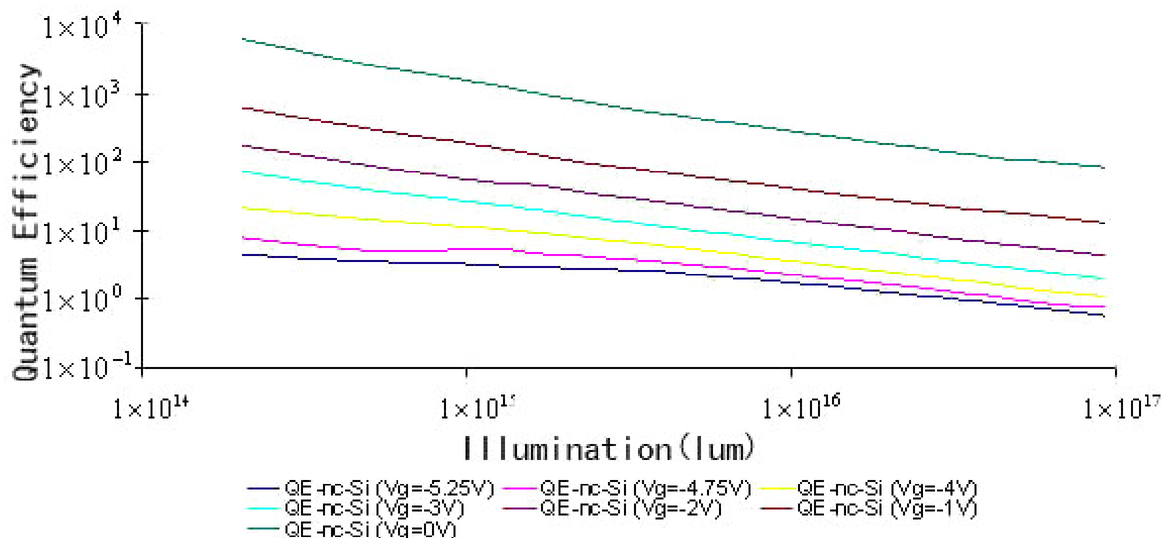


Figure 63: nc-Si Quantum Efficiency with different gate voltages

4.2.8 Effect of Vds, Vgs on Quantum Efficiency & Photo Current Gain Analysis

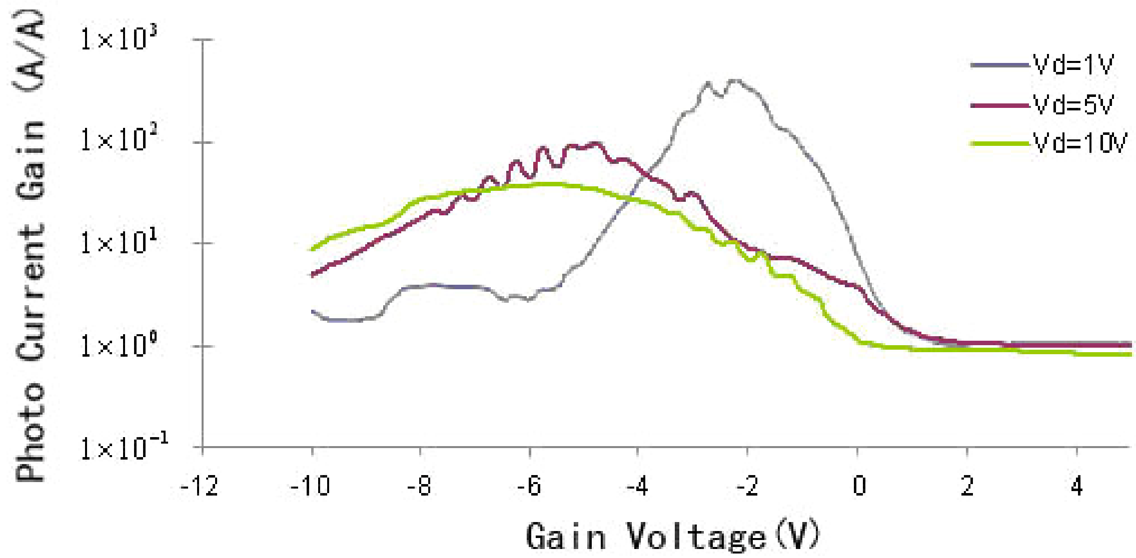


Figure 64: nc-Si Gain Vs Vds

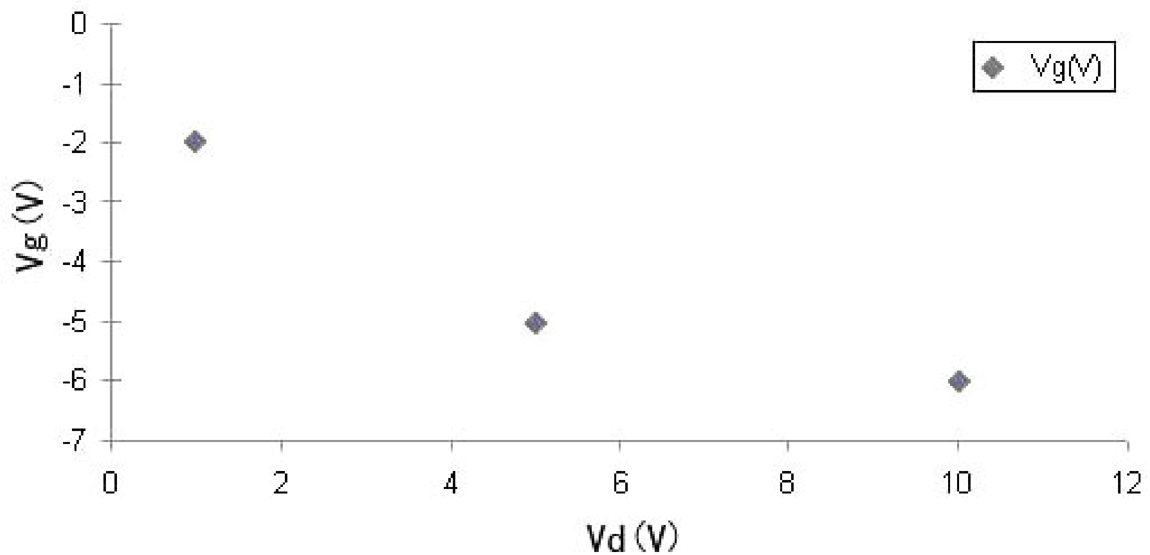


Figure 65: Vd Vs Vg at nc-Si Device Maximum Photo Current Gain

With the increasing of the Drain-source voltage from 1V to 10V, the gate voltage, where

the photo current maximum gain of the nc-Si TFT occurs, is decreasing from -2V to -6V. Therefore, the Vg has a negative correlation with the Vd, in respect to the maximum photo current gain.

From Equation 4-4, the following relation can be obtained.

Equation 4-5: $QE_{PT} \propto I_{DS-PT} \propto V_{ds}$

For a certain quantum efficiency of the nc-Si TFT, the QE always has the positive correlation with the Vd. The virtual relation has been drawn in Figure 66. The relation of Vd, Vg, photo current maximum gain and quantum efficiency has shown in Figure 67.

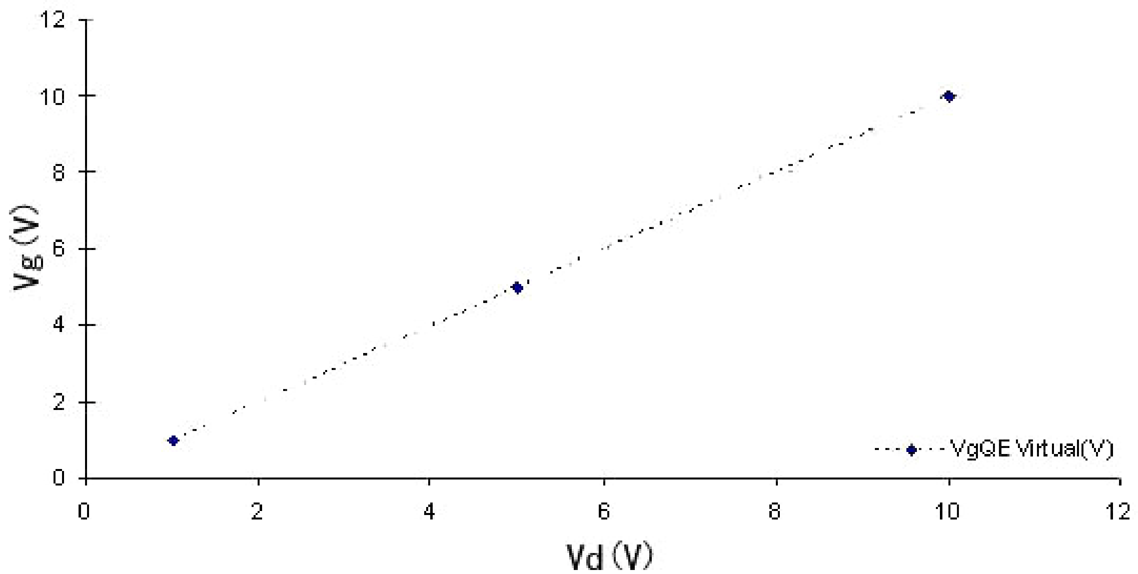


Figure 66:The relation between Vd and Vg at QE(A/A)=constant

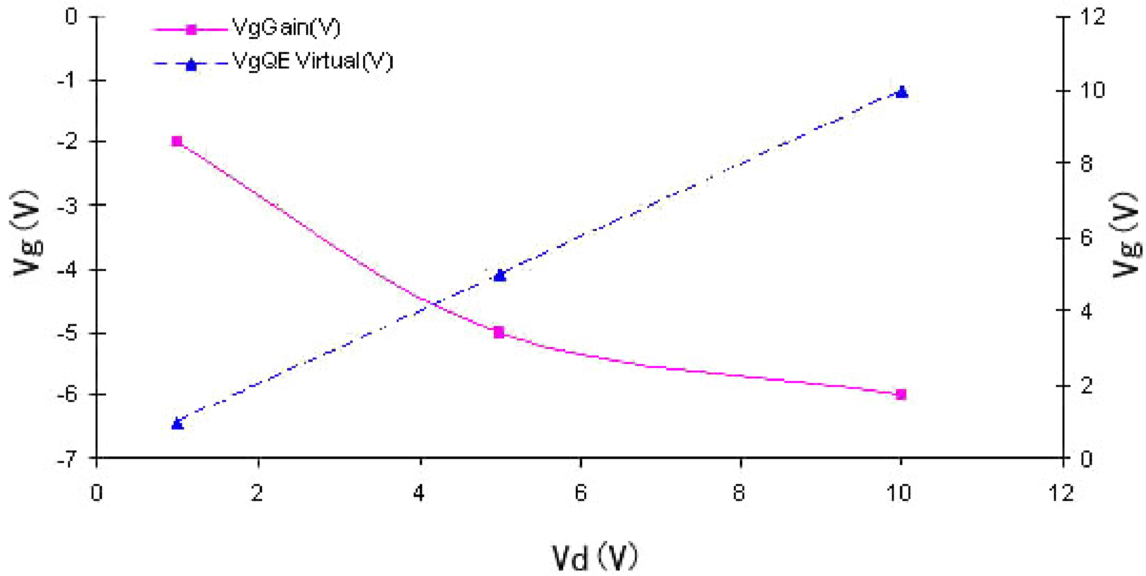


Figure 67:Estimation Vds effect of Maximum Photo Current Gain and Quantum Efficiency

According to Figure 67, if the nc-Si TFT requires a higher gain, the drain/source voltage of the device should be smaller. If the nc-Si TFT requires to produce higher quantum efficiency, the drain/source voltage of the device should be higher. If the nc-Si TFT requires the optimal gain and quantum efficiency, the drain/source voltage of the device should be somewhere in the middle (around 4V).

4.3 Stability Analysis

The nc-Si TFT is more stable than the a-Si:H TFT as shown in Figure 68. A well accepted stretched-exponential model for the nc-Si TFT has been used to verify the stability of the device. The parameters have been extracted as in Equation 4-6.

Equation 4-6: $\Delta V_T = C \cdot (1 - \exp[-\frac{t}{\tau}]^{\beta})$ [10]

where $C = 2.15V; \tau = 7549hr; \beta = 0.3$ [25]

The comparisons of the simulation results and the experimental results are given in Figure 69. It is clear that the experimental results match the simulation result very well. We can conclude that the nc-Si TFT is very stable. All the measurement results can be repeatable.

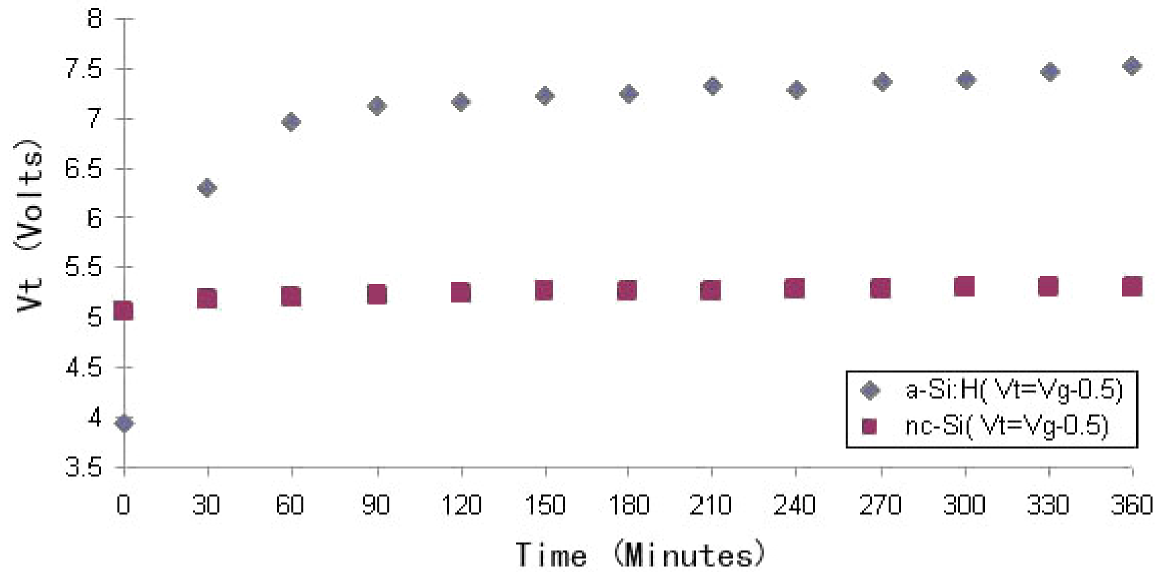


Figure 68: Threshold voltage shift of nc-Si TFT and a-Si:H TFT

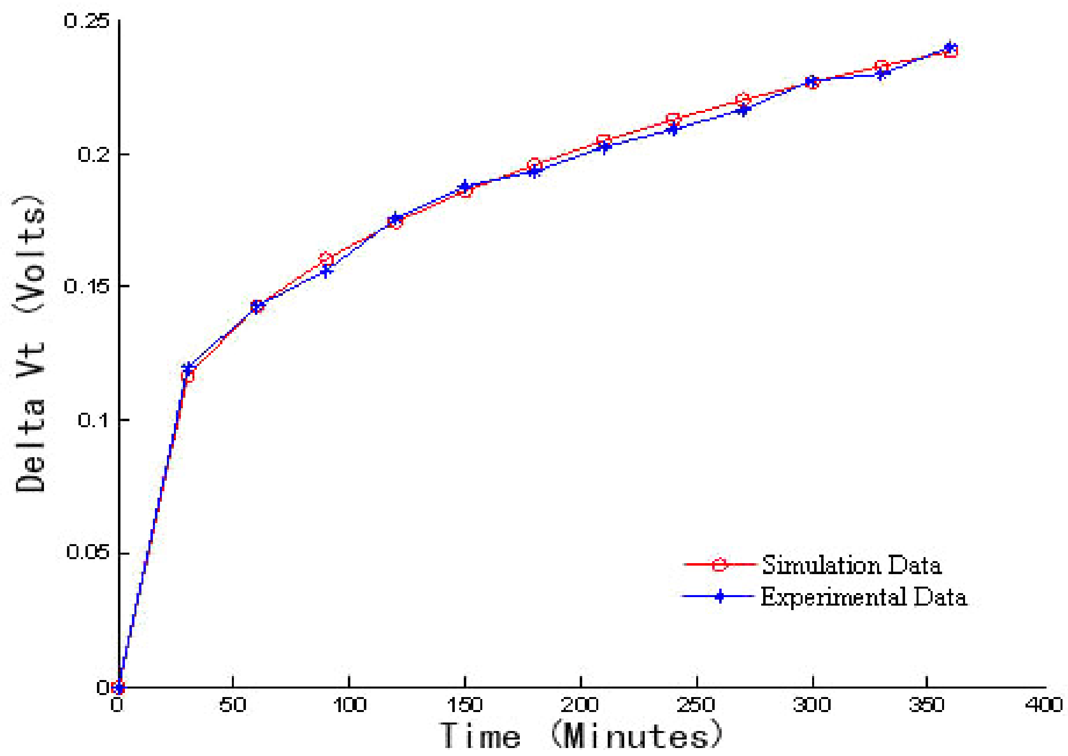


Figure 69: Threshold voltage shift of nc-Si TFT Data

Chapter 5
Conclusions

5.1 Summary

In this thesis, we performed comparison study of a-Si:H and nc-Si photo-TFTs. The performance characteristics were extracted from the test results, such that the mobility is around $1.2cm^2V^{-1}s^{-1}$, the threshold voltage is around 3.9V and the sub-threshold voltage slope is around 0.47V/Dec, which are all in the normal range of the regular TFT. The stability of the nc-Si TFT was also tested to show that it is in agreement with previously published results for a stable nano-crystalline device. For the optical properties, the nc-Si TFT has a better photo current gain under low illumination, 5×10^{14}-7×10^{15} lum. It is also shown that the negative relationship exists between the photo current gain and the Vds and the positive relationship between the external quantum efficiency and the Vds. Therefore, to get the maximum photo gain, one has to reduce the Vd. To get the maximum external quantum efficiency, one has to increase the Vd. To get the optimum photo gain and external quantum efficiency, one has to set Vd in the middle. The value of the Vgs can also control the Vds. In conclusion, the test procedure and analysis of the nc-Si TFT has efficiently shown the devices optical properties under illumination. The test results and calculated data also support that the nc-Si device is well suitable for low illumination applications such as biomedical sampling.

5.2 Future Research and Work

Some future tests can be continued on this nc-Si device such as the stability test , the real relation curve between the Vds and the external quantum efficiency, and the responsivity of the device under certain wavelengths. By applying different Vds and stresses, i.e. current and voltage, the specific range of the stability of the nc-Si TFT can be determined. To get the relationship curve between the Vds and the external quantum efficiency, different Vds can be used under certain Vgs to obtain the different photocurrent so that the corresponding external quantum efficiency can be calculated. By sweeping different wavelengths of the incident lights, we can also get the responsivities of the photo device, which can help to locate the sensitivity light range of the photo device. Furthermore, some fabrication processes can be improved to increase the absolute values of the device's photo current, which decide the requirement of the probe sensitivities of the testing equipments. The last is to expand the input dynamic range of the photo device because this nc-Si device has better performance only in the narrow range under low illumination.

Appendix A
Abbreviation Check List

APS – Active Pixel Sensor

a-Si:H – Hydrogenated Amorphous Silicon

CMOS – Complementary Metal Oxide Semiconductor

Id – Drain current

MOS – Metal-oxide Semiconductor

nc-Si – Nanocrystalline Silicon

PECVD – Plasma Enhanced Chemical Vapor Deposition

QE – Quantum Efficiency

TFT – Thin Film Transistor

Vd – Drain Voltage

Vg – Gate Voltage

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