

Application of Nanocrystalline Silicon in Forward Bias Diodes

By

Ian Chi Yan Kwong

A thesis

presented to the University of Waterloo

in fulfillment of the

thesis requirement for the degree of

Master of Applied Science

in

Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2009

©Ian Chi Yan Kwong 2009

Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

Nanocrystalline silicon (nc-Si:H) is an attractive material for fabrication of low temperature, large area electronic devices due to superior properties versus the traditional amorphous silicon (a-Si:H) and polycrystalline silicon (polySi). Nanocrystalline silicon possess higher carrier mobility and better stability than a-Si:H and better device uniformity and lower fabrication cost than polySi. This thesis looks at the application of nc-Si:H material in fabricating two different diodes used for rectification and light generation.

Optimization of n-type nc-Si:H deposited via plasma enhanced vapor chemical deposition (PECVD) was achieved through adjusting the concentration ratio of phosphine (PH_3) dopant source gas versus silane (SiH_4). Optimizing for dark conductivity, n+ nc-Si:H material with dark conductivity of 25.3 S/cm was deposited using a $[\text{PH}_3]/[\text{SiH}_4]$ ratio of 2%.

Using the optimized n+ nc-Si:H film, a p-n junction diode utilizing an undoped and an n+ nc-Si:H layers was fabricated designed for rectification use. The diode achieved a current density of 1 A/cm^2 , an ON/OFF current ratio of 10^6 and a non-ideality factor of 1.9. When the $200 \times 200 \mu\text{m}^2$ nc-Si:H diodes were employed in a full-wave bridge rectifier, a 2.6 V direct current voltage could be generated from an input sine wave signal with amplitude $2 V_{\text{RMS}}$ and frequency of 13.56 MHz, thus demonstrating the feasibility of using nc-Si:H to fabricate diodes for using on radio frequency identification (RFID) tags.

Nanocrystalline silicon was also applied in fabrication of a light emitting diode (LED), by utilizing the nanocrystals embedded inside nc-Si:H, inside which recombination of carriers could result in radiative recombination. By limiting the deposition time of the nc-Si:H, 10 – 20 nm thick films of nc-Si:H were used to fabrication a p-i-n structure LED with average crystallite size between 7.5 nm to 13.7 nm corresponding to an theoretical emission wavelengths in the near infrared region of 875 nm to 963 nm. Unfortunately, light emission from the nc-Si:H LED were not detected using two different methods. Undetectable emission could have been due to a combination of low recombination efficiency due to carriers recombining in defects in the a-Si:H matrix and majority of current travelling completely through the nc-Si:H films without recombining.

A study of the thin intrinsic nc-Si:H films used in the LED was carried out. The thin films were found to be highly defected, with large variation in current-voltage relationship measured and hysteresis observed in the IV characteristic. Annealing the nc-Si:H films were found to cause a drop in

conductivity explained through hydrogen effusion from the nc-Si:H film during annealing. Passivation of defects was achieved through the use of hydrogen plasma which resulted in a lowering of activation energy measured in the film. Oxygen plasma was also trialed for passivating the nc-Si:H film but the effect was only a temporary increase in current conduction attributed to oxygen ions chemisorbing temporarily at the film surface.

Acknowledgements

I would like to thank my supervisor professor Andrei Sazonov for his guidance and support throughout my research. I would also like to thank Doctor Hyun Jung Lee on which my research work was based and for training me in all the different machines used during my experiments.

I would also like to thank the staff of the Giga-to-Nano Centre, Richard Barber, Robert Mullins and Randy Fangan for their assistance in my research work. Professor Tong Leung and Nina Heinig also helped tremendously by helping me with XRD measurements for my samples. Special thanks go to Cherry Cheng who was a great friend and lab partner throughout my education at the University of Waterloo.

The funding for my research was provided by the National Science and Engineering Research Council of Canada. I would also like to thank the staff at the Electrical and Computer Engineering Graduate office who provided assistance for me as I switched between fulltime and part-time student, especially Wendy Bowles

Lastly, I would like to thank my parents who raised me and supported me and without whom I would not be here today.

Table of Contents

List of Tables	viii
List of Figures	ix
1 Nanocrystalline Silicon.....	1
1.1 Motivation for Research	1
1.2 Plasma Enhanced Chemical Vapor Deposition	2
1.3 Thesis Organization.....	3
2 Properties of Nanocrystalline Silicon and Its Application in Diode	5
2.1 Nanocrystalline Silicon for Diodes in Rectifier for RFID Tags.....	5
2.2 Nanocrystalline Silicon for Light Emitting Diodes	7
3 nc-Si:H Diode for Rectifiers in Radio Frequency Identification Tags	10
3.1 Diode and Mask Designs.....	10
3.2 Optimizing of Dopant Gas Ratio for n+ nc-Si:H Film with PECVD	12
3.2.1 Experiment Description	13
3.2.2 Experiment Results	16
3.2.3 Conclusion about n+ nc-Si:H Film Growth	18
3.3 Diode Measurement.....	19
3.4 Breakdown Voltage of the nc-Si:H Diode	23
3.5 Capacitive Measurements of the nc-Si:H Diode	25
3.6 Current rectification mechanism in nc-Si:H Diode	27
3.7 Rectifier Measurement Setup.....	30
3.8 Rectifier Measurement Results	31
3.9 Comparing nc-Si:H Rectifiers with Rectifiers Made by Other Technologies.....	34
3.10 Further Work in nc-Si:H Diodes for Rectification.....	36
4 Nanocrystalline Silicon for Light Emitting Diode	37
4.1 LED Design	37
4.2 Intrinsic nc-Si:H Thin Film Study	39
4.2.1 Intrinsic nc-Si:H Thin Film Thickness and Crystallinity Results	40
4.2.2 Intrinsic nc-Si:H Thin Film XRD Results	41
4.3 Zinc Oxide Thin Films Characterization.....	43
4.3.1 Experiment Description	44

4.3.2	Experiment Results	45
4.3.3	ZnO Thin Film Discussion	50
4.4	LED Measurement Experiments Setup	51
4.5	LED IV Measurement Results.....	54
4.6	Emission Measurement Results.....	56
4.7	Discussion on Lack of Emission from nc-Si:H LED.....	58
4.8	Thin Film Intrinsic nc-Si:H Experiment.....	59
4.9	IV Characteristics of Intrinsic nc-Si:H Thin Films.....	60
4.10	Thermal Annealing Results	63
4.11	Hydrogen Passivation Results.....	64
4.12	Oxygen Passivation Results.....	67
5	Conclusions and Future Directions	69
	Bibliography	72
	Appendix A.....	75

List of Tables

Table 3.1: Thicknesses of nc-Si:H layers for different sets of diodes	11
Table 3.2: nc-Si:H film deposition parameters for PlasmaTherm.....	12
Table 3.3: Experiment PH ₃ and H ₂ flow rates.....	13
Table 3.4: Comparison of key diode parameters between thin and thick Diode.....	20
Table 4.1: Summary of XRD measurements results and calculated crystallite sizes using the Scherrer equation plus theoretical light emission wavelengths	43
Table 4.2: Deposition conditions for ZnO thin films using the R2R machine	44
Table 4.3: Photodiode measurement results for different samples shows no detectable emission....	56

List of Figures

Figure 1.1: Simplified schematic of the PlasmaTherm 790 series PECVD system. The PlasmaTherm system has the sample substrate resting on the bottom electrode which can be heated by a resistive heater.....	2
Figure 2.1: Photoluminescence experiment results showing photon emission energy of silicon nanocrystals of different diameters [23].....	9
Figure 3.1: Cross section of nc-Si:H diode designed for rectification on RFIDs.....	11
Figure 3.2: Microscope picture of various nc-Si:H diodes at 10X magnification.....	12
Figure 3.3: Shadow mask design used to deposit chromium contacts for resistivity measurement....	15
Figure 3.4: Growth rate of n+ nc-Si:H films with various [PH ₃]/[SiH ₄] ratio.....	16
Figure 3.5: Crystallinity of n+ nc-Si:H films with various [PH ₃]/[SiH ₄] ratio.....	17
Figure 3.6: Dark conductivity of n+ nc-Si:H films with various [PH ₃]/[SiH ₄] ratio.....	18
Figure 3.7: Activation energy of n+ nc-Si:H films with various [PH ₃]/[SiH ₄] ratio.....	19
Figure 3.8: Forward and reverse bias current for thin and thick 150 * 150 μm ² nc-Si:H diodes.....	21
Figure 3.9: Current density of nc-Si:H diodes of different sizes.....	23
Figure 3.10: Reverse bias breakdown of nc-Si:H diodes of various sizes.....	24
Figure 3.11: Optical micrograph of nc-Si:H diode showing physical destruction after high current flow.....	25
Figure 3.12: Capacitance measured in reverse bias regime for nc-Si:H of 200 * 200 μm ² and 250 * 250 μm ² sizes using 20 and 100 Hz AC signal.....	26
Figure 3.13: Forward bias capacitance of nc-Si:H of 200 * 200 μm ² and 250 * 250 μm ² sizes at 100 Hz.....	27
Figure 3.14: Non-ideality factor extracted from IV measurements for the nc-Si:H over various temperatures.....	29
Figure 3.15: 4 nc-Si:H diodes connected in a full-wave bridge rectifier format with contact pads outside the picture.....	30
Figure 3.16: Setup for rectification measurement (a) with a single diode and (b) with 4 diodes in full-wave bridge rectifier.....	31
Figure 3.17: DC output voltage of single diode rectifiers versus input AC signal frequency.....	33
Figure 3.18: DC output voltage of full-wave bridge rectifiers versus Input AC signal frequency.....	34

Figure 3.19: (a) Pentacene-based bottom gate TFT and (b) Full-wave bridge rectifier circuit made using the TFTs [35].....	34
Figure 3.20: Rectification result of organic rectifier vs AC input frequency [35]	35
Figure 4.1: Cross section of nc-Si:H LED.....	38
Figure 4.2: Thickness and crystallinity results for intrinsic nc-Si:H films deposited for varying lengths of time.....	41
Figure 4.3: 2θ XRD measurement intensity for different thicknesses of intrinsic nc-Si:H films.....	42
Figure 4.4: 2θ XRD measurement for 12 nm thick intrinsic nc-Si:H films showed no peaks.....	42
Figure 4.5: ZnO thin film thickness with different deposition conditions	46
Figure 4.6: Optical transparency of ZnO thin films deposited at 200 °C and bare Eagle 2000 wafer....	47
Figure 4.7: Optical Transparency of ZnO thin films deposited at 300 °C and bare Eagle 200 wafer....	48
Figure 4.8: FT-IR measurement of infrared transparency for 300 °C, 6 minute ZnO thin film and bare Eagle 2000 wafer	49
Figure 4.9: Resistivity of ZnO thin films before and after anneal	50
Figure 4.10: Newport 818-UV photodetector mounted above nc-Si:H LEDs on top of the probe station	52
Figure 4.11: Response curve of the ORIEL photodiode assembly [39].....	53
Figure 4.12: Response curve of the Newport 818-UV photodetector [40]	53
Figure 4.13: IV measurement comparison of 150 * 150 μm ² LEDs from samples LED03 and LED06 ...	55
Figure 4.14: Current density measured for 200 * 200, 150 * 150, 100 * 100 μm ² LEDs from sample LED06	55
Figure 4.15: Emission spectrum of store bought infrared LED with 940 nm peak measured using Raman spectroscopy machine	57
Figure 4.16: Emission spectrum of nc-Si:H LED06 measured using Raman spectroscopy machine	58
Figure 4.17: Horizontal current flow in the intrinsic thin film experiment as indicated by the arrows to travel at least 1 mm.	59
Figure 4.18: -20 V to 20 V sweeps showing hysteresis behavior in IV characteristics before and after annealing at 230 °C	62
Figure 4.19: Effect of Delay Factor (DelayF) settings on measurement results with higher DelayF leading to non-linearity	62
Figure 4.20: Current sampling results for 14 nm thick nc-Si:H sample with different constant voltages showing dropping current over time	63

Figure 4.21: Current measured for 12 nm and 14 nm thick samples before and after hydrogen plasma, showing an increased in current after exposure to plasma..... 65

Figure 4.22: A decrease in activation energy was observed after exposure to H plasma..... 66

Figure 4.23: Band diagram showing the before hydrogen plasma (Dotted Line) and after hydrogen plasma (Solid Line) configuration of the Fermi Energy level with a shift due to reduction of midgap defects 66

Figure 4.24: Interface defects could either be trapped at the nc-Si:H to glass interface or at the top of the nc-Si:H Film 67

Figure 4.25: IV measurement results for nc-Si:H sample showing the effect of oxygen plasma 67

1 Nanocrystalline Silicon

Nanocrystalline silicon (nc-Si) describes a specific type of material which is made up of crystals of nanometer dimensions embedded in an amorphous matrix of silicon. The hydrogenated version of nanocrystalline silicon, hydrogenated nanocrystalline silicon (nc-Si:H) has become a material that has researchers interested when discussing low temperature and large area manufacturing.

Like hydrogenated amorphous silicon (a-Si:H) which is the dominant material used for low temperature and large area electronics, nc-Si:H can be deposited using plasma enhanced chemical vapor deposition (PECVD) or with hot-wire chemical vapor deposition (CVD). When compared to amorphous silicon material, nc-Si:H has been shown to have better carrier mobilities and better stability which has been attributed to the presences of the nano-sized crystals [1].

Polycrystalline silicon (poly-Si) material has also been used to manufacture better performing devices than a-Si:H. Compared to poly-Si, nc-Si:H devices possess better uniformity in performance due to roughly uniform distribution of nanosized crystals in a device instead of larger crystals in from polySi resulting in devices potentially crossing grain boundaries. Poly-Si manufacturing also requires additional steps including dehydrogenation and recrystallization leading to higher manufacturing costs [2].

Applications for nc-Si:H has included thin film transistors (TFTs) for making switching back planes for liquid crystal displays (LCDs) and organic light emitting diodes (OLED) arrays [2]. The material has also found use in photovoltaic cells both as recombination layer and for making contact material [3] [4]. Nc-Si:H has also been applied for use in X-ray sensors and color detectors as photodiodes [5].

1.1 Motivation for Research

There has been many work done studying the application of nc-Si:H into diodes; however, the diodes have been used in applications which requires reverse biasing the diode, such as a photodiode. There has been few works studying nc-Si:H diodes in forward bias applications. The motivation for this research is to study the application of nc-Si:H in diodes used in the forward bias regime and understand the challenges in designing, manufacturing and characterizing such devices. A goal of this research is the demonstrate the versatility of the nc-Si:H material and investigate possible new applications for nc-Si:H. Two possible forward bias diode application is discussed here: a diode

for use in rectifiers on radio frequency identification (RFID) tags and a light emitting diode (LED) using quantum confinement in nanocrystals in nc-Si:H for silicon light generation.

1.2 Plasma Enhanced Chemical Vapor Deposition

The PECVD process is the deposition process which allows for the deposition of nc-Si:H and enables nc-Si:H to have the advantages of being able to be deposited at low temperatures and over large areas which are key advantages to nc-Si:H versus traditional crystalline silicon (c-Si). The operating principle behind PECVD, as the name implies, consists of chemical vapor deposition assisted with the addition of plasma. The PECVD machine used for this research is the PlasmaTherm 790 series and a schematic can be viewed in Figure 1.1.

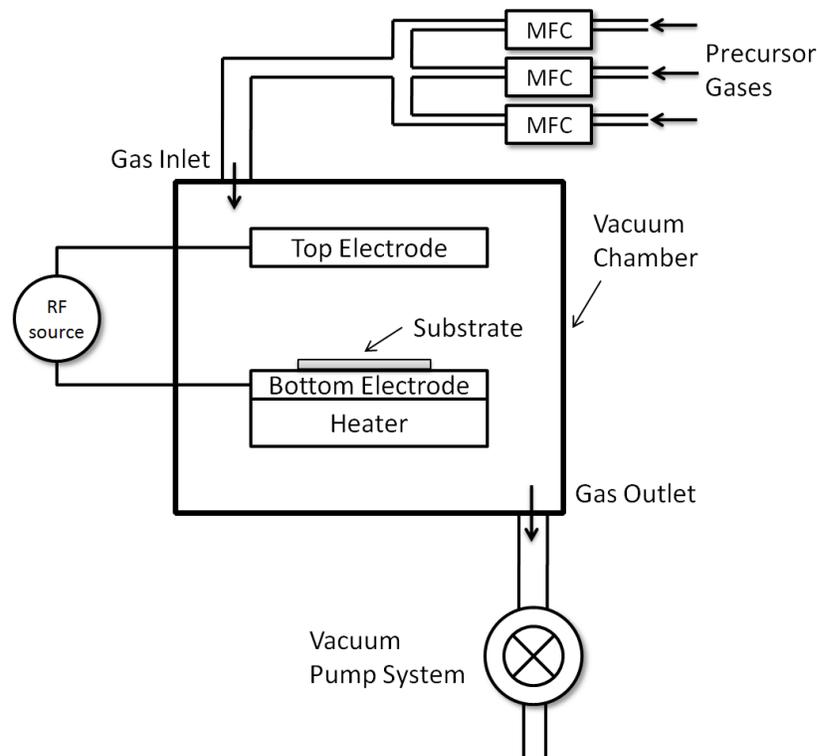


Figure 1.1: Simplified schematic of the PlasmaTherm 790 series PECVD system. The PlasmaTherm system has the sample substrate resting on the bottom electrode which can be heated by a resistive heater

Chemical vapor deposition occurs inside a vacuum chamber where precursor gases are flowed through at a controlled rate. The precursor gases are selected to donate specific molecules necessary for chemical reactions to create the desired material for deposition. Traditional CVD uses heat to break the precursor gas molecules apart into ions and radicals for the chemical reaction to occur and this heating is quite high, 300 °C or more, thus limiting the choices of substrate. Instead, by adding

electrodes inside the chamber and applying a voltage field to create a plasma to break apart the gas molecules, the deposition temperature can be reduced which results in PECVD [6].

PECVD has been used to deposition a-Si:H and nc-Si:H for many years using silane (SiH_4) and hydrogen as typical precursor gas. With deposition temperatures as low as 90°C , the use of many different plastic substrates is possible which leads to the possibility of flexible electronics. Large area deposition is also possible, with PECVD limited by the radio frequency used to generate the plasma. Higher frequency limits the maximum area due to null points in standing waves between the electrodes but lower frequency tends to deposit films with poor electrical properties. Optimization of PECVD process variable becomes an important area of research. Process variables for PECVD include deposition temperature, gas pressure, radio frequency and power density, hydrogen dilution and dopant gas ratios all affect electronic properties of the nc-Si:H material [6].

1.3 Thesis Organization

Chapter 2 discusses properties of nc-Si:H and how these properties applies to the selected diodes for study. Motivation for applying nc-Si:H material in the two chosen diodes applications are outlined. Requirements for diodes used in RFID tag rectifiers are discussed. Background information on using silicon nanocrystals for photon generation and the quantum confinement effect that occurs in silicon nanocrystals are shown.

Chapter 3 discuss the design, fabrication and electrical characteristics of nc-Si:H diodes designed for use in rectifiers for RFID tags. Optimization of the deposition for a n+ nc-Si:H layer used in the diode was conducted. The conduction nature of the nc-Si:H diode is explored. Actual rectifiers made with nc-Si:H are measured for their performances and compared with organic rectifiers also applied towards RFID uses to understand the viability of using nc-Si:H as material for RFID fabrication.

Chapter 4 turns to the application of nc-Si:H material to fabrication light emitting diode. It discusses the design of the nc-Si:H LED studied and the experiment setup for measuring light emission from such an LED. A characterization of the zinc oxide (ZnO) material used as a top transparent metal contact for the LED was also carried out, including light transmission properties, resistivity and deposition conditions. Furthermore, a study of thin film intrinsic nc-Si:H used in making the LED is carried out. Electrical characteristics of the thin films are shown. Passivation techniques to affect the quality of the thin films are also tested and results are shown.

Chapter 5 is a summary of the results and conclusion drawn on nc-Si:H application in diodes used for rectifiers and LEDs. Suggestions are made on future directions for research related to the discussed topics.

2 Properties of Nanocrystalline Silicon and Its Application in Diode

As discussed previously, the goal of this research is to apply nc-Si:H as the semiconductor material in fabricating diodes for using in rectifier for RFID tags and light emitting diodes. Nanocrystalline silicon possess several characteristics which makes it an attractive material for use in the two applications.

2.1 Nanocrystalline Silicon for Diodes in Rectifier for RFID Tags

The use of radio frequency identification (RFID) technology in business is being lauded as the next big revolution in enhancing business intelligent to enhance efficiency and increase productivity. RFID technology consists of “tagging” RFID transponders, or tags, onto items and retrieving information from these tags wirelessly. RFID technology has found a wide variety of applications in many industries from retail industry, pharmaceutical industry to hospitals and livestock farms [7] [8] [9]. However, RFID uptake has been slow and one major factor is the cost associated with deploying large number of RFID tags. It has been estimated that acceptable costs for wide spread adoption of RFID tags is 10 cents or lower for the tag alone. Some very simple RFID tags have reached that level such as passive tags used in retail theft prevent; however, advanced RFID tags that provide data processing and writable storage capability have not. These advanced tags require many transistors leading to increased manufacturing costs. Currently, these advanced RFID tags use traditional crystalline silicon CMOS chips and are still too expensive for wide spread deployment [10].

One method to reduce the manufacturing cost of RFID tags is to switch to using large area electronics manufacturing methods and technology. Current intelligent RFID tags are commonly manufactured using a packaged CMOS chip made on crystalline silicon which is then bonded to an antenna and substrate of the tag. The packaging cost of the CMOS chip, the bonding cost and the subsequent testing cost of the final tag adds to the total cost of the finished RFID tag. By switching to large area electronics technology, where the antenna and active circuitry are manufactured in one integrated process, there is much potential for cost savings.

Research has been done on using amorphous silicon and organic semiconductors in making the active components for RFID tags [11] [12] [13]. Using nc-Si:H is also another option to manufacture RFID tags cheaply. As discussed, nc-Si:H can be manufactured using the same PECVD process as a-Si:H. Deposition using PECVD over a large area is currently done, thus allowing for mass

manufacturing of the tags. At the same time, by using a low temperature PECVD process, nc-Si:H based RFID tags are capable of using flexible plastic substrate. Flexible RFID tags are also important for wide spread adoption in situations such as a super market, where the items being tagged are of irregular shapes, such as metal cans and plastic containers.

An advantage that nc-Si:H possess over a-Si:H is that enhanced carrier mobilities for both electrons and holes. The enhancement in carrier mobilities are attributed to the presence of the nanometer sized silicon crystals in nc-Si:H. Through high hydrogen dilution during the PECVD growth processes, silicon nanocrystals form resulting in films with high crystallinity. Higher crystallinity results in higher carrier mobilities. Conduction is limited by the grain boundaries that exists between the crystallites and the a-Si:H matrix where the defects are concentrated. Typical model of nc-Si:H conduction assumes the crystals are perfect and that the trapping of carriers at the boundaries, where dangling silicon bond exists, limit the mobilities. Carrier mobilities of nc-Si:H ranges from 1 – 100 $\text{cm}^2/\text{V s}$ for electrons and up to 1 $\text{cm}^2/\text{V s}$ for holes which are 2 order of magnitude better than a-Si:H [6].

Higher carrier mobilities equal higher performing devices made with nc-Si:H, with higher current flow and faster switching speed. High current flow and fast switching speed are both important for diodes employed in a rectifier. A rectifier's input consists of a rapidly switching alternating current (AC) which requires the diodes having to response rapidly. A fast switching speed for the diodes will allow for higher power output from the rectifier at the same AC frequency. A higher current conduction for the diodes will allow for more power delivered to the RFID tag circuit. The amount of power delivered to an RFID tag is an important metric because the majority of inexpensive RFID tags deployed are passively powered, where the power to run the circuit is delivered wirelessly to the tag from a reader. Rectification efficiency will determine the maximum range that an RFID tag can be used in [7].

In terms of low power for RFID circuits, nc-Si:H also possess another advantage over a-Si:H and organic semiconductors. It has been demonstrated that nc-Si:H could be use to fabrication both n-type and p-type devices thus making complementary circuit possible with nc-Si:H thin film transistors (TFTs). Organic semiconductor and a-Si:H has been limited to p-type and n-type only TFTs due to low electrons and holes carrier mobilities respectively. By using nc-Si:H, it is possible to integrate an efficient nc-Si:H rectifiers made with diodes with true complementary circuit using nc-Si:H TFTs fabricated on flexible plastic substrate at low cost by using PECVD deposition processes [2][14].

2.2 Nanocrystalline Silicon for Light Emitting Diodes

Light Emitting Diodes (LED) are typically made using gallium based semiconductor due to their direct bandgap nature. The direct bandgap is necessary for efficient light production. Common material used for LEDs include gallium nitride (GaN) and indium gallium nitride (InGaN).

LEDs are being considered as a lighting replacement for traditional incandescent light bulbs. In order to save on energy costs, there has been a push in replacing incandescent light bulbs with more energy efficient alternatives. Compact fluorescent light (CFL) bulbs are being touted in the market as a more efficient replacement than incandescent bulbs. LEDs also have longer lifetimes, higher efficiency, smaller in volume and less fragile than incandescent bulbs. LEDs also contains no mercury and are smaller and more damage resistance when compared to CFLs. Mercury can be damaging to the environment if the mercury is not properly disposed [15]. However, the biggest drawback to LEDs is the cost of manufacturing. Using expensive materials such as Ga and sapphire substrate to get efficient LEDs have led to CFLs being more cost effective as incandescent light replacement for the time being [16].

One drawback of gallium based semiconductor is the much high material cost of gallium when compared to silicon. Silicon has traditionally not been used for LEDs because of its indirect bandgap property. Recently, there had been renewed interests in making silicon photonics, where photons are generated using silicon. The key to silicon photonics lies in the use of quantum effects to produce the direct transition between energy states for photon creation [17].

One method used in silicon photonics is the use of nanometer-sized nanocrystals of silicon to create quantum wells. The discrete energy levels in the silicon quantum wells can lead to photon creations when electrons transition between states. Researchers have previously demonstrated photon creations of various visible wavelengths using a variety of methods to create the silicon nanocrystals. These methods include the use of porous silicon, ion implantation using silicon ions and fabrication using thinned c-Si material [18] [19] [20].

Silicon, being an indirect bandgap material, has the majority of carrier recombinations occurring with the phonon production to account for the difference in potential energy between the conduction band and valence band. This leads to mostly non-radiative recombination in silicon thus making photo generation very inefficient. However, what researchers have discovered was that in nanosized silicon crystals, the confinement of charges on these crystals lead to a higher likelihood of

radiative recombination. Carriers confined in silicon nanocrystals are separated from any defects which only exist at the nanocrystals' grain boundaries [17]. Light emission has been achieved in porous silicon, in which the nanocrystals are surrounded by empty spaces, and also in silicon nanocrystals embedded in an oxide or nitride insulation through ion implantation of silicon atoms in existing oxide or nitride [19][20].

The idea behind making LED using nc-Si:H is to directly grow the silicon nanocrystals using PECVD has part of the nc-Si:H material. Using PECVD for direct growth of the silicon nanocrystals provide several advantages such as large area manufacturing capability, fabrication on flexible substrate and lower costs due to fewer steps and less equipment required when compared to other silicon photonics techniques. Porous silicon requires etching of crystalline silicon and embedded nanocrystals require ion implantation machinery and require post-implantation annealing to form crystals. A possible application of nc-Si:H based LED may be light emitting wallpaper that is flexible. The wall paper can be applied to walls or ceiling to provide complete illumination of a room.

The growth of the nc-Si:H material will need to be controlled. The wavelength of photons generated directly depends on the size of the silicon nanocrystals. In order to obtained a desired wavelength, control of nc-Si:H growth condition must be obtained. Nc-Si:H film growth typically involves an "incubation layer" for the first few nanometers, in which no crystallites exists in the film, on amorphous silicon. As the nc-Si:H film gets thicker, crystallites starts appear and gets larger as the film gets thicker. Eventually the crystallites coalesces together to form columns of nanocrystalline material separated by grain boundary. It has been shown that by adjusting deposition conditions, crystallite sizes can be controlled and the incubation layer thickness reduced or even removed [21].

Confinement of carriers inside the crystals in nc-Si:H can be achieved through the band offsets between the crystal and a-Si:H matrix. It is believed that the bandgap of the nanocrystals in nc-Si:H is smaller than the surrounding a-Si:H bandgap. The a-Si:H bandgap provides a barrier to both electrons and holes with a 0.1 eV offset for the conduction band and a 0.6 eV offset for the valence band [22]. The defects of the nc-Si:H films are also concentrate at the grain boundary only and not inside the nanocrystals thus protecting the carriers from non-radiative recombination.

From porous silicon experiments, researchers have calculated the theoretical emission energy from silicon nanocrystals and came up with an equation that relates the diameter of the crystals to emission energy [18]. Other researchers have experimentally verified the validity of the equation and

shown that quantum confinement, which leads to higher emission energy, does occur in silicon nanocrystals. Figure 2.1 shows the results from a photoluminescence study of silicon nanocrystals of sizes from 2.5 nm to 8 nm, which confirms the theoretical results [23]. The equation relating crystal diameter to emission energy in eV is

$$E = E_0 + \frac{3.73}{d^{1.39}} \quad (2.1)$$

Where d is the crystal diameter in nanometers, E_0 is a curve fitting parameter. From the experimental data, the value for E_0 is approximately 1.19 eV. This Equation (2.1) would allow for estimation of nc-Si:H LED emission wavelength depending on the average size of crystals in the nc-Si:H film.

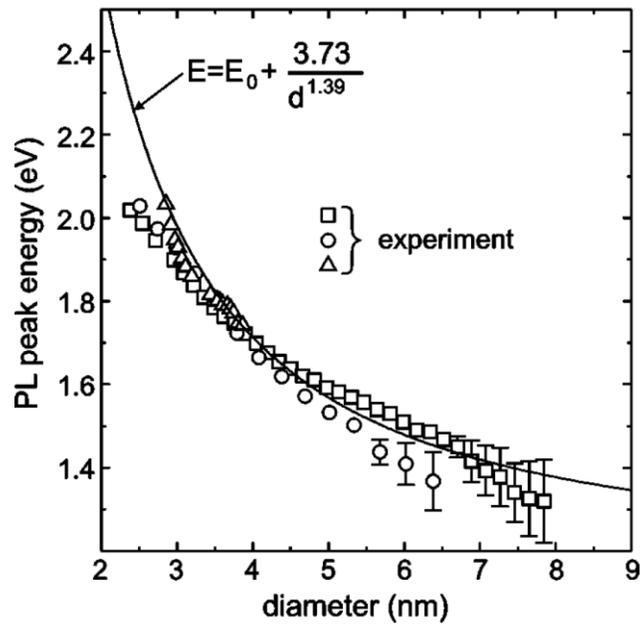


Figure 2.1: Photoluminescence experiment results showing photon emission energy of silicon nanocrystals of different diameters [23]

3 nc-Si:H Diode for Rectifiers in Radio Frequency Identification Tags

In this chapter, a nc-Si:H diode designed for the use as a rectifier in RFID tags is shown. In passive RFID tags, an alternating current (AC) signal is being used to inductively couple the power from an RFID reader to the tag in order to run the circuitry on the tag. AC signal is typically converted to direct current (DC) by a rectifier, which is an essential part of a passive RFID tag.

3.1 Diode and Mask Designs

The nc-Si:H diode was designed as a vertical structure (i.e., the current passed normally to the substrate plane) and the cross-section of the diode is shown in Figure 3.1. The diode was made on Corning 1737 glass substrates which had been cleaned using standard RCA1 cleaning process.

The manufacturing process was a 4 masks process. The first step was to deposit a 300 nm thick layer of chromium (Cr) as the bottom contact metal and interconnect metal for the rectifiers. Deposition was done through metal sputtering with the Edwards RF Magnetron sputtering system. The Cr was patterned using photolithography and wet etched using $\text{Ce}(\text{NH}_4)_2(\text{NO}_3)_6$ plus acetic acid.

The second step was to deposit a bi-layer of nc-Si:H consisting of an intrinsic undoped layer and an highly doped n+ layer. Both layers were deposited using the PlasmaTherm PECVD system without breaking the vacuum in between the layers. The deposition conditions for the n+ nc-Si:H layer were optimized for highest dark conductivity. The optimization of the n+ nc-Si:H film will be discussed in a later section. Like-wise, the intrinsic layer deposition used conditions previously optimized by other researchers in the group. Please refer to Table 3.2 for the deposition conditions. Two sets of diodes with varying thicknesses of intrinsic and n+ layers were made and the thickness chosen can be seen in Table 3.1. The film thicknesses were varied to understand their effect on the diode performance.

The nc-Si:H layers were patterned using photolithography and reactive ion etching (RIE). Diodes with different areas were made. The size of a diode was determined by the patterned nc-Si:H films area. The different areas of the diodes were 50 * 50, 100 * 100, 150 * 150, 200 * 200 and 250 * 250 μm^2 .

A 300 nm thick layer of SiO_2 was deposited using PlasmaTherm PECVD to passivate the nc-Si:H films. Passivation was needed to protect the nc-Si:H films from ambient atmosphere and to define

devices by separating top and bottom metal contacts. Contact hole was opened through the SiO₂ film using photolithography and wet etching using HF acid.

The final step was to deposit aluminum (Al) as the top contact metal also using the Edwards sputtering system. 500 nm or more of Al was deposited to fully cover the vertical sidewall of the diode, which depended on the nc-Si:H layer thicknesses. The Al was patterned and wet etched using phosphoric, acetic and nitric acid (PAN) to define remaining metal traces for the rectifier and contact pads for bonding.

Figure 3.2 shows a microscope picture of the finished diodes at 10X magnification. Different sizes of diodes are visible in the picture. The darker metal contact pads on the right are the Cr and the metal contact pads on the left are Al.

Highlights of the 4 masks used to make the diodes and the rectifier circuits are shown in Appendix A.

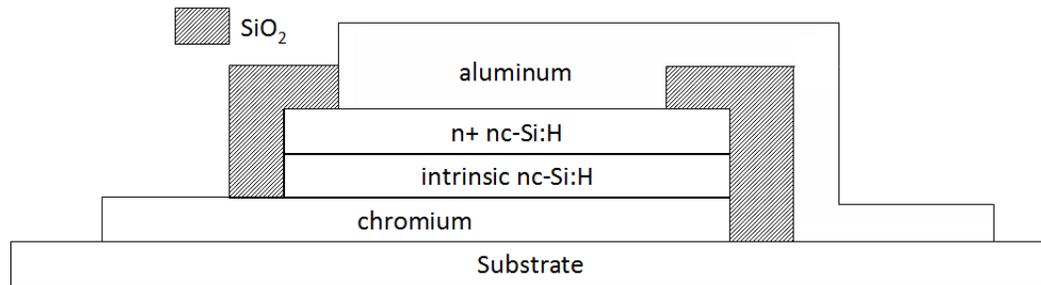


Figure 3.1: Cross section of nc-Si:H diode designed for rectification on RFIDs

Table 3.1: Thicknesses of nc-Si:H layers for different sets of diodes

Sample Layer Thickness	Set 1 (thin diode)	Set 2 (thick diode)
intrinsic layer	100 nm	300 nm
n+ layer	40 nm	100 nm

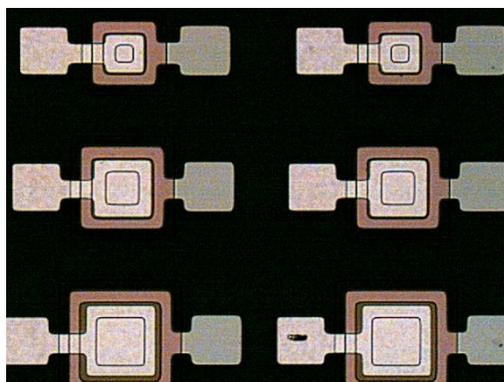


Figure 3.2: Microscope picture of various nc-Si:H diodes at 10X magnification

Table 3.2: nc-Si:H film deposition parameters for PlasmaTherm

Process Parameter	Value
Temperature	260 °C
Chamber Pressure	900 mTorr
RF Power	90 Watts
Silane (SiH ₄) flow rate	15 sccm
Hydrogen Dilution	99%
Deposition Time	15 minutes

3.2 Optimizing of Dopant Gas Ratio for n+ nc-Si:H Film with PECVD

Previous researchers in the group had optimized several deposition parameters for nc-Si:H films using the PlasmaTherm PECVD machine, including hydrogen dilution, chamber pressure, radio frequency power density and temperature.

Doping of nc-Si:H films was achieved by adding dopant gases into the mixture during the deposition. The gases phosphorus hydride (phosphine/PH₃) and trimethylborane (TMB, B(CH₃)₃) were used to provide dopant atoms of phosphor and boron for n-type and p-type doping in the nc-Si:H film respectively.

The ratio of doping gases versus silane gas in the chamber was a parameter which had not been optimized. Varying the ratio would lead to differing amount of dopant atoms being incorporated into the nc-Si:H film. In turns, this could lead to changes in the conductivity, crystallinity and other properties of the film.

The purpose of this experiment was to identify the ratio of PH_3 to SiH_4 which results in the highest dark conductivity for the n+ nc-Si:H film. The n+ nc-Si:H films are used to form contact layers between device and metal lines, thus higher dark conductivity leads to lower contact resistance and more ideal device operation. To form ohmic contacts with the metal lines, the n+ films are typically heavily doped to reduce the thickness of any Schottky barrier that exists and allowing efficient tunneling of current to pass through [24].

3.2.1 Experiment Description

The n-doped nc-Si:H films was deposited on Corning 1737 glass wafers which had been cleaned with standard RCA1 cleaning process.

The deposition was done using the PlasmaTherm 790 series PECVD machine. It utilized a 13.56 MHz radio frequency (RF) generator for plasma generator. The electrodes were 14 inch x 14 inch square with a 1 inch separation between the top and bottom electrode. Previously optimized conditions for nc-Si:H film deposition used are listed in Table 3.2. Deposition time for all the different samples were set for 15 minutes to provide enough thickness.

The experiment variable was to vary the concentration of PH_3 versus SiH_4 , testing for $[\text{PH}_3] / [\text{SiH}_4]$ ratio of 0.5%, 1%, 2% and 3%. Because the PH_3 gas was diluted in H_2 , so in order to maintain the constant 99% hydrogen dilution ratio, the H_2 flow rate was varied according with the PH_3 gas flow rate and this can be seen in Table 3.3.

Table 3.3: Experiment PH_3 and H_2 flow rates

Sample	$[\text{PH}_3] / [\text{SiH}_4]$	PH_3 flow rate (sccm)	H_2 flow rate (sccm)
001	1%	5	495
002	3%	15	485
003	2%	10	490
004	0.5%	2.5	497.5

The n+ films were then characterized. The thickness was the film was measured using the Dektak 8 profilometer after using photolithography to etch micrometer thick lines in the film. From the film thickness, the deposition rate of the film could be easily calculated by dividing by the 15 minute deposition time.

Crystallinity of the nc-Si:H films were measured using Raman spectroscopy with a Renishaw micro-Raman 1000 spectrometer. The laser wavelength used to measure the Raman shift is a He-Ne laser at 633 nm. The Raman shift spectrum from the samples were then de-convoluted into two separate Gaussian peak centered at 520 cm⁻¹ and 480 cm⁻¹ wavenumber to represent the crystalline silicon and amorphous silicon signal respectively. The crystallinity of the sample was then calculated using the Equation (3.1)

$$X_c = \frac{I_c}{I_c + 0.8 * I_a} \quad (3.1)$$

Where X_c is the crystallinity value, I_c is the peak value of the crystalline Gaussian and the I_a is the peak value of the amorphous Gaussian curve [2].

Conductivity of the doped nc-Si:H films was calculated from current-voltage (IV) measurements of the films. Chromium contacts approximately 200 nm thick were deposited on top of the samples through shadow masks using an Edwards radio frequency magnetron sputtering system. The shadow mask was designed by fellow researcher Dr. Hyun Jung Lee and the layout of the various contacts can be seen in Figure 3.3.

For the conductivity measurements, the 7 rectangular contacts on the lower left side were used for IV measurements. The IV measurements were done using a Keithley 4200 Semiconductor Characterization System with the samples in the dark. From the IV measurements, the resistance of the film could be calculated simply by using Ohm's Law and the dark resistivity extracted using a simple rectangle resistor model.

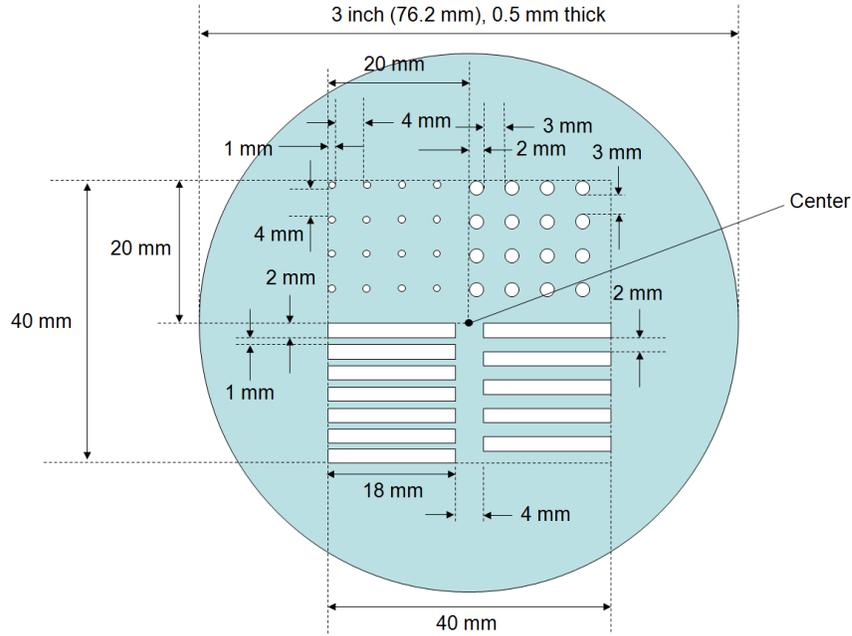


Figure 3.3: Shadow mask design used to deposit chromium contacts for resistivity measurement

To extract the resistivity, the rectangle resistor model was used which treated the nc-Si:H film in between a pair of chromium contacts as a simple resistor. The dimensions of the resistors as can be seen from Figure 3.3 were length of 1 mm, width of 18 mm and the thickness being the thickness of the film. The resistance and resistivity is related using the Equation (3.2) where R is the measured resistance, ρ is the resistivity, L is the length of the resistor, W is the width of the resistor, and t is the thickness of the film.

$$R = \rho \frac{L}{W * t} \quad (3.2)$$

The dark conductivity was simply the inverse of the resistivity extracted from the model.

Furthermore, the activation energy (EA) of the various samples were extracted from temperature-dependent IV measurements. EA is defined as the difference in energy between the Fermi energy level and the conduction band in the nc-Si:H film. The relation between EA, dark conductivity and temperature is given by Equation (3.3).

$$\sigma_d = \sigma_o \exp\left(-\frac{EA}{kT}\right) \quad (3.3)$$

In Equation (3.3), σ_d is the dark conductivity, σ_o is the conductivity prefactor, EA is the activation energy, k is the Boltzmann constant and T is the temperature in Kelvin. By assuming σ_o is

constant over temperature, the EA can be extracted from dark conductivity measurements over a range of temperature. Using a temperature controlled probe station, dark conductivity were measured using the same resistor model method as before. The measurement temperatures ranged from 25 °C (298.15 K) to 100 °C (373.15 K) in increments of 25 degrees.

3.2.2 Experiment Results

The growth rates of the different experimental n+ films can be seen in Figure 3.4. The rates were calculated by dividing the measured thickness of the samples by the deposition time. Of note was the growth rate for the 2% $[\text{PH}_3]/[\text{SiH}_4]$ ratio sample. The sample had a growth rate of 3.68 nm/minute, which was lower than the other samples with growth rates larger than 4 nm/min. This could be attributed to human error in the experimental procedure. During the thickness measurement process, photoresist was used to define the measurement lines and reactive ion etching was used to remove unwanted nc-Si:H material. The photoresist was then removed by soaking in a chemical stripper which could have also etched the nc-Si:H material for the 2% sample if the sample was left in for too long.

Crystallinity values are shown in Figure 3.5. All of the samples had percentages higher than 50%, demonstrating that they are indeed nc-Si:H films due to maintaining 99% hydrogen dilution.

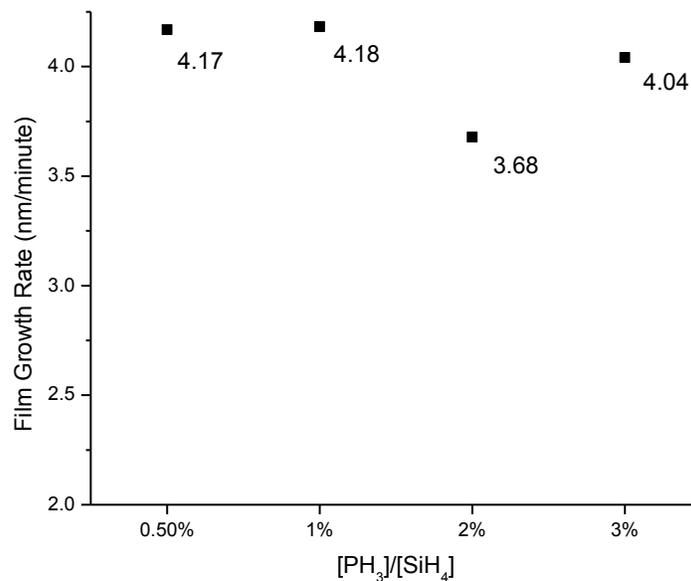


Figure 3.4: Growth rate of n+ nc-Si:H films with various $[\text{PH}_3]/[\text{SiH}_4]$ ratio

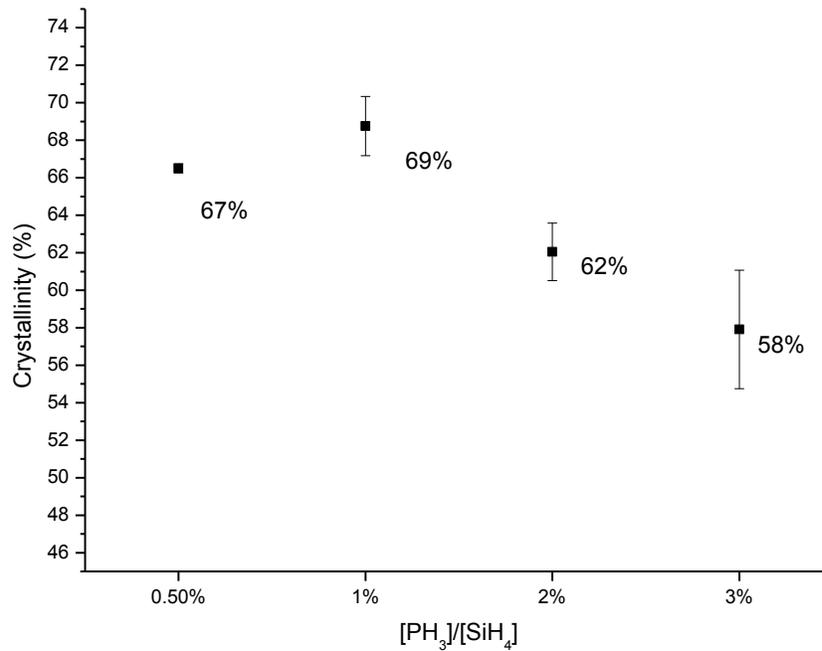


Figure 3.5: Crystallinity of n+ nc-Si:H films with various [PH₃]/[SiH₄] ratio

The trend for the crystallinity percentage was to drop with increasing PH₃ concentration as can be seen in the 2% and 3% samples. This has been observed previously where increase doping led to amorphization of nc-Si:H samples [25].

The dark conductivity of the different samples are shown in Figure 3.6 and it clearly demonstrates that there was an optimal point to growth n+ nc-Si:H film with highest dark conductivity. The 2% sample had the highest dark conductivity, at an average 25.3 S/cm. The drop off in conductivity for the 3% sample could be explained with the decrease in crystallinity as previously observed. High crystallinity of the nc-Si:H is one contributing reason to higher charge mobility and conductivity than amorphous silicon. At the same time, doping with donor atoms can increase the number of carriers in the material but at a cost of decrease crystallinity. There appears to be an optimal point to balance the benefit of doping and crystallinity. Not all of the donor atoms in a nc-Si:H film are electrically active, but the incorporation of more donor atoms causes a decrease in crystallinity [25] [26].

Looking at the activation energy measured for the various films in Figure 3.7, there was an inversely linear relationship between the dark conductivity of the film and the activation energy. This

made sense because lower activation energy meant that there are more free electrons available close to the conduction band which would increase conductivity [26].

The values of the activation energy for all the samples were in the milli-electron voltage range which confirmed that the films were indeed n-type. The milli-eV values for the EA had been observed previous in other n+ nc-Si:H films [27] and was not unexpected. Doping in a-Si:H and nc-Si:H leads to movement of the Fermi energy level. However, due to the existence of deep defects states in the middle of the band gap, the position of the Fermi energy level cannot be controlled precisely. The Fermi energy level exhibits “binary” position, either very close to the conduction/valence band or trapped in the middle of the band gap [6].

3.2.3 Conclusion about n+ nc-Si:H Film Growth

With highest dark conductivity as the target for this experiment, the optimal ratio of $[\text{PH}_3]/[\text{SiH}_4]$ was found to be 2%. There was a peak dark conductivity measured at 2% as the $[\text{PH}_3]/[\text{SiH}_4]$ ratio was increased from 0.5% to 3%. For the remaining experiments in this thesis, this optimized version, using 2% $[\text{PH}_3]/[\text{SiH}_4]$ ratio, of the n+ nc-Si:H film will be utilized in different diodes.

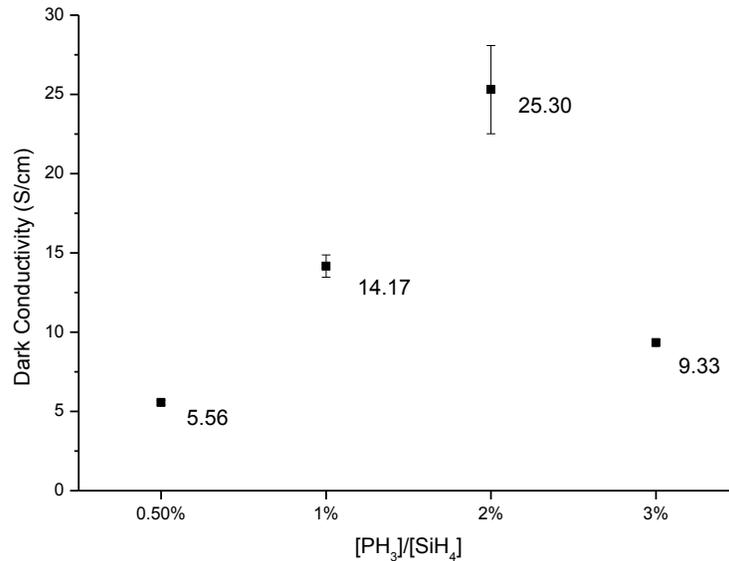


Figure 3.6: Dark conductivity of n+ nc-Si:H films with various $[\text{PH}_3]/[\text{SiH}_4]$ ratio

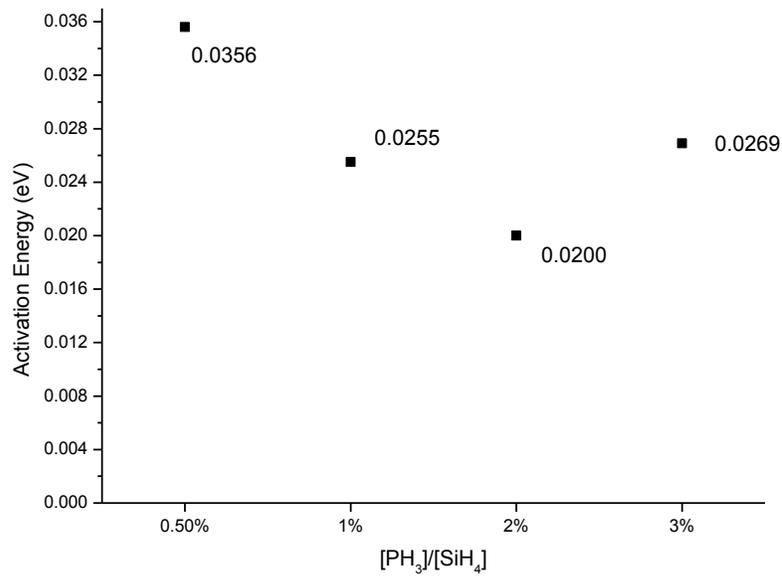


Figure 3.7: Activation energy of n+ nc-Si:H films with various [PH₃]/[SiH₄] ratio

3.3 Diode Measurement

The fabricated diodes had their IV characteristics measured using the Keithley 4200 Semiconductor Characterization System (SCS). Temperature dependence of the IV characteristics was also measured using the Keithley plus temperature controlled probe station. The temperature range was from -30 °C to 125 °C. Capacitance – Voltage (CV) measurements was also performed using a HP 4280A Capacitance measuring devices in conjunction with the Keithley SCS.

The initial study investigated the effect of nc-Si film thickness on the diode performance. The thin diode was the one with 100 nm intrinsic nc-Si:H and 40 nm thick n+ nc-Si:H layer. The thick diode was the set made with 300 nm and 100 nm for intrinsic and n+ nc-Si:H layers respectively. The thicknesses for the diodes were chosen based on previous thin film transistor (TFT) design made with the same nc-Si:H material. The thin diode used the same thickness as the TFT while the thick diode had tripled the thickness to guarantee observable differences. Figure 3.8 shows a comparison of the measured current for a thin and thick diode, both of which were of size 150 * 150 μm². The voltage applied varied from -2V to 2V.

Both diodes displayed a typical diode behavior with non-linear IV characteristic measured. The forward bias current increased quickly until approximately 0.7V. Beyond 0.7V, the current for the diodes leveled off and had a different slope on the log scaled graph. This was typical of nc-Si:H diodes and was attributed to resistance limited effects in diode contacts or space-charge limited current

(SCLC) [28]. SCLC current occurs when the number of injected carriers into the material exceeds the number of trapped carriers. This occurs at high bias when the Fermi energy level passes the trap energy level and fills the trap completely. During SCLC, the current density follows a power-relation with the voltage [24] [29].

The thin diode had a higher current in forward bias mode than the thick diode. However, the thin diode also displayed significant reverse bias leakage current. Compared to the thick diode, the reverse current was approximate 6 orders of magnitude higher. The forward and reverse bias current of the thin diode did not display much difference. A comparison between key parameters is listed in Table 3.4.

ON/OFF current ratio is defined as the ratio of the forward bias current over reverse bias current, both at 1 V bias. This was a measure of the diode’s rectification ability. The diode basic task was to allow current through at forward bias while limiting current at reverse bias. A high ON/OFF ratio was essential for good rectification. The thin diode’s ON/OFF ratio was extremely low, with a measured value of 7.5, due to very high reverse current.

The high reverse current and low ON/OFF ratio of the thin diode was an indication of a fully depleted semiconductor layer in the nc-Si:H layers of the diode. The thicker diode provided a much more diode-like characteristic thus supporting our assumption. With a fully depleted nc-Si:H layer, the thin diode was unable to prevent a sufficiently large barrier to mobile carriers thus acting more like a voltage-dependent resistor than a diode.

Table 3.4: Comparison of key diode parameters between thin and thick Diode

	Thin Diode	Thick Diode
ON/OFF Ratio	25	10^6
Non-ideality Factor	7.5	1.9

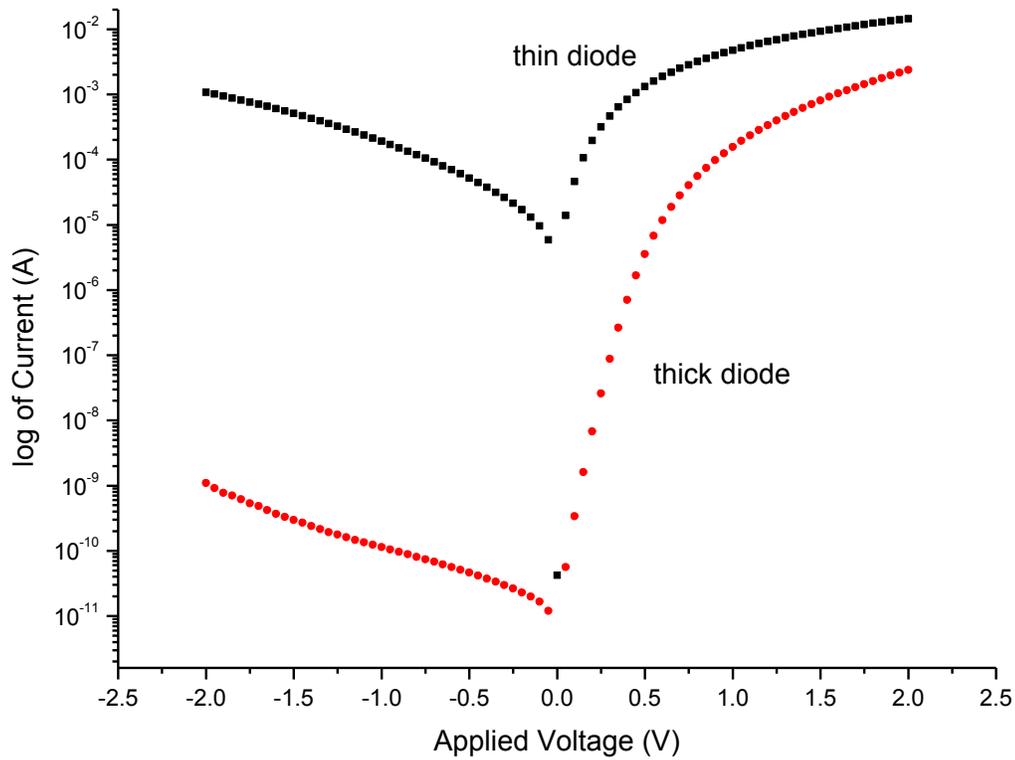


Figure 3.8: Forward and reverse bias current for thin and thick $150 \times 150 \mu\text{m}^2$ nc-Si:H diodes

The non-ideality factor for a diode indicates how well the forward bias IV curve fit the exponential model for a diode. Equation (3.4) shows the non-ideality factor “n” as part of the diode current equation [30].

$$I = I_{Sat} \left[\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1 \right] \quad (3.4)$$

I is the diode current, I_{Sat} is the reverse saturation current, k is the Boltzmann Constant, T is temperature in Kelvin, V is the applied voltage, q is the electron charge and R_s is the series parasitic resistance.

The non-ideality factor was extracted by taking natural log of the IV measurement data and finding the slope with respect to forward bias voltage between 0.2 to 0.5 V. The voltage values were chosen to avoid taking into account other parasitic effects that cause the deviation from the exponential IV curve, such as when SCLC or resistive effects change the current behavior.

The large non-ideality factor for the thin diode, with a value of 8 when typical values are 2 or less, also pointed to the fact that the thin diode did not behave like a diode. The large non-ideality factor could be due low film thickness, which allowed other current mechanism to dominate, such as tunnel current or side-wall leakage current.

Based on these results, a decision was made to only study the thick diode further, as the thin diode did not behave like a diode, with clear differences between forward and reverse bias. The thick diode would be more suitable for the use in a rectifier which will be discussed later. From this point onwards, the diode discussed will only be the thick diode with 300 nm and 100 nm thick intrinsic and n+ nc-Si:H layers.

A comparison of the current density over the operational voltage range of nc-Si:H diodes of different size is shown in Figure 3.9. In the forward bias regime, the 3 largest sized diodes showed higher current density at high bias than the two smaller ones. This can be attributed to contact resistance limiting current in the $50 * 50 \mu\text{m}^2$ and $100 * 100 \mu\text{m}^2$ diodes. The sizes of the vias opened in the oxide for the top Al contacts were scaled with the diode area in order to preserve a 20 μm error margin for lithography alignment safety. This made the opening in the oxide for the smaller diodes much smaller than the larger diode. The larger diode current density at high bias probably showed the maximum achievable density given the limitation of the carrier mobilities of the nc-Si:H. The $150 * 150 \mu\text{m}^2$ had the highest current density, with the 2 larger diodes slightly dropping off in efficiency with respect to the area. However, there was still a linear increase in the current with increase in diode area.

In the reverse bias regime, smaller diodes had larger current density. This could be due to dominance of sidewall leakage current, at the edges of the junction, instead of bulk leakage current as there was an increasing drop in reverse current density with increasing area [31].

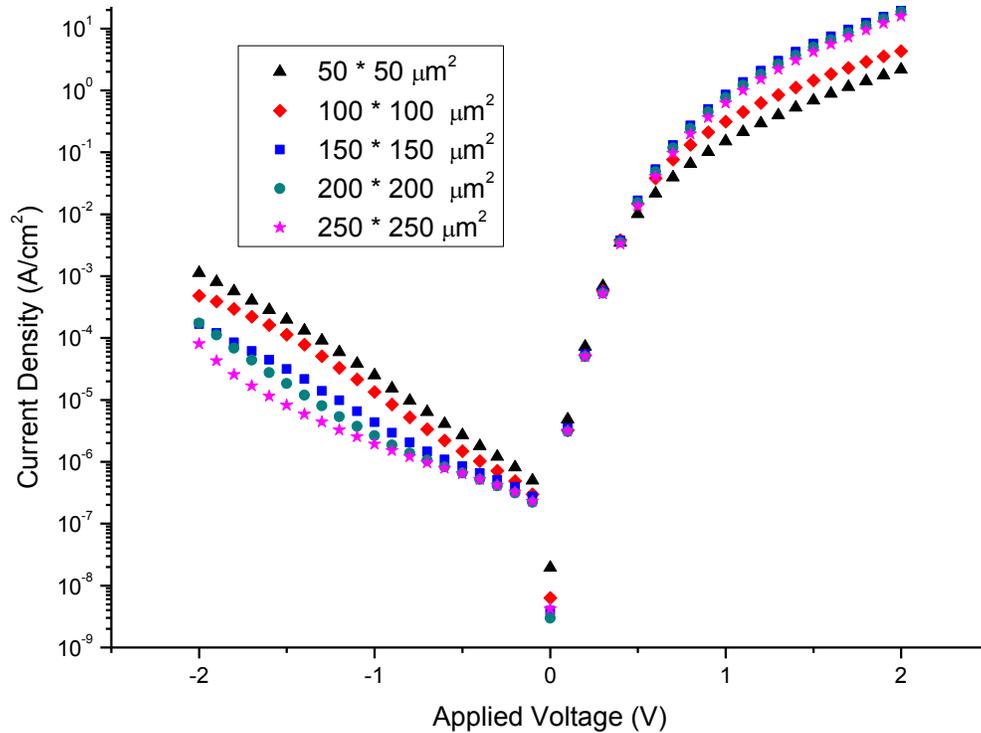


Figure 3.9: Current density of nc-Si:H diodes of different sizes

3.4 Breakdown Voltage of the nc-Si:H Diode

The reverse bias breakdown voltages were measured for all diodes with different sizes and the results are shown in Figure 3.10. The breakdown voltage is defined as the one at which the reverse current takes a sudden jump and after which, the diode loses its rectification ability even at low reverse bias. The larger diodes, the $250 * 250 \mu\text{m}^2$ and the $200 * 200 \mu\text{m}^2$ ones, the reverse breakdown voltages are lower than for the smaller diodes. The breakdown voltages were 15 V and 15.5 V respectively for $250 * 250$ and $200 * 200 \mu\text{m}^2$ diodes. The smaller diodes had a 16.6 – 16.7 V breakdown voltage instead. However, except for the smallest $50 * 50 \mu\text{m}^2$ diode, all of the other diode breakdowns occurred at the approximately same current value of 3.8 mA. This pointed to the fact that the breakdowns were not caused by excessive voltage or electric field, but by excessive current flow. The difference in breakdown voltage can simply be attributed to the larger diodes requiring smaller voltages to achieve the same breakdown current. The flat current measured for the diodes after breakdown was due to limitation of the Keithley, which could only supply current up to 0.105 A for the voltages measured. All of the diodes after reverse bias breakdown behaved as highly conductive resistive elements.

The 50 * 50 diode behaved differently than the rest of the diodes. The breakdown voltage was the highest among the diodes measured at 16.7 V; however, the breakdown current level was only 0.44 mA, almost an order of magnitude smaller than for other diodes. Furthermore, at 20.5V bias, the smallest diode went from highly conductive to highly resistive. This was probably due to high current flow, leading to resistive heating and physical destruction of small part of the diode and thus leading to a partial open fault. The high current flow was due to the lack of a resistor in the test circuit to limit current. Given small physical dimensions of the 50 * 50 μm^2 diode, the diode would have been more susceptible to current crowding thus leading to resistive heating and hence to physical destruction. Discoloration was actually observed at the contact between the Cr and intrinsic nc-Si:H in the 50 * 50 μm^2 tested, and after undergoing high bias, high current of at least 100 mA was observed across the diode in both forward and reverse bias. Figure 3.11 is an optical micrograph of the damage to nc-Si:H diode after very high current flow. The Cr contact pad on the left had been destroyed along with some of the nc-Si:H film on the left side of the diode, close to the Cr contact pad.

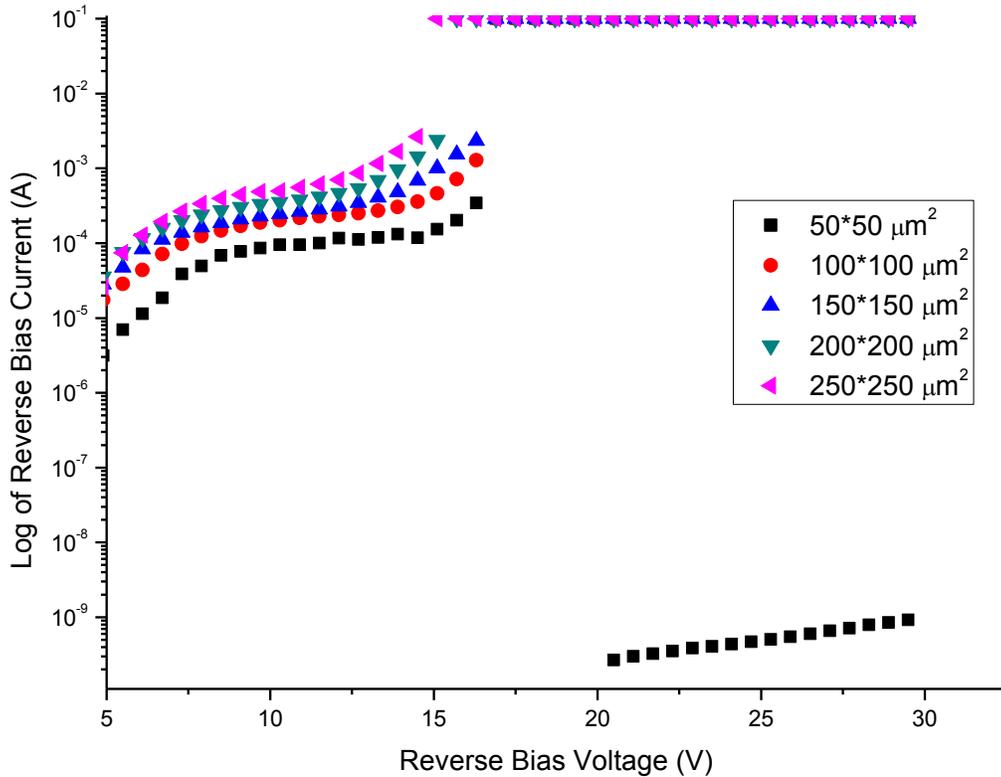


Figure 3.10: Reverse bias breakdown of nc-Si:H diodes of various sizes

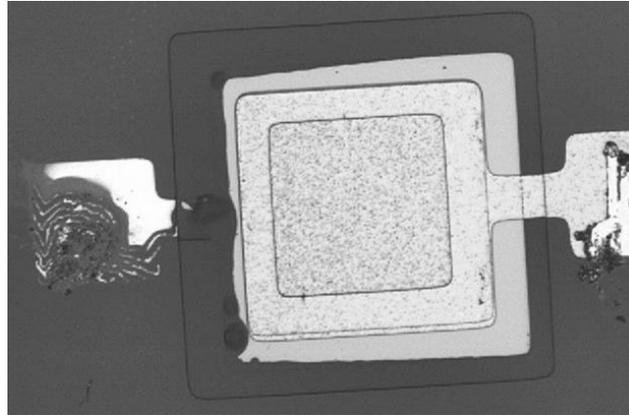


Figure 3.11: Optical micrograph of nc-Si:H diode showing physical destruction after high current flow

3.5 Capacitive Measurements of the nc-Si:H Diode

The capacitance-voltage measurement reveals information on the depletion width that exists inside the diode. Furthermore, capacitance of the diode as it changes with bias and frequency is an important parameter to design optimal RF circuits when employed in an actual RFID tag [32]. The values of the capacitances measured under reverse bias are shown in Figure 3.12. Results from using two different frequencies of AC signal are shown: quasistatic (20Hz) and high frequency (1 MHz).

The 20 Hz frequency was the lowest possible allowed with the measuring equipment. At high values of the reverse bias, the capacitance fluctuated wildly when measured at 20 Hz. This was true for both diode sizes, with some results even indicating negative capacitance. These fluctuating values can be attributed to deep carrier traps that exist inside nc-Si:H material. At high reverse bias, many of these traps were occupied by the carriers. The carrier release time from these traps are independent random events, thus leading to fluctuating capacitance results as the carriers were captured and released randomly at higher bias.

There was a slight decrease in capacitance in the nc-Si:H diodes when reverse bias was increased. This effect lasted until approximate 0.7 V, when the capacitance value stayed constant for higher biases. This indicated that the nc-Si:H diodes were close to being fully depleted, where a slight increase in reverse bias fully depleted the nc-Si:H films. At reverse bias, the capacitance of a diode is attributed to the junction capacitance where the charges are separated by the space charge region. As the space charge region expands with increasing reverse bias, the capacitance value drops. This can be understood from the simple parallel plate capacitance model given by

$$C_j = \frac{\epsilon' A}{d} \quad (3.5)$$

Where d is the separation of the carrier, A is the area of the capacitor and ϵ' is permeability of the material. After becoming fully depleted, the space charge region could not grow any further, d remains constant, thus the capacitance remained constant.

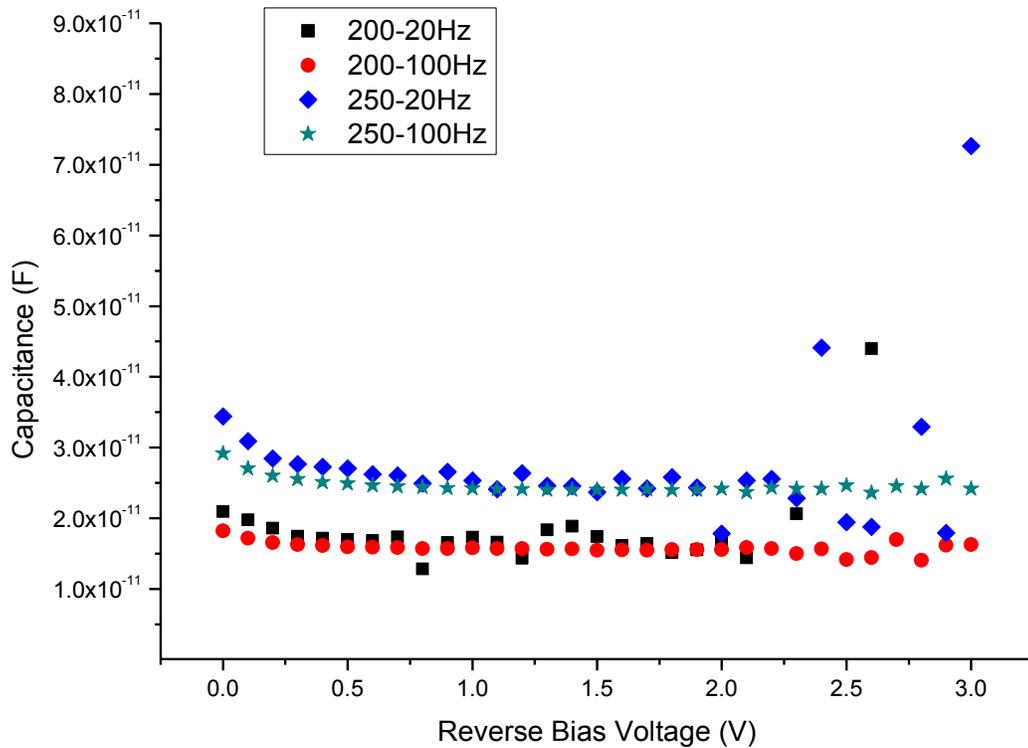


Figure 3.12: Capacitance measured in reverse bias regime for nc-Si:H of 200 * 200 μm^2 and 250 * 250 μm^2 sizes using 20 and 100 Hz AC signal

Figure 3.13 shows the nc-Si:H diode capacitance measured at forward bias, where it is the diffusion capacitance attributed to the distribution of carriers under forward bias. The capacitance showed an exponential growth similar to the exponential dependence of minority carrier with applied voltage. The 250 * 250 μm^2 diode showed larger capacitance values due to its larger area than the 200 * 200 μm^2 diode.

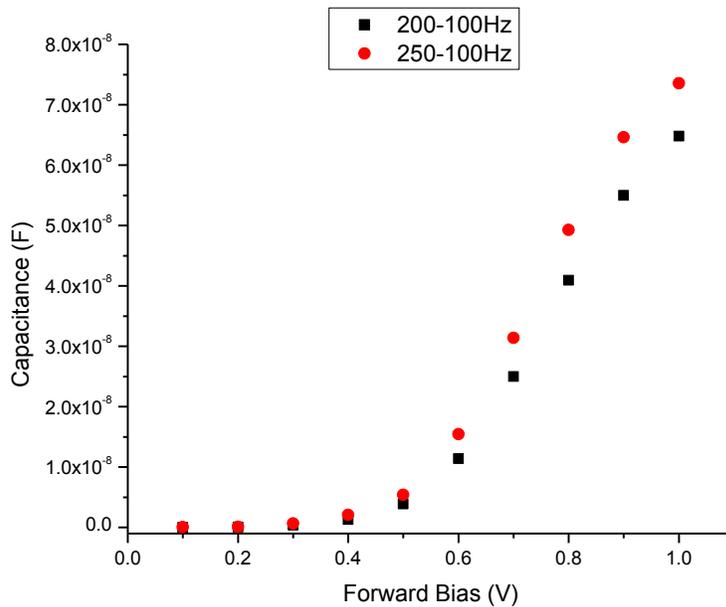


Figure 3.13: Forward bias capacitance of nc-Si:H of $200 \times 200 \mu\text{m}^2$ and $250 \times 250 \mu\text{m}^2$ sizes at 100 Hz

3.6 Current rectification mechanism in nc-Si:H Diode

One important question to investigate about the nc-Si:H diode was whether the diode I-V characteristic observed was due to a Schottky diode formed between the chromium and intrinsic nc-Si:H or a p-n junction diode between the intrinsic nc-Si:H and n+ nc-Si:H.

The original design of the nc-Si:H diode called for a Schottky diode. Schottky diodes typically are able to respond faster due to low diffusion/junction capacitance and are able to drive a larger current than p-n junction diodes. These two properties made them more suitable for the use in rectifiers that need to respond to input AC signal at MHz frequency [32], [33].

The work function of Cr is 4.5 eV and the electron affinity of nc-Si:H is assumed to be 4.01eV. This gave a theoretical ideal barrier height for the Schottky diode between the chromium and intrinsic nc-Si:H to be 0.5eV [32].

In order to elucidate the true nature of the diode observed, the IV measurements for the diodes were compared with theoretical models. The current for a Schottky diode can be attributed to four different sources: thermionic emission (TE), tunneling, generation-recombination and leakage. The models for these current are shown in Equation (3.6) [30].

$$I = I_{TEO} \left[\exp\left(\frac{q(V - IR_S)}{kT}\right) - 1 \right] + I_t \exp\left(\frac{q(V - IR_S)}{E_0}\right) + I_{gr} \left[\exp\left(\frac{q(V - IR_S)}{2kT}\right) - 1 \right] + \frac{V - IR_S}{R_L} \quad (3.6)$$

Where I_{TEO} , I_t , I_{gr} are the saturation current for thermionic, tunneling and generation-recombination respectively. V is the applied voltage, R_S is the parasitic resistance, R_L is the leakage current parameter, E_0 is the tunneling current parameter, k is the Boltzmann's constant and T is the temperature in Kelvin. To simplify Equation (3.6), the simplified diode current equation as shown in Equation (3.4) is used. The value of the non-ideality factor "n" shows which component of the current is dominant [30]. When $n = 1$, it is the TE current that is dominant. Likewise, when $n = 2$, then the generation-recombination current is dominant. For other values of n , tunneling current and leakage current play the role [30].

The thermionic emission saturation current, I_{TEO} , is related to the Schottky barrier height, as shown in Equation (3.7).

$$I_{TEO} = SA^{**}T^2 \exp\left(-\frac{\phi_{B0}}{kT}\right) \quad (3.7)$$

Where S is the surface area of the diode, A^{**} is the effective Richardson constant, k is the Boltzmann's constant, T is the temperature and ϕ_{B0} is the barrier height [30]. In order to accurately calculate the barrier height, the non-ideality factor for the diode should be 1 or as close to 1 as possible. As previously stated, the non-ideality factor for the thick nc-Si:H diode was 1.85. Next, additional IV measurements were carried out at various temperatures (in the range from -30 °C to 125 °C) to see if there is a temperature for which the diode current was dominated by TE. In Figure 3.14, the non-ideality factor extracted from different temperatures is shown. As can be seen, the factor did not approach 1 over the measured temperature range. The values of the factor varied between 1.82 to 2. It should be noted that only limited range of temperatures was available due to equipment limitation: the probe station heating stage on which the measurement was carried out had a maximum temperature of 125 °C. It is still possible that at higher temperature than 125 °C, the diode current would become dominated by TE.

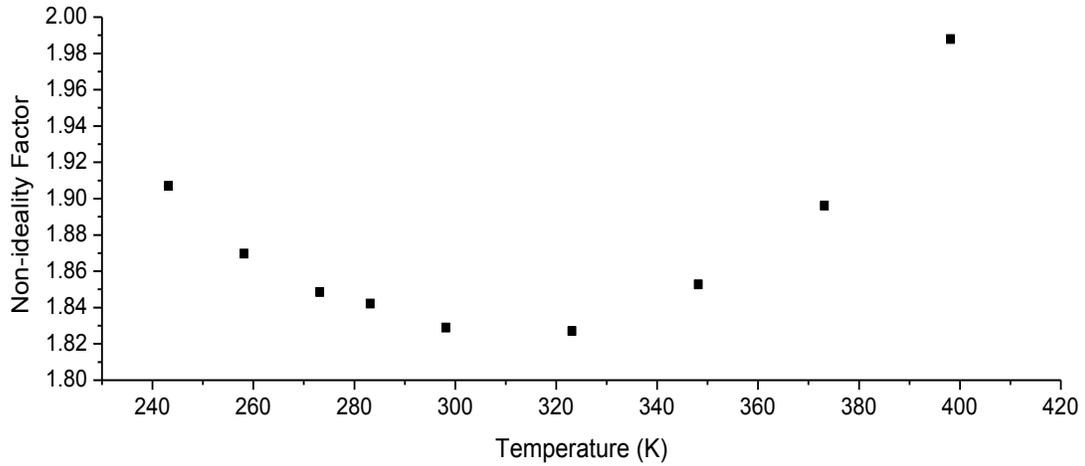


Figure 3.14: Non-ideality factor extracted from IV measurements for the nc-Si:H over various temperatures

Even though the IV measurements within the available temperature range all showed non-ideality factors greater than one, an estimation of the barrier height could still be made. Under the assumption that the current was dominated by TE, the TE saturation current and the barrier height were extracted using the IV data measured versus temperature. The assumption was made to allow for estimating the barrier height with the available data. By taking natural log of the current density, and then finding the intercept with respect to voltage, the natural log of the I_{TEO} values were obtained at different temperatures. Using the natural log of I_{TEO} , the barrier heights were estimated from the slopes with respect to $1000/T$ (Arrhenius plots).

The average barrier height calculated was 0.605 eV with a standard deviation of 0.015 eV over 7 different samples. This calculated barrier height of 0.6 eV was 0.1 eV over the theoretical value of the 0.5 eV Schottky barrier height for a Cr / intrinsic nc-Si:H junction which was a significant amount. Furthermore, the 0.6 eV value corresponds well with the difference in Fermi energy level between the n+ nc-Si:H layer and the intrinsic nc-Si:H. The Fermi energy value was within millielectronvolts of the conduction band in the n+ nc-Si:H layer as shown previously by the n+ activation energy measurements. Assuming the intrinsic nc-Si:H had a Fermi energy level in the midgap due to the charge trapped on deep defects (dangling bonds), and nc-Si:H bandgap of approximately 1.2 eV which is close to the crystalline silicon bandgap [32], this would lead to a barrier of approximately 0.6 eV for a junction formed between the intrinsic and n+ nc-Si:H layers.

Furthermore, the initial assumption for the Schottky barrier estimation was that all of the current in the diode was due to TE. However, from the non-ideality factor values of approximate 1.8,

the diode current was not all from TE. Rather, TE was only a part of the total diode current. The assumption made led to an underestimation of the barrier height, as the actual TE current in the diode was lower than that used for the calculations. Bandgap values for nc-Si:H as high as 1.6 eV had also been reported [1] which would correspond to a higher theoretical pn junction barrier value of 0.8eV matching the underestimation. This was further evidence that the diode was not a Schottky diode.

As one final test, a sample was fabricated with the n+ and intrinsic nc-Si:H layers reversed, with the n+ layer in contact with the Cr instead. What was discovered was that the diode still existed, but the polarity of the diode was reversed. This was further evidence for the p-n junction between causing the occurrence of diode characteristics.

One other conclusion drawn from this was that Cr forms an ohmic contact with intrinsic nc-Si:H. This conclusion was previously drawn by C. H. Lee from nc-Si top gate TFT characteristics and was attributed to chromium silicide formation at the interface between Cr and nc-Si:H [22]. However, it was not confirmed by other researchers until recently[34]. Our results here once again confirmed the existence of ohmic contact between a bottom layer of Cr with an intrinsic nc-Si:H on top.

3.7 Rectifier Measurement Setup

Two types of rectifiers were made using the nc-Si:H diodes and were measured for their ability to convert alternating current (AC) electrical wave form to direct current (DC) voltage. One of the rectifier setups simply consisted of a single diode; as the AC signal swung between positive and negative voltages, the positive voltage would be allowed to pass. The second rectifier setup was a full-wave bridge rectifier consisting of 4 diodes. A microscope picture of a 4 diode setup for the full-wave rectifier can be seen in Figure 3.15

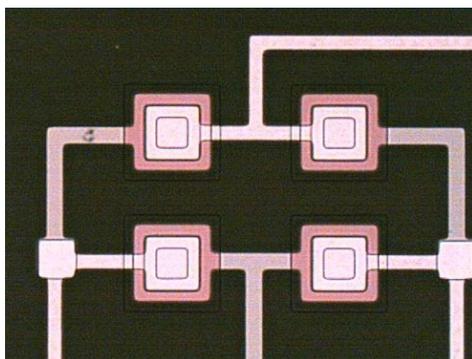


Figure 3.15: 4 nc-Si:H diodes connected in a full-wave bridge rectifier format with contact pads outside the picture

A full-wave rectifier operates for both positive and negative half-periods of the AC signal at an additional cost of more diodes, larger area consumed and more complex routing.

To measure the effectiveness of the rectifier, a test circuit was setup. Schematic of the two rectifiers along with the test circuit can be seen in Figure 3.16.

The AC source in the figure is a wave form generator which was used to input a sine wave signal of various frequencies into the circuit. The frequency ranged from 1 MHz to 16 MHz to understand the effect of frequency on the output voltage. The range covered the important 13.56 MHz frequency that had been designated as a standard RFID frequency which other researchers had also designed rectifiers to operate at. Constant amplitude of $2 V_{RMS}$ was selected for the sine wave input. The sine wave input was selected because of its typical use in amplitude modulation scheme used in RFID communication standards and to be comparable with previous research work done thus allowing for comparison of results.

A $1 M\Omega$ resistor and a $0.22 \mu F$ capacitor served as the load. A Fluke 179 multimeter was used to measure the DC voltage drop across the resistor to determine the output DC voltage.

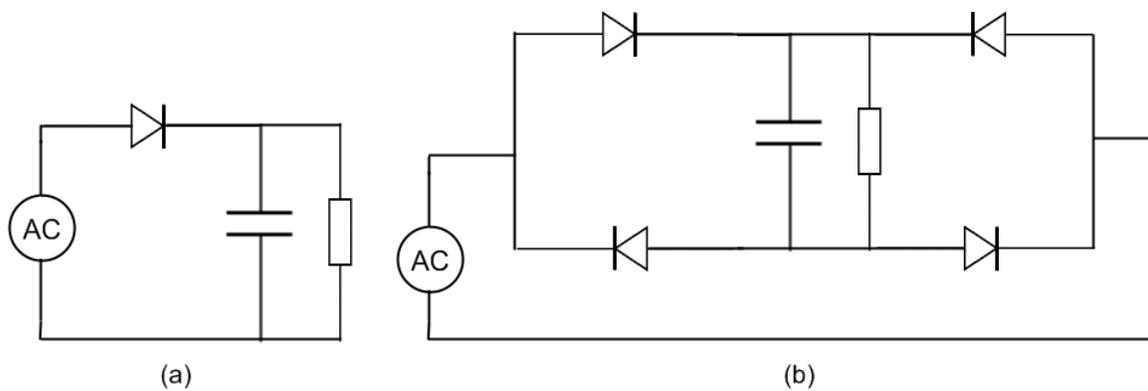


Figure 3.16: Setup for rectification measurement (a) with a single diode and (b) with 4 diodes in full-wave bridge rectifier

3.8 Rectifier Measurement Results

The measured DC voltage output of two different rectifiers described above can be seen below in Figure 3.17 and Figure 3.18, respectively. Diodes of different sizes were used in each case to make the rectifiers and the results are shown in both graphs.

One can see that at AC signal of higher frequencies, the DC output voltage dropped for all measured rectifiers except for one. The drop in DC output could occur due to several effects.

First explanation of the drop in DC output was due to limited carrier mobility in nc-Si:H films. Defect states and traps in the nc-Si:H films reduced the mobility of the carriers. With an AC signal input, the nc-Si:H diodes effectively were switching back and forth between forward bias and reverse bias. As the switching occurred, the carriers moved to either fill the minority carrier profile of either the on state or off state and this required a certain amount of time. At higher frequency, the time left for current conduction in the on state was reduced as the on transient time remained the same. That combined with a minimum voltage before the diodes turned on, led to less current flowing out of the rectifiers at higher frequencies.

Another reason for the drop of DC output voltage was related to the test circuit setup. The sample diodes were connected to the test circuit using a probe station along with micron-sized probe tips because the samples were not diced and wire-bonded. The probe tips had significant attenuation factor at around 7-8 MHz frequency and beyond because the probe tips used were designed for DC measurements only. In order to eliminate this factor, two probe tips were connected to a strip of metal on one of the sample wafers. Sine wave was sent in through one probe tip and measured with an oscilloscope at the other probe tip. 1000 times and more attenuation of the magnitude of the sine wave were observed on the oscilloscope. The attenuation increased with increasing frequency. Thus one contributing factor of the decreasing DC output could be decreasing AC signal magnitude at higher frequencies.

The DC output voltage for the single diode rectifier using a $250 * 250 \mu\text{m}^2$ was the only sample which did not drop at higher frequencies. This could be due to the capacitance and inductance from the diode and the metal contact pads. The design of diodes and metal contact pads did not take into account the target frequency of 13.56 MHz. There were no optimizations done to try to increase the Q factor of the overall circuit. As it turned out, the capacitance and inductance in the $250 * 250 \mu\text{m}^2$ sample created a more optimal circuit for the coupling of the AC signal to the diode. The $200 * 200 \mu\text{m}^2$ single diode rectifier also displayed a less dramatic drop in DC output as well.

Comparing the ability of the single diode rectifier versus the full-wave bridge rectifier, it was apparent that the full-wave bridge rectifier was able to significantly outperform the single diode rectifier. Only the 2 biggest single diode rectifiers, the $250 * 250$ and $200 * 200 \mu\text{m}^2$ had comparable output at the target 13.56 MHz with the full-wave bridge rectifiers. The full-wave rectifiers provided an additional 0.5 – 1V higher output voltage compared to single diode rectifier of the same size. In

single diode configuration, the largest $250 \times 250 \mu\text{m}^2$ diode is able to output 2 V DC at 14 MHz. In full-wave bridge rectifier configuration, the largest diodes used had area of $200 \times 200 \mu\text{m}^2$ and this full-wave bridge rectifier can output 2.6 V DC at 14 MHz. During design stage, full-wave rectifiers using $250 \times 250 \mu\text{m}^2$ diodes were not designed into the mask thus there was no data available for comparison.

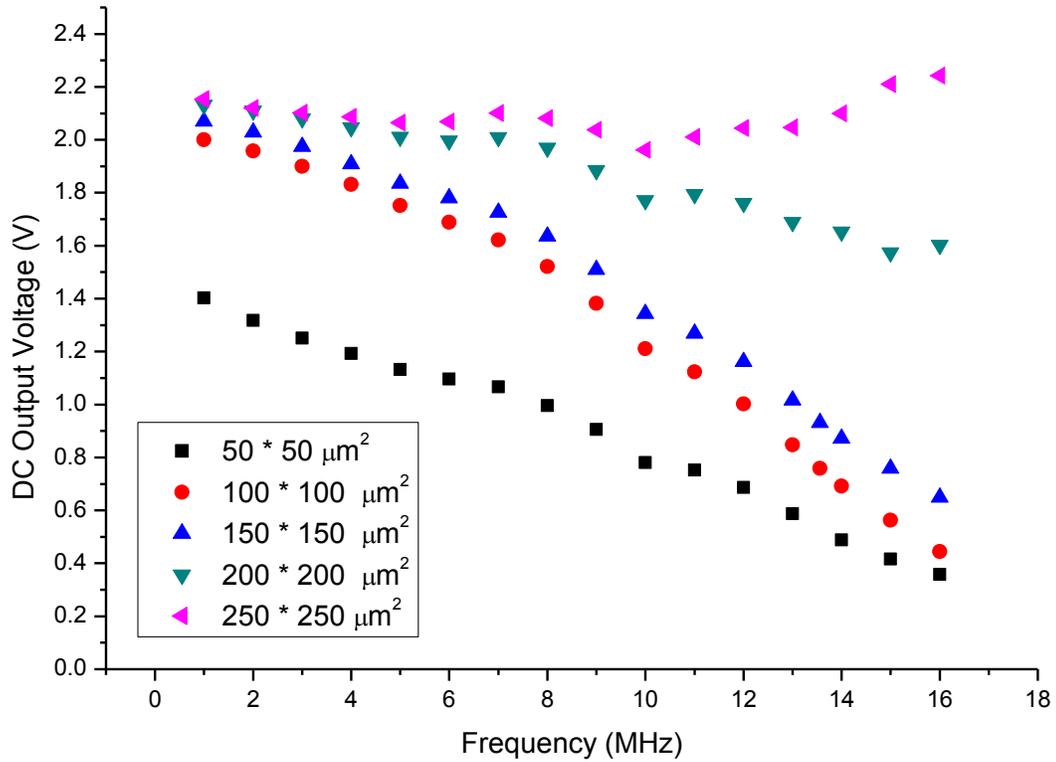


Figure 3.17: DC output voltage of single diode rectifiers versus input AC signal frequency

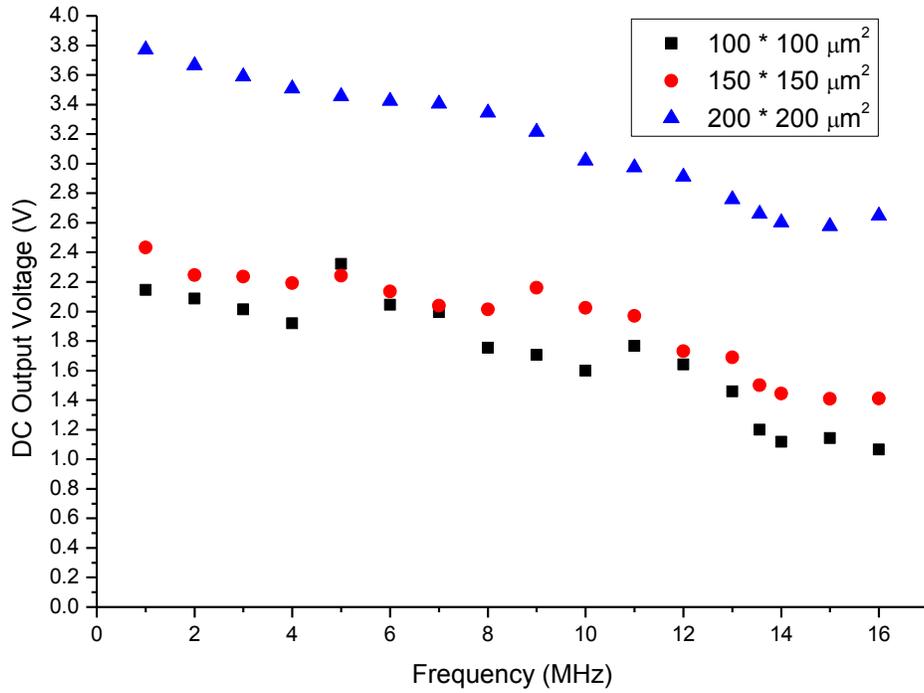


Figure 3.18: DC output voltage of full-wave bridge rectifiers versus Input AC signal frequency

3.9 Comparing nc-Si:H Rectifiers with Rectifiers Made by Other Technologies

Other researchers have attempted to make rectifier using organic semiconductors for RFID applications also. This team from the company OrganicID, Inc. and the University of Texas at Austin, R. Rotzoll et al. fabricated a full-wave bridge rectifier circuit using 4 p-type pentacene thin film transistors (TFTs). The TFTs had a mobility of $0.296 \text{ cm}^2 / \text{V s}$ and a channel length of $3 \text{ }\mu\text{m}$. The cross section of the organic TFT and the rectifier circuit can be seen in Figure 3.19 [35].

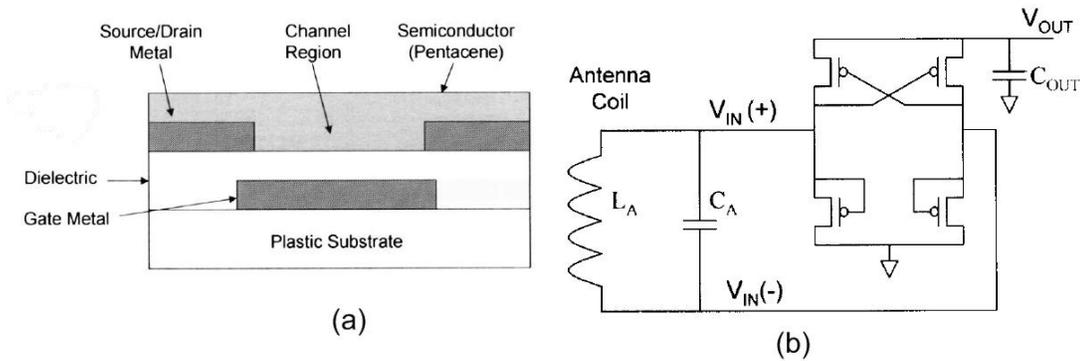


Figure 3.19: (a) Pentacene-based bottom gate TFT and (b) Full-wave bridge rectifier circuit made using the TFTs [35]

The rectification results of the organic rectifier are shown in Figure 3.20. In order to compare our rectifiers with those made by OrganicID, the test conditions of the nc-Si:H diode were selected to mimic the test conditions of the organic rectifier for ease of comparison. For the organic rectifier, the resistive load used at the output of the rectifier was 10 M Ω and the data showed results using 10 V_{RMS} input amplitude for the AC signal [35].

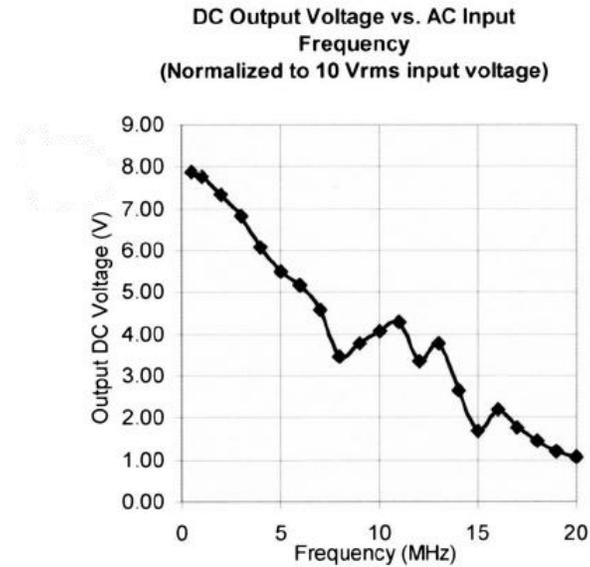


Figure 3.20: Rectification result of organic rectifier vs AC input frequency [35]

The DC output voltage for the organic rectifier measured also showed a dropping output when AC frequency was increased. This was attributed to the limited mobility of the organic TFTs used, where the TFTs were operating in a “nonquasistatic (NQS) operation” mode. NQS operation meant that the TFT was not conducting the maximum current possible due to the rapid changing voltage at the TFT’s input [12].

The organic TFT was able to output 2.8 V at 13.56 MHz, which was comparable to the 2.6 V generated by the nc-Si:H full-wave bridge rectifier. However, the input voltage for the organic rectifier was at 10 V_{RMS} while the nc-Si:H rectifier input voltage was only 2 V_{RMS}. This meant that the nc-Si:H was approximately 5 times more power efficient than the organic rectifier.

Furthermore, the organic rectifier circuit was tuned to operate at 13.56 MHz, by designing the antenna and the capacitance C_A as seen in Figure 3.19 (b) to get a resonant quality factor (“Q” factor) specifically for 13.56 MHz. None of this work was done for the nc-Si:H circuit. The capacitance of the nc-Si:H diode and the contact pads used were not specifically designed for radio frequency use.

Compounded with the lower load resistance used for the nc-Si:H rectifier test circuit, there is very much a chance for even better results from the nc-Si:H rectifier if more engineering work is done to design specifically for 13.56 MHz [33].

3.10 Further Work in nc-Si:H Diodes for Rectification

A working nc-Si:H rectifier has been demonstrated which showed the ability to best organic semiconductor-based rectifier. The next steps to further proving the viability of nc-Si:H as a material for fabricating RFID tags are to fabricate the rectifier on plastic substrate and to fabricate the rectifiers along with working n-type and p-type nc-Si:H thin film transistors. Other researchers in the group have shown working nc-Si:H TFTs of both n-type and p-type fabricated using the same machines [2] [14]. For a truly working RFID tag prototype, a combination of a metal antenna, a nc-Si:H rectifier and nc-Si:H TFTs arranged in a ring oscillator format would be ideal.

Including p-type nc-Si:H TFTs would be an advantage when compared with organic semiconductor. Power efficient digital circuits require both n-type and p-type transistors to form true complementary circuits like Complementary Metal Oxide Semiconductor (CMOS) in crystalline silicon chips. CMOS chips are more power efficient than circuits with only n-type or p-type transistor because of the elimination of short circuit current and short circuit power during idle periods in the circuit operation. Organic semiconductors have been traditionally limited to p-type materials with acceptable carrier mobilities.

Organic semiconductor has been touted to have low cost manufacturing capabilities through the use of spraying or inkjet printing the organic material. However, nc-Si:H also has the capabilities for low cost manufacturing. By doing large area PECVD on flexible substrate, continuous reel-to-reel nc-Si:H device manufacturing is also possible.

4 Nanocrystalline Silicon for Light Emitting Diode

4.1 LED Design

The cross section layer-by-layer view of the nc-Si:H LED can be seen in Figure 4.1 The LED was designed to also be a vertical p-i-n diode with the trilayer of nc-Si:H deposited all at once in the PlasmaTherm PECVD machine. The substrate used for this experiment was Eagle 2000 glass wafers which had been cleaned using standard RCA1 technique.

The bottom metal contact was aluminum sputtered using the Edwards RF sputtering machine. The Al was not patterned and formed a continuous layer across the bottom. Besides being the bottom contact of the diode, the Al layer was intended for use as a mirror-like reflector for any light generated in the LED that emitted downwards. The Al layer would reflect light back upwards which was the intended direction of emission.

The zinc oxide (ZnO) layer at the top of the p-i-n diode was the top metal contact. ZnO is a transparent conductive oxide (TCO) which as the name states, is transparent and conductive. The transparency of the ZnO was necessary to allow light generated inside the LED to be visible. If a metal was used for top contact, the light would be reflected back downwards. The ZnO film was deposited using the RF sputtering chamber of the MVSystem Reel-to-Reel machine with a ZnO target. The thickness of the ZnO film was approximate 120nm thick. A characterization of the ZnO film used will be presented in a following section.

The trilayer of nc-Si:H were deposited using the PlasmaTherm PECVD machine. The n+ and intrinsic layer used the same deposition condition as previously used for the rectifier diode. The p+ layer used conditional optimized by fellow researcher Dr. Hyung Jung Lee. The gas trimethylboron $B(CH_3)_3$, also known as TMB, was used as the doping gas, which donated boron dopant atoms to the film for doping to p-type. The TMB to SiH_4 dilution ratio of 0.5% was used, which was found to produce a p-type nc-Si:H film with the highest dark conductivity [2]. All the other deposition parameters, such as chamber temperature, RF power, hydrogen dilution were kept the same for all three films.

The thicknesses of the three films were 10 nm, 10 nm and 10 – 20 nm for the n+, p+ and intrinsic film respectively. The n+ and p+ films were kept thin to avoid absorbing light generated in the intrinsic layer. The intrinsic layer was also kept thin in hopes of constraining the size of the silicon

nanocrystals found inside the film. The target was for nanocrystals of size less than 10 nm which would be used to generate light.

The p+ film was selected to at the top of the trilayer because of the different mobilities of the holes and electrons inside nc-Si:H films. Typically, the mobilities of the holes in nc-Si:H are much smaller than electrons, approximately $1 \text{ cm}^2/\text{V s}$ compared to $100 \text{ cm}^2/\text{V s}$ for holes and electrons respectively. This means that holes injected from the p+ layer would travel much shorter distance into the intrinsic nc-Si:H than the electrons injected from the n+ layer. This leads to the recombination of electrons and holes occurring much closer to the p+ layer than the n+ layer, thus the p+ layer was placed at the top of the stack so that the light would be generated closer to the exit of the stack [36].

The fabrication process was a simple 1 mask process. The Al was first sputtered on a cleaned glass wafer and then the trilayer nc-Si:H films were deposited consecutively without breaking vacuum. The ZnO was then sputtered on using the Reel-to-Reel system. Afterwards, photolithography was carried out using a mask with square of various sizes to define LEDs of different sizes. 10% Hydrochloric acid (HCl) was used to etch to the ZnO film. Due to the high etch rate with 10% HCl, there were some over etching of the ZnO film under the photoresist. Keeping the photoresist on, the trilayer nc-Si:H films were patterned using RIE with sulfur hexafluoride (SF_6) and oxygen (O_2) gases.

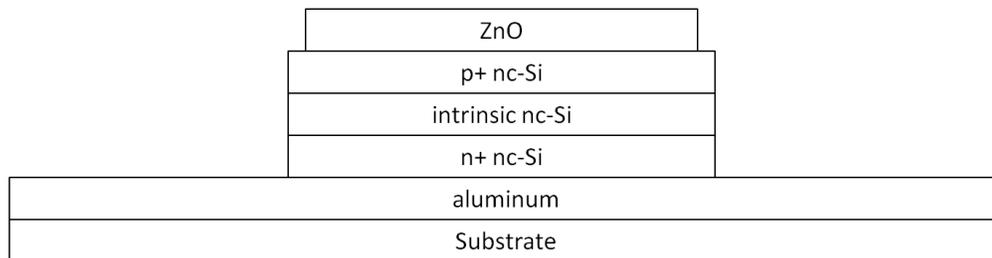


Figure 4.1: Cross section of nc-Si:H LED

For the final LED fabricated, two different sets of samples were made. One set was made with a 3:00 minute deposition for the intrinsic nc-Si:H layer and another was made with a 6:00 minute deposition. As shown later, this would correspond to a 12 nm and 20 nm thick layer of intrinsic nc-Si:H for the 3:00 minute and 6:00 minute sample. The two samples will be referred to as LED03 and LED06 for the 3:00 minute and 6:00 minute sample respectively.

4.2 Intrinsic nc-Si:H Thin Film Study

The key layer for the nc-Si:H LED was the intrinsic nc-Si:H layer. The intrinsic nc-Si:H traditionally had lower defect density than doped nc-Si:H films [26]. The lower defect density should lead to more efficient light emission. Thus the intrinsic layer was the focus for studying light emission characteristics in nc-Si:H deposited by PECVD technique. Intrinsic nc-Si:H films deposited using PlasmaTherm PECVD with such low thicknesses had not be characterized previously. Thus several experiments were carried out to understand the films with a 20 nm thickness or less.

Thin layers of intrinsic nc-Si:H layers were deposited using the same recipe outlined in previous chapters. The thickness was varied by controlling the deposition time. The deposition time ranged from 1 minute to 6 minutes. The thickness of the films was measured using the Dektak 8 profilometer after using photolithography to etch lines on the films. Crystallinity of the films was measured using the Renishaw micro-Raman 1000 spectrometer using a 488 nm blue laser using the same Equation (3.1) to calculate the crystallinity of the samples measured.

One key investigation into the film was to find the average crystallite size of the embedded silicon nanocrystals inside the film as this would influence the wavelength of the emitted light. This was done through using the PANalytical MRD X'pert Pro glancing incident x-ray deflection (GIXRD) machine.

Due to the thinness of the films, obtaining meaningful XRD results were difficult. The films were 10 – 20 nm in thickness and had measurements with such thickness had not been attempted before. It was discovered that the incident x-ray angle, the omega-incident angle of the machine had to set to a very small value (0.2 °) which was atypical of the machine's normal setting of 0.6 °.

Peaks in the 2θ scan of XRD measurements corresponds to the different crystals orientations inside the nc-Si:H films. The Full-Width-Half-Maximum (FWHM) measured the width of the peak in degrees and could be used to calculate the average crystallite size of the corresponding crystal through the use of the Scherrer Equation [2] shown here as Equation (4.1),

$$d_g = \frac{k\lambda}{B \cos\theta_b} \quad (4.1)$$

Where d_g is the grain size, B is the FWHM, θ_b is the angle of the peak. For the PANalytical GIXRD machine the λ is 1.54056 Å.

Using the built-in software accompanying the GIXRD machine plus a correction factor of 0.4° as measured using a tungsten standard, the FWHM for different peaks were measured and converted to crystallite size.

4.2.1 Intrinsic nc-Si:H Thin Film Thickness and Crystallinity Results

The results from the thickness measurements and crystallinity measurements of the intrinsic nc-Si:H films deposited for various time are shown in Figure 4.2. The sample which only had 1:00 minute of deposition time did not show any response to the Raman spectroscopy and had immeasurable thickness on the profilometer and so was excluded from the results.

The thinnest sample which could be measured was the 2:00 minute sample with a thickness of 10.3 nm. The 2:30 sample shared roughly the same thickness and both sample had large errors for the thickness measurements. For the 3:00 to 6:00 samples, there was linear growth in the thicknesses of the films, from 12 nm to 20 nm.

For the crystallinity results, the thinnest films had 55% and 56% crystallinity for the 2:00 and 2:30 minute sample. The high crystallinity for such thin films could be attributed to the high hydrogen dilution (99%) used, as typically, nc-Si:H contains an purely amorphous incubation layer for the first few nanometers of the film. However, optimized growth conditions have been shown to be able to minimize and even such an incubation layer [21]. Crystallinity grew linearly, similar to the thickness, with increasing deposition time. The crystallinity value maxed out at around 74.5% for the 5:00 and 6:00 sample.

The high crystallinity values indicated the PECVD process potentially would work well for LEDs as the film was dominated by crystals in terms of volume where the nanocrystals were the key sites to cause radiative recombination of carriers. However, the diameter of the nanocrystals were also important in determining if the nc-Si:H films were useful in LEDs or not.

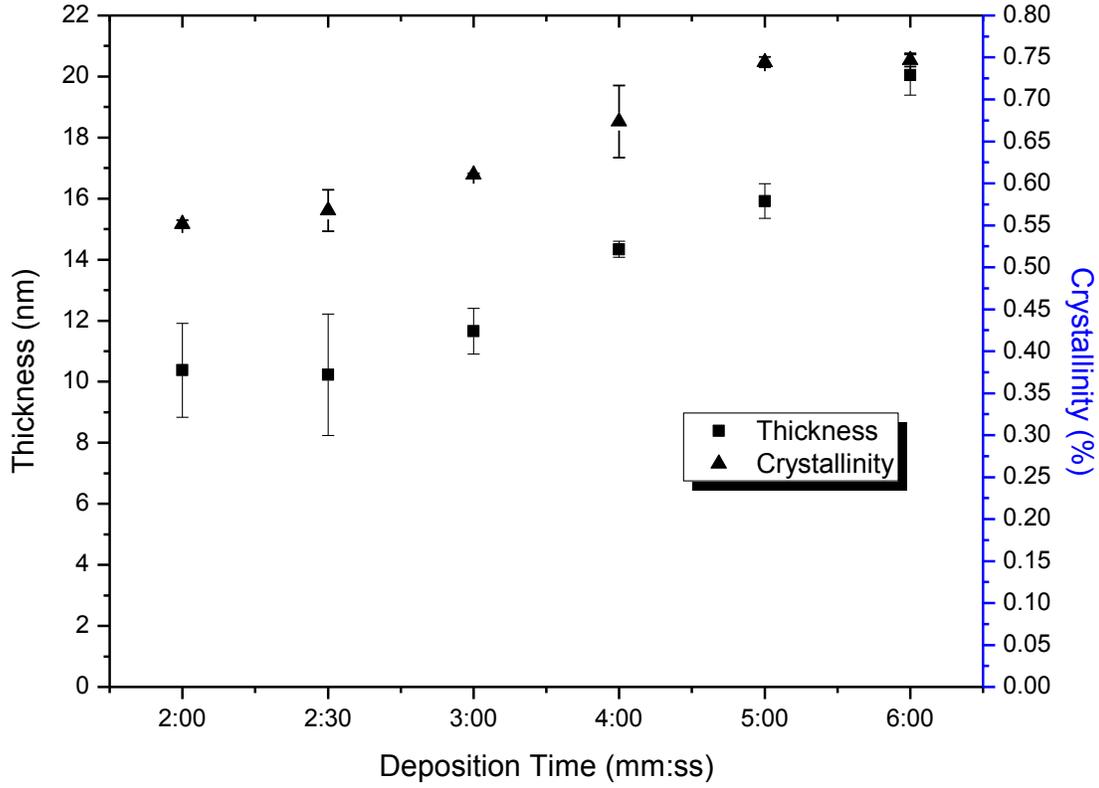


Figure 4.2: Thickness and crystallinity results for intrinsic nc-Si:H films deposited for varying lengths of time

4.2.2 Intrinsic nc-Si:H Thin Film XRD Results

XRD Measurement results of the different thickness nc-Si:H films are shown in Figure 4.3 and Figure 4.4. Two crystalline peaks were measured for the nc-Si:H samples, the (111) and (220) peak. Due to a limitation of time, the 20 nm thick sample did not have its (111) peak measured.

For the thinnest sample, the 12 nm thick intrinsic film, as can be seen from Figure 4.4, there were no measurable peaks. However, Raman measurement suggested that the 12 nm film was indeed partially crystalline and should have had crystallites embedded inside. The missing peak from the XRD measurements could be attributed to the extremely thin sample which had not been attempted before. The XRD measurements were carried out using uncommon settings to even obtain usable results for the thicker nc-Si:H samples. It was possible that due to the thinness of the film, the x-rays were penetrating straight through the nc-Si:H film and were not interacting with the silicon nanocrystals.

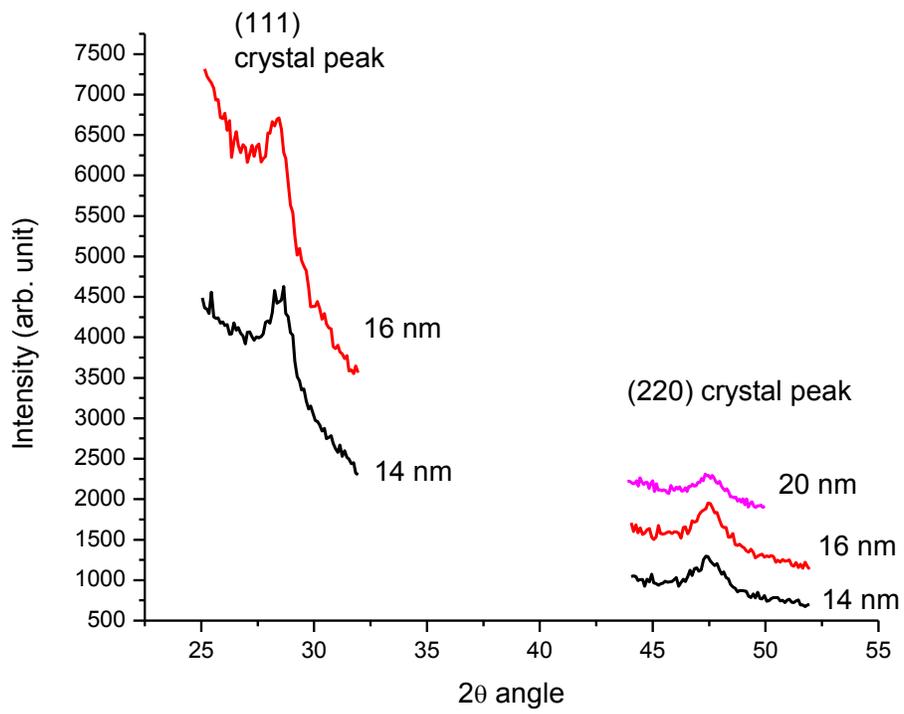


Figure 4.3: 2θ XRD measurement intensity for different thicknesses of intrinsic nc-Si:H films

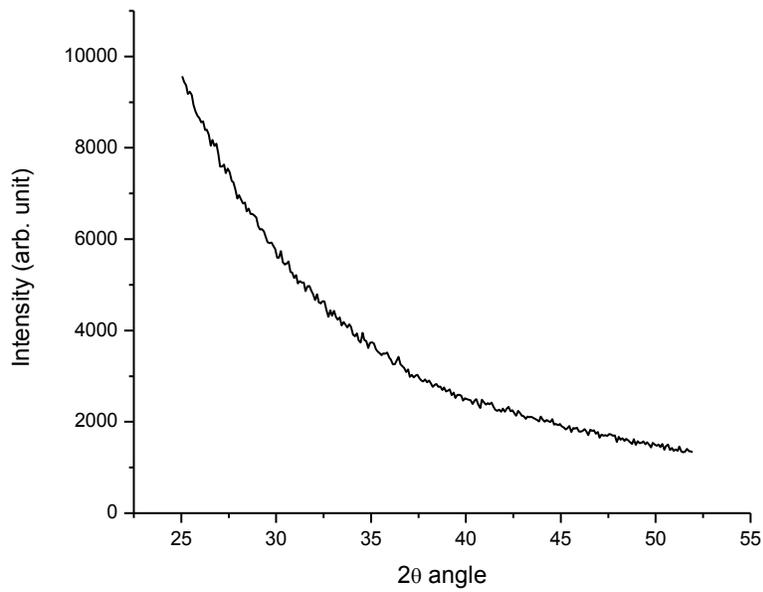


Figure 4.4: 2θ XRD measurement for 12 nm thick intrinsic nc-Si:H films showed no peaks

Table 4.1 lists the 5 identified peaks from the different nc-Si:H samples and their extracted crystallites sizes after using the Scherrer Equation. The average crystallite sizes showed an increase trend with increasing thickness of the films, which was understandable as there were more room for the crystals to grow in the thicker films. The overall crystallite sizes ranged from 7.5 nm to 13.7 nm which were much larger than needed to visible light wavelengths. The corresponding theoretical emission wavelengths from the crystals ranged from 875.2 nm to 962.6 nm, which were in the near infrared region.

Table 4.1: Summary of XRD measurements results and calculated crystallite sizes using the Scherrer equation plus theoretical light emission wavelengths

Film Thickness (nm)	Crystal Peak	FWHM (°)	Peak Position (°)	Crystallite Size (Å)	Wavelength (nm)
14	(111)	1.20	28.62	102	926.8
14	(220)	1.55	47.47	75	875.2
16	(111)	1.00	28.48	137	962.6
16	(220)	1.44	47.52	83	894.0
20	(220)	1.41	47.5	86	900.2

4.3 Zinc Oxide Thin Films Characterization

The top metal contact of the light emitting diode will be a layer of zinc oxide (ZnO) which is a type of transparent conductive oxide (TCO). ZnO is used to allow photon emitted from the middle layers of the LED to escape while still providing a conductive contact area for electrical connection or probing. The design of the LED calls for the use of a thin layers of ZnO, in the range of 100 to 200 nanometer because a thicker ZnO layer will absorb more of the generated photons and thus decrease the efficiency of the LED. There is a tradeoff between the ZnO conductivity and transparency as thicker ZnO film should result in higher conductivity laterally but lower transparency through the film.

ZnO deposition was done using the sputtering chamber of the Reel-to-Reel (R2R) machine through radio frequency (RF) magnetron sputtering of a ZnO target. The R2R system was designed by MVSystem of Colorado and has three chambers: a load lock, a PECVD chamber and a RF sputtering chamber.

The ZnO deposition using the R2R machine was new at the G2N lab, where the other researchers had little experience with the specific process and the machine, especially for thin films of ZnO. Previous trials with the R2R machines deposited 1 μm thick films only. Thus these experiments were performed to characterize ZnO thin films deposited using the R2R machine for transparent top contact uses in LEDs.

4.3.1 Experiment Description

The ZnO thin films were deposited on Eagle 2000 glass wafers after the glass wafers had been RCA1 cleaned. The glass wafers were loaded into the R2R's sputter chamber 1 glass wafer at a time due to the space limitation of the wafer holder of the machine. ZnO thin films were deposited with the R2R machine through radio frequency magnetron sputtering with argon gas and a ZnO target. The base pressure of the sputtering chamber was pumped down to below 6×10^{-6} Torr before deposition was started.

The sputter chamber was set to temperatures of 200 °C or 300 °C using the chamber's graphite heaters. The wafers were left for at least 30 minutes inside the chamber for heating of the substrate holder to stabilize. Two different deposition temperatures were investigated to understand the effect of substrate temperature has on ZnO film characteristics.

The deposition times tested were 4 minutes and 6 minutes. The deposition time were estimated from the previous deposition times used to deposit the 1 μm thick films. The key parameters inputted to the software to control the ZnO sputtering is outline in Table 4.2.

Table 4.2: Deposition conditions for ZnO thin films using the R2R machine

Parameter Name	Value
Argon Pressure	5 mTorr
Argon Flow Rate	30 sccm
RF Power	300 Watts
Temperature	200 / 300 °C
Deposition Time	4 / 6 minutes

The ZnO thin films were then characterized by a variety of methods. Optical transparency of the films was measured using the Shimadzu UV-2501PC UV-vis spectrophotometer from the

wavelength of 190 nm to 900 nm. Infrared transparency of the films was measured using the Shimadzu FT-IR 8400S spectrophotometer, a Fourier Transform Infrared (FT-IR) machine, from wavenumber 7800 cm^{-1} to 350 cm^{-1} .

Resistivity of the films was measured using 4-point probe method with spacing between the probes at $S = 0.1024\text{ cm}$. A BK Precision 1621A DC regulated power supply was used to supply the voltage and voltage drop and current through the ZnO sample were measured using a Fluke 179 multimeter. Given the thin film nature of the film, the resistivity can be calculated using Equation (4.2) [37]

$$\rho = \frac{\pi t}{\ln 2} \left(\frac{V}{I} \right) \quad (4.2)$$

The thickness of the films was measured using the Dektak 8 stylus profilometer after etching 10 nm thin layers using photolithography and HCl.

The ZnO films were also studied before and after a $240\text{ }^{\circ}\text{C}$ anneal for 6 hours to understand the effect of annealing has on ZnO thin film. The annealing was done using a vacuum oven. The temperature of $240\text{ }^{\circ}\text{C}$ was chosen so that the temperature was below that of the deposition temperature of the nc-Si:H used in the LEDs with some safety margins to account for temperature fluctuations in the vacuum oven.

4.3.2 Experiment Results

The thickness of the ZnO thin films are displayed in Figure 4.5. The deposition times estimated from previous experiments was quite accurate. The thickness of the films deposited was between 75 nm to 133 nm. The 6 minute depositions led to higher thicknesses as to be expected.

Interestingly, at $300\text{ }^{\circ}\text{C}$ chamber temperature, the deposition thicknesses were lower than the samples deposited at $200\text{ }^{\circ}\text{C}$. This was something that was unexpected. Evaluated temperatures inside the chamber did lead to an increase in the base pressure which was observed by other users of the R2R machine. At $350\text{ }^{\circ}\text{C}$, the sputter chamber has difficulty reaching acceptable base pressure of $6 * 10^{-6}$ Torr for sputtering. This is possibly due to the out-gassing from the chamber walls given that the R2R machine is a relatively new machine. At $300\text{ }^{\circ}\text{C}$, with a higher pressure inside the chamber, the mean free path of the sputtered ZnO particles may have been shorten and the sputtered material distributed over a larger arc above the target, leading to thinner film deposited.

Film thickness uniformity was good over the wafer. Multiple measurements, more than 6 for each wafer, were taken and the thicknesses measured showed consistencies over the whole wafer. The standard deviations of the thicknesses were between 1 nm to 3.6 nm with the largest one being from sample deposited at 300 °C for 6 minutes.

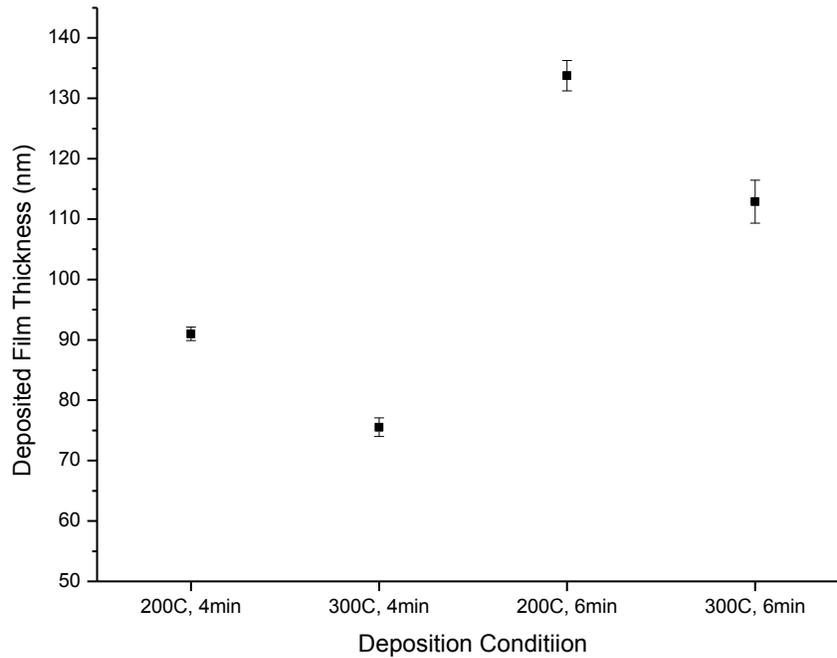


Figure 4.5: ZnO thin film thickness with different deposition conditions

Optical transparency of ZnO thin films deposited at 200 °C chamber temperature can be seen below in Figure 4.6 along with optical transparency of a bare Eagle 2000 wafer with nothing deposited on top.

In general, the transparency of the ZnO film was good for most of the visible spectrum plus the near infrared region. Same can be said for the bare Eagle 2000 wafer on which the ZnO was deposited. Rapid drop off of transparency occurred as the wavelength moved into the deep violet and ultraviolet region, with the drop off occurring with the ZnO samples before the bare wafer samples. Thus we can say that the ZnO has a lower optical bandgap than the glass used to make the Eagle 2000 wafers.

As can be expected, deposition of ZnO film lowered the transparency measured. Surprisingly, the film deposited for longer time, 6 minute, showed higher transparency over a range

of wavelengths between 400 nm to 700 nm than the 4 minute deposition sample. This can be explained by the fact that the thickness can affect transmission when the wavelength of the light and the dielectric constant of the material match up and becomes a quarter-wavelength wave guide for the light.

The effect of annealing on the ZnO film transparency was to slightly increase the transparency across the spectrum. This can be seen for the 6 minute deposition sample, where there was a 2% gain in transparency across a large range of spectrum.

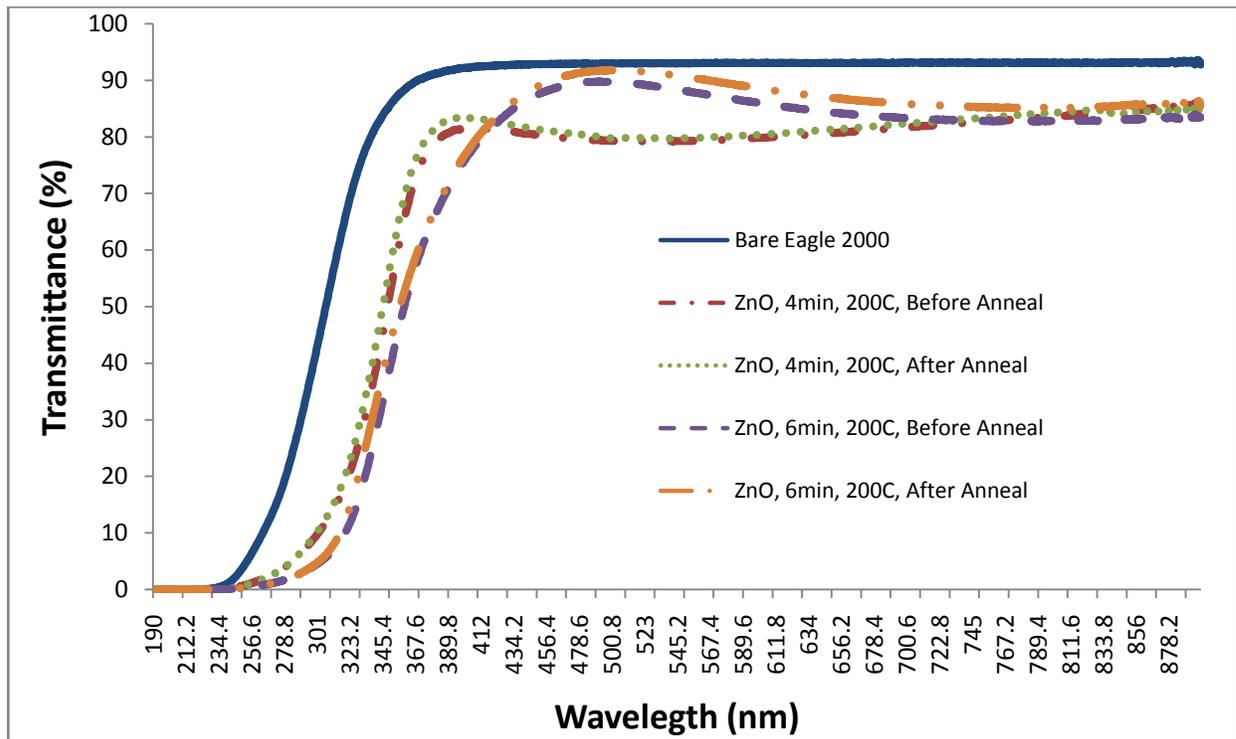


Figure 4.6: Optical transparency of ZnO thin films deposited at 200 °C and bare Eagle 2000 wafer

Figure 4.7 shows the optical transparency measured for the ZnO films deposited at 300 °C. The same observations seen for the 200 °C samples can be seen here. The 6 minute deposition had a region of higher transparency than the 4 minute region. Annealing the ZnO films led to an increase in transparency. The general transmission in the visible and near infrared wavelengths was at quite high, at roughly 80% to 85%.

Comparing between the 200 °C and 300 °C samples, the transparency difference between the two were not significant. There was a shift in the peak transparency wavelength for the 6 minute depositions between 300 °C and 200 °C, but that could be attributed to the difference in thickness of

the films. At the longer wavelengths, the transparency percentages for all the samples merged together and became pretty identical.

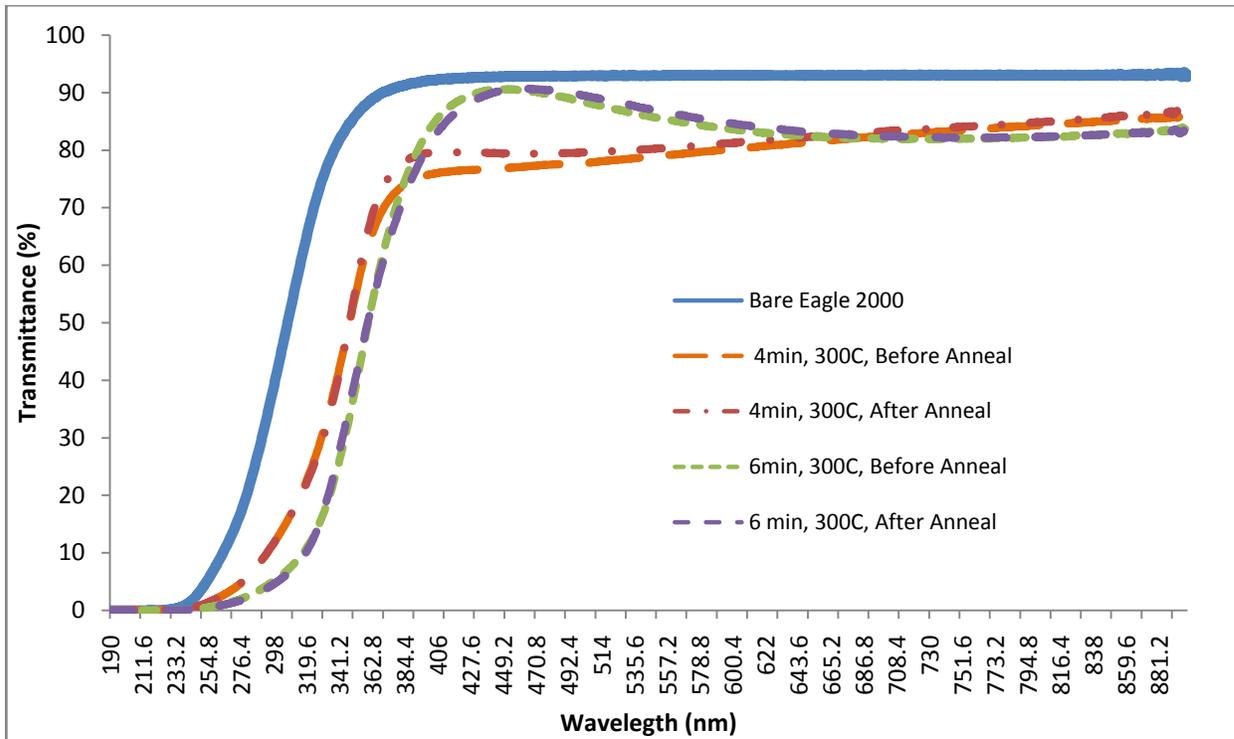


Figure 4.7: Optical Transparency of ZnO thin films deposited at 300 °C and bare Eagle 200 wafer

Additional infrared wavelength transmission measurements measured with the FT-IR machine and the result for a bare Eagle 2000 wafer plus results for the 300°C, 6 minute deposition ZnO sample are shown in Figure 4.8. The measurements have been converted from wave number to wavelength for easier comparison. Only the results for the 300 °C, 6 minute sample are shown because the results for the other samples behave identically.

In the shorter infrared wavelength results, the transmittance percentage of the ZnO film was still very high, at 80% or higher. There was a sharp drop off in transmittance percentage starting at approximate 2300 nm wavelength, both for the glass wafer and the ZnO film. At the deep infrared region of 5000 nm and beyond, the transmittance percentage dropped to 0. Further data was available all the way to wavelength of 25,000 nm but the transmittance percentages were 0 for the whole range and so the graph was truncated for clarity.

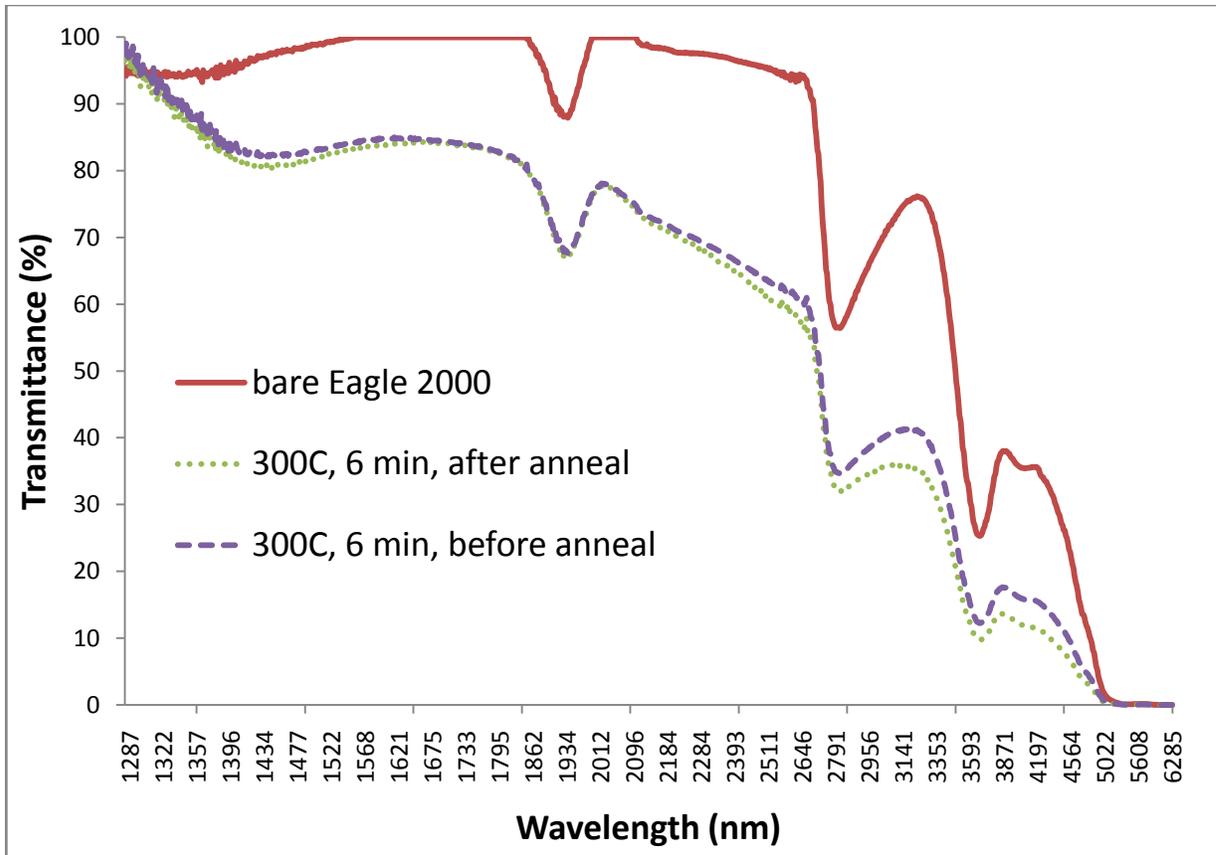


Figure 4.8: FT-IR measurement of infrared transparency for 300 °C, 6 minute ZnO thin film and bare Eagle 2000 wafer

Resistivity measured using 4-point probe methods for the different samples before and after annealing is shown in Figure 4.9. The resistivity of the films deposited at 200 °C showed lower resistivity than the films deposited at 300 °C. In accordance with this fact was that after anneal, the resistivity of all the films increased. However, the increase was much more pronounced with the 300 °C samples. There was a 2.66 times increase in resistivity for the 300 °C, 4 minute deposition sample after annealing and a 1.53 times increase for the 300 °C, 6 minute deposition sample.

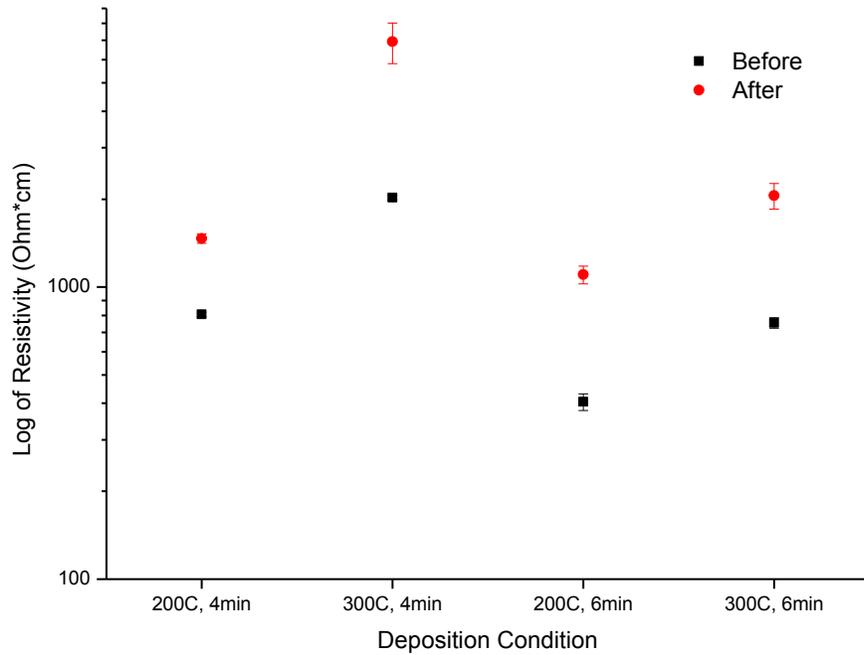


Figure 4.9: Resistivity of ZnO thin films before and after anneal

4.3.3 ZnO Thin Film Discussion

The resistivity of values measured for the ZnO films are within range of other reported values of ZnO thin films.

The increase in resistivity after anneal has also been reported by other researchers. They observed an increase in resistivity when annealed at high temperatures, with the higher increase correlated with higher annealing temperatures. The increase in optical transparency after annealing at high temperature has also been observed [38].

The change in conductivity is attributed to oxygen reaction with the ZnO film. Oxygen atoms can penetrate the film and interact with the film and decrease the amount of donors states by removing oxygen vacancies. Another possible explanation is that oxygen chemisorb on the surface of the film and create electron traps which introduces a space charge region in the surface of the film which inhibits conduction [38].

With related to deposition rate, one important issue to note is the argon pressure inside the chamber during deposition fluctuated. Following the instructions for using the R2R, for plasma ignition, the argon pressure was raised to 20 mTorr inside the chamber. After the plasma had been

ignited, the desired process pressure, namely 5 mTorr, was selected and the machine brought down the chamber pressure to 5 mTorr slowly overtime through controlling the throttle valve to the pump. However, there was no shutter inside the sputter chamber to prevent the sputtered material from reaching the substrate after the plasma has been ignited. This creates a situation at the beginning of the deposition where the actual argon pressure inside the chamber is higher than the process specification of 5 mTorr.

Furthermore, the timer to count down the deposition time started as soon as the plasma had been ignited. So for consistency in the deposition condition, the 20 mTorr was used to ignite the plasma and then 5 mTorr was selected as soon as possible such that the machine would bring down the deposition pressure as soon as possible as well. The process to reduce the deposition pressure took approximate 2 minutes and thus a significant amount of the total deposition time was spent at a higher than specified chamber pressure. This is an inherent flaw in the sputter chamber designed. The addition of a shutter would solve this problem completely, or investigation into using a lower plasma ignition pressure could alleviate this problem.

For nc-Si:H LED, the decision was to use a ZnO layer deposited at 200 °C, for 6 minutes with no post annealing because it had the lowest resistivity in the tested samples. The transmission properties of all of the films were very similar especially at the near infrared region that is of interest and so transmission properties were not considered when picking the ZnO deposition condition to use.

It was also desirable to have a thicker film from the 6 minute deposition because the thicker film would assist in lower the resistance from lateral conduction. The probes used to contact the sample devices on the probe station were quite small. Current exiting the LED at the top contact must travel vertically and laterally to reach the probe tip thus using a thicker film to help lower resistance for conduction laterally.

4.4 LED Measurement Experiments Setup

The LEDs were measured using the Keithley 4200 SCS for their IV characteristics. For light emission, several methods were used to check for light emission.

The first method was the use of a photodiode connected to a resistor while bias was applied using the Keithley and the probe station. Two different photodiodes were used which were an ORIEL 71803 photodiode assembly and a Newport 818-UV photo-detector. The photodiodes were held in

place directly above the LEDs with a mounting assembly as can be seen in Figure 4.10. The output of the photodiodes was connected to a Keithley 427 current amplifier and the output of the amplifier was connected to a 1 M Ω resistor as the load. A Fluke 179 multimeter and a Keithley 6430 sub-femto Amp remote source meter were used to measure the voltage across the resistor. The room was then set to complete darkness and the voltage was measured for before and during applied bias from the Keithley 4200 SCS. The response curves of the two photodiode used are shown in Figure 4.11 and Figure 4.12. Both detectors were responsive over the range of visible wavelengths plus some near infrared wavelength.

This setup was a simple setup, useful only to determine if there was any emission within the responsive range of the photodiodes used. The measurement could not provide any information on the wavelength of the light emitted. Thus a second method was used to determine the wavelength of the light emitted.

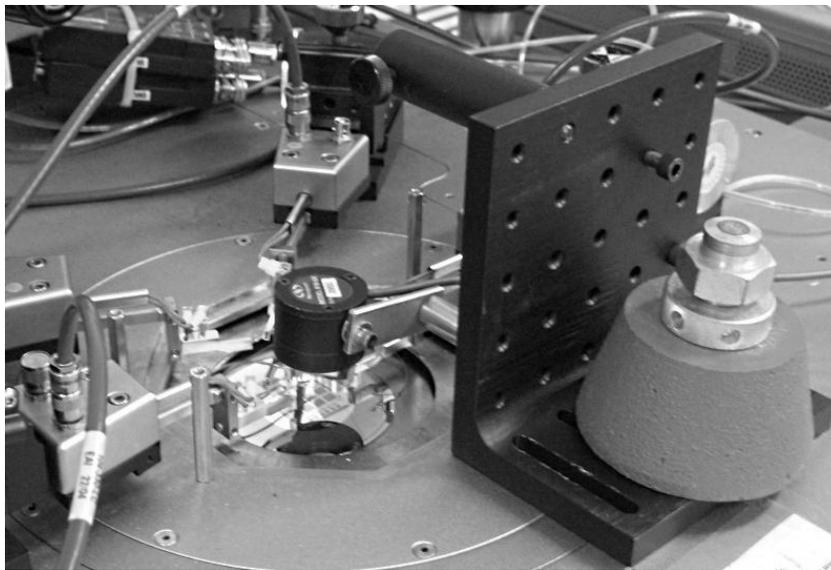


Figure 4.10: Newport 818-UV photodiode mounted above nc-Si:H LEDs on top of the probe station

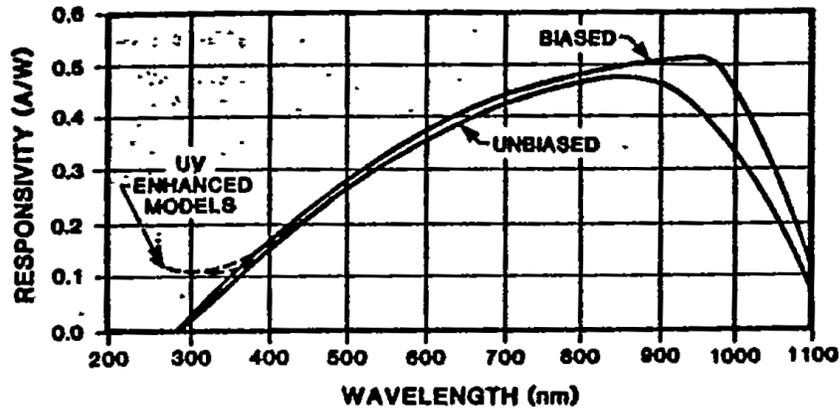


Figure 4.11: Response curve of the ORIEL photodiode assembly [39]

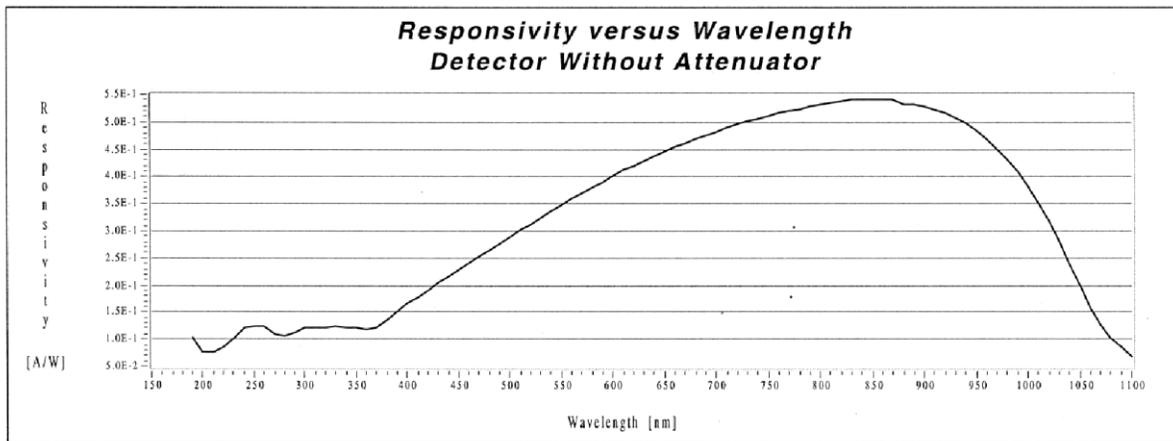


Figure 4.12: Response curve of the Newport 818-UV photodetector [40]

The second method used for emission detection from the nc-Si:H LED was to adapt the Renishaw micro-Raman 1000 spectrometer for use as light detection. The Raman machine contained a photodiode also which was cooled by a Peltier cooler and fan combination. Inside the Raman machine was an optical setup using an optical grating with controlling software which allowed for measurement of photons over different wavelengths. When the Raman machine was setup for 633 nm laser, the range of wavelengths that could be measured was from 633 nm to 1070 nm wavelength. Unfortunately, the response curve of the sensor for the Raman machine was not found.

The samples were connected using wires taped onto the contacts using vacuum tape. An external DC power supply was used to apply a bias. The Raman laser was used to focus the input to the Raman spectrometer at the top of the nc-Si:H diode. The Raman laser was then turned off while emission was measured from the sample.

4.5 LED IV Measurement Results

After characterizing the two key layers in the nc-Si:H LED structure, and selecting the appropriate deposition conditions for the two layers, several samples of the LEDs were manufactured and studied.

A comparison of the IV measurements for the LED03 and LED06 samples, measuring a diode with area of $150 * 150 \mu\text{m}^2$, is shown in Figure 4.13. The comparison shows that the thicker intrinsic film resulted in a higher rectification ratio for LED06 as compared to LED03. This was in line with previous finding from the RFID Diode. The LED03 sample showed symmetric forward and reverse bias behavior. The ON/OFF ratio for the LED03 was at maximum 1.29 at 1.8 V bias. The ON/OFF ratios for the LED06 were relatively higher, with values between 5 to 6 at bias higher than 1 V. Even though LED06 had higher ON/OFF ratio, the values were still far from the ON/OFF ratio measured for the much thicker RFID diodes.

Of note was the lower current level exhibited by both samples. With thinner films, previously we saw high current level with the RFID diodes. However, both of the samples had thinner much thinner film than the thin film RFID diode and still exhibited much lower current, more than 2 orders of magnitude lower. This could be attributed to the higher resistivity of the ZnO film used as the top contact for the LED. When compared to the aluminum top contact of the RFID diode, the resistivity of the ZnO film was 3 orders of magnitude higher.

Figure 4.14 shows the current density measured for different sized LEDs from sample LED06. Once again showing very low ON/OFF ratios and reduced current density when compared with equivalently sized diodes made for the RFID.

The current density showed a drop in current efficiency when increasing in size from $150 * 150 \mu\text{m}^2$ to $200 * 200 \mu\text{m}^2$. This can be once again attributed to the highly resistive ZnO top contact. The probe used for measured was a point probe contacting a small amount of the top contact. Because the ZnO layer was also kept thin, the lateral resistance for the current conducting from the sides of the diode to the probe tip was large. As the diode area increase, the resistance caused by the ZnO would similarly increase which countered the increase in conduction area through the diode thus causing drop in current density at higher diode area.

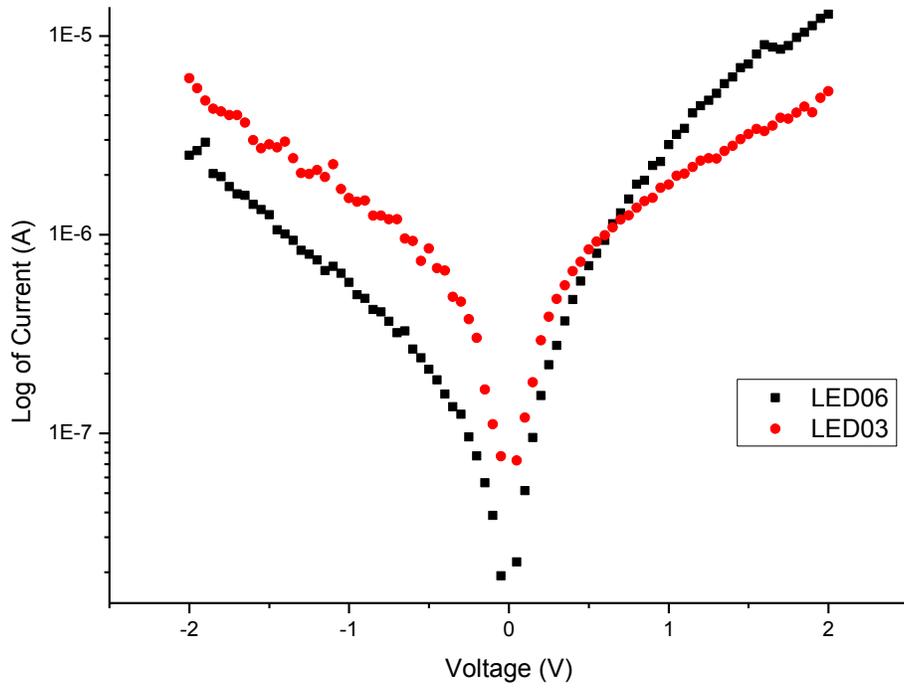


Figure 4.13: IV measurement comparison of $150 * 150 \mu\text{m}^2$ LEDs from samples LED03 and LED06

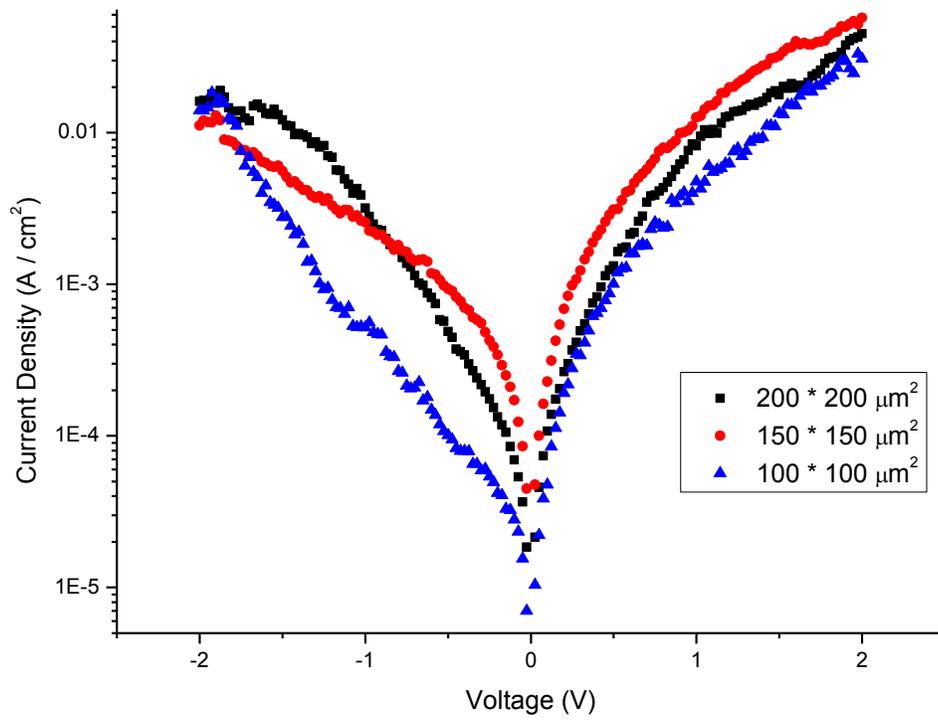


Figure 4.14: Current density measured for $200 * 200$, $150 * 150$, $100 * 100 \mu\text{m}^2$ LEDs from sample LED06

4.6 Emission Measurement Results

The emission measurement results from the two different LEDs described previously are shown below.

Table 4.3 lists the measured results from using the two different photodiodes for the two different LED samples. There were no emissions detected from both LED samples as can be seen from the results. Under dark condition, where all the lights in the room were turned on, the measured values of voltage drop across the load resistor showed no difference whether forward bias was applied across the diode or not. The fluctuation in the measured values was ± 0.002 V, so the differences in the results can be attributed to noise.

To prove the actual effectiveness of the measurement setup, the voltage values were recorded with the room ambient light turned on. Even with the photodiodes facing downwards, away from the room lights, there was dramatic increase in photocurrent and voltage drop measured.

Table 4.3: Photodiode measurement results for different samples shows no detectable emission

Sample	Photodiode	Dark (0 Bias)	Dark (2V Forward Bias)	Room Light ON
LED03	ORIEL	0.014 V	0.013 V	2.806 V
LED03	818-UV	0.006 V	0.006 V	0.296 V
LED06	ORIEL	0.015 V	0.015 V	2.811 V
LED06	818-UV	0.007 V	0.007 V	0.254 V

One issue with the photodiode was that the measurement only measures the instantaneous photons only, where the photocurrent measured was created only by the limited emitted photons. By taking measurements over long periods of time and accumulating the signal, this could increase the signal to noise ratio. To take measurement for longer periods of time was one of the reasons to measure light emission using the Raman spectroscopy machine.

Because there was no information available on the spectrum response of the detector used in the Raman machine, a simple test was devised to ensure that the detector is suitable for detecting photons from the expected emission wavelengths of the nc-Si:H LED. A commercial infrared LED was bought from an electronic supply store and was measured. The LED bought had a center peak wavelength of 940 nm, similar to the range of the theoretical nc-Si:H LED emission wavelengths.

Figure 4.15 shows the measured spectrum using the Raman machine which proved that the measurement setup worked in the near-infrared range.

The nc-Si:H LED samples were then measured using the Raman machine. The result for the LED06 sample is shown in Figure 4.16. The result shown was collected from measurements spanning 5 hours continuously. The settings for the Raman machine was 20 sec measurement time per wave number, 15 accumulations and averaging between accumulations turned on. The nc-Si:H LED was under 2V forward bias.

There were no distinguishable peaks showing emission from any one wavelength. When looking at the signal, there was an upward trend in the data at the higher wavelengths, from 950 nm to 1050 nm. However, this upward trend was not part of an emission peak. Further experiments were performed to verify that the upward trend was not evidence of photon emission. Measurements were carried out with the LED under 0 volt bias and measurements were also carried using a normal ceramic resistor in place of the nc-Si:H LED. 5 hour measurements were also carried. The results from 0 volt bias and the resistors with forward bias all showed the same upward trend. This proved that the upward trend was not due to light emission from the LED because there should be no light emission from normal resistor or at 0 V bias. The effect was probably an intrinsic measurement error of the Raman machine.

From the results of the different measurement methods used, the nc-Si:H LED did not exhibit measurable light emission in the theoretical light emission range.

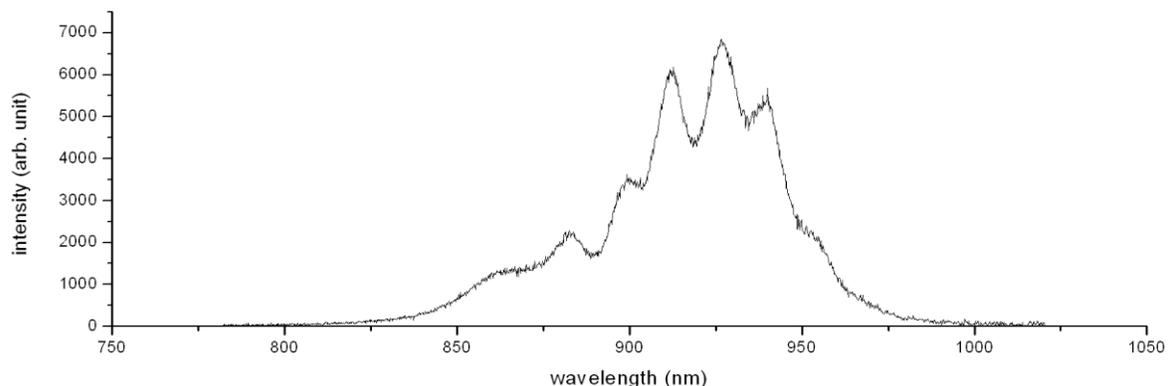


Figure 4.15: Emission spectrum of store bought infrared LED with 940 nm peak measured using Raman spectroscopy machine

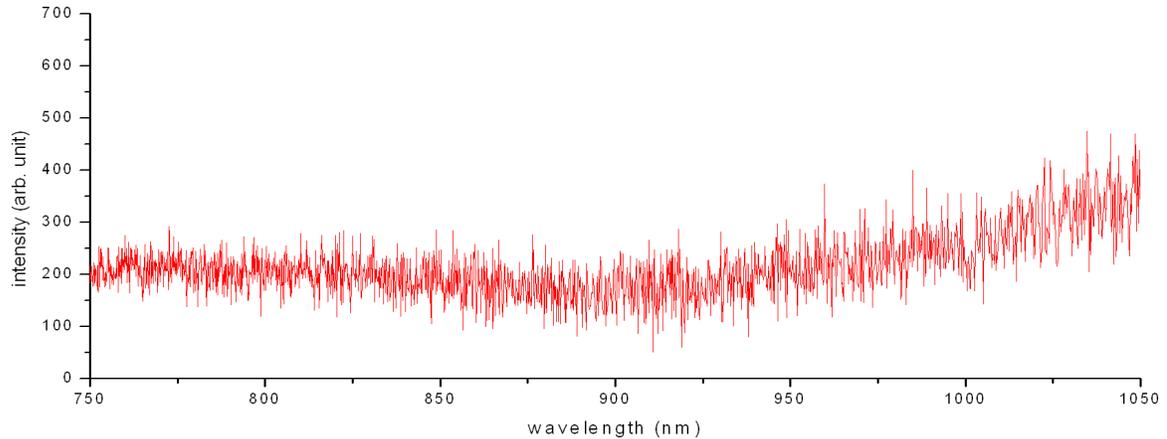


Figure 4.16: Emission spectrum of nc-Si:H LED06 measured using Raman spectroscopy machine

4.7 Discussion on Lack of Emission from nc-Si:H LED

There are several explanations as to why there was emission detectable. Possibly the amount of defects in the nc-Si:H material used were too high. Other reasons could be that the nc-Si:H film thickness used in the LED was too thin or that the barrier height provided by the amorphous silicon matrix was not suitable for quantum confinement.

It is known that there are significant amounts of traps in nc-Si:H due to the amorphous silicon matrix in which broken bonds create a lot of deep defect states [1]. These defect states could act as recombination centers. Potentially, the majority of the carrier recombination happens at the defects without generating photons instead of inside the silicon nanocrystals [36].

The thicknesses of the nc-Si:H films used in the LED were kept thin, at around 6 – 20 nm, to avoid absorption of photons generated. However, this could have led to the result of insufficient carrier trapping within the nc-Si:H layers. At less than 10 nm, the carriers could simply be traveling across the nc-Si:H layer without ever recombining depending on the diffusion length of the carriers which was also a large source of loss in a-Si:H LEDs [36]. The p+ and n+ layers were 6 nm thick, which may not provide sufficient barrier to the carriers, as there would be significant tunneling current with less than 10 nm. Simply, potentially the majority of the carriers were traveling across the nc-Si:H LED from one metal contact to another with complete extraction and no radiative recombination.

One of the important aspects in using silicon nanocrystals to generate light was the quantum confinement that occurs due to the nanometer size of the crystals. However, what had been studied previously had been nanocrystals embedded in SiO₂ or SiN₃ or silicon nanostructure surrounded by

ambient. All of the previous structure had large energy barriers surrounding the silicon nanocrystals due to the surrounding insulator. With nc-Si:H, it is known that the a-Si:H matrix provides an energy barrier on both the conduction band and valence band. However, the barrier height is not large. The barrier height has been described as 0.1 V and 0.7 V for the conduction band and valence band respectively [22]. As compared to the much larger barrier heights from insulators, the a-Si:H may not be providing large enough barrier for effective quantum confinement in order to replicate light emission from nc-Si:H.

4.8 Thin Film Intrinsic nc-Si:H Experiment

In order to further understand the intrinsic nc-Si:H which was considered key for light emission in the LED, films of intrinsic nc-Si:H were further studied. This was also in order to address some of the potential issues that led to the lack of emission from the vertical nc-Si:H LED.

The different intrinsic nc-Si:H films used for XRD and Raman crystallinity measurements had chromium metal contacts deposited using the Edwards sputtering system and the shadow masks as described previously. The film thicknesses were between 12 – 20 nm as reported previously. Detailed study of such thin films had not been carried out before within the G2N lab.

The pairs of contacts were either separated by 1 mm or 2 mm of nc-Si:H material. This addressed concern of carriers not recombining in the vertical LED. In the vertical LED, the current traveled through approximately 20 nm of nc-Si:H material thus might have not recombined within the nc-Si:H. With this horizontal configuration, the carriers must travel at least 1 mm, more than 5 order of magnitude longer. The much longer travel distance would lead to an increase in carrier recombination inside the nc-Si:H material.

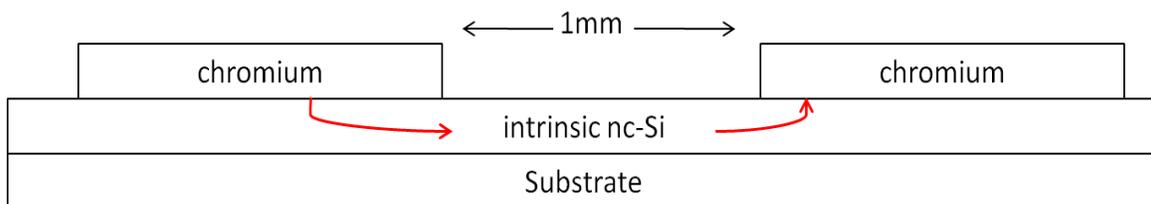


Figure 4.17: Horizontal current flow in the intrinsic thin film experiment as indicated by the arrows to travel at least 1 mm.

IV measurements were carried out across the pairs of the long Cr contacts using the Keithley 4200 SCS. The activation energy of the different intrinsic nc-Si:H films were also carried out using a heated probe station. Annealing in vacuum of the nc-Si:H samples were also tested to understand the effect of low temperature annealing has on such thin films. The annealing temperature was set at 230 °C with annealing time of 6 hours. The activation energy measurement provided the offset of the Fermi energy level from the conduction band.

To reduce the number of defects in the nc-Si:H films, two different plasma passivation methods were trialed and studied. The two passivation methods involved exposing the nc-Si:H films to pure hydrogen or oxygen plasma inside a Trion reactive ion etching (RIE) machine. The pressure inside the chamber was kept at 500 mTorr when the plasma was activated, with a 50 sccm gas flow of the respective gas. The applied DC voltage for the hydrogen plasma was kept at -4V while the oxygen plasma was kept at -20V. The hydrogen plasma DC bias was kept low to decrease the etching of the nc-Si:H from energetic hydrogen ions. The substrate temperature was kept at room temperature during the plasma treatment, no additional heating was adding. After each passivation trial, the IV characteristics and activation energies for the samples were measured.

4.9 IV Characteristics of Intrinsic nc-Si:H Thin Films

The IV characteristics of the different intrinsic nc-Si:H thin films had many interesting and unexpected results.

The first observation was that between different pairs of contacts for the same sample, the measured current varied widely with up to a 3 order of magnitude difference. Over the -20 V to 20 V sweep range, the range of current values was in the pico to nano ampere levels (10^{-9} - 10^{-12} A); however, some contacts were at 5-6 pA while other contacts were measured to have 2 nA.

The large range of measured current values indicated significant intra-wafer variation existed for all the same which could be explained by the thinness of the films. With 10-20 nm thick films, other effects such as interface defects, surface contamination and non-uniform film growth would have much more impact than with thicker films of 50-1000 nm studied previously.

Crystallinity in different locations on the 10-20 nm samples were studied to see if it could explain the variation seen in the current. Raman measurements taken between different pairs of chromium contacts showed that there were no differences in crystallinity of different region of the sample. Thus variation in crystallinity was not shown as a cause of the variation in measured current.

Another surprising finding was that the IV characteristics measured was not ohmic. The chromium to intrinsic nc-Si:H interface had been discussed before and found to be ohmic contact. However, during the voltage sweep from -20 V to 20 V, the measured current was not linear with voltage. Rather it was initially linear and then decayed into a square-root like curve. With back and forth voltage sweeps between -20 V and +20 V, it was observed that hysteresis occurred in the IV characteristics as can be seen in Figure 4.18.

Upon further investigation, the hysteresis effect was tied to the timing of the measurement. There was a temporal effect which leads to the hysteresis but varying how long the voltage was applied to the same before the measurement, different measurement results were obtained. An example of this can be seen in Figure 4.19.

In Figure 4.19, the delay factor during measurement was varied. The delay factor was a parameter of the Keithley 4200, which controlled how long the measurement voltage was applied before the measurement was taken, with a delay factor of 1 being the longest delay and 0 being no delay. As can be seen, with longer delay, the measured IV response became increasingly non-linear.

Sampling experiments were done, where a constant voltage was applied to the sample and the current flow was measured over time. It was discovered that the current measured over time drops as the voltage was continuously applied. The current level eventually settled down to a steady state value after roughly 3 seconds. It was also observed that the drop from initial current to steady state current was bigger for the larger voltages.

This curious temporal behavior would explain the non-linearity measured in simple IV measurements and the hysteresis observed. The purposed explanation for this effect was that there were substantially large amount of carriers trapped in defects in the nc-Si:H. As voltage was applied and current flow, traps began to fill up with carriers which created a space charge region. The trapped carriers repelled additional carriers from flowing into the space and impeded the current flow thus leading to decreased current measured over time. If the voltage was removed and no current flowed, the carriers would eventually escape from the trap through vibration and the effect disappears. This can be seen in Figure 4.19 where 3 measurements at 0 V bias were done after 1 measurement at every voltage. The 3 sequential 0 volt measurements showed a residual negative current that got smaller and smaller.

This pointed to a highly defective nc-Si:H film combined with a conduction region that permeated the whole film thickness. With thicker films and top contacts, the conduction traveled in the top 20 nm while trap charges could occur much deeper into the bulk of the film to lessen the impact of space charge region.

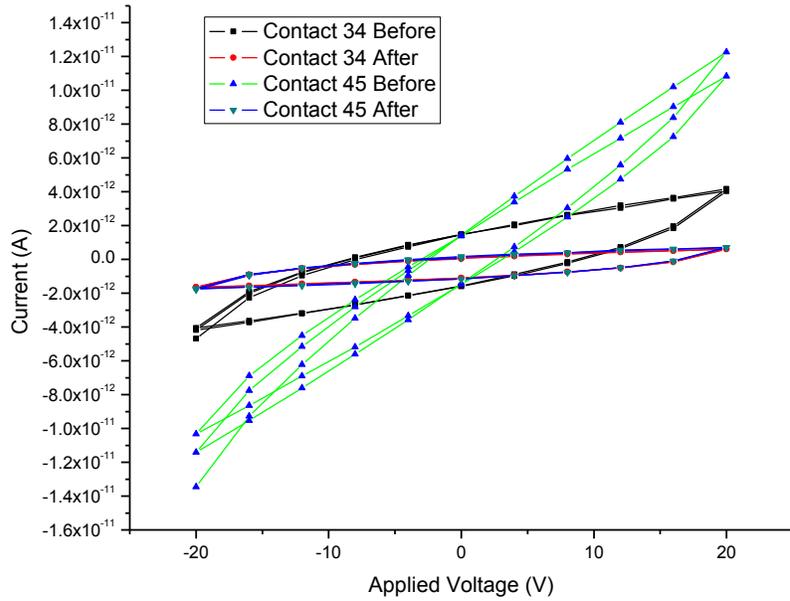


Figure 4.18: -20 V to 20 V sweeps showing hysteresis behavior in IV characteristics before and after annealing at 230 °C

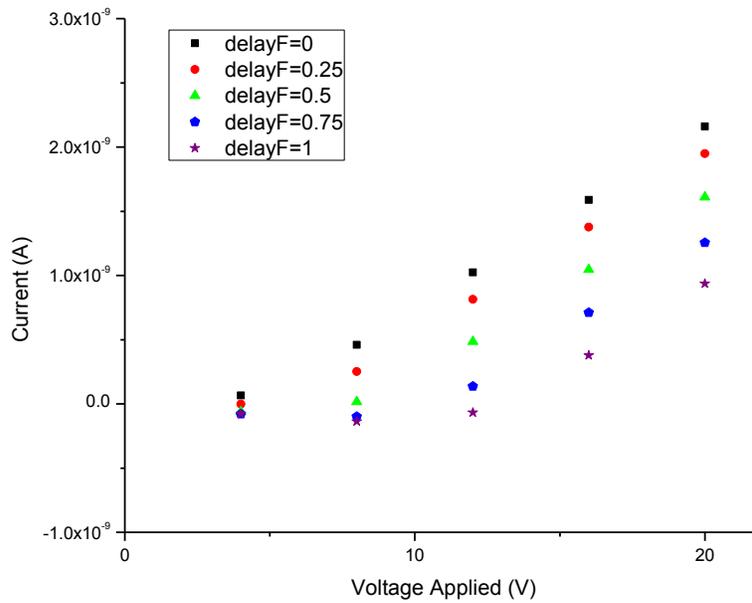


Figure 4.19: Effect of Delay Factor (DelayF) settings on measurement results with higher DelayF leading to non-linearity

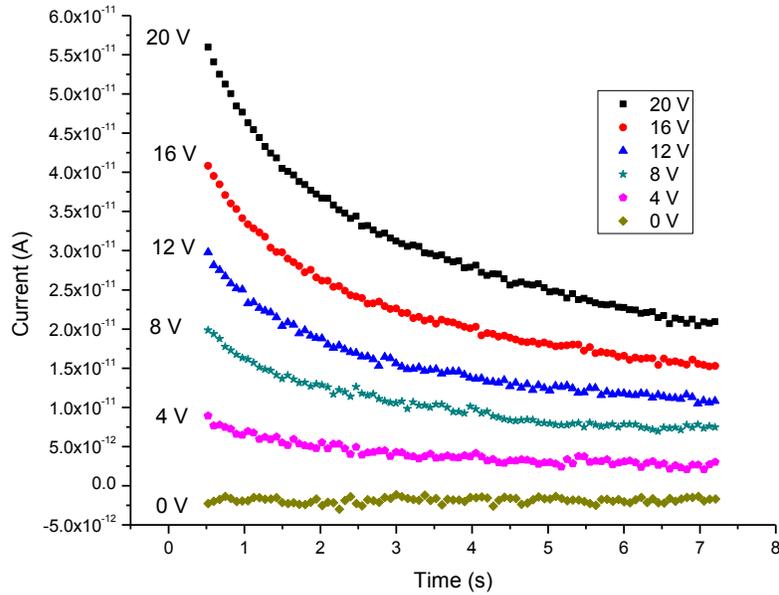


Figure 4.20: Current sampling results for 14 nm thick nc-Si:H sample with different constant voltages showing dropping current over time

4.10 Thermal Annealing Results

In hopes of removing the non-linear behavior from the IV characteristics and to decrease the resistivity in the intrinsic nc-Si:H films, thermal annealing at 230 °C for 6 hours was done on the samples in a vacuum oven. The hope was to use thermal annealing over long period of time to decrease the number of defects inside the film.

The post annealing IV characteristics displayed the opposite results. Resistivity went up as indicated by decrease current flow for all of the annealed samples. The hysteresis behavior persisted in all of the samples.

The increase in resistivity was due to hydrogen effusion from the nc-Si:H film. The temperature of 230 °C was picked because it was a lower temperature than the deposition of 260 °C and was much lower than the 300 °C often cited as the minimum temperature for hydrogen to effuse out of a-Si:H [41].

However, a-Si:H hydrogen effusion does occur at temperature lower than 300 °C, as low as 180 °C [42]. Also, it has been demonstrated that certain metal films deposited on top of a-Si:H can increase the rate of hydrogen effusion at lower temperature and Cr is one such metal [41]. With the

Cr metal contacts deposited on the nc-Si:H samples, it was likely that hydrogen effused out of the nc-Si:H film given the extended period of time for which it was annealed.

Hydrogen effusion would create additional dangling bonds in the nc-Si:H and create more deep carrier traps. Extra defects increased the resistivity by trapping more carriers during conduction [1].

Further discussion of hydrogen's role in the intrinsic nc-Si:H will be presented in the next section when looking at using hydrogen ions to passivate the nc-Si:H films which had been annealed and the passivation's effect.

4.11 Hydrogen Passivation Results

Exposure to hydrogen plasma resulted in increase of current measured for the same sample. Figure 4.21 shows sample measurement from before and after the measurement. The increase in current varied between samples and pairs of contacts measured; however, the increase in current was at least 1 order of magnitude.

At the same time, Raman measurement carried out indicated a decrease in crystallinity for all the samples. The crystallinity showed a drop of 15% to 22% across all of the samples, with the thinnest sample having a crystallinity of 38% and the thickest sample of 60%. Hydrogen ions are a known etchant for nc-Si:H and even though the DC bias was kept low to avoid excessive etching, etching still occurred. Hydrogen ions could have easily penetrated throughout the films and attacked the embedded silicon crystals and shrinking their sizes, thus resulting in the observed lower crystallinity.

Along with the observed increase in current, there was a decrease in activation energy as shown in Figure 4.22. This lowering of the E_a can be attributed to the successful passivation and reduction of deep defects in the nc-Si:H material. Interface defects trap charges which cause band bending at the interface. Oxygen trapped in the nc-Si:H is a known n-type dopant and it is known that there are significant oxygen concentration within the first 20 nm of the nc-Si:H film deposited using the PlasmaTherm system through secondary ion mass spectrometer (SIMS) analysis [14]. Because of the thin nature of the films, 10 to 20 nm meters, the interface effects can fully affect the bulk of the film. Large amount of deep defects from dangling bonds trap the Fermi energy level close to the midgap of the bandgap. As hydrogen passivation reduce the number of deep defects, the interface

trapped charge effects dominates and shift the Fermi energy level closer to the conduction band, resulting in increase in current observed. Figure 4.23 shows on a band diagram the proposed theory.

The interface defects could either be at the nc-Si:H to glass substrate interface or at the top of the nc-Si:H film as shown in Figure 4.24. At the film to glass interface, the defects could have been created at the initial moment when plasma is started. While the interface defects at the top of the film would be resultant of incomplete bonds at the top of the films and from the native oxide growth from exposure to the ambient air.

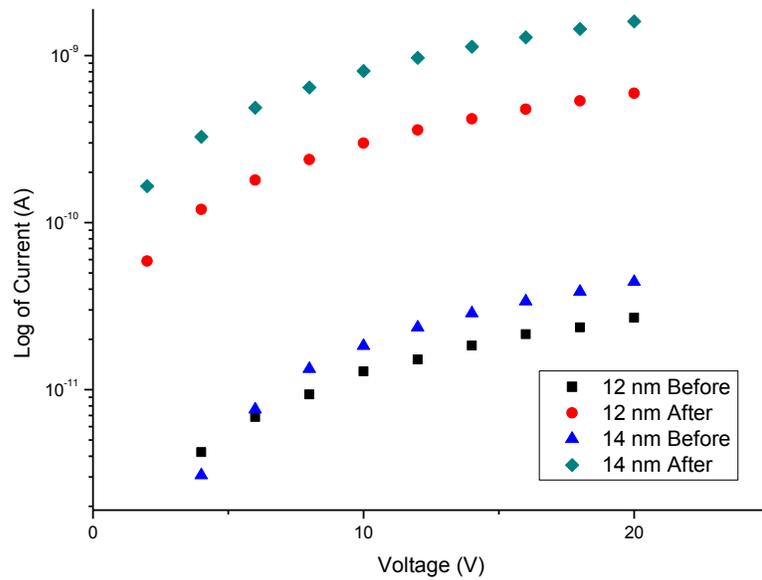


Figure 4.21: Current measured for 12 nm and 14 nm thick samples before and after hydrogen plasma, showing an increased in current after exposure to plasma

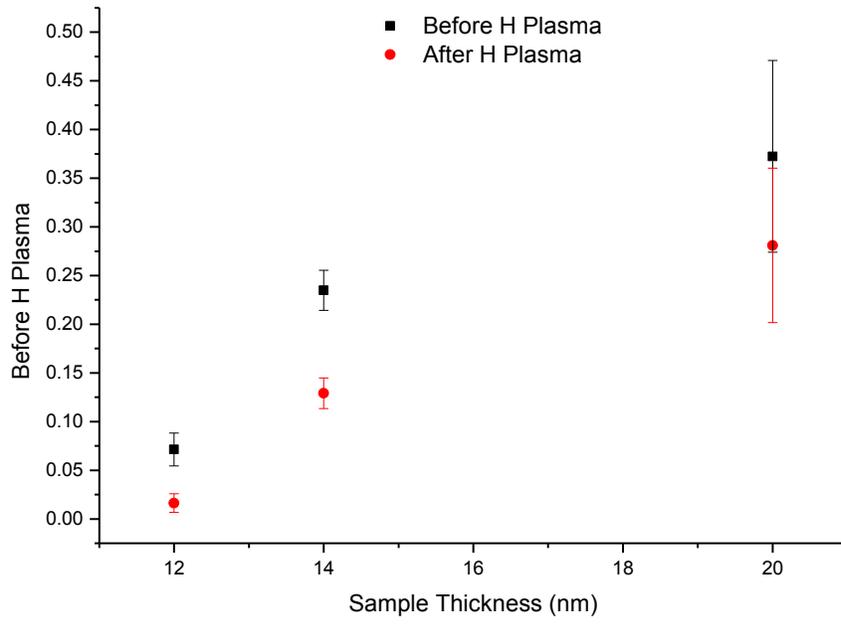


Figure 4.22: A decrease in activation energy was observed after exposure to H plasma

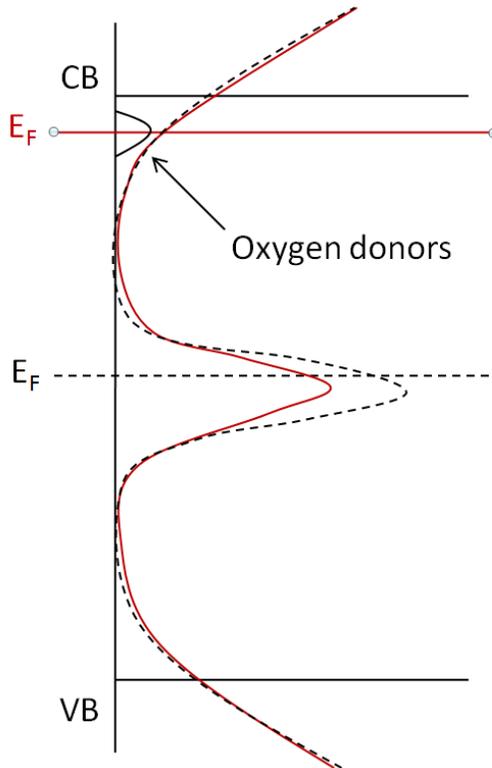


Figure 4.23: Band diagram showing the before hydrogen plasma (Dotted Line) and after hydrogen plasma (Solid Line) configuration of the Fermi Energy level with a shift due to reduction of midgap defects

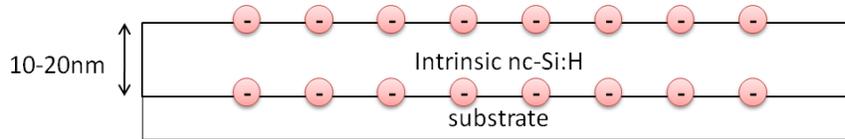


Figure 4.24: Interface defects could either be trapped at the nc-Si:H to glass interface or at the top of the nc-Si:H Film

4.12 Oxygen Passivation Results

Exciting and unexpected results were found after exposure to oxygen plasma. The idea behind using oxygen plasma for passivation was to try growing SiO_x insulator using oxygen ions and the dangling silicon bonds in the a-Si:H matrix which could lead to a reduction of defects in the nc-Si:H material. If SiO_x was grown in the material, it was expected that the conductivity and current measured through the nc-Si:H would drop after oxygen plasma treatment.

However, the opposite results were observed. After oxygen plasma exposure, the conductivity of the nc-Si:H films dramatically increased. The measured current increased by up to 6 orders of magnitude. The IV measurements are illustrated in Figure 4.25.

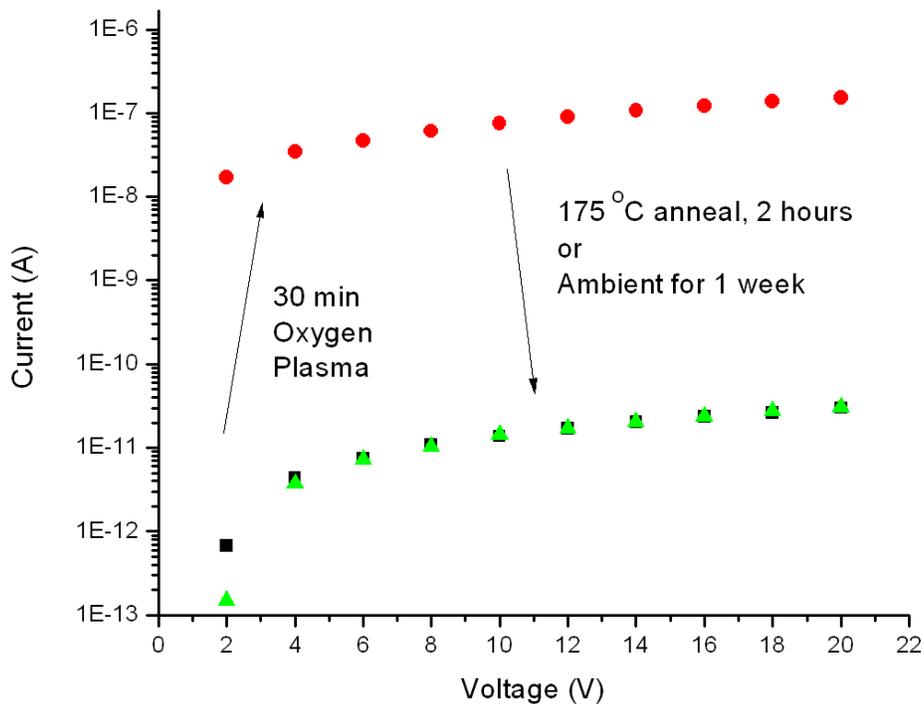


Figure 4.25: IV measurement results for nc-Si:H sample showing the effect of oxygen plasma

The length of time of the oxygen plasma treatment correlated to the amount of increase in measured current. However, the increase in conductivity was only temporary. After one week of sitting in ambient conditions or annealed for two hours at 175 °C, the effect disappeared. This effect was observed across multiple samples and was repeatable.

Activation energy measurements of the samples post oxygen plasma yielded unexpected results also. Measurement over temperature did not yield an exponential dependence between dark conductivity and temperature. Thus when curve fitting the data points was used to extract the activation energy, many of the samples had negative activation energy or large errors in the curve fitting. This was evidence that pointed to a different conduction mechanism than conduction through the nc-Si:H. Raman measurements concluded that oxygen plasma did not affect the crystallinity of the samples.

One possible explanation of this effect could be contaminates from the RIE chamber walls falling onto the substrate during the long oxygen plasma process. The contamination on the film surface could create new conduction pathways through which the higher current travels. Over time, the contamination could leave the surface.

Another possible explanation would be in a similar fashion by with oxygen ions chemisorbed on the surface instead of contamination. Oxygen atoms are known to be n-type dopants [36]. Sufficient amount of oxygen ions at the surface could change the current conduction mechanism of the thin films. The oxygen ions could be weakly attracted to the surface, such that over time, the ions leave the surface even under ambient condition. With annealing, the oxygen ions could leave at an accelerated rate explaining the decrease in time needed to return to the original low conductivity state.

This effect of oxygen plasma still needs to be further investigated. However, it can be concluded that no permanent passivation effects could be seen and thus make it not useful for use in enhancing nc-Si:H LED. However, this points towards the possible application of nc-Si:H thin film for oxygen sensor. The large magnitude of the effect seen could make for a very sensitive device.

5 Conclusions and Future Directions

In this thesis, nc-Si:H material has been applied in use two diodes for different applications and characterization and optimization of nc-Si:H films and a ZnO film had been carried out.

The deposition of n-type nc-Si:H film using a 13.56 MHz RF PECVD machine was optimized for highest dark conductivity by varying the $[\text{PH}_3]/[\text{SiH}_4]$ ratio. It was discovered that a 2% $[\text{PH}_3]/[\text{SiH}_4]$ ratio yielded a film with the highest dark conductivity, with crystallinity of 62%, growth rate of 3.68 nm/minute, activation energy of 0.02 eV and a dark conductivity of 25.3 S/cm. This n+ nc-Si:H film would then be applied in use of nc-Si:H diodes for rectification and nc-Si:H light emitting diode.

A nc-Si:H diode made for rectification on RFID tags was presented. It was discovered that a thicker nc-Si:H films used in the diode resulted in characteristics more suited for rectification. For a diode with 300 nm thick undoped nc-Si:H film and 100 nm thick n+ nc-Si:H film, the diode displayed a ON/OFF ratio of larger than 10^6 and a non-ideal constant of 1.9 with current density of larger than 1 A/cm² and reverse breakdown voltage of 15 V. By fitting the IV characteristic behavior of the diode to traditional diode models of conduction, it was concluded that the nc-Si:H diode was a p-n junction diode between the intrinsic and n+ layer. Using four 200*200 μm^2 nc-Si:H diodes in a full-wave rectifier, at the RFID communication frequency of 13.56 MHz, the rectifier was able to output up to 2.6 V with only a 2 V_{RMS} input sine wave amplitude. The nc-Si:H rectifier results, when compared to an organic-semiconductor-based rectifier, was 5 times more power efficient, requiring only 2 V_{RMS} instead of 10V_{RMS} to get the same DC output voltage.

Even though silicon is a non-direct bandgap semiconductor material, silicon light emission has been shown by using silicon nanocrystals from 1 – 10 nm in length with quantum confinement effect demonstrated. We attempted to create a nc-Si:H LED using PECVD deposited nc-Si:H film which contains many silicon nanocrystals embedded in an a-Si:H matrix. By limiting the deposition time to 6 minutes or less, thin films of nc-Si:H were deposited with thickness equal to 20 nm for 6 minute deposition and 12 nm for a 3 minute deposition. Under XRD, the thin nc-Si:H films were shown to have average crystallite sizes between 7.5 nm to 13.7 nm and the corresponding theoretical light emission from the silicon nanocrystal of the above sizes were from wavelengths 875 nm to 963 nm for 7.5 nm to 13.7 nm crystallite size respectively. Raman analysis showed the films had crystallinity from 55% to 75% with increasing crystallinity as thickness increased from 12 nm to 20 nm. A ZnO top contact was sputtered at 200 °C chamber temperature for 6 minute for use as top contact for the nc-

Si:H LED. The ZnO film had transparency at 80% for the expected theoretical emission range and a resistivity of 0.03 Ohm * cm.

The silicon LEDs displayed low ON/OFF ratios between 2 to 6 due to the low thicknesses of the films used. The LEDs also had low current density of less than 0.01 A/cm² due to resistance from the ZnO top contact. There was no light emission detected from the nc-Si:H LEDs using both photodiodes and a Raman spectroscopy machine adapted to long term measurement of over 5 hours long.

A study of the 12 to 20 nm thick intrinsic nc-Si:H films showed highly non-linear behavior. IV measurements showed hysteresis behavior with time dependence which was attributed to significant build up of trapped charges inside the material during current flow impeding other carriers from flowing. Attempt at annealing the sample at 230 °C lowered the dark conductivity of the film due to hydrogen effusion. Using a hydrogen plasma to passivate the nc-Si:H films were successful, resulting in higher conductivity and lower activation energy. Activation energy shift was due to trapped oxygen ions at the interfaces which resulted in a shift in Fermi energy level as deep midgap defects were passivated by hydrogen. Using oxygen plasma for passivation of nc-Si:H films resulted in a temporary significant boost in conductivity (more than 3 orders of magnitude) but the results only lasted one week in ambient. The effect could have been due to additional oxygen ions temporarily chemisorbing onto the surface of the film. However, light emission was still not detected after passivation steps using either hydrogen or oxygen.

Going forward, the next step of the nc-Si:H diode for RFID rectification would be to design an optimized circuit with the target frequency in mind. The test circuit for the rectifier was not optimized and did not take into account the capacitance and inductance from the metal traces and probe tips used. By properly tuning the circuit for a higher quality factor at 13.56 MHz, further improvement in the results is highly possible. Other area of research would include increasing the reverse bias break down voltage of the nc-Si:H diode. A rectifier is subjected to both positive and negative bias at high frequency, the break down voltage currently limits the amplitude of the AC signal input. Integration with complementary nc-Si:H TFTs to make a fully functional circuit powered by the rectifier would be the ultimate end goal in demonstrating a functional RFID prototype.

The nc-Si:H LED was unable to generate any light emission and will require more research work to enable detectable light emission. The combination of inefficient carrier recombination, current passing completely through the diode and lack of specialized equipment for infrared light detection

all contributed to the result. If the experiment is to be pursued further, specialized light detection equipment over the near infrared wavelength would be desirable.

The deposition of the nc-Si:H thin film should be further optimized. The only variable used in this experiment was the length of the deposition time. By changing over deposition parameters such as RF power, hydrogen dilution and substrate temperature, the silicon nanocrystal sizes could be further reduced in order to produce visible light. Other methods to control crystal size could be changing to a different PECVD machine, such as pulsed PECVD. Another possibility would be to adjust the deposition condition to grow silicon nanocrystals inside a SiO_x or SiN_x matrix instead of a-Si:H matrix by using oxygen or nitrogen donating precursor gasses. The SiO_x and SiN_x would provide a larger bandgap offset between the nanocrystal and the surrounding matrix, thus more effectively trapping the carriers inside a crystal to force radiative recombination.

Bibliography

- [1] Y. L. He, et al., "Conduction mechanism of hydrogenated nanocrystalline silicon films," *Physical Review B*, vol. 59, no. 23, pp. 352-357, Jun. 1999.
- [2] H. J. Lee, "Top-Gate Nanocrystalline Silicon Thin Film Transistors," Ph.D. dissertation, Univ. of Waterloo, Waterloo, Canada, 2008.
- [3] S. Hazra and S. Ray, "Nanocrystalline silicon as intrinsic layer in thin film solar cells," *Solid State Communications*, vol. 109, pp. 125-128, 1999.
- [4] C. Y. Y. Cheng, "Spherical Silicon Photovoltaics: Material Characterization and Novel Device Structure," Master Thesis, Univ. of Waterloo, Waterloo, 2008.
- [5] M. B. Schubert, "Low temperature silicon deposition for large area sensors and solar cells," *Thin Solid Films*, vol. 337, pp. 240-247, 1999.
- [6] A. Sazonov, "ECE639 Characteristics and Applications of Non-Crystalline Silicon," Univ. of Waterloo Course notes, 2004.
- [7] R. Want, "An Introduction to RFID Technology," *PERVASIVE computing*, pp. 25-33, Jan. 2006.
- [8] OATSystems. (2006) Dairy Farmers of America: Putting RFID into Production with OAT tag@source. White Paper.
- [9] V. Chawla and D. S. Ha, "An Overview of Passive RFID," *IEEE Applications & Practice*, pp. 11-17, Sep. 2007.
- [10] N. Huber, K. Michael, and L. McCathie, "Barriers to RFID Adoption in the Supply Chain," *RFID Eurasia, 1st Annual*, pp. 1-6, 2007.
- [11] J. V. Subramanian, et al., "All-printed RFID Tags: Materials, Devices, and Circuit Implications," *Proc. of the 19th Inter. Conf. on VLSI Design*, 2006.
- [12] R. Rotzoll, et al., "13.56 MHz Organic Transistor Based Rectifier Circuits for RFID Tags," *Mater. Res. Soc. Sympo. Proc.*, vol. 871E, no. 111.6.1, 2005.
- [13] B. S. Bae, J.-W. Choi, S.-H. Kim, J.-H. Oh, and J. Jang, "Stability of an Amorphous Silicon Oscillator," *ETRI Journal*, vol. 28, no. 1, Feb. 2006.
- [14] C.-H. Lee, A. Sazonov, and A. Nathan, "High-performance n-channel 13.56 MHz plasma-enhanced chemical vapor deposition nanocrystalline silicon thin-film transistors," *J. Vac. Sci.*

Technol., vol. A24, pp. 618-623, May 2006.

- [15] A. Johnson. (2008, Apr.) MSNBC. [Online]. <http://www.msnbc.msn.com/id/23694819/>
- [16] M. H. Oliver, et al., "Organometallic vapor phase epitaxial growth of GaN on ZrN/AlN/Si substrates," *Applied Physics Letters*, vol. 93, no. 023109, 2008.
- [17] J. Linnros, "Nanocrystals brighten transistors," *Nature Materials*, vol. 4, pp. 117-119, Feb. 2005.
- [18] C. Delerue, G. Allan, and M. Lannoo, "Theoretical aspects of the luminescence of porous silicon," *Physical Review B*, vol. 48, no. 15, pp. 24-36, Oct. 1993.
- [19] N. Lalic and J. Linnros, "Light emitting diode structure based on Si nanocrystals formed by implantation into thermal oxide," *Journal of Luminescence*, vol. 80, pp. 263-267, 1999.
- [20] L.-Y. Chen, W.-H. Chen, and F. C.-N. Hong, "Visible electroluminescence from silicon nanocrystals embedded in amorphous silicon nitride matrix," *Applied Physics Letters*, vol. 86, no. 193506, 2005.
- [21] M. R. Esmaeilli-Rad, F. Li, and A. Sazonov, "Stability of nanocrystalline silicon bottom-gate thin film transistors with silicon nitride gate dielectric," *Journal of Applied Physics*, vol. 102, no. 064512, 2007.
- [22] C.-H. Lee, A. Sazonov, and A. Nathan, "Directly deposited nanocrystalline silicon thin-film transistors with ultra high mobilities," *Applied Physics Letters*, vol. 89, no. 252101, 2006.
- [23] G. Ledoux, J. Gong, F. Huisken, O. Guillos, and C. Reynaud, "Photoluminescence of size-separated silicon nanocrystals: Photoluminescence of size-separated silicon nanocrystals:," *Applied Physics Letters*, vol. 80, no. 25, pp. 4834-4836, Jun. 2002.
- [24] D. P. Stieler, "Measurement of mobility in nanocrystalline semiconductor materials using space charge limited current," Master Thesis, Iowa State Univ., Ames, 2005.
- [25] H. J. Lee, A. Sazonov, and A. Nathan, "Evolution of Structural and Electronic Properties in Boron-Doped Nanocrystalline Silicon Thin Films," *Mater. Res. Soc. Symp. Proc.*, vol. 989, no. A21-07, 2007.
- [26] A. Alpium, V. Chu, and J. P. Conde, "Electronic and structural properties of doped amorphous and nanocrystalline silicon deposited at low substrate temperatures by radio-frequency plasma-enhanced chemical vapor deposition," *J. Vac. Sci. Technol.*, vol. A21, no. 4, Jul. 2003.
- [27] M. H. Gullanar, et al., "Effect of phosphorus doping on the structural properties in nc-Si:H thin films," *Journal of Crystal Growth*, vol. 256, pp. 254-260, 2003.

- [28] Q. Wang, et al., "High-current-density thin-film silicon diodes grown at low temperature," *Applied Physics Letters*, vol. 85, no. 11, pp. 2122-2124, Sep. 2004.
- [29] M. A. Rafiq, et al., "Charge injection and trapping in silicon nanocrystals," *Applied Physics Letters*, vol. 87, no. 182101, 2005.
- [30] I. Ay and H. Tolunay, "The influence of ohmic back contacts on the properties of a-Si:H Schottky diodes," *Solid-State Electronics*, vol. 51, pp. 381-386, 2007.
- [31] Y. Vygranenko, et al., "Segmented Amorphous Silicon n-i-p Photodiodes on Stainless-Steel Foils for Flexible Imaging Arrays," *Mater. Res. Soc. Symp. Proc.*, vol. 989, no. A12, 2007.
- [32] D. A. Neamen, *Semiconductor Physics and Devices: Basic Principles*, 3rd ed. Boston: McGraw-Hill Higher Education, 2003.
- [33] G. Gudnason and E. Bruun, *CMOS Circuit Design for RF Sensors*. Boston: Kluwer Academic Publishers, 2002.
- [34] K.-Y. Chan, J. Kirchoff, D. Knipp, and H. Stiebig, "Ambipolar microcrystalline silicon thin-film transistors," *European Materials Research Society Spring 2008 Meeting Symposium E*, 2008.
- [35] R. Rotzoll, et al., "Radio frequency rectifiers based on organic thin-film transistors," *Applied Physics Letters*, vol. 88, no. 123502, 2006.
- [36] R. A. Street, *Hydrogenated amorphous silicon*. Cambridge: Cambridge University Press, 2005.
- [37] J. Chan. (1994) Four Point Probe Manual. [Online]. http://microlab.berkeley.edu/ee143/Four-Point_Probe/
- [38] D. E. B. D. H. Zhang, "Effects of annealing ZnO films prepared by ion-beam-assisted reactive deposition," *Thin Solid Films*, no. 238, pp. 95-100, 1994.
- [39] ORIEL Corp. (2003) ORIEL Silicon Photodiodes Datasheet.
- [40] Newport Corporation. (2004) Detector Calibration Report.
- [41] H. Ohmi, K. Yasutake, Y. Hamaoka, and H. Kakiuchi, "Metal induced hydrogen effusion from amorphous silicon," *Applied Physics Letters*, vol. 91, no. 241901, 2007.
- [42] W. Beyer, "Diffusion and evolution of hydrogen in hydrogenated amorphous and microcrystalline silicon," *Solar Energy Materials & Solar Cells*, vol. 78, pp. 235-267, 2003.

Appendix A

The following are pictures of the masks used to fabrication the nc-Si:H diodes and the rectifiers.

