Active Pixel Sensor Architectures for High Resolution Large Area Digital Imaging

by:

Farhad Taghibakhsh

A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Doctor of Philosophy
in
Electrical and Computer Engineering

Waterloo. Ontario, Canada, 2008

© Farhad Taghibakhsh 2008

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

This work extends the technology of amorphous silicon (a-Si) thin film transistors (TFTs) from traditional switching applications to on-pixel signal amplification for large area digital imaging and in particular, is aimed towards enabling emerging low noise, high resolution and high frame rate medical diagnostic imaging modalities such as digital tomosynthesis. A two transistor (2T) pixel amplifier circuit based on a novel charge-gate thin film transistor (TFT) device architecture is introduced to shrink the TFT based pixel readout circuit size and complexity and thus, improve the imaging array resolution and reliability of the TFT fabrication process. The high resolution pixel amplifier results in improved electrical performance such as on-pixel amplification gain, input referred noise and faster readouts.

In this research, a charge-gated TFT that operates as both a switched amplifier and driver is used to replace two transistors (the addressing switch and the amplifier transistor) of previously reported three transistor (3T) APS pixel circuits.. In addition to enabling smaller pixels, the proposed 2T pixel amplifier results in better signal-to-noise (SNR) by removing the large flicker noise source associated with the switched TFT and increased pixel transconductance gain since the large ON-state resistance of the switched TFT is removed from the source of the amplifier TFT. Alternate configurations of 2T APS architectures based on source or drain switched TFTs are also investigated, compared, and contrasted to the gate switched architecture using charge-gated TFT.

A new driving scheme based on multiple row resetting is introduced which combined with the on-pixel gain of the APS, offers considerable improvements in imaging frame rates beyond those feasible for PPS based pixels.

The novel developed 2T APS architectures is implemented in single pixel test structures and in 8×8 pixel test arrays with a pixel pitch of 100 μm. The devices were fabricated using an in-house developed top-gate TFT fabrication process. Measured characteristics of the test devices confirm the performance expectations of the 2T architecture design. Based on parameters extracted from fabricated TFTs, the input referred noise is calculated, and the

instability in pixel transconductance gain over prolonged operation tine is projected for different imaging frame rates.

2T APS test arrays were packaged and integrated with an amorphous selenium (a-Se) direct x-ray detector, and the x-ray response of the a-Se detector integrated with the novel readout circuit was evaluated. The special features of the APS such as non-destructive readout and voltage programmable on-pixel gain control are verified.

The research presented in this thesis extends amorphous silicon pixel amplifier technology into the area of high density pixel arrays such as large area medical X-ray imagers for digital mammography tomosynthesis. It underscores novel device and circuit design as an effective method of overcoming the inherent shortcomings of the a-Si material . Although the developed device and circuit ideas were implemented and tested using a-Si TFTs, the scope of the device and circuit designs is not limited to amorphous silicon technology and has the potential to be applied to more mainstream technologies, for example, in CMOS active pixel sensor (APS) based digital cameras.

Organization of the Thesis (6 Chapters)

Chapter 1 presents the general and introductory information on large area digital imaging and x-ray medical diagnostics imaging, followed by ***Chapter 2*** as a short briefing on existing pixel architectures for large area imaging which serves as the intro for ***Chapter 3*** as the core of the thesis on introducing novel pixel architectures for high resolution digital imaging. ***Chapter 4*** explains details of the fabrication process developed for implementing the novel architectures using amorphous silicon technology, followed by ***Chapter 5*** that completes the fabrication process by explaining the integration of the test imager arrays with x-ray amorphous selenium detector and presents results of x-ray response of the developed two-transistor amplified pixel architectures. Finally, the research work is summarized in ***Chapter 6*** with conclusion and contributions of the author to the field of large area digital imaging. Bibliographies are at the end of each chapter.

Acknowledgments

I am honored to express my deep appreciations to Professor Karim S. Karim for his technical instructions on my projects, his insightful supervision on my research work, and for his extraordinary support of my graduate program; I considerably learned a lot by working for, and with him. Also, I acknowledge my family for their everlasting love, plentiful encouragement and their unconditional support throughout my life, especially for the period of time I was perusing my study programs.

There are a number of individuals whose contributions to this work in terms of helps, insights, discussions and cooperation are gratefully recognized and truly appreciated: Mr. Bill Woods who went too far in letting me use the SFU fabrication facilities 24 – 7, Dr. Xinyu Wang for his assistance in use of CVD cluster tool, Dr. Eva, Professor Karen Kavanagh, and of course, my valued colleague, Michael Adachi for his collaboration in HW-CVD.

I specially thank Professor Safa Kasap and Dr. George Belev from University of Saskatchewan for their collaboration on a-Se photoconductor integration, Professor John Rowlands from University of Toronto for his remarks and guidance regarding the science of medical imaging.

I'd like to thank ALL my friends at the school of Engineering Science, SFU, without whom, the university life would had been half spirited (including): Shirin and Raj Pabla who mentored me when I was applying to SFU; my colleagues at STAR group and other SFU friends: Golnaz, Tony, Hadi, Ida, Amir, Michael, Lidya, Lila, Kourosh, and Esmaiel; specially Ida, for our collaborative work on photoconductors. I also thank Linda for our inspiring collaboration on remote heart beat monitoring system. Not forgetting Reza, of course, remembering our short breaks at the Organic Garden café during our long lab work hours, and for the discussion, every time, on who takes the last piece of the Cardamom cake.

My other friends and mentors to be appreciated are: Sam, Allen, Fay, Sharif, Hossein, Simin, Shahram and Sohrab: one can never forget the joy of numerous and lecture-full hiking, skiing and camping trips, and so many other outdoor activities we all did together in the beautiful province of British Columbia, and of course, the great lessons of life I learned from them.

To my family,

whose love and supports are the treasure of my life,

and,

to my teachers,

who nourished me with their knowledge, and
patiently guided me along this path.

Table of Contents

Abstract iii

Acknowledgments v

1. Introduction to Digital X-Ray Imaging for Medical Diagnostics 1

1.1 Introduction 2

1.1.1 Solid state electronic imagers 2

1.2 Large area imaging 3

1.3 Flat panel imagers 4

1.3.1 Silicon thin film technology 5

1.3.2 Amorphous silicon technology 6

1.3.3 Polycrystalline silicon technology 7

1.4 X-ray digital imaging and its applications in medical diagnostics 8

1.4.1 Interaction of x-rays with matter 8

1.4.2 Direct and indirect x-ray detectors 11

1.5 X-ray imaging for mammography 15

1.5.1 Introduction to breast cancer 15

1.5.2 Mammography 15

1.5.3 Tomosynthesis 17

2. Existing Pixel Architectures for Large Area Digital Imaging 22

2.1 Passive Pixel Sensor Architecture 23

2.1.1 Introduction 23

2.1.2 PPS operation 24

2.1.3 Characteristic function of PPS architecture 25

2.1.4 PPS architecture with voltage amplifier 27

2.1.5 Numeric values and practical considerations for PPS architecture 28

2.2 Active Pixel Sensor Architectures ... 28
2.2.1 Introduction ... 28
2.2.2 APS operation and classification ... 29
2.2.3 Voltage mediated APS ... 29
2.2.4 Current mediated APS ... 32
2.3 Hybrid pixel designs ... 35

3. High Resolution Pixel Architectures ... 39
3.1 Charge-Gated Thin Film Transistor ... 40
3.1.1 Introduction ... 40
3.1.2 Charge-gated TFT ... 40
3.1.3 Experimental results and discussion ... 45
3.2 Novel Two-Transistor Pixel Architectures ... 47
3.2.1 Introduction ... 47
3.2.2 Two-Transistor APS Architectures ... 48
3.2.2.1 Pixel architecture using a gate-switched amplifier ... 48
3.2.2.2 2T-APS using a source-switching ... 53
3.2.2.3 2T-APS using a drain switching ... 54
3.2.2.4 Hybrid architectures versus high speed imaging ... 56
3.2.3 Pixel Transconductance Gain ... 57
3.2.4 Noise Performance of 2T-APS ... 60
3.2.5 Metastability ... 65
3.2.6 Transient Response ... 69
3.3 Summary ... 75

4. Fabrication of Test Arrays ... 81
4.1 Thin Film Circuit Fabrication Process ... 82
4.1.1 Thin Film Deposition ... 82
4.1.2 Thin Film Transistor Structure ... 83
4.1.3 Mask Design ... 85
4.1.4 Fabrication Process ... 93
4.2 Characteristics of Fabricated Thin Film Transistors and Arrays ... 96

4.2.1 Thin Film Transistor Characterization ... 96
4.2.2 Two-Transistor APS Array ... 99

5. X-ray Response of the Two-Transistor APS ... 103
5.1 Amorphous selenium x-ray photoconductor coating ... 104
5.2 High Voltage DC Source ... 105
5.3 Dark current measurement ... 106
5.4 X-Ray Measurement ... 108
5.4.1 X-ray cabinet and measurement setup ... 108
5.4.2 X-ray spectrum ... 110
5.4.3 Detective Quantum Efficiency ... 111
5.4.4 X-ray response ... 112
5.4.5 X-ray Sensitivity ... 116
5.5 Summary ... 117

6. Conclusion and Contributions ... 119

Appendix A
List of Scholarly Contributions ... 121

Appendix B
Selected Papers ... 123

1

Introduction to Digital X-Ray Imaging for Medical Diagnostics

This chapter briefly reviews the history of digital imaging, and introduces principals of x-ray imaging and its applications in medical diagnostics. Because the main focus of this research is to provide an x-ray detector solution for the emerging medical diagnostic modality of mammography tomosynthesis, which requires a high resolution low noise and high speed x-ray imager, this chapter is to provide essential introductory information that helps understanding the importance of the information brought up in the rest of the thesis.

1.1 Introduction

1.1.1 Solid state electronic imagers

The invention of transistor in 1947 phenomenally accelerated advances in solid state electronics leading to replacement of amplifying and switching vacuum tubes by their more reliable and less expensive solid state counterparts. The electronic imaging tube, known as vidicon, was not exempted and was later replaced by emerging solid state electronic imaging devices, CCDs. Willard Boyle and George E. Smith invented Charge Coupled Devices (CCDs) for memory applications at AT&T Bell Labs when developing semiconductor bubble memory devices in 1969. Although CCD was basically an electric charge shift register, it was immediately understood that the device can receive photo generated charge in the semiconductor substrate to capture images. In 1971 Bell researchers were able to demonstrate simple linear imagers, and therefore CCD for electronic imaging was born. Two dimensional arrays of CCDs have been shown to be of the highest quality imagers, and yet, the most expensive ones. The biggest disadvantage of CCDs is that their fabrication is not compatible with CMOS technology, with which the CCD drivers, image capturing and processing circuits are fabricated. It was apparent that an image detector technology developed using CMOS will dominate the market thanks to more available and less expensive fabrication lines, and less complicated assembly because the imager and driving/processing circuits are fabricated on the same substrate; a system on a chip.

The idea of Active Pixel Sensor (APS) arrays was developed separately by Nobel [1] and Chamberlain [2] in late 60s, when they were able to demonstrate image capturing using sensor arrays and active MOS readout amplifiers per pixel. In 1992 it was predicted that APS will commercially appear as the successor of CCDs [3] and between 1993 and 1995 Jet Propulsion Laboratory (JPL) developed a number of prototype CMOS imagers and demonstrated the key features of the technology. APS provides faster imaging with less image lag and considerably lower power consumption compared to CCDs, although it suffers from high fixed pattern noise. In 1995 Photobit corporation span off the JPL and

successfully commercialized APS technology for different applications such as web cams, digital cameras, digital radiography and many more.

1.2 Large area imaging

Optical imaging, no matter digital or analog, is usually tied up with optical lenses to project a reflectance image of large objects on to small capturing devices such as CCDs or emulsion films. The imaging principals and techniques fundamentally change when it comes to high penetrating x-rays, which are absolutely difficult, if not impossible, to focus them on a small image recording device. In case of x-rays therefore, a straight line configuration of source-object-imager is formed to cast a shadow of the object, or a transmission image, on to the imager which is as large as the object itself (Fig. 1.1).

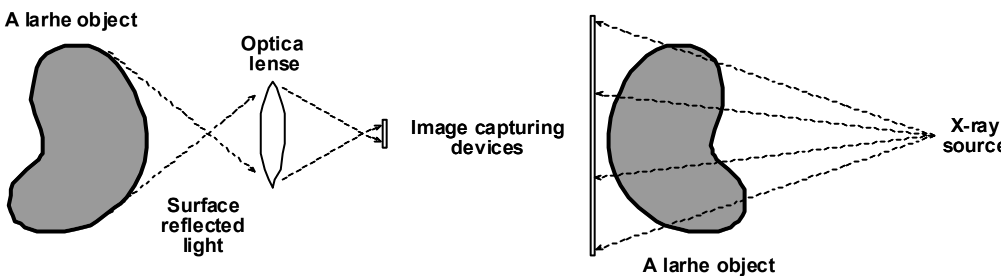


Figure 1.1. In optical imaging (left) using lens and a small image capturing device, versus x-ray imaging (right) using a large area imager.

As in office scanners or x-ray security baggage checking systems, scanning large objects using a linear imager is a low cost solution at the expense of lower imaging speed and/or more complex mechanical systems for large area imaging. However, such methods are not used for medical x-ray imaging, except for computed tomography, because of the potentially high dose the patient can receive as the result of excessive exposure to radiation.

Thanks to the modular nature of CMOS imagers it is possible to tile a number of imaging modules together to assemble a large area imager [4]. However, the high price of large area processed silicon and challenges of tiling and assembling has proved the mosaic large area imagers technology to be expensive.

1.3 Flat panel imagers

Large area electronics was developed mainly in attempt to replace bulky CRTs with flat panel displays, which require a matrix of switching elements deposited on glass or plastic; an active matrix. Such switching devices, known as Thin Film Transistors, TFTs, are connected to passive display elements such as liquid crystal cells [5], or active devices such as Light Emitting Diodes LEDs [6]. Once the active matrix is developed, a large area flat panel imager is obtained if the active matrix is connected to light sensing elements such as *pin* diodes (Fig. 1.2). To have x-ray imaging capability, the imager is coated with a phosphor or scintillator materials such as gadolinium oxisulfide or cesium iodide that convert energetic x-rays photons to optical photons. As a result, a large area x-ray imager suitable for applications such as radiology or non destructive inspections is developed.

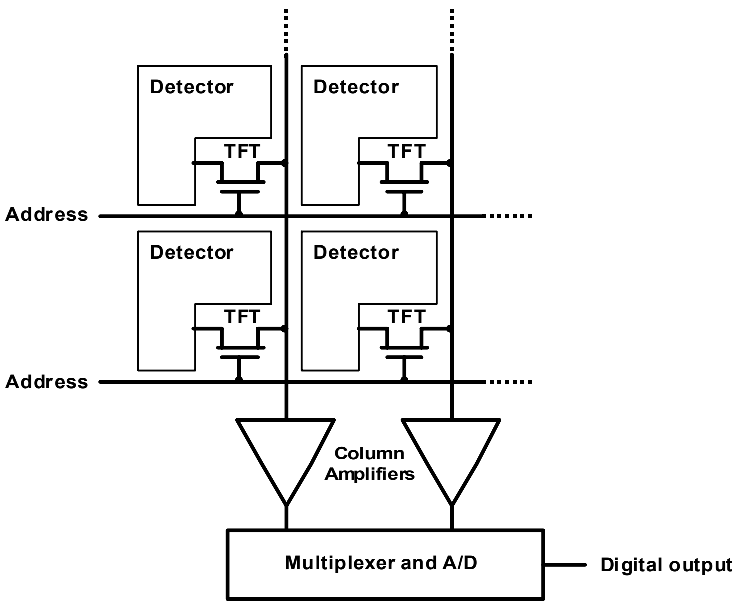


Figure 1.2 .Schematic diagram of a flat panel imager based on PPS architecture

X-ray imaging method explained above is called indirect method, because the x-ray photon is first converted to visible photons, and then these visible photons are converted to electric signal by the photo-sensing element such as the *pin* diode. Diffusion of light in the phosphor or scintillator layer renders blurred images, especially if thicker layers are needed to stop high energy x-rays. Direct detection scheme has been proposed and developed to solve this problem by using a photocoducting material such as amorphous selenium (a-Se) that generates electric charge upon absorbing x-rays. The generated charge is directed toward collecting electrode under very high biasing electric field which prevent diffusion of charge and blurring. Both direct and indirect flat panel x-ray imagers fabricated using hydrogenated amorphous silicon (a-Si:H) active matrix on glass substrates are commercially available today. They are based on passive pixel sensor (PPS) architecture (Fig. 1.2) a predecessor of the APS. Although x-ray imaging using APS has been extensively researched [7-11], commercial products have not yet been reported.

1.3.1 Silicon thin film technology

It is well accepted that thin film field effect devices were first introduced solid state transistors [12], and first tried. Although the problem of high interface states redirected thin film device research to the invention of point contact transistor, however the work on TFTs continued using compound semiconductors such as cadmium sulfide and cadmium selenide, under the motivation from display industry, and resulted in development of many Active Matrix LCD (AMLCD) prototypes [13]. Although CdSe based TFTs show very high electron mobility, the display industry and device physicists preferred amorphous silicon TFTs (mobility ≤ 1 $cm^2/V.s$) upon introduction [14] basically because of its amorphous and amphoteric nature, compared to polycrystalline and reactive nature of CdSe to environmental conditions. Silicon thin film technology is now the work horse of the today's $80B flat panel display market, which is projected to be a $100B business by 2009.

1.3.2 Amorphous silicon technology

Amorphous silicon (a-Si) is an allotropic form of silicon known to have a random network of atoms with only short range order (Fig. 1.3). In a-Si, not all atoms in a-Si have four-fold coordination, which results in dangling bonds for some atoms. Presence of dangling bonds introduces trap level energies between the valance and the conduction band of a-Si; diminishing a clear cut between the two to have a bandgap. Passivation of dangling bonds using hydrogen, considerably reduces density of states, resulting in a bandgap-like structure that makes it possible to dope the material using phosphor and boron to produce n-type and p-type s-Si:H for device applications; the deep level, and band tail states are the main characteristics of the electronic structure of a-Si:H with an optical bandgap of ~1.8 eV.

Plasma Enhanced Chemical Vapor Deposition (PECVD) is the most common method for depositing a-Si:H thin films using Silane (SiH_4) and hydrogen as precursor gases. The structural and electronic quality of the deposited film is controlled by a number of PECVD chamber parameters such as chamber pressure, gases flow rate, plasma power and frequency, the distance between plasma electrode and substrate temperature [15].

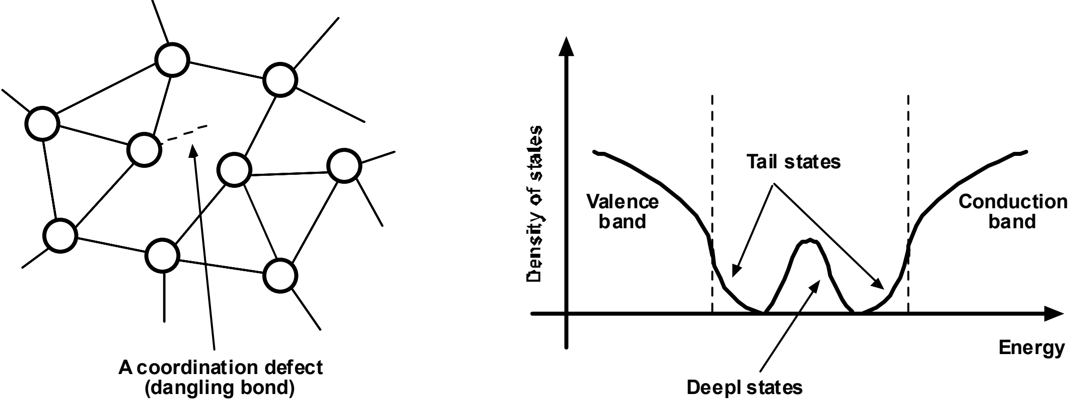


Figure 1.3. Diagram of amorphous silicon network (left), and resulting band energy (right)

Hydrogenated amorphous silicon is a metastable form of polycrystalline silicon. Re arrangement of bonding configuration Si-Si weak bonds and Si-Hi bonds are accelerated under external excitement. The bonding energy of hydrogen to silicon dangling bonds is low, especially in Si-H_2 form. Such weak bonds easily break under moderate applied electric field, or absorption of light which causes defect creation, leading to the known metastability problem in a-Si:H devices. For passivation of dangling bonds, only hydrogen atoms incorporated in form of Si-H bonds (and not Si-H_2) are considered suitable for device quality films [16].

Table 1.1. Properties of device quality a-Si:H [17]

Material constant	**Typical value**
Dark conductivity	10^{-11} S/cm
Conductivity activation energy	0.82 eV
Photoconductivity (100 mW/cm^2)	10^{-4} S/cm
Optical bandgap	1.7-1.8 eV
Electron mobility	0.5–1.0 cm^2/V.s
Hole mobility	~10^{-3} cm^2/V.s
Refractive index	4.3
Hydrogen content	18 at.%
Densiy	2.2 g/cm^3
Valence-band tail slope	42–50 meV
Conduction-band tail slope	25 meV

1.3.3 Polycrystalline silicon technology

While amorphous silicon TFTs offer a low cost solution for large area electronics such as display applications, a-Si:H technology seriously suffer from two major drawbacks: 1) very low electron mobility of about 1 cm^2/V.s that limit a-Si:H TFTs applications to low speed electronics, and 2) much lower hole mobility that makes it very challenging

development of a-Si:H complementary devices like CMOS circuits for low power low cost processing applications. Polycrystalline silicon (p-Si) technology was developed to overcome such shortcomings of amorphous silicon technology [18]. The technology provides an electron mobility as high as a couple of hundreds $cm^2/V.s$, and complementary NMOS and PMOS devices which enables manufacturers to integrate driving circuits of an active matrix on the same substrate to considerably reduce the product assembly cost and complication [19]. However, fabrication of polycrystalline silicon devices requires higher thermal budget and expensive facilities such as lasers or ion implantation for lengthy processes like re-crystallization or doping, which adds up to the manufacturing cost, and lowers the throughput [18].

Non-uniform characteristic of micron-sized devices heavily challenges process scientists and engineers when dimensions of the polycrystalline silicon device become comparable to the grain size. Such non-uniformities root back in uncertainties in the grain size, and the number of grain boundaries that may appear within the channel of a p-Si TFT [14]. While polysilicon TFTs are considered to be the next generation of devices for thin film electronics, intermediate phases of silicon like nanocrystalline silicon (nc-Si) also show promising future [20].

1.4 X-ray digital imaging and its applications in medical diagnostics

1.4.1 Interaction of x-rays with matter

Electromagnetic waves of wavelength around 10 nm or shorter are called X-rays. They are subdivided into soft and hard x-rays, where the latter overlaps a range of long-wavelength gamma rays (Fig. 1.4). While there is no difference in their wavelengths or radiation properties, the distinction between the two types, i.e., hard x and gamma rays, comes from the source of radiation. In case of x-rays, deceleration of electrons, or

transition of electrons in atomic orbital is responsible for radiation, however, inter nuclei energy state transitions generate gamma rays.

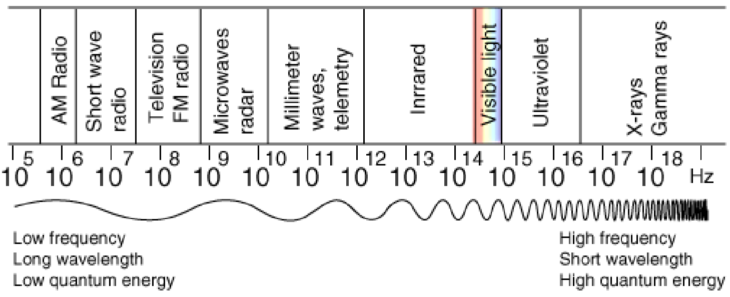


Figure 1.4. Span of electromagnetic wave, and associated labels

The basic generation of x-rays is by accelerating electrons in order to collide with a heavy metal target (copper, molybdenum or tungsten usually). Here the electrons suddenly decelerate upon colliding with the metal target and continuous spectrum of x-ray energies are emitted which is called bremsstrahlung. If enough energy is contained within the electron it is able to knock out an electron from the inner shell of the metal atom and as a result electrons from higher energy levels then fill up the vacancy and characteristics x-ray photons are emitted which their energy is depended to the metal target. Nowadays, for many applications, x-ray production is achieved by synchrotrons. However because of high complexity and cost synchrotron x-ray imaging has limited applications.

X-rays are high penetrating radiation, e.g., 37% of a 60 keV radiation will pass through 3 centimeter of a material like bone. The intensity of the radiation at any given depth of the absorbing material is given by equitation 1.1.1 which shows the absorption exponentially increases as the radiation penetrates through the material with an absorption coefficient which is energy and material depended (Fig. 1.5).

$$I(x) = I_0 \exp\left[\left(-\frac{\mu}{\rho}\right)\rho\, x\right] \tag{1.1}$$

Depending on the incident photon energy and the material, X-rays interact with mater in three different mechanisms; photoelectric, Compton and pair generation (Fig. 1.5). In the first method, the X-ray gives its energy to an orbital electron and kicks it out. Where in the second, virtually same thing happens but not all the incoming photon energy is consumed; therefore the X-ray loses part of its energy and changes its wavelength. In pair generation, the X-ray energy is higher than two times the rest mass of electron, so, its quantum energy is converted to an electron-positron pair.

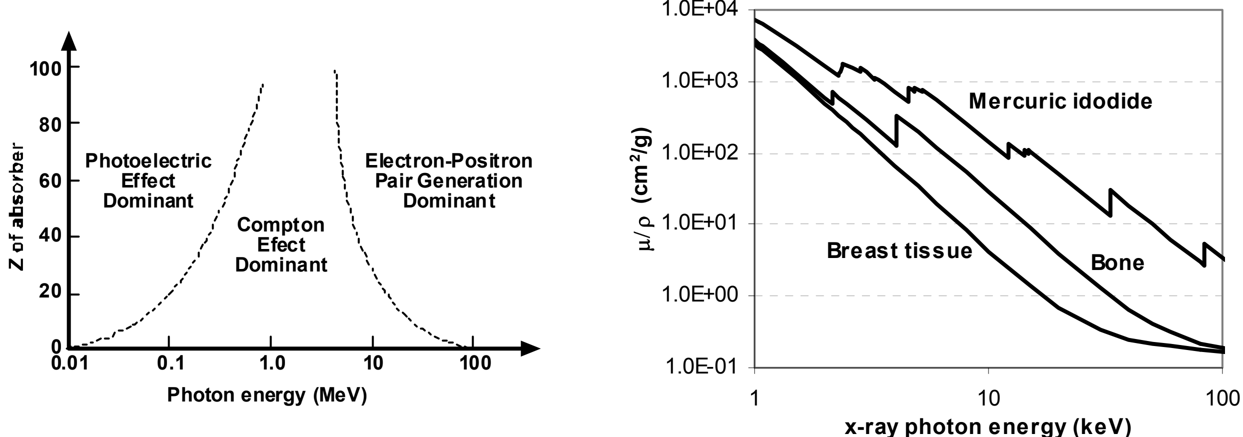


Figure 1.5. Different mechanisms of x-ray absorption in material (left), graph of mass attenuation coefficient for different materials versus x-ray photon energy (data compiled from: physics.nist.gov)

Although the absorption of an X-ray quantum is a single and momentary event, conversion of an X-ray to electric charge is a sequential process. For energies lower than 150 keV which is basically used for medical imaging, photoelectric effect is the dominant mechanism of X-ray absorption in materials. Upon absorption, the energy of the X-ray quantum is transferred to an electron which will produce numbers of electron-hole pairs or other energetic electrons through impact ionization. Secondary X-ray radiation my also happen if the incoming radiation quantum is stopped by an inner shell orbital electron. Secondary radiations will be absorbed the same way as the original incident X-ray and generate numbers of electron-hole pairs depending on the energy of the incoming radiation quantum and type of the absorbing material. The amount of energy required to

produce one electron hole pair in different materials is named as W. If an x-ray photon is absorbed, the number of generated electron hope pairs, N, would therefore be E/W, with E representing the energy of the absorbed X-ray photon.

Because the generated x-ray from an x-ray tube, for example, contains photons of different energy with different fluence, $\phi(E)$, the total absorbed x-ray energy, E_{ab}, in a detector with area of A is calculated as [21]:

$$E_{ab} = \sum_{E} \phi(E) A \eta(E) \frac{\mu_{ab}(E)}{\mu(E)} E \tag{1.2}$$

in which, E is the x-ray energy, $\mu(E)$ and $\mu_{ab}(E)$ are the x-ray attenuation, and absorption coefficients, and $\eta(E)$ is the x-ray quantum efficiency (QE) determined from:

$$\eta(E) = 1 - \exp[-\mu(E)d]. \tag{1.3}$$

where, d is the depth of the detector material. The x-ray spectra used in calculations of the fluence are obtained from a computer model. From this, the generated charge in the detector material Q_{gen} is determined by the ratio of absorbed energy per pixel E_{ab} and the energy W needed to create an electron-hole pair in the target material:

$$Q_{gen} = \frac{E_{ab}}{W}. \tag{1.4}$$

1.4.2 Direct and indirect x-ray detectors

Different detector materials are used for X-ray detection. If generated electron hole pairs have enough high mobility and long recombination life time they could be collected by applying a DC electric field to the detector. Such detectors are called photoconductor or semiconductor photodetectors, and the mechanism of X-ray detection using photoconductors is called direct detection (Fig. 1.6) because the X-ray energy is directly converted to electric charge. Direct detection of X-rays in photoconductors depends on

how many electron-hole pairs (EHPs) are generated upon absorption of X-rays and how effectively they are collected (charge collection efficiency). Therefore, any detector with lower value of (*W)* (equivalent to higher number of EHPs generated by an X-ray quantum) and higher carrier mobility-time product ($\mu\tau$) would be considered better, if the dark current is sufficiently low and the detector has a low image lag. Image lag is related to the memory effect of photoconductors which is primarily caused by slow de-trapping of trapped charges upon absorption of X-ray. Properties of a few of common photoconductors are listed in Table 1.1 among which amorphous selenium is the most common.

An ideal photoconductor for X-ray detection should have very small absorption thickness (less material and less applied voltage), high bandgap energy to have less dark current, and low value of *W* to generate more electron hole pairs, and high (and matched) value of mobility-life time constant for both electrons and holes to maintain efficient charge collection and fast imaging.

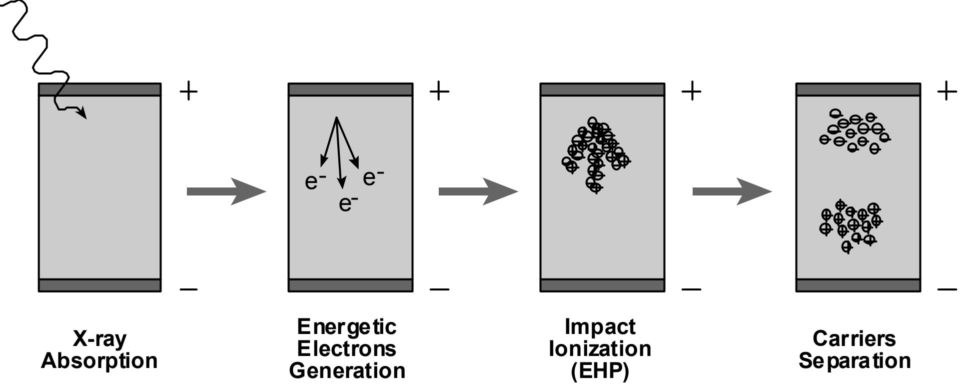


Figure 1.6. Different steps of direct x-ray detection using a biased photoconductor detector

Table 1.2. Common semiconductor x-ray detectors and their specifications [22]

Photoconductor	**Absorption depth for 60 keV(μm)**	**Eg (eV)**	**W± (eV)**	**$\mu_e\tau_e$ (cm^2/V.s)**	**$\mu_h\tau_h$ (cm^2/V.s)**
a-Se	976	2.3	45	$0.3 - 3 \times 10^{-6}$	$0.6 - 6 \times 10^{-5}$
HgI2	252	2.1	5	1.5×10^{-5}	10^{-7}
CdZnTe	280	1.7	5	5×10^{-4}	10^{-4}
Desired to be	***Low***	***high***	***Low***	***High***	***High***

Phosphorescent (and/or fluorescent) materials are widely used as X-ray detectors in which, generated electron hole pairs can quickly recombined in a direct band to band (or band-trap or trap-trap) transition and emit UV or visible photon of a specific wavelength; they are called phosphors and/or scintillators. In order to detect X-rays using scintillators, the visible photons emitted by the scintillator are next detected by a photodetector such as a pin diode, optically coupled to the scintillator (Fig. 1.7). Such detection mechanism is called indirect detection because of the two step conversion involved. Decay time and after glow are among most important and limiting factors of scintillators; short decay time and no afterglow are requited for high speed detection for real time applications. The disadvantage of scintillators is the fact that visible photons once generated scatter everywhere in the detector and therefore the spatial resolution would be poor compared to direct detection where high biasing electric field in the photoconductor reduces lateral diffusion of generated charge carriers. Special types of columnar scintillators, or composite materials should be used in order to improve the image resolution captured through indirect X-ray detection. Common scintillator materials are listed in Table 1.3.

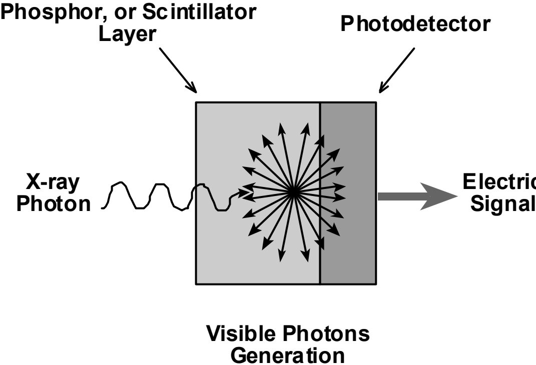


Figure 1.7. Indirect x-ray detection mechanism involves generation of visible photons in a phosphor (or scintillator) layer, and detection of those photons by a photodetector

Table 1.3. Common scintillator x-ray detectors (phosphors / scintillators) and their specifications (wikipedia.org)

Phosphor / Scintillator	**Color (wavelength)**	**Decay to 10%**	**Afterglow**
Gd_2O_2S:Tb	Green (545 nm)	1.5 ms	Low
Gd_2O_2S:Pr,Ce,F	Green (513 nm)	4 μs	No
Y_2O_2S:Tb	Light green (513 nm)	7 μs	No
$CaWO_4$	Blue (410 nm)	20 μs	No
CsI:Tl	Green (454 nm)	5 μs	High
CdS:In*	Green (525 nm)	<1 ns	No

* Basically used for detection of energetic electrons.

1.5 X-ray imaging for mammography[1]

1.5.1 Introduction to breast cancer

Breast cancer is caused when the body loses its control over proliferation of glandular cells in the breast. A death rate of 24.3% is reported among 179,000 women diagnosed with breast cancer in US in 1998. Breast cancer is considered one of the major killers of women. While some specific mutated genes are recognized to be responsible for at least 4% of breast cancer occurrence, the exact cause of breast cancer is still unknown to a large extent. Lack of sufficient information abut the cause of breast cancer has considerably increased the importance of mammography to detect breast cancer in its very early stages (in situ, or minimally invasive) as the only effective way to control it; i.e., before it reaches the point (metastasis) when treatment is ineffective.

1.5.2 Mammography

Mammography, or the X radiology of the breast is used for different purposes including a) investigating symptomatic patients (those who have been diagnosed with breast cancer), or screening of women in different ages, or to locate suspicious areas prior to a surgery or biopsy. Detection of breast cancer depends on identification of following traces in a mammogram:

- Appearance of a tumor mass
- Detection of certain amount of mineral deposits which is called microcalcification
- Distortion in normal tissue pattern
- Asymmetry between corresponding regions of left and right breast

[1] Information of this section is adapted or compiled from "Digital Mammography" by M. J. Yaffe, in "Handbook of Medical Imaging", Volume 1. Physics and Psychophysics, ch. 5, pp. 331-367, Edited by J. Beutel, SPIE publications, 1999

A mammography imaging system must be capable of visualizing above listed main features of the disease, encoded in minor changes in tissue x-ray attenuation associated with breast cancer. The imaging system should be able to perform following tasks with the least amount of patient delivered dose:

- Accurately measure intensity of transmitted x-ray through all regions of the breast.
- Amplify small contrast differences resulting from subtle differences in x-ray attenuation coefficient of the breast tissue.
- Provides high spatial resolution to visualize fine details of microcalcification

Because of these stringent requirements digital mammography is one of the most demanding but challenging medical x-ray modalities. General specifications of a mammography imager are listed in Table 1.4 [7].

Table 1.4. General requirements and specifications of a mammographic imager

Imager size (cm)	Small & medium: 18×24 Large: 24×30
Dell pitch (μm)	Best: 50 Typical: 75 Max: 100
X-rar spectrum (kVp)	30
Exposure range (mR)	0.6 – 240
Image charge per pixel for a-Se direct photoconductor detector (e^-/dell/mR)	1.68×10^5
Dynamic range (e^-)	$10^5 - 40\times10^6$

In addition to the previous list of tough requirements of digital mammography, an imager with high dynamic range is needed with pixel architecture capable of holding up to 40 million electrons, as well as providing linear response.

1.5.3 Tomosynthesis

Blurring tomography technique involves in moving both x-ray source and the detector during exposure, in such a manner that anatomical structures out of a plane of interest are blurred; rendering a relatively sharp image of that particular plane. This technique has been adapted to digital imaging and is refined to tomosynthesis in which, a series of 2D images are taken from different viewing angles. These images are then digitally processed to render tomographic images. Digital imaging has made it possible to extract tomographic images of different planes from the same set of images. In addition to that, tomosynthesis can be performed without breast compression, and therefore it can provide better Z information of suspicious tissues, and reduced structure noise compared to normal mammography.

Patient dose is a critical aspect of tomosynthesis. While certain amount of dose is required to obtain sufficiently high contrast mammograms, tomosynthesis should not delivered more than that dose, independent of the number of frames captured. If the dose is taken to be the same for mammography and tomosynthesis, it means less dose is available for each frame as the number of images is increased. Low noise imaging is therefore required to render sufficiently high contrast images with the reduced dose per frame in tomosynthesis. Fast imaging is the other requirement of tomosynthesis. While the total exposure time is limited, and should be kept as short as practical to eliminate image blurring due to patient's movements, taking a large number of frames in a limited short time requires high frame rate. Table 1.5 compares and contrasts general specifications and detector requirements of regular mammography and mammography tomosynthesis.

Table 1.5. Requirements of a tomosynthesis imager with pixel pitch of 100 μm

	Tomosynthesis	**Mammography**
Imager size (cm)	18×24	18×24
Pixel pitch (μm)	100	100
X-ray spectrum (kVp)	30	30
Number of frames	100	1
Frames per second	High: 50 – 100	-
Exposure range (mR)	0.006 – 0.24 /frame	0.6 – 240
Image charge per pixel for a-Se direct detector (e^-/pixel/mR)	6.72×10^5	6.72×10^5
Dynamic range (e^-)	$4\times10^3 – 1.6\times10^6$	$4\times10^5 – 1.6\times10^7$
Quantum noise level (e^-)	~1264	~12,640

It is expected that a digital imagers has the following features for mammography, in general, and mommography tomosynthesis, in particular:

- High resolution
- High dynamic range
- High gain and low noise
- High frame rate for fast imaging

Bibliography

[1]: P. J.W. Noble "Self-Scanned Silicon Image Detector Arrays", *IEEE Journal of Electron Devices*, vol. 15, no. 4, pp. 202–209, April 1968.

[2]: S. G. Chamberlain, "Photosensitivity and Scanning of Silicon Image Detector Arrays", *IEEE Journal of Solid-State Circuits*, vol. 4, no. 6, pp. 333–342, December 1969.

[3]: E. Fossum, “Charge-Coupled Devices and Solid State Optical Sensors”, Proc. SPIE vol. 1900, p. 2-14,

[4]: K. Spariotis et. al, “Novel direct digital modular x-ray device and system”, Proc. SPIE vol. 3336, pp. 529-536, Medical Imaging 1998.

[5]: B. J. Lechner, F. J. Marlowe, E. O. Nester, and J. Tults, “Liquid Crystal Matrix Displays,” Proceedings of IEEE vol. 59, pp. 1566, (1971).

[6]: A. Nathan et al, “a-Si AMOLED display backplanes on flexible substrates”, MRS Spring Meeting , Flexible Electronics-Materials and Device Technology, vol. 814, p.I3.1, (2004).

[7]: K.S. Karim, A. Nathan, J.A. Rowlands, "Alternate Pixel Architectures for Large Area Medical Imaging," in Medical Imaging 2001: Physics of Medical Imaging, L. Antonuk, M. Yaffe, Editors, SPIE vol. 4320, pp. 35-46, February 2001.

[8]: Karim, K.S., Nathan, A., Rowlands, J.A., Kasap, S.O., ‘X-ray detector with on-pixel amplification for large area diagnostic medical imaging,’ IEE Proceedings on Circuits, Devices and Systems, 2003, **150**, (4), pp. 267-273.

[9]: Karim, K.S., Sanaie, G., Ottaviani, T., Izadi, M.H., Taghibakhsh, F., ‘Amplified pixel architectures in amorphous silicon technology for large area digital imaging applications,’ Journal of Korean Physical Society, 2006, **48**, (1), pp. 585-591.

[10]: Karim, K.S., Nathan, A., Rowlands, J.A., ‘Amorphous silicon pixel amplifier with VT compensation for low noise digital fluoroscopy’, IEEE International Electron Devices Meeting (IEDM) Technical Digest, 2002, pp. 215-218.

[11]: F. Taghibakhsh, K. S. Karim, ‘High Dynamic Range 2-TFT Amplified Pixel Sensor Architecture for Digital Mammography Tomosynthesis’, IET Circuits Devices and Systems, vol. 1, issue 1, pp. 87-92, February 2007

[12]: J. E. Lilienfeld, “Device for Controlling Electric Current,” US Pat. 1,900,018 (1933).

[13]: M. Dobler, R. Bunz, E. Lueder, and T. Kallfass, “Fabrication of CdSe-TFTs with High Mobility of 300 cm^2/V-s for a 140,000-pel AMLCD,” op. cit.

[14]: P. G. LeComber, W. E. Spear, and A. Ghaith, “Amorphous Silicon Field-Effect Device and Possible Application,” Electronic Letters, vol. 15, pp. 179, (1979).

[15]: P. G. LeComber, W. E. Spear, and A. Ghaith, “Amorphous Silicon Field-Effect Device and Possible Application,” Electron. Lett. 15, 179 (1979).

[16]: W. M. M. Kessels, A. H. M. Smets, D. C. Marra, E. S. Aydil, D. C. Schram, and M. C. M. van de Sanden, “On the growth mechanism of a-Si:H,” Thin Solid Films, vol. 383, pp. 154–160, 2000.

[17]: J. Jang, “Preparation and Properties of Hydrogenated Amorphous Silicon Thin-Film Transistors”, chap. 2, sec. 2, in “Thin Film Transistors”, 1st edition, Marcel Dekker, Inc., NY, 2003, edited by C.R. Kagan and P. Andry.

[18]: A.T. Voutsas, M.K. Hatalis, “Thechnology of Polysilicon Thin-Film Transistors”, chap. 4 in “Thin Film Transistors”, 1st edition, Marcel Dekker, Inc., NY, 2003, edited by C.R. Kagan and P. Andry.

[19]: M. Lee, J. Yoo; M. Han, “Low-temperature polysilicon TFT with counter-doped lateral bodyterminal”, Electronics Letters, vol. 38, no. 5, pp. 255 – 256, (2002).

[20]: M. Fonrodona, J, Escarre, F. Villar, D. Soler, J. Bertomeu, J. Andreu, A. Saboundji, N. Coulon, N. Mohammed-Brahim, 2005 Spanish Conference on Electron Devices, 183-186, (2005).

[21]: W. Zhao and J. A. Rowlands, “X-ray imaging using amorphous selenium: Feasibility of a flat panel self-scanned detector for digital radiology,” *Medical Physics*, 22(10), pp. 1595-1604, 1995.

[22]: M. Yunus, “Monte Carlo Modeling of the Sensitivity of X-ray Photoconductors”, Master of science thesis, Department of Electrical Engineering, Saskatoon, University of Saskatchewan, April 2005.

2

Existing Pixel Architectures for Large Area Digital Imaging

This chapter describes various existing pixel architectures for large area digital imaging to provide the background information [1] for the next chapter where novel architectures for high resolution digital imaging are introduced. Transfer function of existing architectures are calculated, using which different pixel architectures are compared and contrasted based on their performances such as conversion gain, and readout speed, as well as pixel complexity, size and fabrication reliability.

2.1 Passive Pixel Sensor Architecture

2.1.1 Introduction

The passive pixel sensor (PPS) is possibly the simplest architecture for large area imaging [2, 3], and provides the most compact pixel design for high resolution imaging. The architecture of a PPS as shown in Fig. 2.1 consists of a detector connected to a transistor switch. It is called "passive" because in PPS architecture the transistor operates as passive switch rather than an active amplifying device. Large area two dimensional arrays of passive pixel sensors employing direct or indirect x-ray detectors have been developed and are commercially available, known as, flat panel imagers (FPIs) or flat panel detectors (FPDs) [4]. Today, the PPS is the industry standard architecture for large are x-ray imagers for both direct and indirect x-ray detectors.

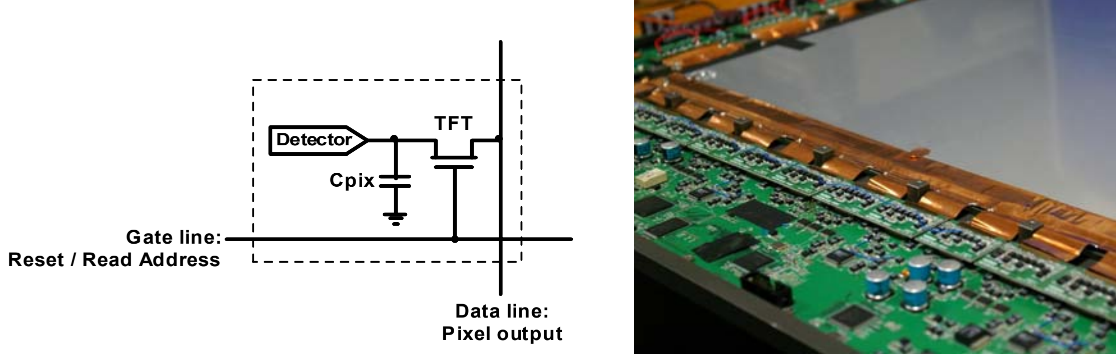


Figure 2.1. Architecture of a passive pixel sensor (left), close-up picture of a corner of a Samsung (039-s) PPS based 45 cm × 45 cm indirect detection flat panel detector with 149μm pixel pitch (http://www.gizmag.com/samsung-digital-x-ray-detector/8396)

The detector can be either a photo diode, such as a-Si pin diode coupled to a scintillator layer for x-ray detection, or a photoconductor such as amorphous selenium (a-Se) for direct x-ray detection. In case a photodiode is used, the junction capacitance of the diode would be the large enough, so that there would be no need of a physical pixel capacitor.

In case of using a photoconductor such as a-Se, because of the large a-Se thickness required to stop x-ray, the detector capacitance would be small, so that a physical capacitance is needed to hold the detector charge.

2.1.2 PPS operation

Capturing images using PPS architectures consists of two steps: 1) *Integration*, and 2) *readout/reset* [1, 2]. During *Integration* mode, the TFT switch is OFF, and the electric charge generated in the detector as the result of incident radiation, is deposited on C_{pix}. In the *Readout/Reset* mode the TFT switch is turned ON and the stored charge on the C_{pix} is transferred to the charge amplifier via data line, where it is converted to an equivalent voltage, V_{out}. Figure 2.1 shows the circuit diagram of a PPS connected to the column charge amplifier via data line. When the charge is read out at the end of the readout mode, C_{pix} charge is reset to zero and the pixel is ready for the next *Integration*.

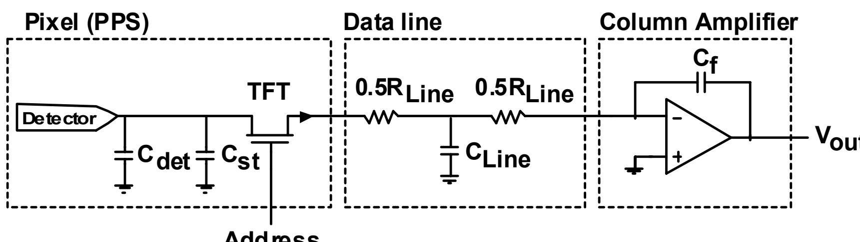


Figure 2.2. The circuit diagram representing a passive pixel sensor connected to the column charge amplifier via the data line

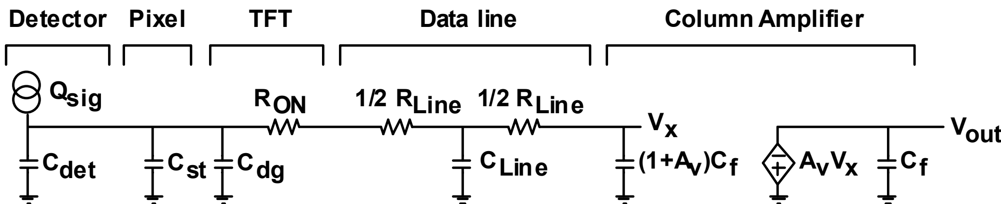


Figure 2.3. The circuit model of one PPS pixel connected to the column charge amplifier

2.1.3 Characteristic function of PPS architecture

The circuit model of a passive pixel connected to a charge amplifier via a resistive/capacitive data line is shown in Fig. 2.3, where the switching TFT is simply modeled by its gate overlap capacitances and drain-source resistance. The pixel capacitance C_{pix}, is the sum of detector capacitance, C_{det}, the pixel storage capacitance, C_{st}, and the drain-gate capacitance, C_{dg} [1]

$$C_{pix} = C_{\det} + C_{st} + C_{dg} \tag{2.1}$$

The data line is simply modeled by a line resistance and capacitance, R_{Line} and C_{Line} respectively. For each column, the parasitic line capacitance, C_{Line}, has three major components: 1) the source-gate capacitance of all TFTs connected to the column, 2) the cross-over capacitances of the said column data line with all the gate lines, and 3) pissible cross-over capacitance of the data line with detector bias line or other metal layers depending on the design. Assuming the voltage gain of the charge amplifier is A_v, the miller capacitance of the feedback capacitor C_f, i.e., $(1+A_v)C_f$ appears at the input of the charge amplifier. At the end of a very long readout time, the detector deposited signal charge, Q_{sig}, is distributed over all capacitors of the system, and a steady state V_{out} is generated.

$$V_{out} = A_v V_x = \frac{A_v Q_{sig}}{C_{Pix} + C_{Line} + (1 + A_v)C_f} \tag{2.2}$$

Therefore, for finite readout time, when Q_{sig} is not fully distributed over all capacitances, the output voltage is approximated to:

$$V_{out} = \frac{\eta_{TR}\, Q_{sig}}{C_f} \tag{2.3}$$

where η_{TR} is the charge transfer efficiency of the readout cycle, i.e., the ratio of transferred to detector deposited charge due to finite readout time. In the rest of this

section we attempt to evaluate η_{TR} based on response time of the PPS architecture to calculate the output voltage of the PPS architecture with charge amplifier.

Figure 2.4. The circuit model for estimation of charge transfer time constant of PPS architecture

Zero time constant approximation is used to estimate the time constant associated with transfer of charge from pixel detector to the integrator capacitor. Given the fact that the input of the charge amplifier is virtually grounded (Fig. 2.2), there would be three time constants associated with each of C_{Line}, C_{GS} and C_{Pix} independently as: $\tau_1 = C_{Line} R_{Line}/2$, $\tau_2 = C_{GS} R_{Line}$, $\tau_3 = C_{Pix}(R_{ON} + R_{Line})$. The charge transfer time constant τ_{TR} is then calculated as:

$$\tau_{TR} \approx \sqrt{\tau_1^2 + \tau_2^2} = \sqrt{C_{Pix}^2 (R_{ON} + R_{Line})^2 + C_{Line}^2 R_{Line}^2 / 4} \tag{2.4}$$

Because of the large value of R_{ON} compared to R_{Line}, τ_2 is the much larger than τ_2, and it dominates the time constant.

$$\tau_{TR} \approx C_{Pix} (R_{ON} + R_{Line}) \tag{2.5}$$

The ON state resistance of a switch TFT, derived from its linear characteristic region, depends on its geometry as well as its gate-source voltage, and is defined by the following equation:

$$R_{ON} = [K(V_{read} - V_t)]^{-1} \tag{2.6}$$

Here, K is the gain factor of the TFT equal to the product of field effect mobility, μ_{FE}, gate capacitance per unit area, C_0, and the aspect ratio, W/L of the switch TFT, with V_t representing its threshold voltage. V_{read} is the voltage applied to the gate line, and should

be high enough to R_{ON} as low as practical When the pixel is read out for t_{Read} seconds, the charge transfer efficiency is calculated as follow:

$$\eta_{TR} = \frac{A_v\left(1-\exp\left(-t_{\mathrm{Re}ad}/\tau_{TR}\right)\right)}{1+A_v+\left(C_{Pix}+C_{Line}\right)/C_f} \tag{2.7}$$

Equation 2.7 clearly shows the role of different components of the PPS architecture in charge transfer efficiency which determines the output voltage as stated in Eqn. 2.3 Also, it shows that high value of A_v and enough long readout time are necessary to have close to unity charge transfer efficiency. Substituting Eqn. 2.7 in 2.3 results in characteristic equation of PPS with charge gain as follow:

$$V_{out\ PPS} = \frac{Q_{sig}}{C_f}\frac{A_v\left(1-\exp\left(-t_{\mathrm{Re}ad}/\tau_{TR}\right)\right)}{1+A_v+\left(C_{Pix}+C_{Line}\right)/C_f} \tag{2.9}$$

2.1.4 PPS architecture with voltage amplifier

In PPS architecture, non-inverting voltage amplifiers (with voltage gain of A_v, and high input impedance), or inverting voltage amplifiers [1] can also be used in place of charge amplifiers, which are considered to be expensive components. Assuming large enough input impedance column amplifier for no loss of charge, Q_{sig} will be distributed over C_{pix} and C_{Line}, and the output voltage is calculated to be:

$$V_{out\ V-PPS} = \frac{Q_{sig}}{C_{pix}+C_{Line}} A_v\ \left(1-\exp\left(-t_{\mathrm{Re}ad}/\tau_{TR}\right)\right) \tag{2.10}$$

Although Eqn. 2.10 shows that the charge to voltage conversion gain could be considerably large with large enough A_v, but because C_{Line} is much larger than C_{pix}, the input voltage at the column voltage amplifier would be very small, making this readout approach vulnerable to noise, especially for low input signal values [1].

2.1.5 Numeric values and practical considerations for PPS architecture

To compare the two different readout schemes of PPS architecture discussed, the charge to voltage conversion gain, or, the ratio of V_{out}/Q_{sig} is calculated [1] based on nominal values of parameters as listed in table 2.1.

Table 2.1. Nominal values of parameters for PPS architecture

Parameter	Value	Parameter	Value
μ_{FE}	0.5 cm^2/Vs	C_{pix}	0.5 pF
C_0	20.0 nF/cm^2	C_{Line}	50.0 pF
W	50 μm	R_{Line}	1.0 kΩ
L	10 μm	τ_{TR}	1.0 μs
$V_{read} - V_t$	10.0 V	C_f	0.5 pF
R_{ON}	2.0 MΩ	A_v	100
$\boldsymbol{V_{out\ PPS} / Q_{sig}}$	0.99 V/pC	$\boldsymbol{V_{out\ V\text{-}PPS} / Q_{sig}}$	1.98 V/pC

2.2 Active Pixel Sensor Architectures

2.2.1 Introduction

As introduced in chapter 1, the Active Pixel Sensor (APS) architecture appeared succeeding CCDs as an electronic imaging device fully compatible with the CMOS technology to provide low-power and low-cost solution for digital imaging. The classical APS architecture consists of a pixel detector and three transistors (Fig. 2.5), and is known as three-transistor (3T) APS. In contrast to PPS where the pixel output signal is the original detector integrated charge, in APS the sensor value is converted to an equivalent voltage or current using an on-pixel amplifier. This results in improved noise and/or readout speed performance [5-7].

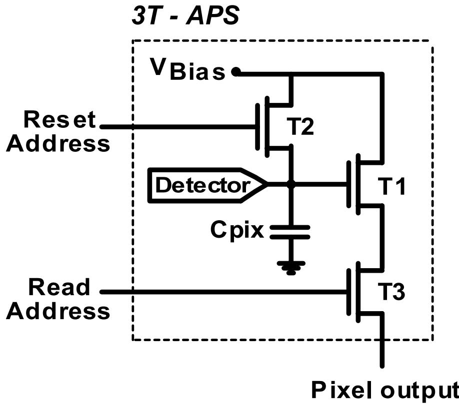


Figure 2.5. Standard three-transistor APS architecture

2.2.2 APS operation and classification

The operation of APS consists of three steps: *Reset*, *Integration*, and *Readout* [1]. A transistor switch, T2, is used to reset the pixel sensor to a preset voltage prior to integration. The collected charges during integration are deposited on the pixel capacitor, C_{pix}, modulating its preset voltage. To read the pixel value, transistor T3 is switched on and the voltage of the pixel sensor is buffered out by transistor T1. Depending on the type of column amplifier connected to the APS imager, the output of the APS circuit can be read either in terms of voltage, which is called voltage mediated APS (V-APS), or in terms of current, in which case, the APS pixel is called current mode (or current mediated) APS (C-APS).

2.2.3 Voltage mediated APS

A voltage buffer (or a voltage amplifier) is used as the column amplifier of a V-APS imager, with a load resistance across which the output voltage is dropped (Fig. 2.4) [8]. During readout when transistor T3 is switched on, the drain current of T1 charges up the parasitic line capacitance of the data line and the voltage at the input of the column

voltage buffer reaches the value of $\frac{R_{load}}{R_{load}+R_{ON}}\left(V_{pix}-V_{t}\right)$. The time variation of the output voltage is approximated with a single pole system having a single the constant of $(R_{ON} \| R_{Load})\ C_{Line}$. Therefore the output voltage of the V-APS is approximated by:

$$V_{out\,V-APS} \approx \frac{R_{load}}{R_{load}+R_{ON}}\left(V_{RST}-V_{t}-\frac{Q_{sig}}{C_{Pix}}\right)\left(1-e^{-t/R_{ON}\|R_{Load}C_{Line}}\right) \quad (2.11)$$

Here, the $V_{RST} - Q_{sig}/C_{Pix}$ is the pixel voltage at the end of the integration period when Q_{sig} has been deposited on the pixel capacitor C_{Pix}, and t is the readout time. As (2.11) shows, R_{Load} should be much higher than R_{ON} to have high enough output voltage. In that case, the time constant is mostly determined by R_{ON}. For readout times much larger than the time constant, the output voltage of the V-APS approaches $V_{RST} - V_t - Q_{sig}/C_{Pix}$; gain of $-1/C_{pix}$, and offset value of $V_{RST} - V_t$. The offset value is corrected by subtracting the image from a dark frame, which is called *Double Sampling*. That is, the output voltage containing image information is subtracted from a previously read value of the output voltage with no radiation (i.e., when $Q_{sig} = 0$). Double sampling makes the output independent of inevitable variations in V_t across the large area imager. Therefore, the final DS corrected value of the output voltage for V-APS architecture is described as:

$$\Delta V_{out\,V-APS} = V_{out}\big|_{Qsig=0} - V_{out}\big|_{Qsig\neq 0} = \frac{Q_{sig}}{C_{Pix}} \quad (2.12)$$

$$Gain_{V-APS} = \frac{\Delta V_{out\ V-APS}}{Q_{sig}} = \frac{1}{C_{Pix}} \quad (2.13)$$

As described by Eqn. 2.13, the V-APS charge to voltage conversion gain of $1/C_{Pix}$ would be high if the pixel sensor capacitance is kept as low as possible, which enables detection of very weak signal charges, while the architecture is amenable to noise because the voltage at the input of the column voltage buffer is not attenuated. However, because of

the long RC time constant associated with the high ON state resistance of T3 a-Si TFT, R_{ON}, and large value of parasitic capacitance of the data lines, C_{Line}, the readout time of V-APS architecture is long, and therefore the architecture is not suitable for fast imaging if the large area FPI is fabricated using a-Si technology. The most important aspect of V-APS is that, the voltage at the input of the column amplifier is almost equal to the detector node voltage and is not attenuated the way it is in PPS with voltage amplifier. This provides the possibility of using inexpensive voltage buffers in place of charge integrators for column amplifier without comprising the noise performance of the imager. Equation 2.13 shows that the charge to voltage conversion gain of the V-APS is 1 V/pC in the best scenario [8].

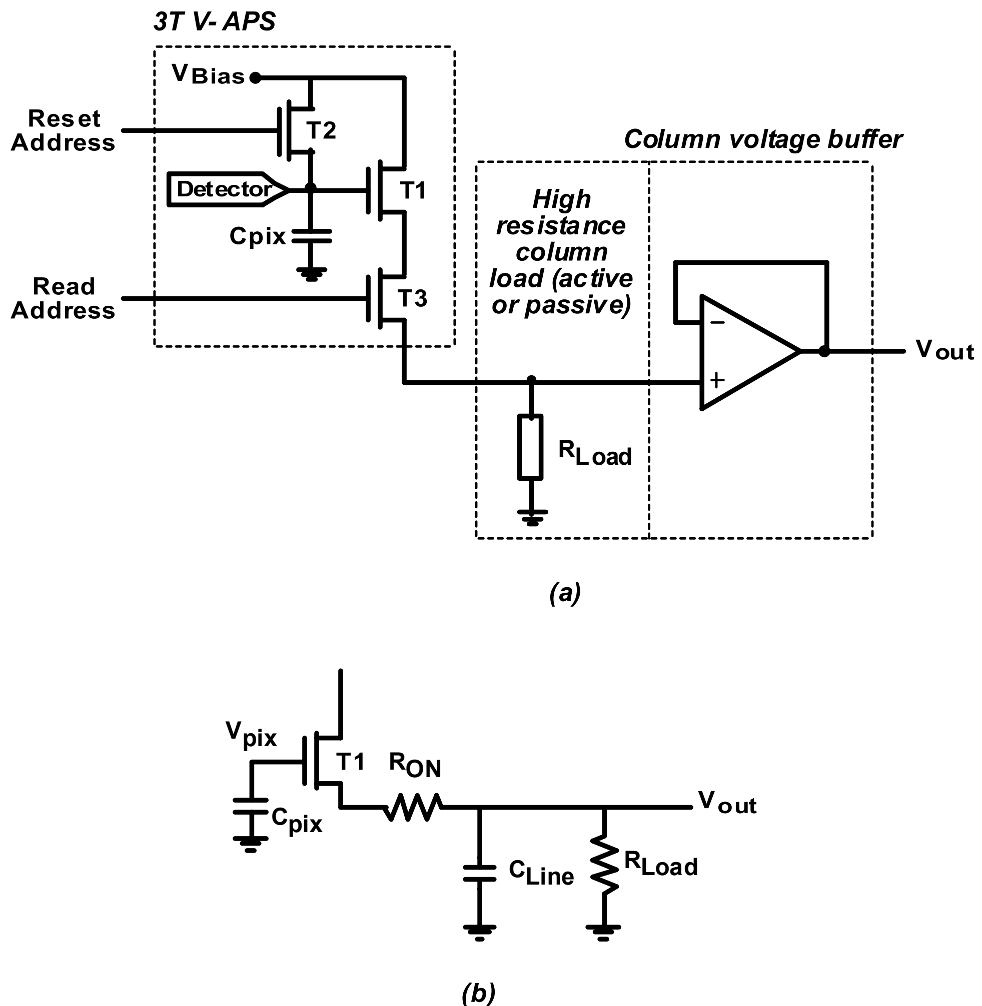
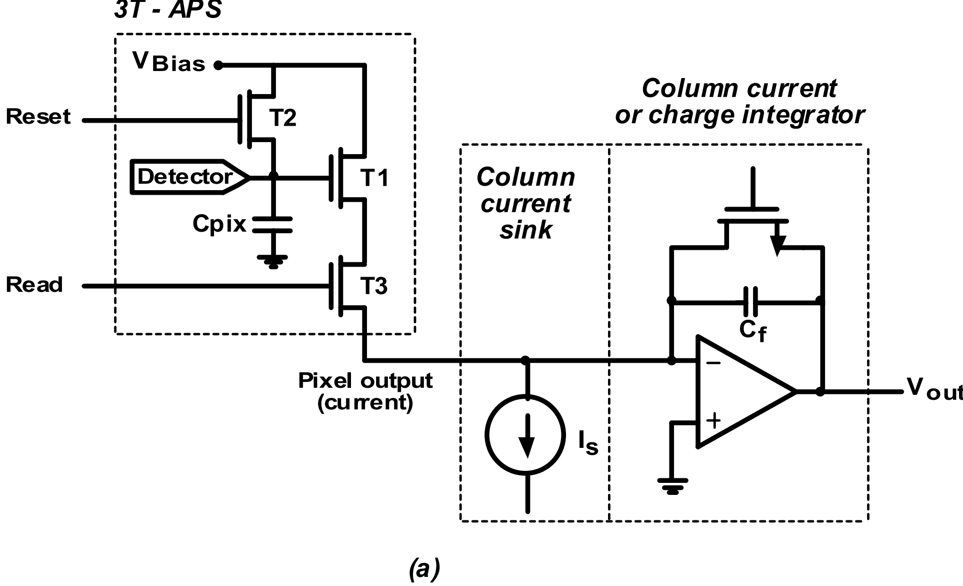


Figure 2.6. (a): Diagram of a V-APS architecture. (b): The circuit model in *Readout* mode

2.2.4 Current mediated APS

In order to suppress the long time-constant associated with the V-APS readout, current mediated active pixel sensor is developed [9] in which the data line is virtually grounded by a high gain charge amplifier or a trans-impedance amplifier more or less the same as in PPS described previously (Fig. 2.2).



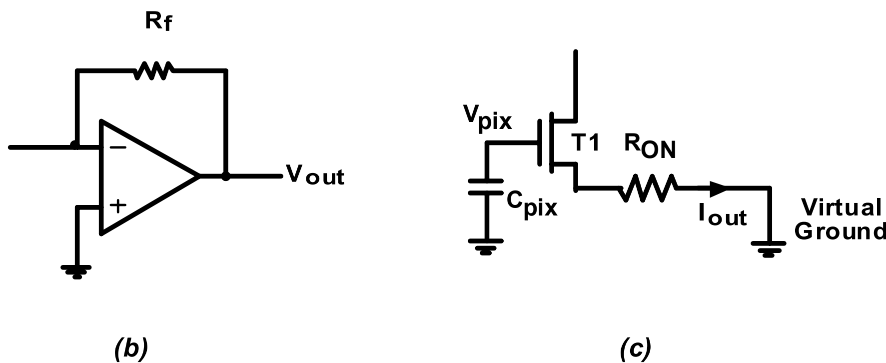


Figure 2.7. (a): Illustration of C-APS architecture with current integrator. (b) Trans-impedance amplifier that can be used in place of the current integrator as the column amplifier. (c): The pixel circuit model in *Readout* mode

Figure 2.7 shows the C-APS pixel circuit connected to the column amplifier which can be a current integrator or a transimpedance amplifier. The pixel output current of a C-APS architecture (Fig. 2.7.c) is derived as a function of pixel sensor voltage at the pixel sensor capacitance, V_{pix} [9].

$$i_D = \frac{1 + KR_{ON}\left(V_{Pix} - V_t\right) - \sqrt{1 + 2KR_{ON}\left(V_{Pix} - V_t\right)}}{KR_{ON}^2} \tag{2.14}$$

In which K is the gain factor ($C_0\,\mu_{FE}\,W/L$) of the AMP TFT, and V_{Pix} is equal to $V_{RST} - Q_{sig}/C_{Pix}$. With double sampling, the change in the drain current is attributed to Q_{sig} and can be expressed as a linear function for small variations in Q_{sig}.

$$\Delta i_D = i_D\big|_{Qsig=0} - i_D\big|_{Qsig\neq 0} = \frac{1}{R_{ON}}\left(1 - \frac{1}{\sqrt{1+2KR_{ON}\left(V_{RST}-V_t\right)}}\right)\frac{Q_{sig}}{C_{Pix}} \tag{2.15}$$

In case a trans-impedance amplifier is used, the change in output current is converted to a voltage change at the output of the trans-impedance amplifier.

$$\Delta V_{out} = \frac{R_f}{R_{ON}}\left(1 - \frac{1}{\sqrt{1+2KR_{ON}\left(V_{RST}-V_t\right)}}\right)\frac{Q_{sig}}{C_{Pix}} \tag{2.16}$$

The gain of the APS architecture, with a trans-impedance amplifier here, is defined as the ratio of changes in the output voltage to the signal charge, or:

$$Gain_{C-APS} = \frac{\Delta V_{out}}{Q_{sig}} = \frac{R_f}{C_{Pix}R_{ON}}\left(1 - \frac{1}{\sqrt{1+2KR_{ON}\left(V_{RST}-V_t\right)}}\right) \tag{2.17}$$

Compared to the gain of V-APS from Eqn. 2.13 which is $1/C_{Pix}$, by proper choice of feed back resistor and proper design of the READ and AMP transistor, the C-APS gain could be larger than pixel gain of V-APS.

Charge amplifiers can also be used for column readout circuitry, in that case, the output current is integrated over the readout time to build the output voltage on the feedback capacitor of the charge amplifier. The gain of the C-APS with charge amplifier Eqn. 2.16, is derived similar to Eqn. 2.17.

$$Gain_{C-APS} = \frac{\Delta V_{out}}{Q_{sig}} = \frac{t_{\text{int}}}{C_{Pix}C_f R_{ON}}\left(1 - \frac{1}{\sqrt{1+2KR_{ON}\left(V_{RST}-V_t\right)}}\right) \tag{2.18}$$

Equation (2.18) shows a time varying gain, which is interesting from static and real time imaging applications point of view, for providing a method of linear gain control.

Table 2.2. Nominal values of parameters for C-APS architecture

Parameter	Value	Parameter	Value
μ_{FE}	0.5 cm^2/Vs	C_{pix}	0.5 pF
C_0	20.0 nF/cm^2	C_{Line}	190 pF
W/L	100 μm/10 μm	R_{Line}	1.0 kΩ
R_f	1 MΩ	τ_{TR}	0.5 μs
$V_{read} - V_t$	10.0 V	C_f	0.5 pF
R_{ON}	1.0 MΩ	$V_{RST} - V_t$	10.0 V
K	0.1 μA/V^2	t_{int}	5 μs
$\boldsymbol{V_{out\ C\text{-}APS} / Q_{sig}}$ (Eqn. 2.17)	2.0 V/pC	$\boldsymbol{V_{out\ C\text{-}PPS} / Q_{sig}}$ (Eqn. 2.18)	8.45 V/pC

Comparing this result with those for V-APS and PPS, we see that we have on-pixel gain. The fact is that increasing the integration time will increase the gain. For example, in tint is taken to be 10 μs, then the C-APS gain would be 16.9 V/pC resulted from Eqn. 2.18. This high value of the pixel gain helps detection of weak signals.

2.3 Hybrid pixel designs

Because of providing gain, APS is particularly a suitable architecture for low dose applications, such as fluoroscopy. However, for higher dose modalities such as chest radiography and mammography where the changes in the sensor signal is large, the inherent nonlinearity of C-APS becomes a big issue. Hybrid passive-active pixel architectures are one solution for this problem (Fig. 2.8) [10]. Depending on dose level, it is possible to read the pixel output both in PPS or APS, providing high gain for low

dynamic range modalities such as fluoroscopy, and linear response and high dynamic range for high dose modalities such as mammography.

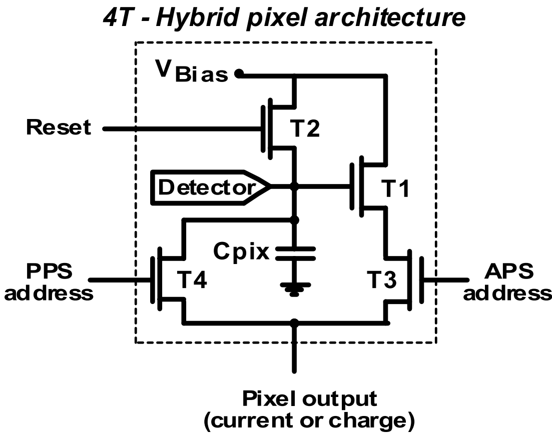


Figure 2.8. Hybrid pixel architecture, employing both PPS and APS

Because of increased transistor and line counts per pixel [11] which inversely affect pixel size and resolution as well as fabrication reliability, four-transistor hybrid designs are not considered for high resolution large area digital imaging applications here in this thesis.

Bibliography

[1]: K.S. Karim, “Pixel Architectures for Digital Imaging Using Amorphous Silicon Technology”, Ph.D. Thesis, University Of Waterloo, 2002.

[2]: I. Fujieda, R.A. Street, R.L. Weisfield, S. Nelson, P. Nylen, V. Perez-Mendez, and G. Cho, “High Sensitivity Readout of 2D a-Si Image Sensors,” Japan Journal of Applied Physics, 32, pp. 198-204, 1993.

[3]: W. Zhao and J. A. Rowlands, “Digital radiology using active matrix readout of amorphous selenium: Theoretical analysis of detective quantum efficiency,” Medical Physics, 24(12), pp. 1819-1833, 1997.

[4]: http://www.japancorp.net/Article.Asp?Art_ID=5742, accessed on: Thursday, May 01, 2008.

[5]: Karim, K.S., Nathan, A., Rowlands, J.A., Kasap, S.O., ‘X-ray detector with on-pixel amplification for large area diagnostic medical imaging,’ IEE Proceedings on Circuits, Devices and Systems, 2003, 150, (4), pp. 267-273.

[6]: Karim, K.S., Nathan, A., Rowlands, J.A., ‘Amorphous silicon pixel amplifier with VT compensation for low noise digital fluoroscopy’, IEEE International Electron Devices Meeting (IEDM) Technical Digest, 2002, pp. 215-218.

[7]: street Poly APS

[8]: K.S. Karim, A. Nathan, J.A. Rowlands, "Active pixel sensor architectures in a-Si:H for medical imaaging," Journal of Vacuum Science and Technology A, 20(3), pp. 1095-1099, May 2002.

[9]: K.S. Karim, A. Nathan, J.A. Rowlands, "Amorphous silicon active pixel sensor readout circuit for digital imaging," IEEE Transactions on Electron Devices: Special Issue on Image Sensors, 50(1), pp.200-208, January 2003.

[10]: M.H. Izadi, K.S. Karim, A. Nathan, J.A. Rowlands, “Low-Noise Pixel Architectures for Advanced Diagnostic Medical X-ray Imaging Applications ,” in SPIE Medical Imaging 2006: Physics of Medical Imaging, Feb 2006.

[11]: M.H. Izadi, K.S. Karim, "High dynamic range pixel architecture for advanced diagnostic medical X-ray imaging applications," Journal of Vacuum Science and Technology A, 24(3), pp 846-849, May 2006.

3

High Resolution Pixel Architectures

This chapter which is in fact the summary of a few publications (see Appendix B), introduces a new generation of pixel architectures for high resolution low noise large area imagers as the core of this thesis on pixel circuit design. The novel architectures are designed based on a two-transistor (2T) hybrid active/passive architecture where the main thin film transistor of the pixel circuit operates switched amplifier, eliminating the need for a row-select (or read) transistor that appears in the standard APS architecture. This has been made possible by employing a novel charge-gated thin film transistor. Different 2T pixel architectures are compared and contrasted with existing architectures (previously studied in chapter 2) based on their performance, fabrication reliability and imager system complexity. Criteria such as on-pixel gain, input referred noise and pixel size are used for performance evaluation, whereas, architecture complexity, density of transistors and number of lines per pixel are the measures for fabrication reliability. Finally, circuit requirements for operating the imager such as driving and signal processing circuits and their compatibility with the existing flat panel technology are discussed to evaluate system complexity of images fabricated using such pixel architectures.

3.1 Charge-Gated Thin Film Transistor

3.1.1 Introduction

Thin film transistors (TFTs) originally developed as switching elements for large area active matrix liquid crystal displays (AMLCDs) and flat panel imagers [1, 2] are finding analog applications such as current drivers in Organic LED displays [3] or as amplifiers in active pixel sensor (APS) imaging arrays [4]. The analog implementation is a result of advances in amorphous silicon (a-Si) fabrication technology, as well as use of innovative circuits to overcome speed, stability and noise shortcomings in the a-Si material [5].

Compared to crystalline silicon transistors implemented a-Si TFTs are large in size. Therefore, employing TFT circuits at the pixel level requires minimizing pixel transistor counts for high resolution applications, as well as reducing gate/data line interconnections to reduce reliability issues in large area fabrication. In large area sensor arrays using a classic three transistor (3T) APS architecture for example [6], electric charge generated in the pixel detector, e.g., an amorphous selenium photoconductor, is deposited on the pixel storage capacitor connected to the gate of an amplifying transistor. The amplifying transistor is connected to the column output line by an addressing switch transistor and yet another switch transistor is used to reset the sensor node voltage.

In this section, a charge-gated TFT (CG-TFT) capable of integrating the sensor charge as well as switching its output current ON and OFF is introduced to replace the amplifier and readout TFT in the 3T APS architecture; The readout circuit fabricated using CG-TFT was reported to IEEE International Electron Devices Meeting (IEDM 2007) [7].

3.1.2 Charge-gated TFT

A charge gated transistor is obtained when a second gate (i.e. the charge gate) is introduced between the traditional gate and semiconductor layer of a field effect transistor. Fig. 3.1 shows two configurations of a staggered top gate TFT with the charge gate between the gate and the semiconducting channel. The charge gate is electrically

floating, i.e., it is embedded inside the insulating gate dielectric, and connected to a high resistance, low parasitic capacitance photoconductive detector, e.g., amorphous selenium. Fig. 3.1 shows two implementations of the charge gated TFT, the latter, a bottom gate coplanar configuration is sometimes preferable because it requires fewer masks and fabrication steps, as well as providing a completely exposed charge gate electrode for direct contact to an overlying detector. Because the charge gate is electrically conductive, the two device configurations shown in Fig. 3.1 are electrically identical. In either case, the gate is capacitively coupled to the TFT channel via the charge gate. The coupling capacitance between the gate and the charge gate is C_g, and the capacitance between the charge gate and the channel (including overlap) is C_c. The dielectric thickness for these capacitances is not necessarily the same and can be optimized independently. For example, in the coplanar configuration of Fig. 3.1, t_1 is always smaller than t_2 when a fabrication process using double dielectric deposition is used [8].

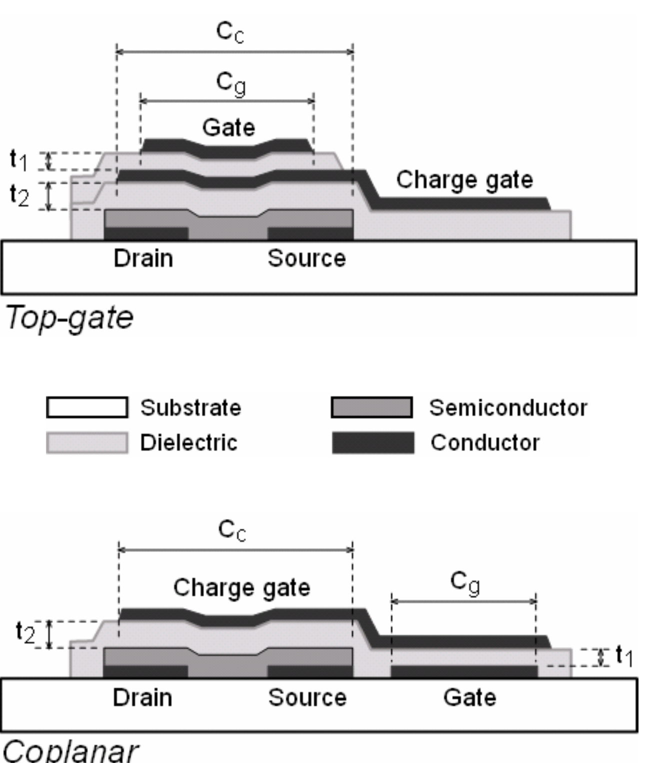


Fig. 3.1. Cross-section of charge-gated field effect transistors in a top gate and coplanar configuration - the two devices are electrically identical

The electronic band diagrams of the device are shown in Fig. 3.2. Assuming zero flat band voltage when gate and source voltages are zero and the same area for C_g and C_c, the device is normally biased as a conventional TFT and the potential of the floating charge gate with respect to source, V_{gs}, follows the potential induced by the gate due to the applied gate voltage, V_G. When F_n, the quasi Fermi level for electrons, is close to the conduction band, we neglect small variations of semiconductor surface potential (since F_n is effectively pinned due to the channel screening effect) compared to the large changes in applied V_G. Thus, V_{gs} is approximated as:

$$V_{gs} \approx \frac{C_g}{C_g + C_c} V_G \tag{3.1}$$

A large enough V_G increases V_{gs} to allow accumulation of carriers in the channel for the device to turn ON. When positive electric charge is deposited on the charge gate, as shown in Fig. 3.2, V_{gs} increases to V_{gs1}, and subsequently increases the carrier concentration in the channel, in spite of the constant gate voltage, V_G. Deposition of negative charge results in a reduction of carrier concentration in the channel, which allows the current conduction in the channel to be modulated by charge deposited on the charge gate. Even with positive charge on the charge gate, the device can be turned OFF (non-conducting) by applying a negative voltage to the gate as shown in Fig. 3.2.

The voltage difference between the charge gate and the source can be expressed as a function of V_G, and deposited charge, ΔQ. Using the current equation for field effect transistors, the drain current of the CG-TFT can be obtained. The equivalent capacitance at the charge gate node is $C_c + C_g$, where C_c is approximately constant and given as, $C_c \approx C_0 W\left(L_g + L_{ov}\right); C_0 = \frac{\varepsilon_0 \varepsilon_r}{t_2}$. Here, ε_r is the relative permittivity of the dielectric, W and L_g are the channel width and length of the device and L_{ov} is the total overlap length of the charge gate on drain and source contacts. The amount of voltage change as the result of depositing ΔQ on the gate charge is:

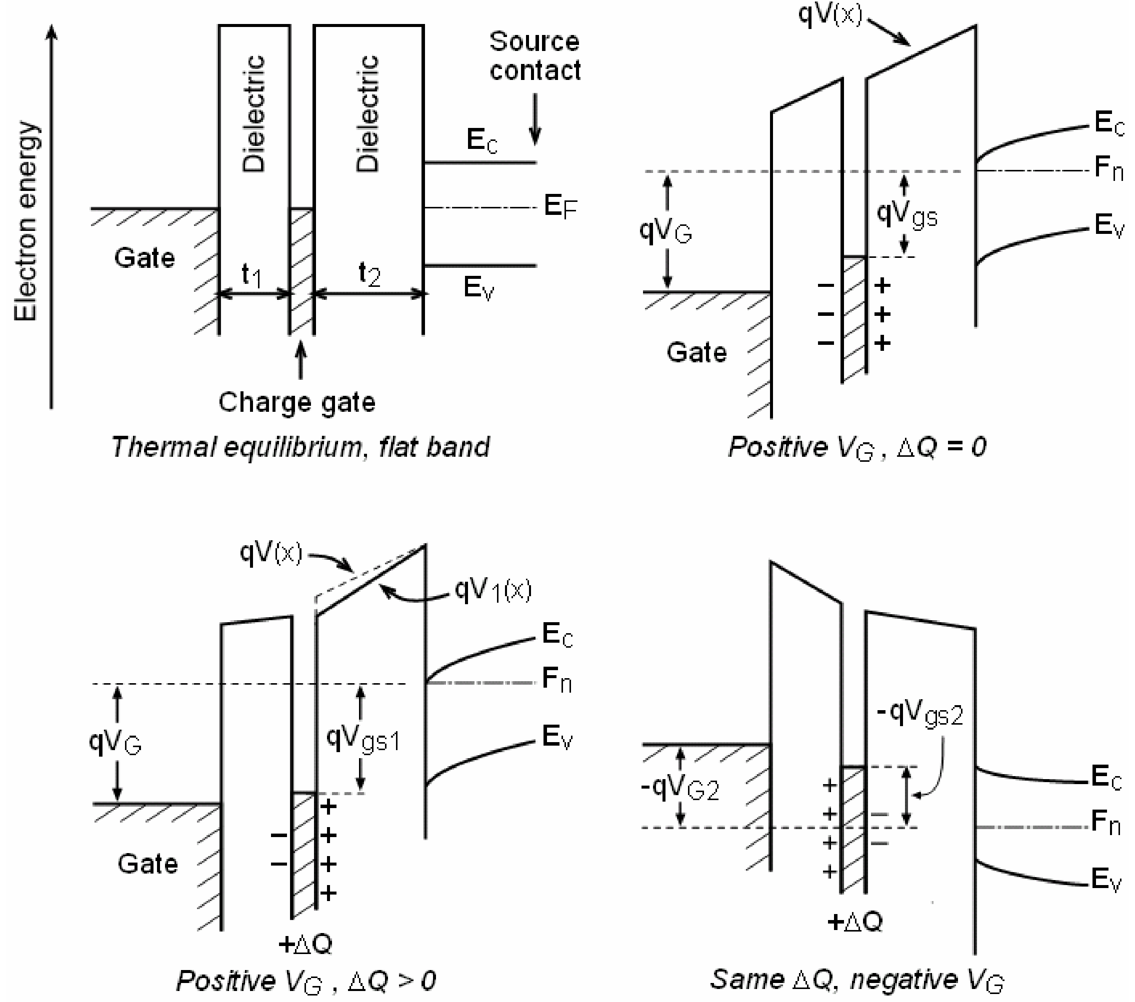


Fig. 3.2. Electronic band diagrams of a CG-TFT under different bias conditions (flat band, positive VG, positive VG with deposited charge, ΔQ on the charge gate, negative VG with ΔQ on charge gate).

$$\Delta V_{gs} = \frac{\Delta Q}{C_g + C_c} \tag{3.2}$$

Putting Eqn. 3.1 and Eqn. 3.2 together to obtain V_{gs} as a function of gate voltage and deposited charge, the transistor current in the linear mode is expressed as follows:

$$I_{D\,Lin} = \mu_{FE} C_0 \frac{W}{L_g}\left(\frac{C_g V_G + \Delta Q}{C_g + C_c} - V_t - \frac{V_{DS}}{2}\right)V_{DS}\,. \tag{3.3}$$

Here, V_t is the TFT threshold voltage and V_{DS} is the drain source bias. The drain current in saturation mode would be:

$$I_{D\,Sat} = \mu_{FE} C_0 \frac{W}{2L_g}\left(\frac{C_g V_G + \Delta Q}{C_g + C_c} - V_t\right)^2. \tag{3.4}$$

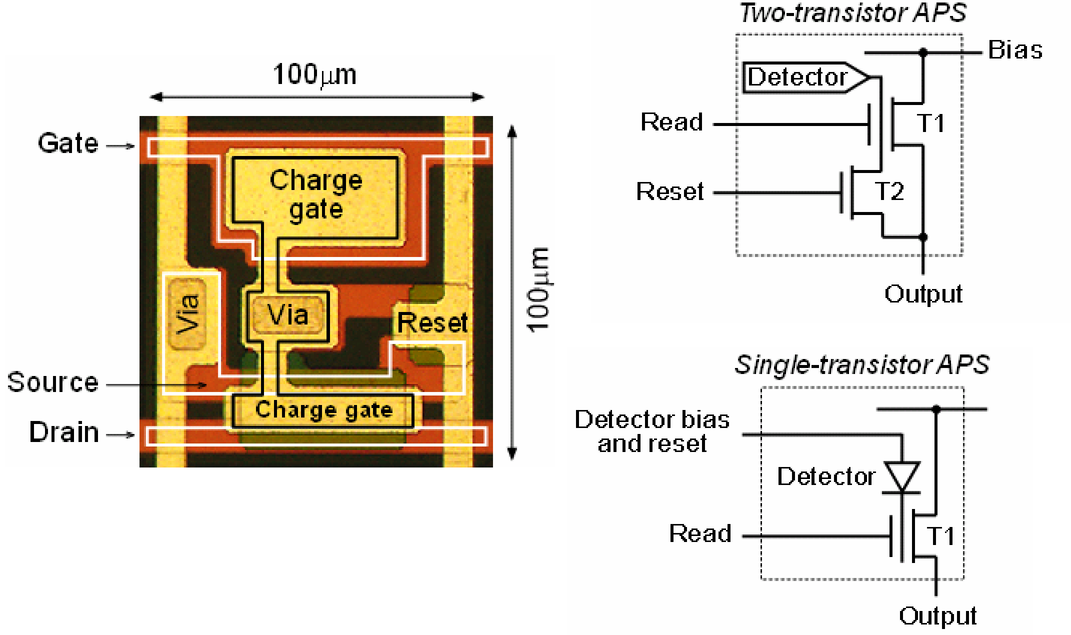


Fig. 3.3. 2T-APS die micrograph and circuit diagrams for 2T and 1T high resolution active pixel sensor (APS) circuits using an amorphous silicon CG-TFT. For clarity, the TFT drain, source, and gate terminals are outlined in white on the micrograph, and the charge gate is outlined in black.

3.1.3 Experimental results and discussion

Coplanar charge-gated a-Si TFTs shown in Fig 3.1 were fabricated using a four-mask double dielectric top-gate fabrication process using an in-house TFT fabrication facility. A die micrograph of the fabricated 2T APS structure is shown in Fig. 3.3. The voltage on the charge gate is reset via the *Reset* TFT (see. Fig 3.3) in order to discharge the deposited charge from a low leakage current photoconductor such as a-Se after the sensor value is readout. When the *Reset* TFT is turned ON, it discharges the charge gate to the grounded source, i.e., it resets the charge gate voltage to zero. Similarly, the charge gate can be reset to a non-zero voltage. However, during detector integration and charge deposition, the *Reset* TFT is kept OFF to keep the charge gate floating. It is important to note that if photodiode detectors are used, the sensing node, i.e., the charge gate, can be reset by forward biasing the photodiode. Here, the need for a reset TFT is eliminated and thus, a single-transistor (1T-APS) circuit can be realized (Fig. 3.3) using either *pin* or MIS photodiodes.

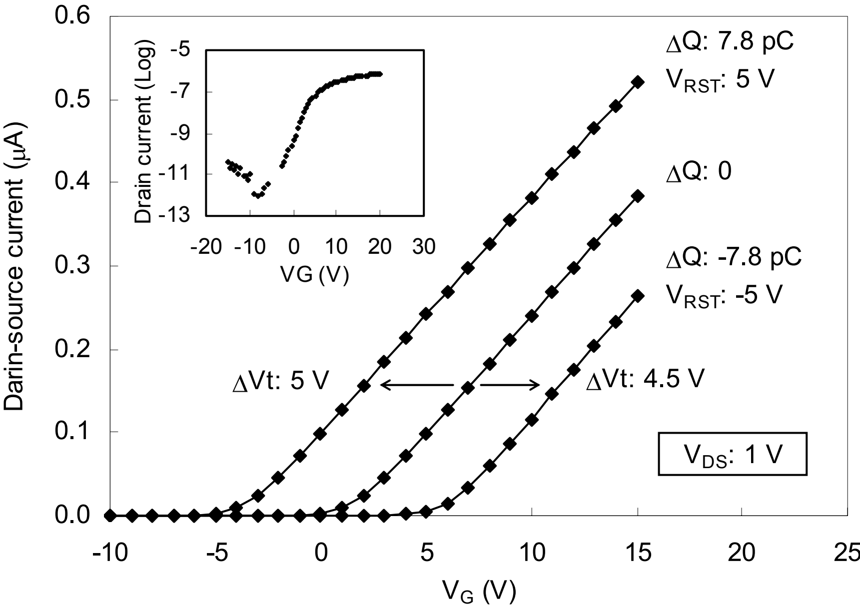


Fig. 3.4. Measured transfer characteristics of charge-gated TFTs test structure with W/L of 5, and the output characteristics of the two-transistor APS circuit of Fig. 3.3.

The measured transfer characteristics for different reset voltages of a test CG-TFT with W/L = 5, L_g = 10 µm, C_g = 1.35 pF and C_c = 0.22 pF are shown in Fig. 3.4. Here, the deposited charge on the charge gate strongly modulates the threshold voltage of the device, and therefore the output current. Calculated values from Eqn. 3.3 are within 15% of the measured values for $\Delta Q = 0$. The reset voltage, V_{RST}, was changed between +/- 5 V to obtain +/- 7.8 pC of charge on the charge gate as shown in Fig. 3.3. In practice however, there are voltage drops across the reset TFT drain and source contacts which result in a smaller reset voltage appearing on the charge gate. The shift in V_t is calculated from Eqn. 3.3:

$$\Delta V_t = \frac{\Delta Q}{C_g + C_c} \times \frac{C_g + C_c}{C_g} = \frac{\Delta Q}{C_g} \tag{3.5}$$

The term $(C_g + C_c)/C_g$ appears in Eqn. 3.5 because the shift in V_t is read on the V_G axis in Fig. 3.4 with V_G being scaled by $C_g/(C_g + C_c)$ in Eqn. 3.3. The change in V_t can also be expressed in term of the reset voltage if $\Delta Q/(C_g + C_c)$ is substitute by its equivalent value, V_{RST}, i.e.

$$\Delta V_t = V_{RST} \frac{C_g + C_c}{C_g} \tag{3.6}$$

Eqn. 3.6 suggests equal threshold voltage shift of 5.8 V for a resetting voltage of +/-5 V. However values of 5 V and 4.5 V are measured as shown in Fig. 3.4.a. Knowing the capacitance ratio and the measured shift in V_t, the actual value of charge gate reset voltage is extracted from Eqn. 3.6 to be 4.3 V and -3.9 V for V_{RST} equal to 5V and -5V respectively. We attribute these differences to the voltage drops across the *Reset* TFT, incomplete resetting of the charge gate, and loss of charge due to leakage current. The operation of the CG-TFT is different from dual-gate or double-gate TFTs where the semiconductor is sandwiched between two gates and the channel is formed under one of the gates, i.e. the primary gate. In such devices the threshold voltage is weakly modulated by the secondary gate voltage with a proportionality factor of ~ 0.15 [9]. For charge-gated TFTs however, Eqn. 3.6 shows that the threshold voltage is modulated by the reset

voltage on the charge gate with a proportionality factor of grater than unity.

The output characteristics of the charge-gated TFT for the high resolution imaging pixel of Fig. 3.3 are also shown in Fig. 3.4 [7]. There a strong dependence of I_{DS} on the applied V_{DS}. This is due to feedthrough from the TFT drain to the charge gate via the overlap capacitance as V_{DS} is swept. The overlap capacitances should be minimized to reduce current modulation by drain-source voltage, however, this will not be a problem when the charge gated TFT is used in the common drain configuration, which is the case for most image sensor applications.

3.2 Novel Two-Transistor Pixel Architectures

3.2.1 Introduction

Active pixel sensor (APS) architectures for large area imaging applications using thin film transistors (TFTs) have received considerable attention in recent years [10-13] for their ability to provide high signal to noise ratio [14], or fast operating speed [15]. Due to its single switched transistor architecture, the single switch passive pixel sensor (PPS) [10] provides a compact solution for large area imaging using TFTs; however, its noise performance is inadequate for very low input signal applications such as real-time medical fluoroscopy, where the APS is a promising replacement. [14]. In addition, current mode APS pixel architectures have recently been shown to outperform the PPS in terms of imaging speed thus presenting new opportunities in high frame rate applications such as computed tomography [15].

Compared to the PPS pixel, amorphous silicon (a-Si) current mode APS architectures consists of three transistors that require a larger pixel area comparatively. For applications such as fluoroscopy where the pixel pitch is relatively large (150-200 μm), APS architectures are feasible since they meet the requirements of low noise performance, fast readout for real time imaging as well as pixel size. However, for mammography applications where high resolution images are necessary (pixel pitch of

50μm – 100μm), pixel size remains a challenge for APS architectures. Furthermore, emerging applications such as mammography tomosynthesis are becoming popular where multiple images are obtained from different viewing angles using a fraction of the allowable dose and time of regular 2D mammography to render a three dimensional image. The two-transistor (2T) APS was proposed as an alternative to the 3T APS to address the detector array resolution challenge while the simplicity of the architecture also provided improvements in electrical performance [15, 16]. Part of the results presented in this section were published at IEDM 2007 [7], the performance of different 2T APS architectures is discussed in detail in terms of pixel gain, noise and stability performance. Measured results from in-house fabricated 2T-APS test pixels are presented as well as driving schemes for minimizing the threshold voltage metastability problem and increasing frame rate.

3.2.2 Two-Transistor APS Architectures

3.2.2.1 Pixel architecture using a gate-switched amplifier

The 2T APS architecture using a gate-switched amplifier (Fig. 3.5.a) consists of a pixel detector, for example an amorphous selenium (a-Se) photoconductor that converts the incident radiation to electric charge, a resetting transistor, T_R, which is used to reset the detector node to a preset voltage, and an amplifying transistor, T_A, which drives the pixel output current based on the change in detector node voltage (at gate of T_A), and a capacitor, C_g, which serves as the pixel storage capacitor, as well as providing access to the gate of T_A to switch it ON and OFF [16]. Here, T_A is a switched amplifier integrating the functions of both the amplifier TFT (T_A) and the series connected switch TFT (T_S) of the standard APS architecture (Fig. 3.5.d). Similar to the previously reported 3T APS architecture [3], the 2T APS operates in *Resetting*, *Integration* and *Readout* modes as shown in Table 3.1.

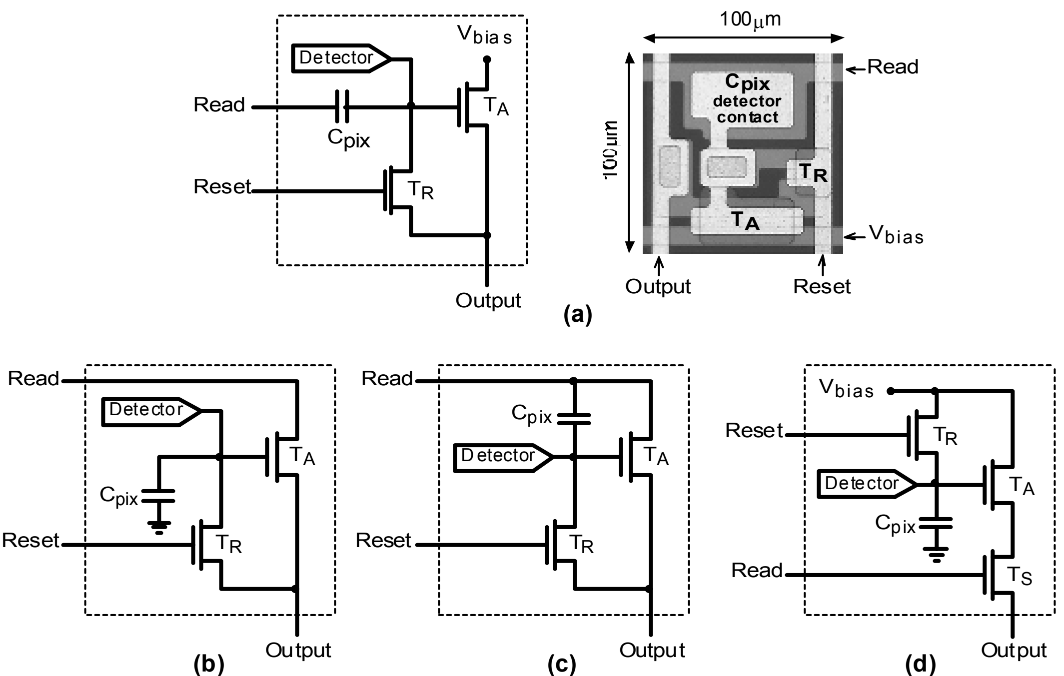


Fig. 3.5. (a) Two-transistor APS architecture and its die micrograph using gate-switched amplifier [7]. (b) Two-transistor APS architecture using source switching (c) Two-transistor APS architecture using drain switching [15]. (d) The standard three-transistor APS architecture [2].

Table 3.1. Status of transistors and Driving signals for operation of the 2T APS of (Fig. 3.5.a, gate-switched amplifier) in different modes.

	Resetting	*Integration*	*Readout*
Read			
Reset			
Output	0	0	0 (I_{out})
T_A-T_R	OFF-ON	OFF-OFF	ON-OFF

In *Resetting* mode, when T_R is turned on the detector node voltage is set to zero by discharging it to the grounded output; T_A is turned OFF. During the *Integration* mode the preset voltage of the detector node is modulated by the charge generated in the detector as the result of radiation absorption; both T_A and T_R are in OFF state. When T_R is OFF, because of the extremely high resistance photoconductor detector, the detector node is effectively floating [17]. This makes it possible to read the pixel value by applying a

voltage pulse to the pixel capacitor which consequently increases the gate-source voltage of T_A, $V_{GS\ TA}$, beyond its threshold voltage while preserving the charge on its gate [16], which provides non-destructive readout capability. Figure 3.6 shows the non-destructive readout, and long-time charge holding capability of the 2T APS pixel.

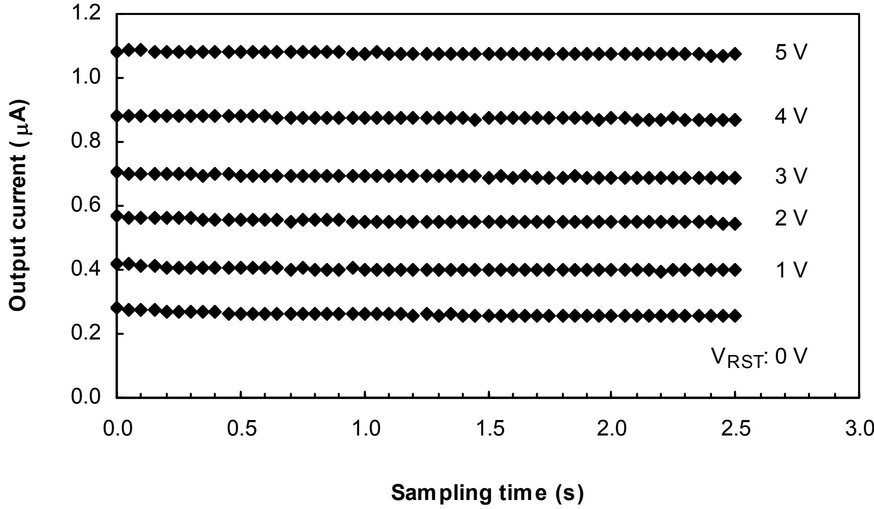


Fig. 3.6. Successive readout of the 2T APS for different values of detector node preset voltage, V_{RST}, at the rate of 20 samples per second.

Eqn. 1 describes $V_{GS\ TA}$ in the readout mode. As shown in Fig. 3.5.a, V_{READ} is the amplitude of the read voltage pulse, C_{gs} is the gate-source capacitance of T_A, and C_{eff} represents the total detector node capacitance, i.e., gate capacitance of T_A (including gate-drain and gate-source overlaps), detector capacitance, drain-gate capacitance of T_R, and the storage capacitance C_{pix}. Because other capacitances are small, $C_{eff} \sim C_{pix} + C_{gs}$. ΔQ, which is usually selected to be negative by proper choice of detector biasing voltage [18], is the detector deposited charge.

$$V_{GS\ TA} = V_{READ} \frac{C_{pix}}{C_{eff}} + \frac{\Delta Q}{C_{eff}}. \qquad (3.7)$$

Depending on the level of bias voltage, V_{bias}, and the amplitude of the read voltage, T_A is biased in linear or saturation mode and drain current, modulated by ΔQ, flows to the output line for further processing. Fig. 3.6 shows the transfer characteristics of a test 2T

APS (ΔQ = 0) biased in linear and saturation modes as a function of the V_{READ} and V_{bias} voltages. When the pixel is reset with non zero voltage, charge is deposited on the pixel capacitance and the second term of Eqn. 3.7 appears as a shift in threshold voltage (Fig. 3.6.b) which strongly modulates the output current as described by Eqn. 3.8 [17]. Bearing in mind that the field effect mobility is bias dependent, and the effective gate-source voltage must be calculated based on the voltage drop due to the source contact resistance, we can use MOSFET model level 1 to approximate the drain current as:

$$I_{out} = I_{D-TA} = K_A \left(\frac{C_{pix}}{C_{eff}} V_{READ} + \frac{\Delta Q}{C_{eff}} - V_t - \frac{V_{bias}}{2} \right) \cdot V_{bias} \,. \tag{3.8}$$

The above equation describes the pixel output current, I_{out}, when transistor T_A is biased in linear mode. K_A is the gain factor of T_A, or the product of the field effect mobility, μ_{FE}, gate capacitance per unit are, C_0, and aspect ratio of T_A, W_A/L_A, and V_t is the threshold voltage. Alternately, when V_{bias} is high to bias T_A in saturation mode, the output current is described as:

$$I_{out} = \frac{K_A}{2} \left(\frac{C_{pix}}{C_{eff}} V_{READ} + \frac{\Delta Q}{C_{eff}} - V_t \right)^2 . \tag{3.9}$$

Figures 3.6 and 3.7 show the output current, I_{out}, for different values of V_{read} and V_{Bias}, indicating that TA in the 2T APS can be biased in both linear and saturation modes. epending on the type of column amplifier used, the APS circuits can be read in terms of voltage when voltage buffers/amplifiers are used [19], or in terms of current when current integrators [12] or transimpedance amplifiers are used.

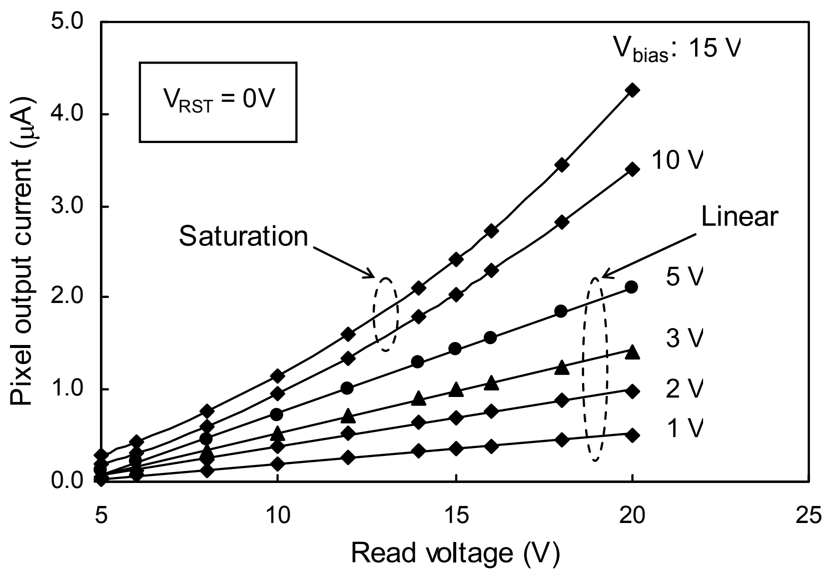


Fig. 3.6. Measured transfer characteristics of the 2T APS test circuit.

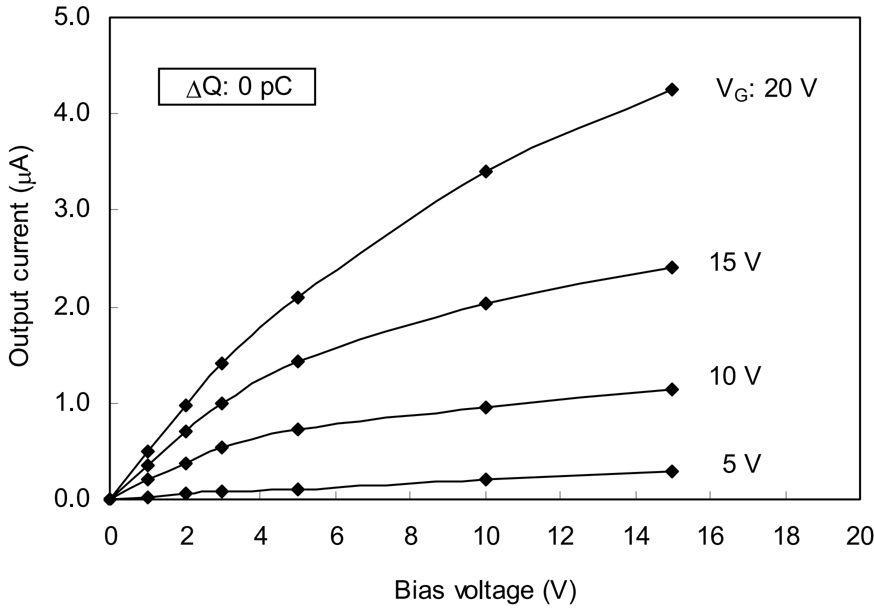


Fig. 3.7. Output current of a 2T-APS against V_{Bias} voltage for different values of V_{read}.

3.2.2.2 2T-APS using a source-switching

Another possible approach to obtain a 2T APS architecture is to relocate the row-select or addressing switch transistor (Ts) of a traditional 3T APS pixel from within the pixel to the common row line and address the pixel by switching the drain or source bias voltage of the T_A [14, 15]. In a 3T APS, when the pixel is addressed, T_S connects the source of T_A to the output (Fig. 3.5.d). In the 2T APS however (Fig. 3.5.c), both source and drain terminals of T_A are directly accessible, making it possible to use one terminal as the addressing line and the other for the output.

Table 3.2. Status of transistors and driving signals for operation of the 2T APS using source switching.

	Resetting	*Integration*	*Readout*
Read			
Reset			
Output	High	High	High (I_{out})
T_A-T_R	OFF-ON	OFF-OFF	ON-OFF

When the source of T_A is used for addressing, the drain (output) is kept at a constant positive bias voltage (Table 3.2). The pixel is reset when T_R is turned on and the detector node voltage is reset to a positive voltage namely, V_{RST}, by the output (the drain) voltage, V_{bias}. During *Integration* when deposited charge from detector modulates the voltage of the detector node, T_A is OFF because its drain and source are both at positive V_{bias}, resulting in gate-source or gate-drain voltages of T_A to be either zero or negative depending on the level of V_{RST}. For *Readout*, the source voltage is grounded resulting in positive $V_{GS\,TA}$ across the gate-source of T_A that switches T_A ON and the output current is read from the drain terminal. It is important to note that C_{pix} plays a vital role in proper operation of the pixel. Because the gate of T_A is effectively floating during *Readout*, reducing the source voltage of T_A from V_{bias} to zero results a voltage drop of $V_{bias} \cdot C_{gs} / C_{eff}$ on its gate.

$$V_{GS\ TA} = V_{RST} - \frac{C_{gs}}{C_{eff}} V_{bias} \tag{3.10}$$

Similar to Eqn. 3.7, C_{eff} is the total detector node pixel capacitance observed at the gate of T_A, and C_{gs} is the gate source capacitance of T_A. If detector capacitance is small and no physical pixel storage capacitance is used, C_{eff} would be effectively equal to C_{gs} which makes it practically impossible to switch T_A ON by reducing its source voltage when its gate is floating since the gate voltage follows that of the source. This is particularly important in small pitch pixels with a-Se detectors, where the detector capacitance is negligibly small. Equation 3.10 indicates that for the best case when the pixel is reset up to V_{bias}, i.e., $V_{RST} = V_{bias}$, C_{eff} must be sufficiently larger than the gate source capacitance of T_A to have positive gate source voltage on T_A during *Readout*, which requires a large space consuming physical storage capacitor, C_{pix}.

3.2.2.3 2T-APS using a drain switching

The architecture of 2T APS using drain voltage switching is shown in Fig. 3.5.c, where the pixel storage capacitance is connected between the detector node and drain of T_A. C_{pix} can be implemented via an extension of gate-drain overlap of T_A, and acts as the storage capacitance during *Reset* and *Integration* when drain is grounded as well as providing bias voltage for the gate of T_A during *Readout* when *Read* voltage (drain voltage of T_A) increases from zero to V_{READ}. In fact, this architecture is similar to that of the gate-switched amplifier of Fig. 3.5.a where the pixel bias voltage is connected to *Read* to reduce the number lines per pixel from 4 to just 3. The driving signals are similar to those displayed in Table 3.1. In the *Resetting* mode the detector node voltage is reset to zero by switching T_R ON, connecting the detector node to grounded output. During *Integration* mode T_A would be OFF because same as the case for switched amplifier design, which prevents T_A from experiencing threshold voltage shift during the long integration time. For *Readout*, the read voltage applied to the drain of T_A is increased from zero to V_{READ}, resulting in a positive gate-source voltage and the output current respectively described by Eqn 3.7 and Eqn 3.9. Unlike the switched amplifier architecture of Fig. 3.5.a that can

be biased in both linear and saturation modes, the drain switched architecture is only biased in saturation due to the fact that gate voltage of T_A is always less than its drain voltage.

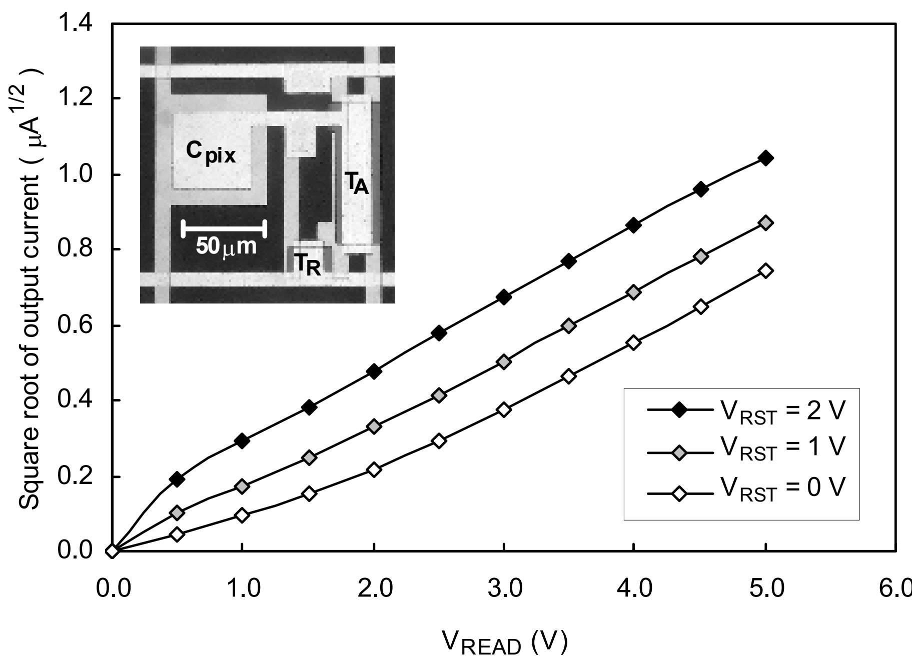


Fig. 3.8 Measured transfer characteristics of 2T APS using drain switching. The inset is the micrograph of the 2T pixel used for this measurement; the *Read* and V_{bias} lines were externally connected.

Fig. 3.8 shows square root of output current of drain switched 2T APS pixel versus *Read* voltage for different reset voltages. Straight lines clearly indicate T_A is biased in saturation mode. However, as mentioned above, this architecture has only three lines per pixel, akin to the PPS, which is the fewest among the architectures reported in this paper.

Other driving scheme of the drain-switched 2T APS are also possible [16], however, both drain switched or source switched 2T APS require different driving circuits compared to standard 3T APS. It is worth noting that the 2T APS using gate-switched amplifier uses the same driving scheme of the traditional APS, i.e. the addressing signal is applied to a capacitive gate. On the other hand, in the drain/source switching 2T APS architectures the addressing pulse is applied to the conductive drain or source terminals that carry large

currents, thus gate drivers currently employed for display and imaging arrays cannot be used for the drain/source switching pixel architectures. A 2400 column imager for example, with a nominal pixel output current of 2μA, requires drivers capable of switching ~3 mA of current per channel.

3.2.2.4 Hybrid architectures versus high speed imaging

In all 2T APS architectures of Fig. 3.5, connecting T_R between the detector node and the output provides PPS operation, i.e. direct readout of the pixel stored charge. While the APS provides on-pixel signal amplification to improve noise performance in low input signal mode, PPS performance is satisfactory when input signal is high. In contrast to the high linearity of the PPS output, the nonlinear behavior of APS becomes an issue in the case of large input signals. Four and three-transistor hybrid architectures based on 3T APS have been proposed to address this problem [20] at the cost of an additional transistor to connect the detector node to the output. While the 2T APS pixel architectures are inherently hybrid, disconnecting T_R from output (Fig. 3.9) and providing an independent reset enables *Readout* and *Resetting* operations independent of each other to increase imaging speed at the cost of one additional line per pixel [14].

For example, the charge gain of 12 drops to 3 if the readout time is decreased by a factor of four, from 30μs to 7.5μs. Now, instead of resetting each row for 30μs, 4 rows are simultaneously reset for only 7.5μs [7]. The whole resetting window and the row being read, sweep the array one row at a time, each 7.5μs, which results in four fold higher readout frame rate, while it ensures each row is reset for a combined time of 30μs for proper operation of the imager.

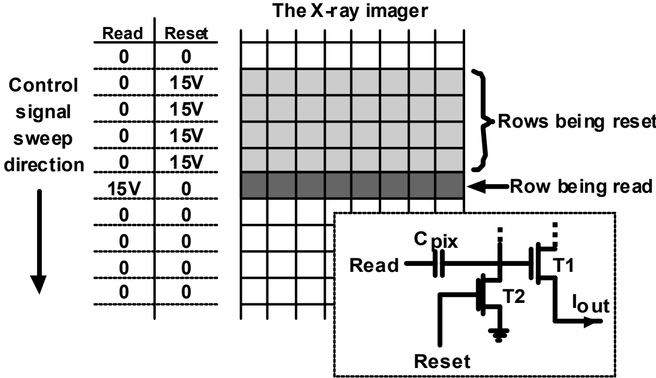


Fig. 3.9. Higher frame rates are obtained by shortening the readout time and multiple row resetting. This technique is possible only is a separate resetting voltage is provided at the source of T2 (same as T_R in Fig. 3.5).

3.2.3 Pixel Transconductance Gain

On-pixel pre-amplification of the signal provided by APS improves signal to noise ratio (SNR) [13] and potentially enhances imaging speed [14]. One advantage of the 2T APS architectures over the previously reported 3T APS [11] is the increase in pixel gain due to removing the series connected T_S from the source of T_A (Fig. 3.5.d). Defining V_G as the detector node (gate of T_A) voltage, and I_{out}, the output current, as the drain current of T_A the pixel transconductance gain, G_m, is defined as $\partial I_{out}/\partial V_G$ when V_G is set to its biasing voltage value, V_{RST}. For 2T APS (Fig. 3.5.a or 3.5.c), G_m is the transconductance of a single transistor T_A. In order to arrive at closed form results for comparison we use level 1 MOSFET model for calculations. g_m of T_A when biased in saturation mode is calculated as:

$$g_{m-TA} = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial I_{out}}{\partial V_G} = G_{m-2T} = K_A \left(V_{RST} - V_t\right). \tag{3.11}$$

For the 3T APS, assuming T_S is biased in linear mode (T_A saturated) G_m would be [2]:

$$G_{m-3T} = \frac{1}{R_{ON}}\left(1 - \frac{1}{\sqrt{1+2K_A R_{ON}\left(V_{RST} - V_t\right)}}\right). \qquad (3.12)$$

in which R_{ON} is the ON state resistance of T_S and K_S is the gain factor of T_S. Replacing $1/R_{ON}$ with K_S $(V_{READD} - V_t)$ or channel conductance of the transistor T_S biased in linear mode, G_m becomes:

$$G_{m-3T} = K_S\left(V_{READ} - V_t\right)\left[1 - \left(1 + 2\frac{K_A\left(V_{RST} - V_t\right)}{K_S\left(V_{READ} - V_t\right)}\right)^{-1/2}\right]. \qquad (3.13)$$

Equation 3.13 shows that the pixel gain of 3T APS is basically governed by the linearly biased T_S rather than T_A which is biased in saturation mode. Moreover, the last term of Eqn. 3.7 in brackets further reduces $G_{m\text{-}3T}$ because of the feedback effect of R_{ON} [11]. For example, when $K_A = K_S$ and $V_{READ} = V_{RST}$, comparing Eqns. 3.10 and 3.12 results in:

$$G_{m-2T} \approx 2.4\,G_{m-3T} \qquad (3.14)$$

Fig. 3.10 compares pixel transconductance gain of a 2T and 3T a-Si APS pixel circuits with $K_A = K_S = 0.045$ µA/V, and aspect ratio of 100µm/10µm. At $V_{RST} - V_t = 10$V when V_{READ} is equal to V_{RST}, $G_{m\text{-}2T}$ is almost 3 times $G_{m\text{-}3T}$ which is close to the value predicted by Eqn. 3.14.

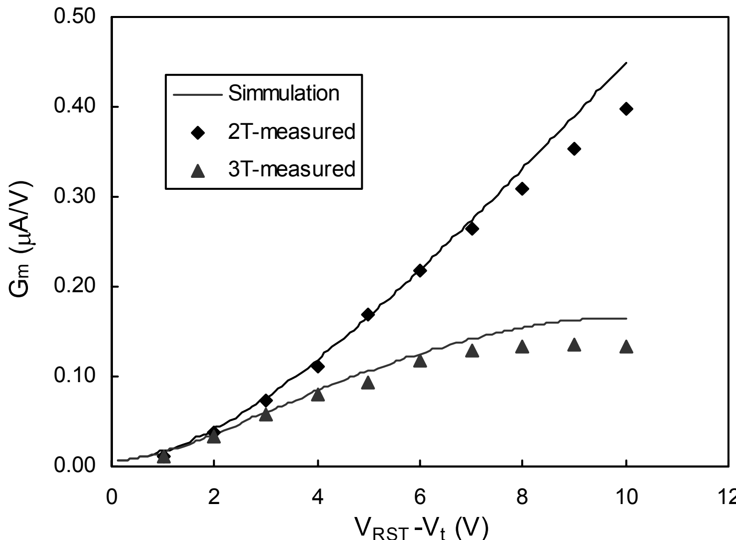


Fig. 3.10. Comparison of pixel transconductance gain of 2T and 3T a-Si test APS circuits.

As mentioned earlier, R_{ON} acts as a degenerate feedback resistor at the source of T_A, damping any nonuniformity or variations in characteristics of T_A such as changes in μ_{FE} or V_t, resulting from fabrication or long term drift. However, because R_{ON} is implemented using T_S, some of the compensation benefit is lost due to variations in T_S. Eqn. 3.12 shows that variations in T_S are reflected in the pixel transconductance gain of the 3T APS, G_{m-3T}. In contrast, 2T APS architectures can mitigate this concern by apply external feedback to TA via an external resistor placed in the output of each column at the input of the output column amplifier. Providing such feedback is necessary to improve uniformity in pixel performance at the cost of reduced gain.

In order to increase pixel gain, K_A is made large by increasing the aspect ratio of T_A in 2T APS as indicated in Eqn. 3.11. For the 3T APS, if K_S is made much larger than K_A, Eqn. 3.13 reduces to Eqn. 3.11. On the other hand, G_{m-3T} in Eqn. 3.13 approaches $K_S.(V_{READ} - V_t)$ if $K_A >> K_S$. In either case, the pixel gain of the 3T APS is actually limited to the smaller g_m if the aspect ratio of one transistor is much larger than that of the other. In other word, both K_A and K_S should be made large to increase pixel gain of 3T APS which is in accordance with presented experimental data previously by Siemens [12]. This

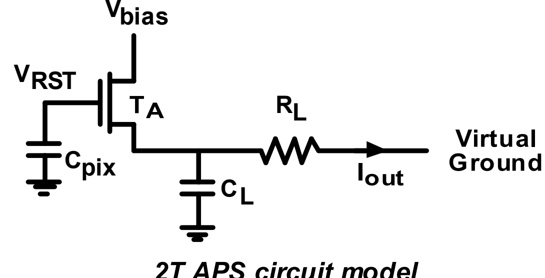
highlights an advantage of the 2T APS for high resolution imaging where, if the pixel area is small, it is challenging to implement two large aspect ratio transistors for high gain, as is necessary for the 3T APS architecture.

3.2.4 Noise Performance of 2T-APS

In order to evaluate the noise performance of the 2T APS we consider the circuit diagrams of Fig. 3.11, which show a general 2T APS pixel during readout, (T_R is off, and not considered) and calculate the total input referred noise by considering three major noise sources: flicker, reset and thermal noise [21]. The input referred noise is defined as the output referred noise divided by the DC gain, and is calculated in order to be compared with the quantum noise associated with the input signal [11]. In this work, we only consider the imaging pixel in our noise calculations. However, this does not affect the overall analysis since it was previously shown that off-pixel noise sources, such as data line thermal noise or column amplifier (charge amplifier or transimpedance amplifier) noise, have a small contribution on the total input referred noise for current mode APS circuits with charge gain [21].

In Fig. 3.10, I_{nA} represents the flicker and thermal noise current components of T_A. The data line is modeled by a single resistor, R_L and a single capacitor, C_L which their values are selected in such a way to limit the bandwidth to 1 MHz. Using small signal analysis, the transfer function that maps I_{nA} to the output, H_I, is calculate as:

$$H_I(s) = \frac{I_{out}}{I_{nA}} = \frac{1}{1+sC_L R_L}\left(1+\frac{g_{mA}R_L}{1+sC_L R_L}\frac{C_{pix}}{C_{pix}+C_{gs}}\right)^{-1}. \tag{3.15}$$



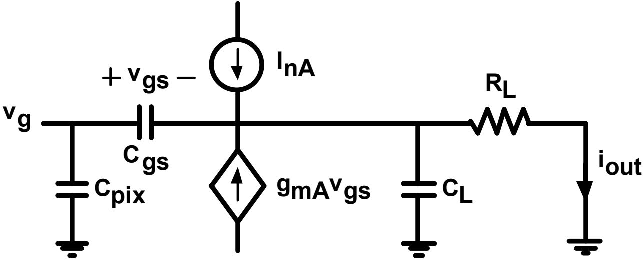


Fig. 3.11. Circuit model and small signal circuit of the 2T APS for noise calculations.

With the output of the pixel to be I_{out}, and the input as detector deposited charge, ΔQ, the DC gain of the pixel, G_i, is calculated in Eqn. 3.16 [11].

$$G_i = \frac{\Delta I_{out}}{\Delta Q} = \frac{g_{mA}}{1 + g_{mA} R_L} \frac{1}{C_{eff}} \approx \frac{G_{m2T}}{C_{eff}} . \tag{3.16}$$

With upper limit of g_{mA} being in the order of 10^{-6} V/A and R_L in the order of 10^3 Ω, the product of $g_{mA}.R_L$ would be more than 3 order of magnitudes smaller than 1 which makes the approximation of Eqn. 3.16 valid, and also results the last term of Eqn. 3.15 being effectively equal to unity. Flicker current noise component of T_A is calculated based on measured pixel current, extracted noise parameters from fabricated TFTs, and an already reported model [22, 23],

$$S_{1/f} = \frac{1}{f} \frac{\alpha_H \, q \, I_D^2}{(V_{GS} - V_t) C_0 WL} . \tag{3.17}$$

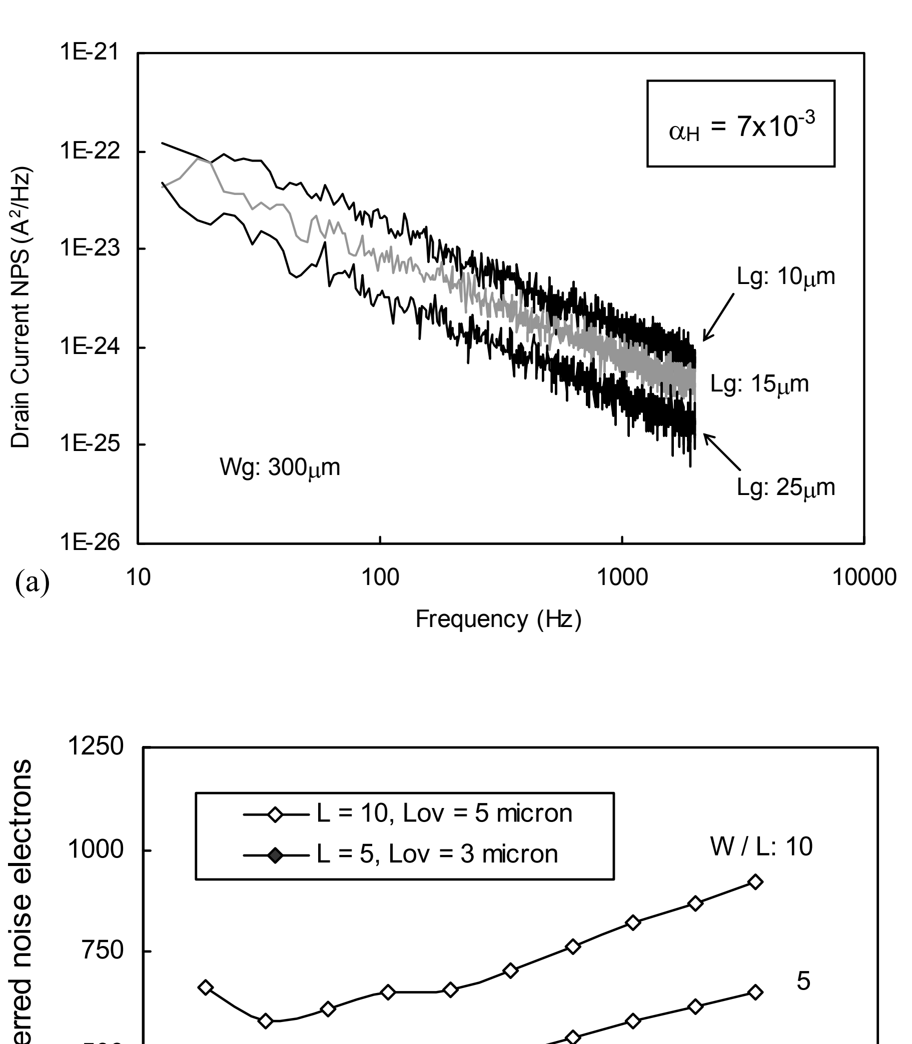


Fig. 3.12. (a): Extraction of α_H from measured drain current noise of fabricated TFTs. (b): Input referred noise of 2T APS architecture for different aspect ratios, gate length and gate overlap of T_A.

Here, q is the electronic charge and α_H, a technology dependent coefficient, is taken to be 0.01 for a-Si TFTs biased in saturation mode, and half of that for linear mode [23]. We verified the choice of 0.01 for α_H, by extracting α_H from measured drain current noise power spectrum (for different TFTs biased at different gate-source and drain source voltages) to be 0.7×10^{-3} for our in-house fabricated TFTs, but we decided to use an upper limit value of 0.01 which is most reported in the literature [23]. Thermal noise spectral current density of the a-Si TFTs is calculated via measured channel conductance [13]:

$$S_{th} = \beta 4kTg_{ds} . \tag{3.18}$$

Here, k is the Botzmann constant, T is the absolute temperature, g_{ds} is the channel conductance, and β is 1 for transistors biased in linear mode, or 2/3 for saturated transistors [22]. If TFTs are biased in saturation with a relatively large voltage across their drain source, the flicker noise dominates the noise current [22]. Due to the small g_{ds}, thermal noise does not contribute significantly to the input referred noise [21]. While this is the case for drain or source switched APS architectures (Fig. 3.5.b and c) that are always biased in saturation during readout, we included thermal noise into our calculations to evaluate the noise performance of 2T APS pixel with gate switched amplifier (Fig 3.5.a) where T_A is biased in linear mode and the flicker noise is reduced as noted earlier. The reset noise voltage of the imaging pixel at the detector node is given by Eqn. 3.19 [11] and it appears as DC noise voltage at the gate of T_A with a transfer function of G_{m-2T},

$$V_{n\ RST}^2 = kT / C_{eff} . \tag{3.19}$$

Eqn. 3.20 describes the input referred noise in terms of number of electrons where q, the electronic charge, converts the charge noise into number of electrons, and T_S, the readout time, has been incorporated to avoid the singularity of integrating 1/f at zero frequency for the flicker noise calculation [24].

$$Input\ referred\ noise = \frac{\sqrt{G_m^2 \cdot V_{n\ RST}^2 + \int_{1/Ts}^{\infty} S_{1/f} \left| H_I \right|^2 df + \int_0^{\infty} S_{th} \left| H_I \right|^2 df}}{q \cdot G_i}. \tag{3.20}$$

For all calculations we took T_S equal to 10 μs, which corresponds to 100 frames per second readout rate for an imager having 1000 rows [14], and the storage capacitance, C_{pix}, was taken to be half the value of the gate source capacitance of T_A. This allows keeping both C_{eff} and the voltage drop across gate source in Eqn. 3.7 at a low level. Fig. 3.12 shows the total input referred noise of the 2T APS versus the effective read voltage that appears across the gate source of T_A, for different aspect ratios and gate length of T_A. As can be seen, for TFTs with gate length of 10 μm, and a gate-source overlap of 5 μm (shown as white diamonds in Fig 3.12) the input referred noise decreases as the transistor width is decreased from 100μm (W/L = 10) to 25μm (W/L = 2.5) which is due to reduction of C_{eff}. Calculations show that for TFTs with W = 25 μm if gate length is reduced from 10 μm to 5 μm from 10 μm but keeping the gate source overlap as 5μm, the input referred noise does not noticeably change despite the fact that G_m increases as the result of doubling the aspect ratio. However, reducing the gate-source overlap from 5 μm to 3 μm results in considerable enhancement in the input referred noise (shown as black diamonds in Fig. 3.12), again, because of lower C_{eff}. Thus, the 2T APS is compatible with high resolution imaging applications where scaling down the pixel size improves noise performance.

For $V_{GS} - V_t$ between 2 to 4 V, the calculated input referred noise was between 222 to 251 noise electrons for typical W/L of 25μm/5μm and a gate overlap of 3 μm, which could be well accommodated in a 50μm × 50 μm pixel size. For the minimum value of 222 total input referred noise, the contribution of flicker and reset noise were 205 and 85 noise electrons, respectively, with negligible contribution of thermal noise. Even for the large size TFTs with W/L of 100μm/10μm and gate overlap of 5μm, the minimum input referred noise is 585 noise electrons, which is well below the 1000 quantum noise level for real-time digital medical fluoroscopy [11, 21]. For this configuration, C_{eff} is about 330 fF, and detector capacitance is 2.5 fF (for a 150μm × 150 μm pixel size, and 500μm thick

a-Se, $\varepsilon_{a\text{-}Se}$ = 6.3) where again, the pixel capacitance is dominated by the gate capacitance of T_A and C_{pix}, the pixel storage capacitance.

3.2.5 Metastability

The drift in threshold voltage of biased or relaxed a-Si TFTs is one of the major metastability issues of a-Si devices, which is mainly caused by charge trapping/detrapping in the silicon nitride gate dielectric or via defect creation in a-Si [25]. When biased, the a-Si TFT V_t shift shows different behavior depending on the polarity of gate bias voltage (stress voltage), as well as its frequency and duty cycle [26]. When pulse biased, the duty cycle of the stress voltage pulse reduces the effective stress time, hence, decreasing the V_t shift. While for positive stress voltages the VT shift depends on effective stress time, and not the pulse width, the negative V_t shift resulted from negative pulse bias is highly depended on the gate bias pulse width [26]. Minimizing the duty cycle and applying alternating positive and negative stress voltages are the main technique to control the V_t shift of a-Si TFTs, for example in liquid crystal display applications (TFT-LCD). [26, 27]. The time variation of V_t shift for an a-Si TFT, is described as the sum of positive V_t shift, $\Delta V_t^+(t)$, and negative V_t shift, $\Delta V_t^-(t)$, [26],

$$\Delta V_t^{\pm}(t) = \Delta V_t^+(t) + \Delta V_t^-(t). \tag{3.21}$$

$$\Delta V_t^+(t) = A^+ \frac{Q_G}{Q_{G0}} \left(V_{GS} - V_{ti}\right)^{\alpha+} \left(t \cdot DC\right)^{\beta+}. \tag{3.22}$$

$$\Delta V_t^-(t) = A^- \frac{Q_G}{Q_{G0}} \left(V_{ti} - V_{GS}\right)^{\alpha-} \left(t \cdot (1 - DC)\right)^{\beta-} \cdot F_{PW}. \tag{3.23}$$

Here, A, α and β are model parameters that we extracted from our fabricated TFTs separately for positive and negative stress voltages (Table 3.3), V_{ti} is the initial threshold voltage, t, the operating time, DC, pulse duty cycle, and F_{PW} is the pulse width factor for negative V_t shift as mentioned above [26]. We also consider the effect of drain bias on V_t shift by introducing the Q_G/Q_{G0} term in Eqns. 3.22 and 3.23, which is the ratio of channel charge at the biased drain-source voltage to the maximum channel charge when the drain-source voltage is zero [28].

To compare the stability of different 2T APS architectures under prolonged operation time, we calculated the V_t shift of T_A for 2T APS architectures of Fig. 3.5 at different biasing conditions of TFTs and projected the variations in the pixel transconductance gain of each APS architecture respectively. As the stressing voltages are the same for drain or source switched architectures (Fig. 3.5.b and c), there would be no difference in their long term stability performance. For 2T APS using gate switched amplifier however (Fig. 3.5.a), the drain is always biased, at V_{bias}, and gate voltage of T_A is set independently, which result in different long term stability behavior. Considering a 1000 row imager operating in real time with 30 frames per second, the readout time and the frame time would be 33 μs and 33 ms respectively, resulting in a duty cycle of 0.001 [11]. Compared to 100 frames per second which was the case with noise analysis, we considered 30 frame per second for stability projection to worsen the stressing condition as the time when T_A experiences negative stress increased almost three folds from ~10 ms to ~33 ms [11]. As in G_m measurement and noise calculations, V_{bias}, is again taken to be 10 V, and Fig. 3.13 shows the V_t shift of T_A in different 2T APS architectures of Fig. 3.5 versus prolonged operating time.

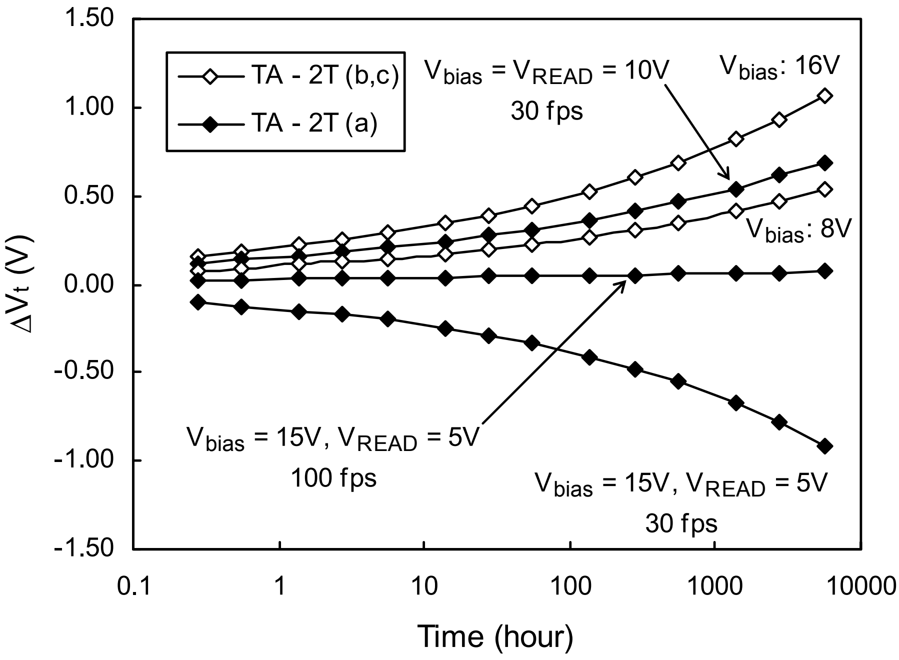


Fig. 3.13. Threshold voltage shift of T_A (for different 2T APS architectures of Fig 3.5) versus operating time for different biasing conditions and frame rate.

In Fig 3.13, for 2T(a) T_A is positively stressed during readout time and negatively stressed in integration which is 1000 times longer compared to very short readout time. The negative stress is caused by positive V_{bias} on drain and zero resetting voltage on the gate (output is grounded). The long negative stress time is responsible for negative V_t shift. However, the V_t shift is manageable by changing the bias voltage from 10 to 5 volts, which can balance the positive shift and virtually eliminates prolonged V_t. For 2T(b,c) however, because the drain-gate or source gate voltage is zero during integration, TA never experiences negative stress. The positive V_t shift is minimized by the very small duty cycle typical in medical imaging applications. Reducing bias voltage, reduces the positive stress voltage on the gate, and improves long term stability behavior. However, due to the fact that restoration of V_t shift during relaxation time has not been included, Eqn. 3.22 overestimates the actual V_t shift when only positive stress pulses are applied especially at very small duty cycles [26], which is the case for 2T APS studied here.

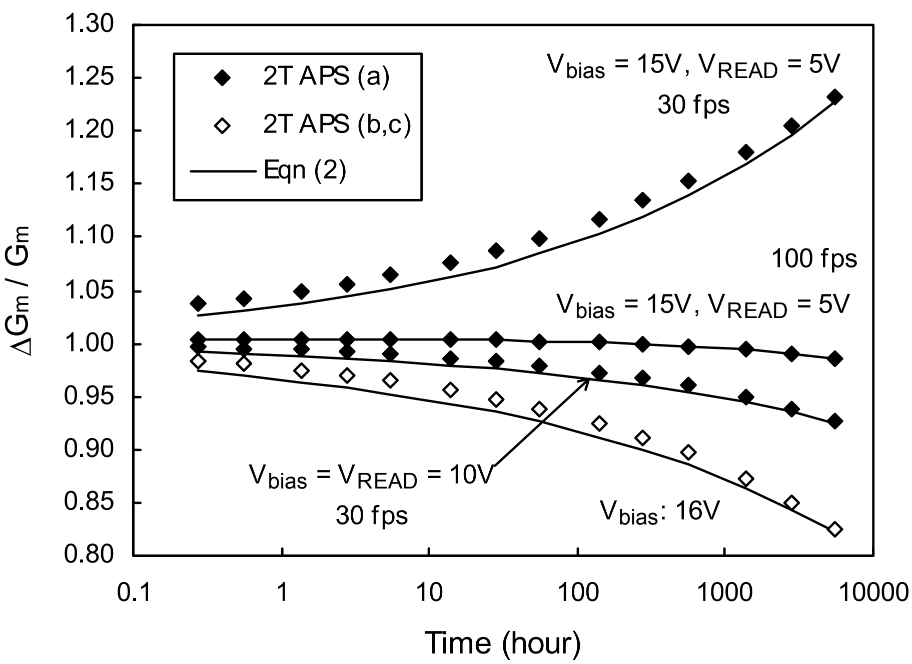


Fig. 3.14. Simulated variations of pixel transconductance gain, G_m, of different 2T APS architectures (see Fig. 3.5) over prolonged operating time for different biasing conditions and frame rate based on ΔV_t extracted from fabricated TFTs shown in Fig. 3.13. Solid lines are calculated from Eqn. (3.11).

Table 3.3. Extracted Model Parameters for V_t Shift calculations.

	Positive stress	*Negative stress*
A	9.37×10^{-3} *	-4.92×10^{-3} *
α	1	1.55
β	0.191	0.205
F_{PW} *(10 ms)*	-	0.2
F_{PW} *(33 ms)*	-	0. 5

* Time in minutes

It is noteworthy that for larger imagers, as is the case for mammography [13], the duty cycle becomes smaller which diminishes the effect of positive stress. More importantly, increasing the frame rate, which is the case for tomosynthesis, shrinks the integration time, i.e., the time when T_A is under negative stress which reduces F_{PW} [26] (Table 3.3),

hence the negative V_t shift. Therefore, Fig. 3.13 is considered to be a worst case scenario. The effect of V_t shift on pixel transconductance gain was studied for 2T APS architectures at V_{RST} = 10 V (Fig. 3.14). G_m is related to the threshold voltage shift simulated in Fig. 3.13 where the 2T APS (a) can be controlled to have a constant G_m over the prolonged operating time, while variations in the G_m of 2T APS (b,c) can be made small by design.

3.2.6 Transient Response

In this section performance of 2T APS and 3T APS are compared and contrasted. This study has been done based on circuit simulation of one pixel of an array. The TFT model has been extracted from fabricated TFTs (see chapter x, section y), and the effect of all other pixels have been included into the model by considering parasitic capacitances resulted from cross-over lines, and gate-drain/source overlaps, as well as including parasitic resistance of data and gate lines. Fig. 3.15 shows the circuit modes used, and Table 3.3 provides detailed calculations of the circuit parameters included into the model.

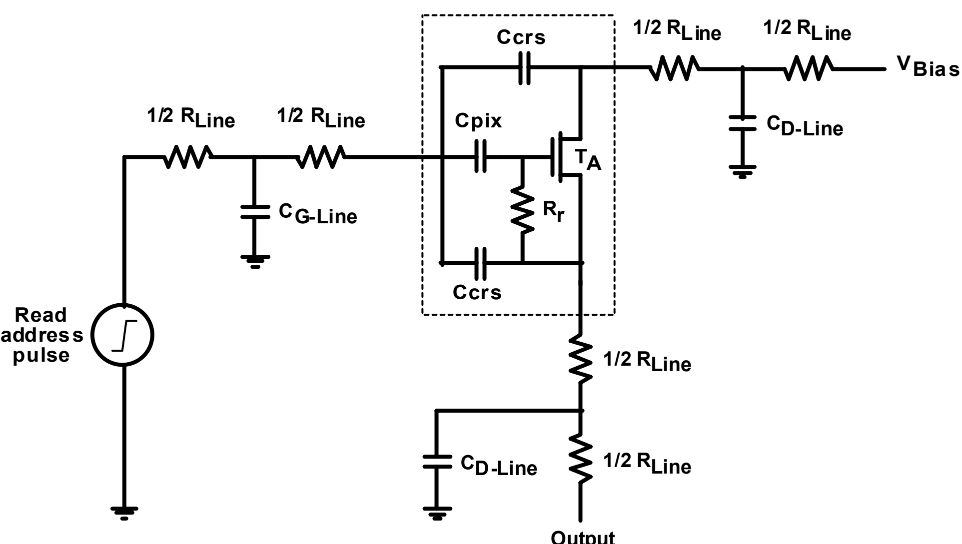


Figure 3.15. The circuit model for simulating 2T-APS array.

In the circuit model of Fig. 3.15, $C_{G\text{-}Line}$ and $C_{D\text{-}Line}$ are the parasitic capacitances of the gate line and data line respectively, and R_{Line} is the line resistance. Data line and gate line cross-over capacitance is C_{crs}, and R_r is the OFF state resistance of the reset transistor T_R. For both the 2T and 3T APS, CD-Line is calculated from:

$$C_{D-Line} = N\left(2C_{crs} + C_{GS-OV}\right). \tag{3.24}$$

Where N is the number of rows and $C_{GS\text{-}OV}$ is the gate-source overlap capacitance of T_A. Two cross-over capacitances have been considered because there are two gate lines, one for T_A (or T_S in 3T APS) and the other for T_R crossing over the data line. Based on 10μm line width, gate-source overlap of 2.5μm and 250nm silicon nitride dielectric (ε_r = 6.5), the data line parasitic capacitance of a 2000 row imager is calculated as:

$$C_{D-Line} = 2000 \times \left(2 \times 23.01\, fF + 57.53\, fF\right) = 207.09\, pF\,. \tag{3.25}$$

The gate line and data line resistance are calculated based on 10μm line width, 0.5μm thickness of aluminum with resistivity of $26.5\times10^{-7}\Omega$cm, for 150μm pixel pitch:

$$R_{Line} = 2000 \times \left(26.5 \times 10^{-7} \frac{150 \times 10^{-4}}{10 \times 10^{-4} \times 0.5 \times 10^{-4}}\right) = 1590\Omega\,. \tag{3.26}$$

Because 3T APS has one extra bias line compared to 2T APS, its gate line capacitance is different from that for the 2T architecture. For the 2T APS:

$$C_{G-Line-2T} = N\left(2C_{crs} + C_{pix} \,\|\, C_{G-TA}\right) = 441.38\, pF\,. \tag{3.27}$$

Here, C_{pix} considered to be 0.5 pF, and the gate capacitance of T_A, $C_{G\text{-}TA}$, been calculated to be 268.45 fF for a 100μm/10μm TFT biased in saturation mode. For the 3T APS, however, $C_{G\text{-}Line}$ is calculated from:

$$C_{G-Line-3T} = N\left(3C_{crs} + C_{G-TS}\right) = 828.36\, pF\,. \tag{3.28}$$

In which, $C_{G\text{-}TS}$ is calculated to be 345.15 fF for a 100μm/10μm TFT biased in linear mode.

For simulating C-APS (current mode), the pixel output node is virtually grounded and the output signal is taken to be current, while for V-APS (voltage mode), the output is left open, and output voltage is considered.

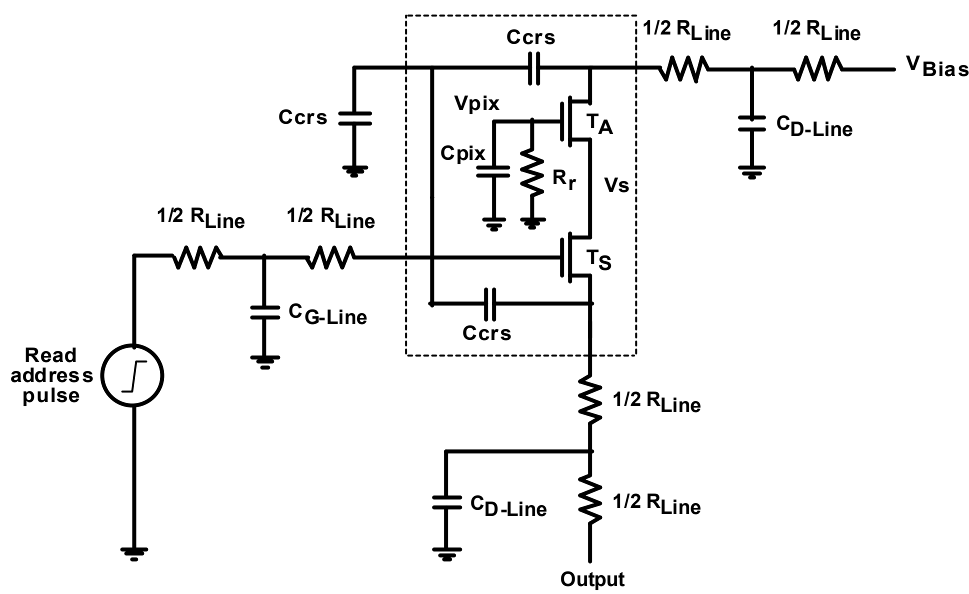


Figure 3.16. The circuit model for simulating 3T-APS array.

The settling time of APS architecture is important in determining the frame rate of the imager; shorter settling time results in faster readout and hence, higher frame rate. Figure 3.17 the simulated response of current mode 2T and 3T APS to a 10V step on the read addressing line (V_{Bias} = 10V).

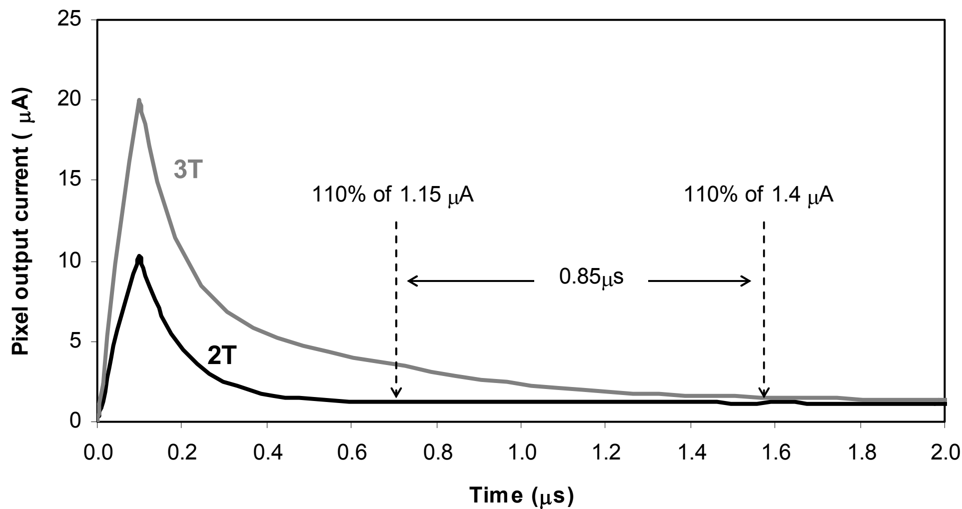


Fig. 3.17. Transient response of 2T and 3T C-APS

It is observed that 2T C-APS reaches the steady state current in about 0.7 microseconds, which is more two times faster compared to the 3T C-APS. The main reason for this long settling time is the fact that the source voltage of T_A in the 3T APS architecture, V_s, must be reduced from its high value of $V_{Bias} - V_t$, to a low value of 2-3 V in steady state. However, when T_S is turned on, it starts discharging the node voltage to the grounded output, but T_A is turned on too, which pumps current in to the parasitic capacitances of the said node.

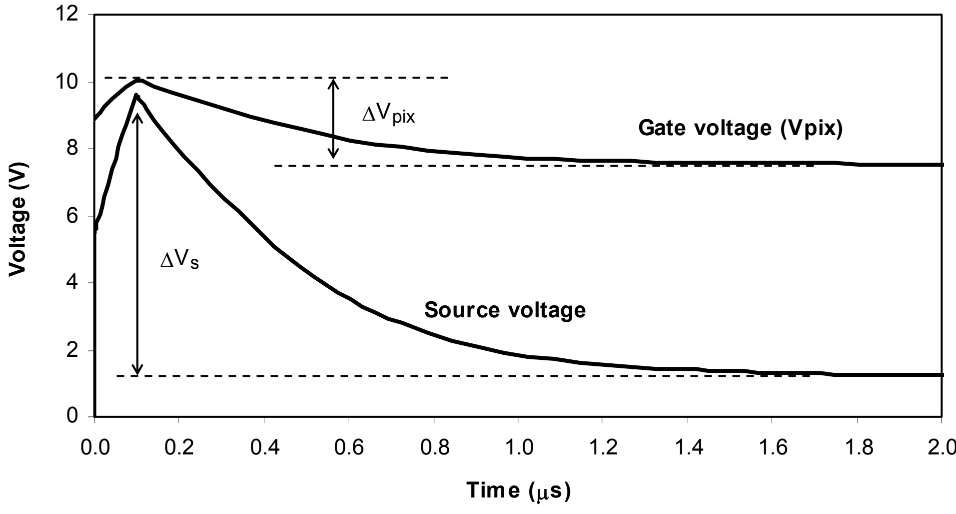


Figure. 3.18 Transient response of gate and source voltages of TA in 3T C-APS.

Figure 3.18 shows the transient response of the source voltage confirming the effect of changes in source voltage on the output current of 3T APS.

One other important aspect of the transient response of 3T APS is that the inevitable changes in the source voltage of T_A during readout transient time is followed by the gate voltage because the R_r is extremely high and the gate voltage is practically floating over C_{pix}. This results in considerable reduction of the preset value of the gate voltage (ΔV_{pix}, as expressed by Eqn. 3.29, leading to reduced transconductance gain of the T_A and subsequently reduced pixel gain, which is one of the drawbacks of the 3T APS architecture with small C_{pix}.

$$\Delta V_{pix} \approx \frac{C_{GS-OV} + C_{GS}}{C_{GS-OV} + C_{GS} + C_{GD-OV} + C_{pix}} \Delta V_S \, . \qquad 3.29$$

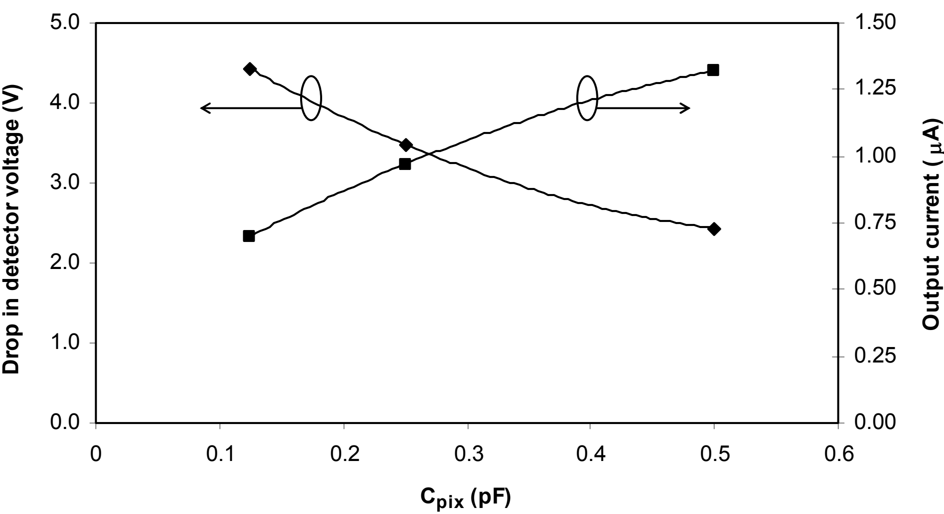


Figure 3.19. Effect of reduction of C_{pix} on detector preset voltage and pixel output current of the 3T C-APS

Reduction of C_{pix} is important in low noise imaging [21], especially for a-Se x-ray detectors where detector capacitance is very small because of the thick detector (500 – 1000µm), however, in the standard 3T C-APS, reducing C_{pix} degrades pixel transconductance gain and, more importantly, reduces the pixel dynamic range because of considerable drop in detector preset voltage. Fig. 3.19 shows the effect of reducing C_{pix} on the increased detector voltage drop, and reduced pixel output current. According to Eqn. 13.cc, if C_{pix} becomes very small, the detector voltage drop would approach that of the source voltage drop, especially for TFTs with small overlap capacitance.

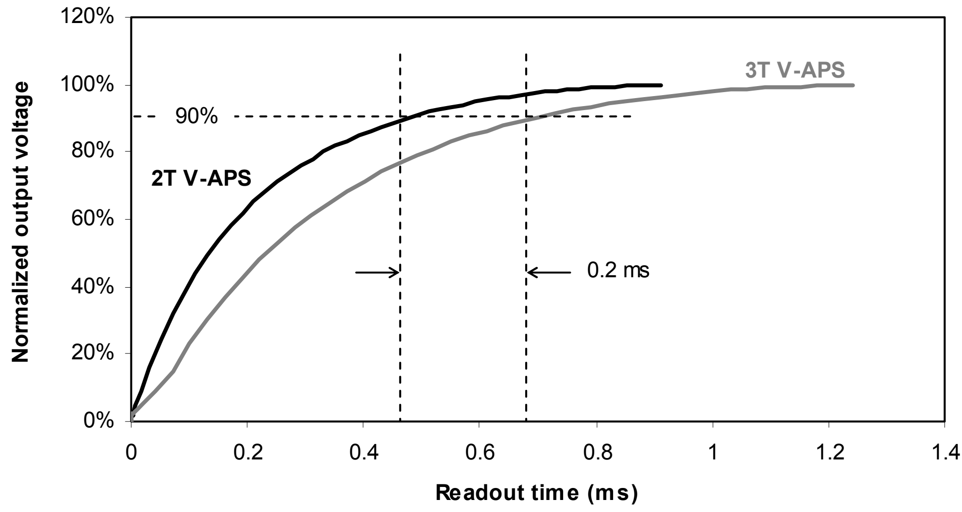


Fig. 3.20 Comparing the transient response of the 2T and 3T V-APS

The response time of voltage mode APS fabricated with a-Si TFTs is long because of low current level of a-Si TFTs, and the large parasitic line capacitance associated with very large area arrays. Figure 3.20 compares the output voltage of 2T and 3T V-APS pixels for $C_{D\text{-}Line}$ = 50 pF. It is observed that the 2T APS has faster response time, primarily because in 2T APS the line capacitance is charged through one TFT, where as for the 3T APS two TFTs in series charge up the line capacitance.

3.3 Summary

A novel thin film device, the charge-gated thin film transistor (CG-TFT), that has two gates: a regular voltage gate and a new added charge gate, was introduced and successfully tested to exhibit the capability of being switched ON and OFF, as well as modulating its ON state current depending on the amount of charge deposited on its charge gate. This device was incorporated in a novel two-transistor active pixel sensor readout circuit for high resolution large area digital imaging.

A novel two-transistor APS was introduced that employs a CG-TFT to replace the source-follower and the row-select transistors of the standard three-transistor APS. The 2T APS was successfully implemented in a 100μm pixel pitch 8×8 test array using amorphous silicon TFTs. Having the row-select TFT removed from the source of the source follower TFT, the transistor counts per pixel is reduced from 3 to 2 resulting in a smaller pixel size of 2T APS for higher resolution imaging, as well as reduced input referred noise performance owing to fewer noise sources and increased pixel transconductance gain.

Other configurations of two-transistor APS architectures, such as drain switched and source switched APS were also introduced, studied, and evaluated. It was shown that 2T APS using gate-switched amplifier is superior to drain or source switched architectures due to the fact that it can be operated by regular gate drivers in contrast to the other 2T architectures that require high current drivers. Additionally, it is possible to bias the gate-switched amplifier in both saturation and linear modes to adapt the readout circuit to low and high level input signals respectively. However, because of requiring only three lines per pixel, the 2T APS using drain switching has the simplest architecture.

By defining a resetting window, an alternative driving scheme for imagers based on APS was proposed in which multiple rows are reset at the same time, while the resetting window scans the imager array at a higher speed compared to traditional single row resetting in real time imaging. Owing to the APS charge gain, this technique can

potentially increase the imaging frame rate of the APS images compared to the industry standard PPS based imagers.

Study of the stability of 2T APS architectures under prolonged operation time confirmed that changes in pixel transconductance gain, as the result of V_t shift of a-Si TFTs, is manageably small and can be controlled by biasing voltages in gate-switched architecture.

Bibliography

[1] A. Madan, M. P. Shaw, "The Physics and Applications of Amorphous Semiconductors", Academic Press Inc, San Diego, 1988.

[2] Y. Kuo, Editor of textbook "Amorphous Silicon Thin Film Transistors," Kluwer Academic Publishers, Norwell, MA, 2003.

[3] L. Hojin, L. Yen-Chung, H.-P.D. Shieh, J. Kanicki, "Current-Scaling a-Si:H TFT Pixel-Electrode Circuit for AM-OLEDs: Electrical Properties and Stability" IEEE Transactions on Electron Devices, vol. 54, no. 9, pp. 2403-2410, September 2007.

[4] R.A. Street, J. P. Lu, S.R. Ready, New materials and processes for flat panel X-ray detectors", IEE proc. Circuits Devices and Syst,, vol. 150., no. 4, August 2004.

[5] K.S. Karim, A. Nathan, J.A. Rowlands, "Amorphous silicon pixel amplifier with V_T compensation for low noise digital fluoroscopy," *IEDM Technical Digest*, pp. 215-218, December 2002.

[6] S. O. Kasap, J. A. Rowlands, 'Direct-conversion flat-panel X-ray image sensors for digital radiography', Proceedings of the IEEE, vol. 90, no. 4, pp. 591–604, April 2002.

[7] F. Taghibakhsh, K.S. Karim, "Two-Transistor Active Pixel Sensor for High Resolution Large Area Digital X-ray Imaging" *IEEE Electron Devices Meeting, IEDM 2007,* pp. 1011-1014, December 2007.

[8]: M. J. Powell, C. Glasse, P. W. Green, I. D. French, and I. J. Stemp, "An Amorphous Silicon Thin-Film Transistor with Fully Self-Aligned Top Gate Structure", IEEE Electron Device Letters, vol. 21, no. 3, pp. 104-106, March 2000.

[9]: P. Servati, K.S. Karim, A. Nathan, "Static characteristics of a-Si:H Dual-Gate TFTs", IEEE Transactions on Electron Devices, 50(4), pp. 926-932, April 2003.

[10] R.A. Street, X.D. Wu, R. Weisfield, S. Ready, R. Apte, M. Nguyen, P. Nylen, "Two dimensional amorphous silicon image sensor arrays," MRS Symposium Proceedings, vol. 377, pp. 757-766, 1995.

[11] N. Matsuura, W. Zhao, Z. Huang, J.A. Rowlands, "Digital radiology using active matrix readout: amplified pixel detector array for fluoroscopy", *Med. Phys.*, vol. 26, no. 5, May 1999.

[12] K.S. Karim, A. Nathan, J.A. Rowlands, "Amorphous silicon active pixel sensor readout circuit for digital imaging", *IEEE Trans. Electron Devices*, vol. 50, No. 1, January 2003.

[13] S. Tedde, E. S. Zaus, J. Fürst, D. Henseler, P. Lugli, "Active pixel concept combined with organic Photodiode for Imaging Devices", *IEEE Elec. Device Lett.*, vol. 28, no. 10, October 2007

[14] K.S. Karim, A. Nathan, "Noise performance of a current-mediated amplified pixel for medical imaging", *J. Vac. Sci. Technol. A*, vol. 22, pp. 1010–1014, 2004.

[15] F. Taghibakhsh, K.S. Karim, "Amplified pixel sensor architectures for low dose computed tomography using silicon thin film technology", *Proc. of SPIE*, vol. 6510, pp. 65103W-1, March 2007.

[16] F. Taghibakhsh, K.S. Karim, "High dynamic range 2-TFT amplified pixel sensor architecture for digital mammography tomosynthesis", *IET Circuits Devices Syst.*, vol. 1, no. 1, February 2007.

[17] F. Taghibakhsh, K.S. Karim, "Charge-Gated Thin Film Transistors for High Resolution Digital Imaging Applications", *IEEE Trans. Elec. Devices*, under revision, April 2008.

[18] S.O Kasap, J.A. Rowlands, "Direct-conversion flat-panel X-ray image sensors for digital radiography", *Proceedings of the IEEE*, vol. 90, no. 4, pp.591-604, April 2002.

[19] K.S. Karim, A. Nathan, J.A. Rowlands, S.O. Kasap, “X-ray detector with on-pixel amplification for large area diagnostic medical imaging’, *IEE Proc., Circuits Devices Syst.*, vol. 150, no. 4, pp. 267–273, 2003.

[20] V. Gruev, Z. Yang, J.V. Spiegel, R. Etienne-Commings, “Two Transistor Current Mode Active Pixel Sensor”, *Proc. IEEE (ISCAS)*, pp. 2846-2849, May 2007.

[21] M.H. Izadi, K.S. Karim, “High dynamic range pixel architecture for advanced diagnostic medical X-ray imaging applications”, *J. Vac. Sci. Technol. A*, vol. 24, no. 3, pp 846-849, May 2006.

[22] M.H. Izadi, K.S. Karim, “Noise optimisation analysis of an active pixel sensor for low-noise real-time X-ray fluoroscopy”, *IET Circuits, Devices & Systems*, vol. 1, no. 3, pp. 251-256, June 2007.

[23] J.M. Boudry, L.E. Antonuk, “Current-noise-power spectra of amorphous silicon thin-film transistors”, *J. Applied Physics*, vol. 76, no. 4, pp. 2529-2534, August 1994.

[24] J. Rhayem, D. Rigaud, M. Valenza, “1/*f* noise modeling in long channel amorphous silicon thin film transistors”, *J. Applied Physics*, vol. 87, no. 4, pp. 1982-1989, February 2000.

[25] C. van Berkel and M. J. Powell, “The resolution of amorphous silicon thin film transistor instability mechanisms using ambipolar transistors,” *Appl. Phys. Lett.*, vol. 51, pp. 1094-1096, 1987.

[26] C. Chiang, J. Kanicki, and K. Takechi, “Electrical instability of hydrogenated amorphous silicon thin-film transistors for active-matrix liquid-crystal displays,” *Jap. J. Appl. Phys.*, vol. 37(1), no. 9A, pp. 4704–4710, 1998.

[27] C. Huang, T. Teng, J. Tsai, and H. Cheng, “The instability mechanisms of hydrogenated amorphous silicon thin film transistors under AC Bias stress,” *Jpn. J. Appl. Phys.*, vol. 39(1), no. 7A, pp. 3867–3871, 2000.

[28] K.S. Karim, A. Nathan, M. Hack, W. I. Milne, "Drain-bias dependence of threshold voltage stability of amorphous silicon TFTs", *IEEE Elec. Device Lett.*, vol. 25, no. 4, pp. 188 – 190, April 2004.

4

Fabrication of Test Arrays

This chapter describes thin film deposition conditions for PECVD deposition, the structure of thin film transistor and the active pixel sensor, the photomasks required for fabrication, and the complete fabrication process, as well as characterization of the TFTs and test arrays made.

Owing to their superior stability compared to PECVD fabricated TFTs [1], Hot-wire (HW) deposition was initially considered as an option for fabrication of TFTs required for developing the 2T APS. Even rugged substrates were considered as a replacement for brittle and relatively expensive corning glass [2], or more stable nano-crystalline silicon with higher carrier mobility was considered to replace a-Si [3]. But for the reason that the project of expansion of our test HW chamber to a full 5” deposition chamber stopped, PECVD fabrication was used to implement 2T-APS.

4.1 Thin Film Circuit Fabrication Process

4.1.1 Thin Film Deposition

Fabrication of thin film circuits using a-Si TFTs requires the following three different silicon films, as well as metal layers [4].

- Hydrogenated amorphous silicon (a-Si:H) as the semiconducting later
- Hydrogenated amorphous silicon nitride (SiN_x:H) for gate dielectric, and
- Phosphor doped microcrystalline silicon (n+ μc-Si) for formation of ohmic contacts.

Plasma enhanced chemical deposition (PECVD) is the common method for depositing thin films [5], and an MV-System® CVD cluster tool was used for deposition and characterization of these films [6]. RF sputtering technique [7] was used to deposit aluminum as the metal layer. The five major process control parameters for PECVD are camber pressure, substrate temperature, gas mixture, gas flow rate, and plasma power [8]. For sputtering, the pressure of Argon gas, electrode to substrate distance and the plasma power are the main the process control parameters. Table 4.1 shows the deposition conditions and measured properties of the various films used for fabrication of a-Si TFTs for this research. It is worth noting that these deposition conditions were developed and/or trimmed by the author in order to arrive at acceptable TFT characteristics.

Table 4.1. Deposition conditions for PECVD films.

	a-Si:H	SiN_x	n^+ μc-Si
Gases mixture	$SiH_4 + H_2$	$SiH + NH_3 + H_2$	**$SiH_4 + PH_3 + H_2$**
Flow rates	3 : 20 sccm	4 : 16 : 100 sccm	**1 : 0.05 : 200 sccm**
Chamber pressure	0.5 Torr	1.3 Torr	**1.9 T**
Substrate temp.	250 °C	250 °C	**250 °C**
Plasma power	**1 W**	**20 W**	**20 W**

For hydrogenated amorphous silicon, deposited using reported conditions in Table 4.1, the deposition rate was measured to be 12 nm/min with minimum dark conductivity of 4×10^{-9} S/cm, and a maximum photo to dark conductivity ratio of 6.2×10^{4} for a 120 nm thick a-Si film deposited on corning glass 1337. The bandgap, extracted using Tauc method, was 1.85 eV, with the dark fermi level of 0.65 eV, and the hydrogen content of the film was estimated to be 15-18%.

For silicon nitride film the deposition rate was 16 nm/min, and the etch rate in buffered HF was 1.1 nm/sec. Tauc bandgap was extracted to be 4.5 eV, and breaking electric field of more than 7.2 MV/cm was measured, with a relative permittivity of 6 for samples.

For the n+ doped microcrystalline film, the dark conductivity was measured to be 25 S/cm for 40-50 nm thick films, and 84.5 S/cm for thicker films of 160-180 nm thicknesses. The ratio of photo to dark conductivity was up to 4, with carrier activation energy of 0.06 eV.

Standard electronic grade aluminum (+ 1% silicon) was used in the sputtering target for deposition of metal layers in an in-house assembled sputtering chamber. The aluminum deposition rate was measured to be 7.5 nm/min at substrate-target distance was 11 cm, and 50W DC argon plasma at 5 mTorr chamber pressure. The conductivity of the sputtered aluminum was measured to be ~ 2×10^{6} S/cm.

4.1.2 Thin Film Transistor Structure

Compared to bottom-gate TFT structure which is the most common structure used for fabrication of amorphous silicon TFTs [9], top-gate structure is preferred for fabrication of x-ray detector arrays with amorphous selenium detector for two main reasons:

- Simpler fabrication process because of elimination of the need for an electrostatic shield to protect the channel of the reset TFT.
- Ease of detector integration to the top gate of the amplifier TFT.

As illustrated in Fig. 4.1, in case a bottom gate TFT is used the voltage of the detector bottom electrode acts as a second gate for the reset, (and amplifier) TFT leading to unwanted change in its characteristics [10]. In a top gate configuration, the channel is automatically protected by the metal gate.

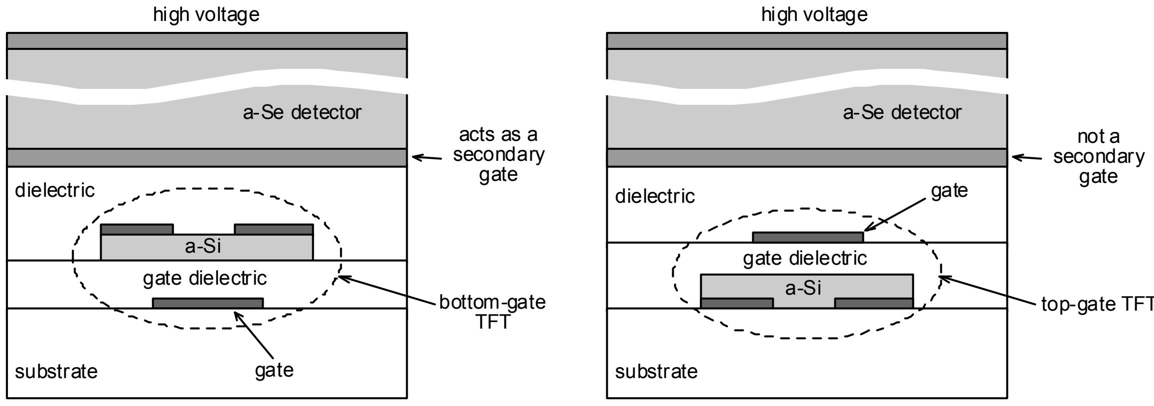


Fig. 4.1. Detector electrode acts as a secondary gate if bottom-gate TFTs are used (left), whereas, top-gate TFTs find no such problem (right)

A top-gate staggered TFT structure with double gate dielectric [11] (Fig. 4.2) was selected for fabrication of active pixel sensor circuits using a-Si TFTs in this research. As shown in Fig. 4.2, the possibility of connecting the two metal layers is provided using vias in the second silicon nitride layer. This metal interconnect between gate and drain/source is needed for fabrication of integrated circuits such as active pixel circuits.

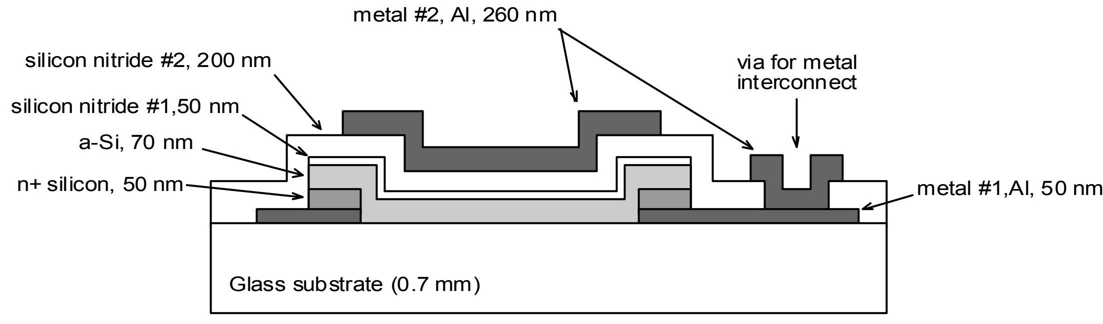


Figure. 4.2 Details of the structure of the top-gate staggered film transistor used in this research.

In order to provide the possibility of integrating the TFT circuit with a-Se x-ray photoconductor, a bottom electrode for the photoconductor must be provided and connected to the TFT circuit underneath. To maximize the fill factor, i.e. the ratio of detector area to the pixel area, a fully overlapped photoconductor was considered. It is preferred to use a low-k dielectric, or a very thick one, to reduce the capacitive coupling of the gate and data lines with the detector bottom electrode [12]. Three micrometers of Polyimide was used as the dielectric between x-ray photoconductor and the TFT circuit, on top of a thin capsulation silicon nitride film. Fig. 4.3 shows the schematic diagram of the cross-section of the photoconductor bottom electrode connected to the gate of the TFT under the electrode.

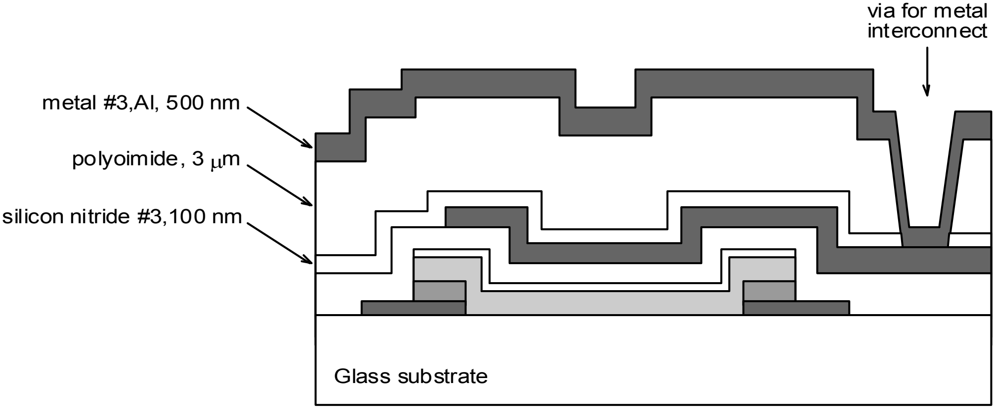


Figure. 4.3 Details of the dielectric between the fully overlapped photoconductor electrode (metal #3) and the thin film circuit.

4.1.3 Mask Design

A six-mask process was designed [13] to fabricate the complete TFT circuit and the detector electrode. Four masks are required to fabricate the thin film circuit, and two masks for integrating and patterning the detector electrode. The six photomasks were made at the nanofabrication lab of University of Alberta, AB, Canada. Table 4.1 describes mask designations and their application.

Table 4.2. Designations and descriptions of the 6 mask used.

Mask number	Usage	Description
# 1	Pattering metal #1 and n+ film	TFT drain-source contacts, and bias line formation
# 2	Patterning a-Si silicon island and silicon nitride #1	Amorphous silicon channel formation
# 3	Opening via #1	Providing gate to drain-source interconnection
# 4	Patterning metal #2	TFT Gate contacts, and array gate lines formation
# 5	Opening via #2	Providing photoconductor bottom electrode to TFT interconnection
# 6	Patterning metal #3	Photoconductor bottom electrodes and array bond pads formation.

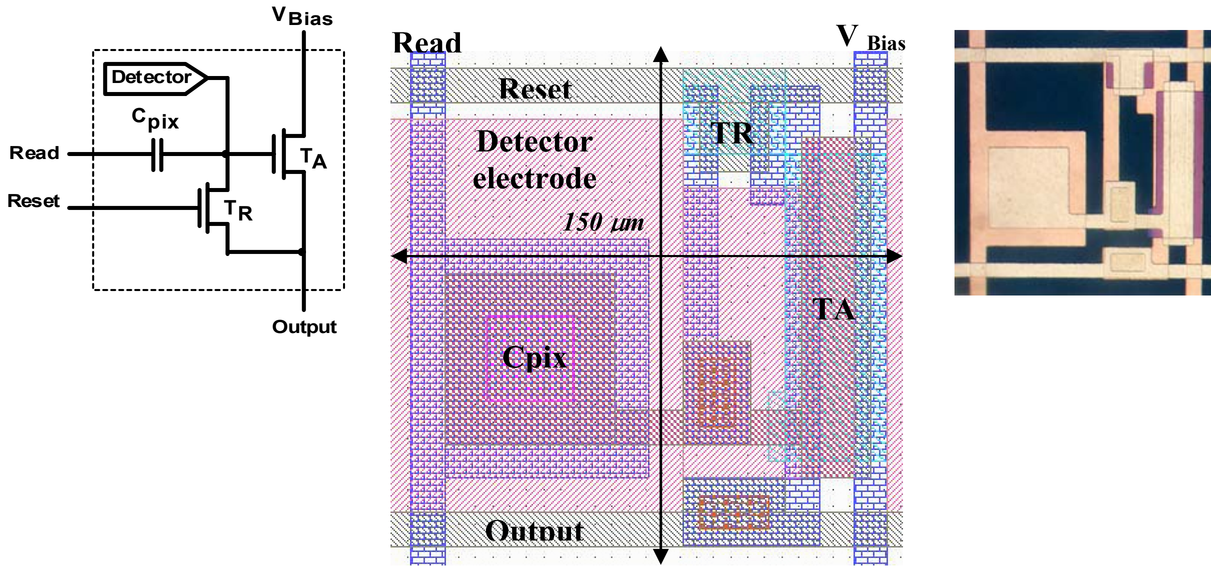
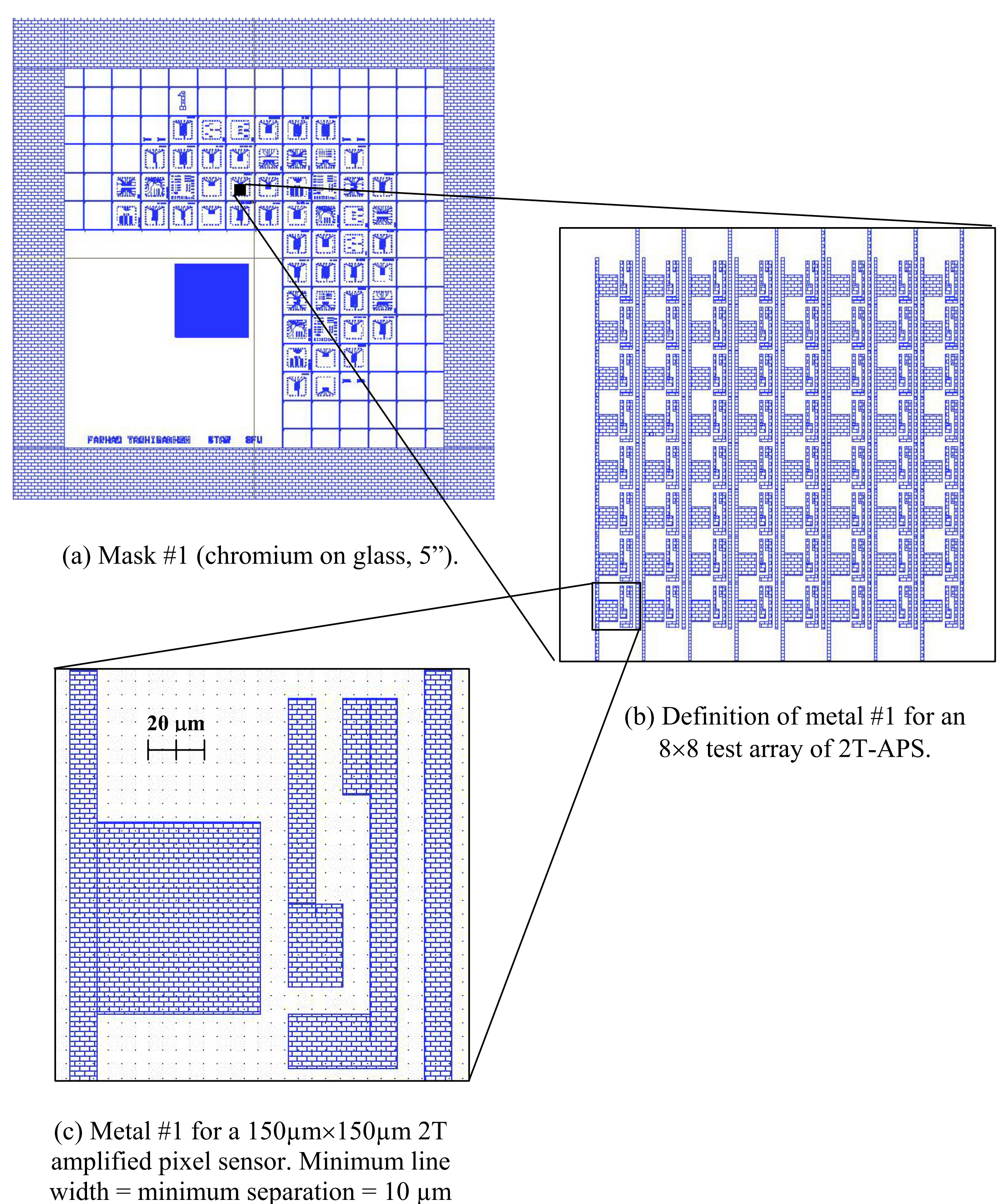


Fig. 4.4. The 2T APS circuit diagram (left) and its overplayed masks with pixel pitch of 150µm (middle). The fabricated thin film circuit not including the detector electrode (right).

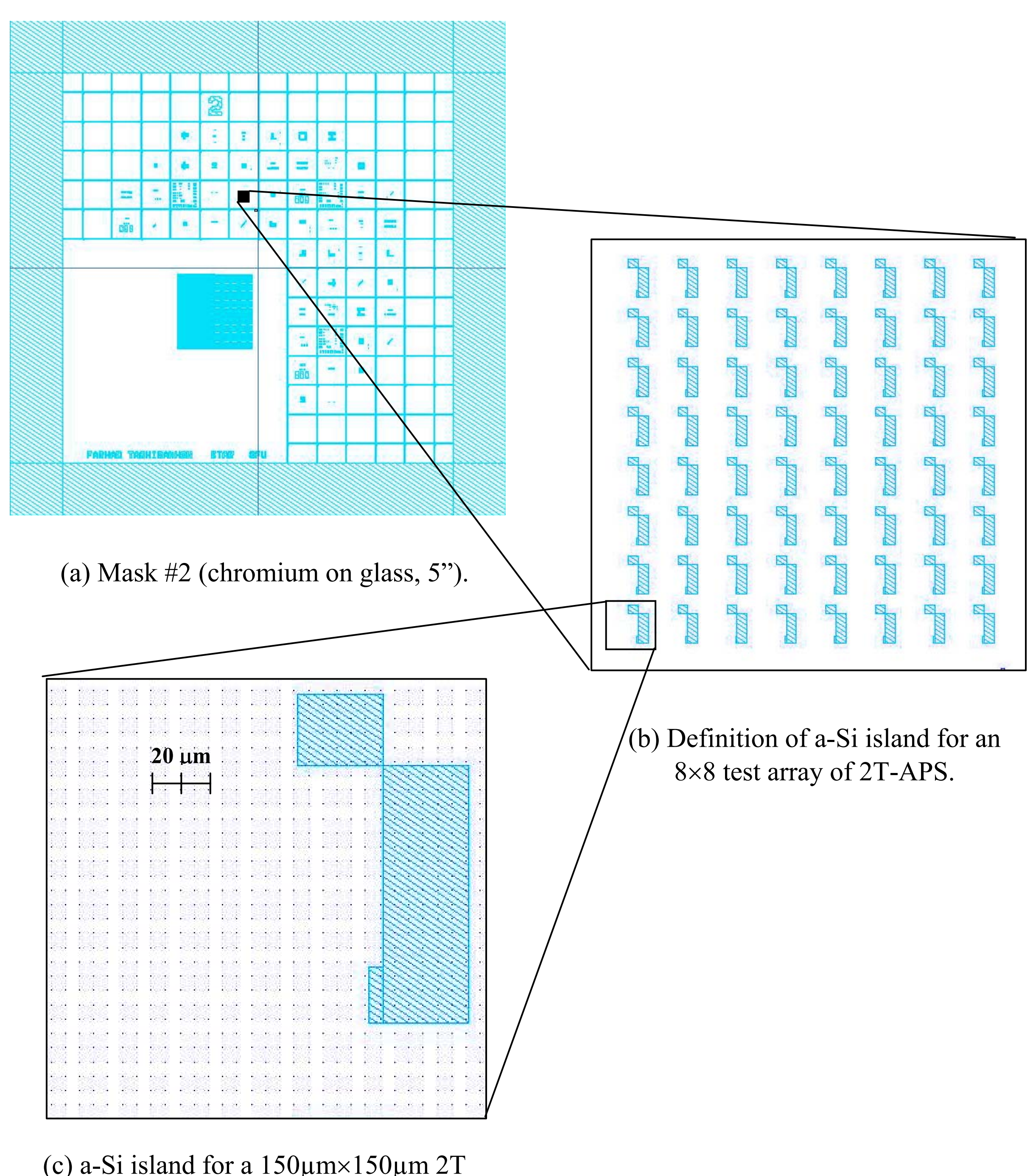


(a) Mask #1 (chromium on glass, 5”).

(b) Definition of metal #1 for an 8×8 test array of 2T-APS.

(c) Metal #1 for a 150μm×150μm 2T amplified pixel sensor. Minimum line width = minimum separation = 10 μm

Fig. 4.5. Pictures of mask #1, an example of its test arrays, and one pixel.

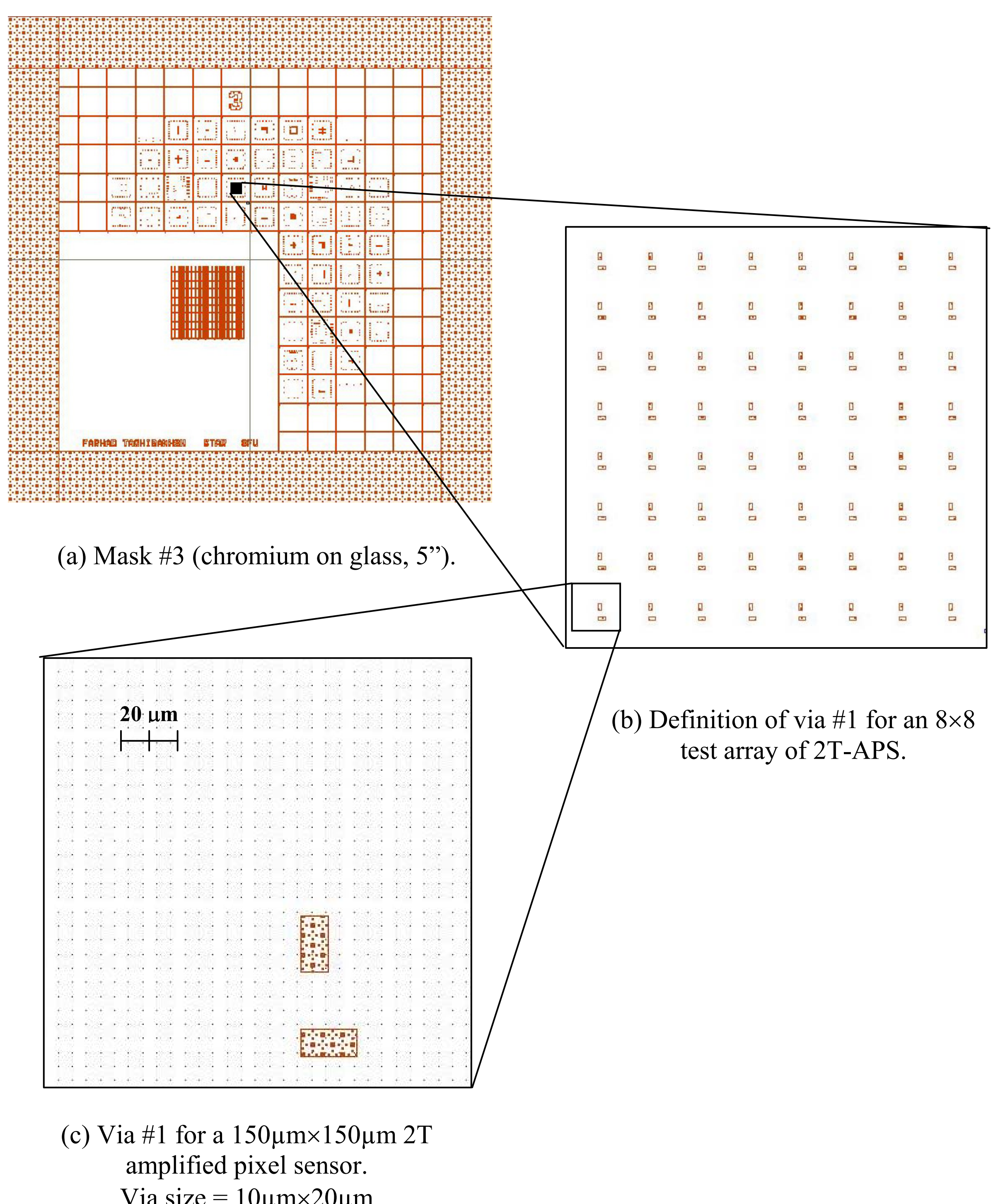


(a) Mask #2 (chromium on glass, 5”).

(b) Definition of a-Si island for an 8×8 test array of 2T-APS.

(c) a-Si island for a 150µm×150µm 2T amplified pixel sensor.

Fig. 4.6. Pictures of mask #2, an example of its test arrays, and one pixel.

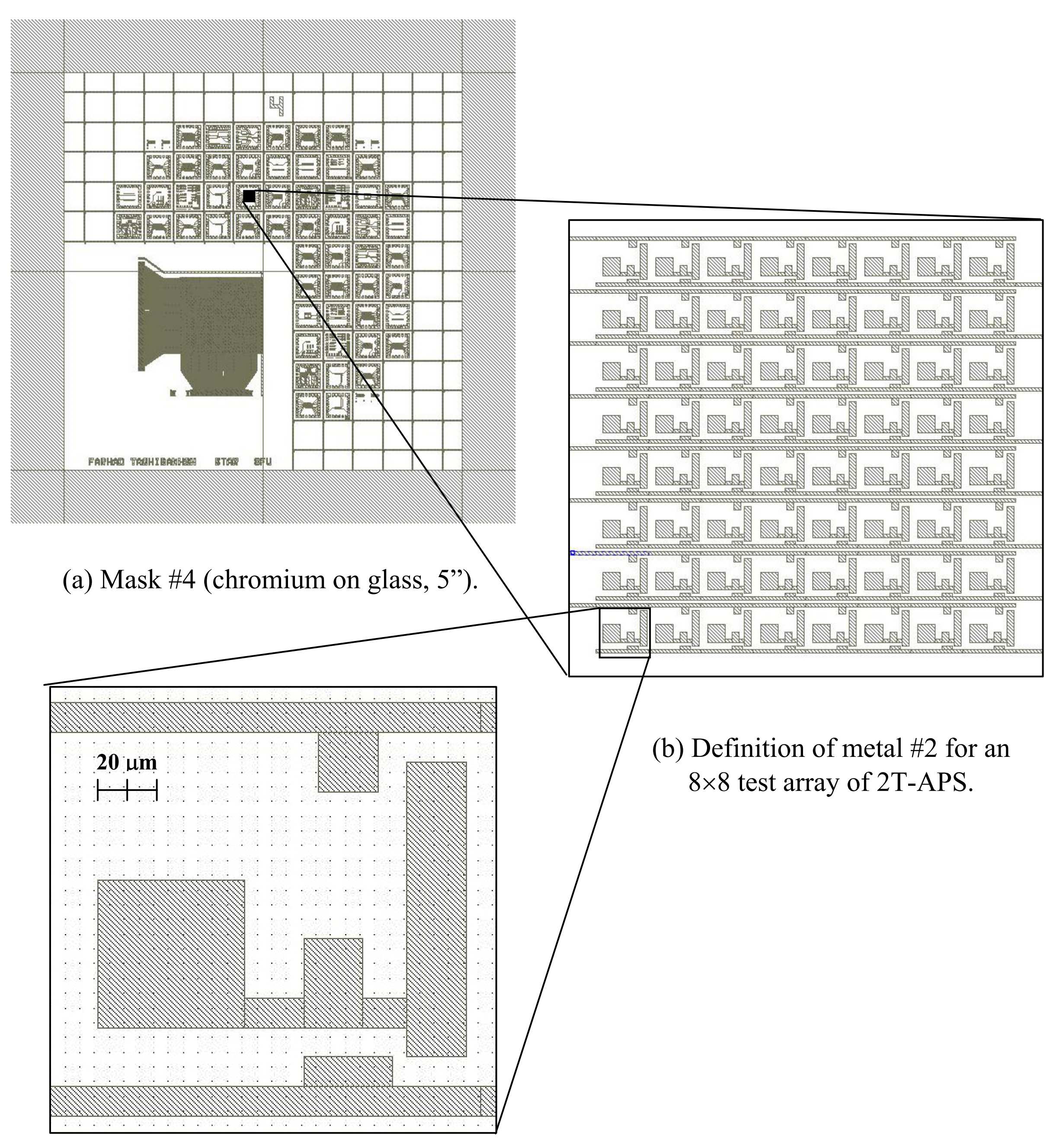


(a) Mask #3 (chromium on glass, 5”).

(b) Definition of via #1 for an 8×8 test array of 2T-APS.

(c) Via #1 for a 150μm×150μm 2T amplified pixel sensor.
Via size = 10μm×20μm

Fig. 4.7. Pictures of mask #3, an example of its test arrays, and one pixel.

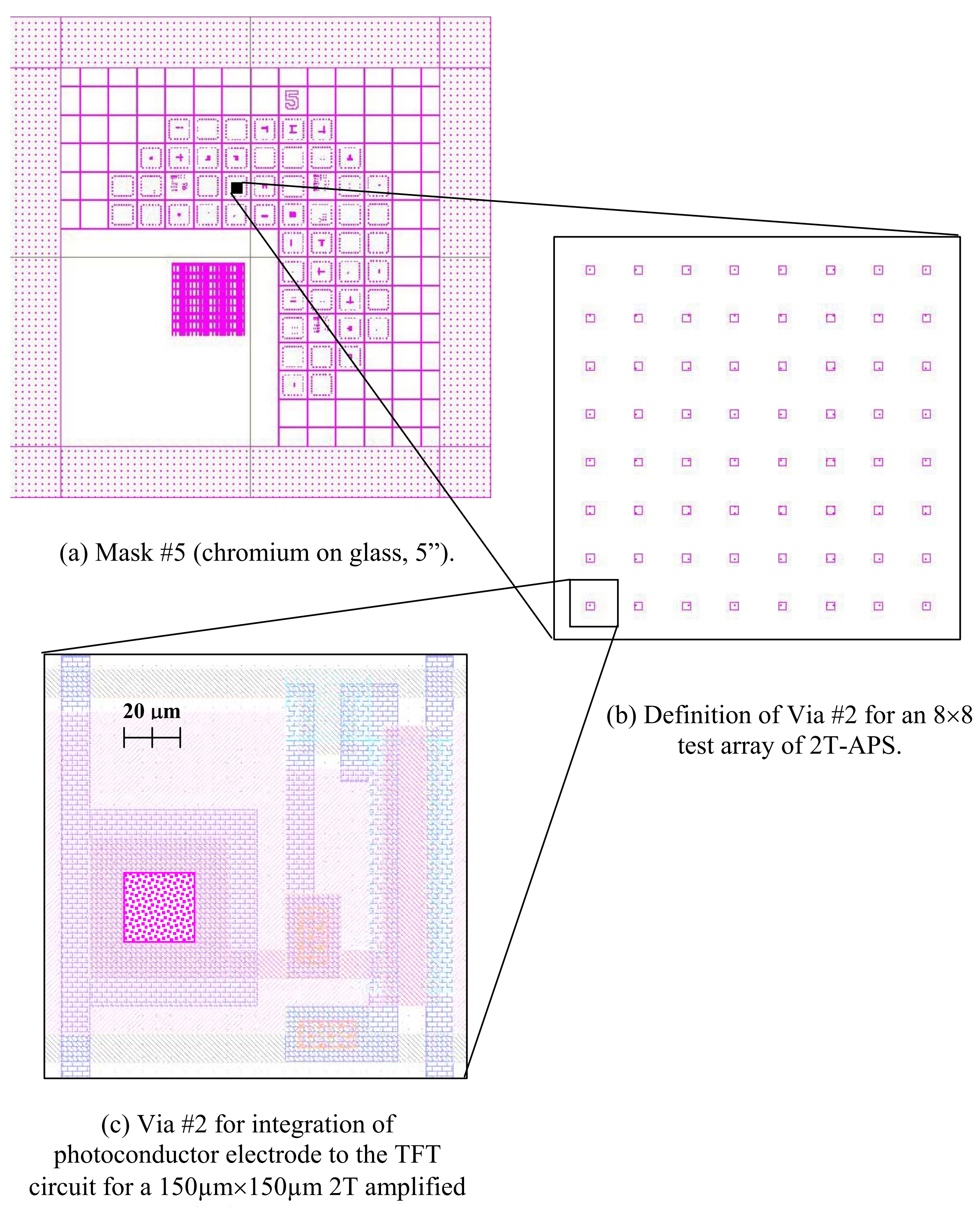


(a) Mask #4 (chromium on glass, 5”).

(b) Definition of metal #2 for an 8×8 test array of 2T-APS.

(c) Gate contacts and gate lines for a 150µm×150µm 2T amplified pixel sensor. Minimum line width = 10µm.

Fig. 4.8. Pictures of mask #4, an example of its test arrays, and one pixel.

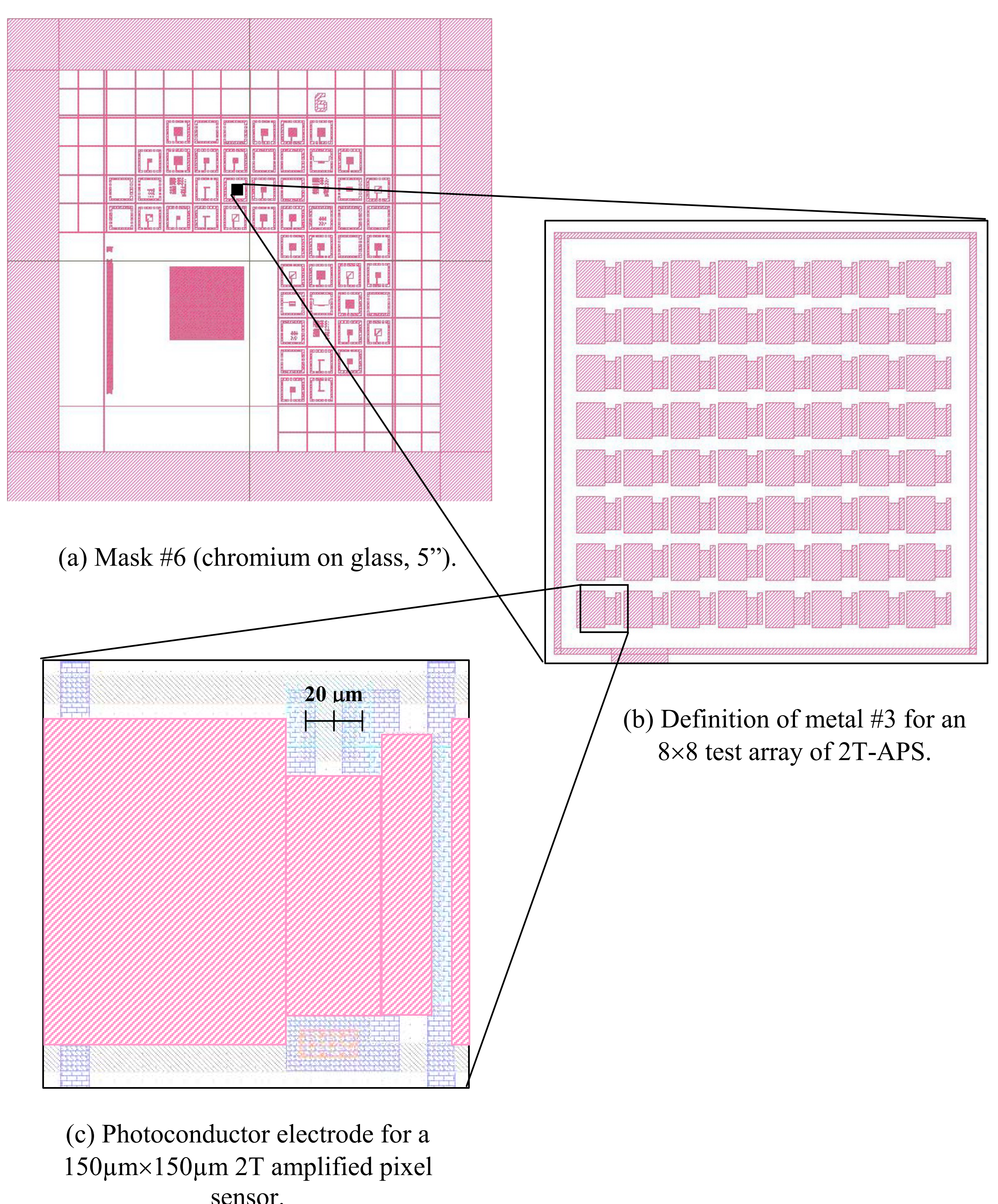


(a) Mask #5 (chromium on glass, 5”).

(b) Definition of Via #2 for an 8×8 test array of 2T-APS.

(c) Via #2 for integration of photoconductor electrode to the TFT circuit for a 150μm×150μm 2T amplified pixel sensor.

Fig. 4.9. Pictures of mask #5, an example of its test arrays, and one pixel.



(a) Mask #6 (chromium on glass, 5”).

(b) Definition of metal #3 for an 8×8 test array of 2T-APS.

(c) Photoconductor electrode for a 150μm×150μm 2T amplified pixel sensor.

Fig. 4.10. Pictures of mask #6, an example of its test arrays, and one pixel.

4.1.4 Fabrication Process

The complete 46-step thin film active pixel fabrication process, including formation of the photoconductor bottom electrode is listed in Table 4.3.

Table 4.3. Fabrication process of thin film circuit fabrication process

Step	Description	Mask	Conditions
	Drain-source contact formation		**(8 steps)**
1	Aluminum sputtering		50 nm
2	PECVD n+ μc-Si		50 nm, according to Table 4.1
3	Spin coating photoresist (PR)		4700 rpm, 30 sec
4	Soft baking		100 °C, 20 min in oven, or, 105 °C, 90 sec on hotplate
5	Patterning PR	#1	UV exposure, 8 sec, MF-319 developer, 60 sec
6	Dry etching n+ μc-Si		CF_4:O_2, 50:5 sccm, 100 mTorr, 100W, 90 sec.
7	Wet etching aluminum		Standard Al etchant, 50°C
8	Stripping PR		Acetone, 2 min + 30 sec ashing at 50 W
	Active island formation		**(7 steps)**
9	PECVD a-Si		70 nm, according to Table 4.1
10	PECVD SiNx		50 nm, according to Table 4.1
11	Spin coating PR		4700 rpm, 30 sec
12	Soft baking		100 °C, 20 min in oven, or, 105 °C, 90 sec on hotplate
13	Patterning PR	#2	UV exposure, 8 sec, MF-319 developer, 60 sec
14	Dry etching SiNx, a-Si, n+ μc-Si		CF_4:O_2, 50:5 sccm, 100 mTorr, 100W, 5:30 min.
15	Stripping PR		Acetone, 2 min + 30 sec ashing at 50 W
	Gate dielectric and via formation		**(6 steps)**
16	PECVD SiNx		200 nm, according to Table 4.1
17	Spin coating PR		4700 rpm, 30 sec
18	Soft baking		100 °C, 20 min in oven, or, 105 °C, 90 sec on hotplate
19	Patterning PR	#3	UV exposure, 10 sec, MF-319 developer, 60 sec

20	Dry etching SiNx		CF4:O2, 50:5 sccm, 100 mTorr, 100W, 5 min.
21	Stripping PR		Acetone, 2 min + 30 sec ashing at 50 W
D	***Gate and interconnect formation***		**(6 steps)**
22	Aluminum sputtering		260 nm
23	Spin coating PR		4700 rpm, 30 sec
24	Soft baking		100 °C, 20 min in oven, or, 105 °C, 90 sec on hotplate
25	Patterning PR	#4	UV exposure, 8 sec, MF-319 developer, 60 sec
26	Wet etching aluminum		Standard Al etchant, 50°C
27	Stripping PR		Acetone, 2 min + 30 sec ashing at 50 W
	Thick dielectric formation		**(13 steps)**
28	PECVD SiNx		100 nm, according to Table 4.1
29	Spin coating polyimide (PI)		Coat at 500 rpm, ramp to 7000 rpm in 20 sec, leave at 7000 rpm for 30 sec
30	Hard baking		4 min at 80°C + 3 min at 150°C, ramp to 250°C at 240 °C/h and leave for 2 hours
31	Spin coating thick PR		900 rpm, 30 sec
32	Soft baking		100 °C, 20 min in oven
33	Spin coating thick PR		900 rpm, 30 sec
34	Soft baking		100 °C, 20 min in oven
35	Spin coating thick PR		900 rpm, 30 sec
36	Soft baking		100 °C, 20 min in oven
37	Patterning PR	#5	UV exposure, 60 sec, MF-319 developer, 3 min
38	Dry etching PI		O2:CF4, 50:10 sccm, 100 mTorr, 100W, 15 min.
39	Dry etching SiNx		CF4:O2, 50:5 sccm, 100 mTorr, 100W, 5 min.
40	Stripping PR		Acetone, 5 min + 30 sec ashing at 50 W
	Photoconductor bottom electrode formation		**(6 steps)**
41	Aluminum sputtering		500 nm
42	Spin coating PR		4700 rpm, 30 sec
43	Soft baking		100 °C, 20 min in oven, or, 105 °C, 90 sec on hotplate
44	Patterning PR	#6	UV exposure, 8 sec, MF-319 developer, 60 sec
45	Wet etching aluminum		Standard Al etchant, 50°C
46	Stripping PR		Acetone, 2 min + 30 sec ashing at 50 W

Figure 4.11 shows the TFT circuit of a 2T APS circuit with 150μm pixel pitch (up to step 27, not including the detector electrode), as well as the overplayed picture of its four masks, mask #1 to #4. The fabrication process continues with annealing the glass wafers in 170 ºC for 1 hour, followed by dicing, packaging and bonding the dies.

Fig. 4.11. Fabricated thin film circuits on a 3” corning glass wafer.

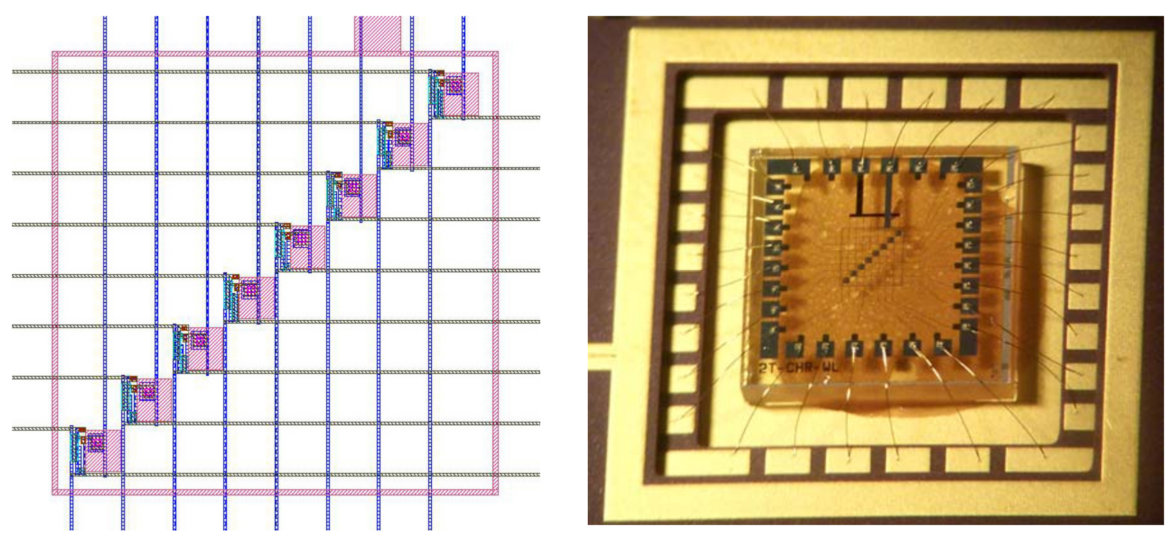


Fig. 4.12. Six overlaid masks of a characterization array of 2T APS pixels (left) and its die bonded to a standard 28-pin package after fabrication and dicing (left).

4.2 Characteristics of Fabricated Thin Film Transistors and Arrays

4.2.1 Thin Film Transistor Characterization

Figure 4.13 shows the transfer characteristics of a fabricated TFTs with W/L of 300µm/10µm, where the ON-OFF ratio as high as 4.1×10^7 and 2.75×10^7 for V_{DS} equal to 1 V and 10 V respectively. The graph also shows the low leakage current of less than 10-12 A up to -10V of V_{GS}, as well as extracted sub-threshold swing of 0.43 V/decade. The output characteristic of the TFT if shown in Fig. 4.14, where the linear behavior of the I-V curve at low V_{DS} voltages indicates good quality ohmic contact between drain-source and the channel by proper choice of n+ µc-Si thickness.

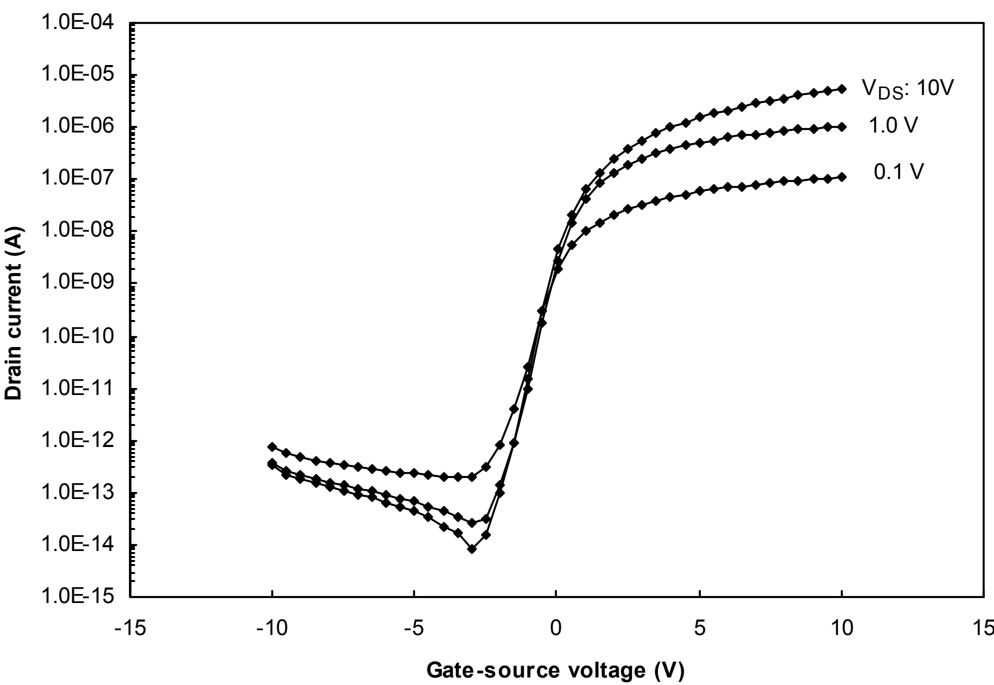


Figure. 4.13. The transfer characteristics of a fabricated a-Si TFT with W/L of 300µm/10µm.

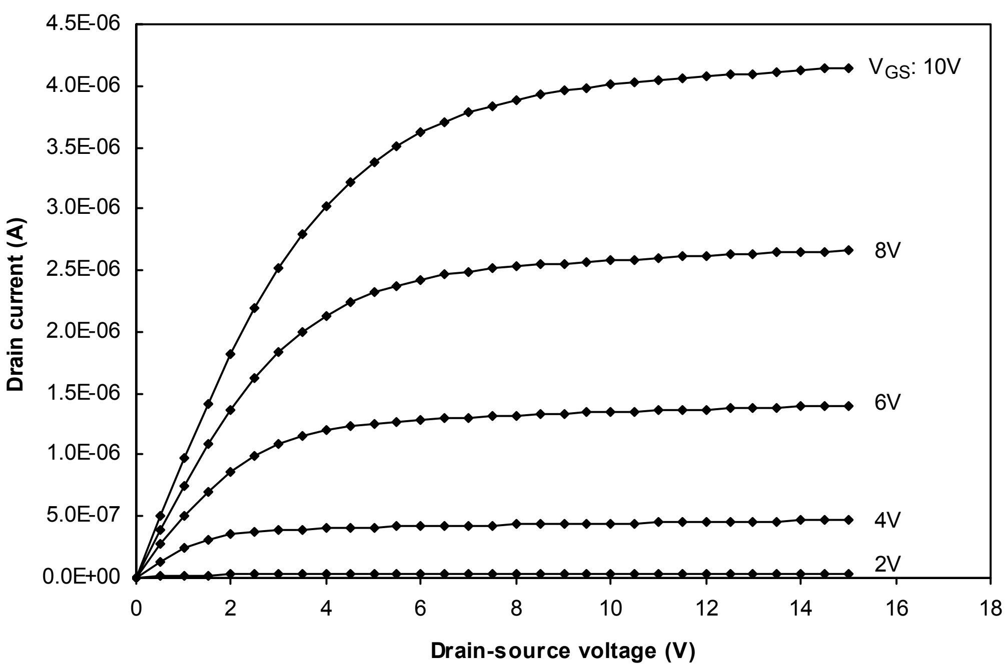


Figure. 4.14. The transfer characteristics of a fabricated a-Si TFT with W/L of 300μm/10μm.

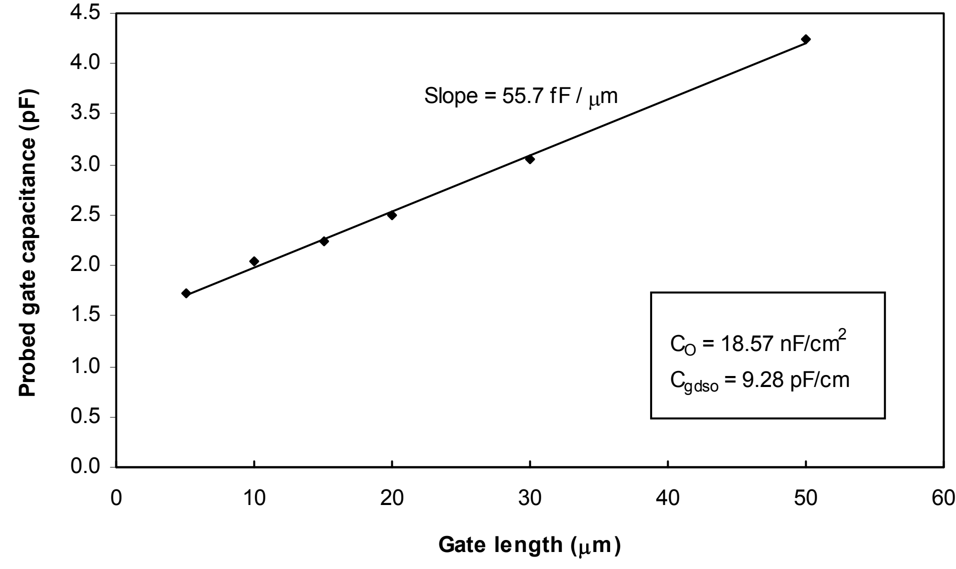


Figure. 4.15. Extraction of C_0, from probed gate capacitance of TFTs with different gate length.

Quasi static C-V measurements were performed for TFTs with different gate lengths to extract the gate capacitance per unit area, or C_0, from the slope of the probed gate capacitance, C_G. All TFTs had gate width of 300 μm and gate to drain-source overlap of 5 μm.

$$C_G = C_{probe} + C_{G-OV} + C_{ch} = C_{const} + C_0 W.L \tag{4.1}$$

$$C_0 = \frac{1}{W}\frac{\partial C_G}{\partial Lg} = \frac{1}{300\times10^{-4}}\times 55.7\, fF/\mu m = 18.57\, nF/cm^2 \tag{4.2}$$

As indicated in Eqn. 4.1, the measured probed gate capacitance is equal to some stray capacitances plus the channel capacitance C_{ch} which is proportional to gate area, $W.L$, so that C_0 is calculated from the slope of the line as expressed in Eqn. 4.2.

The field effect mobility is extracted from slope of channel conductance versus gate length measured in linear mode (at low V_{DS} voltages). The specific drain-source resistance R_{DS}, is the slope of the ratio of I_D to V_{DS} with respect to the gate-source voltage which is the sum of channel resistance per unit voltage of gate, $L.r_{ch}$ and the contact resistance of drain or source, R_C expressed in 4.3 [6].

$$R_{DS} = \frac{V_{DS}}{I_{DS}} = L\cdot r_{ch} + 2R_C \tag{4.3}$$

Fig. 4.16 shows the channel resistance of different TFTs measured for two values of V_{DS}, where the field effect mobility is calculated to be

$$\mu_{FE} = \frac{1}{367.3\times10^3}\times\frac{1}{W}\times\frac{1}{C_0} = 0.504\, cm^2/Vs \qquad (4.3)$$

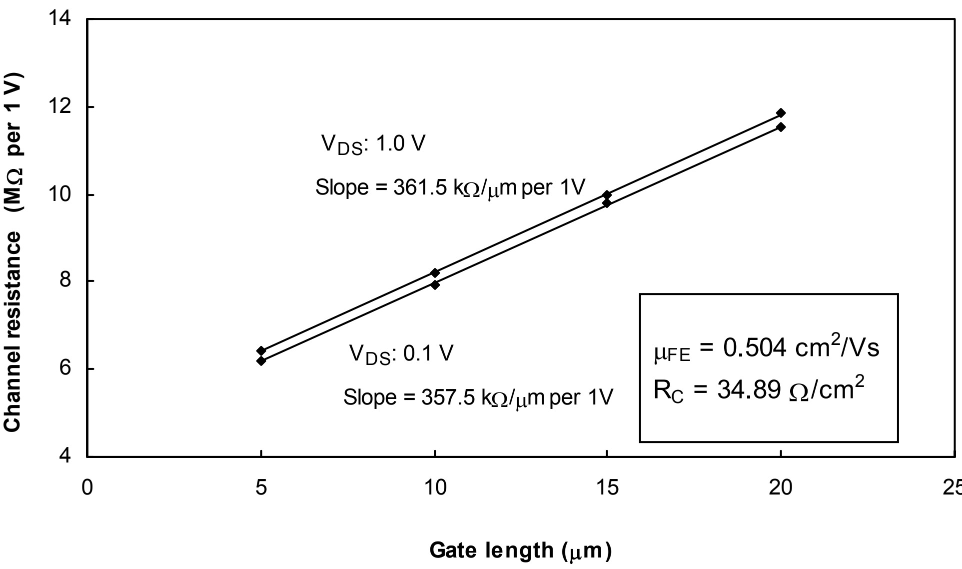


Figure. 4.16. Extraction of field effect mobility and specific contact resistance from channel resistance measured in linear region (V_{DS} = 0.1V and 1.0 V) of TFTs with different gate lengths (W = 300μm)

The apparent threshold voltage was extracted from the linear characteristics to be between 1.01 V to 1.1 V for TFTs with gale length of 5 μm to 50 μm, whereas the intrinsic threshold voltage extracted from measured channel conductance [6] was between 0.21 V and 0.3 V for the same TFTs.

4.2.2 Two-Transistor APS Array

The test array of Fig. 4.12 consists of different two-transistor pixels with different aspect ratio for T_A. For constant gate width of 100μm, there are gate lengths of 5μm, 7.5μm and 10μm, whereas for constant gate length of 10μm, there are three pixels with T_A gate width of 100μm, 70μm, and 50μm. Pixel transconductance gain ($G_m = \partial I_{out} / \partial V_{read}$) of the packaged die was measured by mounting the package on the test box of the Agilent semiconductor parameter analyzer as illustrated in Fig. 4. 17. These data are used for designing desired pixel gain for a particular application [11].

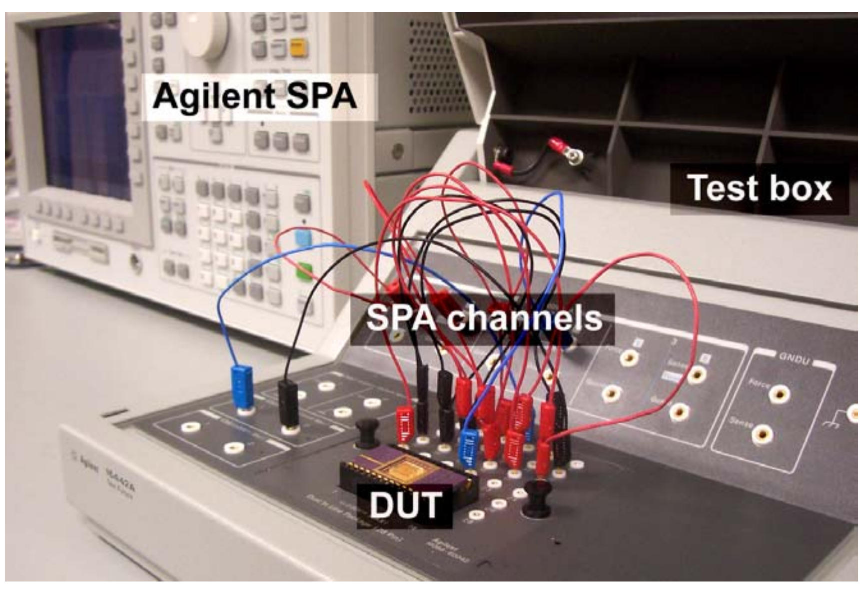


Fig. 4.17. Connection of packaged devices to the Agilent 4156 Semiconductor Parameter Analyzer (SPA) using the Agilent® test box.

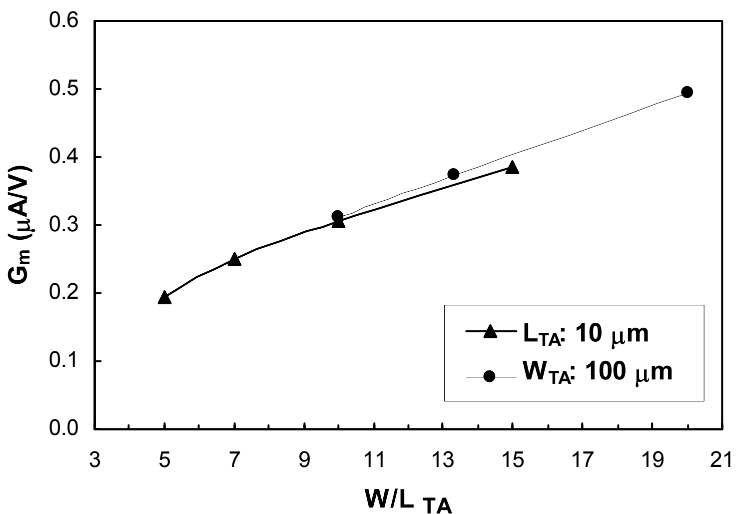


Fig. 4.18. Measured different pixel transconductance gain for different aspect ratio of TA at V_{read} = 15V and V_{Bias} = 10.

Bibliography

[1]: 2. F. Taghibakhsh, K. S. Karim, A. Madan, 'Low leakage a-Si:H Thin Film Transistor Deposited on Glass Using Hot-wire Chemical Vapor Deposition', Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, Volume 24, Issue 3, pp. 866-868, 2006.

[2]: J. Jang, "Preparation and Properties of Hydrogenated Amorphous Silicon Thin-Film Transistors", in "Thin Film Transistors", Edited by C. R. Kagan and P. Andry, Marcel Dekker Inc., New York, 2003.

[3]. 5. F. Taghibakhsh, K. S. Karim, 'Hot-wire CVD a-Si TFTs on Plastic Substrate', Proceedings of Material Research Society, vol. 910, A18-02, April 2006.

[4]. F. Taghibakhsh, M. M. Adachi, K. S. Karim, 'Hot-wire Deposited Nanocrystalline Silicon TFTs on Plastic Substrates', Proceedings of Material Research Society, vol. 989, A20-04, April 2007.

[5]: Y. Kuo, "Plasma Etching and Deposition for a-Si:H Thin Film Transistors," J. Electrochem. Soc. 142, No. 7, 2486 (1995).

[6]: http://mvsystemsinc.com/, accessed on: Thursday, May 01, 2008.

[7]: http://www.ajaint.com/whatis.htm, accessed on: Thursday, May 01, 2008.

[8]: Smith, Donald, "Chemical Vaour Deposition", ch. 7, in: Thin-Film Deposition: Principles and Practice, MacGraw-Hill, 1995.

[9]: J. Kanicki and S. Martin, "Preparation and Properties of Hydrogenated Amorphous Silicon Thin-Film Transistors", in "Thin Film Transistors", Edited by C. R. Kagan and P. Andry, Marcel Dekker Inc., New York, 2003.

[10]: P. Servati, K.S. Karim, A. Nathan, "Static characteristics of a-Si:H Dual-Gate TFTs", IEEE Transactions on Electron Devices, 50(4), pp. 926-932, April 2003.

[11]: M. J. Powell, C. Glasse, P. W. Green, I. D. French, and I. J. Stemp, “An Amorphous Silicon Thin-Film Transistor with Fully Self-Aligned Top Gate Structure”, IEEE Electron Device Letters, vol. 21, no. 3, pp. 104-106, March 2000.

[12]: M. Sakamoto, T.Ukita, A. Maeda and S. Ohi, Digest SID’96, p.681, 1996.

[13]: A. Miri, “Development of a Novel Wet Etch Fabrication Technology for Amorphous Silicon Thin-Film Transistors”, Ph.D. Thesis, University Of Waterloo, 1996.

[14]: F. Taghibakhsh, K.S. Karim, “Two-Transistor Active Pixel Sensor for High Resolution Large Area Digital X-ray Imaging” *IEEE Electron Devices Meeting, IEDM 2007,* pp. 1011-1014, December 2007.

5

X-ray Response of the Two-Transistor APS

In this chapter various preparation steps such as: shadow masks for a-Se deposition on packaged devices, high voltage DC source and its connection to the package, test setups for dark and x-ray measurements are described, and results of x-ray measurements on 2T-APS test pixels coated with a-Se detector are presented and discussed.

5.1 Amorphous selenium x-ray photoconductor coating

Aluminum shadow masks were used to cover packaged and bonded dies for amorphous selenium photoconductor coating (Fig 5.1). Packages were sent to University of Saskatchewan (Prof. S. O. Kasap's Lab) for photoconductor coating, where 80 μm of amorphous selenium was thermally evaporated on the test arrays followed by a thin layer of chromium top contact. Thermal evaporation of a-Se takes place at 265 ºC, however, the target substrate is kept at low temperatures (~25 ºC) [1]. Figure 5.1 shows the shadow mask covering of the bond pads, as well as an a-Se coated die.

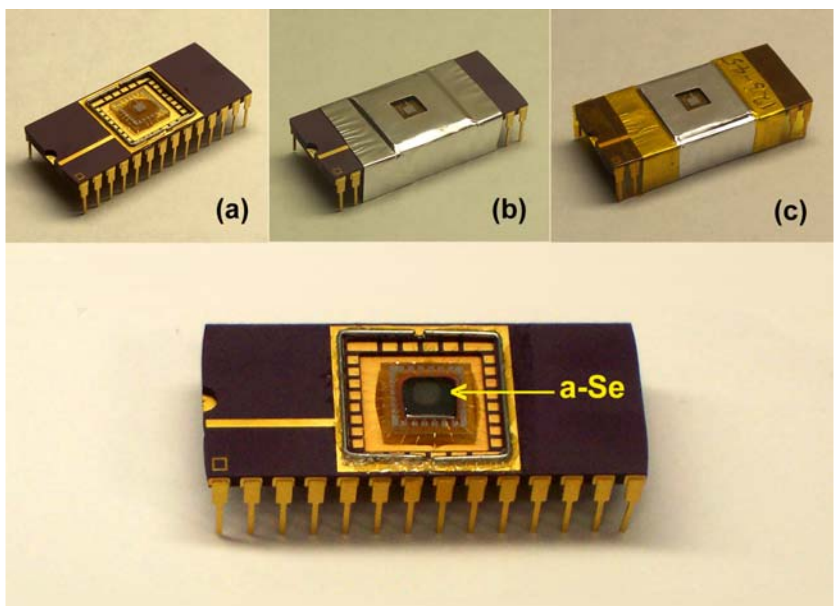


Figure 5.1 (a) spacers provide proper separation of the shadow mask and the die. (b) Shadow mask covered package. (c) High temperature Kapton® tape was used to secure the shadow mask. Amorphous selenium coated package; the chromium top contact is visible as a faint circle on the dark a-Se.

Transconductance gain of the test array pixels were measured before and after a-Se photoconductor deposition (with a 4-month gap in between). Considerable reduction in pixel gain, down to 58% of the initial value was measured. We attribute this gain reduction to degradation of a-Si TFT over time, or possible due to hostile environment of a-Se deposition.

5.2 High Voltage DC Source

As indicated in chapter 1, amorphous selenium photoconductor requires high electric field for effective detection of absorbed radiation. The average amount of energy required to detect an electron-hole pair (EHP), W, has been shown to be a function of electric field bias across the detector [2]:

$$W \approx 6 + 400 / E \tag{5.1}$$

Here E is the electric field in V/μm and W in electron volts. As Eqn. (5.1) suggests, the the average photon energy for producing a detectable pair of carriers is as high as 46 eV at the bias filed of 10 V/μm. One drawback of a-Se is the high voltage required for biasing the photoconductor. For example to absorb most of the x-ray radiation of 120 kVp, the a-Se photoconductor thickness is around 1 mm, which translates to 10,000 V biasing DC voltage.

For the 80 μm deposited a-Se, 800V is needed to bias the photoconductor at 10 V/μm. 240 × 3.3V CR2032 small coin size batteries were used to make two constant (no ripple) high voltage DC sources of each ~ 400V (Fig. 5.2).

By measuring the voltage drop of a 100V (stack of 30 batteries) DC source across a small resistance, the average internal resistance of each battery was calculated to be ~ 25Ω. This results in a total internal resistance of 6 kΩ for the 800V source, which is many orders of magnitude smaller than the photo resistance of a-Se. Therefore, this approach would be suitable for providing long lasting, low noise, ripple free high voltage source for research activities on small detectors.

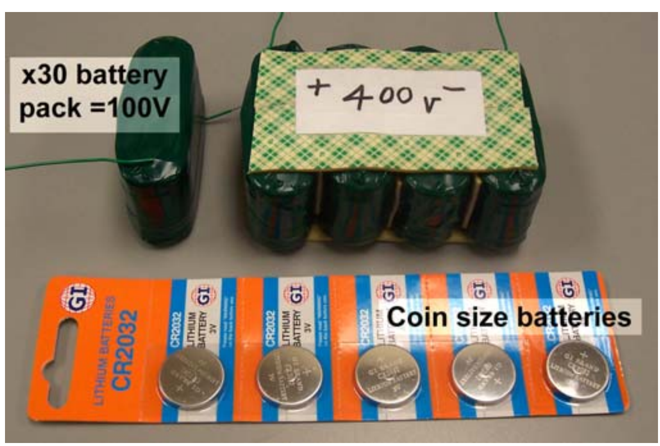


Fig. 5.2. A 400V DC voltage source made up of small 3.3V coin batteries.

5.3 Dark current measurement

In addition to coating the test arrays, a reference detector was also provided for characterization. The test setup of figure 5.3 was used to measure dark current of the photoconductor at different biasing fields. Fig. 5.3 also shows the dark current of the photoconductor as well as the effect of x-ray exposure.

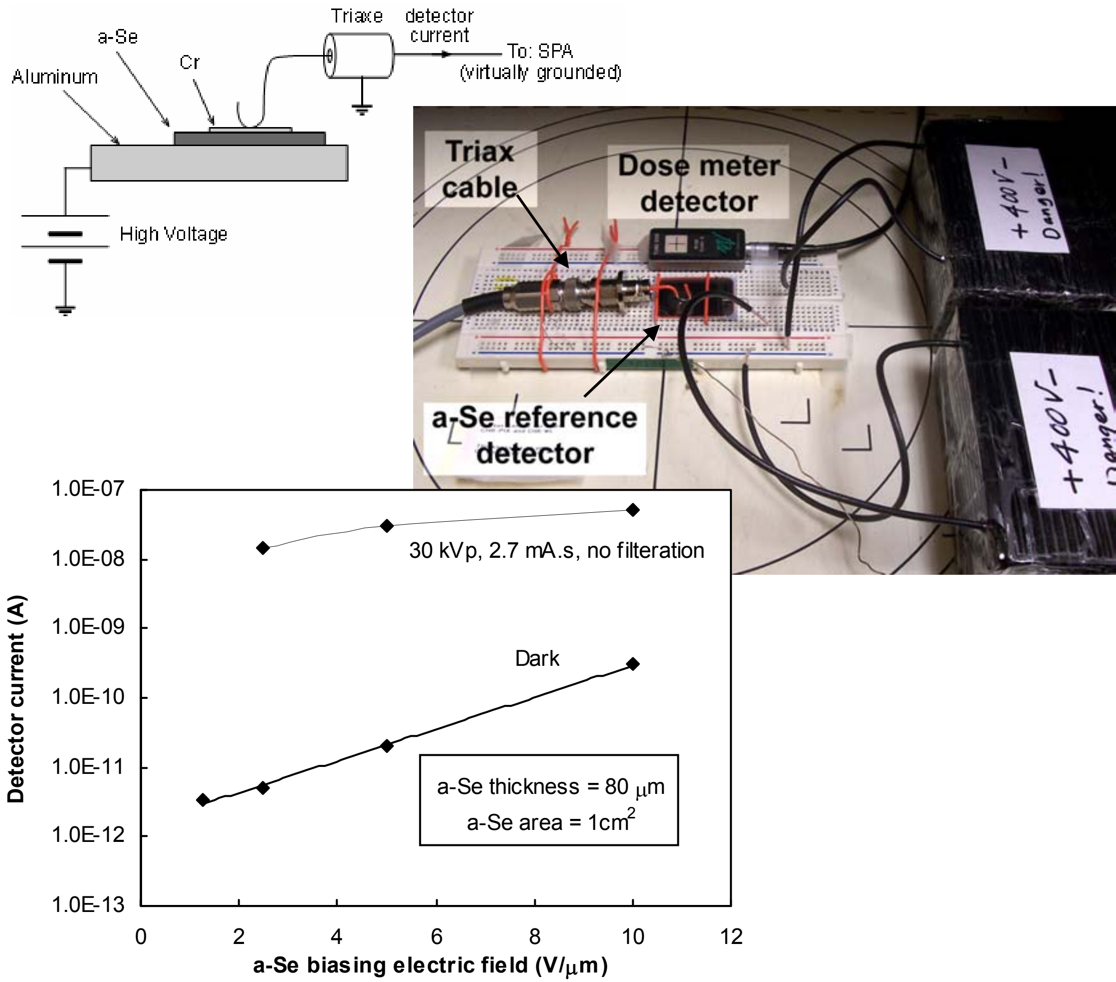


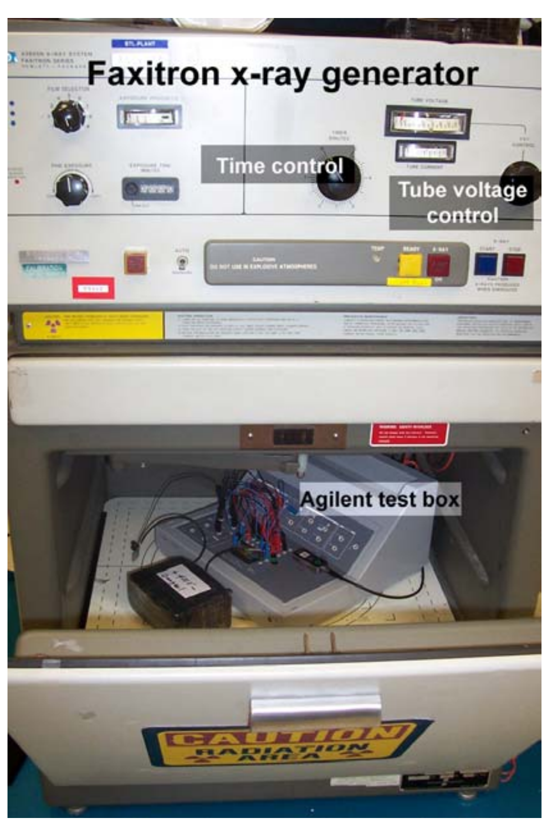
Figure 5.3. The schematic diagram, test setup and results of dark current measurement on the a-Se reference photoconductor. The response of the detector to 2.7 mA.s x-ray exposure at 30kVp is also depicted on the graph.

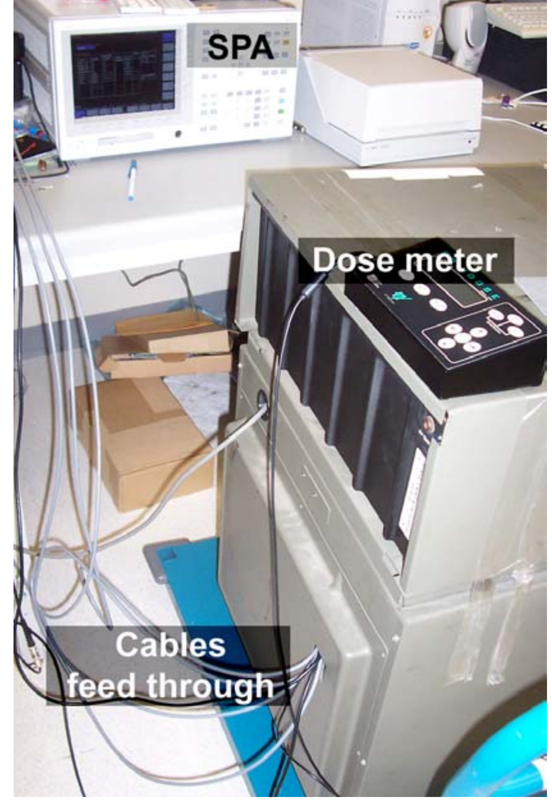
The blocking contacts of a-Se photoconductor were deposited in such a way that electrons are deposited on the bottom electrode rather than the top one which is the common form. This is why the positive high voltage is connected to the aluminum substrate in the diagram of Fig. 5.3. reverse biasing the photoconductor results in excessive dark current. As observed, the dark current increases exponentially with increase of biasing electric field while the radiation current exhibits slower increase rate, resulting in lower signal to noise ratio at higher biasing electric fields.

5.4 X-Ray Measurement

5.4.1 X-ray cabinet and measurement setup

An HP Faxitron 4380N table top x-ray machine (Fig. 5.4) was used for measuring x-ray response of the 2T APS arrays in this research. The machine is equipped with a single phase stationary tungsten anode x-ray tube with tube voltage control of 10 kV to 120 kV, and exposure time control of up to 10 min. However, the mA.s is not controllable and varies between 2.25 to 3.00; increasing with tube voltage. In order to measure the x-ray response of the test pixels, the Agilent® test box was placed inside the cabinet, and cables were routed to the semiconductor parameter analyzer (SPA) from the back of the x-ray cabinet. An RTI® SOLIDOSE dose meter was used to monitor the x-ray exposure.





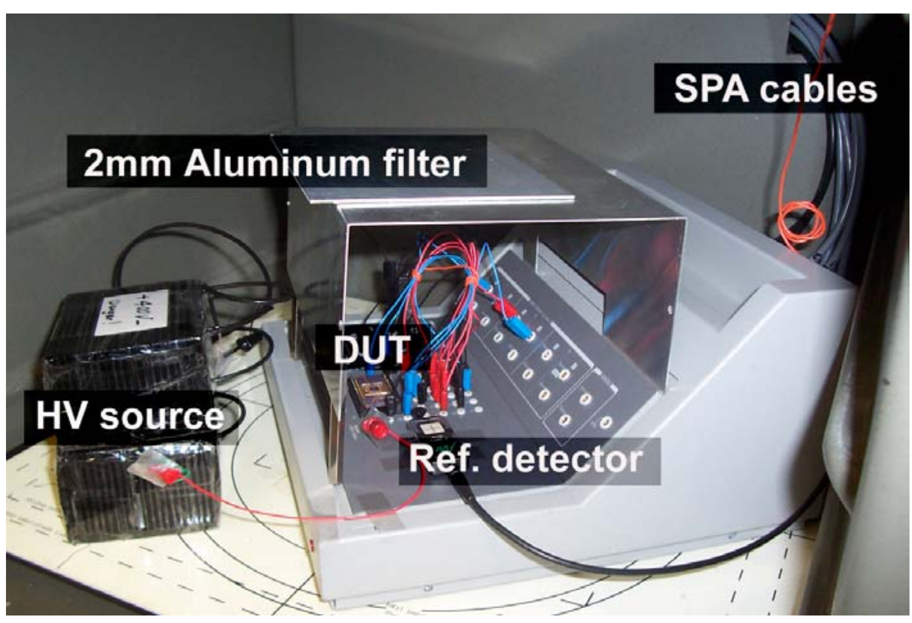


Figure 5.4. (a): The Faxitron x-ray cabinet, with the test box inside. (b) Dose meter and the cables connecting the textbox to the semiconductor parameter analyzer. (c) Inside the cabinet.

It is worth noting that the high voltage was mechanically connected to the top electrode contact using a thin copper wire; care was taken not to shadow on the array though. Figure 5.5. shows the details of high voltage connection.

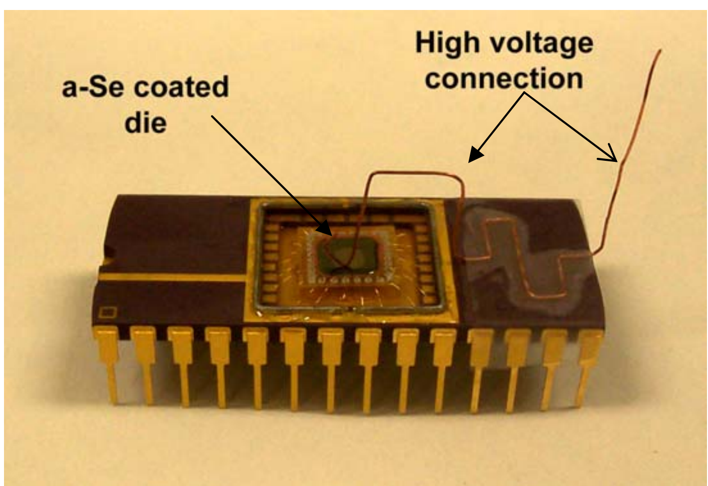


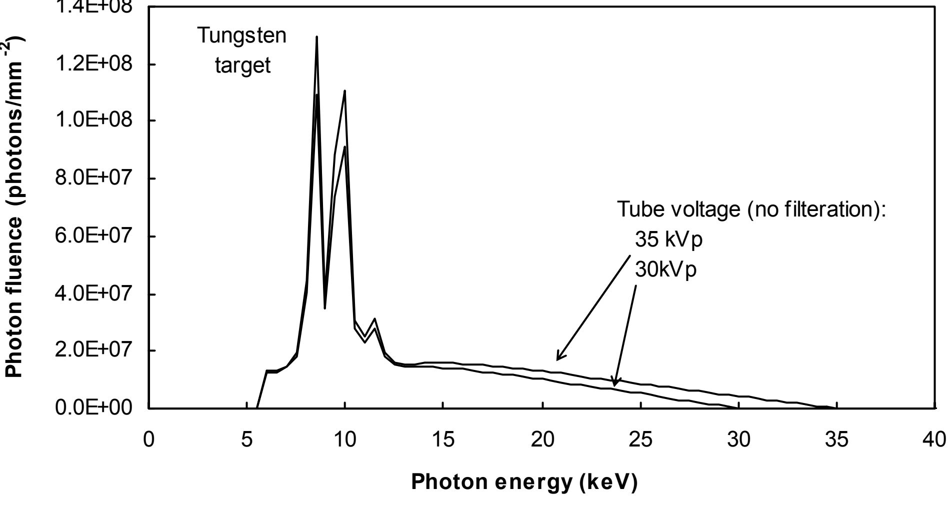
Figure 5.5. A taped copper wire was used to connect the high voltage to the top electrode of a-Se photoconductor coated on the packaged dies.

5.4.2 X-ray spectrum

Two different tungsten target x-ray spectrum, 30 kVp and 35 kVp were used in this study. The radiation was filtered using 2 mm aluminum, basically because the RTI dose meter detector was calibrated with 2 mm aluminum filtration. Figure 5.6 shows non-filtered tungsten spectrum, Φ(E), for the two tube voltages of 30 kV and 35 kV, and compares that to the filtered spectrum. The original tungsten spectrum was downloaded from [3] [4], and the filtered spectrum is calculated from Eqn 5.2. However, the filtered spectrum was generated by X-RAYLIB software and was properly scaled to produce the measured dose by the reference RTI detector at the distance of 50 cm from the x-ray tube, where the device under test was mounted.

$$\Phi(E)\Big|_{Filtered} = \Phi(E)\, e^{-\mu(E)\cdot t_D} \tag{5.2}$$

Here, E is the photon energy, $\Phi(E)$ is the radiation spectrum in photons fluence per energy interval, and $\mu(E)$ is the linear attenuation coefficient of the filter material, and t_D is the filter thickness.



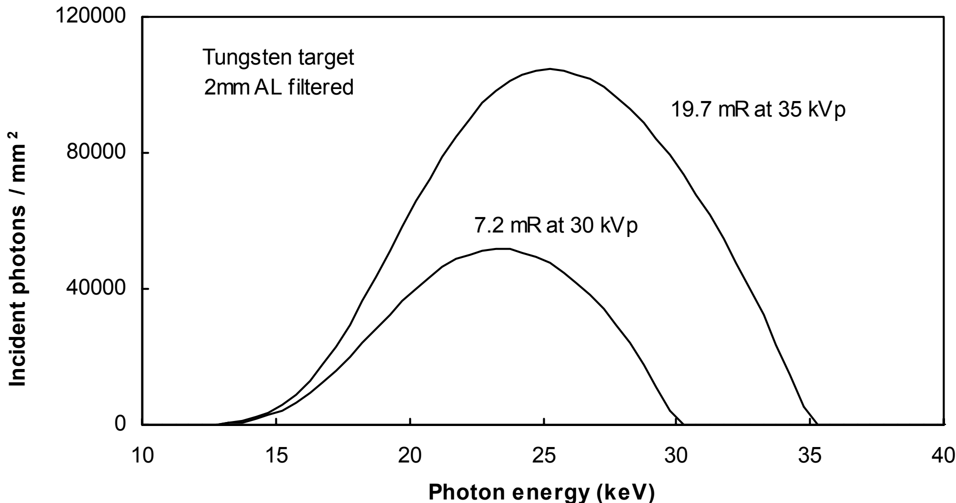


Figure 5.6. (a): Tungsten non-filtered spectrum, (b): tungsten spectrum filtered by 2 mm Al.

5.4.3 Detective Quantum Efficiency

Not all incident x-ray photons are absorbed in the detector, if it is not thick enough to stop the high energy radiation. The detective quantum efficiency (QE), expressed in Eqn. 5.3, provides a measure of how effectively a detector absorbs the radiation.

$$QE = \frac{\int_{E=0}^{E_{\max}} \Phi(E)\left(1 - e^{-\mu(E)\cdot t_D}\right) dE}{\int_{E=0}^{E_{\max}} \Phi(E)\, dE} \tag{5.3}$$

Equation 5.3 that measure how much of the incident radiation is attenuated by the detector, was numerically calculated for spectrums of Fig. 5.6.b, and detector material of a-Se with thickness of 80 μm. The result is listed in table 5.1. Energy dependent mass attenuation coefficient of a-Se and Al which were used to calculate the QE, are shown in Fig. 5.7.

Table 5.1. Calculated DQE of a-Se photoconductor for 2 mm Al filtered tungsten spectrum

Tungsten x-ray spectrum	DQE (80 µm a-Se)
30 kVp	69 %
35 kVp	60 %

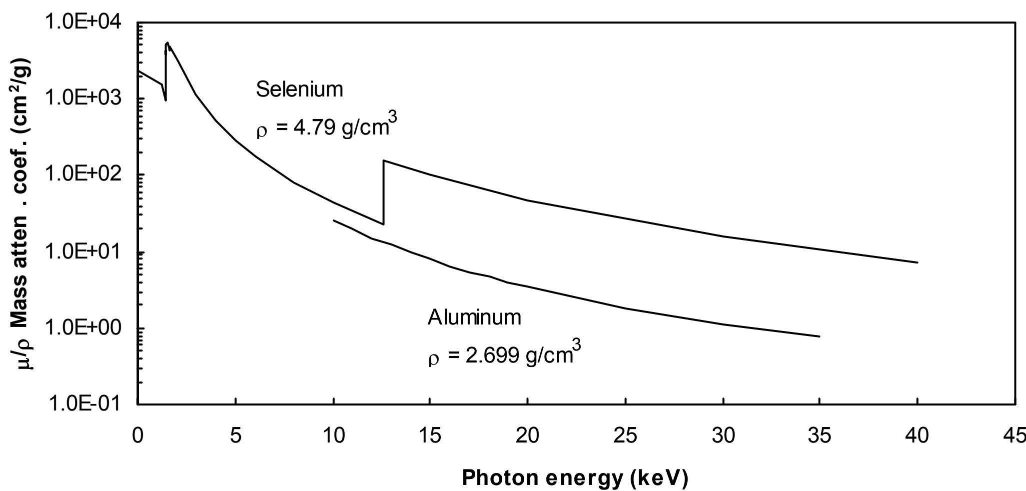
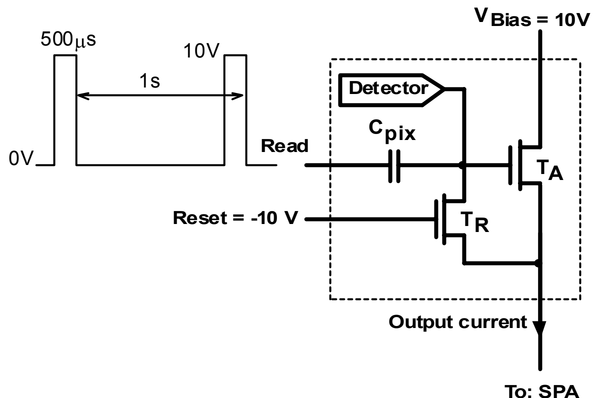


Figure 5.7. Mass attenuation coefficient of a-Se and aluminum versus x-ray photon energy.

5.4.4 X-ray response

A 150 µm pixel pitch 2T APS test array was used in the experiment. The pixel was biased by a DC voltage of 10V, and by applying a 10V pulse with frequency of 1 Hz, and pulse width of 500 µs, the output current of one pixel was sampled at the rate of 1 sample per second. Successful readout rates of up to 100 samples per second (the maximum limit of the SPA used) were examined, however results for 1 sample per second is reported

here. The a-Se photoconductor was biased at 5 V/µm as well as 10 Vµm. Figure 5.8 shows the schematic diagram of the test setup, and the response of the test 2T APS pixel to 7.2 mR and 19.7 mR of x-ray exposure at 30 kVp and 35 kVp respectively.



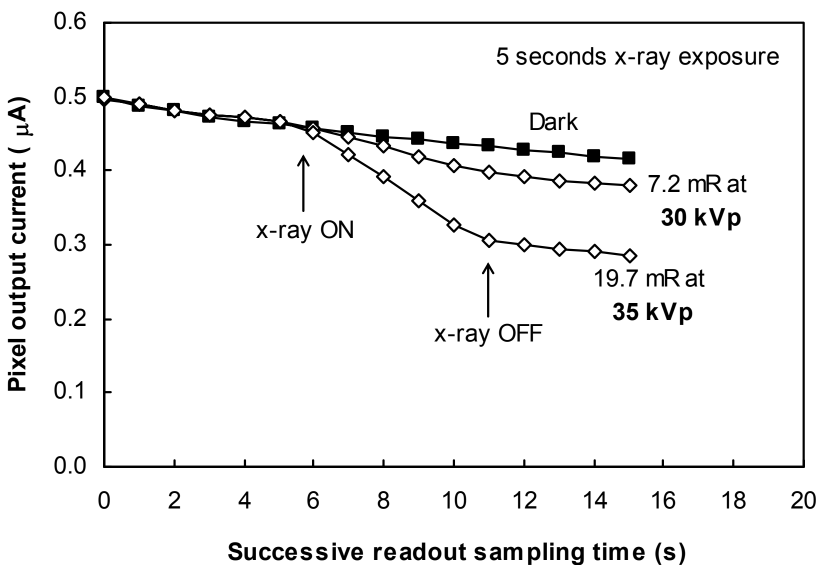


Figure 5.8. Readout sampling diagram and the x-ray response of one 2T APS pixel with 150µm pixel pitch for two different x-ray spectrum.

The pixel is initially reset (at t = 0s) by applying a positive 5 V to 10 V pulse to the reset line (gate of T_R). During the readout time, *Reset* was kept at -10 V to ensure the cgarge gate is floating. The x-ray (with spectrum depicted in Fig. 5.5.b) was delivered to the pixel in 5 seconds, during which, the pixel was constantly being read. The a-Se is biased with negative voltage connected to the top electrode. In this configuration, electrons are

deposited on the pixel capacitance as the result of x-ray absorption in the photoconductor, which reduces the voltage of the charge gate (gate of T_A), resulting in reduction of output current. The large slope for the graph for dark current indicates a large level of dark current, which can be, in part, due to not perfect light-tight condition inside the x-ray cabinet too.

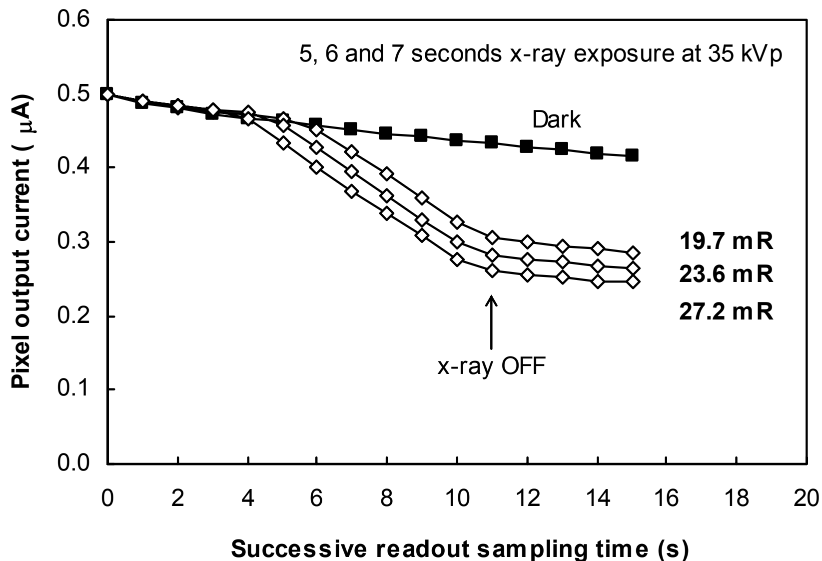


Figure 5.9. X-ray response of the 2T-APS to different dose levels of the same x-ray spectrum (35 kVp)

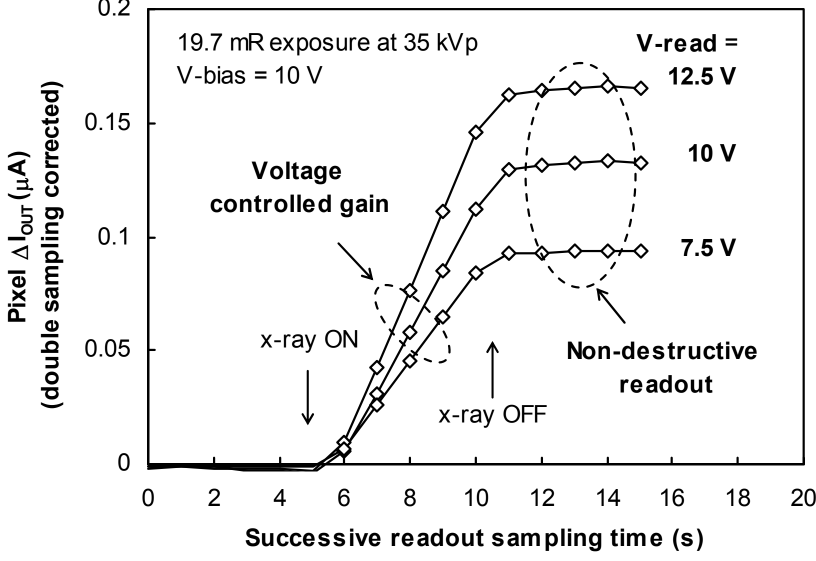


Figure 5.10. Illustration of double sampling correction, as well as voltage controlled pixel gain.

Response of the 2T APS pixel to different dose levels of the same spectrum is shown in Fig, 5.9, and, Fig. 5.10 illustrates double sampling (DS) corrected output values (readout values are subtracted from dark current), as well as capability of programming the pixel gain using readout sampling pulse height. Measured data shoes that 5 volts increase in the voltage level of the *Readout* sampling pulse from 7.5 V to 12.5V results in 75 % increase in pixel gain from 0.095 μA/V to 0.165 μA/V.

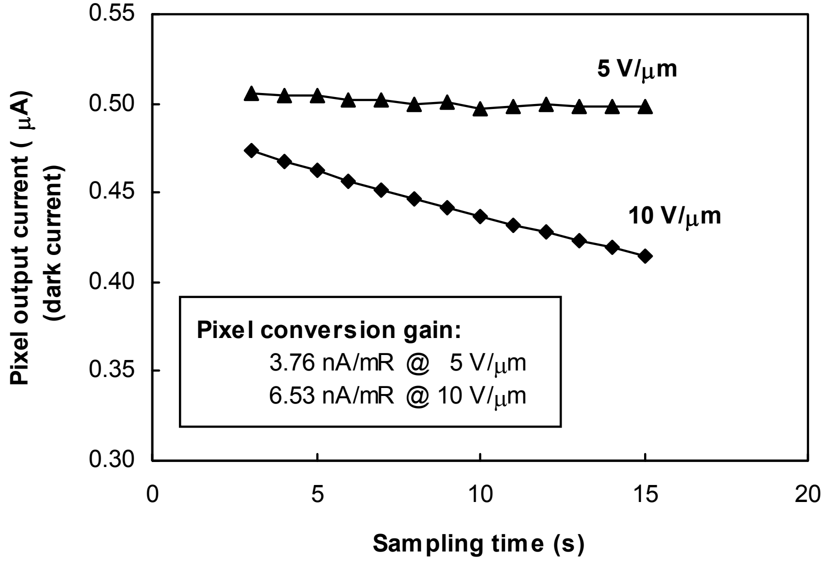


Figure 5.11. Effect of a-Se biasing field on dark current response and pixel x-ray conversion gain.

To evaluate the effect of photoconductor biasing electric field on the x-ray response of the pixel, similar measurements were carried out when a-Se was biased at at 5 V/μm. Fig. 5.11 shows that effect of dark current is considerably improved (more than 7 times less dark current). The pixel conversion gain however, is not reduced to half, as expected, when the electric field is made one half.

5.4.5 X-ray Sensitivity

The sensitivity of the output current to the incident x-ray radiation is calculated based on photoconductor deposited charge, Q_p, on the pixel storage capacitance. Intuitively the pixel charge can be calculated from Eqn 5. 4 [5], in which A_P is the pixel area, and FF is the pixel fill factor.

$$Q_P = A_P \cdot FF \cdot \int_{E=0}^{E_{\max}} \left(\frac{\mu_{en}(E)}{\mu(E)}\right)\left(\frac{E}{W_{\pm}}\right)\Phi(E)\left(1-e^{-\mu(E)\cdot d}\right)dE \tag{5.3}$$

For the pixel under test, A_P and FF are 0.0225 mm^2, and 88% respectively. Pixel deposited charge, Q_p, was calculated for four different exposures and measured change in the output current was measured for different exposures as well as different readout pulse height. Figure 5.12 shows the x-ray sensitivity or the gain of the pixel. It is observed that the sensitivity (gain) of the pixel is programmable, which means the pixel gain can be adapt to the level of incoming radiation, should more amplification or attenuation be necessary.

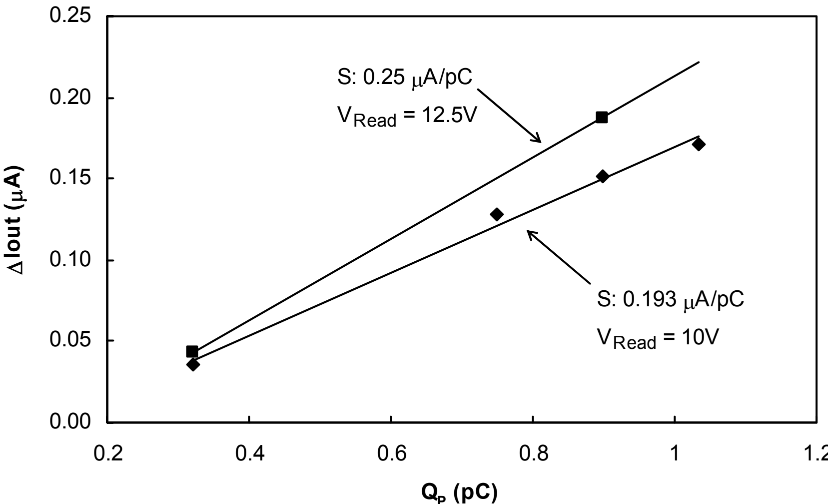


Figure 5.12. Measured x-ray sensitivity of the pixel. The gain (sensitivity) is controlled by readout pulse.

5.5 Summary

Two-transistor amplified pixels integrated with amorphous selenium x-ray photoconductor were successfully tested for different x-ray exposures at two different photoconductor biasing electric field of 10 V/µm, and 5 V/µm. With calculated QE of 69% and 60% for 2 mm aluminum filtered tungsten spectrum of 30 kVp and 35 kVP respectively, a 150 µm pixel pitch 2T APS showed a sensitivity of 0.25 µA/pC at 12.5V read voltage pulse height. The sensitivity of 0.25 µA/pC suggests if the pixel output is integrated over time, there would be larger than unity charge gain after 1/0.25, or 4µs. For example if the output current is integrated for 20 µs, the pixel charge gain would be equal to 5. the other interpretation of this pixel gain is that for a readout time of 5 µs, almost equal to PPS output signal is generated, however, the frame rate could be as high as 100 frames per second for a 2000 row imager.

In addition, measured conversion gains of 3.76 nA/mR and 6.53 nA/mR at 5 V/µm and 10 V/µm respectively, indicates dynamic range control capability of the pixel using photoconductor biasing electric field (see Fig. 5.11). Here, dropping the field from 10 V/µm to 5 V/µm results in 74% increased dynamic range (ratio of the conversion gains)

Measurements also verified programmable pixel gain capability of the 2T APS using the readout voltage pulse height (see Fig. 5.10). Here, 5 V increase in the pulse height resulted 75% increased pixel transconductance gain.

Bibliography

[1]: R.E. Johanson, S.O.Kasap, J.A. Rowlands, B. Polischuk, "Metallic electrical, contacts to stabilized amorphous selenium for use in X-ray image detectors," Journal of Non-Crystalline Solids, 227-230, pp. 1359-1362, 1998.

[2]: G. Belev, S.O. Kasap, "Amorphous selenium as an X-ray photoconductor", Journal of Non-Crystalline Solids, vol. 345-346, pp. 484-488, October 2004.

[3]: ftp://ftp.aip.org/epaps/medical_phys/E-MPHYA-24-1863/, accessed on: Thursday, May 01, 2008.

[4]: "X-ray production, interaction, and detection in diagnostic imaging" by J. M. Boone, in "Handbook of Medical Imaging", Volume 1. Physics and Psychophysics, ch. 1, pp. 331-367, Edited by J. Beutel, SPIE publications, 1999

[5]: W. Zhao, J. Law, D. Waechter, Z. Huang, J.A.Rowlands, "Digital radiology using active matrix readout of amorphous selenium: Detectors with high voltage protection," Medical Physics, 25(4), p. 539-549, 1998.

6

Conclusion and Contributions

In this thesis we have developed a novel thin film device, a charge-gated TFT structure for use as a switched amplifier/driver for high resolution imaging applications. The reported charge-gated TFT enables high resolution sensor readout circuits including single-transistor and two-transistor APS pixel architectures for large area digital imaging applications.

A new generation of active pixel sensor readout circuits is introduced, particularly for use in high resolution sensor arrays. The novel APS circuits are based on two-transistor architectures, in which the amplifier/driver transistor is itself switched ON and OFF, eliminating the need for a separate switched transistor for addressing. This work demonstrates that employing fewer on-pixel transistors improves detector array resolution and signal-to-noise ratio (SNR) by virtue of both, an increase in the pixel amplification gain and a reduction in the input referred noise.

Alternate designs of 2T APS were investigated. It was shown two-transistor pixel architectures using a gate-switched amplifier design that employs charge-gated TFTs, has a key advantage over drain or source switched architectures because they can be operated by regular gate drivers in contrast to the other 2T architectures that require high current drivers. This is of particular importance for incorporating the new pixel architecture into the current technology of flat panel detectors. The charge gated design also overcomes the speed limitations associated with repeatedly charging and discharging the large column bus capacitance for source and drain switched 2T pixels.

The two-transistor APS using charge-gated TFTs was successfully implemented in test arrays with 100 μm pixel pitch as the smallest a-Si APS reported to date. The 2T APS

was also integrated with a-Se direct x-ray detector. Voltage programmable pixel gain control, and non destructive readout capability of the 2T APS was verified by x-ray response measurements, indicating the possibility to adapt the on-pixel gain of the 2T APS to the incident x-ray dose level.

Additionally, by introducing multiple-row resetting technique as a new driving scheme for APS imagers, it is possible to operate active pixel based imagers at frame rates beyond that of PPS based imagers for real time imaging.

The original contributions of the research presented in this thesis to the field of large area digital imaging are listed below:

Charge-gated thin film transistor:

- A single switched amplifier/driver device as the readout circuit for high resolution sensor arrays.

Two-transistor active pixel sensor architectures (source, drain and gate switched designs):

- Reduced transistor count per pixel, pixel size and complexity for higher detector resolution and improved fabrication reliability.
- Improved input referred noise because of fewer on pixel noise sources, as well as increased pixel transconductance gain.
- Alternative drain switched architecture for fewer biasing lines per pixel in order to further reduction in pixel size and complexity

High resolution, fast frame rate active pixel sensor based X-ray imager:

- Integration of amorphous selenium direct x-ray detector with 2T APS and successful demonstration of voltage controlled pixel gain.
- Multiple-row resetting driving scheme for increased frame rate for real time imaging

Appendix A

List of Scholarly Contributions

First-author referred publications

Materials and Device related publications

1. F. Taghibakhsh, I. Khodami, K. S. Karim, 'Characterization of Short Wavelength Selective a-Si MSM Photoconductors for Large Area Digital Imaging', IEEE Transaction on Electron Devices, vol. 55, no. 1, pp. 337-342, January 2008.

2. F. Taghibakhsh, K. S. Karim, A. Madan, 'Low leakage a-Si:H Thin Film Transistor Deposited on Glass Using Hot-wire Chemical Vapor Deposition', Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, Volume 24, Issue 3, pp. 866-868, 2006.

Refereed Conference Publications

3. F. Taghibakhsh, M. M. Adachi, K. S. Karim, 'Hot-wire Deposited Nanocrystalline Silicon TFTs on Plastic Substrates', Proceedings of Material Research Society, vol. 989, A20-04, April 2007.

4. F. Taghibakhsh, K. S. Karim, 'Fabrication and Characterization of Nickel Amorphous Silicon Metal-Semiconductor-Metal Photoconductors', Proc. IEEE CCECE, pp. 1664-1667, April 2007.

5. F. Taghibakhsh, K. S. Karim, 'Hot-wire CVD a-Si TFTs on Plastic Substrate', Proceedings of Material Research Society, vol. 910, A18-02, April 2006.

Device and Circuit related publications

6. F. Taghibakhsh, K. S. Karim, 'Charge-Gated Thin Film Transistor for Large Area High Resolution Imaging Applications', IEEE Electron Device Letters, April 2008, ***submitted.***

7. F. Taghibakhsh, K. S. Karim, 'Two-Transistor Amplified Pixel Readout Circuits in Amorphous Silicon Technology for High Resolution Digital Imaging', IEEE Transaction on Electron Devices, March 2008, ***in press.***

8. F. Taghibakhsh, K. S. Karim, 'High Dynamic Range 2-TFT Amplified Pixel Sensor Architecture for Digital Mammography Tomosynthesis', IET Circuits Devices and Systems, vol. 1, issue 1, pp. 87-92, February 2007.

Refereed Conference Publications

9. F. Taghibakhsh, K. S. Karim, 'Two-Transistor Active Pixel Sensor for High Resolution Large Area Digital X-ray Imaging', International Electron Devices Meeting, IEEE - IEDM, pp. 1011-1014, December 2007.

Medical Imaging related publications

10. F. Taghibakhsh, K. S. Karim, G. Belev, S. O. Kasap, 'X-Ray Detection using a Two-Transistor Amplified Pixel Sensor Array Coupled to an a-Se X-Ray Photoconductor', IEEE Sensors Journal, April 2008, ***submitted***.

Refereed Conference Publications

11. F. Taghibakhsh, K. S. Karim, 'High Resolution Amplified Pixel Sensor Architectures for Large Area Digital Mammography Tomosynthesis', Proceedings of SPIE, Physics of Medical Imaging, vol. 6913, pp. 6913R1-9, February 2008. ***(Honorable Mention Poster Award)***.

12. F. Taghibakhsh, K. S. Karim, 'Amplified Pixel Architectures for Low Dose Computed Tomography using Silicon Thin Film Technology', Physics of Medical Imaging, Proceedings of the SPIE, Volume 6510, pp. 65103W, February 2007. ***(Honorable Mention Poster Award)***.

Collaborative publications

13: K.S. Karim, M.H. Izadi, F. Taghibakhsh, G. Sanaie, 'Intelligent Pixel Architectures for Digital Medical Imaging Applications', ECS Transactions, 8(1), pp. 289-293, July 2007

14: K. S. Karim, G. Sanaie, T. Ottaviani, M. H. Izadi, F. Taghibakhsh, 'Amplified Pixel Architectures in Amorphous Silicon Technology for Large Area Digital Imaging Applications', Journal of Korean Physical Society, vol. 48(1), (2006).

Refereed Conference Publications

15: M. M. Adachi, F. Taghibakhsh, K. S. Karim, 'Structural Analysis of Nanocrystalline Silicon Prepared by Hot-wire Chemical Vapor Deposition on Polymer Substrates', Proceedings of Material Research Society, vol. 989, A22-03, April 2007.

16. G. Sanaie, F. Taghibakhsh, K. S. Karim, 'Low noise, high dynamic range pixel architecture in amorphous silicon technology for diagnostic medical imaging applications', Proceedings of the 29th Canadian Medical and Biological Engineering Conference, June 2006.

17. I. Khodami, M. M. Adachi, M. Malhotra, F. Taghibakhsh, J. A. Rowlands, K. S. Karim, K. L. Kavanagh, 'Light Induced Degradation in Amorphous Silicon Photodiodes', Proceedings of SPIE, Medical Imaging, vol. 6142, pp. 61422U, February 2006.

Appendix B

Selected Papers

Two-Transistor Active Pixel Sensor for High Resolution Large Area Digital X-ray Imaging, International Electron Devices Meeting, IEEE - IEDM, pp. 1011-1014, December 2007.

Amplified Pixel Architectures for Low Dose Computed Tomography using Silicon Thin Film Technology, Physics of Medical Imaging, Proceedings of the SPIE, Volume 6510, pp. 65103W, February 2007. **(Honorable Mention Poster Award)**.

Characterization of Short Wavelength Selective a-Si MSM Photoconductors for Large Area Digital Imaging, IEEE Transaction on Electron Devices, vol. 55, no. 1, pp. 337-342, January 2008.

Two-Transistor Active Pixel Sensor for High Resolution Large Area Digital X-ray Imaging

Farhad Taghibakhsh[1], Karim S. Karim[1,2]

[1] School of Engineering Science, Simon Fraser University
Burnaby, British Columbia, V5A 1S6, Canada

[2] Electrical & Computer Engineering Department, University of Waterloo,
Waterloo, Ontario, N2L 3G1, Canada

Abstract

A novel architecture for active pixel sensor (APS) arrays with only two thin film transistors (TFTs) is presented, and a new driving scheme for minimizing the threshold voltage metastability problem and increasing frame rate is discussed. The fewer number of on-pixel elements, and reduced pixel complexity, results in a smaller pixel pitch and increased pixel gain, and makes the presented APS architecture promising for high resolution, high speed imaging modalities such as digital mammography tomosynthesis.

Introduction

Low noise APS architectures based on current mode amplifier designs were previously reported for large area medical imaging in amorphous silicon (a-Si) technology (1, 2). However, they were based on a three-transistor (3T) (Fig. 1.a) approach that results in large pixel size because of the large size associated with a-Si TFTs. This research work introduces a two-transistor (2T) pixel architecture (Fig 1.b) and presents results on in-house fabricated test arrays with a pixel pitch of 100 μm. The proposed architecture achieves a smaller pixel size while providing similar functionality to its 3T counterpart. Unlike other 2T architectures already reported (3), the architecture does not require any modification in the standard driving circuits and can be used as either a current or voltage mediated APS, depending on the readout circuitry connected.

Although the pixel architecture is presented for use with a-Si TFTs in this research, the applications of the proposed 2T pixel are not limited to a-Si technology or medical imaging and can potentially be used for high resolution digital imaging applications using crystalline or polycrystalline silicon technologies.

Two transistor pixel architecture and operation

A. Pixel architecture

In the 2T APS architecture, T1 operates as a switched amplifier, integrating functions of both the READ and AMP TFTs of the 3T design. The 3T APS architecture and the novel 2T pixel circuit architectures are shown in Fig. 1. Compared to the 3T pixel architecture, the READ (or row select) transistor has been removed from the pixel in the 2T design, and the read pulse is directly applied to the gate of T1 through the pixel capacitor, C_{pix}. The READ (row select) TFT in the 3T pixel appears as a degenerate resistor in the source of the AMP TFT, which tends to reduce the overall transconductance gain of the pixel, G_m. In order minimize its ON-state resistance; the READ TFT is usually made as large as the AMP TFT. In contrast to its 3T counterpart, removing the READ TFT not only considerably reduces pixel area and complexity, but also results in increased pixel gain. Effects of removing the READ (row select) transistor on G_m, its variations and V_T shift are more investigated in details in subsequent sections.

B. Reset and integration

The voltage on the gate of T1 is set to zero volts (or a small positive voltage below the threshold voltage, V_T) in the reset phase, prior to integration (see Table 1).

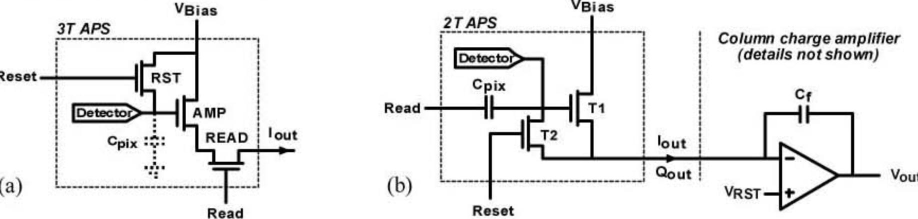


Fig. 1. The classical three-transistor APS architecture (a), and the novel two-transistor multimode APS pixel design connected to a column charge amplifier (b)

TABLE 1. DRIVING SIGNALS FOR OPERATING 2T APS IMAGER. PEAK OF VOLTAGE PULSES ARE LISTED IN LEVEL COLUMN. READ AND RESET PULSE WIDTH ARE AS LOW AS 10-30 µS.

	Resetting	Integration	Readout	Level
Read				5 to 20 V
Reset				15 V
V_{RST}				0 or < V_T
T1-T2	OFF-ON	OFF-OFF	ON-OFF	

The zero (or below V_T) voltage at gate of T1 ensures T1 is OFF during reset and integration which isolates the integrating pixels from the output lines of the other pixels for proper operation of the imager array. A zero V_{GS} during the reset and integration phase also contributes to a reduced V_T shift associated with a-Si devices (4).

C. Readout

To read the pixel value, a voltage pulse with a positive edge is applied to the pixel capacitor. Positive charge is induced on the gate of T1 and depending on the values of the reset, bias, and read pulse voltages, T1 is biased in saturation or linear mode. At the end of the output sampling time, the voltage on the read line drops to zero, and the negative voltage change on C_{pix} removes the charge that had been deposited on the gate of T1, restoring the gate voltage to its value before reading.

In the readout phase when the gate-source voltage (V_{GS}) is higher than V_T, T1 experiences threshold voltage shift, however, the negative voltage that appears between gate and drain (V_{GD}) of T1 (since the source of T1 is grounded in 2T pixel) reduces the effect of the positive V_{GS} on V_T (4).

D. Multimode operation

In the two-transistor pixel architecture of Fig.1.b, T2 serves as the switch for resetting the gate voltage of T1 prior to integration. Also, connects the detector node to the output line as in passive pixel sensor (PPS) architectures, therefore, the resetting charge can be integrated as the pixel is being reset in the resetting phase, to implement PPS operation in the 2T pixel.

Pixel transconductance gain

Taking g_m and R_{ds} to be the transconductance and drain-source resistance of a TFT respectively, (1) and (2) represent the circuit transconductance, G_m, of the 3T and 2T pixels.

$$G_{m\,3T} = \frac{g_{m\,AMP}}{1 + g_{m\,AMP} R_{ds\,READ}} \quad (1)$$

$$G_{m\,2T} = g_{m\,T1} \quad (2)$$

Equations (3) and (4) define the gate-source voltage of AMP and T1 TFTs (see Fig. 1) in the readout mode, where V_{RST} and C_G are the reset voltage of the gate of AMP ($V_{Bias} - V_T$), and gate capacitance of T1, respectively.

$$V_{GS\,AMP} = V_{SET} - I_D R_{ds\,READ} \quad (3)$$

$$V_{GS\,T1} = V_{READ} \frac{C_{pix}}{C_{pix} + C_G} \quad (4)$$

To have similar output current levels for the 3T and 2T pixels, the gate-source voltage of AMP and T1 need to be equal, (where $V_{GS\,AMP} = V_{GS\,T1} = V_{GS}$), which results in the same g_m for AMP and T1, and consequently, a larger G_m for 2T pixel. However, as shown in (1), the negative feedback inherent in the 3T architecture mitigates the effect of changes in V_T on the pixel G_m. This compensation effect can be replicated for the 2T pixel by placing a degenerate resistor at each column, where the output line connects to the amplifier.

Fabrication and measurements

2T APS test arrays were implemented using a-Si top-gate double dielectric layer TFTs at our in-house fabrication facilities using a four-mask process for the TFT backplane (Fig. 2). With the aspect ratio of T1 equal to 10, and minimum feature size of 10 µm, pixel pitch of 100 µm was realized. Characteristic measurements show high output current modulation by V_{Bias} (Fig. 3.a) that is caused by charge injection to the floating gate of T1.

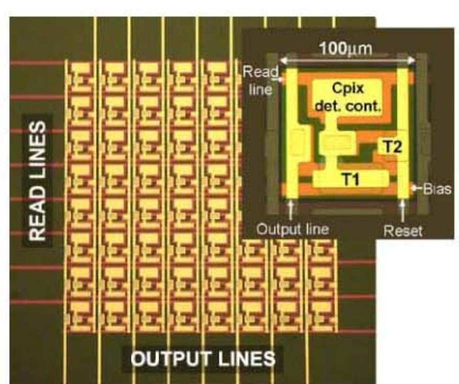
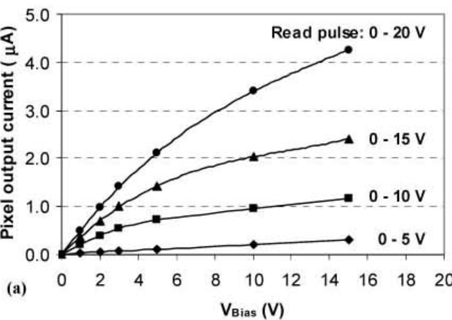


Fig. 2. Die micrograph of a test 8×8 two-transistor APS array (pixel pitch: 100µm, W/L_{T1}: 10), in-house fabricated using a 4-mask process for top-gate TFTs backplane (the inset, a highlighted magnified pixel, shows details of the 2T pixel architecture). Two more masks are used to pattern the x-ray detector pad on top of Cpix (det. cont.) which yield 50% or 81% fill factor, for a non-overlapping or fully overlapped detector respectively.



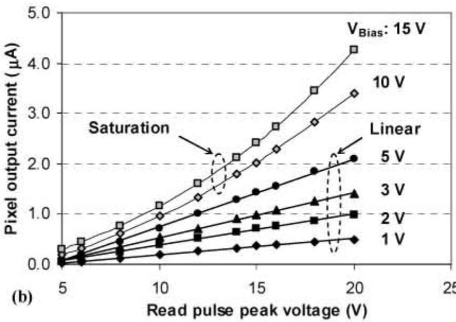


Fig. 3. Measured output characteristics (a), and transfer characteristics (b) of the 2T pixel.

Transfer characteristics (Fig. 3.b) show high linearity of pixel response for low values of V_{Bias}, as well as highlighting the gain programmable capability of the pixel. Transconductance gain of 2T pixels with different aspect ratio of T1 and constant C_{pix} were are shown in Fig. 4. Measurements indicated that the gain of the 2T pixel is immune to gate length scaling, because, as T1 becomes smaller, more of the read voltage drops across the shrinking gate capacitance than the constant C_{pix}. For example, gain of 0.5 µA/V for W/L_{T1} of 20, drops to only 0.3 µA/V (instead of 0.25 µA/V) for W/L_{T1} of 10.

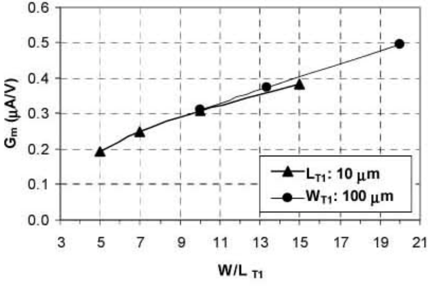


Fig. 4. Measured pixel transconductance gain for different aspect ratio of T1 (V_{bias}: 10V, Read pulse: 0-15V).

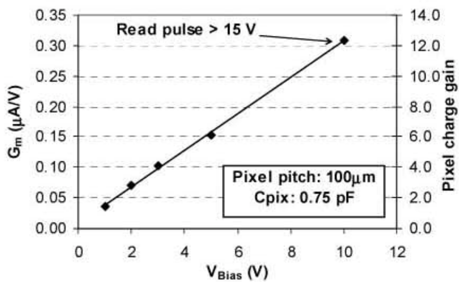


Fig. 5. Pixel transconductance and charge gain control by the bias voltage. Readout time for charge gain measurements = 30 µs.

From the other hand, when increasing gate width, the gate capacitance becomes larger and less of the read voltage drops across it, compared to that of C_{pix}, Which results in less pixel gain. For example, gain of 0.2 µA/V increases to only 0.3 µA/V (instead of 0.4 µA/V) when W/L_{T1} increases from 5 to 10.

The gain control capability of the 2T APS is illustrated in Fig. 5, where measured pixel transconductance and charge gains are plotted against the bias voltage. Charge gain of 12 was obtained for readout time of 30µs and a biasing voltage of 10 V. Charge gain of the APS shows how much the detector signal is amplified compared to PPS. Even for V_{Bias} of 1V, the measured charge gain is above unity. The reading method employed temporarily deposits charge on the gate of T1 but does not destroy the signal charge already deposited by the detector. This is necessary for the double sampling technique to correct fixed pattern noises associated with variations in pixel characteristics in large area imagers. The output current was successively sampled after resetting the pixel at the rate of 20 samples per second and the result is shown in Fig. 6 for different reset voltages.

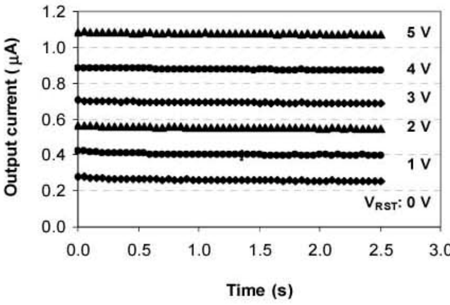


Fig. 6. Successive readouts of the output current after resetting with different voltages shows the new readout method does not destroy the signal, and therefore double sampling technique can be used to remove fixed-pattern noises.

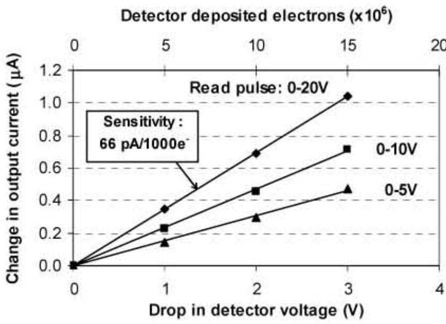


Fig. 7. Measured Changes in the output current of the pixel versus changes in detector voltage, representing the actual performance of APS.

Changes in pixel output current versus the drop in the detector voltage was measured and is shown in Fig. 7. This graph represents the actual APS operation of translating detector deposited charges to a constant output current flow. Here, the pixel gain is controlled by the read voltage because it determines the biasing point of T1. The sensitivity at 20V read voltage was extracted to be 66 pA/1000 electrons. For an integration time of 30 µs, the 66 pA builds ~2 mV on a 1 pF charge amplifier feedback capacitor, which is detectable, and also comparable to those from reported 3T APS test arrays (1). Given the fact that the electronic noise of current mediated APS architectures can be less than 1000 electrons, the fabricated pixels are considered quantum noise limited (3, 5).

High readout frame rates are often desirable, but both resetting and readout times are the limiting factors. By reducing readout time at the expense of less charge gain, and defining a resetting window (multiple row resetting) to break down the resetting time, high frame rates are obtained. A slight modification of the pixel layout is required to provide a separate resetting voltage (Fig. 7). For example, the charge gain of 12 drops to 3 if the readout time is decreased by a factor of four, from 30µs to 7.5µs. Now, instead of resetting each row for 30µs, 4 rows are simultaneously reset for only 7.5µs. The whole resetting window and the row being read, sweep the array one row at a time, each 7.5µs, which results in four fold higher readout frame rate, while it ensures each row is reset for a combined time of 30µs for proper operation of the imager.

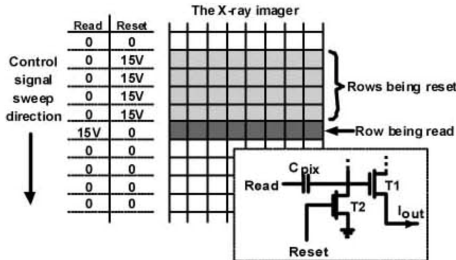


Fig. 8. Higher frame rates are obtained by shortening the readout time and multiple row resetting. This technique is possible only is a separate resetting voltage is provided (source of T2 is at zero volts).

Conclusion

A novel two-transistor active pixel sensor architecture was introduced. Experimental results from in-house fabricated test a-Si TFT arrays with a pixel pitch of 100 µm were presented, and an alternate driving scheme for a high readout frame rate was discussed.

In addition to being smaller in size, the 2T pixel yields higher gain compared to the previously reported 3T current mode pixel amplifier, while providing the same functionality, and compatibility in driving/readout circuitry.

This research not only extends the application of a-Si on-pixel amplifiers to emerging high resolution, fast readout, low noise large area digital imaging applications such as digital mammography tomosynthesis, but also provides a potentially new pixel design for high resolution CMOS digital imaging.

References

(1) K.S. Karim, A. Nathan, J.A. Rowlands, "Amorphous silicon pixel amplifier with V_T compensation for low noise digital fluoroscopy," *IEDM Technical Digest*, pp. 215-218, December 2002.

(2) S.O. Kasap, J.A. Rowlands, "Direct-conversion flat-panel X-ray image sensors for digital radiography," *Proc. of IEEE*, Vol. 90, No. 4, pp. 591–604, 2002.

(3) F. Taghibakhsh, K.S. Karim, "High dynamic range 2-TFT amplified pixel sensor architecture for digital mammography tomosynthesis," *IET Devices Circuits and Systems*, Vol. 1, No. 1, pp. 87-92, February 2007.

(4) K.S. Karim, A. Nathan, M. Hack, W. Milne, "Drain-bias dependence of threshold voltage stability of amorphous silicon TFTs," *IEEE Electron Device Letters*, Vol. 25, No. 4, pp. 188-190, April 2004.

(5) M.H. Izadi, K.S. Karim, "Noise optimization of an active pixel sensor for real-time digital x-ray fluoroscopy," *Proc. of the SPIE on Noise and Fluctuations in Circuits, Devices, and Materials*, Vol. 6600, pp. 66000Y, 2007.

Characterization of Short-Wavelength-Selective a-Si:H MSM Photoconductors for Large-Area Digital-Imaging Applications

Farhad Taghibakhsh, *Student Member, IEEE*, Ida Khodami, *Student Member, IEEE*, and Karim S. Karim, *Member, IEEE*

***Abstract*—Photoconductor-type photodetectors are attractive as sensors due to their compatibility with thin-film-transistor (TFT) fabrication processes. Since they exhibit photogain, photoconductor detectors have better or comparable responsivity and quantum efficiency (QE) compared to p-i-n photodiodes. In this paper, the operation of metal–semiconductor–metal photoconductor-based photodetectors using aluminum electrodes and thin hydrogenated amorphous-silicon (a-Si) films is investigated. The experimental results of photocurrent measurements, as well as the responsivity and QE for different a-Si film thicknesses, bias voltages, and electrode gaps, are presented. Integration with TFT fabrication and its application in large-area digital imaging are discussed.**

***Index Terms*—Amorphous silicon (a-Si), metal–semiconductor–metal (MSM) devices, photoconducting devices, photodetectors.**

I. Introduction

Amorphous silicon (a-Si) and its alloys have been exploited in large-area applications such as backplane electronics for flat-panel displays and X-ray imagers, solar cell, and photodetector technologies [1]–[4]. Its broad absorption spectrum, high photoconductivity, and fairly low cost large-area deposition setup have made the hydrogenated a-Si (a-Si:H) and its alloys (a-Si carbon and germanium) as among the most attractive materials in photodetector research and industry [5], [6].

Wavelength selectivity of photodetectors, which is determined by the thickness and optical properties of the semiconductor material, is an important factor particularly in indirect X-ray imaging where the peak of emission spectra of the scintillator and the peak of absorption spectra of the photodetectors must be matched in order to have an optimum performance. Blue-emitting scintillators such as sodium iodide and sodium-doped cesium iodide emit 2.2 and 1.8 times more efficiently at 410 and 420 nm, respectively, compared with thallium-doped cesium iodide in green (550 nm). Therefore, imagers with better performance can be expected by the fabrication of a-Si photodetectors with higher sensitivity in the blue region coupled to the blue-emitting scintillators.

Manuscript received June 20, 2007; revised October 10, 2007. This work was supported in part by the Natural Sciences and Engineering Research Council of Canada (NSERC), by the Canada Foundation for Innovation (CFI), and by the British Columbia Knowledge Development Fund (BCKDF). The review of this paper was arranged by Editor H.-S. Tae.

The authors are with the Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, ON N2L 3G1, Canada (e-mail: ftaghiba@uwaterloo.ca).

Digital Object Identifier 10.1109/TED.2007.911094

Photodetectors are usually of two different types: photovoltaic, such as p-i-n photodiodes, and photoconductive, such as n-i-n or metal–semiconductor–metal (MSM) photoconductors. In comparison to the p-i-n photodiodes, the a-Si:H photoconductor-type detectors are attractive from an integration point of view because their fabrication process is fully compatible with that of the a-Si thin-film transistors (TFTs) where there are no p-doped layers or SiC alloy films involved. It is worth noting that, in an imaging application, photoconductor detectors are not necessarily used in the same way that photodiodes are used in integrating mode (i.e., charging a storage capacitor). It is possible to read out the photocurrent of a biased photoconductor directly through a switching device such as a TFT [8].

The motivation behind this paper is to develop a low-cost fabrication process in which wavelength-selective photodetectors and TFT driving circuits are fabricated simultaneously in the same fabrication process, saving a number of masks, process steps, materials, and equipment. In this paper, characterization of very thin aluminum a-Si MSM photoconductors is presented, and results are discussed.

II. Detector Structure and Operation

The structure of a coplanar photoconductor photodetector is similar to a TFT with no gate (Fig. 1). Upon exposure to light, the absorbed photons in the channel area create electron-hole pairs, and therefore, channel conductance is modulated. The semiconductor film thickness determines photodetector selectivity; for very thin a-Si:H layer thickness, only a small portion of the green and red lights is absorbed, whereas most of the blue and UV are absorbed and contribute to channel-conductance modulation (Fig. 2). Different device topologies have been proposed or reported as coplanar structure for photoconductor detectors [8], among which the metal–a-Si:H–metal structure with ohmic or Schottky contacts was reported to have high sensitivity as well as compatibility in process with TFT fabrication (there is no p^+ layer involved, as is the case for photodiode detectors) [10]. Fig. 1 shows the schematic diagram of a coplanar photoconductor (center), as well as two different practical methods for its fabrication: bottom- and top-electrode configurations. The top-electrode configuration is compatible with a trilayer bottom-gate staggered TFT fabrication [11], whereas the bottom-electrode structure is compatible with a top-gate staggered TFT.

0018-9383/$25.00 © 2008 IEEE

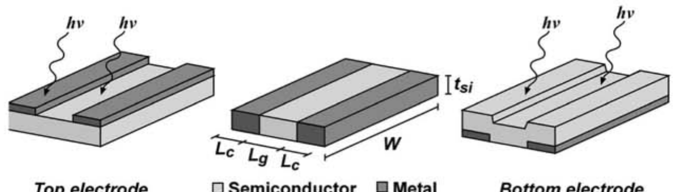


Fig. 1. Schematic diagram of coplanar photoconductor detectors: Top electrode (left) and bottom electrode (right). Both bottom- and top-electrode configurations are compatible with TFT fabrication.

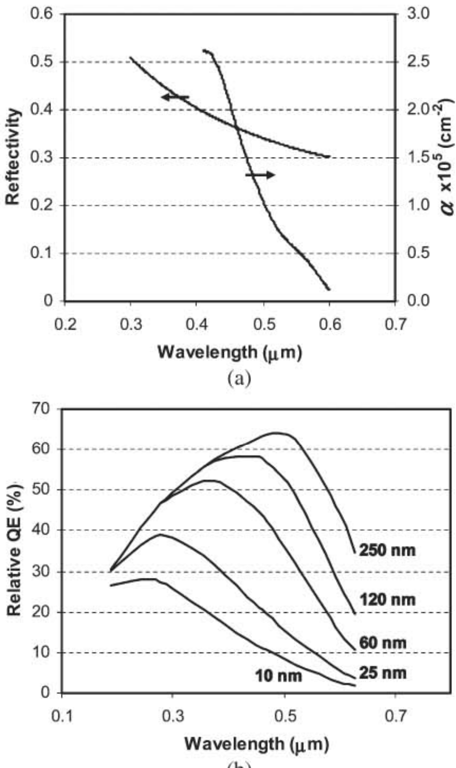


Fig. 2. Wavelength dependency of (a) reflectivity and absorption coefficient of a-Si and (b) calculated NQE for different values of a-Si film thicknesses.

The fill factor is taken to be $L_g/(L_g + 2L_c)$ for both top- and bottom-electrode configurations. Compared to top-electrode devices, the bottom-electrode configuration has a larger absorption area; however, photo-generated carriers on top of the electrodes are not effectively collected due to the lack of electric field, specifically for very thin semiconductor layers on the order of 10–20 nm.

III. Quantum Efficiency (QE) of Coplanar Photoconductors

Assuming ohmic contacts and no space-charge-limited current, the drift of optically generated carriers under externally applied electric field is the main mechanism of generating photocurrent in an illuminated coplanar photoconductor. In steady-state condition, the density of excess carriers is equal to $G_{\mathrm{opt}}\tau_r$, and if this value is much larger than the intrinsic carrier concentration, the photocurrent is written in the form of the standard drift equation as

$$J_{\mathrm{ph}} = qG_{\mathrm{opt}}\tau_r\mu E \tag{1}$$

where q is the electronic charge, G_{opt} is the optical generation, τ_r is the effective recombination time, μ is the carrier mobility, and E is the applied electric field. A photoconductor that is illuminated under the optical power density P_{opt} receives a photon flux $\Phi_{\mathrm{ph}} = P_{\mathrm{opt}}WL_g/h\nu$, where W and L_g are the photoconductor-contact width and the gap between the contacts, respectively, and $h\nu$, which is equal to hc/λ, is the photon energy. The optical generation is equal to the absorbed flux of photons per volume. Therefore, assuming that the optical absorption efficiency is η, the G_{op} in the active volume of WL_gt_{si} between the photoconductor contacts is found to be

$$G_{\mathrm{opt}} = \frac{\eta\Phi_{\mathrm{ph}}}{WL_gt_{\mathrm{si}}} = \frac{\eta P_{\mathrm{opt}}}{h\nu t_{\mathrm{si}}} \tag{2}$$

where t_{si} is the a-Si photoconductor thickness. Because of the reflection from the surface, only part of the incident photons enter the device, and if the photoconductor thickness is small, only part of the photons entering the device are actually absorbed.

Assuming that all the absorbed photons generate an electron-hole pair, η is written as

$$\eta = (1 - R)\left(1 - \exp(-\alpha t_{\mathrm{si}})\right) \tag{3}$$

where $R = (n-1)^2/(n+1)^2$ is the surface reflectivity, and α and n are the wavelength-dependent absorption coefficient and the refractive index of the photoconductor material, respectively [11]. Knowing that the area of the photoconductor through which the photocurrent flows is Wt_{si} and that the applied electric filed is equal to V/L_g, substituting (2) into (1) results in the photocurrent as

$$I_{\mathrm{ph}} = J_{\mathrm{ph}}Wt_{\mathrm{si}} = q\eta\frac{\lambda P_{\mathrm{opt}}}{hc}\mu\tau V\frac{W}{L_g}. \tag{4}$$

Equation (4) shows the linear proportionality of the photocurrent-to-photoconductor aspect ratio W/L_g, the photoconductor biasing voltage V, the transport properties of the photoconductor $\mu\tau$, and the density of photon flux $\lambda P_{\mathrm{opt}}/hc$. However, because mobility-lifetime product is photon-flux-dependent, the photocurrent appears to be slightly sublinear with respect to incident light intensity [13]. As a first-order

approximation, I_{ph} was taken to be linear with respect to the density of the incoming photon flux $\lambda P_{\mathrm{opt}}/hc$ [11]. At high electric fields, where the device enters the space-charge-limited current regime, the photoconductor current becomes nonlinear with respect to the applied voltage; however, linear approximation holds at low operating-voltage points.

The external QE (EQE), which is defined to be the ratio of charge flux to photon flux, shows how effectively the incident photon flux is converted to charge carriers and how effectively those carriers are collected [14]

$$\mathrm{EQE} = \frac{I_{\mathrm{ph}}/q}{P_{\mathrm{inc}}/h\nu} = \frac{I_{\mathrm{ph}}}{P_{\mathrm{opt}}A}\frac{hc}{\lambda q} = \eta\mu\tau V\frac{W}{AL_g}. \quad (5)$$

Here, A is taken to be the total illuminated area of the device. For example, for photoconductors shown in Fig. 1, the total area of the device is $W(L_g + 2L_c)$. Substituting (3) into (5), and recalling that $L_g/(L_g + 2L_c)$ is equal to the fill factor FF, the EQE is written as

$$\mathrm{EQE} = \eta G_{\mathrm{ph}}\mathrm{FF} = (1 - R)\,(1 - \exp(-\alpha t_{\mathrm{si}}))\,\frac{\mu\tau_r V}{L_g(L_g + 2L_c)} \quad (6)$$

where $G_{\mathrm{ph}} = \mu\tau_r V/L_g^2$ is called the photogain and can be above unity unlike the p-i-n photodiodes. The photogain of photoconductor devices depends on the many factors including the photoconducting material, the device structure, and the biasing condition; it is not provided by external devices. The gain can reach as high as 10^6 in short-length devices made from materials with long lifetimes and high values of low-field mobility. Photogains that are as high as 1000 have been reported in silicon photoconductors and upward of 50 for InGaAs [11]. For photoconductors like the a-Si, although $\mu\tau$ is low, a higher than unity photogain can compensate the low fill factor so that a better or comparable EQE compared to the p-i-n photodiodes can be expected. Proportionality of G_{ph} and EQE to an applied voltage is an advantage from circuit design point of view when photogain and EQE can be set based on requirements or adjusted according to the drift of device characteristics.

To compare wavelength selectivity of different photoconductors, internal QE (NQE) is used, which is an EQE normalized by photogain and fill-factor product

$$\mathrm{NQE} = \frac{\mathrm{EQE}}{G_{\mathrm{ph}}\mathrm{FF}} = (1 - R)\,(1 - \exp(-\alpha t_{\mathrm{si}}))\,. \quad (7)$$

Equation (7) is used to design the semiconductor film thickness to have the QE peak at a desired wavelength. As shown in Fig. 2, a photoconductor detector with 25-nm-thick a-Si:H layer will have the maximum QE at 300 nm.

IV. Experimental Methods, Measurements, and Results

A. Device Fabrication

Bottom-electrode coplanar photoconductors with three different a-Si film thicknesses of 15, 25, and 60 nm were fabricated in-house. First, a 60-nm aluminum was sputtered on corning glass substrates and was patterned using standard lithography and wet etching to have various electrode spacings (L_g) of 5, 10, 15, 20, and 30 μm, and a contact length (L_c) of 10 μm (Fig. 3). A a-Si:H was next deposited using plasma-enhanced chemical vapor deposition (PECVD), which was followed by a very thin silicon nitride layer to protect the photoconductor film from oxidation; deposition conditions are listed in Table I. Finally, silicon islands were patterned over electrodes using dry etching, and samples were annealed at 200 °C in vacuum for 1 h before any measurement.

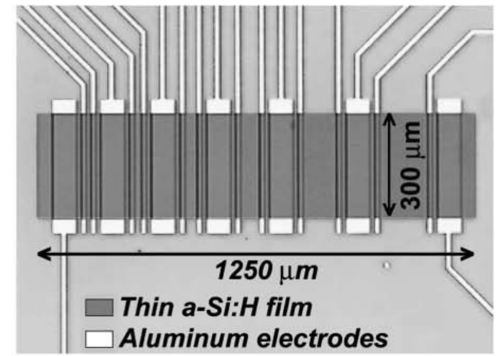


Fig. 3. Photomicrograph of fabricated photoconductor photodetectors with different electrodes spacings of 5, 10, 15, 20, 30, 50, 100, and 150 μm. All devices have the same width of 300 μm.

TABLE I
Deposition Condition for PECVD Films Used

Film	Gas mixture	Flow rate (sccm)	Pressure (m Torr)	Temp. (°C)	Power (W)
a-Si:H	*SiH_4/H_2*	*20/100*	*500*	*250*	*1W*
SiN_X	*$SiH_4/NH_3/H_2$*	*2/16/100*	*1900*	*250*	*20W*

Absorption coefficient of the a-Si layer was extracted from the measured transmission data and shown in Fig. 2. The Tauc optical bandgap was also extracted to be 1.81 eV.

B. Selectivity

The theoretical expression of selectivity is obtained by substituting (3) into (4) and calculating the ratio of the detector photocurrent for two different wavelengths

$$S = \frac{\lambda 1(1 - R_{\lambda 1})\,(1 - \exp(-\alpha_{\lambda 1}t_{\mathrm{si}}))}{\lambda 2(1 - R_{\lambda 2})\,(1 - \exp(-\alpha_{\lambda 2}t_{\mathrm{si}}))}. \quad (8)$$

For an optical power density of 184 μW/cm^2 and a biasing voltage of 20 V, the blue-to-green photocurrent selectivity (S) values of the fabricated detectors were measured to be 1.2 and 1.25 for detectors with 60 and 25 nm of a-Si photoconductor thickness, respectively, which are comparable with the calculated values of 1.18 and 1.35, respectively. However, for detectors with $t_{\mathrm{si}} = 15$ nm, the measured values were neither consisting nor following the expected trend. We concluded that the bad quality of electrical contacts between very thin a-Si film and side walls of the patterned electrodes might be

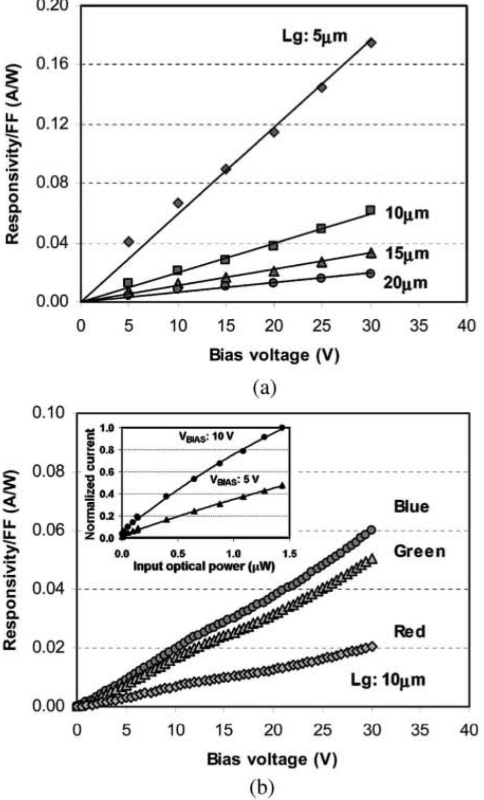


Fig. 4. Measured blue responsivity of the 25-nm-thick photoconductor versus biasing voltage for (a) different electrode spacings and (b) different colors. The blue responsivity is as high as almost 180 mA/W for an electrode spacing of 5 μm in (a). The normalized photocurrent against input optical power depicted in the inset of (b) shows a slightly sublinear behavior.

the reason for the inconsistent characteristics of 15-nm-thick samples.

C. Photoresponsivity and Photogain

Photoresponsivity PR, which is a measure of electro-optic transfer gain of photodetectors, is the ratio of photocurrent to photoconductor incident power. Dividing (4) by $P_{\rm opt}A$ results in

$$\mathrm{PR} = \eta \frac{q\lambda}{hc} \mu\tau_r \frac{V}{L_g(L_g + 2L_c)} = \eta \frac{q\lambda}{hc} G_{\rm ph} FF. \quad (9)$$

Blue-light responsivity of photoconductors with a different gap between electrodes was measured versus the bias voltage (Fig. 4). As expected, a close-to-linear dependency of responsivity to the bias voltage was observed. For the shortest gap between electrodes, i.e., $L_g = 5$ μm, responsivity as high as 180 mA/W for blue light was measured, which is comparable with or better than the reported values for other detectors [15].

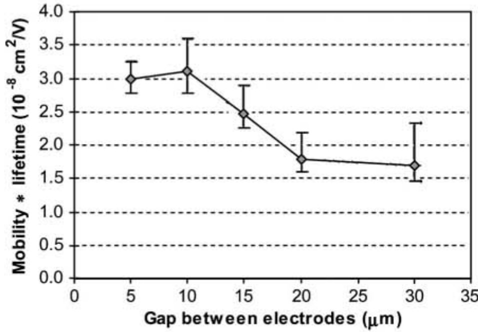


Fig. 5. Extracted mobility-lifetime product from photocurrent measurements for different gaps between electrodes. The $\mu\tau$ product is the maximum value for $L_g = 10$ μm.

The extrinsic mobility-lifetime product was extracted from the calculation of slope of the photocurrent versus the applied bias voltage $\Delta I_{\rm ph}/\Delta V$ and versus the inverse of the gap between electrodes $\Delta I_{\rm ph}/\Delta(1/L_g)$. The result is shown in Fig. 5, where the mobility-lifetime product reaches its maximum value for 10-μm gap between electrodes. For photovoltaic-type photodetectors such as the p-i-n diodes, carriers move perpendicular to the substrate; hence, they do not experience the substrate surface roughness and are not trapped in surface states as compared with carriers moving in coplanar detectors. For very thin films, the surface states on the top and bottom interfaces of the narrow conduction channel play a major role in the trapping of carriers, which results in low mobility-lifetime product. The lateral flow of charge carriers, parallel to the substrate, also forces the carriers to follow the roughness of the substrate which is another cause of increased trapping and, subsequently, a low mobility-lifetime product. Therefore, it is expected that the mobility-lifetime product will be low, particularly for very thin a-Si layers. It is observed that the mobility-lifetime product slightly increases as the gap between electrodes decreases. This is probably due to the reduced chance of trapping in surface states. Assuming a recombination time of 10^{-7} s, the mobility would be 0.3 $\mathrm{cm^2/V \cdot s}$ for 10-μm electrode-gap devices, which is in the range of reasonable number for a-Si. Even though the mobility-lifetime product is small, an above unity photogain was observed. For photoconductors with 5-μm gap, photogain was measured to be slightly above one for a bias voltage of 15 V, which was linearly increasing to 2.37 at a bias voltage of 30 V. For all other detectors with longer L_g, photogain was measured to be less than unity.

D. Quantum Efficiency and Photo-to-Dark-Current Ratio

As expressed in (6), EQE is a function of gap between electrodes and applied voltage, as well as contact length L_c. To suppress the effect of contact length, the ratio of QE to fill factor, i.e., EQE/FF, is shown in Fig. 6. QE greatly improves as the gap between electrodes becomes smaller. However, the ratio of illuminated current to dark current $R_{\rm L/D}$ decreases for smaller values of L_g. This is due to the fact that, for a photoconductor under illumination, fewer holes are trapped

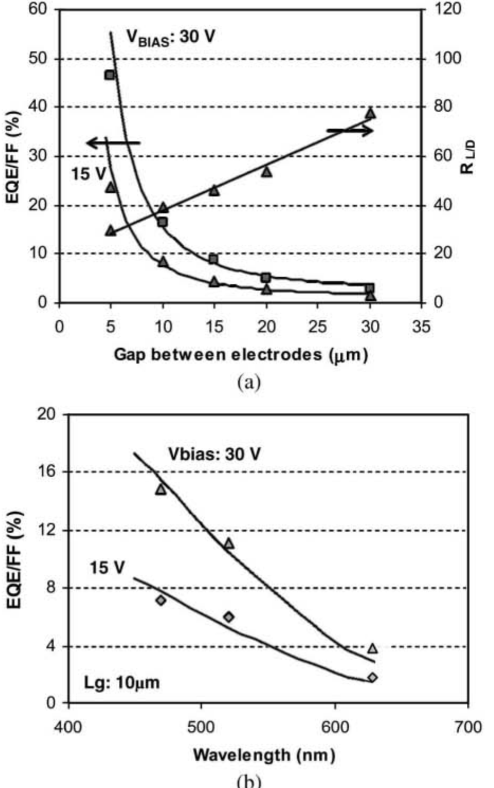


Fig. 6. Calculated (solid) and measured values (dots) of EQE of fabricated photoconductors for two biasing voltages of 15 and 30 V (a) versus gap between electrodes and (b) versus different wavelengths.

because of photon bombardment; therefore, the photocurrent is not space-charge-limited as the dark current is. Assuming a photocurrent to be proportional to $1/L_g$ [(4)], and a dark current to be proportional to $1/L_g^2$ [16], then $R_{\mathrm{L/D}}$ would be proportional to L_g. The spectral QE shows considerably higher values for blue than green, as the spectral responsivity was. Based on calculation [Fig. 1(b)], it is expected that EQE peaks at about 300 nm of wavelength.

E. Dark-Current Stability

The dark current of various metal–semiconductor structures are unstable over time [17]. The instability, which is caused by hole trapping at cathode junction, has been studied in detail [18]. We observed almost the same trend for thick a-Si films (~350 nm) on nickel electrodes before [19]; however, for very thin layers of ~20-nm a-Si on aluminum, the increase in the current was very slow, and it started to roll down after reaching its peak value (Fig. 7). The peak value, however, is much less than what was predicted for metal–semiconductor structures [18]. Preliminary results of dark-current instability of a photodetector with 20-μm electrode spacing biased at 20 V is shown in Fig. 7, which shows that the device is reasonably stable at low bias voltages [19].

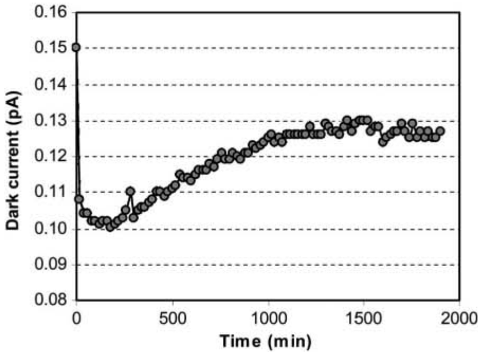


Fig. 7. Instability of photodetector dark current under constant bias voltage of 5 V over a long period of time.

V. CONCLUSION

We have reported the electrical characteristics, optical selectivity, and QE of MSM photodetectors using very thin a-Si:H layers with aluminum electrodes having different gaps between them. Also, we have measured the performance of fabricated photodetectors at different biasing voltages, and under different monochromatic illuminations, for different electrode spacings. Expected values and measured data exhibit a close match. For detectors with 25-nm-thick a-Si layer and 5-μm gap between electrodes, which are biased at 30 V, a higher sensitivity in the blue region (as compared with the green one) of the spectrum was measured, with a photogain of 2.3, a responsivity reaching 0.176 A/W, and an EQE of more than 45%. The linear dependence of responsivity and QE of MSM detectors on the applied bias voltage provides a programmable gain characteristic. For example, the well-known light-induced degradation of a-Si may be compensated by adjusting the bias voltage in such detectors.

The fabrication process for a-Si:H MSM photodetectors presented in this paper is fully compatible with a-Si TFT fabrication processes, which can result in potentially lower fabrication costs for high-gain short-wavelength-selective imaging arrays for indirect digital X-ray imaging using blue-emitting scintillators.

ACKNOWLEDGMENT

This paper was done at the Engineering Science Department, Simon Fraser University, Burnaby, BC, Canada.

REFERENCES

[1] R. A. Street, X. D. Wu, R. Weisfield, S. Ready, R. Apte, M. Nguyen, and P. Nylen, "Two dimensional amorphous silicon image sensor arrays," in *Proc. MRS Symp.*, 1995, vol. 377, pp. 757–766.

[2] A. Nathan, K. Sakariya, A. Kumar, P. Servati, K. S. Karim, D. Striakhilev, and A. Sazonov, "Amorphous silicon TFT circuit integration for OLED displays on glass and plastic," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2003, pp. 215–222.

[3] K. S. Karim, A. Nathan, and J. A. Rowlands, "Amorphous silicon active pixel sensor readout circuit for digital imaging," *IEEE Trans. Electron Devices—Special Issue Image Sensors*, vol. 50, no. 1, pp. 200–208, Jan. 2003.

[4] D. E. Carlson, "Amorphous-silicon solar cells," *IEEE Trans. Electron Devices*, vol. 36, no. 12, pp. 2775–2780, Dec. 1989.

[5] R. A. Street, *Technology and Applications of Amorphous Silicon*, 1st ed. New York: Springer-Verlag, 1999.
[6] M. Topic, H. Stiebig, M. Krause, and H. Wagner, "Adjustable ultraviolet-sensitive detectors based on amorphous silicon," *Appl. Phys. Lett.*, vol. 78, no. 6, pp. 2387–2389, Apr. 2001.
[7] J. I. Ruy, S. H. Won, J. H. Hur, H. J. Kim, and J. Jang, "Simulation of a novel amorphous silicon photoconductor array," *J. Korean Phys. Soc.*, vol. 39, pp. S112–S115, Dec. 2001.
[8] A. M. Castillo, A. T. Jacome, A. Heredia, and R. Ramos, "An a-SiGe:H,F based thin film MSM high-speed photodetector," in *Proc. 6th Int. Caribbean Conf. Devices, Circuits Syst.*, 2006, pp. 91–94.
[9] M. Hillebrand, F. Blecher, J. Sterzel, and M. Bohm, "An amorphous silicon photoconductor for UV detection," in *Proc. MRS*, 2003, vol. 762, pp. 211–216.
[10] L.-H. Laih, Y.-A. Chen, W.-C. Tsay, and J.-W. Hong, "High responsivity a-Si:H bottom-electrode metal–semiconductor–metal photodetector," *Electron. Lett.*, vol. 32, no. 10, pp. 929–930, May 1996.
[11] D. B. Thomasson and T. N. Jackson, "High mobility tri-layer a-Si:H thin-film transistors with ultrathin active layer," *IEEE Electron Device Lett.*, vol. 18, no. 8, pp. 397–399, Aug. 1997.
[12] M. Shur, "Photonic devices," in *Physics of Semiconductor Devices,* 1st ed. Englewood Cliffs, NJ: Prentice-Hall, 1990, ch. 5, Sec.4, pp. 501–504.
[13] R. E. Stearns and R. L. Weisfield, "Two dimensional amorphous-silicon photoconductor array for optical imaging," *J. Appl. Opt.*, vol. 31, no. 32, pp. 6874–6881, Nov. 1992.
[14] M. C. Hamilton and J. Kanicki, "Organic polymer thin-film transistor photosensors," *IEEE J. Sel. Topics Quantum Electron.*, vol. 10, no. 4, pp. 840–848, Jul./Aug. 2004.
[15] M. Krause, M. Topič, H. Stiebig, and H. Wagner, "Thin-film UV detectors based on hydrogenated amorphous silicon and its alloys," *Phys. Stat. Sol. A*, vol. 185, no. 1, pp. 121–127, May 2001.
[16] J. Sworakowski and G. F. Ferreira, "Space-charge-limited currents and trap-filled limit in one-dimensional insulators," *J. Phys. D, Appl. Phys.*, vol. 17, no. 1, pp. 135–139, Jan. 1984.
[17] N. Kopiadakis, "Formation and properties of metastable defects induced by pulsed laser irradiation in hydrogenated amorphous silicon," Ph.D. Dissertation, Phys. Dept., Univ. Crete, Crete, Grece, 1998.
[18] K. Aflatooni, R. Hornsey, and A. Nathan, "Reverse current instabilities in amorphous silicon Schottky diodes: Modeling and experiments," *IEEE Trans. Electron Devices*, vol. 46, no. 7, pp. 1417–1422, Jul. 1999.
[19] F. Taghibakhsh and K. S. Karim, "Fabrication and characterization of nickel amorphous silicon metal–semiconductor–metal photoconductors," in *Proc. 20th Can. Conf. Elect. Comput. Eng.*, Vancouver, BC, Canada, Apr. 2007, pp. 1664–1667.

Farhad Taghibakhsh (S'04) received the B.Sc. degree in electrical and electronic engineering from the University of Zahedan, Zahedan, Iran, in 1996, and the M.Sc. degree from K.N. Toosi University of Technology, Tehran, Iran, in 1999. He is currently working toward the Ph.D. degree in the Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, ON, Canada.

His research interests include thin-film electronics, semiconductor devices, and X-ray medical imaging.

Ida Khodami (S'05) received the bachelor degree of applied science in electrical engineering from Simon Fraser University, Burnaby, BC, Canada, in 2005. She is currently working toward the M.S. degree in the Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, ON, Canada.

Her interests include ultraviolet photodetectors and their application in biomedical devices. She holds a Natural Sciences and Engineering Research Council of Canada Graduate Scholarship.

Karim S. Karim (S'96–M'00) received the Ph.D. degree from the University of Waterloo, Waterloo, ON, Canada, in 2002.

He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, University of Waterloo. His current research interests include large-area circuit, device, and process development in both amorphous- and crystalline-silicon technologies for biomedical-imaging applications.

Dr. Karim has received the Canadian Association for Graduate Studies/University Microfilm International Distinguished Dissertation Award for the best doctoral thesis in science and medicine in Canada, the Natural Sciences and Engineering Research Council of Canada Doctoral Prize, and the Douglas Colton Medal for Research Excellence in microelectronics applied to medical imaging.

Honorable Mention Poster Award

Amplified Pixel Sensor Architectures for Low Dose Computed Tomography using Silicon Thin Film Technology

F. Taghibakhsh*, K.S. Karim
Simon Fraser University, School of Engineering Science,
Burnaby, British Columbia, Canada, V5A 1S6

ABSTRACT

Cone beam computed tomography (CBCT) has been recently reported using flat panel imagers (FPI). Here, detector technology capable of high speed imaging, high spatial resolution, large volume coverage, better contrast resolution and, in particular, lowered patient dose is required. Employing active matrix flat panel imagers (AMFPIs) as cone beam CT detectors has been proposed as a solution for improving volume coverage, contrast and resolution; however, clinical evaluations have shown that they suffer from low speed read out.

Unlike passive pixel architecture which is currently the state-of-the-art technology for AMFPIs, our preliminary studies have shown that novel amplified pixel sensor (APS) architectures can overcome the low readout speed, and moreover, they provide gain which can be traded for higher frame rate and lower X-ray doses. Although APS architectures can meet the high dynamic range and low noise requirements of CT imaging, linearity and variations between pixel characteristics are major issues. In this study we will investigate novel APS architectures to address these concerns.

Keywords: Cone beam computed tomography, flat panel imager, TFT, amorphous silicon, medical imaging, high frame rate, amplified pixel sensor, pixel architecture.

1. INTRODUCTION

Research on cone beam computed tomography (CBCT) has been growing fast in recent years. There are a considerable number of reports that flat panel imagers (FPI) have been successfully mounted on commercial CT scanners resulting in excellent image resolution due to small pixel size of the FPI, full organ coverage and efficient use of x-ray dose because of large area of the detector panel [1-4]. FPIs can provide sufficient dynamic range for CT applications [2], however, the major impediment for commercialization of CBCT scanners using flat panel imagers, to date, is the low frame rate of FPIs [1].

The state-of-the-art flat panel imagers are based on passive pixel sensor (PPS) architecture fabricated using amorphous silicon (a-Si) thin film transistor (TFT) and photodiode arrays coupled to a scintillator layer, which is usually made of cesium iodide (CsI). The readout speed of such arrays is *RC* time limited, with *R* representing the "ON" resistance of the a-Si TFT switch (in the order of mega ohms) and, *C*, the parasitic capacitance of data lines of the array (a few tens of pico farads) . The *RC* time constant is usually minimized by reducing parasitic capacitances and resistances of the imager array, as well as, and more importantly, reduction of the access resistance (or series resistance) of the TFT to have the maximum frame rate. The other approach to increase the frame rate is pixel binning, i.e., grouping neighboring pixels together to reduce the total number of pixels to read. Although pixel binning increases the frame rate by decreasing the time it takes to read out imager data, it also deteriorates image resolution which tends to degrade the high resolution image obtained by flat panel detectors.

In this paper, two different approaches are evaluated in order to increase frame rate readout of FPIs by reducing the readout time: circuit architecture approach, and material approach. For the former, current mediated amplified pixel sensor (C-APS) architecture is introduced as a promising candidate for FPIs for CBCT applications; it is faster to read, because it is not RC time limited like PPS circuits, and also, it provides pixel-level signal gain compared to PPS arrays. By providing gain, C-APS arrays will have higher signal to noise ratio, (SNR), which can be traded for lower dose imaging while keeping the image quality the same.

*ftaghiba@sfu.ca

Medical Imaging 2007: Physics of Medical Imaging, edited by Jiang Hsieh, Michael J. Flynn,
Proc. of SPIE Vol. 6510, 65103W, (2007) · 1605-7422/07/$18 · doi: 10.1117/12.710147

Adding signal amplification in pixel level, requires addition of a few more TFTs to each pixel which leaves less area available for detector. This causes the fill factor of the pixel to be reduced, as well as potential fabrication reliability issues. Different C-APS architectures are discussed to specifically address these problems. As for the latter approach, nanocrystalline silicon (nc-Si) TFTs are suggested to replace amorphous silicon devices. Thin film transistors fabricated using nc-Si, exhibit much higher electron mobility, resulting in higher speed and gain which can further help reduce readout speed and x-ray dose.

In section 2, after a brief review of different pixel architectures, we present a new compact multimode pixel circuit for high dynamic range low noise imaging suitable for cone beam CT applications. Imager array configurations and required circuitry are discussed in section 3, followed by noise analysis in section 4. Finally, we conclude our findings and present our plans for continuation of this work.

2. MULTIMODE PIXEL ARCHITECTURES

CT detectors are fabricated using discrete *pin* photodiode coupled to a ceramic scintillator with each detector wired to a separate readout channel. This detector configuration provides the fastest readout operation. As the number of detectors increases in multi-slice CTs, providing separate channels for all detectors becomes a real challenge. In some cone beam CT applications, where millions of pixel detectors are required, flat panel imagers have been successfully tested. In a flat panel imager, integrated detectors are addressed using a TFT switch, row by row in an array, and readout channels are provided for each column. Here, scintillator detectors such as cesium iodide, CsI, or photoconductor detectors like amorphous selenium, a-Se, can be used (Figure 1.a and 1.b).

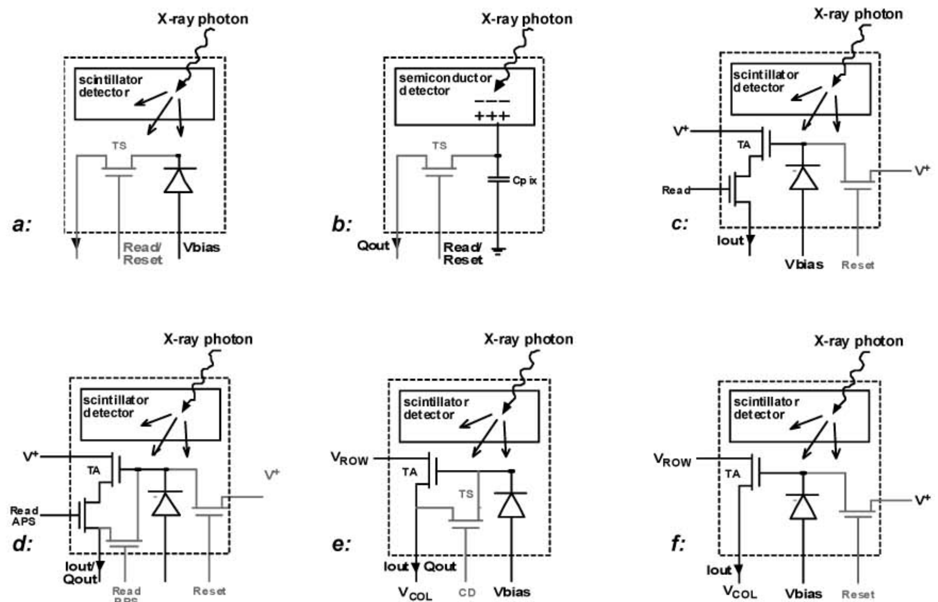


Figure 1. Schematic diagram of one pixel of different FPI architectures. (a): PPS architecture consisting of a TFT switch and pin photodiode with scintillator detector; (b): same PPS architecture using photoconductor detector and direct detection method; (c): current mediated active pixel sensor (C-APS) architecture for low dose high frame rate applications; (d): multimode 4-TFT C-APS architecture for high frame rate high dynamic range imaging; (e): multimode 2-TFT architecture with shared reset line for high resolution high dynamic range x-ray imaging; (f): 2-TFT C-APS architecture for high frame rate, high resolution , high dynamic range x-ray imaging applications.

Different amplified pixel sensor architectures have been introduced using three TFTs capable of producing the output signal in the form of voltage or current which are known as V-APS and C-APS (Figure 1.c) respectively [5]. Multimode architectures have been also proposed using 3 or 4 TFTs capable of operating in PPS or C-APS modes for different x-ray imaging modalities such as fluoroscopy and chest radiography [6]. Here, we introduce multimode architectures using only 2 TFTs, capable of working in two different modes of operation: PPS, and C-APS (Figure 1.e and 1.f).

The new active pixel architecture, as shown in Figure 1.e, has two TFTs, T_A and T_S in which, T_A functions as a transconductance amplifier, and T_S is a switch that is used to charge and discharge (set and reset) the voltage of pixel *pin* diode detector. In C-APS mode, T_S is off and a biasing voltage is applied to V_{ROW}, while V_{COL} is grounded. Depending on values of V_{ROW} and preset voltage of the detector, T_A is biased in linear or saturation mode. In either case, the output current, which is modulated by the detector voltage applied at the gate of T_A, is integrated in a column charge amplifier as long as the bias voltage is provided. In the PPS mode however, both V_{ROW} and V_{COL} are grounded (V_{ROW} can also be floated), and T_S is turned on by applying a high voltage to its gate, *CD*. Therefore the stored charge in the detector is transferred to the column charge amplifier via the data line for integration and further signals processing.

A schematic diagram of an imager array composed of 2-TFT C-APS pixel architecture (as in Figure 1.f) is shown in Figure 2, and corresponding biasing conditions for different operation cycles are listed in Table 1. For resetting the pixel detector, a high positive voltage is applied to charge-discharge lines (*CD*) that turns T_S transistors on and pixel detector is reset. While resetting, the row-select lines (*RS*) are low, so that row select transistors are OFF. This makes sure no current flows in T_A transistors of the line being reset. In integration mode where X-ray is exposed, grounding all *RS* and *CD* lines ensures all row select switches and all T_S TFTs are OFF.

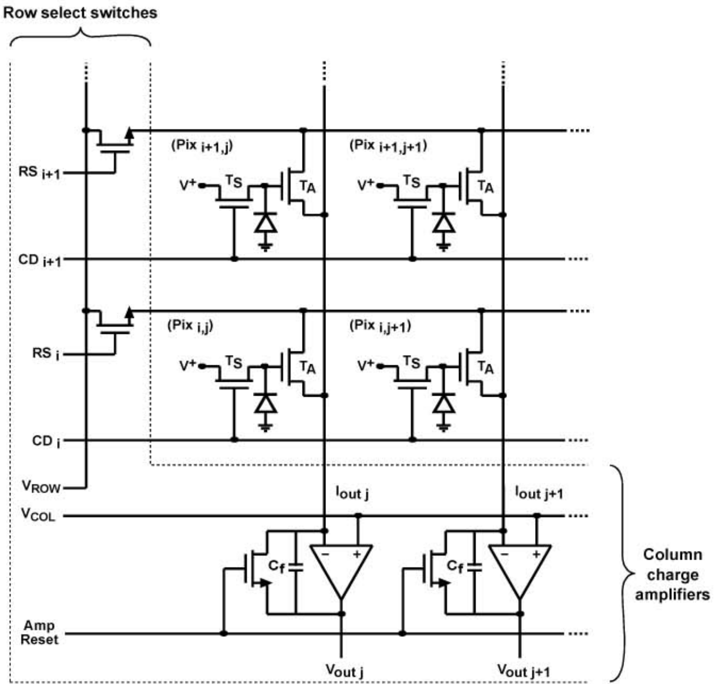


Figure 2. Configuration of an imager array of 2-TFT multimode pixel sensors with integrated reset bias, consisting of row select switches, column charge amplifiers and pixel array. Row addressing is performed by turning ON the row select switch which applies the bias voltage, V_{ROW}, to the corresponding row of the imager.

In readout cycle, the charge amplifiers reset switches are OFF (Amp-*Reset* grounded) allowing charge amplifiers integrate the output current while V_{COL} is grounded. To read the pixel, a biasing voltage, V_{ROW}, is applied to the row being read, by turning ON the corresponding row switch (*RS* is high) allowing current flows through drain of TA TFT, and to be integrated in charge amplifiers.

In order to compensate inherent V_T shift of TFTs, the idle cycle is defined in which sufficiently high positive voltage is applied to VCOL while row select switches are off. This results in negative V_{GD} and V_{GS} for T_A TFTs. For Ts TFTs a negative voltage is applied to *CD* lines directly in idle mode.

Table 1. Biasing conditions for different operation cycles of the 2-TFT imager array

Cycle name	***Amp-Reset***	V_{ROW}	V_{COL}	***RSi***	***CDi***	T_A	T_S
Pixel reset	Low	-	Grounded	Low	High	Float	ON
Amp reset	High	-	Grounded	-	-	-	-
Integration	Low	-	Grounded	Low	Low	Float	OFF
Readout	Low	$+V_{bias}$	Grounded	High	Low	ON	OFF
Idle mode	High	-	High	Low	Negative	OFF	OFF

3. PIXEL CHARACTERISTICS AND NOISE PERFORMANCE

Assuming an electron-hole pair is generated for each absorbed photon in the *pin* diode, we have previously shown that, by proper biasing of the pixel so that T_A operates in linear mode, the change in the output current of the pixel is written as a function of number of absorbed photos, N, as [7]:

$$\Delta I_{out}(N) = q\frac{\mu_{FE} C_0 W}{LC_{PIX}} V_{ROW} N \qquad (1)$$

In which, q is the electronic charge, C_{PIX} , the capacitance of the pixel detector, μ_{FE}, C_0, W/L and V_T are the field effect mobility, gate capacitance per unit area, geometric aspect ratio and the threshold voltage of T_A thin film transistor respectively. As it is seen in (1) the gain of the pixel is linearly controlled by the applied voltage V_{ROW}, and is directly proportional to μ_{FE}. Linear proportionality to the field effect mobility is of great importance here. This indicates that for imagers built in nanocrystalline silicon, nc-Si, or microcrystalline silicon, μc-Si, thin films which exhibit much higher μ_{FE}, not only the readout time would be shorter because of less parasitic resistances, but also the gain would be higher compared to amorphous silicon imagers. For PPS imagers, only readout time will decrease upon use of silicon thin films with higher mobility; there is no charge gain associated with PPS architecture. Below, we will show how the charge gain can be traded for shorter readout time (higher frame rate) as well as better noise performance (higher SNR).

Simulation results confirms integrity of (1); for W/L = 100μm/10μm, Co = 18 nF/cm^2 V_{ROW} = 5 V, and a given set of model parameters extracted from a-Si TFTs fabricated in-house [7, 8], integrated charge in 25μs readout time was simulated for different number of deposited charge on the detector. The result is plotted against absorbed charge on the detector in Figure 3.

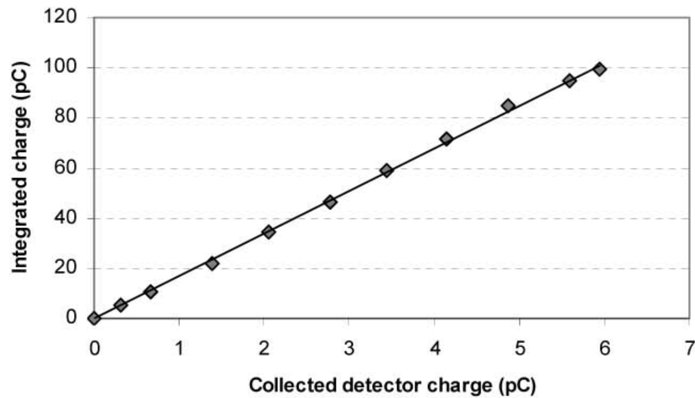


Figure 3. Simulation result of integrated charge at the column charge integrator versus collected charge at the pixel detector for V_{ROW} = 5 V, and readout time of 25μs. The slope of the line indicates the pixel gain in APS mode, which is 16.

The slope of the line was extracted to be 16, which is the charge gain of the 2-TFT C-APS pixel for the given parameters. This relatively high gain implies that if the readout time is reduced by a factor of 16 (i.e., by the charge gain of the C-APS imager), the amount of charge integrated at column charge integrator will be equivalent to that of a PPS imager. However, with a C-APS imager, the x-ray image can be read out 16 times faster, hence, the frame rate is enhanced. Figure 4 schematically describe how C-APS out performs PPS in readout speed.

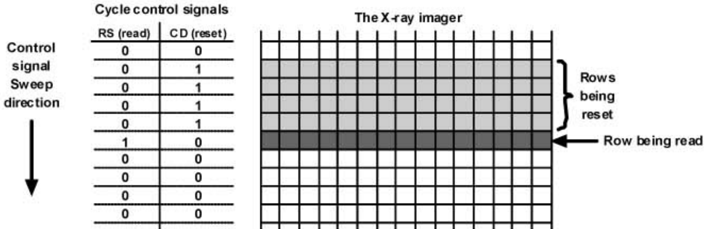


Figure 4. Sharing reset time in a resetting window results in fast readout of C-APS imager by shortening the readout time at the expense of charge gain. Higher frame rates in a-Si flat panel imagers are feasible compared to FPIs using PPS architectures.

Having same amount of RC delay, the time it takes to reset/read a PPS or a C-APS imager is the same. Assuming that 16 microseconds is needed to reset/read one line of a PPS imager, a C-APS imager with charge gain of 16 can be read in ~ 4 microsecond by spending charge gain to shorten the readout time by 4 times, yet integrating same amount of charge at column charge amplifiers as in the PPS imager (now the charge gain has dropped to 16/4 = 4). In order to allow all pixels in each row of the C-APS imager get reset for 16 micro seconds, 4 consecutive rows of imager, prior to the line being read, are activated. Shifting control signals down each 4 microseconds, an imager with 3000 rows is entirely read out in just 12 milliseconds, resulting in 83.3 fps. It is noted that increasing resetting window width reduces the exposure time (x-ray integration time) however, for large imagers having thousands of rows the reduction in exposure time is negligible. For example, in the above case the exposure time has dropped from 12 ms to 12 ms – 16 μs.

3. NOISE PERFORMANCE

The pixel and its small signal equivalent circuit for noise performance evaluation has been shown in figure 5, where I_N is the flicker and thermal noise current source of the T_A TFT of the pixel being read in APS readout time when T_S is OFF [9]. Using a single resistance and a capacitance to model the data line (C_L: 30 pF, R_L: 10 kΩ),

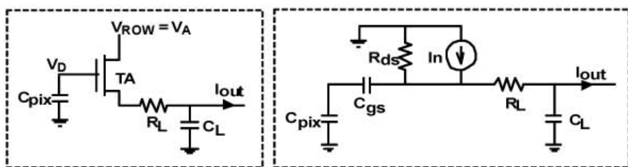


Figure 5. The pixel circuit (left) and its small signal equivalent circuit (right) used in noise analysis.

The reset noise of the pixel capacitor, $I^2_{N\ RESET}$, the thermal noise of R_L and T_A, $I^2_{N\ Thermal}$, and the flicker noise components of T_A, $I^2_{N\ Flicker}$, were calculated as follow [6, 9]. All calculated values are noise components of the output current, I_{out}.

$$I^2_{N\,RESET} = 2g_m\, kT/C_{pix} \tag{2}$$

In which g_m is the transconductance of T_A, k is the Boltzmann constant, and T, absolute temperature. The factor 2 has appeared because of double sampling that doubles the variance of the reset noise [6]. For thermal noise calculation, we simply assumed an ideal low pass filter with bandwidth of f_{eq} = 1 MHz, and drain source resistance of T_A , R_{ds}, to be the ratio of drain current to the drain source voltage, i.e., $I_{D\,TA}/V_A$.

$$I^2_{N\,Thermal} = 4\pi kTf_{eq}R_{ds} = 4\pi kT\, f_{eq}\, I_{DTA}/V_A \tag{3}$$

The flicker noise of the amplifier TFT in both linear and saturation region is calculated using double sampling (DS) as follow:

$$I^2_{N\,Flicker} = \frac{2q\alpha_H I_D^2}{\mu_{FE}C_oWL(V_{GS}-V_T)} \int_0^\infty \frac{1-\cos(x)}{x\left(1+x^2/x_{eq}^2\right)}dx \tag{4}$$

In which α_H is a constant related to fabrication technology, and x_{eq} is $2\pi f_{eq}.t_s$, and ts represents the time difference between acquisitions of the two samples in DS technique. The number of equivalent noise electrons at the input, N_{eq}, is calculated in (5) by referring the total output current to the input using pixel current gain, $\Delta I_{out}/N$ defined in (1).

$$N_{eq} = \frac{\sqrt{I^2_{N\,RESET} + I^2_{N\,Thermal} + I^2_{N\,Flicker}}}{\Delta I_{out}/N} \tag{5}$$

We have previously shown the effect of different biasing conditions on the noise performance of the pixel and reported conditions where N_{eq} is well below 1000 noise electrons [7]. In this report, we have evaluated noise performance of the pixel for different silicon thin films from amorphous to nanocrystalline silicon by changing the field effect mobility in the noise model. The α_H constant was selected to be 1×10^{-2}. The input referred noise was calculated for different values of field effect mobility and the result is shown in Figure 6. It is observed that higher the mobility, better the noise performance of the pixel, and better *SNR*.

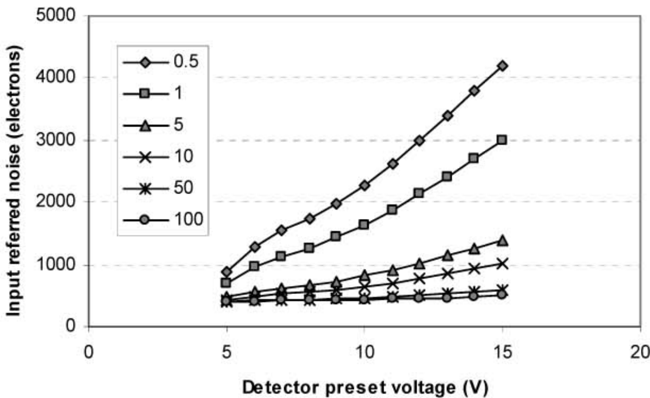


Figure 6. Number of input referred electrons calculated versus detector preset voltage for V_{ROW} equal to 5 V and for different values of field effect mobility (cm^2/Vs).

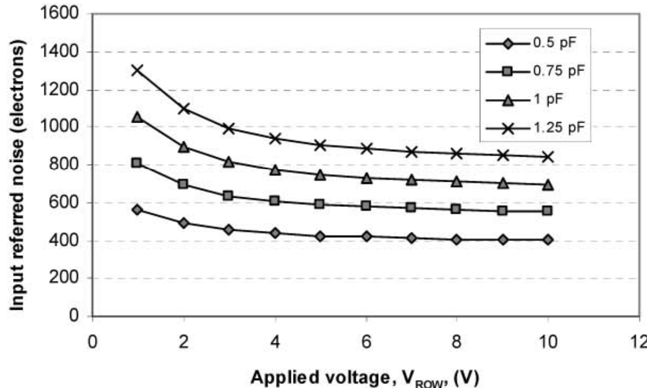


Figure 7. Number of input referred electrons calculated versus applied voltage to V_{ROW} for detector voltage of 5 volts, and field effect mobility of 0.8 cm^2/V.s and for different values of detector pixel capacitance.

The other very important parameter affecting the noise performance of the pixel is the capacitance of the pixel detector. Calculated input referred noise shows that with pixel capacitance of less than 1 pF, N_{eq} is effectively below 1000 noise electrons for low values of detector preset voltage (see Figure 7). This is particularly important and shows for APS pixel designs where there is less space available for the detector, the high pixel gain can compensate the lowered fill factor, as the noise performance becomes better for smaller detectors.

5. CONCLUSION

By implementing a *reset window*, current mode a-Si APS circuits can be operated faster than PPS imagers due to their charge gain capability that can be traded for faster readout time, no matter how long it takes to reset an individual pixel. For example, a 4000×3000 pixel imager can be read out in 12 milliseconds, or, at a frame rate of 83.3 fps using reset time and readout time of 16 and 4 microseconds respectively. So, C-APS flat panel imagers based on amorphous silicon can be effectively used for cone beam CT. In the above example, an FPI with PPS architecture can be read at a maximum frame rate of 20.8 fps. Use of other silicon thin film materials such as nanocrystalline or microcrystalline silicon improves device mobility that can further enhances pixel gain, resulting in higher imaging speed and *SNR*.

2-TFT current mode APS architectures were introduced, showing linear gain over a wide range of exposures. The fact that the novel C-APS architectures are realized using only two TFTs implies that imagers based on 2-TFT a-Si C-APS architectures can be suitable for high resolution high dynamic range fast x-ray imaging applications such as cone beam CT.

6. ACKNOLEDGEMENTS

This work was partially founded by Natural Sciences and Research Council of Canada (NSERC), and Canada Foundation for Innovation (CFI).

7. REFERENCES

1. R. Ning, D. Conover, Y. Yu, Y. Zhang, W.Cai, D. Yang, and X. Lu, "Flat panel detector-based cone beam CT for dynamic imaging: system evaluation", Proceedings of the SPIE, Volume 6142, pp. 808-814 (2006).
2. S.J. Boyce, A. Chawla, and E. Samei, "Physical evaluation of a high-frame-rate extended dynamic range flat panel detector for real-time cone beam computed tomography applications", Proceedings of the SPIE, Volume 5745, pp. 591-599 (2005).
3. T. Xu , J.L. Ducote , J.T. Wong, and S. Molloi, "Feasibility of real time dual-energy imaging based on a flat panel detector for coronary artery calcium quantification", Med Phys., vol. 33, pp. 1612-16122, 16872069 (2006).
4. S. Hirota1, N. Nakao1, S. Yamamoto1, K. Kobayashi1, H. Maeda1, R. Ishikura1, K. Miura1, K. Sakamoto1, K. Ueda, and R. Baba, "Cone-Beam CT with Flat-Panel-Detector Digital Angiography System: Early Experience in Abdominal Interventional Procedures", Journal of Cardiovascular and Interventional Radiology, vol. 29, no. 6, pp. 1034-1038 (2006).
5. K.S. Karim, A. Nathan, J.A. Rowlands, "Alternate pixel architectures for large-area medical imaging", Proceedings of the SPIE, Volume 4320, pp. 35-46 (2001).
6. M.H. Izadi, K.S. Karim, A. Nathan, J.A. Rowlands, "Low-Noise Pixel Architectures for Advanced Diagnostic Medical X-ray Imaging Applications ," Proceedings of the SPIE, Volume 6142, March 2006.
7. F. Taghibakhsh and K.S. Karim, "High Dynamic Range 2-TFT Amplified Pixel Sensor Architecture for Digital Mammography Tomosynthesis', IET proceedings on Circuits, Devices and Systems, June 2006, in press.
8. F. Taghibakhsh and K.S. Karim, "Low leakage a-Si:H thin film transistors deposited on glass substrates using hot-wire chemical vapor deposition", Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, Volume 24, Issue 3, pp. 866-868 (2006).
9. K.S. Karim and A. Nathan, 'Noise performance of a current-mediated amplified pixel for medical imaging', Journal of Vacuum Science and Technology A, Volume 22, pp. 1010-1014 (2004).