Low Power Clock and Data Recovery Integrated Circuits

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

Shahab Ardalan

I understand that my thesis may be made electronically available to the public.

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Abstract

Advances in technology and the introduction of high speed processors have increased the demand for fast, compact and commercial methods for transferring large amounts of data. The next generation of the communication access network will use optical fiber as a media for data transmission to the subscriber. In optical data or chip-to-chip data communication, the continuous received data needs to be converted to discrete data. For the conversion, a synchronous clock and data are required. A clock and data recovery (CDR) circuit recovers the phase information from the data and generates the in-phase clock and data.

In this dissertation, two clock and data recovery circuits for Giga-bits per second (Gbps) serial data communication are designed and fabricated in 180nm and 90nm CMOS technology. The primary objective was to reduce the circuit power dissipation for multi-channel data communication applications. The power saving is achieved using low swing voltage signaling scheme. Furthermore, a novel low input swing Alexander phase detector is introduced. The proposed phase detector reduces the power consumption at the transmitter and receiver blocks.

The circuit demonstrates a low power dissipation of 340μW/Gbps in 90nm CMOS technology. The CDR is able to recover the input signal swing of 35mVp. The peak-to-peak jitter is 21ps and RMS jitter is 2.5ps. Total core area excluding pads is approximately 0.01mm^2.

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Dedication

To My Mom, Dad and brother.

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Glossary

bps	bit per second
CDR	Clock and Data Recovery
CML	Current Mode Logic
CMOS	Complementary metal–oxide–semiconductor
DA	Distributed Amplifier
DCT	Data and Clock Transition
DFF	D-Flip-Flop
DNS	Domain Name Service
DSP	Digital Signal Processing
FD	Frequency Detector
I/O	Input/Output
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
ISI	Inter Symbol Interference
LAN	Local Area Network
LPF	Low Pass Filter
NRZ	Non-Return to Zero

PCB	Printed Circuit Board
PD	Phase Detector
PFD	Phase and Frequency Detector
PLL	Phase Locked Loop
RMS	Root Mean Square
RZ	Return to Zero
SAW	Surface Acoustic Wave
SBDFF	Switched Buffer D-Flip-Flop
SDFF	Switched D-Flip-Flop
SNR	Signal-to-Noise Ratio
SOC	System on Chip
SONET	Synchronous Optical Network
TIA	Trans-Impedance Amplifier
TL	Transmission Line
V/I	Voltage to Current
VCCS	Voltage Controlled Current Source
VCO	Voltage Controlled Oscillator
WAN	Wide Area Network

Chapter 1

Introduction

1.1 Introduction

Advances in technology and the introduction of high-speed processors have increased the demand for fast, compact and commercial methods for transferring large amounts of data. People and businesses rely increasingly on the Internet for Web access, virtual private networks, e-commerce, video streams, training and customer support. According to the International Domain Survey made by Network Wizard, the number of hosts advertised in the domain name system (DNS) jumped from 4 million on January 1995 to 450 million on January 2007 (Figure 1-1)[1].

The amount of information traveling over a long haul wide-area-network (WAN) and a short reach local-area-network (LAN) is growing at the rate of 200 percent each year [2], [3].

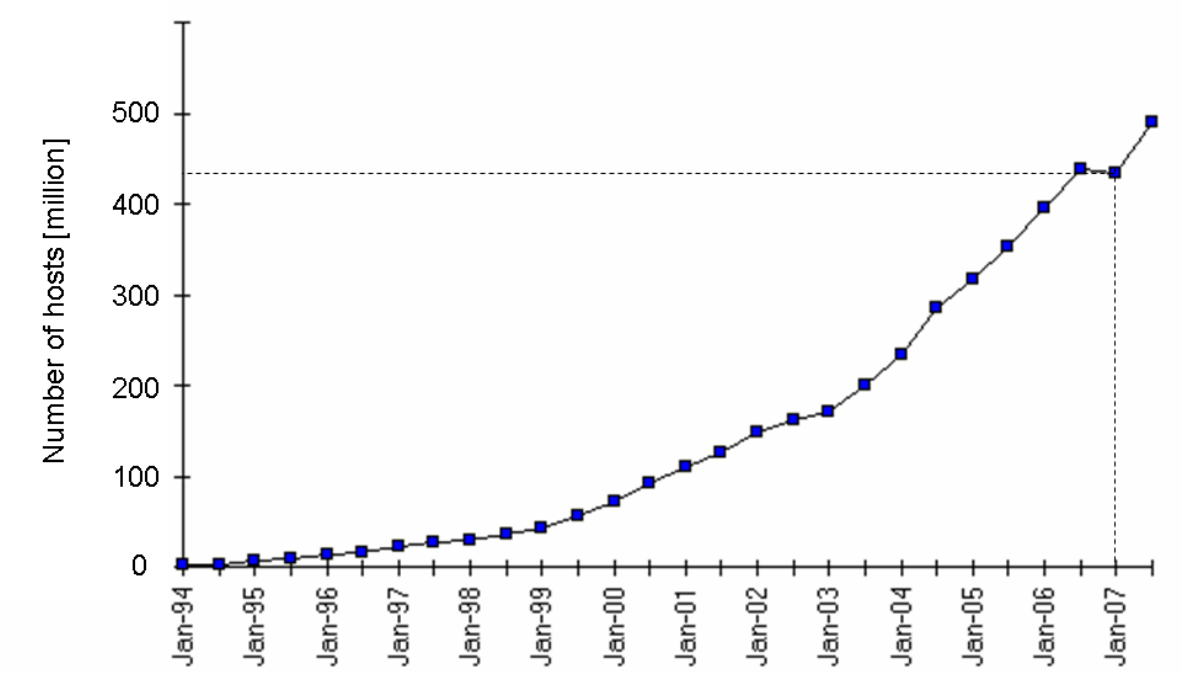

Figure 1-1: Host count over years [1].

A LAN is a computer network covering a small geographic area, like a home, office, or group of buildings (distance less than 10km). The combination of several LANs generates a WAN, which covers larger distance (more than 100km). The block diagram of a present day communication access network is shown in Figure 1-2. The subscribers and local exchanges are connected by a LAN, and these LANs are connected to the central office through a WAN. Copper cables are used between the subscriber and the local exchange. The local exchange includes electronic cross point switches and electro/optical (E/O) converters [4].

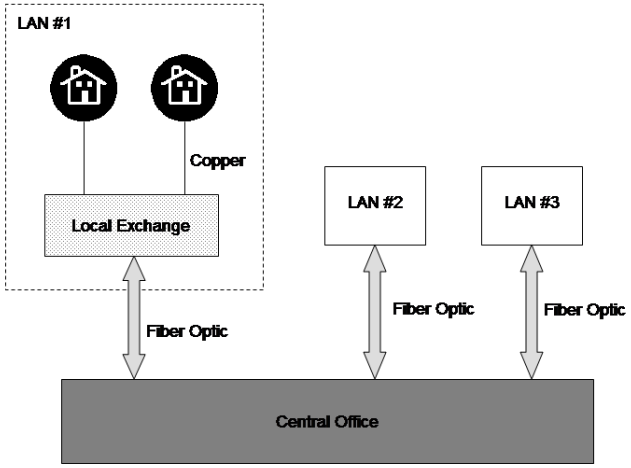

Figure 1-2: Present day data distribution network.

A future communication access network is shown in

Figure 1-3. The optical fiber will extend all the way to the subscriber terminal replacing the current copper cable infrastructure [3]. Employing the high bandwidth media such as fiber optic in local area networks provides the ability of voice and video signal transition.

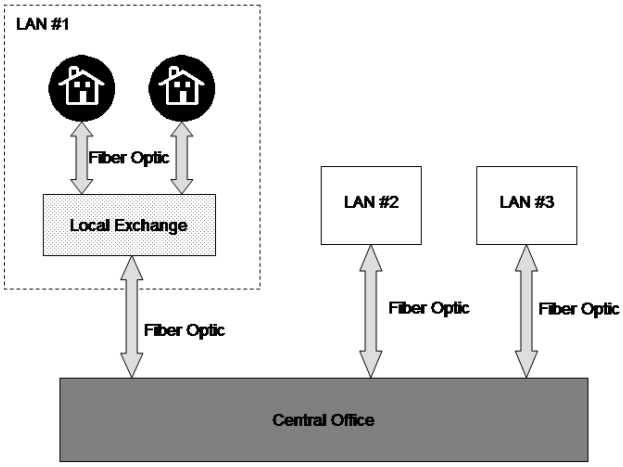

Figure 1-3: Future data distribution network.

Despite the fact that a completely optical transmission system is the objective, there is still need for E/O converters in the implementation of fiber optic transceiver systems. For example, an E/O converter is needed to connect electronic equipment, such as a computer to the other parts of the optical network. Also, E/O converters are used in moderate-speed (less than 10Gbps) single-wavelength fiber optic regenerators [5], [4]. In the high bandwidth media such as fiber optic, the electronic circuits dictate the limit of the data transmission.

Meanwhile when networking companies decide on a cabling system, they make a decision that is critical to the network infrastructure and long term in its horizon [6]. With the ratification of 1000BASE-T in June 1999 (IEEE 802.3 Ethernet Standard for Gigabit Ethernet on Category 5 copper), the one Gigabit Ethernet standard is already being deployed in large numbers in both corporate and public data networks. The 10 Gigabit Ethernet standards are being driven not only by the increase in normal data traffic, but also by the proliferation of new bandwidth-intensive applications. The standard for the 10 Gigabit Ethernet is significantly different in some respects from the earlier Ethernet standards, primarily in that it will only function over optical fiber, and only operate in full-duplex mode, meaning that collision detection protocols are unnecessary. Ethernet can now step up to 10 Gbps, however, it remains Ethernet. The packet format and the current capabilities are compatible with the old version. The 10 Gigabit Ethernet standard provides a significant increase in bandwidth while maintains maximum compatibility with the

installed base of 802.3 standard interfaces. At the present, researchers are designing building blocks for the 10 Gigabit Ethernet. The 10 Gigabit Ethernet does not obsolete current investments in network infrastructure. The standard enables Ethernet packets to travel across synchronous optical networking (SONET) links with very little inefficiency [7].

1.2 A Fiber Optic Transceiver System

In a typical fiber optic transceiver, the data is converted to light pulses by the transmitter and detected by the receiver (Figure 1-4). At the transmitter side of a typical fiber optic transceiver, the high speed digital data is converted to high frequency optical pulses with a laser driver. These ultra-fast laser pulses are transmitted over the fiber optic channel. An ultra-pure glass fiber is used to guide the light.

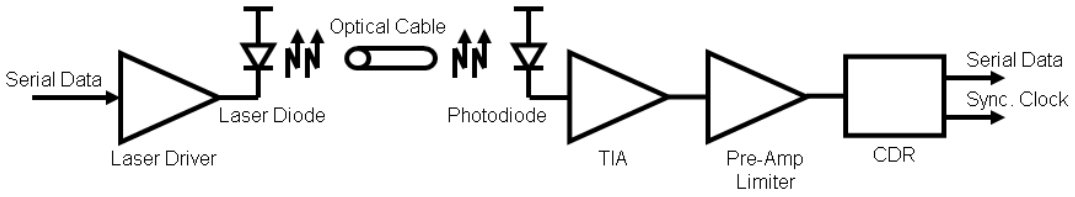

Figure 1-4: Typical fiber optic transceiver.

At the receiver side of a typical optical transceiver, a photo diode converts the optical signal to an electric signal. With a pre-amplifier and a limiter, the voltage pulses, with the appropriate logic levels, are produced at the receiver. A clock and data recovery circuit

(CDR) extracts an in-phase clock from the data. The extracted clock is used to sample the analog waveforms at the optimum sampling time. Figure 1-5 shows the optimum sampling time at a given eye diagram.

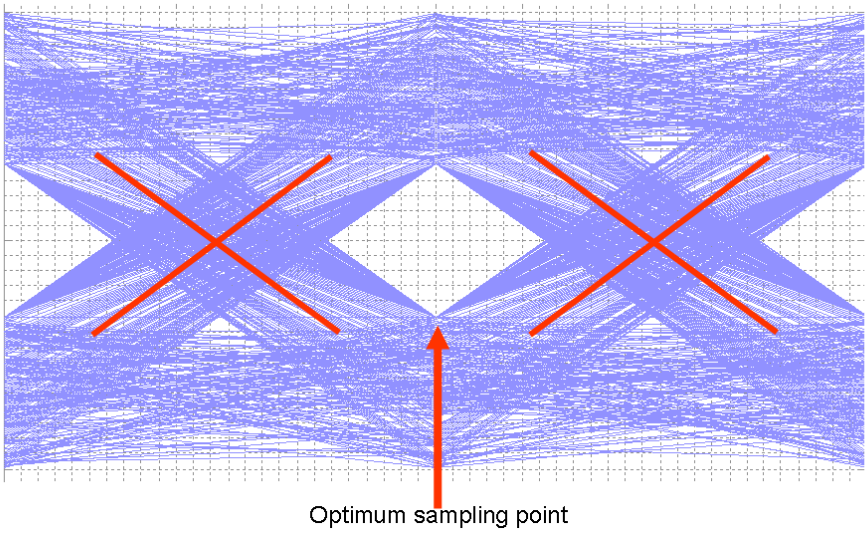

Figure 1-5: Optimum sample point.

1.3 Chip-to-Chip Communication

The desire for higher chip-to-chip bit rates stems from the computer industry. For most of the history of the computer, system performance has been limited by the maximum clock frequency of the CPU. In recent years, improvements in integrated circuit (IC) fabrication technology have led to computer chips running at speeds approaching 4 GHz. This frequency is approximately equal to the bandwidth of a typical chip-to-chip channel on a printed circuit board (PCB). An important performance-limiting factor is the speed at which data can be sent between different chips in the same system. As the operation speed

of the chip increased over the past two decades, the aggregate chip-to-chip bit rate was typically grown by increasing the number of input/output (I/O) pins. Nevertheless, the the aggregate bit rate equals to bit rate per channel multiply by the number of channels [8].

1.4 Clock and Data Recovery Circuit

In order to sample the continuous-time received signal and convert it to a discrete-time sequence, the receiver needs an in-phase clock at the symbol rate. In some digital systems such as on-board chip-to-chip communication, the clock signal is transmitted separately. However, in most digital systems, transmission of a separate clock will increase the expense of the system and make it inefficient. Thus, the necessary timing information should be extracted from the data at the receiver side.

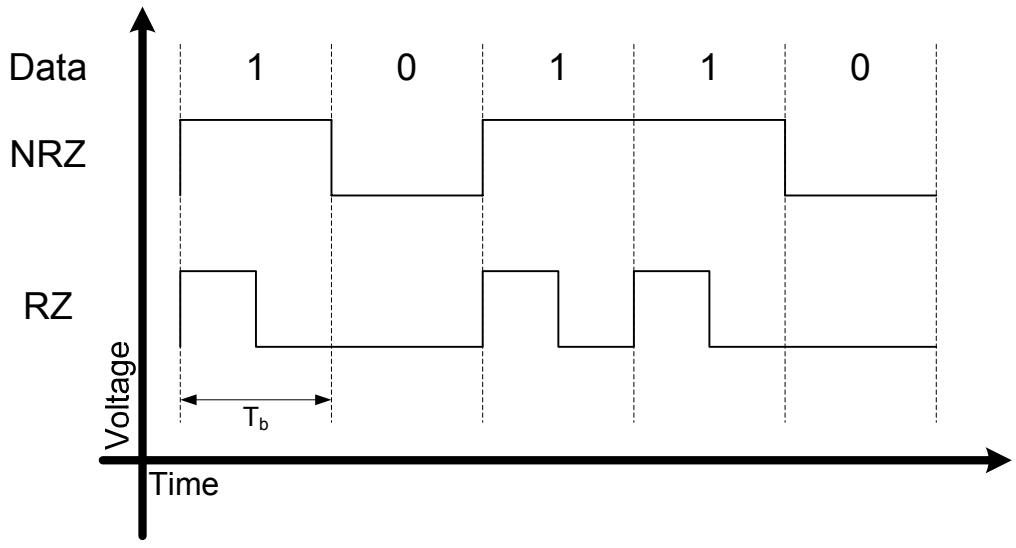

Figure 1-6: NRZ and RZ data stream.

If the spectral energy of the incoming data is not zero at the clock frequency, such as return-to-zero (RZ) signals (Figure 1-6), the timing reference can be extracted by simply passing the data through a band-pass filter with a center frequency equal to the symbol rate.

The autocorrelation function (R_X) of the signal with a null in its spectrum at the clock frequency, such as non-return-to-zero signals (Figure 1-6) is given by (1-1).

$$R_X(\tau) = \begin{cases} 1 - \dfrac{|\tau|}{T_b} & |\tau| < T_b \\ 0 & |\tau| > T_b \end{cases} \tag{1-1}$$

where $\tau = t_1 - t_2$ and T_b is the bit time. $R_X(\tau)$ results into a power spectral density (PSD) function given by the following equation [9]

$$S_X(f) = T_b \left[\frac{\sin(\pi T_b f)}{\pi T_b f} \right]^2 \tag{1-2}$$

The power spectral density function of NRZ data is shown in Figure 1-7. If the input signal has a null in its spectrum at the clock frequency, such as non-return-to-zero (NRZ) signals shown in Figure 1-7, this spectral energy can be generated using a nonlinear element (Figure 1-8).

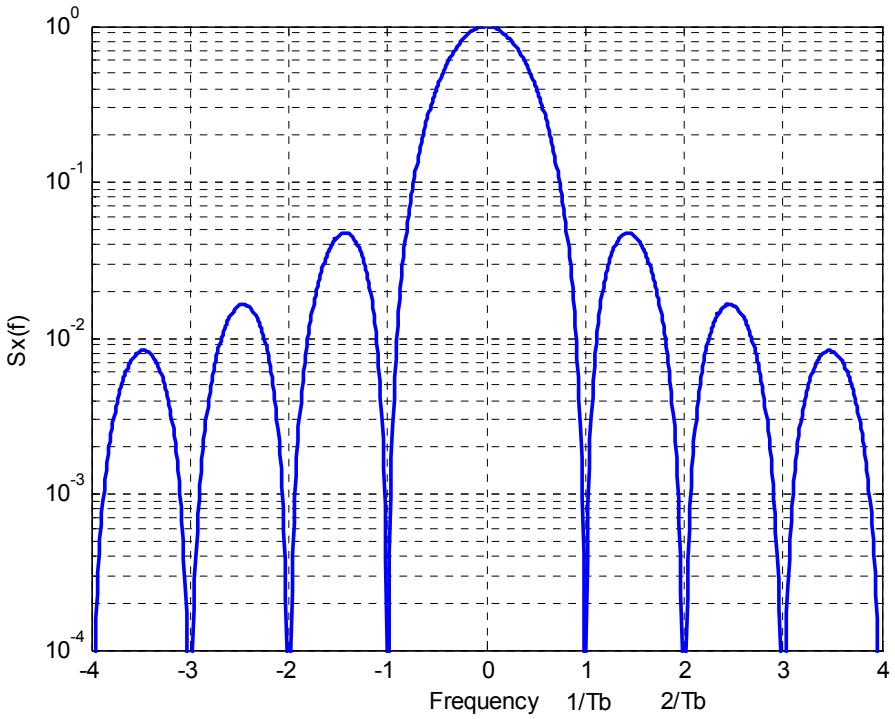

Figure 1-7: Power spectral density of random NRZ data.

Edge detectors and squaring circuits are two of the commonly used nonlinearities. The required band-pass filter can be realized with an LC-tank or with a surface acoustic wave (SAW) filter. This filter is tuned to the desired frequency. Alternatively, this filter can be implemented using a phase-locked loop (PLL). The LC-tanks or SAW filters are neither tunable nor monolithic. A PLL can lock over a wide tuning range and it is also monolithic, making it preferable to the two other filters. This dissertation focuses on the phase-locking CDR architectures.

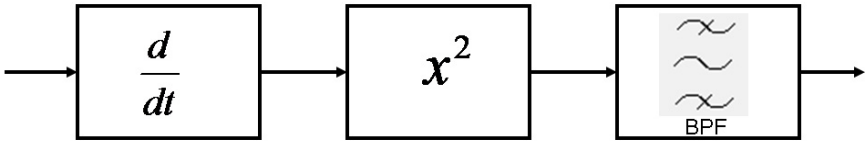

Figure 1-8: Open loop CDR.

1.5 Power Awareness in Serial Data Communication

Reported serial data transceiver systems consume around 20 to 30mW/Gbps. Figure 1-9 shows the power reduction trend over the years, which has been achieved by CMOS scaling.

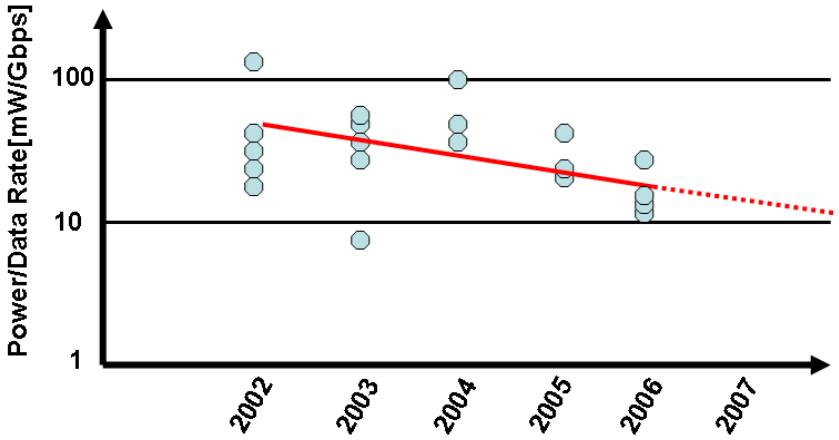

Figure 1-9: Reported power per data rate over years [10].

On the other hand, the power break down of a typical serial link receiver is shown in Figure 1-10.

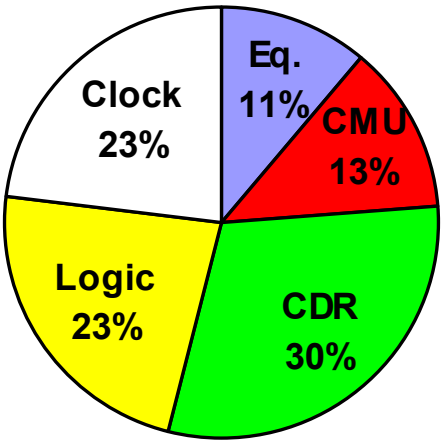

Figure 1-10: Serial data link receiver power break down [10].

The CDR block dissipates around 30% of the total power consumption of the receiver block. High-speed operation in CMOS technology requires high power dissipation. Realizing multi-GHz logic in the phase detector block makes the CDR the most power consuming block among other blocks of the serial data link receiver.

In the last decade, cost and integration of CMOS technology encouraged designers to design high-speed CMOS circuits. However, designing CMOS transceivers faces multifold challenges such as noise, speed, voltage headroom, and substrate noise [9].

1.6 Summary and Motivation

The thesis started with an introduction to data communication and necessity of the CDR in data communication system. Next chapter includes the present clock and data recovery architectures and the building blocks of CDRs. Chapter 3 is devoted to system level

simulation of the different types of CDR systems. Proposed strategies for power reduction are disclosed in chapter 4. Chapter 5 presents the experimental results of two low power CDR circuits and chapter 6 concludes the thesis and suggested area for future work.

The main focus of the thesis is on power reduction of a high speed clock and data recovery. This goal has been achieved by implementing the CDR circuit in static CMOS circuit. However, a conventional static CMOS sampler (DFF) is not able to sense the small input swing data. A new architecture for static CMOS DFF, called Switched DFF (SDFF) has been introduced in chapter 4, and it is able to sample low input signal swing data. Future more to reduce the effect of substrate noise on VCO, a new architecture for low power single ended ring VCO has been disclosed on Chapter 4. The novel low substrate noise VCO uses current time sharing technique to keeps the switching current constant during operation and results in lower ground rail variation. The jitter performance is reduced due to less ground variation. The SDFF and low substrate noise VCO have been implemented in two different CMOS technology and the implementation results are presented in Chapter 5.

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Chapter 2
CDR Architecture

2.1 Introduction

The clock and data recovery (CDR) circuit architectures are categorized in two major groups; open-loop CDRs, and phase-locking CDRs [1].

2.1.1 Open-Loop CDR

The spectrum of an NRZ sequence does not carry a frequency tone at the data rate (Figure 1-7). However, the information about the frequency of the data can be extracted from the spacing between its transitions. These transitions appear as the rising and falling edges of the data signal. If a high-speed data sequence is passed through a differentiator, the resulting signal will carry positive and negative pulses for rising and falling edges of the clock signal, respectively. This differentiated signal does not provide a strong spectral line at the frequency of the data because the polarity of these pulses is random [1].

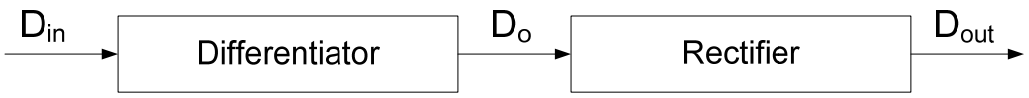

Figure 2-1: Open-Loop CDR Architecture.

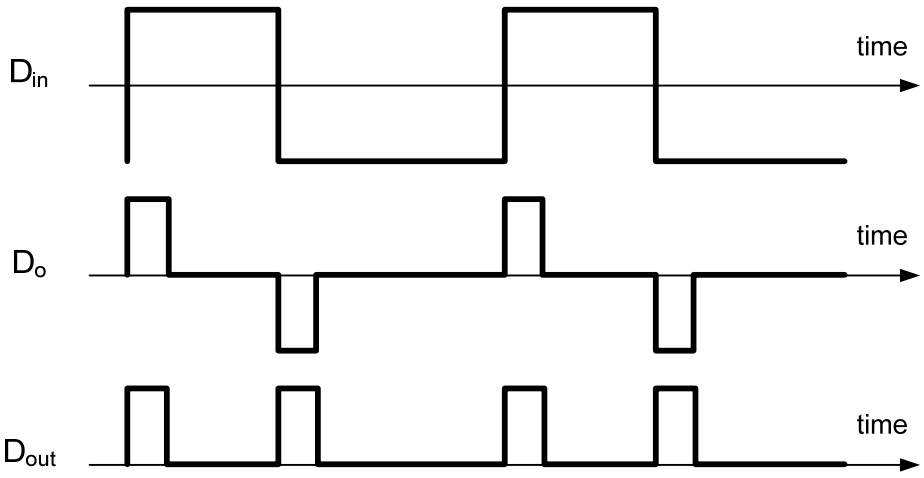

Figure 2-2: Signals of Open-Loop CDR.

Figure 2-1 shows the open-loop CDR architecture. If the output of differentiator is passed through the rectifier, all edges will be converted to positive pulses, as shown in Figure 2-2 (no random polarity).There are some limitations for using this type of CDR in high-speed data commutation systems. Implementing a narrow band band-pass filter in silicon is a challenging task due to the process variation of fabrication. Different architectures, shown in Figure 2-3, had been used to implement the open loop CDR.

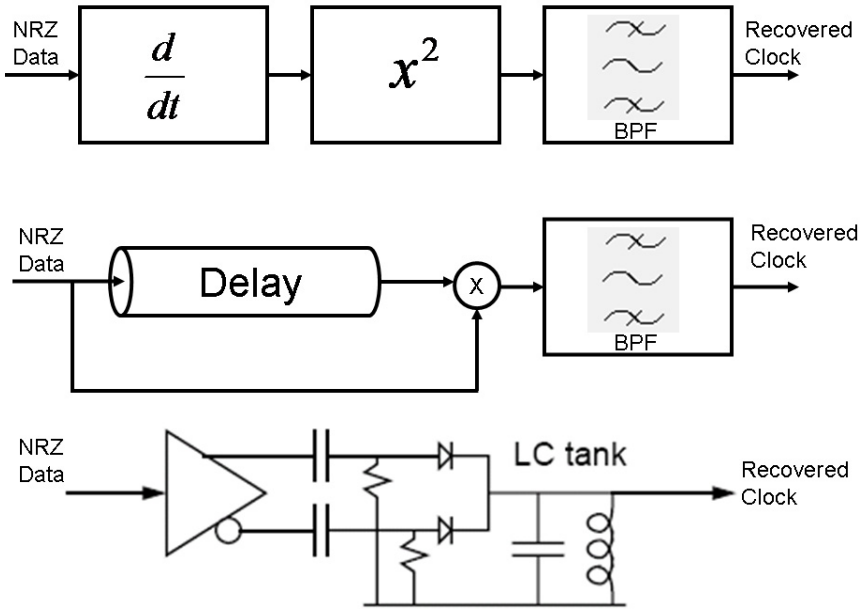

Figure 2-3: Different architecture for Open loop CDR [2].

2.1.2 Phase-Locking CDR

A simple block diagram of a PLL is shown in Figure 2-4. The Voltage-Controlled Oscillator (VCO) attempts to produce a signal, $Y(t)$, which tracks the phase of the input, $X(t)$. The phase detector (PD) measures the phase error between $X(t)$ and $Y(t)$. This phase error is passed through a low-pass filter (LPF), thus producing the control voltage for the VCO. In the locked state, the output phase tracks the input phase with a constant phase difference. This constant phase error depends on the structure of the LPF and the PD.

The structure of the PLL is simple, but it is difficult to analyze. This is because the system is inherently nonlinear. For small phase errors, however, a linear model for studying the

PLL can be used (Figure 2-5). The behavior of an unlocked PLL is very nonlinear and complicated to analyze. Further work can be found with details in [3], [4].

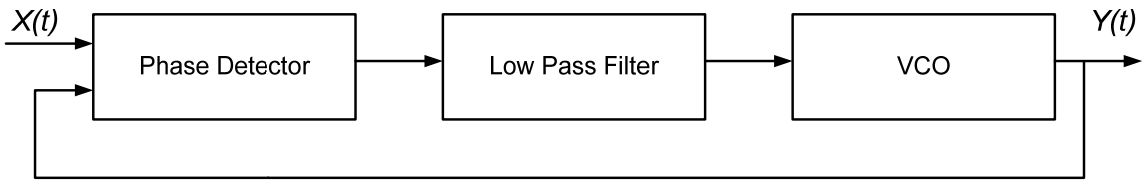

Figure 2-4: Phase-Locking PLL architecture.

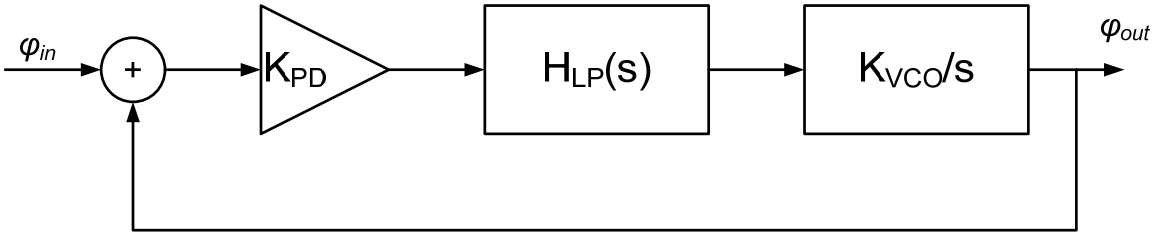

Figure 2-5: PLL linear model.

The PD is the most nonlinear block of the CDR. Most PDs have linear relationships between their average outputs and phase difference inputs for small phase errors (ignoring digital PDs) [3]. Using a simple feedback analysis, the ratio of the VCO phase to the input phase of a PLL that is, the jitter transfer function, can be obtained as:

$$H(s) = \frac{K_{PD}K_{VCO}H_{LP}(s)}{1 + K_{PD}K_{VCO}H_{LP}(s)} \qquad (2\text{-}1)$$

where K_{PD} is phase detector gain, K_{VCO} is the VCO constant and $H_{LP}(s)$ is loop filter transfer function.

The performance of a CDR is very dependent on its jitter transfer function and hence the choice of LPF. Temperature and process variations can cause significant changes in the VCO free-running frequency. These changes could be large such that the PLL may not achieve the locked state. The acquisition behavior of a CDR can be improved by employing a Frequency Detector (FD). In Figure 2-6, a block diagram of an aided acquisition PLL with frequency detector is shown. The FD must be turned off whenever the frequency error is small [5], which is controlled via a lock detector. Complexity of the circuit and extra required blocks are major drawbacks of this architecture.

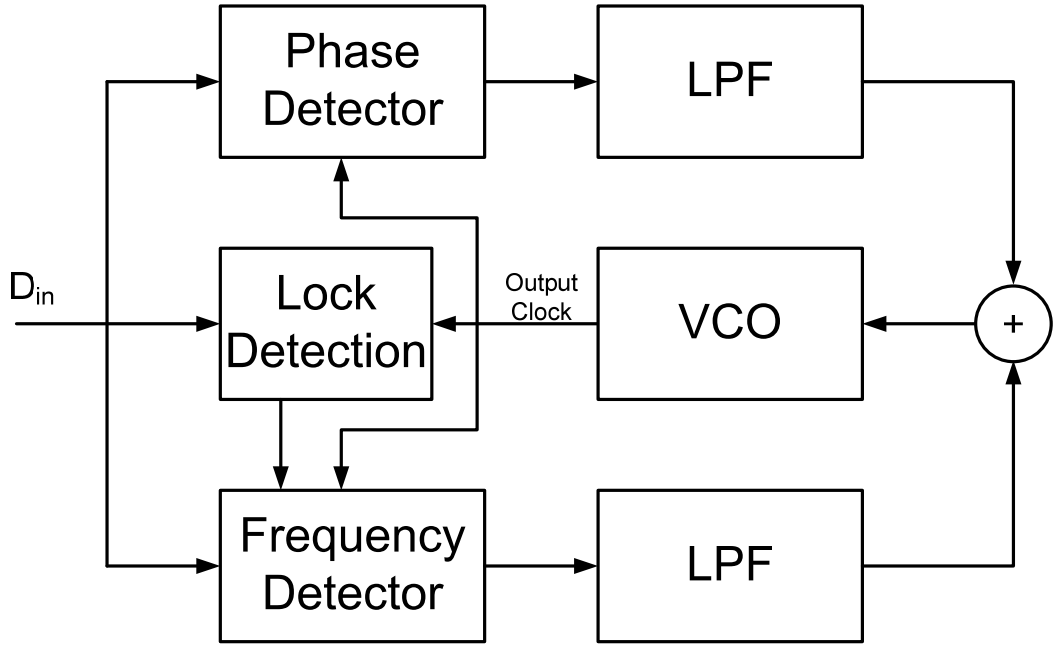

Figure 2-6: Aided Acquisition with Frequency Detector.

2.2 Pre-Amplifier and Limiter

The signal traveling through the channel (wire or fiber) experiences loss before reaching a receiver. Therefore, the received signal needs to be amplified at the receiver before sampling and clock recovery. The amplifier must have a minimal bandwidth to reduce the total integrated noise. However, the limited bandwidth introduces intersymbol interference (ISI). Accordingly proper bandwidth selection is required. Nevertheless, the pre-amplifier must have enough gain to overcome the signal loss and make the signal level detectable. Thus, at high speed of operation and low supply voltage realizing pre-amplifier is a crucial task. Most of the limiters are designed using distributed amplifier concept [6], [7]. The theory of distributed or traveling-wave amplification using discrete transistors is a technique whereby the gain–bandwidth product of an amplifier may be increased. In this approach, the input and output capacitances of the transistors are combined with lumped inductors to form artificial transmission lines (TL). These lines are coupled by the trans-conductance of the devices. The amplifier can be designed to give a flat, low-pass response up to very high frequencies [8]. A distributed integrated circuit design is one of the effective approaches for the design of optical communication ultra-wideband circuits, particularly in CMOS technology [9]. Early distributed amplifiers were implemented using vacuum tubes and high-speed GaAs MESFETs [10]-[14]. Wide-band pre-amplifiers and gain-controlled amplifiers (or limiting amplifiers) are the key building blocks of optical receivers [15]. Since distributed amplifiers (DAs) have no gain-bandwidth trade-off, unlike

other amplifier configurations, they can offer wide-band amplification for high speed application.

Conventional microwave DAs are constructed of two TLs that connect the drain and gate terminals of several field effect transistors. The CMOS interconnects with typical length (less than a few hundred micro meters) are not considered to be TLs at frequencies up to 80 GHz. Thus, the TLs are artificially constructed using a ladder of lumped-element inductors and capacitors in Figure 2-7.

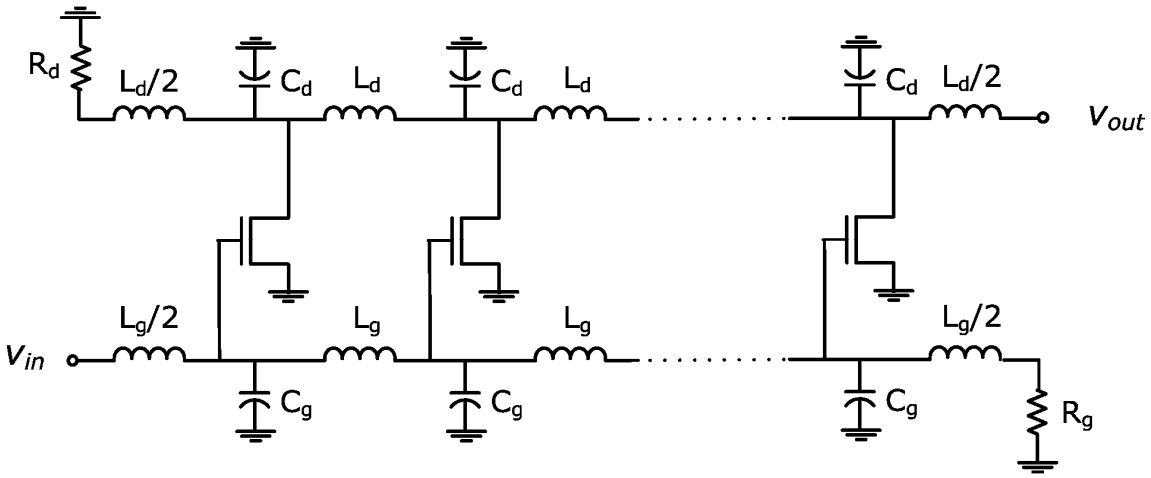

Figure 2-7: Distributed amplifier.

The intrinsic capacitors of transistors – the main cause of bandwidth limitation – are separated by series on-chip inductors to form a low-pass filter topology. This structure provides a relatively low gain due its additive nature of the paralleled gain cell, but achieves wideband amplification due to distribution of the parasitic capacitors in a low-pass LC circuit topology. The main drawback of distributed amplifier topology is its large die area

because it requires several on-chip inductors. Similar to two cascaded low-pass LC filters, the maximum bandwidth of a DA is limited to the cutoff frequencies of the artificial gate and drain TLs. In practice, the bandwidth is further limited by the resistive loss of the TLs and by the output resistance of the amplifier cell gains.

2.3 Phase Detector

Phase detectors generate a DC component proportional to deviation of the sampling point from center of data cycle [2]. In this section different architecture for phase detector is explained.

2.3.1 Linear and Binary Phase Detector

Phase detectors for random NRZ data can be divided into two major groups: linear and digital (binary). For the linear phase detector, each data transition produces an error pulse whose width is linearly proportional to the phase error between the data edge and the clock edge. For small phase errors, the resulting pulse width will be small. This phenomenon makes the circuit design complicated and is often not practical in some technologies.

A digital phase detector produces only two states: clock up and clock down. If no data transition happens, the phase detector keeps its former state and may generate a large amount of data pattern dependent jitter. A three-state phase detector has zero output in the absence of any data transitions. This keeps the charge-pump output unchanged, and, hence, produces less jitter. During the locked state, the digital phase detector produces up

and down signals, which are random in nature, with an average that keeps the phase error zero. These random up and down pulses will increase the phase noise of the recovered clock.

2.3.1.1 Hogge Linear Phase Detector

The Hogge phase detector [16] is popular in the literature and applications. Several modified versions of this phase detector have also been reported [17]. Figure 2-8 depicts the block diagram of Hogge phase detector. The data signal is sampled at clock with a D-flip-flop (DFF) to generate the error signal. The second DFF samples the error signal at opposite phase of the clock to produce the reference signal. The width of the reference signal is fixed at half of the clock period. The width of the error signal is proportional to the phase difference between the clock edge and the data edge.

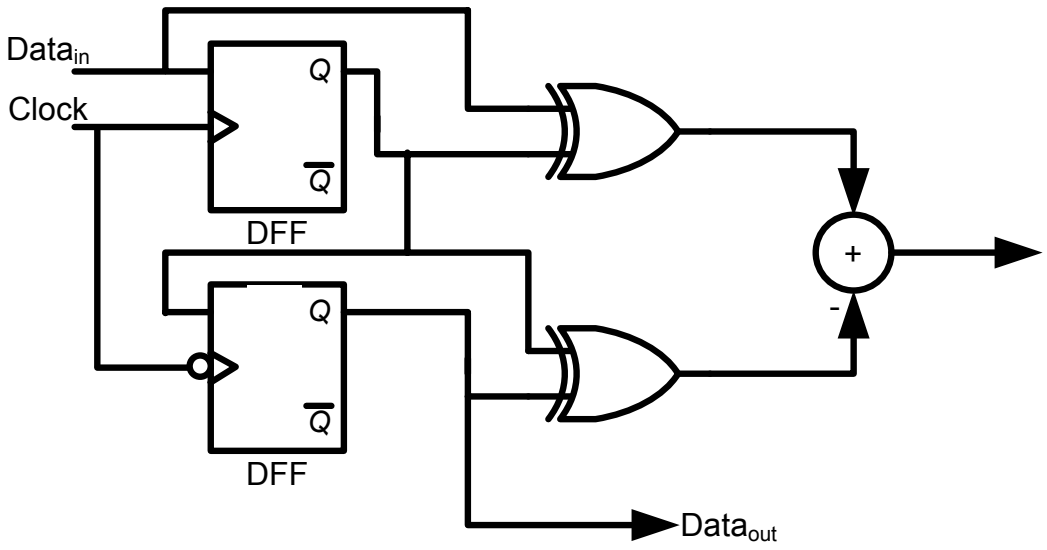

Figure 2-8: Hogge linear phase detector.

The DC value of the difference between the error signal and reference signal is linearly proportional to the phase error. In the absence of any data transition, both error and reference signals become zero and the charge-pump output stays constant.

2.3.1.2 Alexander's Binary Phase Detector

In a binary phase detector, the detected phase error is digitized. If the clock edge is leading the data edge, the down signal becomes high, regardless of the amount of leading phase. If the clock edge is lagging behind the data edge, the up signal becomes high, and the down signal becomes low. If no data transition occurs, the PD keeps its previous state. This phenomenon increases the recovered clock jitter for long periods following ones or zeros. Loop dynamics of a PLL with a binary phase detector are very complicated to analyze. Simplified analysis can be found in [21], [22].

A three-state PD adds a tri-state to the binary PD. Up and down signals are set to be pulses with fixed width. In case of a data transition, proper up or down pulses are generated. If no data transition happens, no up or down pulse is generated. In this case, the charge-pump is off and the charge on the LPF capacitors is not changed. This will keep the VCO control voltage constant and no excess jitter is produced.

A simple algorithm for implementing a binary PD suitable for the NRZ data type was first suggested by Alexander [18]. A block diagram of Alexander's PD is shown in Figure 2-9. With proper selection of the PD logic, the Alexander's binary PD can be modified to a

three-state PD [23]. Table 2-1 shows the proper logic for a three-state Alexander phase detector.

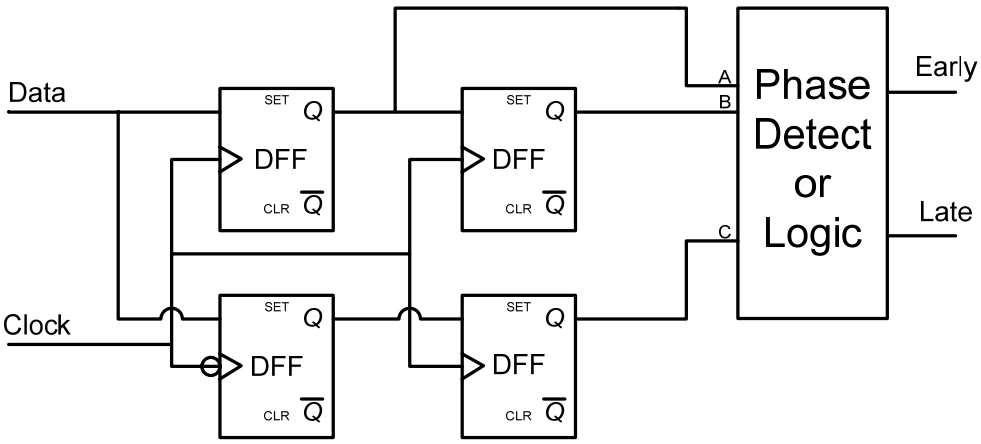

Figure 2-9: Alexander's binary phase detector.

Table 2-1: Logic for a three-state Alexander Phase Detector

A	B	C	
0	1	0	Clock is fast
1	0	1	Clock is fast
0	1	1	Clock is slow
1	0	0	Clock is slow

2.3.1.3 Pottbacker Binary Phase Detector

The Alexander phase detector samples the data signal on clock0 and clock180 edges. Then the PD logic block decides if the clock is early or late. As opposed to Alexander's PD,

Pottbacker's PD samples the clock with the data signal [5]. A simplified block diagram of this phase detector is shown in Figure 2-10.

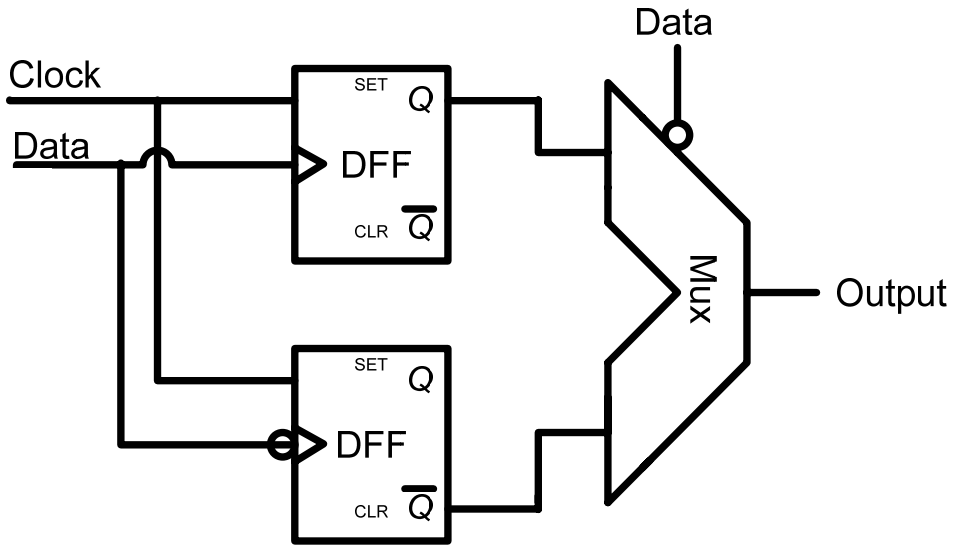

Figure 2-10: Pottbakcer's binary phase detector.

2.3.2 Full-Rate and Fractional-Rate Phase Detector

The architecture of the closed-loop CDR can be grouped into two main categories: full-rate and fractional-rate. The idea of fractional-rate phase detector started by half-rate phase detector. Figure 2-11 shows the signals (clock and data) for full-rate and 1/2 – rate phase detector. There have also been some half-rate linear phase detectors reported in papers [20], [28], [29].

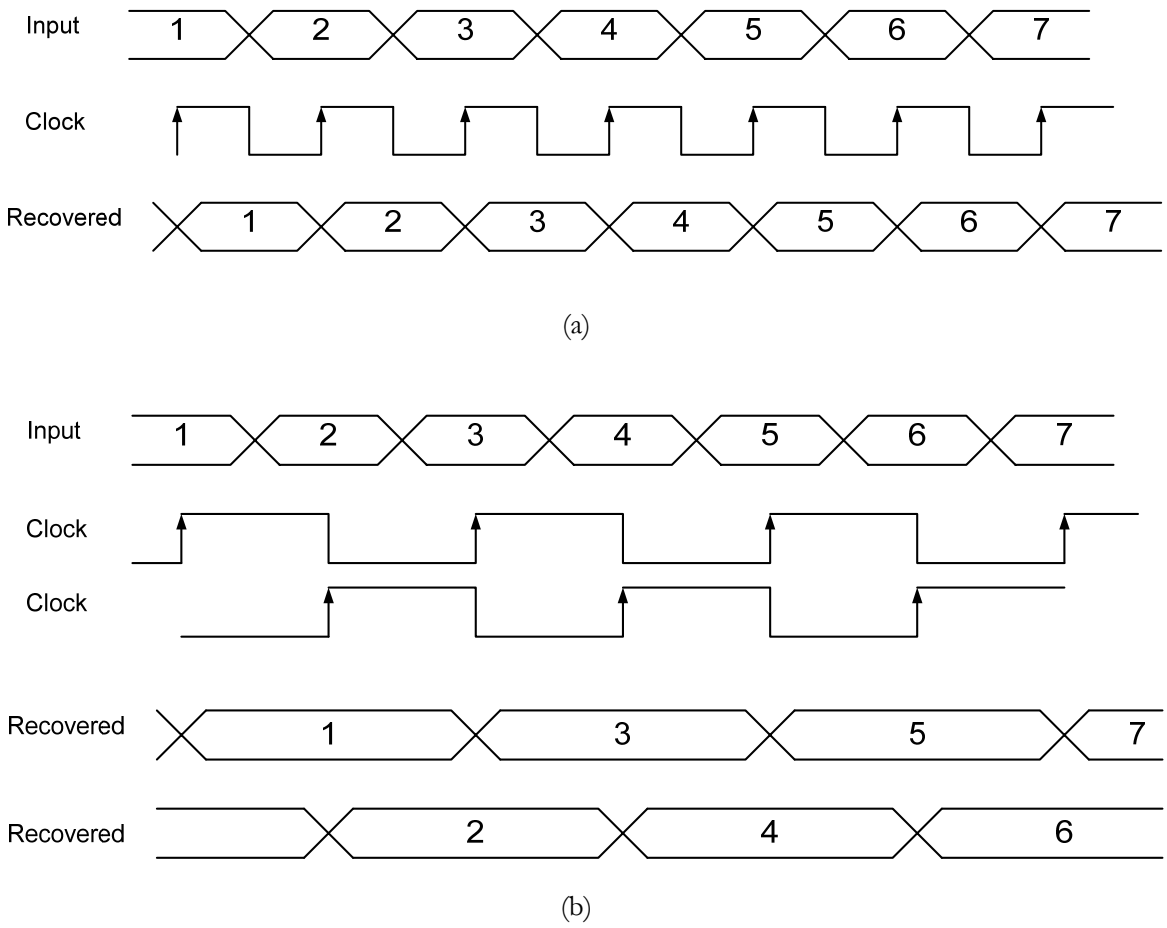

Figure 2-11: Waveforms for full-rate and half-rate CDR: (a) full-rate, (b) half-rate.

In the fractional-rate phase detector the clock frequency is a fraction of the input data rate, hence, the phase detector can be implemented in a technology with a lower bandwidth. Using a fractional-N rate phase detector has the advantage of reducing the required clock frequency by a factor of N. Furthermore, without additional circuitry, the implementation provides a 1:N demultiplxing that simplifies the design of the demultiplexer which is usually needed at the output of a serial receiver.

In design of a fractional rate CDR the major concern is the clock duty cycle mismatch that causes an intrinsic static phase error between the clock and the data optimum sampling point [27].

2.3.2.1 Half-Rate Alexander Phase Detector

A half rate PD uses a clock with frequency equals to half of the bit rate. The key idea in a half-rate PD is to utilize the in-phase and quadrature phases of the half rate clock signal. A block diagram of a half-rate Alexander PD is shown in Figure 2-12.

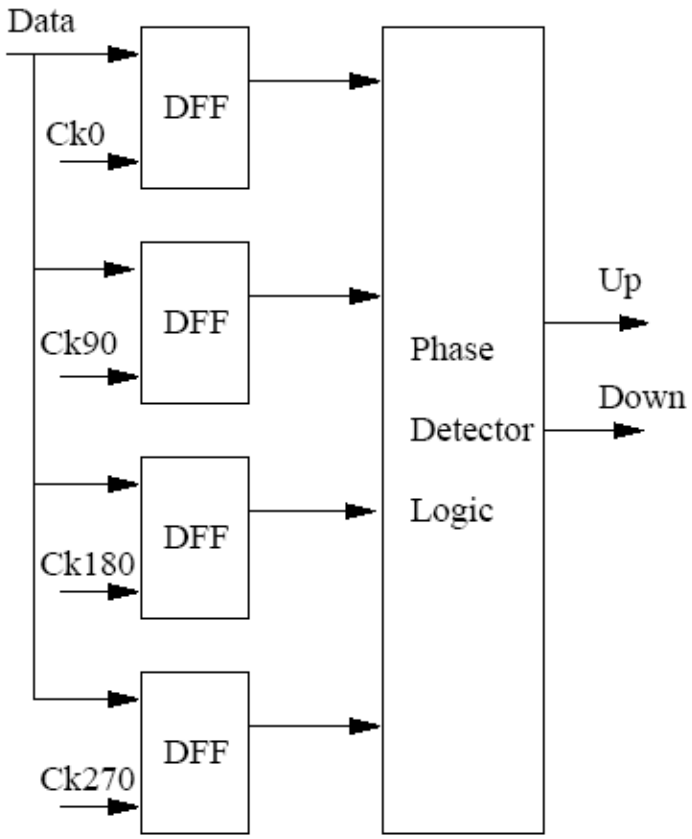

Figure 2-12: Half-Rate Alexander phase detector.

The proper selection of the PD logic is important for the operation of the circuit in high bit rates. The logic should be simple in order to decrease the delay in the loop. Also, the logic circuits should have a symmetric structure to make the delays in the PD matched. Haueneschild in [24] uses a complicated logic that increases the delays in the PLL loop (Figure 2-13). Haueneschild's phase detector has also been implemented in CMOS technology [21]. Ramezani [26] implements a half-rate Alexander PD with a simple logic (Figure 2-14). The AND gates inputs of this circuit are not symmetric, and, hence, it is difficult to match the signal paths through the AND gate.

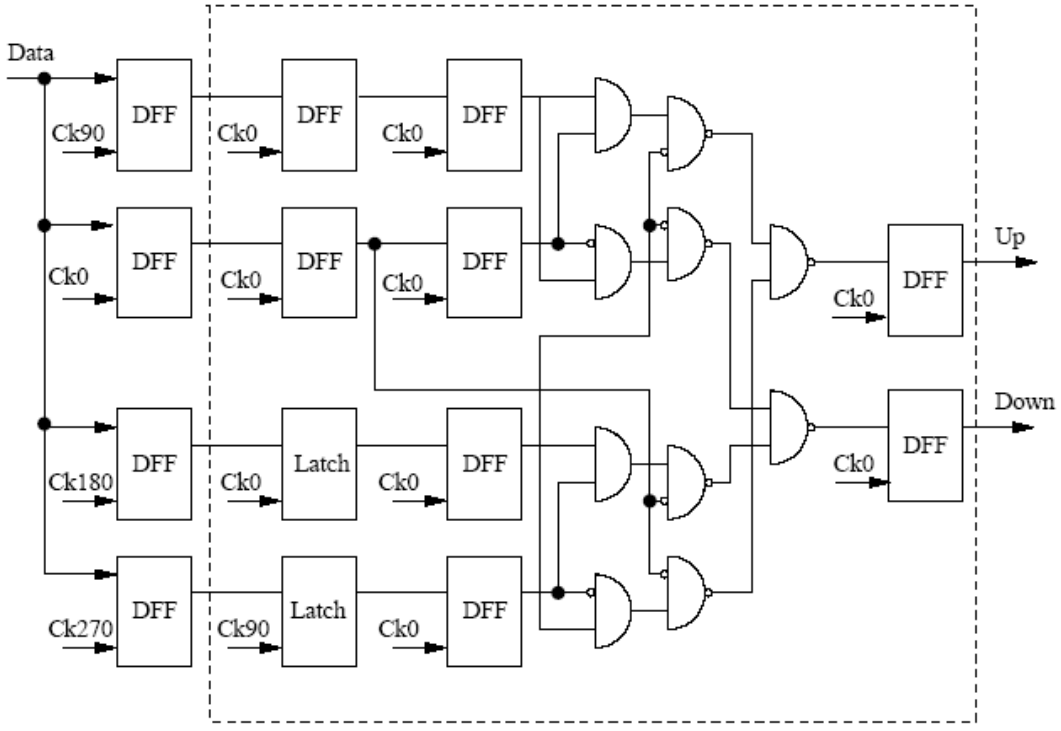

Figure 2-13: Haueneschild's phase detector.

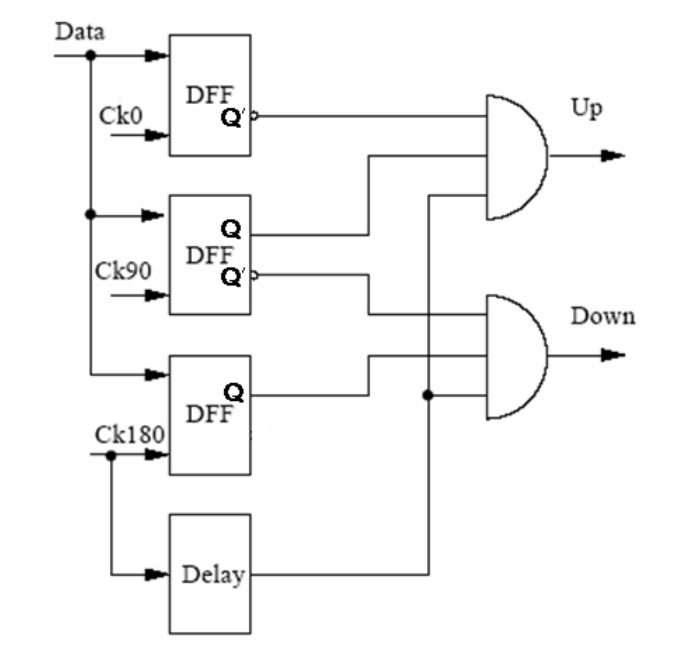

Figure 2-14: Ramezani's half-rate phase detector.

2.3.2.2 Anderson's Phase Detector

A binary version of Anderson's phase detector [19] was used by Savoj in [30]. This phase detector (shown in Figure 2-15) consists of two double-edge triggered DFFs. If during any two sequential in-phase clock edges, any data transition happens, the output of the upper DFF complements. Note that this transition is in-phase with the clock and triggers the output DFF.

The output DFF, using the information provided by DFF2, makes the *up* or *down* decision. Note that DFF2 samples the data at quadrature clock edges. If a data transition happens,

the output of DFF2 identifies whether the data has gone from either high to low or from low to high.

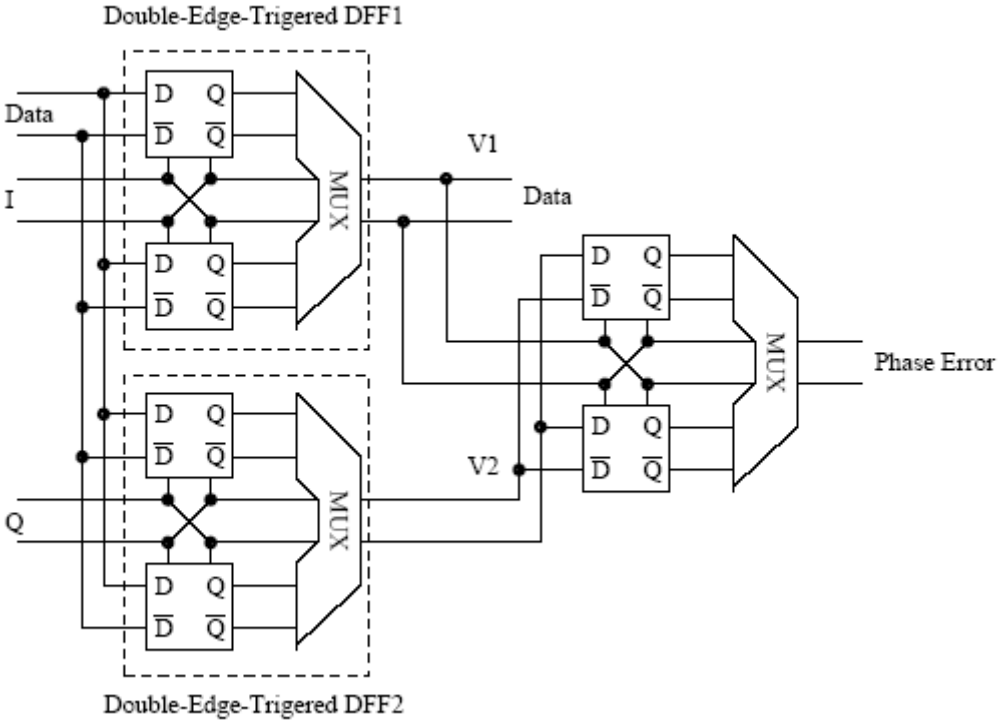

Figure 2-15: Anderson's half-rate phase detector.

Savoj's version of Anderson's phase detector suffers from its two-state behavior. If no data transition occurs, the phase detector keeps its previous state and continually outputs either up or down signal. This causes a significant amount of data-dependent jitter. This phase detector can be modified as shown in Figure 2-16 [28]. This modified version of

Anderson's phase detector is a three-state PD and produces less data-dependent jitter. A linear version of Anderson's phase detector has also been implemented [20].

This phase detector utilizes sample and hold (SAH) blocks instead of DFF and hence has a linear behavior.

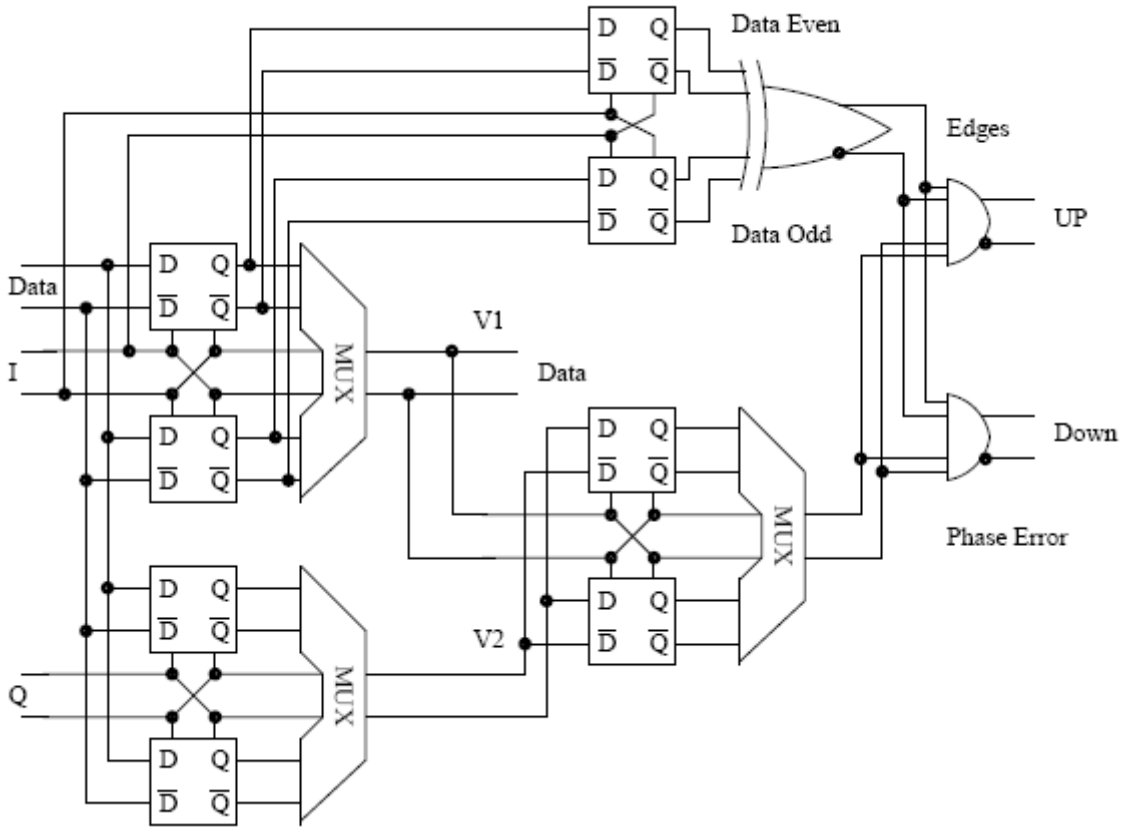

Figure 2-16: Modified half-rate Anderson's phase detector

2.3.2.3 Binary 1/4 Rate-Phase Detector

Another fractional phase detector was published in [25], the proposed architecture employs a clock whose frequency is 1/4 of the full-rate phase detector frequency. This phase

detector (shown in Figure 2-17) is very similar to Alexander phase detector. The PD compares every two consecutive samples by means of an XOR gate, generating a 1 if an edge has occurred. To determine the polarity of the phase error from three consecutive samples, the outputs of two XORs are applied to a voltage to current (V/I) converter, which produces a net current if its inputs are unequal. In lock condition, every other sample serves as a retimed and demultiplexed output.

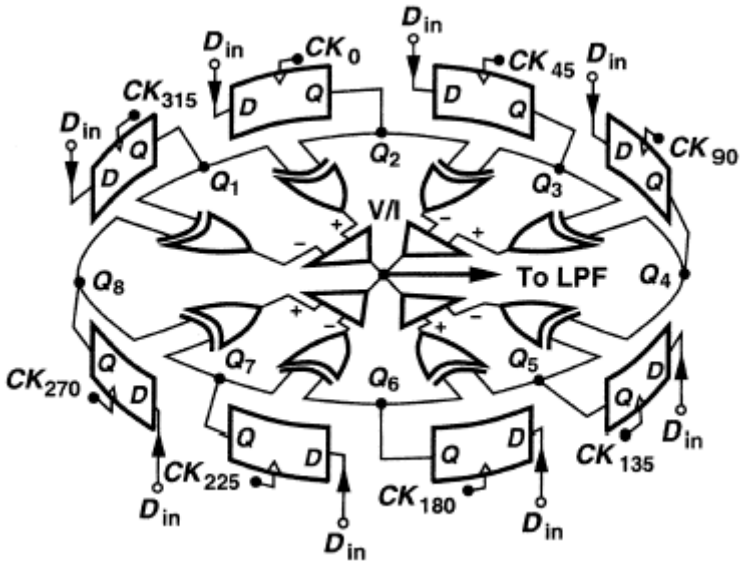

Figure 2-17: Lee's 1/4 Rate-Phase Detector.

It is important to note that, in the absence of data transitions, the DFFs generate equal outputs, and each V/I converter produces a zero current, in essence presenting a tri-state (high) impedance to the oscillator control. This is in contrast to other bang-bang topologies [32], [29] that continue to apply a high or low logic level to the VCO during long runs. Therefore, it creates a potentially high jitter at the output [25].

2.3.2.4 Linear 1/8-Rate Phase Detector

Figure 2-18 shows the block diagram of the linear 1/8-rate PD. It consists of eight data sampling latches, a data and clock transition (DCT) detector, and a DCT generator. The linear 1/8-rate PD accomplishes three tasks with no systematic offset: data transition detection, linear phase error detection, and data regeneration. In the latch stage, the incoming NRZ data stream is sampled in each bit at every rising and falling edges of the four half-quadrature clocks. Then, the DCT detector generates the four DCT signals (DCT0–DCT3) and provides the retimed data output (D0-D3) which are the 1:4 demultiplexed data. With the incoming four DCT signals, the DCT generator produces the DT and CT signals to determine the phase error between the data and the clock [31].

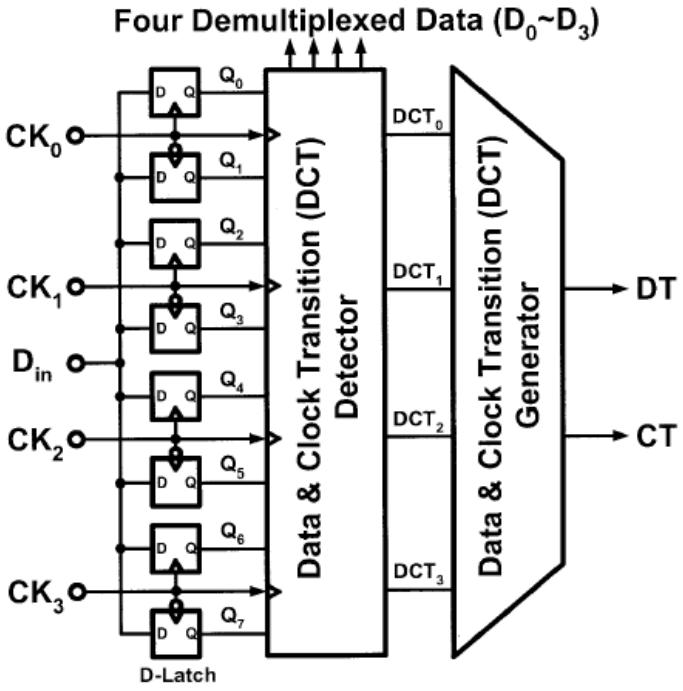

Figure 2-18: Linear 1/8 Rate-Phase Detector.

2.3.2.5 Binary 1/8 Rate Phase Detector

The structure of the proposed 1/8 rate PD is shown in Figure 2-19. The input data signal is applied to 16 master/slave DFFs. Sixteen different clocks are used (together with their complements), where each clock is offset by 22.5 degrees with respect to the adjacent clocks. The phase detector is an improved version of the digital 1/4-rate phase detector published in [25]. Figure 2-20 shows a 10Gbps 1/8-rate binary phase detector characteristic in 0.18μm CMOS process.

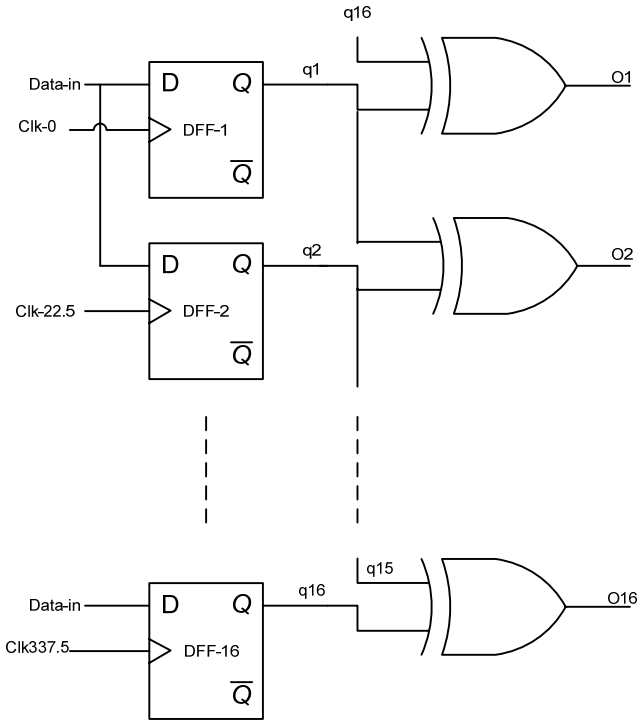

Figure 2-19: Proposed binary 1/8-rate-phase detector.

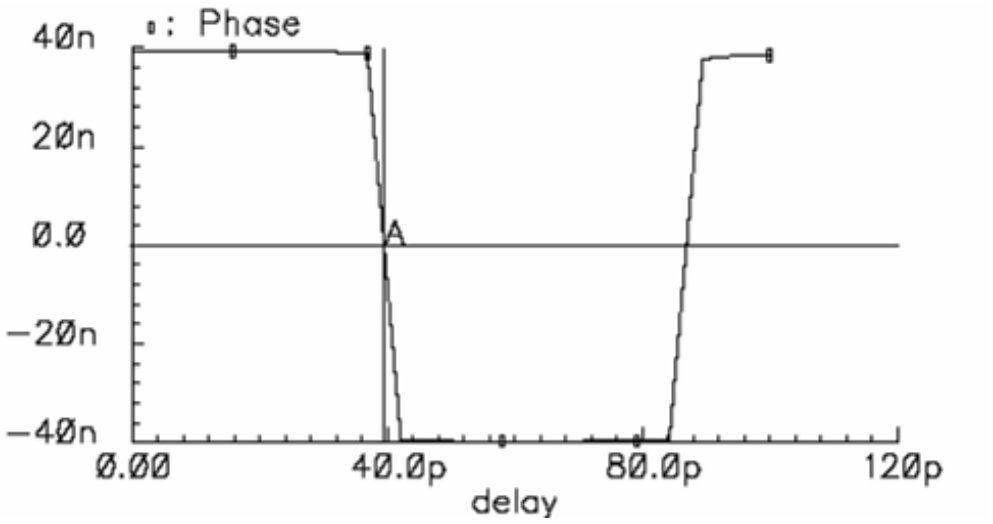

Figure 2-20: 10Gbps phase detector characteristic.

2.4 Voltage-Controlled Oscillators

A Voltage-Controlled Oscillator (VCO) generates the clock signal in a CDR circuit. The design of the VCO directly impacts the jitter performance of the CDR system. The two common methods for designing VCOs for CDR applications are the LC topology; and the ring oscillator.

2.4.1 LC Based VCO

The majority of the LC oscillators have a structure similar to the one shown in Figure 2-21 [1], [34], [27]. Due to the narrow bandwidth of the LC-tank, the oscillator inevitably has a frequency that is equal to the tuned frequency of the tank as long as the gain of the circuit is larger than one. To tune the oscillator, a varactor is used in conjunction with LC

structure. Changing the control voltage (V_C) changes the varactor capacitance and it results in variation of the LC oscillator center frequency.

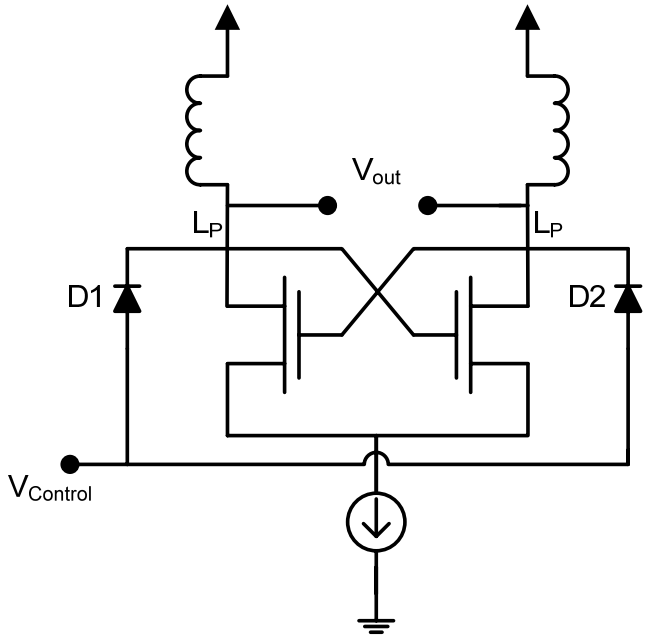

Figure 2-21: Schematic of an LC-tank oscillator.

With an LC based VCO it is possible to achieve frequencies close to f_{MAX} (Transistor cut-off frequency). The disadvantages of using an inductor are the large chip area and the process dependency. Furthermore, this type of VCOs does not provide a wide frequency range to compensate for process and temperature variations and usually needs design and fabrication iteration to achieve the desired frequency range. An LC-based VCO is suitable for application with strict phase noise or jitter requirements such as SONET regenerators [34]. This structure is not economical for LAN applications.

2.4.2 Ring Oscillator VCO

A ring oscillator is formed by using a cascade of odd number of single-ended gain stage in a loop. At the frequency of oscillation total phase shift is 180° and the loop gain of the system is larger than one. An even number of differential delay cells is commonly used for the ring oscillator VCOs to provide quadrature signals in communications circuits. To make the total phase shift of 180°, in an even number differential delay cells, it is necessary to flip the output of one of the delay cells before closing the loop. The schematic of a four-stage differential ring oscillator is shown in Figure 2-22. Parasitic capacitors are usually used with active resistors to provide the phase shift. Control voltage changes the size of the active resistor to change the phase shift and as a result the frequency variation of the oscillator. A ring oscillator VCO has a lower center frequency and larger phase noise compared to an LC based VCO. However, the ring oscillator consumes less chip area and is more suitable for implementation in a CMOS process. Also, the operating frequency of the ring oscillator VCO can be changed faster than the LC one. This makes the ring oscillator VCOs preferable in a binary CDR, where the small delay of the closed loop results in less jitter generation. A ring oscillator VCO is a better choice for applications that do not have strict phase noise or jitter transfer requirements such as LAN [33].

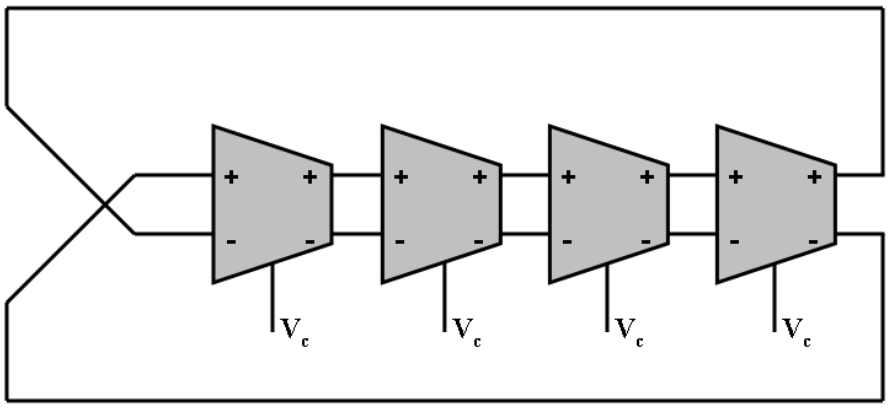

Figure 2-22: Schematic of a four-stage differential ring oscillator.

2.5 Loop Filter and Charge pump

PLLs based on charge-pumps exhibit a number of desired features. First, they do not exhibit false lock. Second, when the system is in lock, the phase error between the VCO output and the input data becomes almost zero [35]. A simple block diagram of a charge-pump PLL [37] is shown in Figure 2-23. The phase detector produces *up* or *down* signals, and the charge-pump injects or extracts the charge stored across the capacitors in the LPF. If the phase detector can not make correct decision about the phase error, no up or down signals should be generated. In this case, the charge-pump does not change the charge of the LPF capacitors, and, hence, leaves the VCO control voltage unchanged.

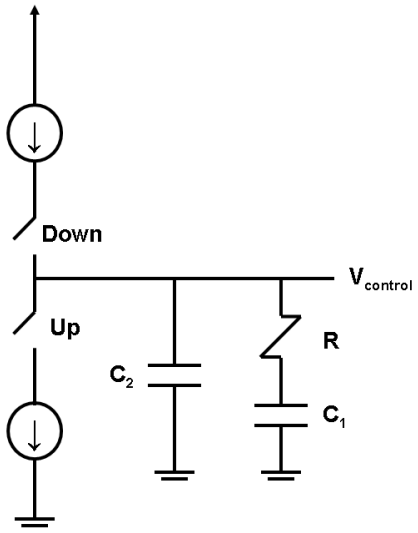

Figure 2-23: Simple Charge-Pump and Loop-Filter.

The charge-pump PLL loop dynamics can be simplified as follows. It is necessary to assume that the phase error between the VCO output signal and input signal does not vary rapidly. In other words the frequency error is small. In this case, the average current flowing through LPF will be:

$$I_{Avg} = \frac{\Delta\phi_{in}}{2\pi} I_{Ch} \tag{2-2}$$

where the I_{Ch} is the charge pump current. Without considering the effect of C_2, which is usually very small compared to C_1, the voltage over the LPF will be:

$$V_{LPF}(s) = I_{Avg}(s)\frac{1+sRC_1}{sC_1} \tag{2-3}$$

The necessary stabilizing zero is provided by the resistor. Every time the charge-pump switches are turned on, the charge-pump current flows through the resistor, which is in series with the capacitor. This creates a ripple in the VCO control voltage. This voltage ripple will then modulate the VCO and add jitter to the recovered clock. The resistor in the LPF is necessary for the PLL loop stability and can not be deleted. In order to suppress these ripples, a smaller capacitor (C_2) is added. The value of C_2 is normally 1/20 of C_1 or even smaller [28]. Introducing this second capacitor decreases the jitter significantly, however, it makes the CDR a third order system. Because C_2 is small, the pole due to this second capacitor is far from the loop resonant frequency, and second order approximation for the loop transfer function is valid [17], [36].

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Chapter 3
Analysis of CDR Circuit

3.1 Introduction

The PLL based CDR is a non-linear system and mathematical analysis is quite difficult. A non-linear theory that could adequately explain the behavior of the loop has not been published yet. The analog CDR analysis can be categorized in two groups:

1) Analog CDR: when the phase detector is linear and the loop filter is analog circuit.

2) Hybrid CDR: when the phase detector is binary and the loop filter is analog circuit.

3.2 Analog CDR

An analog CDR (analog PLL) can be classified based on the number of integrator and the loop filter order. In general, type of PLL is dictated by number of integrators in the loop plus one [1].

3.2.1 Analog CDR Type I

The analysis of analog CDR (or analog PLL) can be divided in two conditions, locked condition and un-locked (tracking) condition.

In the locked condition, a CDR can be analyzed by approximating each block with a linear transfer function.

The time domain function of a VCO is given by:

$$f_o(V_C) = f_c + K_{VCO}V_C \tag{3-1}$$

As the phase detector operates in phase domain, the VCO phase domain equation can be derived as:

$$\omega_o(V_C) = \omega_c + K_V V_C \tag{3-2}$$

The integral of ω_o over the time results in the phase of the VCO.

$$\Delta\omega_o = K_V \Delta V_C \tag{3-3}$$

$$\Delta\varphi_o = \int \Delta\omega_o dt = K_V \int \Delta V_C dt \tag{3-4}$$

Using Laplace transform (3-4) can be derived as

$$H_{VCO}(s) = \frac{\varphi_o(s)}{V_C(s)} = \frac{K_V}{s} \tag{3-5}$$

On the other hand, phase domain function of a linear phase detector can be given by:

$$\varphi_{PD} = K_\varphi(\varphi_r - \varphi_o) = K_\varphi \varphi_e \tag{3-6}$$

then

$$H_{PD}(s) = K_\varphi \varphi_e \tag{3-7}$$

Nevertheless, the low pass filter transfer function is

$$H_{LPF}(s) = \frac{1}{1 + s/\omega_{LPF}} \tag{3-8}$$

Bringing these equations into play results a linear model for analog PLL in lock condition (shown in Figure 3-1).

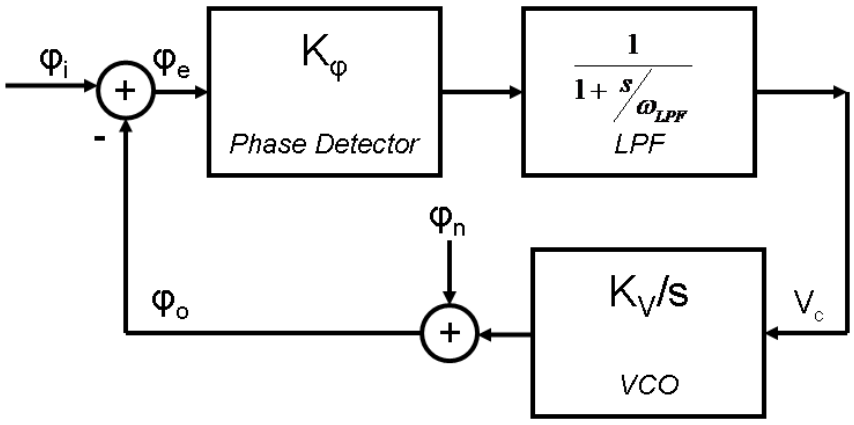

Figure 3-1: Linear model of an analog CDR.

The open loop transfer function, G(s), can be derived as:

$$G(s) = K_{\varphi}\left(\frac{1}{1+\frac{s}{\omega_{LPF}}}\right)\frac{K_V}{s} \tag{3-9}$$

or

$$G(s) = K\frac{1}{\frac{s^2}{\omega_{LPF}}+s} \tag{3-10}$$

where K is the loop gain.

$$K = K_{\phi}K_V \tag{3-11}$$

According to the (3-9, 3-10, and 3-11) there is one pole at s = $-\omega_{LPF}$ and another at s = 0. It can be observed that for low frequency (small s) open loop gain goes to infinity due to existing of a pole at origin. In this case, the feedback circuit passes the small changes in the φ_i to the φ_o. In other words, if the input excess phase varies very slowly, the output excess phase "track" it. However, if the transients in φ_i have decayed, then the change in φ_o is precisely equal to the change in φ_i [2].

Bode plot of an analog CDR based on (3-10) is shown in Figure 3-2. The closed loop transfer function can be written as:

$$H_{Closed-Loop}(s) = \frac{G(s)}{1+G(s)} \tag{3-12}$$

$$H(s) = \frac{\varphi_o}{\varphi_{in}}(s) = \frac{K_\phi K_V}{\frac{s^2}{\omega_{LPF}} + s + K_\phi K_V} \tag{3-13}$$

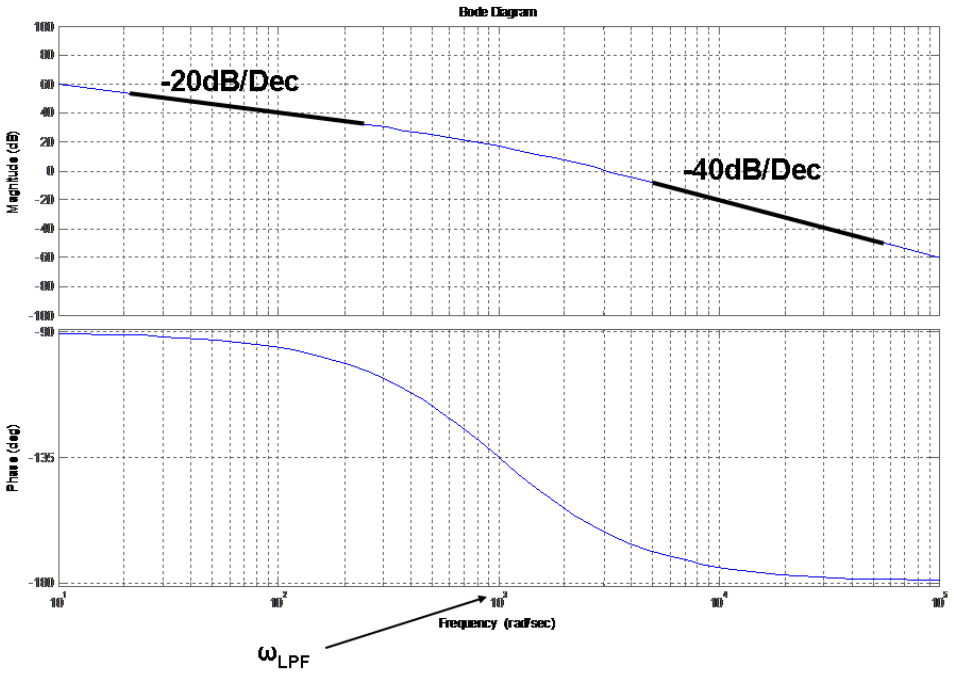

Figure 3-2: Bode plots for analog CDR.

Equation 3-13 can be rewrite in the form of

$$H(s) = \frac{\omega_n}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{3-14}$$

where

$$\omega_n = \sqrt{\omega_{LPF} K_\varphi K_V} \tag{3-15}$$

$$\xi = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_\varphi K_V}} \tag{3-16}$$

The close loop transfer function has two poles (3-17). If ξ > 1, both poles are real and system is over-damped. If ξ < 1, system is under-damped and the poles are complex furthermore the response to an input frequency step $\omega_{in}=\Delta\omega u(t)$ is equal to

$$\omega_{out}(t) = \left[1 - \frac{1}{\sqrt{1-\xi^2}} e^{-\xi\omega_n t} \sin(\omega_n \sqrt{1-\xi^2}\, t + \theta)\right] \Delta\omega u(t) \tag{3-17}$$

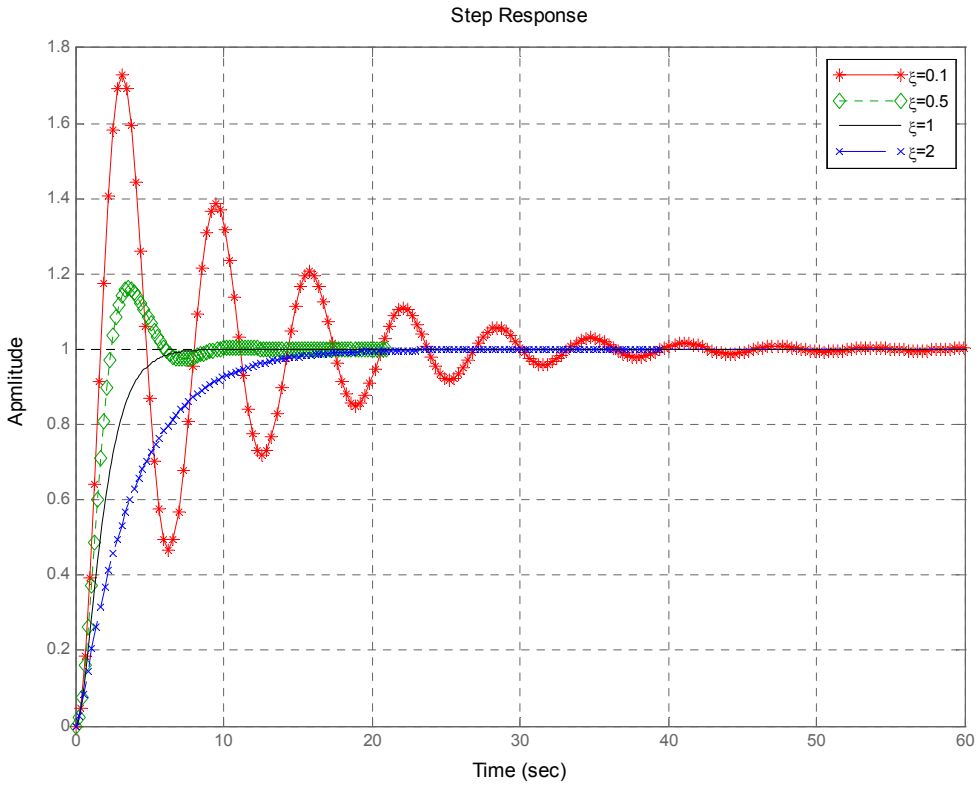

Figure 3-3: Step response for an analog CDR.

Phase error transfer function can be derived as:

$$H_e(s) = \frac{\varphi_e}{\varphi_i}(s) = \frac{s^2 + 2\xi\omega_n s}{s^2 + 2\xi\omega_n s + \omega_n{}^2} \tag{3-18}$$

Above equations show $K=K\varphi.K_V$ and ω_{LPF} cannot be chosen independently. As phase error and damping factor are inversely proportional to K; lowering the phase error inevitably makes the system less stable. These constraints translate to significant phase error between the input and the output as well as a narrow capture range [3]. In summary the analog CDR type-I suffers from trade-offs between the settling time, the ripple on the control voltage of the oscillator, the phase error and stability [2].

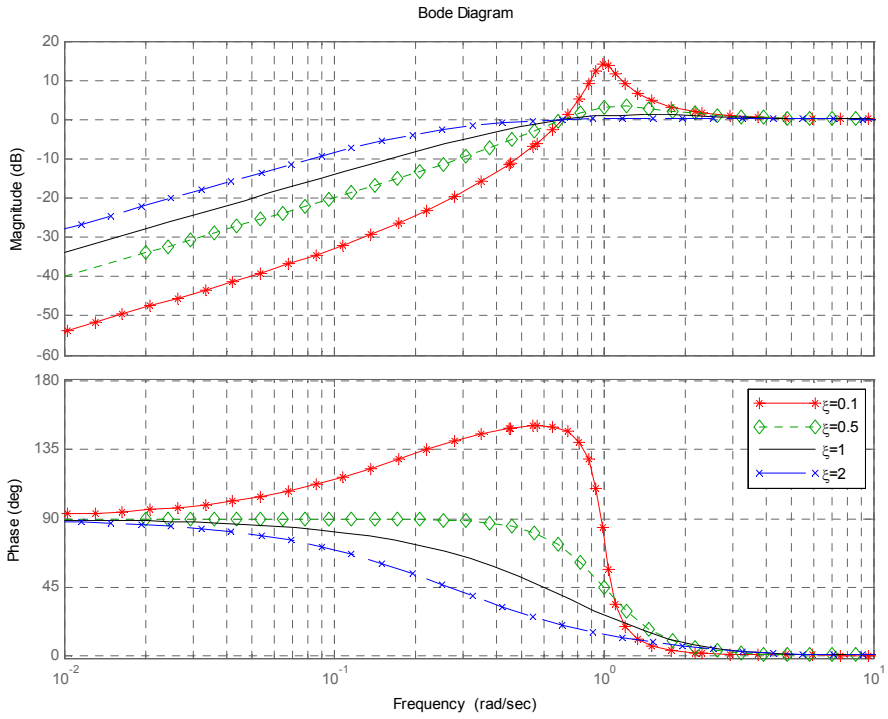

Figure 3-4: Bode diagrams of the error transfer function.

3.2.2 Analog CDR Type-II

The analysis of Analog CDR Type-I (section 3.2.1) shows some shortcomings such as limited acquisition range, and trade-offs between damping factor and ω_{LPF}. Analog CDR type II is used in many modern applications to have more freedom to chose the PLL parameters such as damping factor and ω_{LPF} separately. Figure 3-5 shows a charge pump with associated capacitor.

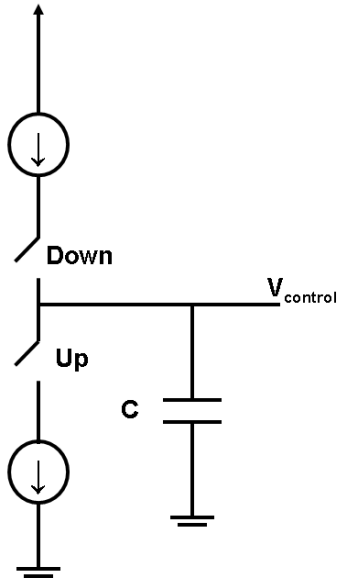

Figure 3-5: Charge pump and capacitor.

The linear model for analog CDR with phase detector and charge pump loop filter is shown in Figure 3-6.

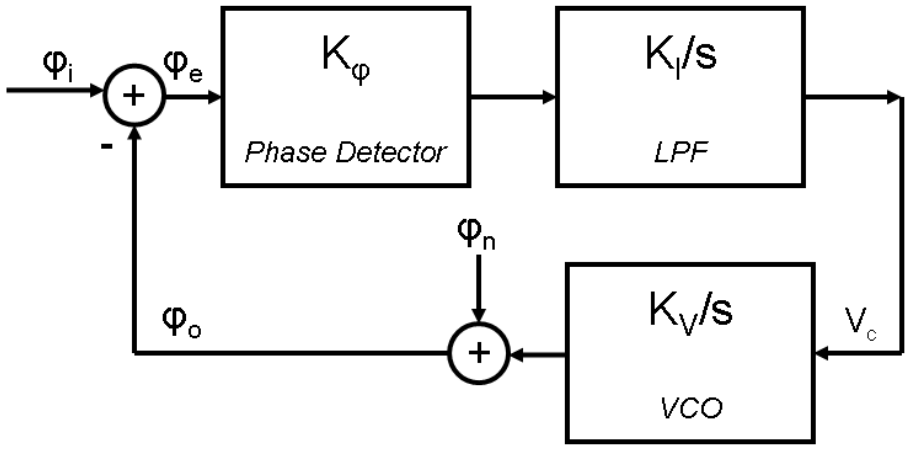

Figure 3-6: Analog CDR linear model block diagram.

The transfer functions of phase detector, charge-pump and loop filter are given by:

$$H_{LPF}(s) = \frac{K_I}{s} \tag{3-19}$$

where

$$K_I = {}^{1}\!/_{C} \tag{3-20}$$

and

$$K_\phi = {}^{I_{CP}}\!/_{2\pi} \tag{3-21}$$

The open loop transfer function is derived as:

$$G(s) = \frac{K_{VCO} K_\varphi K_I}{s^2} \tag{3-22}$$

Therefore, close loop transfer function is equal to

$$H(s) = \frac{K_{VCO} K_{\varphi} K_I}{s^2 + K_{VCO} K_{\varphi} K_I} \tag{3-23}$$

Figure 3-2 shows Bode diagrams for analog CDR with charge pump.

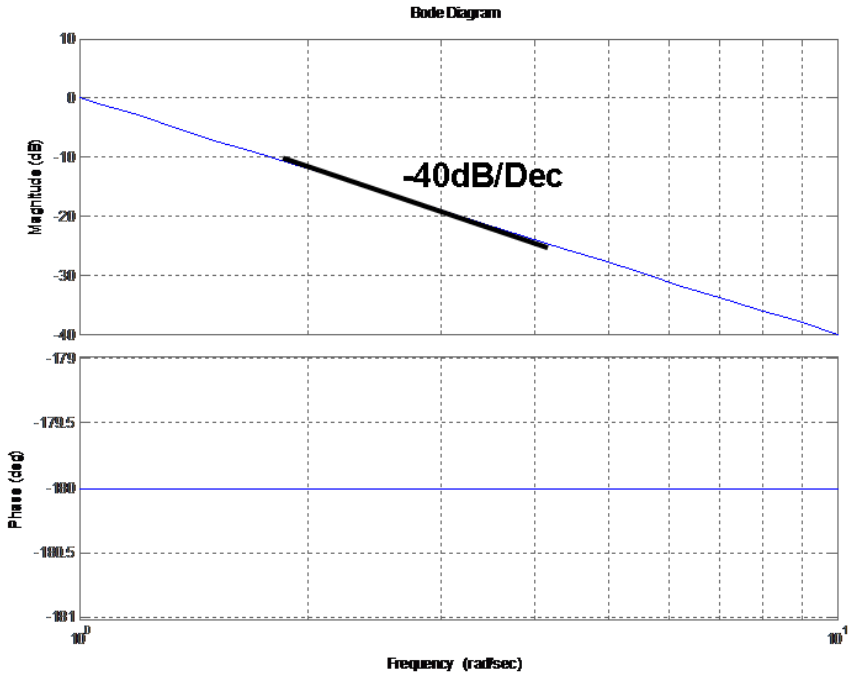

Figure 3-7: Bode diagram for analog CDR with charge pump.

As Bode diagrams show, the two poles results in -180° phase shift allowing the system to oscillate at the gain cross over frequency. To make the system stable we need to decrease the absolute phase shift and one can add a zero to the system.

Figure 3-8 shows the block diagram of PLL based CDR with the new loop filter.

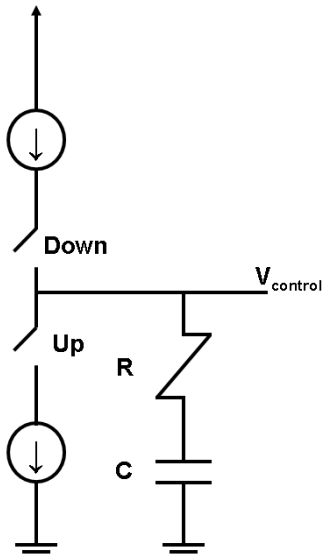

Figure 3-8: charge pump with new loop filter.

The modified loop filter has the transfer function of

$$H_{LPF}(s) = K_p + \frac{K_I}{s} \tag{3-24}$$

then the open loop transfer function is changed to

$$G(s) = \frac{K_{VCO}K_{\varphi}(K_p + \frac{K_I}{s})}{s} = \frac{K_{VCO}K_{\varphi}(K_p s + K_I)}{s^2} \tag{3-25}$$

Therefore, the close loop transfer function is equal to

$$H(s) = \frac{K(1+\frac{s}{z})}{s^2 + K\frac{s}{z} + K} \tag{3-26}$$

where

$$K = K_{VCO} K_{\varphi} K_I \tag{3-27}$$

$$z = \frac{K_I}{K_p} \tag{3-28}$$

Bode diagrams for two different systems one with zero and one with added zero are shown in Figure 3-9. It shows that added zero is able to compensate the phase shift and makes the system stable.

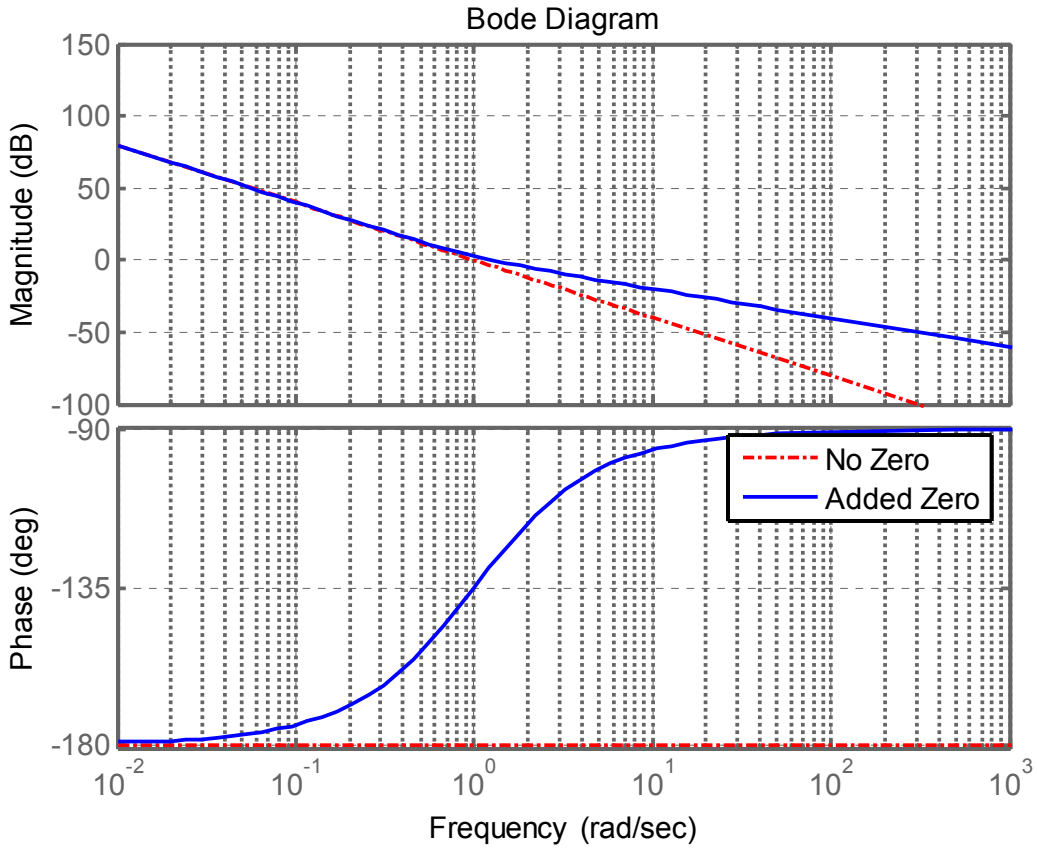

Figure 3-9: Bode diagrams for system with zero and without zero.

Equations (3-25) and (3-26) can be rewritten in the form of

$$G(s) = \frac{2\xi\omega_n s + \omega_n^{\,2}}{s^2} \tag{3-29}$$

and

$$H(s) = \frac{2\xi\omega_n s + \omega_n^{\,2}}{s^2 + 2\xi\omega_n s + \omega_n^{\,2}} \tag{3-30}$$

where

$$\omega_n = \sqrt{K_I K_\varphi K_V} = \sqrt{\frac{I_{IP} K_V}{2\pi C}} \tag{3-31}$$

$$\xi = \frac{\omega_n}{2}\frac{K_P}{K_I} = \frac{R}{2}\sqrt{\frac{I_{IP} K_V C}{2\pi}} \tag{3-32}$$

The closed loop transfer function has two poles and stability analysis is quite similar to type-I. However, Figure 3-10 demonstrates that increasing the open loop gain (K) (3-27) increases the phase margin and system moves toward more stability [4].

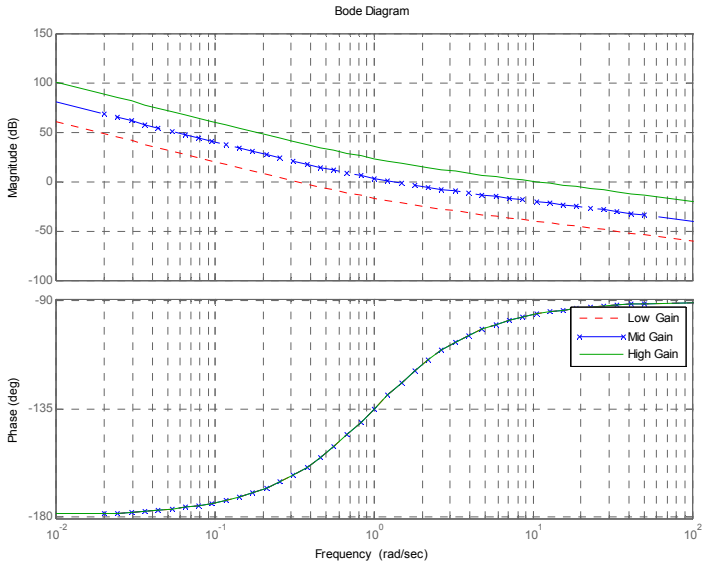

Figure 3-10: Open loop transfer function with different loop gains.

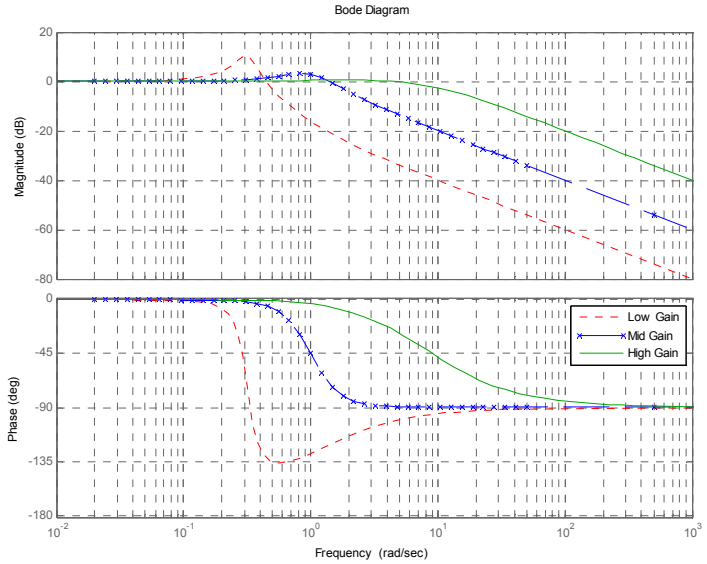

Figure 3-11: Close loop Bode diagram with different loop gains.

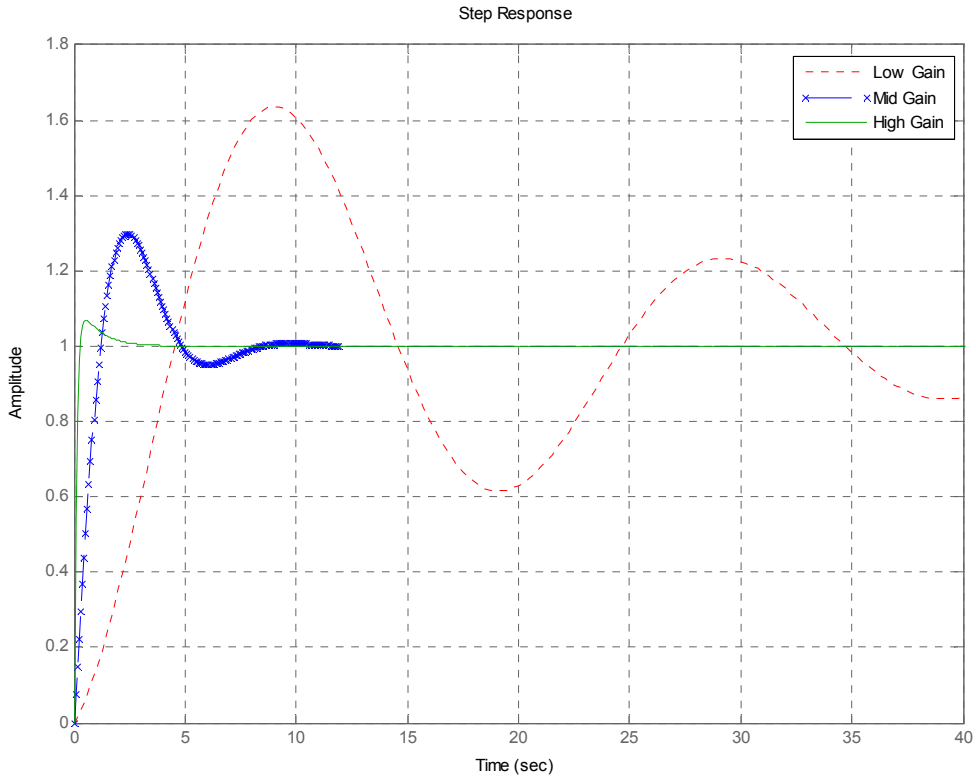

Figure 3-12: Step response to close loop system with different loop gains.

The compensation method (adding a zero) suffers from a critical draw back. Since the charge pump drives the series combination of resistor and capacitor, each time a current is injected into the loop filter; the control voltage experiences a large jump. Even in lock condition there could be an injected current, as a result of mismatch between up and down current sources and clock feed through. A second capacitor (C_E) in parallel to the RC network should be added to the loop to suppress the initial step. Now the loop filter is 2nd

order, yielding a 3rd order PLL-based CDR. If C_E is about one-tenth of C_{CP}, the closed-loop time frequency remain relatively unchanged [2].

The error transfer function can be derived as

$$H_E(s) = \frac{s^2}{s^2 + 2\xi\omega_n s + \omega_n{}^2} \tag{3-33}$$

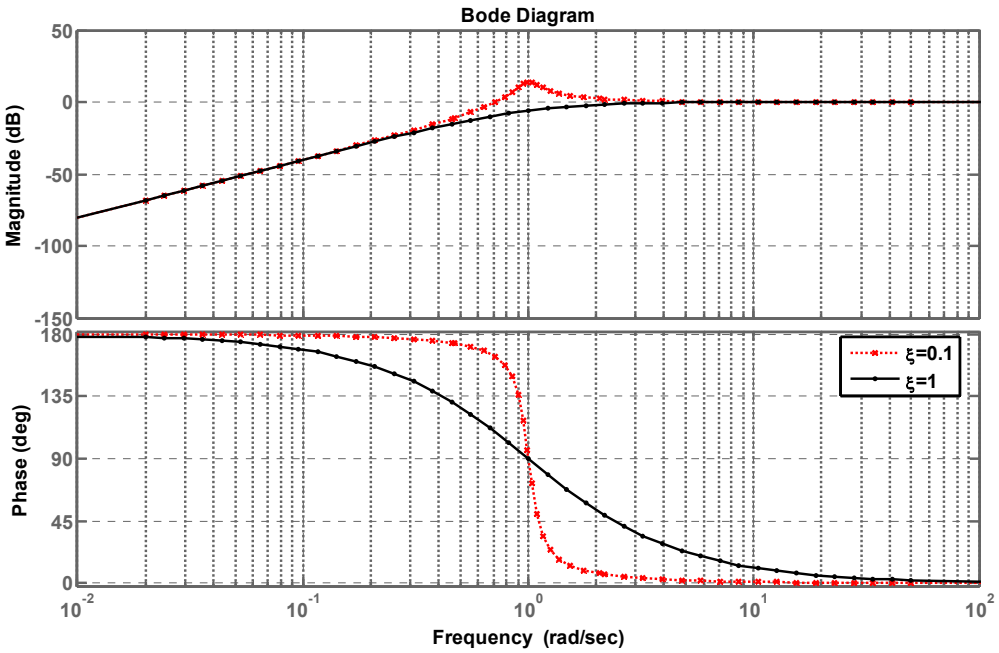

Figure 3-13: Bode diagrams for error transfer function.

Bode diagram of the error transfer function (Figure 3-13) shows the high frequency noise (jitter) from the VCO can travel to the output. Figure 3-14 conceptually summarizes the response of PLL based CDR to input jitter and VCO jitter. Depending on the application

one or both sources may be significant, requiring an optimum choice of the loop band width.

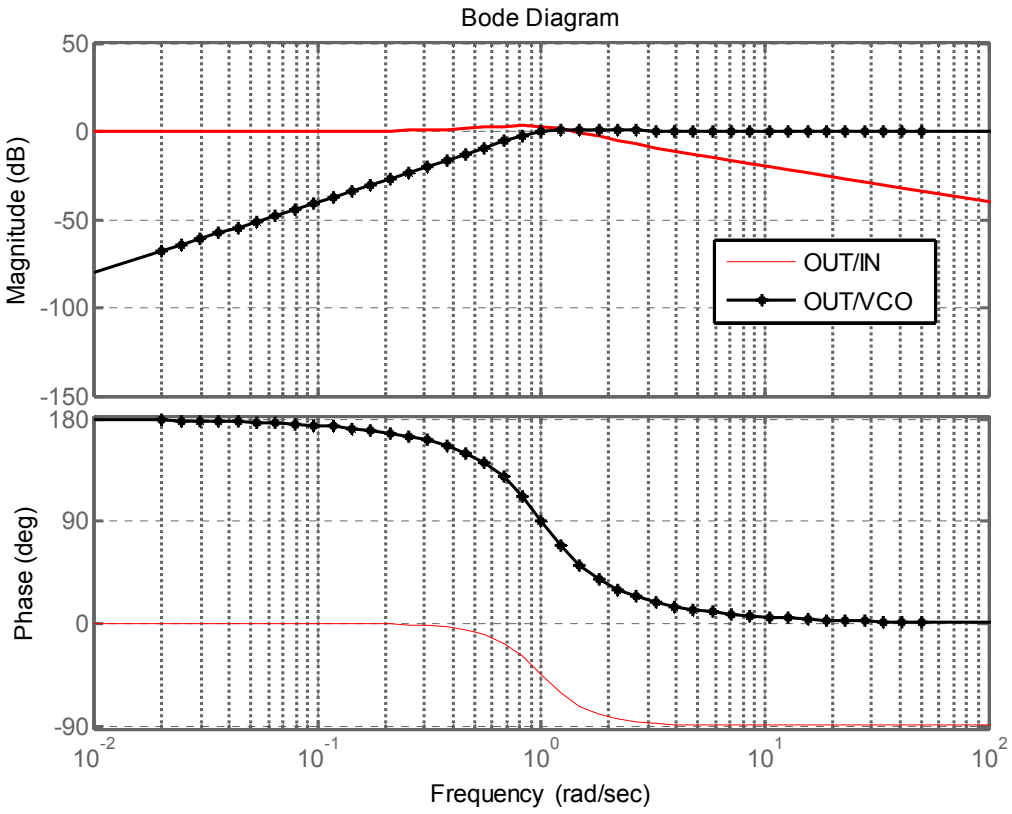

Figure 3-14: Filtering the input jitter and VCO jitter.

3.3 Hybrid CDR

The hybrid CDR employs the binary phase detector and analog loop filter to recover the synchronous clock with input data. The hybrid CDR can be categorized based on the number of the integrator in the loop as follows.

3.3.1 First order hybrid CDR

The 1st order hybrid CDR employs the binary (Bang-Bang) phase detector. The binary phase detector is able to provide only early or later phase information. This non-linearity in the loop structure leads to an oscillatory steady-state and rendering the circuit un-analyzable with standard linear PLL theory [5].

The block diagram and linear model of a 1st-order hybrid CDR are shown in Figure 3-15 and Figure 3-16, respectively.

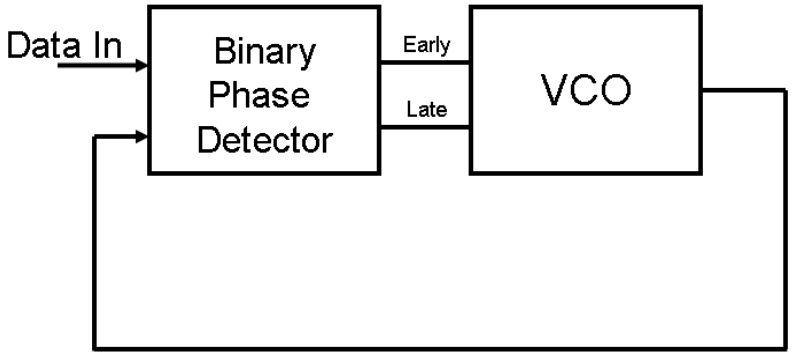

Figure 3-15: The first order hybrid CDR.

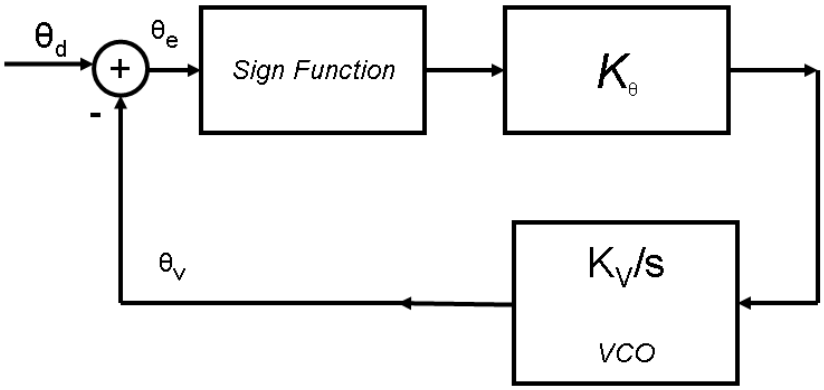

Figure 3-16: Phase linear model of the 1st order hybrid CDR.

According to [5] and [6], the θ_n is defined as the difference between the data phase θ_d and the VCO phase θ_V. The frequency of the incoming data differs from the VCO center frequency by δf . The phase detector is binary phase detector therefore

$$\varepsilon_n = sign[\theta_e(t_n)] \tag{3-34}$$

then the VCO frequency is given by

$$f_{VCO} = f_{nom} + \varepsilon_n f_{bb} \tag{3-35}$$

where f_{bb} is frequency variation range of the VCO and typically is around 0.1% of f_{nom}.

The loop time domain equation can be derived as

$$\theta_V(t_{n+1}) = \theta_V(t_n) + \theta_{bb}\, sign[\theta_d(t_n) - \theta_V(t_n)] \tag{3-36}$$

and the lock range is

$$-f_{bb} \le \delta f \le +f_{bb} \tag{3-37}$$

Meanwhile, the peak-to-peak jitter is given by

$$J_{PP} = 4\pi \frac{f_{bb}}{f_{nom}} \tag{3-38}$$

Equation 3-35 is a starting point for designing the CDR.

Figure 3-17 depicts simulink simulation results showing the locking range and jitter in lock condition. CDR is in locking range and generates relatively small jitter at the output around time interval of 150 to 250. However, when the input frequency passes the upper limit

(1.0005 GHz) the CDR is not able to lock to the frequency and results in output jitter growth.

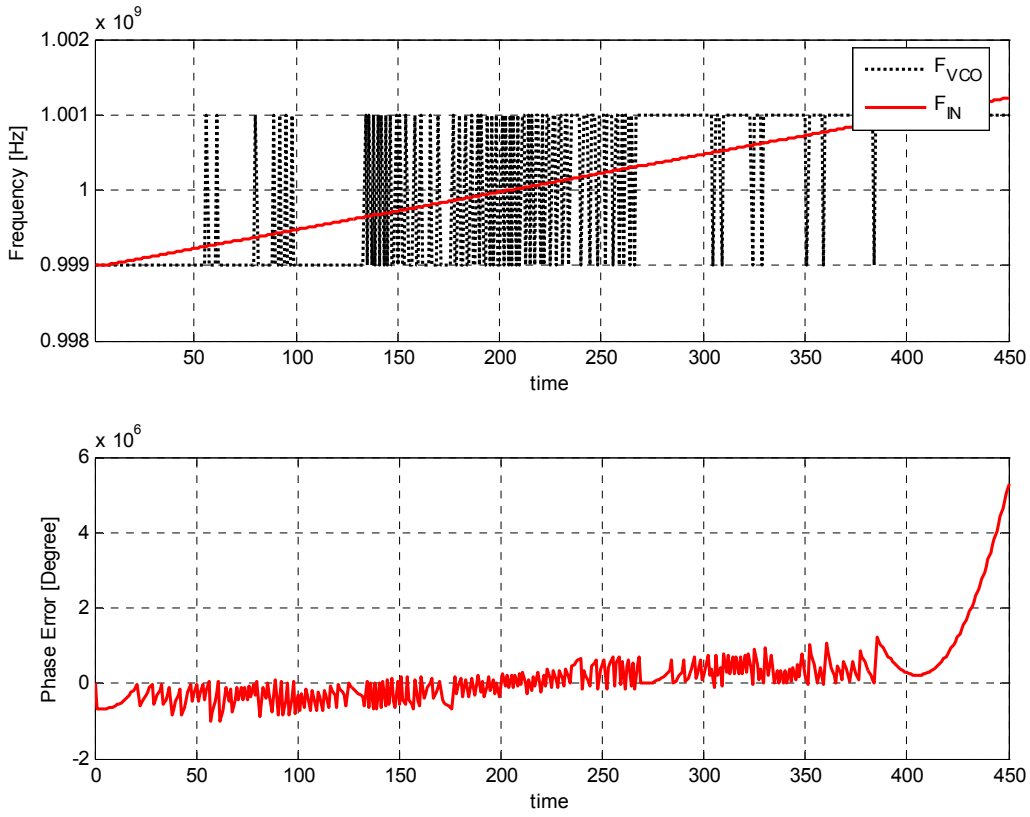

Figure 3-17: Simulink simulation of 1st order hybrid CDR.

3.3.2 Second-order hybrid CDR

The first-order hybrid CDR has only one degree of freedom. All the parameters are controlled by one parameter, f_{bb}. To overcome this problem, employing a second control loop to dynamically adjust the nominal VCO frequency is suggested.

The schematic of a second-order hybrid CDR is shown in Figure 3-18 [5] and corresponding phase model block diagram is shown in Figure 3-19.

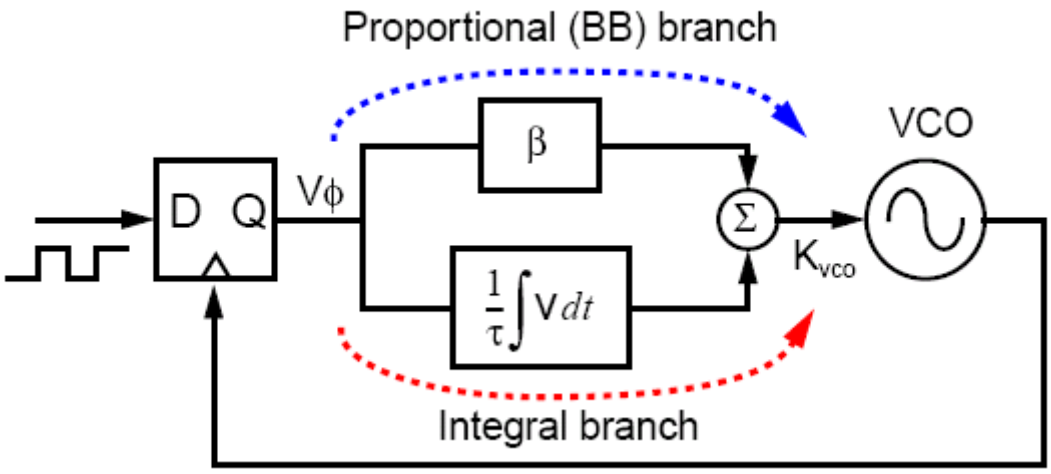

Figure 3-18: Block diagram of the 2nd-order hybrid CDR [6].

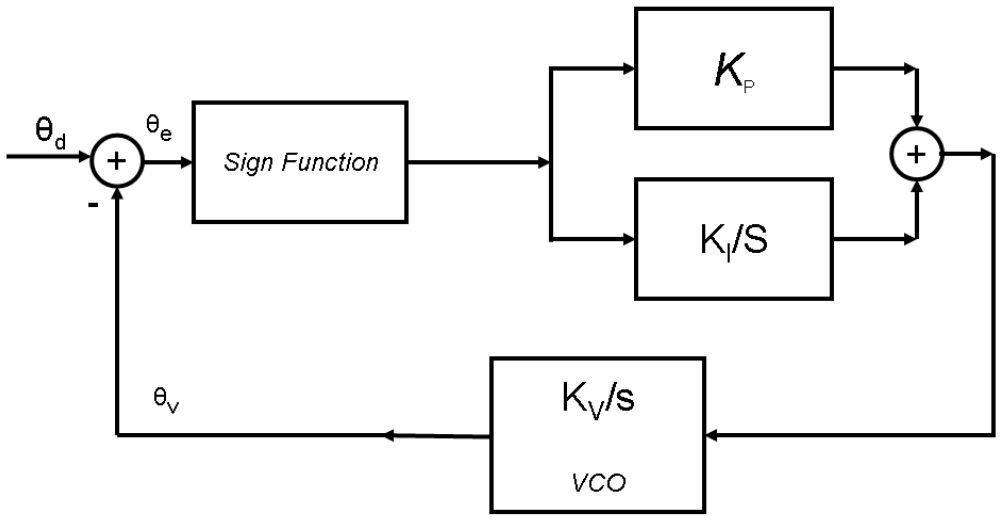

Figure 3-19: phase model for 2nd-order hybrid CDR.

The loop equation can be derived as

$$\theta_V(t_{n+1}) = \theta_V(t_n) + \theta_{bb}\left[\varepsilon_n + \frac{\varepsilon_n}{\xi} + \frac{2}{\xi}\sum_0^n \varepsilon_n\right] \tag{3-39}$$

$$\varepsilon_n = sign[\theta_d(t_n) - \theta_V(t_n)] \tag{3-40}$$

By adding second path to system, now the VCO frequency is a function of two paths: integral path and bang-bang (proportional) path. The second integral makes the system vulnerable to oscillate. Walker in [5] introduced a stability factor for the system as ξ.

$$\xi = \frac{\Delta\theta_{Bang-Bang}}{\Delta\theta_{Integral}} = \frac{K_P K_V V_\phi t_{update}}{K_I K_V V_\phi t^2_{update}/2} = \frac{2K_P}{K_I t_{updtae}} \tag{3-41}$$

If ξ is greater than 1, the proportional and integral path can be considered non-interacting as long as system is not in slew rate limiting. If ξ is less than 1, the proportional path does not stabilize the system and large low frequency oscillation may occur [7].

Reference

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[2] Razavi, B., "Design of Integrated Circuits for Optical Communications," McGraw Hill, 2003.

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Chapter 4

Power Reduction Strategies

4.1 Introduction

Advances in technology and the introduction of high-speed processors have increased the demand for fast, compact and commercial methods for transferring large amounts of data.

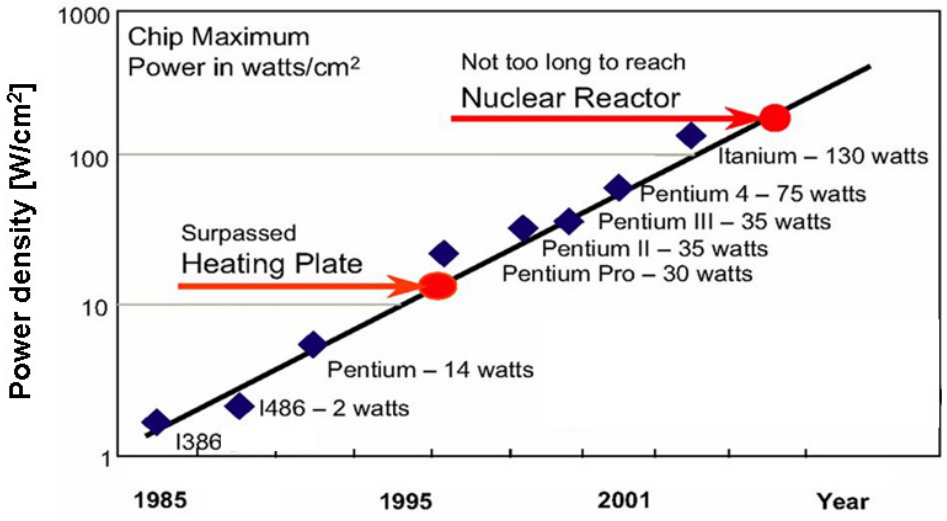

Figure 4-1: power vs. performance over years [1].

Meanwhile, the higher data rate dictates higher power consumption, while thermal and battery-life requirements are demanding lower power consumption.

Figure 4-1 shows the power density and performance over the years. The figure indicates power density (Max power per cm^2) grows exponentially. However, according to Figure 4-2, cooling cost is considerable as power is increasing. As described in Section 1.5, CDR is a power hungry device. In this chapter, the two proposed methods for power reduction in CDR are discussed.

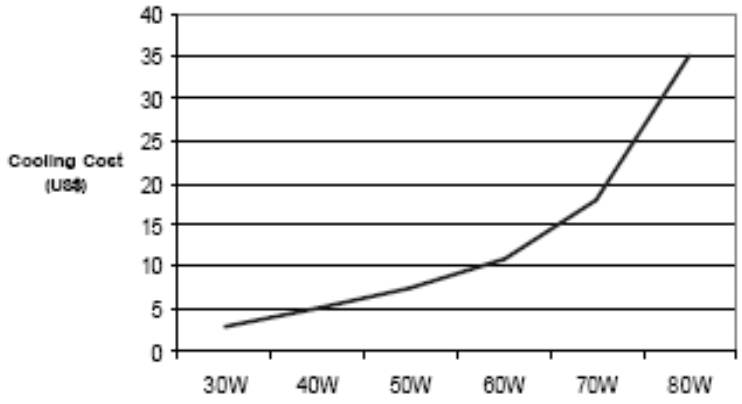

Figure 4-2: Cooling cost vs. power dissipation [2].

4.2 Static CMOS Logic vs. CML

Almost all high-speed CMOS CDRs are based on current-mode logic (CML) topology. When operating in the high-speed switching domain, the performance of conventional full swing CMOS degrades and causes the functional failure at high speeds.

Meanwhile, by migrating to the CML we need to dissipate huge amount of power to reach Gbps functional bit rates. Furthermore, CML inherently has smaller SNR compared to the conventional CMOS due to the small noise margin of CMLs. Advances in technology and CMOS scaling in recent years enables high-speed operation of conventional CMOS circuits. Employing standard CMOS circuit to construct a high-speed clock and data recovery circuit has some pros and cons.

Power consumption reduction can be achieved due to naturally low power consumption of standard CMOS circuits. However, standard CMOS circuit operates at full swing signal regime. Full swing operation in mixed-mode circuit results in a high substrate noise, which is not a problem in CML due to the constant current switching.

On the other hand, the input data needs to have high swing to be able to be detected by standard CMOS sampler.

To overcome these two dilemmas two strategies have been proposed:

1) Low input swing data standard CMOS sampler

2) Low substrate noise ring VCO

These two strategies are discussed in following and experimental results are presented in Chapter 5.

4.3 Low Input Swing Data Sampler

Static memories use positive feedback to create a bi-stable circuit, a circuit having two stable states that represent 0 and 1. The basic idea is shown in Figure 4-3, which shows two inverters connected in cascade along with a voltage-transfer characteristic typical of such a circuit, shown in Figure 4-4 [5].

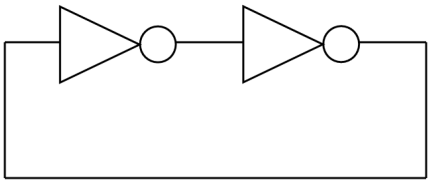

Figure 4-3: Basic bi-stable circuit.

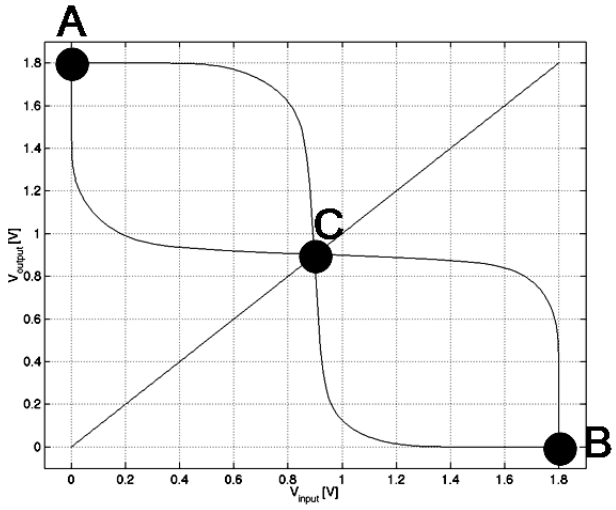

Figure 4-4: bi-stable circuit voltage transfer characteristic.

4.3.1 Normal D- Flip Flop

Normal master-slave D-flip flop (NDFF) can be implemented by two latches. Figure 4-5 shows the NDFF block diagram (For simplicity the single-ended block diagram is shown). SM1, SM2, SS1 and SS2 are the switches and Inv1 to Inv4 are the inverter cells.

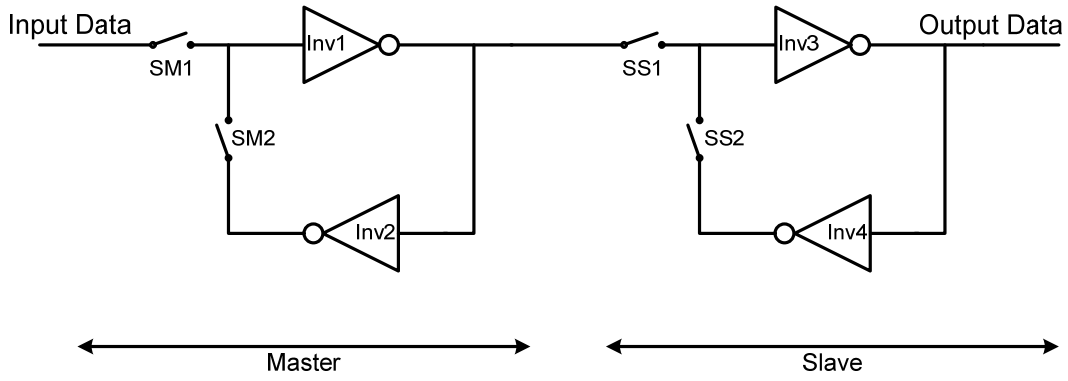

Figure 4-5: Block diagram of master slave D-Flip-Flop.

Figure 4-6 shows schematic diagram, all the switches are minimum size and for inverters $\frac{W_n}{L_n} = \frac{500n}{180n}$ and $\frac{W_p}{L_p} = \frac{830n}{180n}$. NDFF parameters vs. data input-swing are shown in Figure 4-7, where Min PW is the minimum pulse width. C2Q F and C2Q R stand for clock-to-Q (output) delay in falling and rising edge of output, respectively.

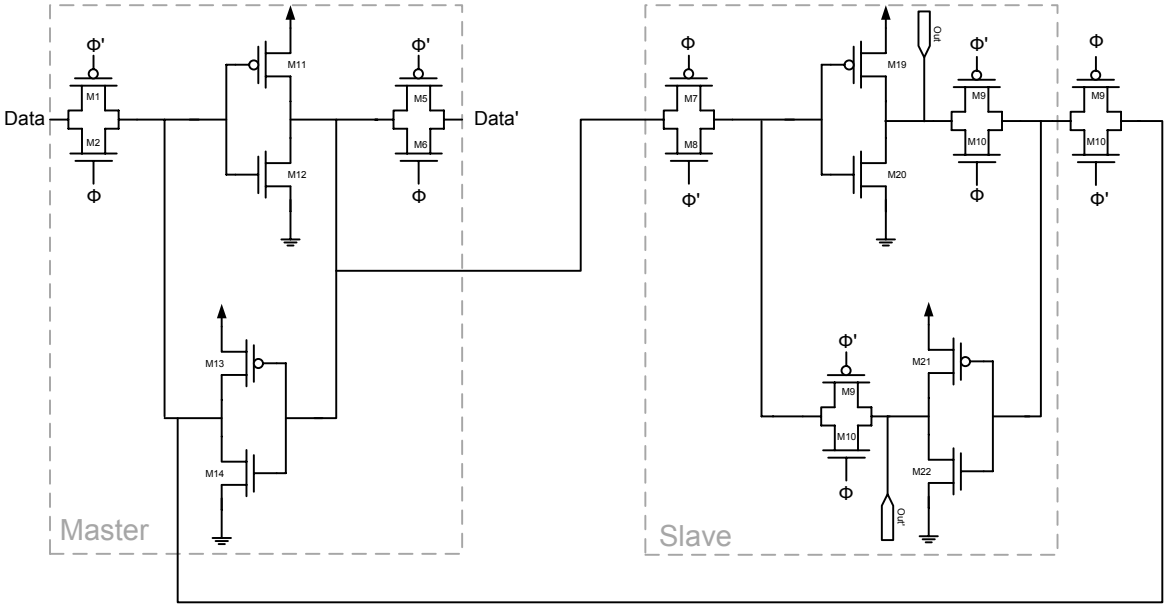

Figure 4-6: Schematic diagram of master-slave D-Flip-Flop.

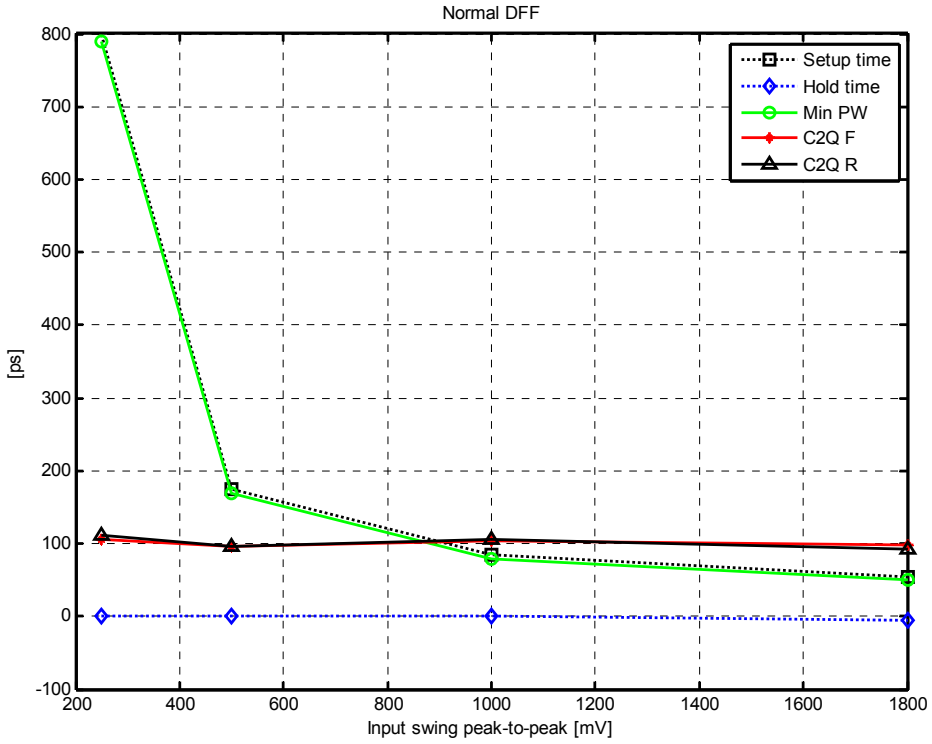

Figure 4-7: NDFF parameters vs. input data swing.

4.3.2 Switched D- Flip Flop

Figure 4-4 shows only three possible operation points (*A*, *B,* and *C)* for a latch cell. This circuit has only two stable points, and point *C* owing to gain of more than 1 is meta-stable operation point. Assume that latch is biased at point *C*. A small swing of input data can be detected by this latch. At the meta-stability point, *C*, input voltage and output voltage are equal. To bias and keep the latch at meta-stability operation, input and output can be connected together. Figure 4-8 shows the block diagram of proposed switched DFF (SDFF) (For simplicity the single-ended block diagram is shown).

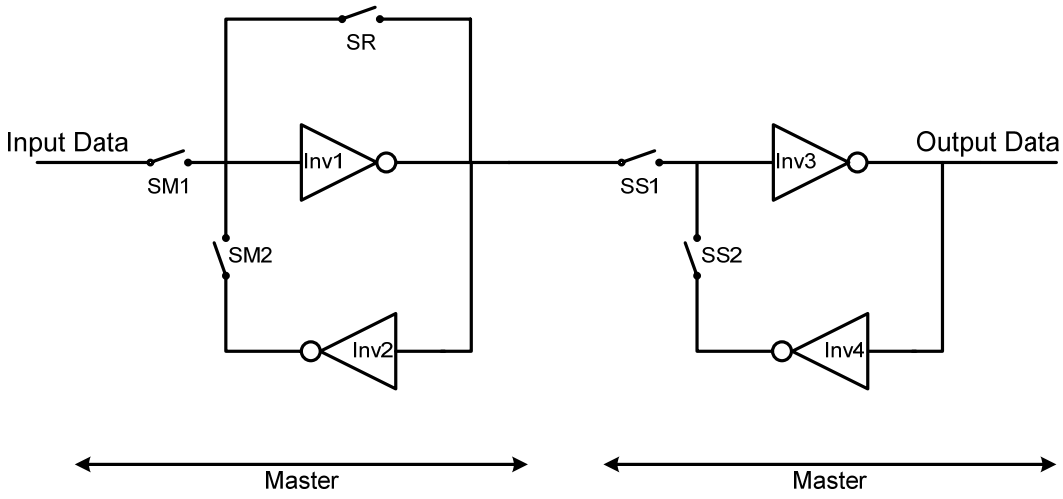

Figure 4-8: Single-ended SDFF block diagram.

As it is shown in Figure 4-9, before sampling the data by master latch, switch SR is closed for short period of the time (300 ps) and it makes master biased in meta-stability point. At

the time of sampling, switch SR will be open and master latch continues normal sampling procedure. Figure 4-10 shows the block diagram of a differential switched D-flip flop.

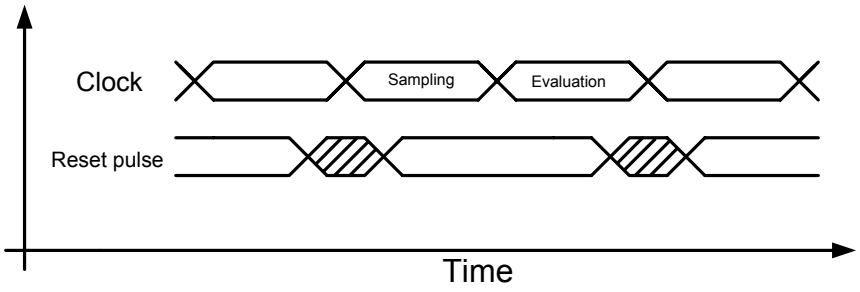

Figure 4-9: Reset pulse timing wave form in the respect to clock

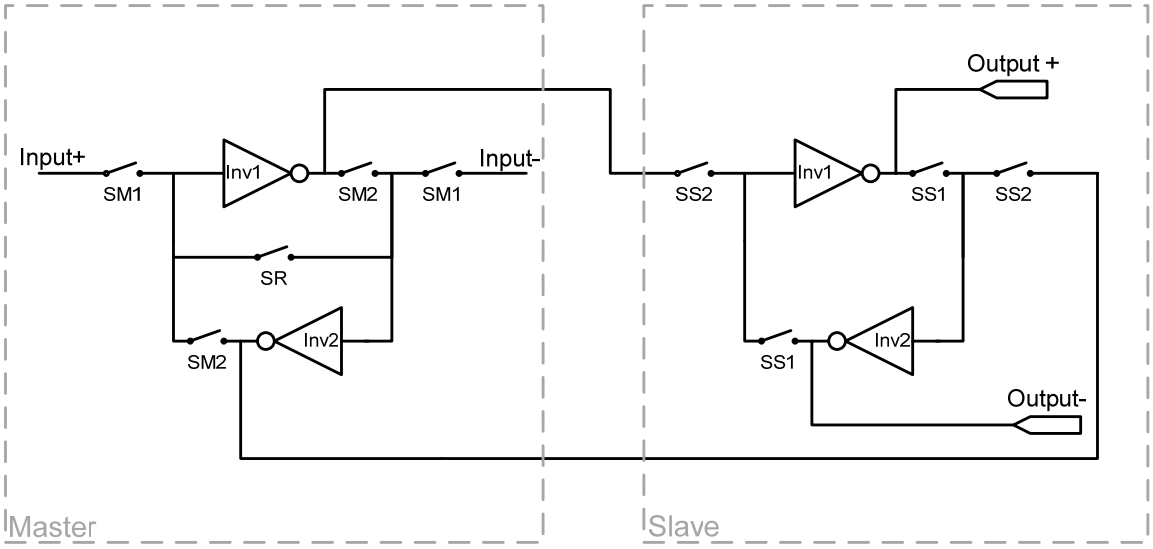

Figure 4-10: Differential SDFF block diagram.

Schematic diagram of differential-ended SDFF is shown in Figure 4-11. Transistor sizing is the same as in NDFF. Figure 4-12 shows SDFF parameters vs. data input-swing.

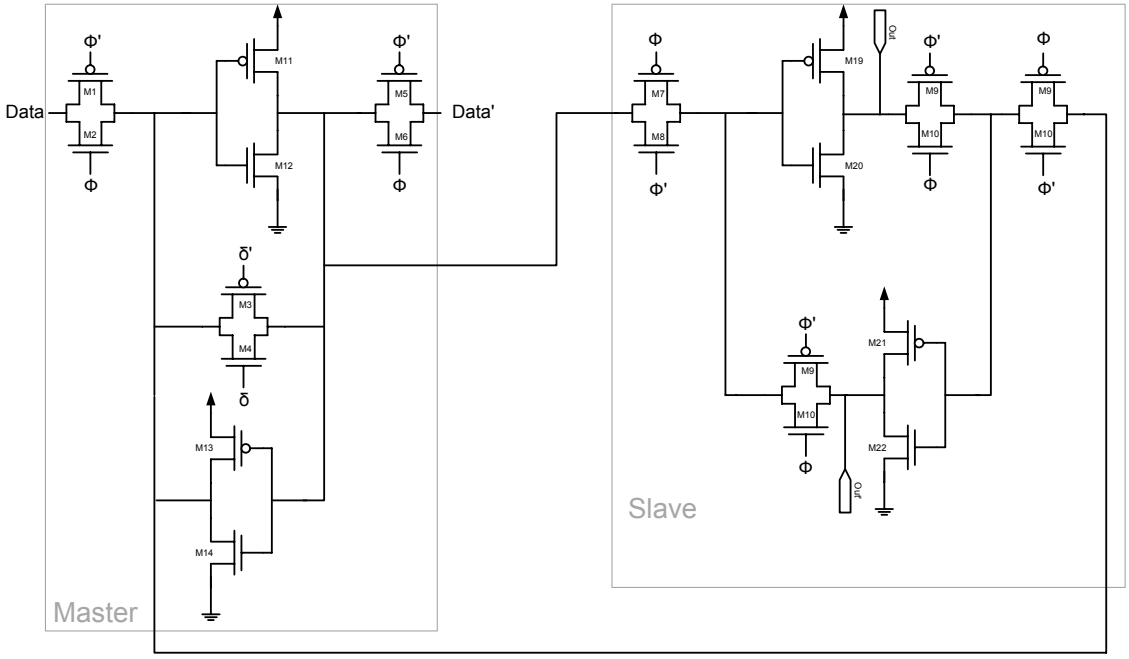

Figure 4-11: Schematic diagram of master-slave SDFF.

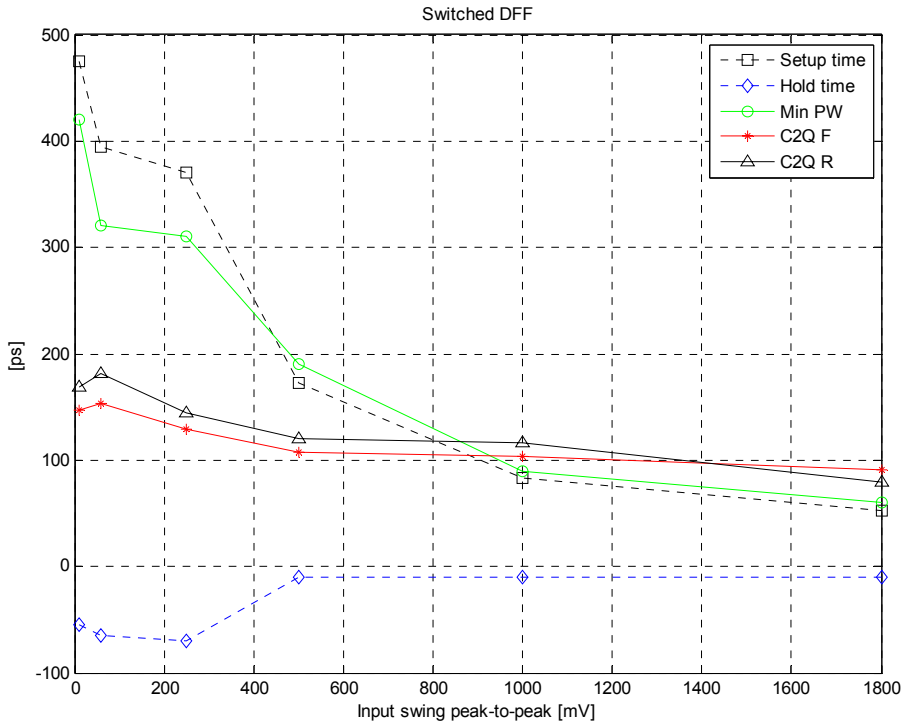

Figure 4-12: SDFF parameters vs. input data swing.

4.3.3 Switched-Buffered D-Flip Flop

To decrease the capacitance of the switches and improve the performance of the SDFF in low swing operation, we can insert a buffer between the master and the slave. These buffers can boost up the speed of the DFF in low swing operation. However, in high swing due to the delay of the inverters, performance will degrade. Figure 4-13 shows the block diagram of Switched-Buffered D-flip flop (SBDFF). SBDFF parameters are shown in Figure 4-14 in different input swing levels.

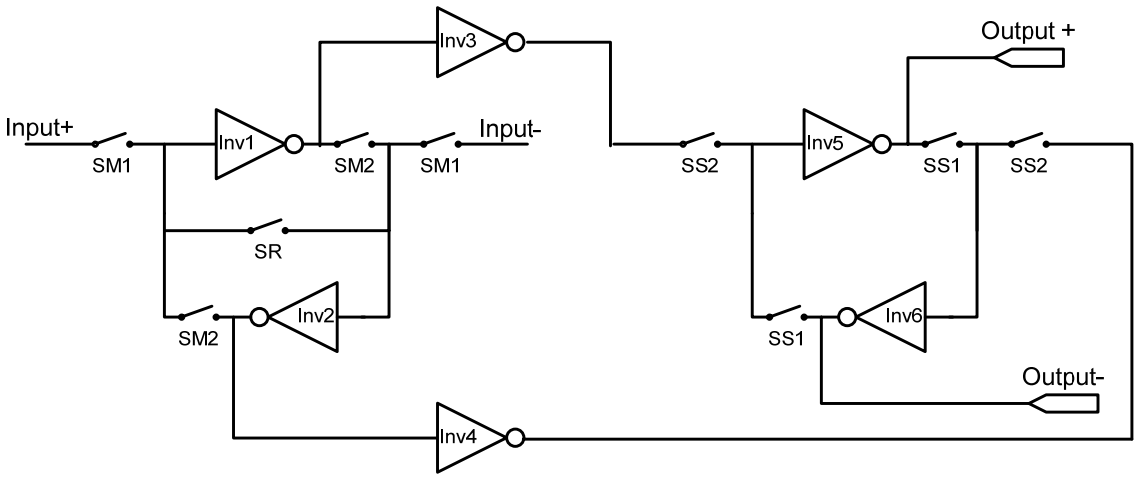

Figure 4-13: SBDFF block diagram.

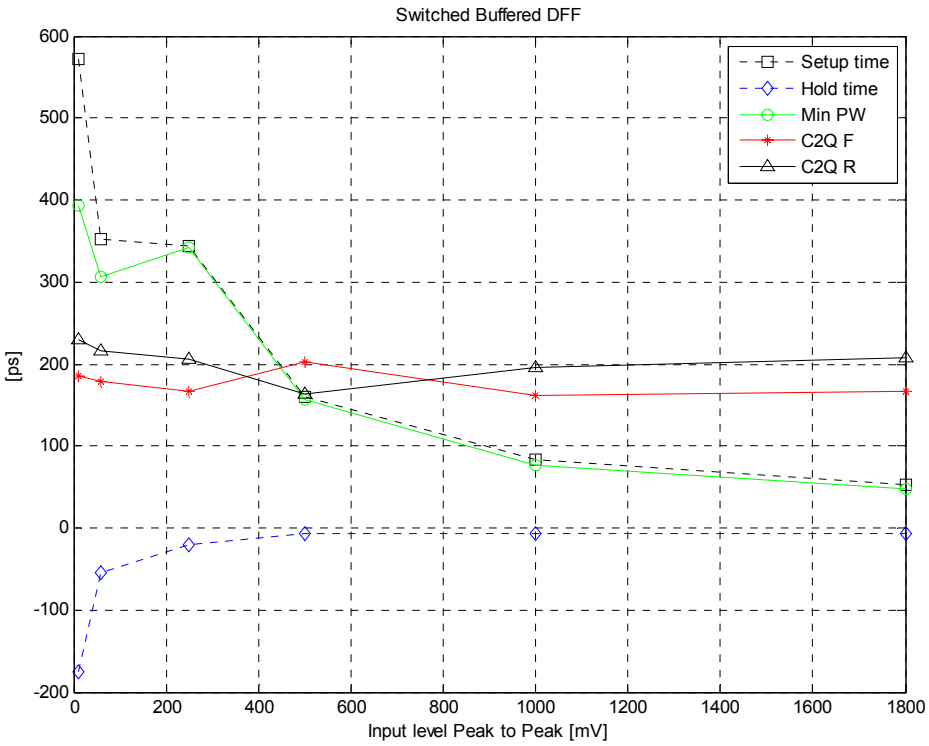

Figure 4-14: SBDFF Parameter vs. Input Swing.

4.3.4 Comparison

Based on the simulation result, the minimum data swing for NDFF is around 150mVp. However, the SDFF is able to operate with only 15mVp swing. The speed of operation of the NDFF is almost the same as the SDFF with a high swing, but due to switching between the meta-stability point and one of the stable points in each period SDFF dissipates more power. In the situation when the data swing is 150mVp and the clock operates at 1 GHz, the NDFF dissipates 221μW and the SDFF dissipates 321μW. The comparison between the delay (Setup time + Clock to output) of these DFFs vs. input swing is shown in Figure 4-15.

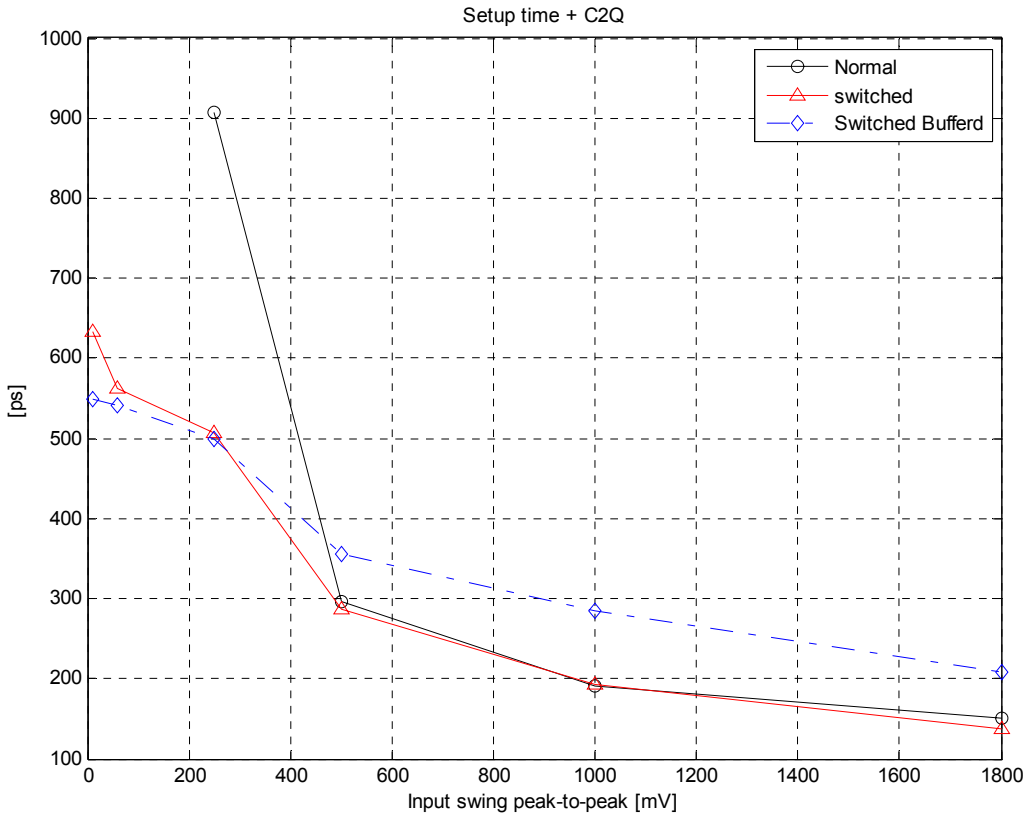

Figure 4-15: Delay comparison.

4.4 Low substrate noise VCO

4.4.1 Substrate Noise

Any switching node can couple noise into the substrate. The finite resistivity of the substrate allows that noise to be transmitted to the neighboring blocks. For instance in a transistor, the drain voltage changes, it induces some currents into the substrate, as is illustrated in Figure 4-16. These spurious currents injected into the substrate travel through the bulk reaching various depths and are collected by low-resistivity pick-ups.

These current paths are determined according to the relative position of the noise injector, substrate doping and location of other contacts.

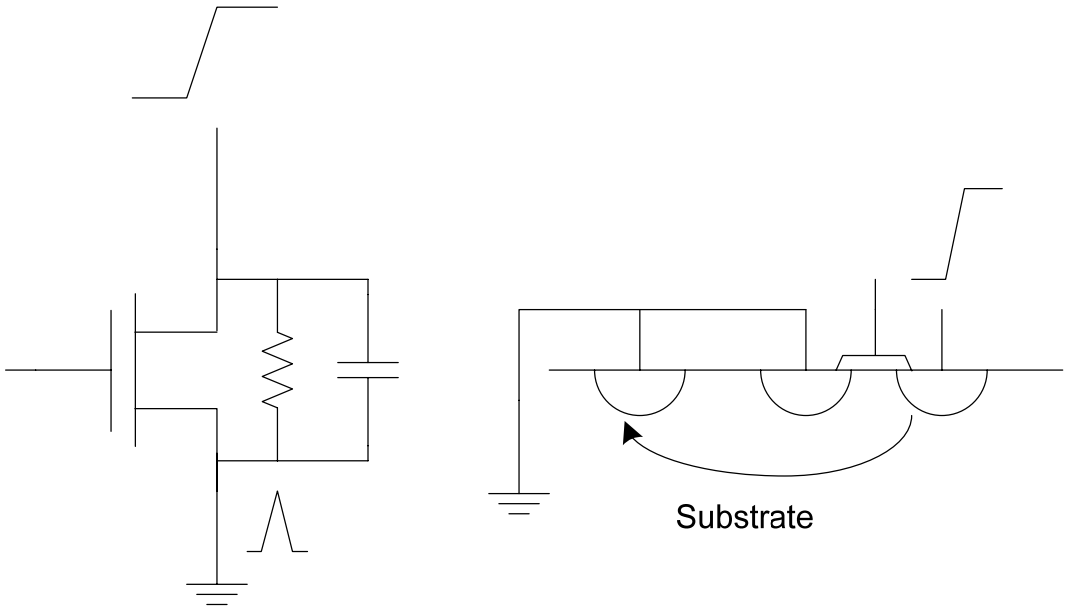

Figure 4-16: Substrate noise propagation.

In mixed-signal circuits, complex and noisy digital circuits are integrated on the same substrate with sensitive analog circuits. In these circuits, the digital part switches fast and induces noise currents to the substrate which are picked up by analog parts and change the operation and functionality of these parts (Figure 4-17). For example, suppose that we have a DSP block which is switching very fast in the vicinity of a broadband receiver. We can observe that there are some unwanted frequency components with considerable magnitude in the receiver spectrum due to substrate noise degrading the performance. Now the challenge in mixed signal design is to reduce the effect of substrate noise on analog blocks.

Substrate coupling in mixed-signal IC's has been identified as a major problem due to the technology trend to integrate as many circuits as possible on the same die, or in other words, system-on-chip (SOC) approach.

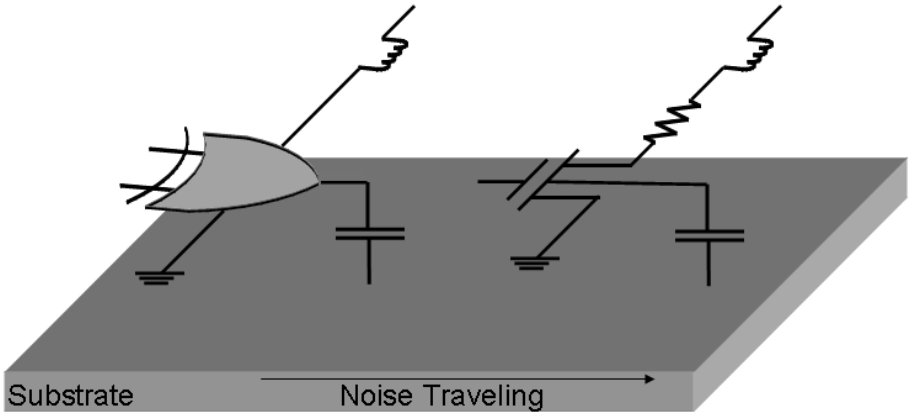

Figure 4-17: Substrate noise in mixed-signal circuits.

4.4.2 Substrate Noise in VCO

High-speed digital circuits such as microprocessors and memories use a phase locking system at the board-chip interface to keep in check timing skews between the on-chip clock and the system clock. Fabricated phase-locked loops (PLL) sharing the same substrate as the digital circuits have been affected by substrate noise [3].

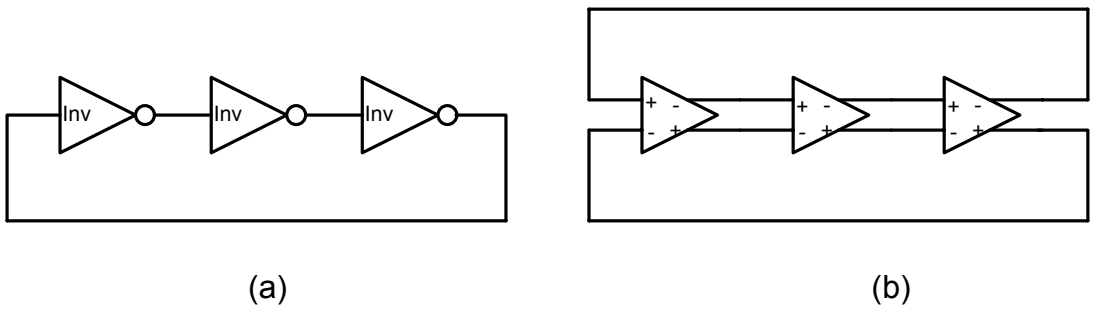

Figure 4-18: (a) Single-Ended ring oscillator, (b) Differential ring oscillator.

The substrate noise manifests itself as jitter at the output of the PLL, primarily through various mechanisms in the voltage-controlled oscillator. The author in [4] investigated the noise sensitivity of single-ended ring oscillators and differential ring oscillators (Figure 4-18) in [4]. Figure 4-19 shows cycle jitter and cycle-to-cycle jitter of (a) the single-ended ring oscillator and (b) the differential ring oscillator. The figures show that the single-ended ring oscillator has higher jitter in comparison with the differential ring oscillator.

Also, shown in Figure 4-20 is the jitter of three-stage and six-stage oscillators designed for a frequency of 500MHz with similar tail current and voltage swings. We observe that the minimum values of cycle jitter and cycle-to-cycle jitter are smaller in a three-stage topology. This is because for the three-stage oscillator, the reduction of the oscillation frequency to the desired value is obtained by means of the fixed load capacitance rather than by the voltage-dependent capacitances of the transistors. Hence, a smaller fraction of the total load capacitance is subject to variations with substrate noise [4].

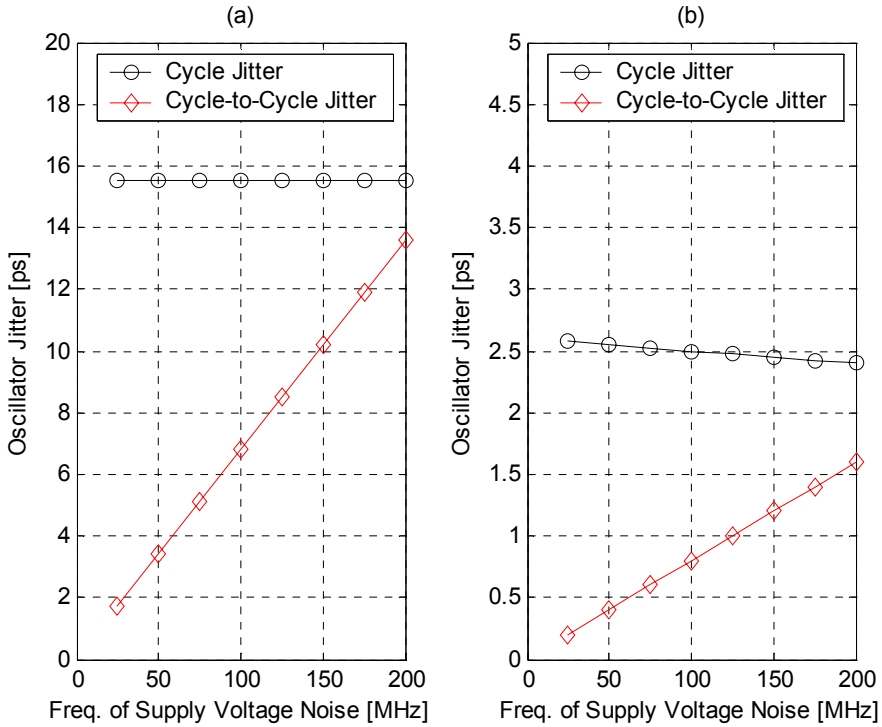

Figure 4-19: Cycle jitter and cycle-to-cycle jitter of (a) the single-ended ring oscillator and (b) the differential ring oscillator [4].

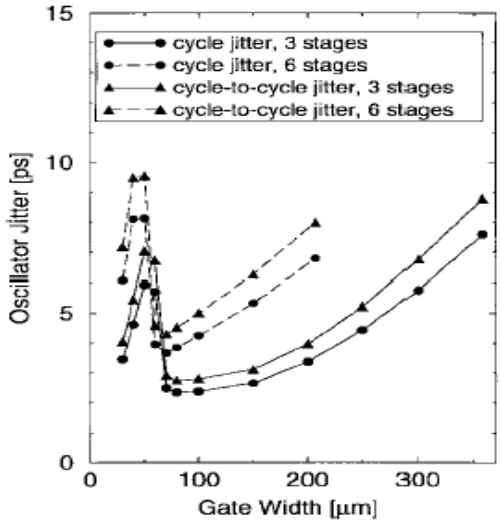

Figure 4-20: Jitter of the three-stage and the six-stage of the differential ring oscillator [5].

4.4.3 Low Substrate Noise Ring Oscillator

As mentioned in section 4.4.2, a differential ring oscillator has better phase noise compared to a single-ended ring oscillator due to better common-mode rejection ratio; and constant switching current. On the other hand, single-ended ring oscillator has better power consumption compared to the differential one.

The conventional single-ended ring oscillator consists of odd number of delay cells in a row (Figure 4-21). Each delay cell has separate voltage-controlled current source (VCCS). Consequently, different amount of current results in different delay, which results in frequency variation over the different control voltages.

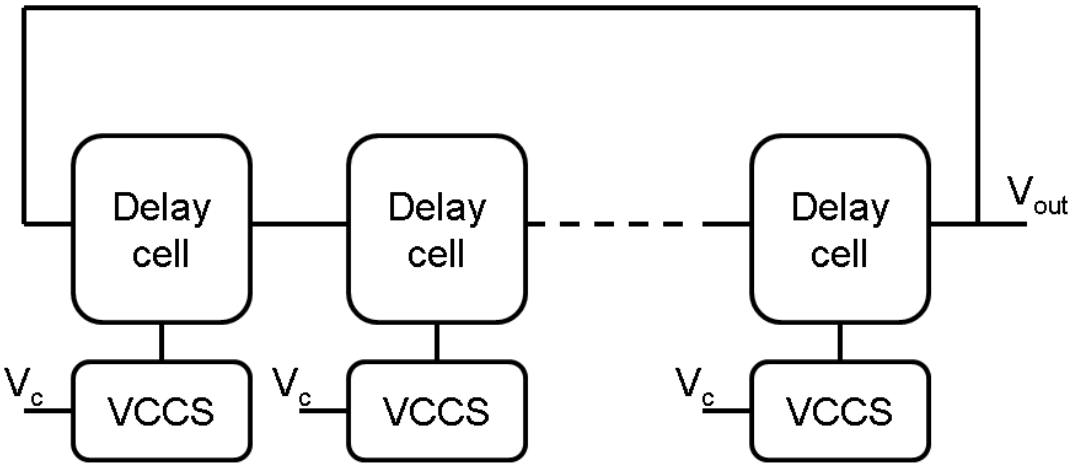

Figure 4-21: Conventional single ended ring VCO.

A close look at conventional single-ended ring VCO architecture reveals that each cell has separate current source and the current source will be switching on and off with the

frequency of the VCO. This switching activity is the major source of substrate noise for VCO. As delay cell is a part of VCO, none of physical level blocking techniques [6] can be used to mitigate the substrate noise.

Using one current source shared between delay cells has been proposed to reduce the effect of the switching on delay cells (VCO). Figure 4-22 shows the architecture for the novel low substrate noise single ended VCO.

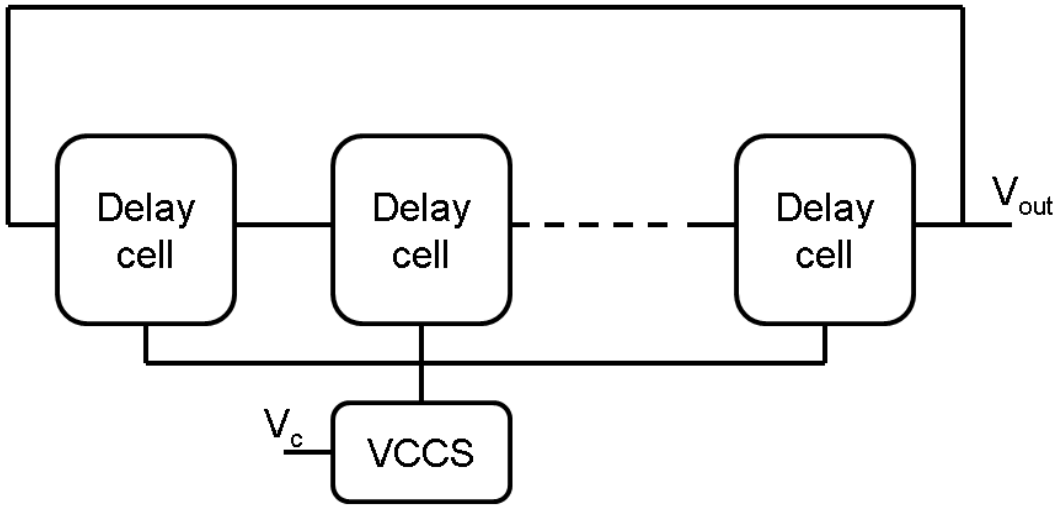

Figure 4-22: Architecture for proposed VCO.

The new VCO has only one shared VCCS. The VCCS is always ON and it is not switching in this architecture as each delay cell needs power (current source) only during switching time. Figure 4-23-(a) shows the voltage wave form (one transition) at the output of a inverter chain with three inverters. Figure 4-23-(b) shows the short circuit current for each inverter which results in substrate noise. As shown in Figure 4-23-(b) each inverter (delay

Cell) dissipates current at different timing. The proposed low substrate noise circuit shares one current source for all delay cells and provides constant current during operation of the VCO. At Figure 4-23-(c) wave form (1), depicts the over lap waveforms and summation of the current is shown in wave form (2). Current source sharing technique results in constant current discharging to ground through the VCCS and reduction in substrate noise.

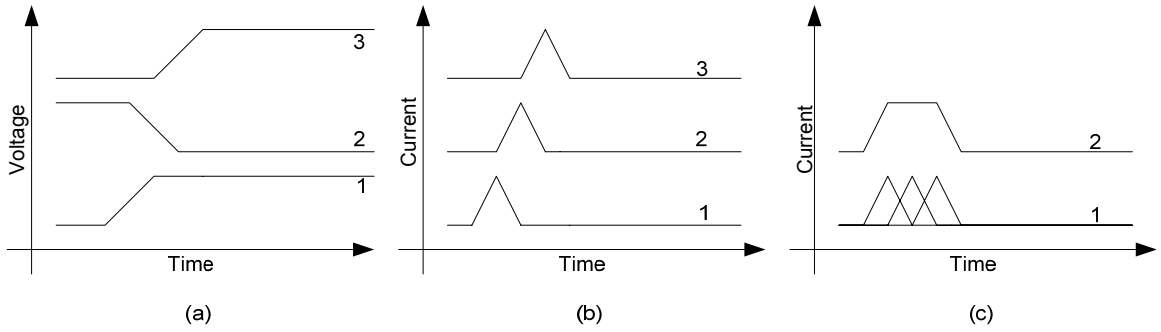

Figure 4-23: Voltage and Current waveforms for a single ended VCO

Measuring substrate noise is not a trivial task. Our approach to monitor the substrate noise is to measure the ground voltage variation and jitter at the output of the oscillator. As discussed in section 4.2, substrate noise manifests itself as jitter at the output of VCO.

Figure 4-24 and Figure 4-25 show the schematic for conventional and proposed single ended ring oscillator, respectively.

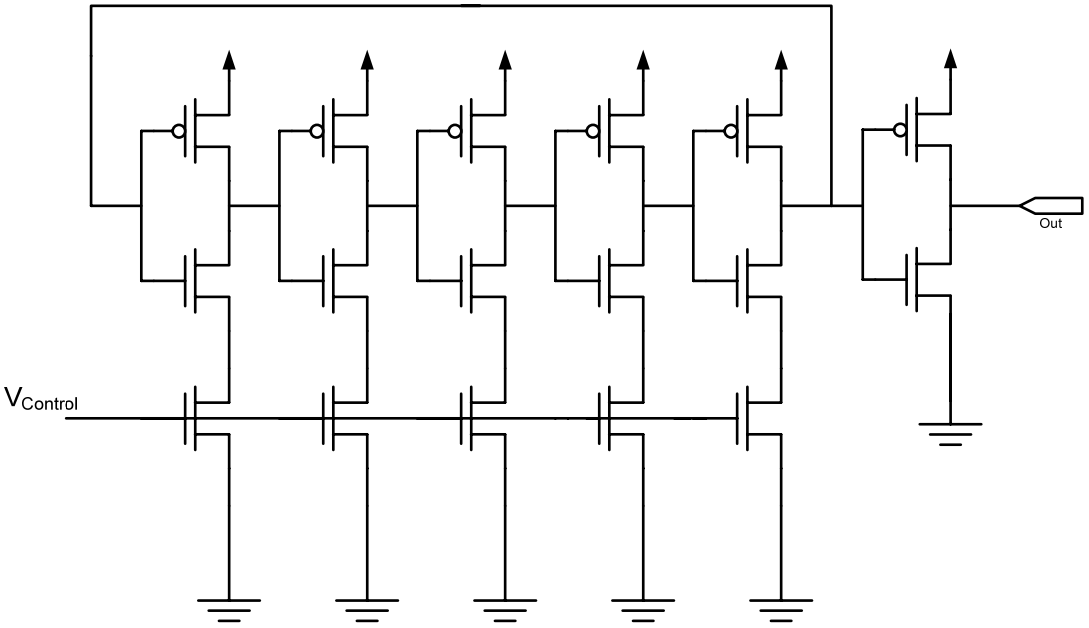

Figure 4-24: Schematic for conventional ring VCO.

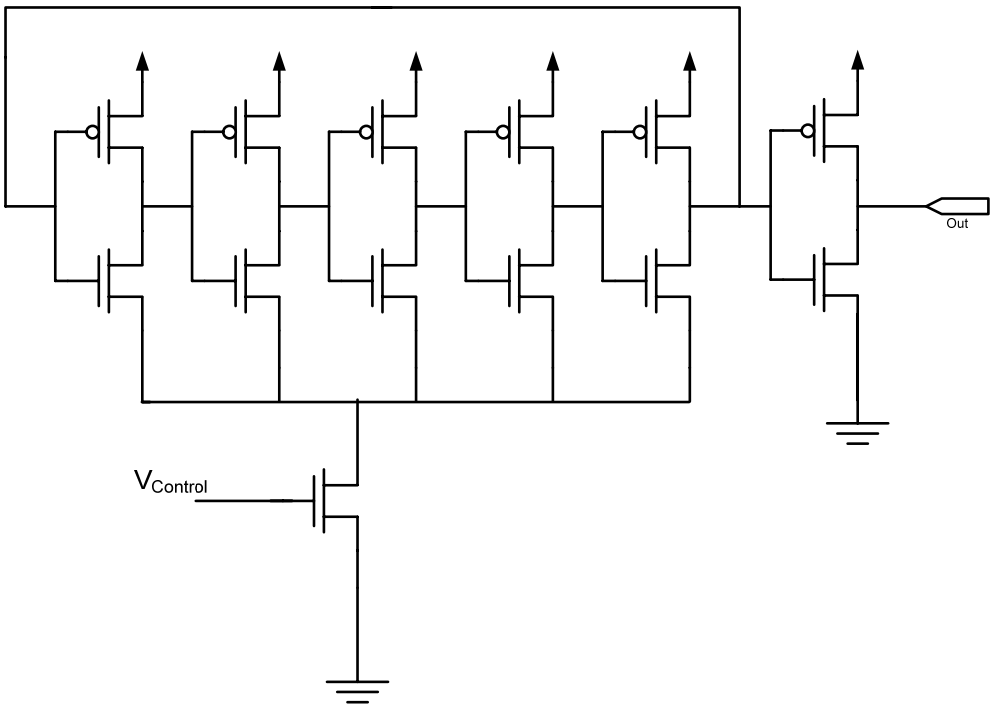

Figure 4-25: The schematic of proposed ring VCO.

To have right simulation condition, the test bench includes the bond wire model to observe the effect of switching current on power/ ground voltage variation. The test bench has been shown in Figure 4-26. Simulation results shows 50% reduction on ground variation and peak-to-peak jitter in 5GHz frequency of operation (Figure 4-27).

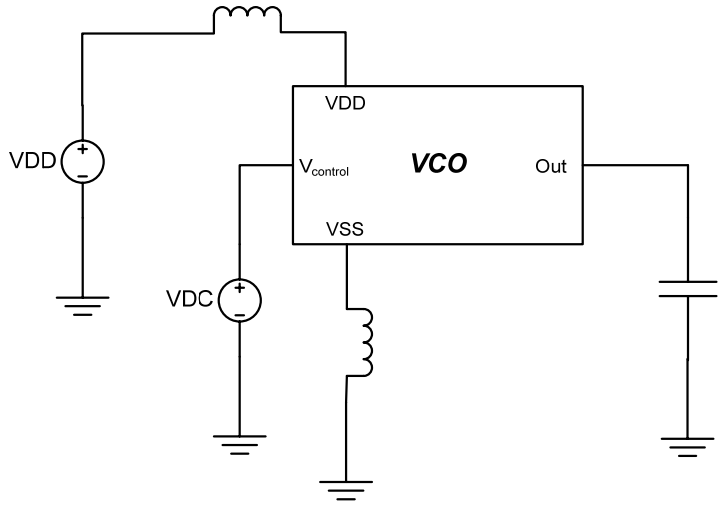

Figure 4-26: Test bench schematic.

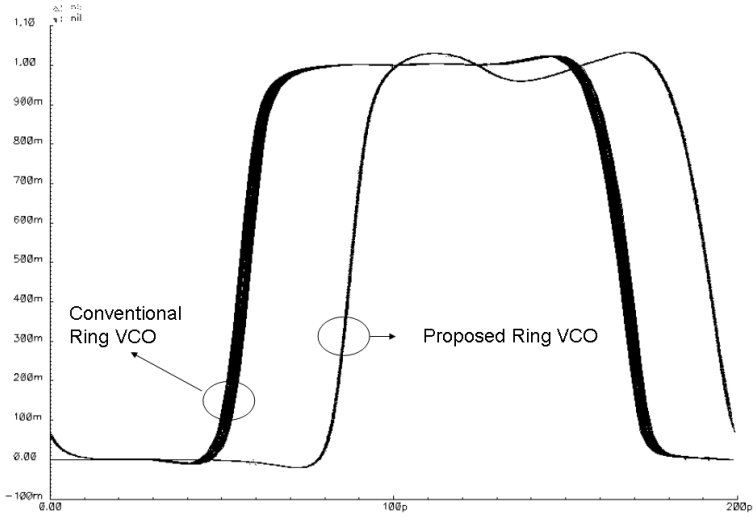

Figure 4-27: Eye-diagrams for conventional and proposed VCOs.

Reference

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Chapter 5
Low Power CDR

5.1 Introduction

In Chapter 2, different CDR architectures were discussed and different types of phase detector were explained. Various analog and hybrid CDR systems were examined along with their system level simulation in Chapter 3. Furthermore, loop dynamics and their associated parameters were analyzed. In Chapter 4, two techniques have been proposed to realize the low power, high speed CDR circuit. In this chapter, the circuit design, simulation and physical implementation of two CDR chips are presented. A 2 Gbps CDR in 0.18μm CMOS technology process and a 5 Gbps CDR in 90nm CMOS technology process are implemented. This chapter concludes with measurement results.

5.2 The 2 Gbps Low-Power CDR Implementation

The CDR block diagram of a PLL-based CDR is shown in Figure 5-1. The CDR is designed in a 0.18μm CMOS technology process, using single 1.8V supply voltage.

The following section explains the design of each block.

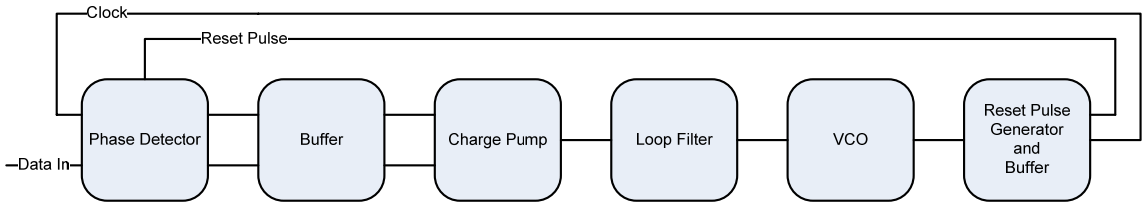

Figure 5-1: Block diagram for the PLL based CDR.

5.2.1 Phase Detector

The Alexander phase detector architecture has been selected to design the phase detector. Shown in Figure 5-2, the Alexander phase detector consists of four D-Flip-Flops and two XORs. Since the input data is low swing, sampling the data with the conventional static DFF is not feasible. Thus, SDFFs are used to sample the low swing input data (as explained in Chapter 4). Since the output of the SDFF is full-swing, the conventional DFF can be used to resample the data (The second set of flip-flops). Figure 5-3 shows the schematic for switched DFF. Device sizes are listed in Table 5-1. The SDFF is a master-slave DFF and consists of two latches. The layout is shown in Figure 5-4.

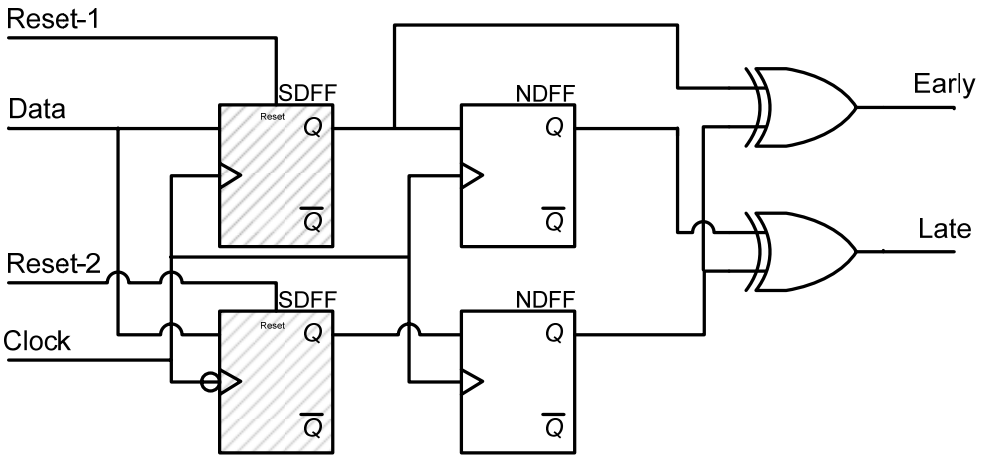

Figure 5-2: Alexander phase detector.

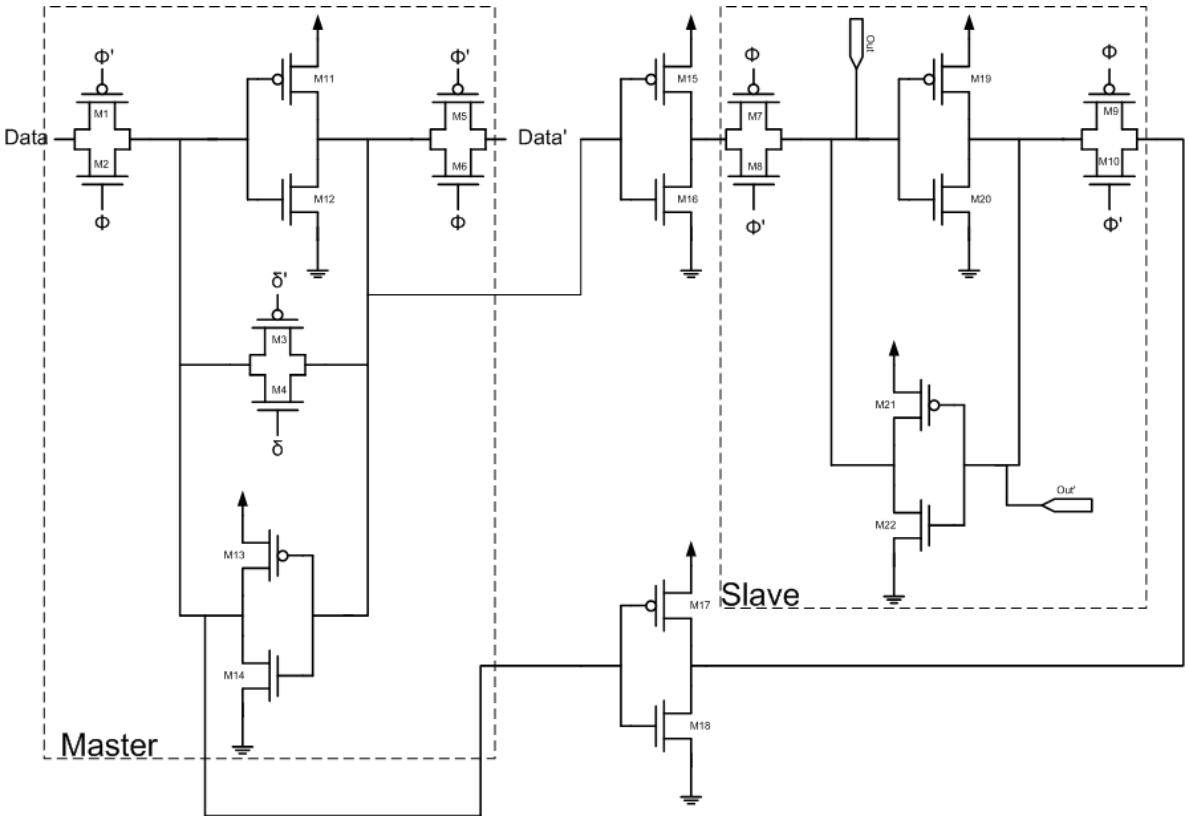

Figure 5-3: SDFF Schematic.

Table 5-1: Transistor sizing for SDFF

M1, M2, M4, M5, M6, M7, M8, M9, M10	5µm/0.180µm
M3, M4	3µm/0.180µm
M11, M13, M15, M17	3.3µm/0.180µm
M12, M14, M16,M18	1µm/0.180µm
M19, M21	0.850µm/0.180µm
M20, M22	0.500µm/0.180µm

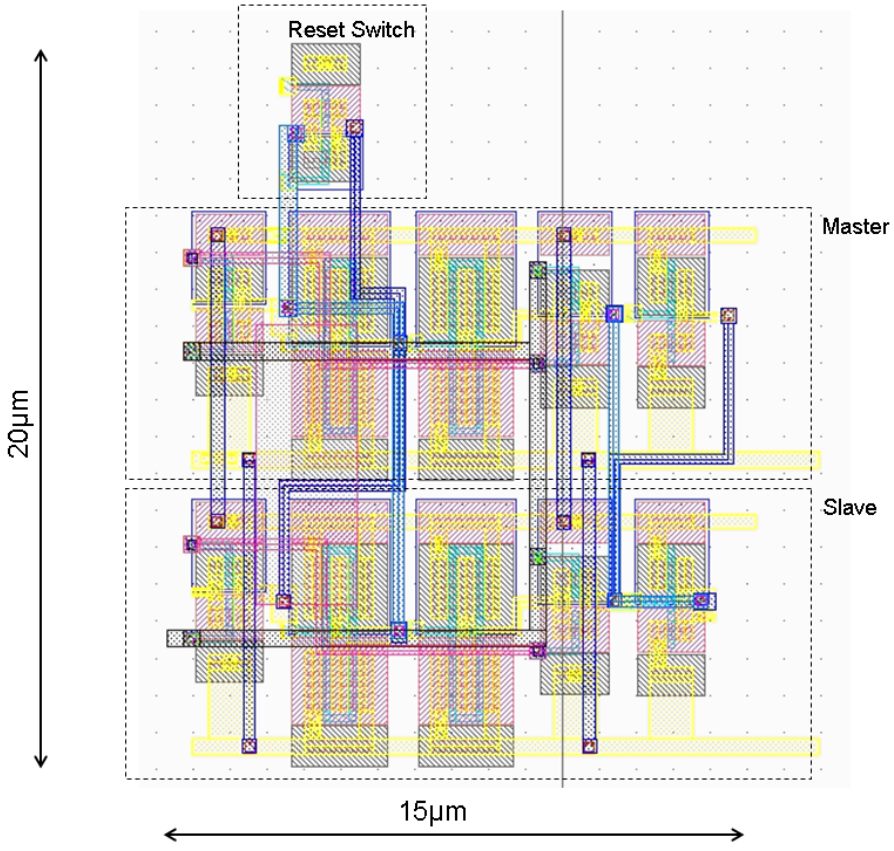

Figure 5-4: SDFF Layout.

The XOR schematic is shown in Figure 5-5. Figure 5-6 shows the simulation results. The XOR generates complementary outputs which can be used by differential charge pump.

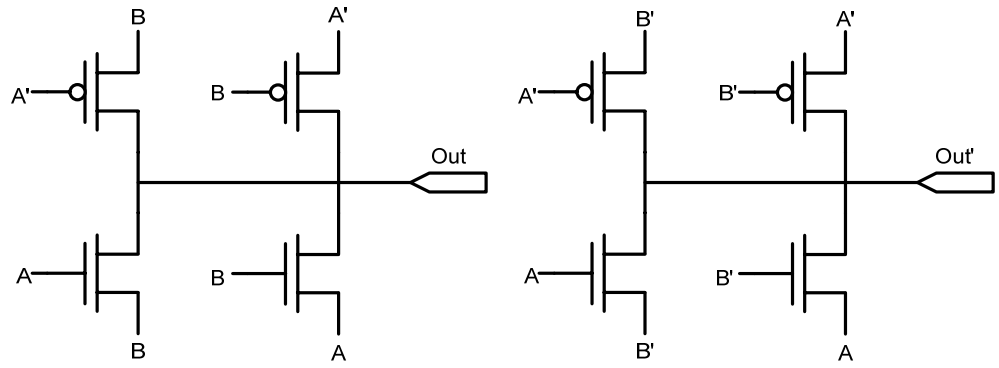

Figure 5-5: Schematic for XOR.

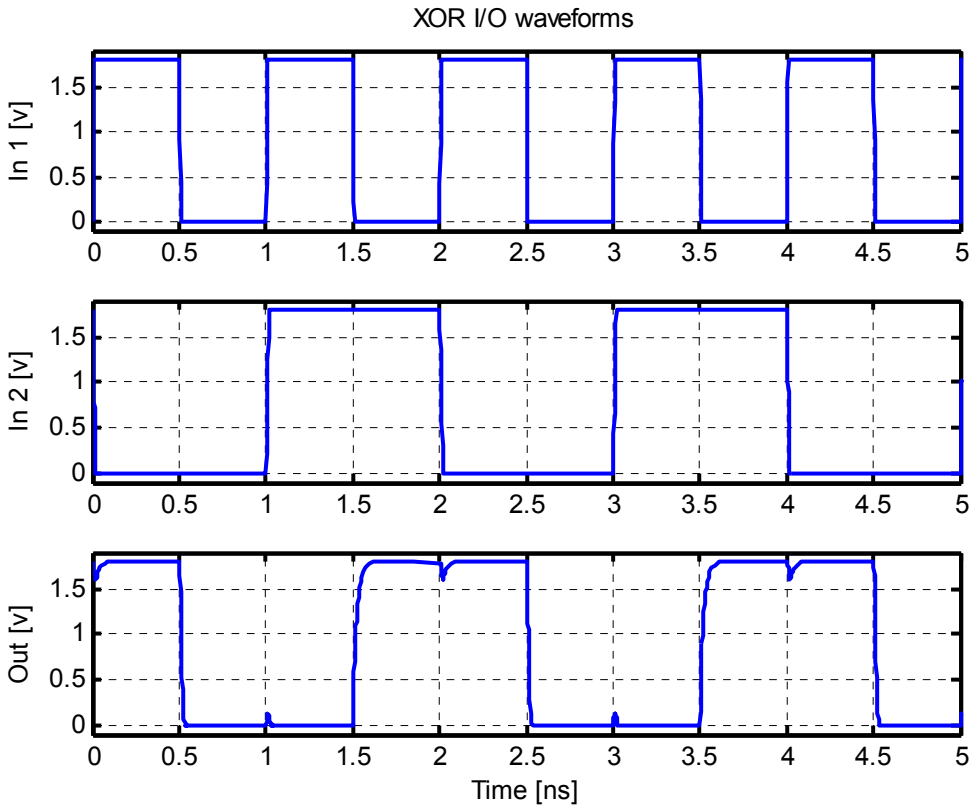

Figure 5-6: Inputs and output wave forms of the XOR block.

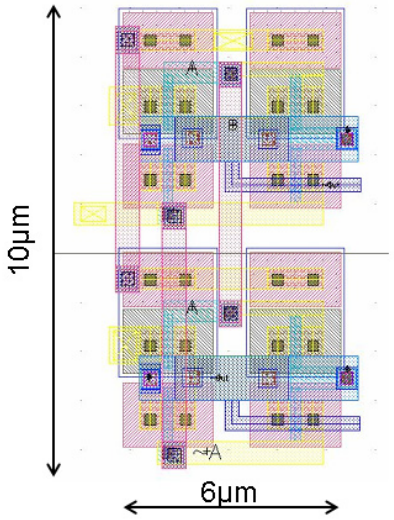

Figure 5-7: XOR layout.

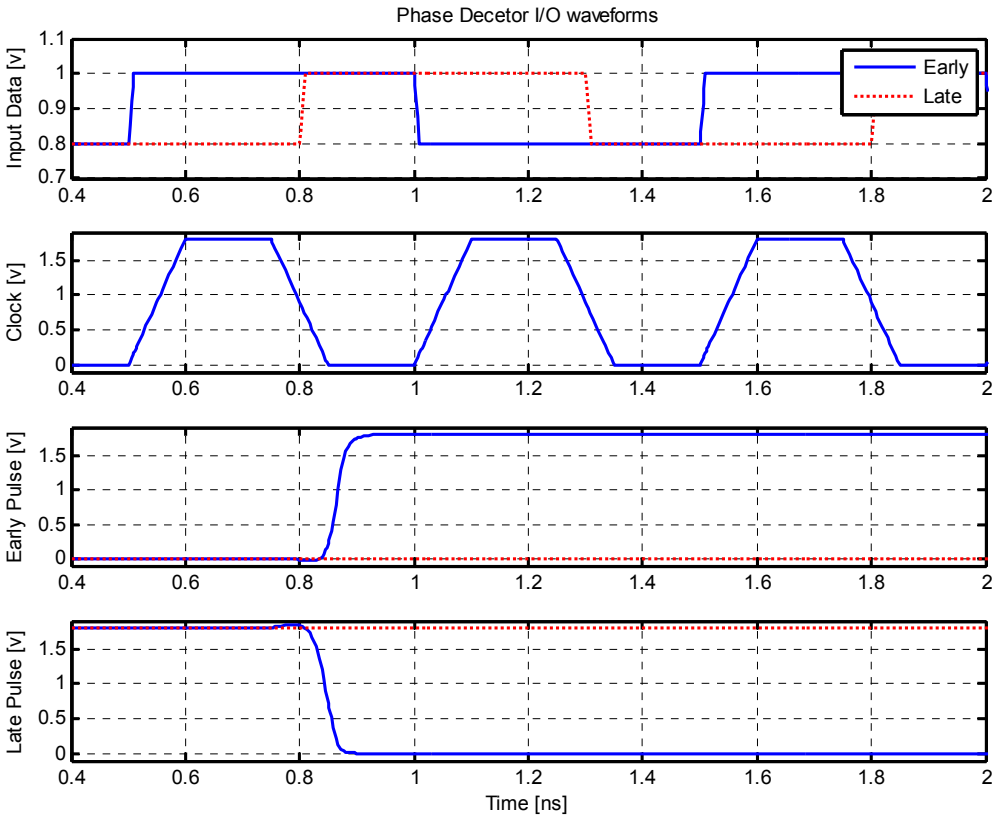

Figure 5-8: Phase Detector input/output wave forms.

The layout for the XOR block is depicted in Figure 5-7. The phase detector output signals (Figure 5-8) show the functionality of the phase detector based on the early or late clock input. The phase detector characteristic graph is illustrated in Figure 5-9.

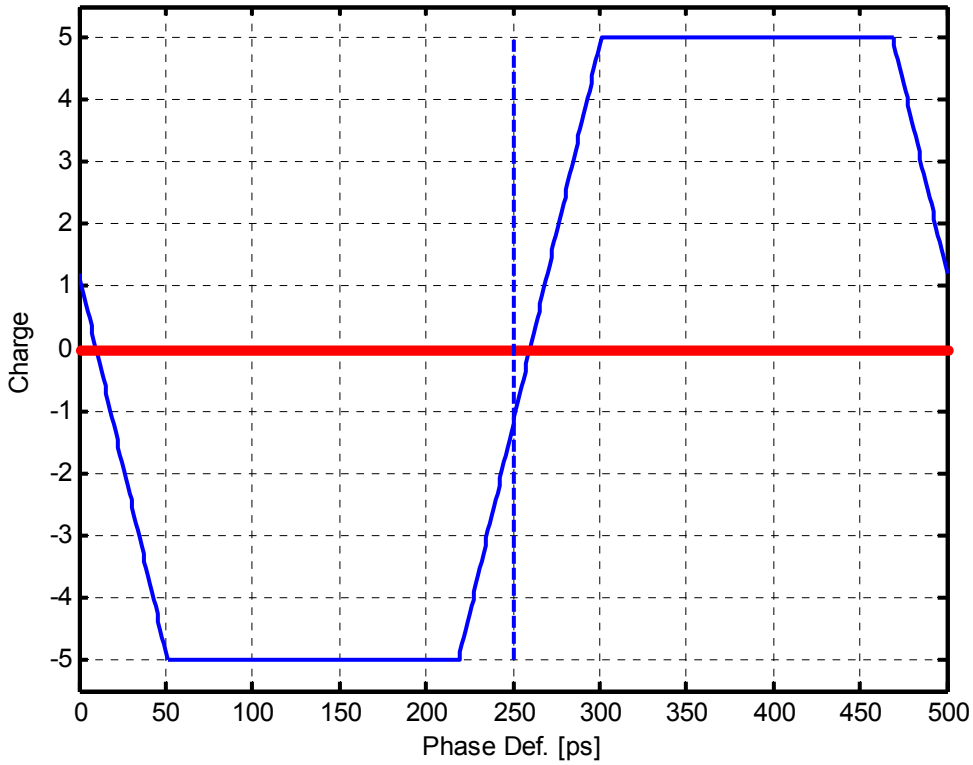

Figure 5-9: Phase Detector characteristic graph.

5.2.2 Charge Pump

A charge pump is needed to convert the early/late pulses to appropriate current signals. The current signals are passed to the loop filter and generate the VCO control voltage (Chapter 3). Figure 5-10 shows the schematic of the charge pump.

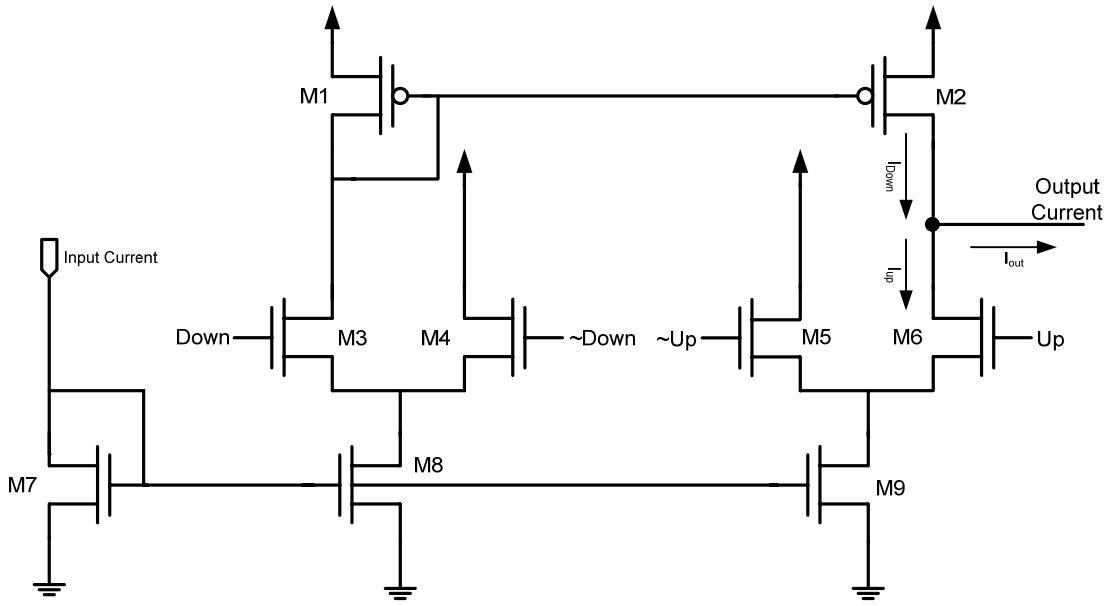

Figure 5-10: Schematic of the charge pump.

Transistor M7 takes the input current from an off-chip supply. The input current gets mirrored at M8 and M9. The output current is given by

$$I_{out} = I_{Down} - I_{Up} \tag{5-1}$$

where

$$I_{Down} = k(V_{Down} - V_{\sim Down}) \tag{5-2}$$

$$I_{Up} = k(V_{Up} - V_{\sim Up}) \tag{5-3}$$

The constant k, in both equations (5-2 and 5-3) could be assumed equal (disregarding parasitic and mismatches). Therefore:

$$I_{out} = k\,[(V_{Down} - V_{Up}) - (V_{\sim Down} - V_{\sim Up})] \quad (5\text{-}4)$$

It should be noticed that the digital output signals from the phase detector are pseudo-complementary and the common noise is not canceled out by phase detector. The layout for the charge pump block is depicted in Figure 5-11.

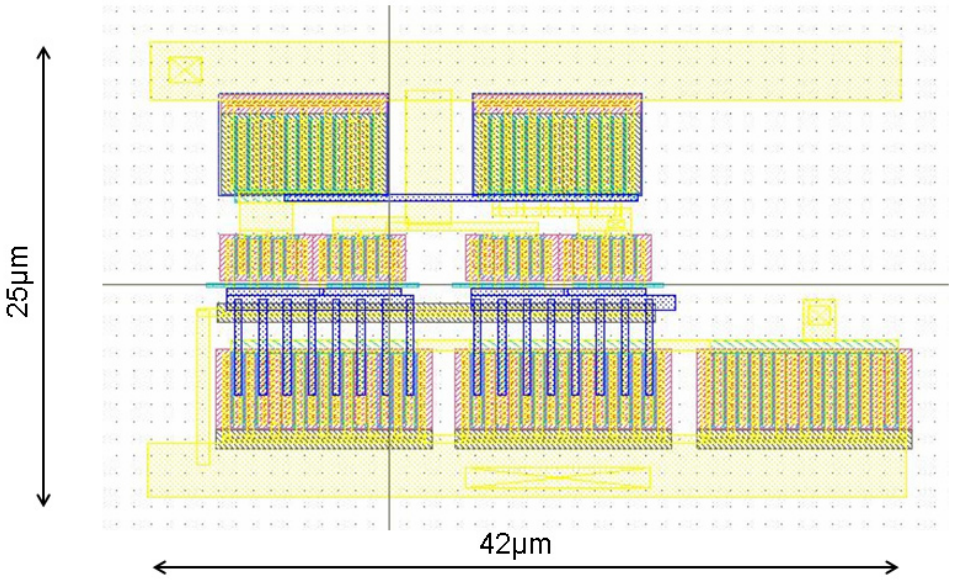

Figure 5-11: The layout for charge-pump block.

5.2.3 Voltage Controlled Oscillator

The VCO takes the filtered controlled voltage from the charge-pump and loop filter and creates the square wave signal. The frequency of the output is proportion to the input control voltage. The schematic of a single-ended low substrate noise VCO (Section 4.4) is shown in Figure 5-12.

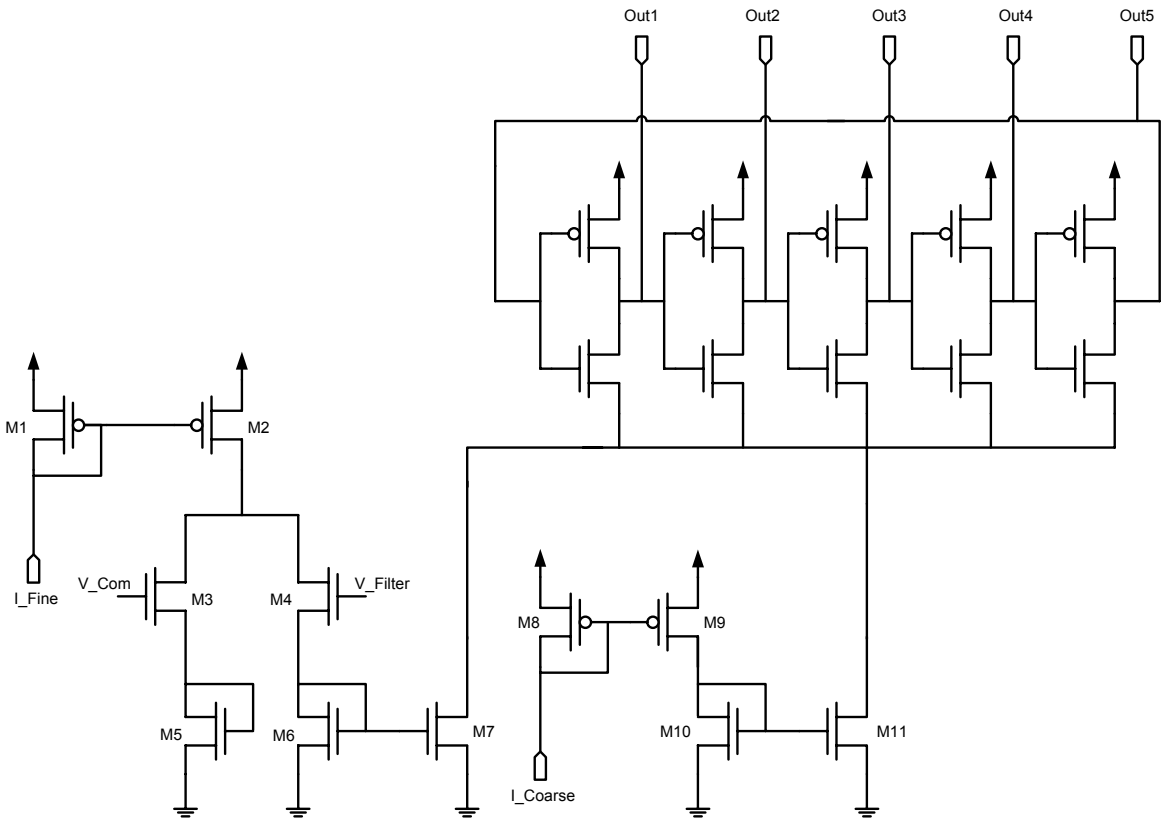

Figure 5-12: Schematic of the VCO.

The ring oscillator has two separate current bias paths. Transistors M8 to M11 are current supplier for the ring oscillator. I_Coarse gets buffered and amplified then provides a fixed amount of current for biasing the ring. The bias is constant and used to set and tune the free running frequency of the VCO. Providing the I_Coarse from the external off-chip source makes center frequency of the VCO tunable and independent of process variations. The second path is fine tune path, consist of M1-M7. This path controls the frequency of the VCO. Depending on the V_Filter voltage, part of I_Fine will be mirrored to the ring.

The output frequency of the VCO is given by

$$f_{VCO} = f_C + K_{VCO}V_C \tag{5-5}$$

where f_c is free running frequency of the VCO and can be tuned by I_Corase. K_{VCO} is constant factor of the VCO and V_c is control voltage. K_{VCO} can be tuned by adjusting I_Fine.

The frequency variation over control voltage is shown in Figure 5-13, where I_fine is 350μA and I_Corase is set to 250μA.

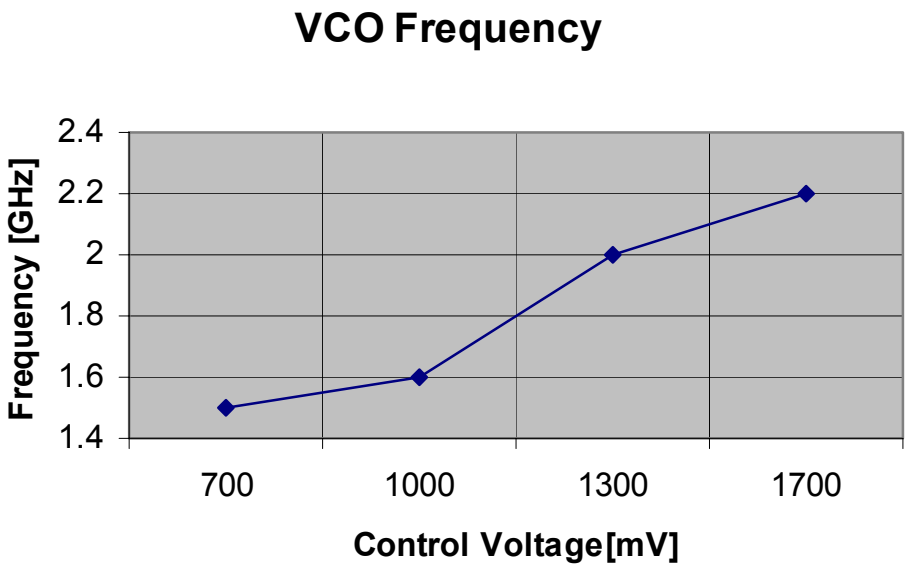

Figure 5-13: VCO tuning characteristic.

The VCO layout is shown in Figure 5-14.

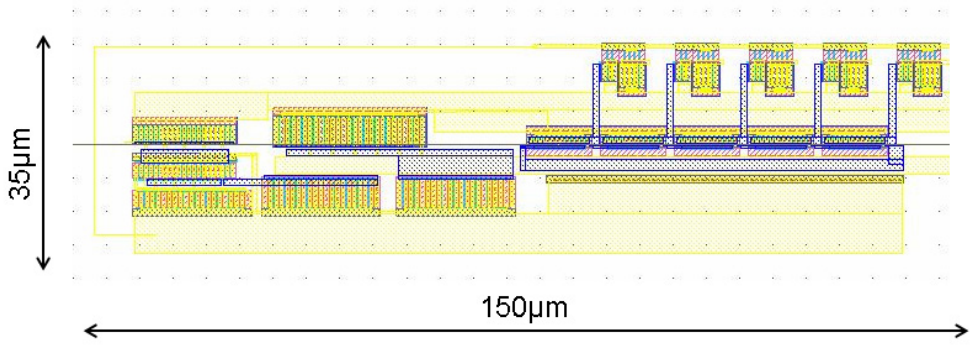

Figure 5-14: Layout of the VCO.

5.2.4 Pulse Generator

As discussed in chapter 4, the SDFF requires reset pulses to operate. An extra block, pulse generator, is designed to generate the reset pulses from the different phases of the VCO outputs. The clock and reset pulses are also buffered in this block. The pulse generator is implemented in static CMOS logic. The schematic diagram of the pulse generator is shown in Figure 5-15. Layout for pulse generator block and buffers are illustrated in Figure 5-16. The generated reset pulses can be seen in Figure 5-17. The reset generator block can be turned off using enable pins. When the block is disabled, the reset pulses stay at low logic. Therefore, the SDFFs operate as NDFF. This option facilitates the comparison of the low swing CDR to the normal CDR.

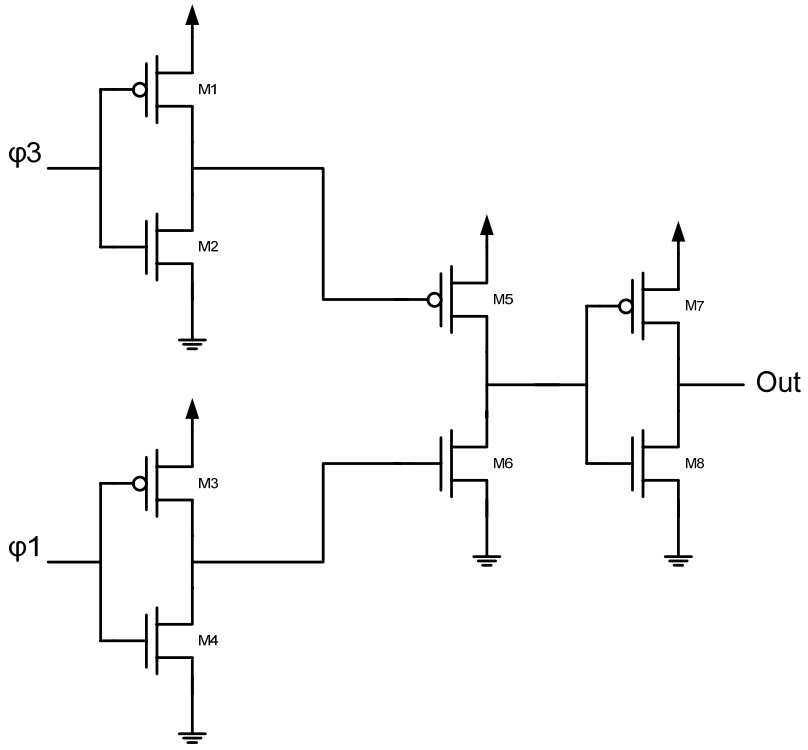

Figure 5-15: Reset pulse generator.

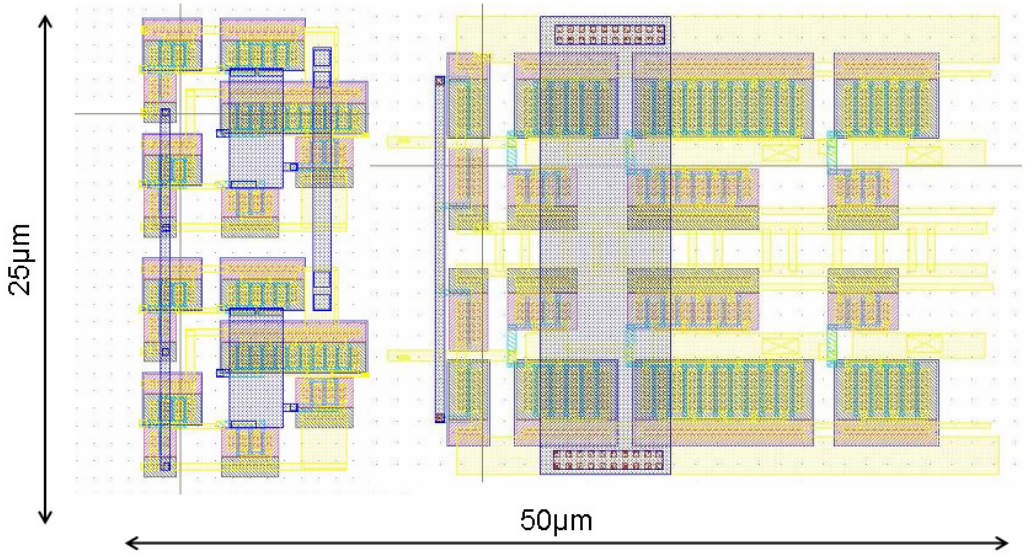

Figure 5-16: Pulse generator and buffers layout.

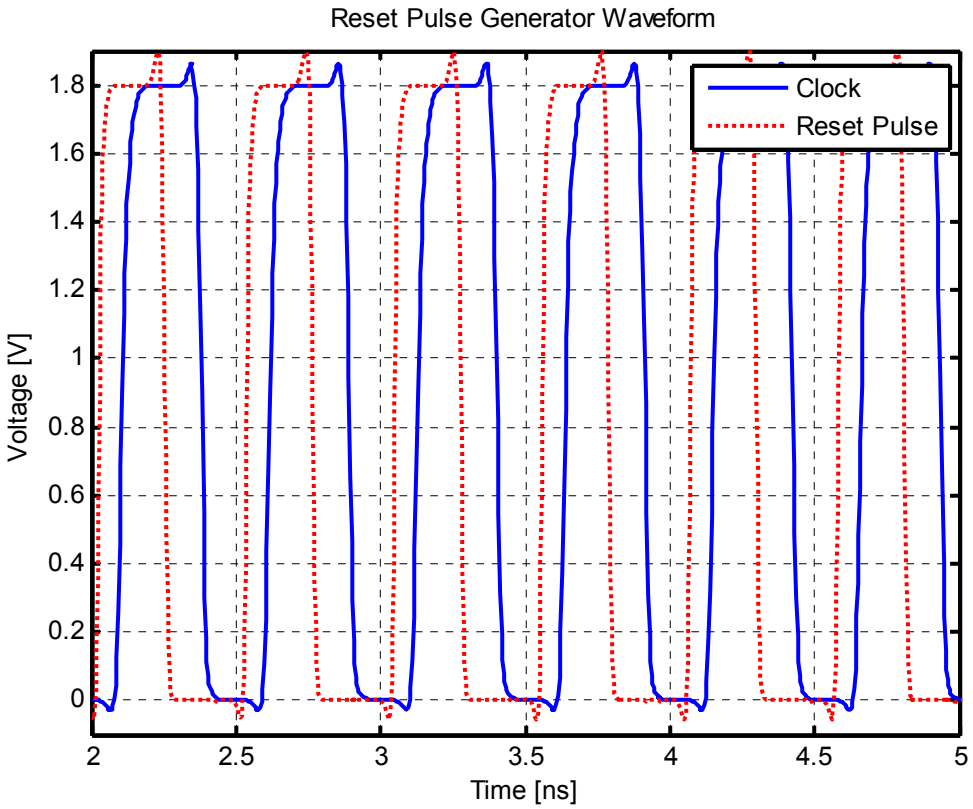

Figure 5-17: Reset pulse wave forms.

5.2.5 Measurement Result

The complete CDR using an external loop filter has been fabricated in the TSMC 180nm CMOS technology. The total area of chip is around 0.02mm^2 and the total power dissipation excluding output drivers is around 4mW from a 1.8V supply voltage. The die micrograph is shown in Figure 5-18. The summary of the CDR performance is given in Table 5-2.

Table 5-2: 2Gbps CDR parameter

Process	180nm CMOS, TSMC
Data rate	2Gbps
Partial rate	Full rate
Input swing	100mV
Peak-to-Peak Jitter	52ps
RMS Jitter	6.2ps
Total power	4mW
Phase detector power	2mW
Core Area (Ex. Pads)	0.02 mm^2

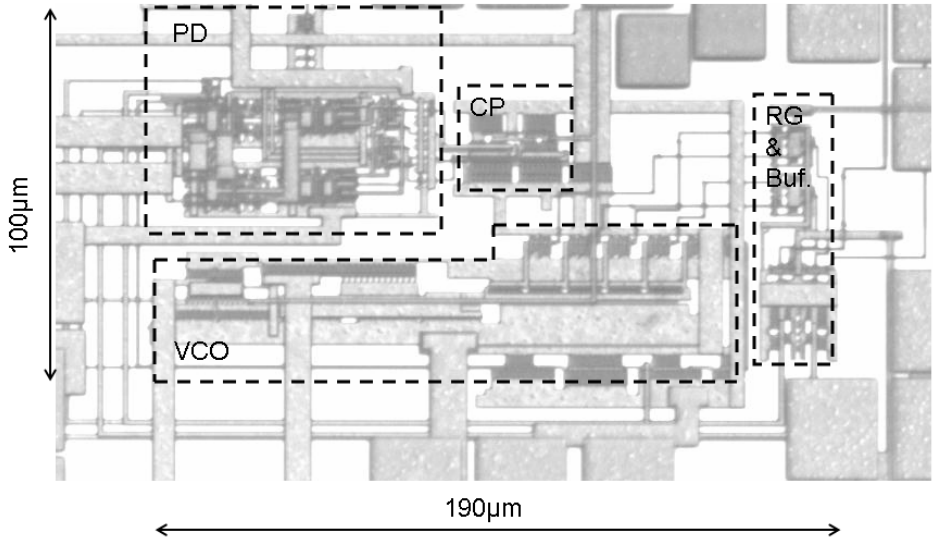

Figure 5-18: Die photograph.

A test bench was setup to measure the CDR's performance. The die was directly bond wired to the high frequency PCB (shown in Figure 5-19). The second PCB has been used to generate the required bias voltages.

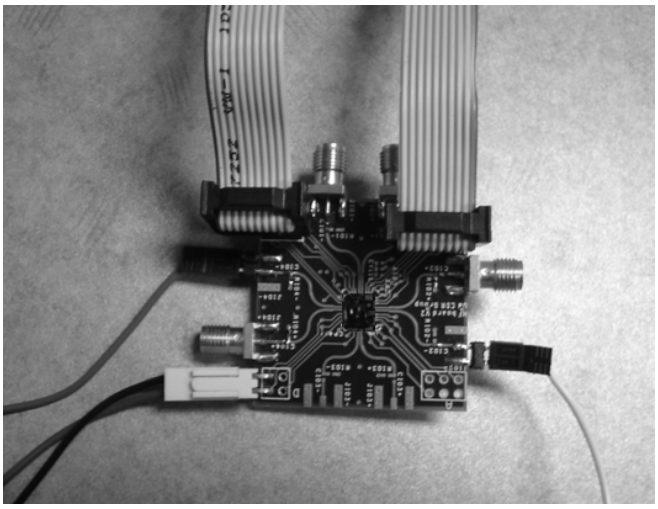

Figure 5-19: PCB board.

The peak-to-peak jitter and bit-error-rate (BER) for PRBS 2^{23}-1 have been measured for different data input swing and shown in Figure 5-20 and Figure 5-21. The minimum detectable data swing was 60mVp with the jitter of 59ps and BER of 1.7E-12. However, by increasing the input data swing jitter and BER both will decrease. When input swing reaches 100mVp, the CDR operates with the peak-to-peak jitter of 52ps. The eye diagram for input swing of 100mV is show in Figure 5-22. The measured RMS jitter is 6.2ps.

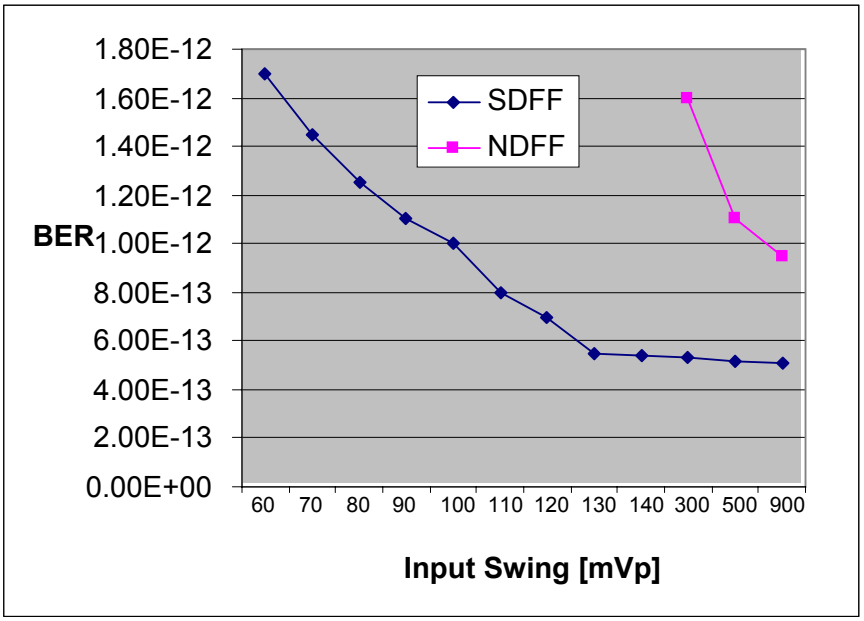

Figure 5-20: BER vs. input data swing.

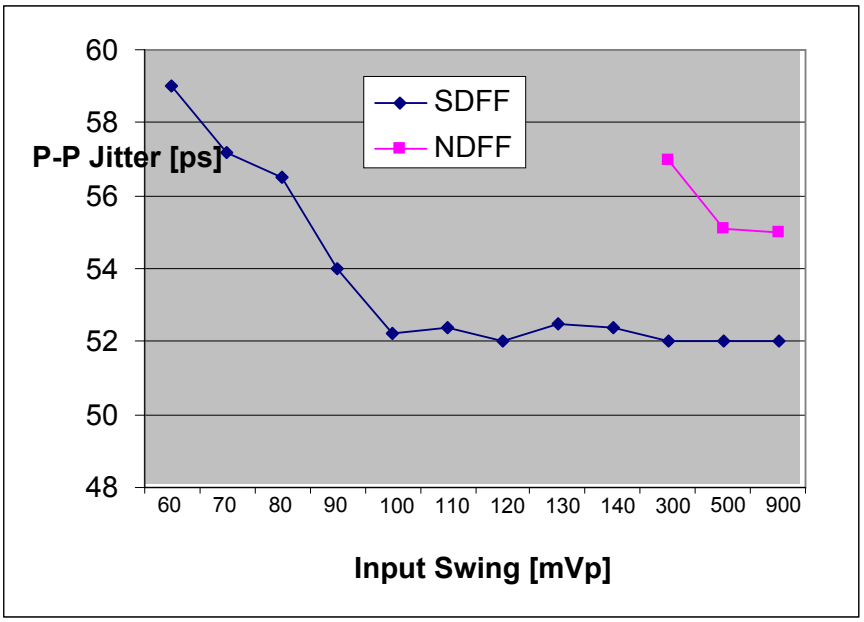

Figure 5-21: Peak-to-Peak jitter vs. input data swing.

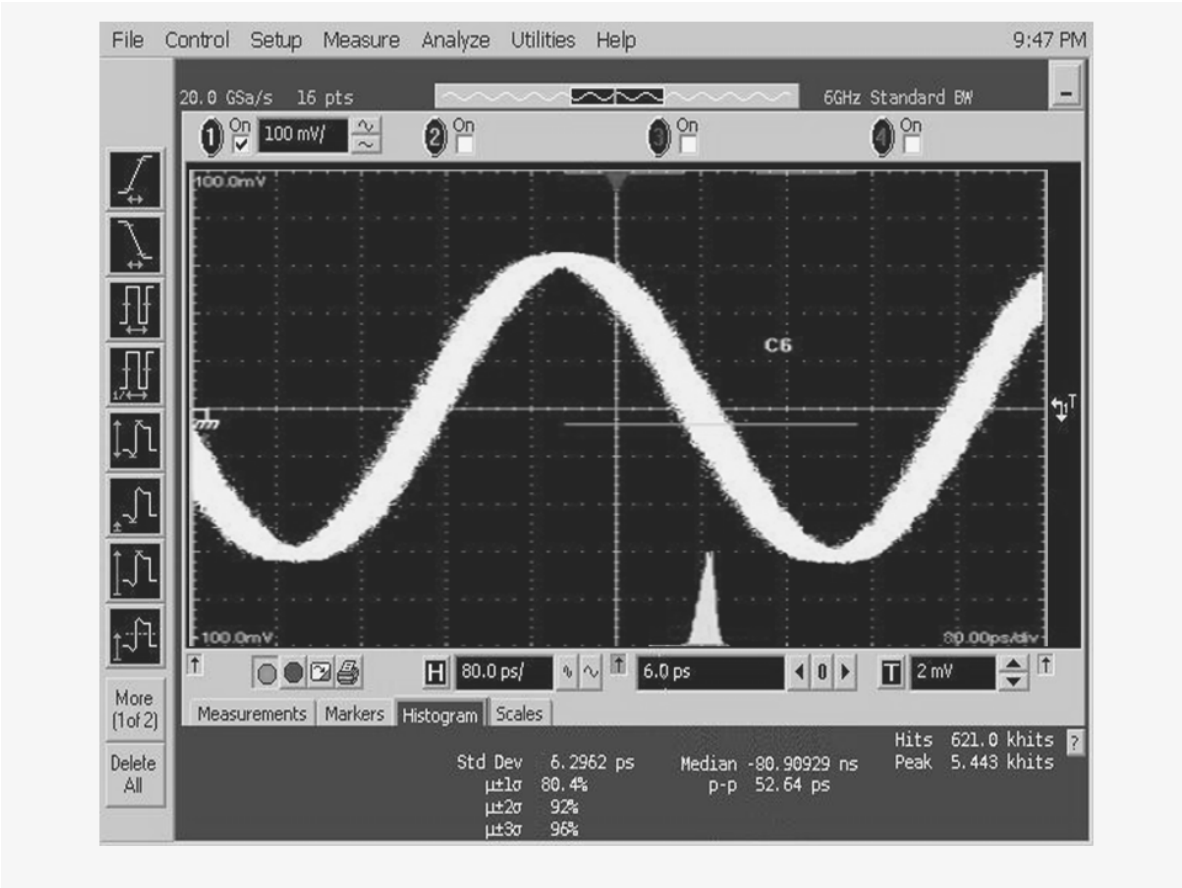

Figure 5-22: Output eye diagram.

If the reset pulses disconnected from the SDFF, then the SDFF will operate as NDFF. In the reset-pulse-off mode, the CDR is able to lock in with a 300mVp input swing with the peak-to-peak jitter of 59ps. When the reset pulses are ON (even in high swing operation), the output jitter is less as compared to the conventional CDR. This improvement is achieved due to the delay reduction of the SDFF at high swing operation. Setup time violation of the CDR results in a nonlinearity at the phase detector characteristic. The

nonlinearity is a function of meta-stability of the D-Flip Flops (wrong sampling of the CDR). As SDFF has less setup time and delay compared to NDFF, jitter and BER are improved.

5.3 The 5 Gbps Low Power CDR Implementation

The second version of the low power CDR was implemented in 90nm CMOS technology. The architecture of the CDR is almost the same as the first version, except a modification on phase detector.

5.3.1 Alexander Phase Detector

The Alexander phase detector in the 0.18μm version (Section 5.2.1) had been designed using two SDFFs followed by two NDFFs. More investigation revealed that the first set of DFFs might result in low-swing output. The low swing output appears in the input of the second set of the DFFs. Consequently, the NDFFs sample the wrong data and result in degrading the BER of the CDR. The new version of the Alexander phase detector consist of four SDFFs. Having the SDFFs in the second row is beneficial for unlocked condition to avoid wrong sampling and results in a better BER. Figure 5-23 shows the schematic of the modified Alexander phase detector and the corresponding layout is illustrated in Figure 5-24.

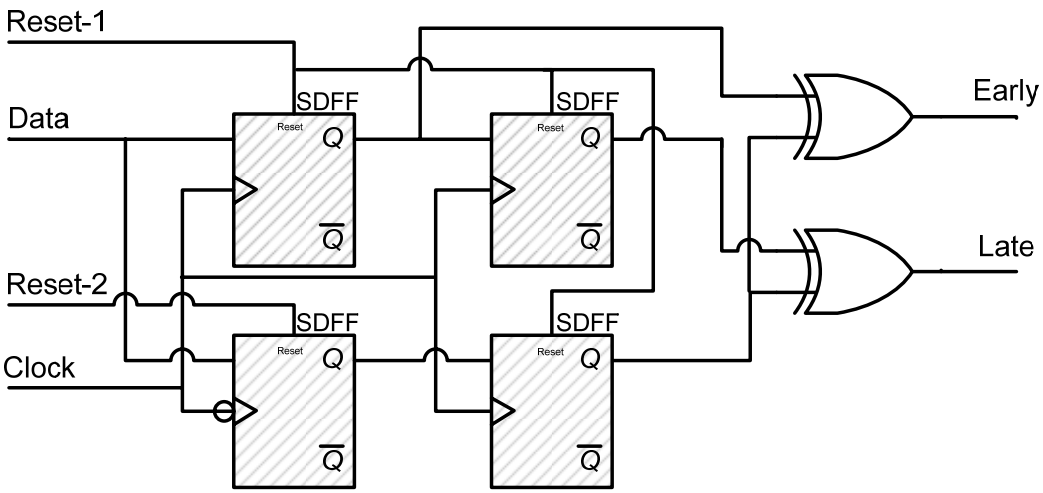

Figure 5-23: Alexander phase detector.

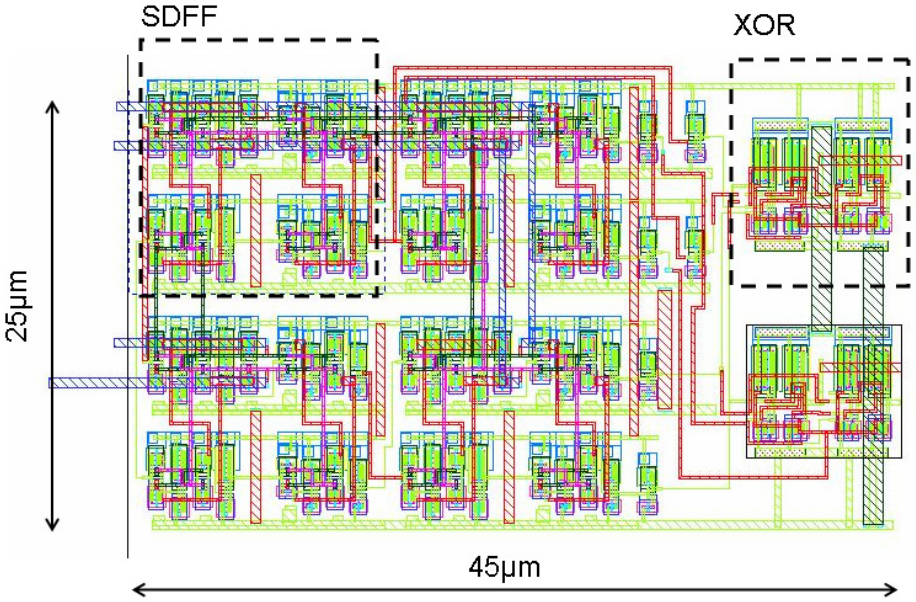

Figure 5-24: Alexander phase detector layout in 90nm.

The phase characteristic of the modified phase detector (Figure 5-25) has smaller linear region as compared to a normal one when the input signal has 50mVpp swing.

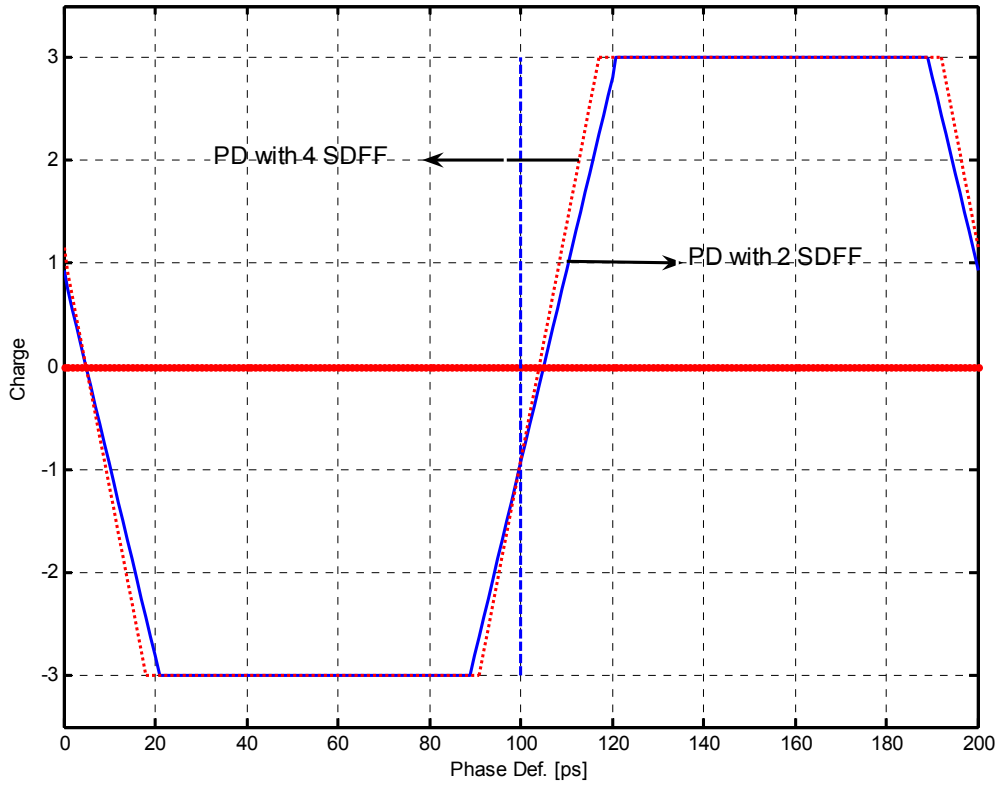

Figure 5-25: 5Gbps binary phase detector characteristic.

5.3.2 Measurement Result

The complete CDR fabricated in the ST Microelectronic 90nm CMOS technology. The supply voltage is 1V. The die micrograph is shown in Figure 5-26.

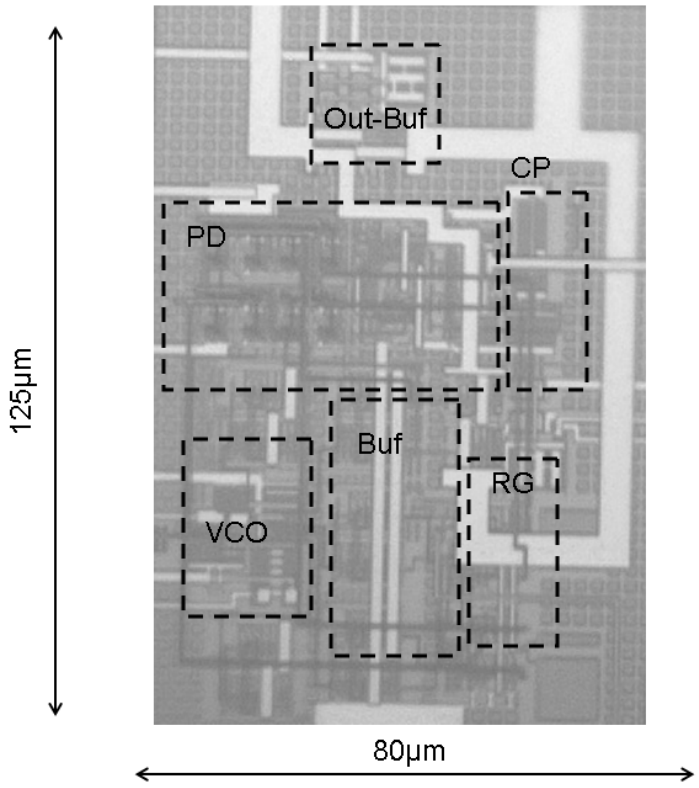

Figure 5-26: 5Gbps CDR die photograph.

Table 5-3 shows the measurement results of the CDR and extracted parameters.

Table 5-3: 5Gbps CDR parameter

Process	90 nm CMOS, ST
Data rate	5Gbps
Partial rate	Full rate
Input swing	70mVpp

Peak-to-Peak Jitter	21ps
RMS Jitter	2.5 ps
Total power	1.7 mW
Phase detector power	0.57 mW
Core Area (Ex. Pads)	0.01 mm^2

A test bench was setup to measure the CDR's performance. The die was directly bond wired to the high frequency PCB (shown in Figure 5-27). The second PCB has been used to generate the required bias voltages.

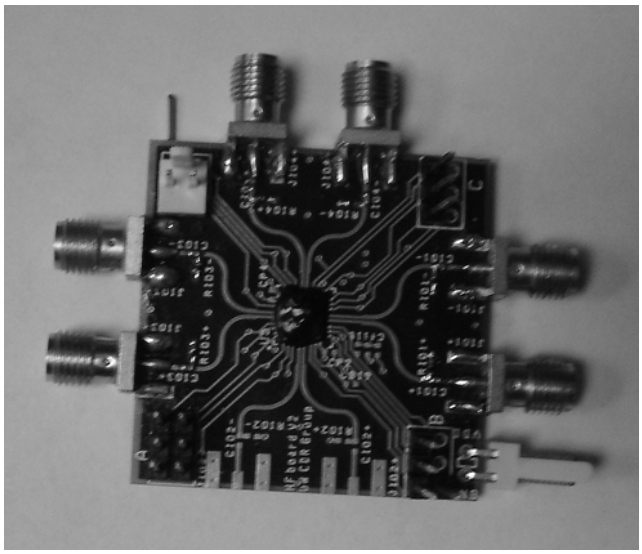

Figure 5-27: PCB board.

The peak-to-peak jitter and bit-error-rate (BER) for PRBS 2^{23}-1 have been measured for different data input swing and shown in Figure 5-28 . The minimum detectable data swing was 15mVp with the jitter of 30ps and BER of 1.1E-12. However, by increasing the input data swing jitter and BER both will decrease. When input swing reaches 35mVp, the CDR operates with the peak-to-peak jitter of 21ps. The eye diagram for input swing of 35mVp is show in Figure 5-29. The measured RMS jitter is 2.5ps.

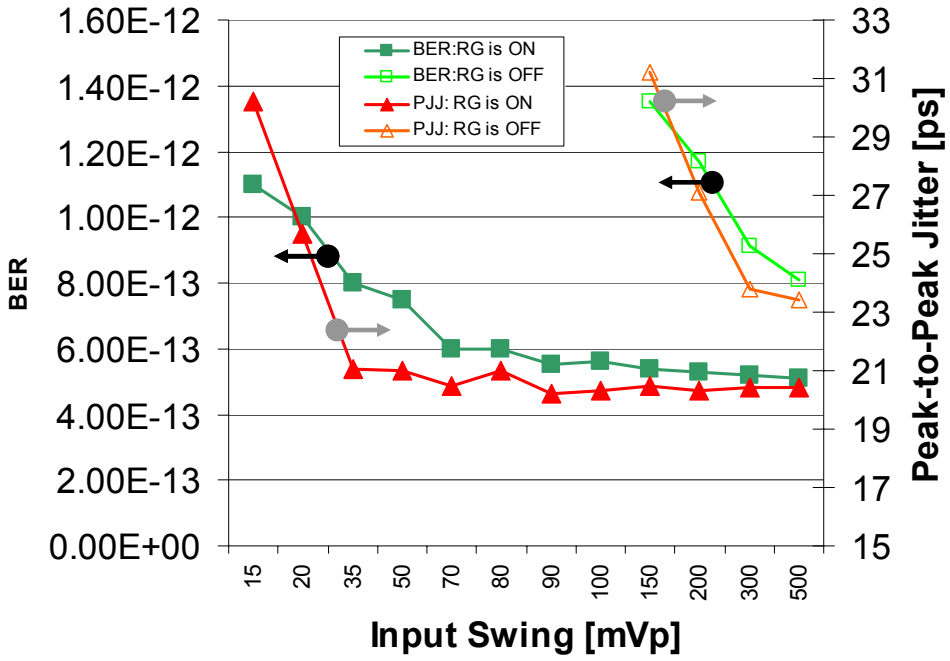

Figure 5-28: RMS Jitter and BER vs. input data swing.

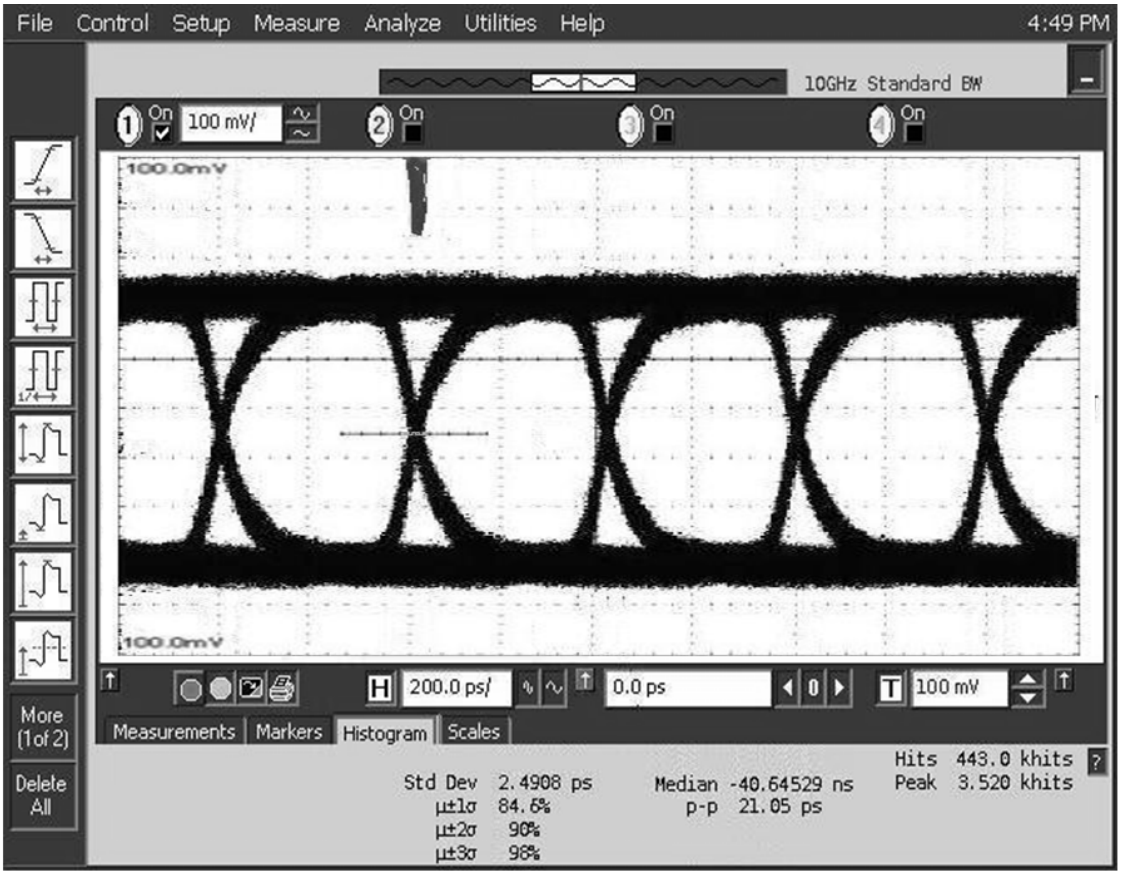

Figure 5-29: Output eye diagram.

By turning off the reset pulse generator, the CDR is able to lock in with a 150mVp input swing with the peak-to-peak jitter of 31ps(Figure 5-28).

Chapter 6

Conclusion

6.1 Conclusion

Serial link communications are widely used in today's data communication. CMOS technology enables more integrity, less power, and lower cost as compared to other technologies such as SiGe. The CMOS implementation of high speed CMOS data transceivers requires high power dissipations. Advances in technology and CMOS scaling in recent years enable the high speed operation of conventional CMOS circuits. Employing standard full swing CMOS circuits to construct a high speed clock and data recovery is beneficial when the low input swing is detectable by standard CMOS sampler. A novel D-Flip Flop (SDFF) has been proposed in standard CMOS to sample the low input swing data. The SDFF dissipates less power compare to the low swing current mode logic DFF. As full swing operation results in more substrate noise, a low substrate noise single ended ring oscillator has been proposed. Single-ended architecture of the proposed VCO results

in low power dissipation. However, it generates less substrate noise in comparison with conventional single-ended VCOs. Two separate CDRs are implemented by employing the SDFF and the low substrate noise VCO. The CDRs are able to detect a low input swing data. Figure 6-1 shows the reported power dissipation for different transceivers over the years. The best power performance has been reported by Rambus Incorporated.

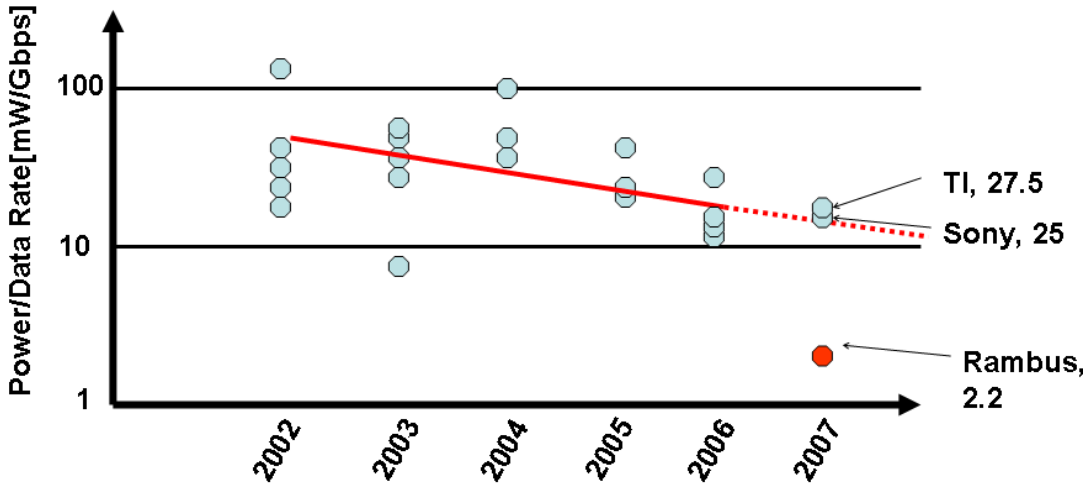

Figure 6-1: Power to data rate ratio over years [1].

Rambus's key to power reduction is the low-swing voltage mode signaling instead of the current mode signaling. Table 6-1 summarizes the Rambus receiver parameters compared to the proposed 90nm CDR.

Table 6-1: Rambus receiver and 90nm proposed CDR parameters

	Rambus (Receiver)[1]	**This Work**
Signal	Reduced Voltage (170mVpp)	Reduced Voltage (70mVpp)
Data Rate	2 X 3.125Gbps	5Gbps
Rate	Half-Rate	Full-Rate
Process	90nm	90nm
Supply	1V and 2.5V	1V
Output Swing	600mV	1V
CDR Power	2.8mW(450μW/Gbps)	1.7mW (340μW/Gbps)
Jitter	PP=14.4ps, RMS=1.27ps (PRBS 2^15-1)	PP=21ps, RMS =2.5ps (PRBS2^23-1)
BER	< 1x10-15 @ 210mVppd	8x10-13 @ 70mVppd
Pre-Amp	2-stage, 6 dB gain, 560μW	None

The proposed 90nm CDR operates at 5Gbps full data rate and dissipates 340μW/Gbps compared to Rambus's transceiver which consumes 450μW/Gbps and operates at half-data rate. In addition, Rambus receiver employs a Pre-Amp with the gain of 10dB and power dissipation of 560μW.

6.2 Future Work

A higher data rate, such as 10 Gbps, can be achieved through mapping the design from CMOS 90nm technology to CMOS 65nm. Fractional-rate clock and data recovery circuit architecture, such as half-rate bang-bang, can be implemented using Switched-DFF to design high data rate CDRs. Jitter performance improvement can be attained by dissipating

more power in the VCO block and implementing the VCO in a differential architecture. The proposed CDRs employ the off-chip analog loop filter. However, the on-chip analog loop filter implementation requires larger silicon area. The new line of research targets the substitution of analog filters by digital filters [2]. The state-of-the-art CDR benefits from automatic calibration techniques to compensate for process variation. The proposed CDRs have manual calibration at this stage.

Reference

[1] Palmer, R.; Poulton, J.; Dally, W.J.; Eyles, J.; Fuller, A.M.; Greer, T.; Horowitz, M.; Kellam, M.; Quan, F.; Zarkeshvari, F., "A 14mW 6.25Gb/s Transceiver in 90nm CMOS for Serial Chip-to-Chip Communications," Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International, vol., no., pp.440-614, 11-15 Feb. 2007.

[2] Liming Xiu; Wen Li; Meiners, J.; Padakanti, R., "A novel all-digital PLL with software adaptive filter," Solid-State Circuits, IEEE Journal of , vol.39, no.3, pp. 476-483, March 2004.