

Sensor System for High Throughput Fluorescent Bio-assays

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

This thesis presents consolidated research results of a low-cost, high efficiency, high throughput detection system for fluorescence-based bio-assays. Such high throughput screening process is an invaluable tool for the multifaceted field of Systems Biology, where it is widely used in genomics and proteomics for drug and gene discovery applications. The thesis is divided into three parts: addressing the feasibility of using hydrogenated amorphous silicon photodiodes as the sensor, the development of an associated compact model suitable for circuit-level simulations, and integration of the sensors and switches to realize the array. Requirements of fluorescent bio-assays demand low sensor dark current densities in the order of 10^{-11}A/cm^2 at room temperature. Fabrication of high quality segmented a-Si:H *n-i-p* photodiodes with such specification is achieved by tailoring defects at photodiode junction sidewalls, where both the dry etching and passivation conditions play important roles. Measurements of the fabricated photodiodes at different temperatures allowed the extraction of reverse current components, which are necessary in modeling such sensors in Verilog-A. Two prototype array designs are fabricated with pixel dimensions matching ANSI standard microwell plates. The functionalities of the small arrays are demonstrated with green LEDs to simulate fluorescent dyes that are commonly used in the high throughput bio-assay processes.

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*To my family
for their unwavering support*

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List of Abbreviations

α	—	Absorption coefficient
α_λ	—	Extinction coefficient
α_{pf}	—	Poole-Frenkel pre-exponential factor
β	—	Transient current power constant
β_{pf}	—	Poole-Frenkel exponential factor
β_{pd}	—	Partial depletion exponential factor per K
β_t	—	Thermally assisted tunnelling exponential factor
β_v	—	Voltage dependence exponential factor
γ_c	—	Voltage proportionality constant for capacitance
δ	—	Absorption depth
δn	—	Change in photodiode ideality factor per K
δn_h	—	Change in photodiode power-law parameter per K
δn_l	—	Change in photodiode ideality factor per K
ϵ_i	—	Linear regression analysis error
ϵ_o	—	Permittivity of free space ($8.854187817 \times 10^{-12}$ [F/m])
ϵ_r	—	Relative permittivity
η_c	—	Charge collection efficiency
η_g	—	Internal quantum efficiency
η_{qe}	—	External quantum efficiency
λ	—	Wavelength
λ_c	—	Vacuum wavelength
λ_d	—	Drift length
λ_{nm}	—	Wavelength in nano-meters
μ_d	—	Drift mobility (effective carrier mobility)
μ_{de}	—	Electron drift mobility
μ_{dh}	—	Hole drift mobility
μ_o	—	Free carrier mobility
$\mu\tau$	—	Mobility-lifetime product
ξ	—	Electric field
ξ_i	—	Electric field across the i -layer
ρ	—	Space charge density
ρ_i	—	Space charge density in i -layer
ρ_n	—	Space charge density in n -layer

ρ_p	—	Space charge density in p -layer
σ	—	Conductivity
σ_e	—	Electron capture cross section
σ_{ext}	—	Extended states conductivity
σ_h	—	Hole capture cross section
σ_{hop}	—	Hopping conductivity at E_F
σ_{oe}	—	Extended states conductivity prefactor
σ_{oh}	—	Hopping conductivity prefactor
σ_{ot}	—	Band tail states conductivity prefactor
σ_{tail}	—	Band tail states conductivity
τ	—	Carrier lifetime
τ_e	—	Electron recombination lifetime
τ_f	—	Frame time
τ_h	—	Hole recombination lifetime
τ_{ill}	—	Illumination duration
τ_{int}	—	Integration time
τ_{max}	—	Maximum time constant for carrier release
τ_{reset}	—	Reset time given to the feedback capacitor
τ_{sam}	—	Sampling time
τ_{select}	—	The address line pulse width
φ_{ph}	—	Photon flux
ω	—	Angular frequency in rads
ω_{oe}	—	Electron excitation rate prefactor
ω_{oh}	—	Hole excitation rate prefactor
2D	—	Two-dimensional
AC	—	Alternating Current
ADC	—	Analog-to-Digital Converter
ADE	—	Analog Design Environment
AGND	—	Analog ground
A_{ill}	—	Transient current constant parameter
A_j	—	Photodiode junction area
Al	—	Aluminum
A_l	—	Photodiode area of large photodiode
AMS	—	Analog and Mixed-signal
ANSI	—	American National Standards Institute
A_o	—	Pre-exponential factor for parameter $J_{D_o}(T)$
A_{oh}	—	Power-law constant for high forward bias region

A_{ol}	—	Pre-exponential factor for low forward bias region
AR	—	Anti-reflection
Ar	—	Argon
A_s	—	Photodiode area of small photodiode
a-Si:H	—	Hydrogenated amorphous silicon
a-SiN _x :H	—	Non-stoichiometric hydrogenated amorphous silicon nitride
BHF	—	Buffered Hydrofluoric Acid
CCCS	—	Current Controlled Current Source
CCD	—	Charge-coupled Device
cDNA	—	Complementary Deoxyribonucleic Acid
CDS	—	Correlated double sampling
C_{int}	—	Feedback Integration Capacitance
C_j	—	Photodiode junction capacitance
C_{line}	—	Data line capacitance
CMOS	—	Complementary Metal-Oxide-Semiconductor
COC		Cyclo-olefin Co-polymer
CPLD	—	Complex Programmable Logic Device
Cr	—	Chromium
Cy3	—	Cyanine with 3 counts of the methines
C-V	—	Capacitance-Voltage
c-Si	—	Crystalline silicon
d	—	Mean free path
DAQ	—	Data Acquisition
DI	—	Deionized
DIP	—	Dual Inline Package
DNA	—	Deoxyribonucleic Acid
DOS	—	Density of States
DR	—	Digital Radiography
E	—	Energy
E_μ	—	Mobility gap
E_a	—	Activation energy
E_C	—	Conduction band mobility edge
E_{CT}	—	Average energy of hopping conduction path
E_F	—	Fermi energy
E_{FD}	—	Quasi-Fermi energy
E_{FN}	—	Fermi energy of n -doped contact
E_{Fn}	—	Electron quasi-Fermi level

E_{FP}	—	Fermi energy of p -doped contact
E_{Fp}	—	Hole quasi-Fermi level
E_g	—	Energy gap
EHP	—	Electron-Hole Pair
EM	—	Electromagnetic
EMI	—	Electromagnetic Inter
E_o	—	Electric field around z_o
E_{ph}	—	Photon energy
E_T	—	Energy of trap state
E_V	—	Valence band mobility edge
f	—	Frequency in Hertz
$f(E)$	—	Fermi-Dirac function
FITC	—	Fluorescein Isothiocyanate
f_p	—	Scaling parameter for forward bias weighting function
f_{ph}	—	Scaling parameter for high forward bias weighting function
f_{pl}	—	Scaling parameter for low forward bias weighting function
FPD	—	Flat-panel Displays
FPGA	—	Field-Programmable Gate Array
FPI	—	Flat-panel Imagers
f_q	—	Center parameter for forward bias weighting function
f_{qh}	—	Center parameter for high forward bias weighting function
f_{ql}	—	Center parameter for low forward bias weighting function
$G(z)$	—	Generation rate
$g(E)$	—	Energy dependent density of states
$g_A(E)$	—	Acceptor-like density of states
G_{amp}	—	Gain of charge amplifier
$g_D(E)$	—	Donor-like density of states
g_{dc}	—	Acceptor-like deep states at the conduction band edge
g_{dv}	—	Donor-like deep states at the valence band edge
GND	—	Power ground
g_{tc}	—	Acceptor-like tail states at the conduction band edge
g_{tv}	—	Donor-like tail states at the valence band edge
GUI	—	Graphic User Interface
h	—	Plank's constant ($6.626069311 \times 10^{-34}$ [Js])
\hbar	—	Dirac's constant (reduced plank constant) ($1.0545716818 \times 10^{-34}$ [Js])
HD	—	High-definition
HDL	—	Hardware Description Language

HGP	—	The Human Genome Project
HTS	—	High Throughput Screening
I_B	—	Bulk or central current component
I_D	—	Photodiode dark current
I_D-V	—	Dark current versus voltage
I_{ill}	—	Maximum illumination current
I_i	—	Measured current for large photodiode
I/O	—	input/output
I_o	—	Miscellaneous current component
I_P	—	Edge or peripheral current component
I_{PD}	—	Total photodiode current
I_{ph}	—	Photocurrent
i_{ph}	—	Current released by photodiode
I_s	—	Measured current for small photodiode
I_{th}	—	Thermal generated current
ITO	—	Indium Tin Oxide
IZO	—	Indium Zinc Oxide
J_B	—	Bulk or central current density
J_{Bo}	—	Pre-exponential parameter for central current density
J_D	—	Dark current density
$J_{Do}(T)$	—	Temperature dependent saturation current density
J_n	—	Electron conduction current density
J_o	—	Saturation current density
J_{oh}	—	Saturation current density for high forward bias
J_{ol}	—	Saturation current density for low forward bias
J_P	—	Peripheral current density
J_p	—	Hole conduction current density
JTAG	—	Joint Test Action Group
J_{th}	—	Thermal generated current density
k_B	—	Boltzmann's constant ($1.380650524 \times 10^{-23}$ [J/K])
L	—	Side length of the photodiode
LASER	—	Light Amplification by Stimulated Emission of Radiation
LCD	—	Liquid Crystal Display
LED	—	Light-emitting Diode
m	—	demagnification
MIS	—	Metal-Insulator-Semiconductor
Mo	—	Molybdenum

mRNA	—	Messenger Ribonucleic Acid
N	—	Nitrogen
n	—	Diode ideality factor or electron concentration
n_0	—	Photodiode ideality factor interpolated at 0K
n_{0h}	—	Photodiode power factor interpolated at 0K
n_{0l}	—	Photodiode ideality factor at low bias interpolated at 0K
NA	—	Numerical Aperture
N_A	—	Acceptor density
n_{air}	—	Index of refraction of air
N_C	—	Effective density of states of the conduction band
N_{dc}	—	Carrier density at E_C for tail states
n_f	—	Free electron density
n_h	—	Power parameter for high forward bias region
n_l	—	Photodiode ideality factor for low forward bias region
n_o	—	Reference electron concentration
n_r	—	Index of refraction
n_{si}	—	Index of refraction of Silicon
n_{sin}	—	Index of refraction of Silicon Nitride
n_t	—	Trapped electron density
N_{tc}	—	Carrier density at E_C for deep states
p	—	Hole concentration
PAN	—	Phosphoric acetic nitric
PCB	—	Printed Circuit Board
PCI	—	Peripheral Component Interconnect
PCR	—	Polymerase Chain Reaction
PECVD	—	Plasma Enhanced Chemical Vapour Deposition
PF	—	Poole-Frenkel
p_f	—	Free hole density
P_l	—	Perimeter of large photodiode
PMT	—	Photomultiplier Tube
p_o	—	reference hole concentration
P_{PF}	—	Probability for Poole-Frenkel
P_{ph}	—	Optical power of incident photons
P_s	—	Perimeter of small photodiode
p_t	—	Trapped hole density
P_{TAT}	—	Probability for thermally assisted tunnelling
q	—	Elementary charge ($1.6021765314 \times 10^{-19}$ [C])

Q_D	—	Depletion charge
Q_e	—	Electron charge
Q_h	—	Hole charge
q_{ph}	—	Charge released by photodiode
R	—	Responsivity or Resistance
r	—	Ratio of electron capture cross section to hole capture cross section
$R(z)$	—	Recombination rate
<i>RESET</i>	—	Reset switch of the charge amplifier
RF	—	Radio Frequency
RIE	—	Reactive Ion Etching
R_o	—	Equivalent shunt resistance
R_r	—	Reflection coefficient
R_s	—	Series contact resistance
R_x	—	Reflectance
R_{\square}	—	Square series contact resistance
SBS	—	Society for Biomolecular Sciences
SNP	—	Single Nucleotide Polymorphism
SNR	—	Signal to Noise Ratio
SPICE	—	Simulation Program with Integrated Circuit Emphasis
SRH	—	Shockley-Read-Hall recombination
S_x	—	First sample switch of CDS
S_y	—	Second sample switch of CDS
T	—	Temperature
t	—	Time
t_{ar}	—	Thickness of the anti-reflection coating
TAT	—	Thermally Assisted Tunnelling
TCO	—	Transparent Conducting Oxide
T_{dc}	—	Characteristic temperature of the deep acceptor-like states
T_{dv}	—	Characteristic temperature of the deep donor-like states
TFT	—	Thin-film Transistors
t_i	—	Thickness of the i -layer
T_{ITO}	—	Transmittance of ITO film
TMB	—	Trimethylborane $B(CH_3)_3$
t_n	—	Thickness of the n -layer
T_{tc}	—	Characteristic temperature of the tail acceptor-like states
TTL	—	Transistor-Transistor Logic
T_{tv}	—	Characteristic temperature of the tail donor-like states

T_x	—	Transmittance
USB	—	Universal Serial Bus
UV	—	Ultraviolet
V_a	—	Applied voltage
v_{amp}	—	Charge amplifier output voltage
V_{bi}	—	Built-in voltage
v_f	—	Free carrier velocity
VHDL	—	VHSIC Hardware Description Language
VHSIC	—	Very High Speed Integrated Circuits
V_i	—	Voltage across the i -layer
V_{in}	—	Input voltage at the charge amplifier
V_n	—	Potential barrier near the n contact
V_p	—	Potential barrier near the p contact
V_T	—	Threshold Voltage
W	—	Hopping energy
W_d	—	Total depletion width
W_n	—	Depletion width in n -layer
W_p	—	Depletion width in p -layer
YAG	—	Yttrium Aluminium Garnet
z_o	—	SRH maximum

Chapter 1: High Throughput Fluorescence-based Bioassays

The completion of the *Human Genome Project* (HGP) in April 2003 marks the advent of the post-genomic era [1]. The primary intention of the project is to attain a complete set of the human genome akin to that of the Periodic Table. The seemingly quixotic task is originally estimated to span over fifteen years. However, owing largely to the improved repertoire of research tools and *high throughput screening* (HTS) processes, the first draft of the human genome is delivered almost four years ahead of schedule [2]. The early completion of HGP and the increasing public awareness of genomics and proteomics relating to personal health have catapulted the introduction of the new interdisciplinary science of Systems Biology where biologists, engineers, chemists, computer scientists, and physicist collaborate to understand the intricate biological systems that exist in multitude of scales. The fruit of Systems Biology introduces an era where predictive, preventive, and personalized medicines are readily available, thus greatly improving the quality of life.

This chapter provides an overview of the HTS process with emphasis on fluorescence-based bio-assays. The current administered technologies are discussed in hopes of ushering the practical application relevance and necessity of this research work. Concurrently, this chapter serves as an introduction where the research motivation and objectives are conveyed.

1.1 *Bio-assays*

The HGP paved the necessary foundations for synthesizing predictive, preventive, and personalized medicines. Due to the complexity and seemingly infinite number of assays performed, large-scale high-volume assay platforms are not only applauded but required.

1.1.1 *From Genomics to Pharmacology*

The importance of predictive, preventive, and personalized medicines is felt by the welcoming improvements of personal healthcare where treatments can potentially be addressed to the need of individual patients. This task may be achieved through the careful orchestration between genomics, proteomics, and pharmacology experiments, which in turn signifies the important social impact of this research work.

Predictive medicine aims to identify the biological markers inherent in individuals that place them at higher risks of developing certain known diseases. This is complemented with preventive medicine which aims to suppress sources of diseases that may affect an entire population; it tries to prevent diseases rather than curing them. The outgrowth of predictive medicine is personalized medicine, where genotypes of patients are used to select medications or therapy targeted to each particular patient.

To synthesize personalized medicine, it is necessary for pharmaceutical companies to assess the drug reactions on individual patients. This is accomplished by exhaustive examination of the protein interactions with

the treatments. The enumeration and quantity of proteins the body produces is dictated by the genes integrated within the *deoxyribonucleic acid* (DNA) of the individual. The length of the human genome is astronomical. The twenty-four distinct chromosomes in a normal human encapsulate 3×10^9 base pairs; within it are the $\sim 30,000$ genes [3]. The DNA sequence of the patients must be mapped since the triple nucleotide codons in the genes moderate the protein productions. Both gene expression analysis and protein interaction observations require HTS processes. Convincingly, high throughput bio-assay platform is an integral part of genomics, proteomics, and pharmacology, where discovery of new genes and drugs relies upon.

1.1.2 Identification Processes

The detail of the assay processes is dictated by the objective of the experiment; therefore, the process for sequencing a DNA fragment is different from those for drug screening or toxicity assessment. To illustrate the high throughput fluorescence-based bio-assay platform, the widely used gene expression profiling process with DNA microarray is presented. Gene expression profiling refers to the analysis of genes in a DNA sequence that is used to produce functional proteins. DNA microarrays are small solid supports containing strands of nucleotides immobilized at regular spacings in a *two-dimensional* (2D) matrix fashion. The solid supports are usually constructed from glass, silicon or nylon membranes. The nucleotide molecules, typically referred to as probes, are usually oligonucleotides, *complementary DNAs* (cDNA), or *polymerase chain*

reaction (PCR) products that correspond to specific *messenger ribonucleic acid* (mRNA). Using borrowed techniques from nanotechnology such as photolithography, ink-jet printing, and nanoimprinting, the probes are fabricated with a known genetic sequence. The 2D array formations of the DNA microarray allow hundreds to tens of thousands of assays to be performed in a single experiment; therefore, it is an excellent example of a high throughput bio-assay platform.

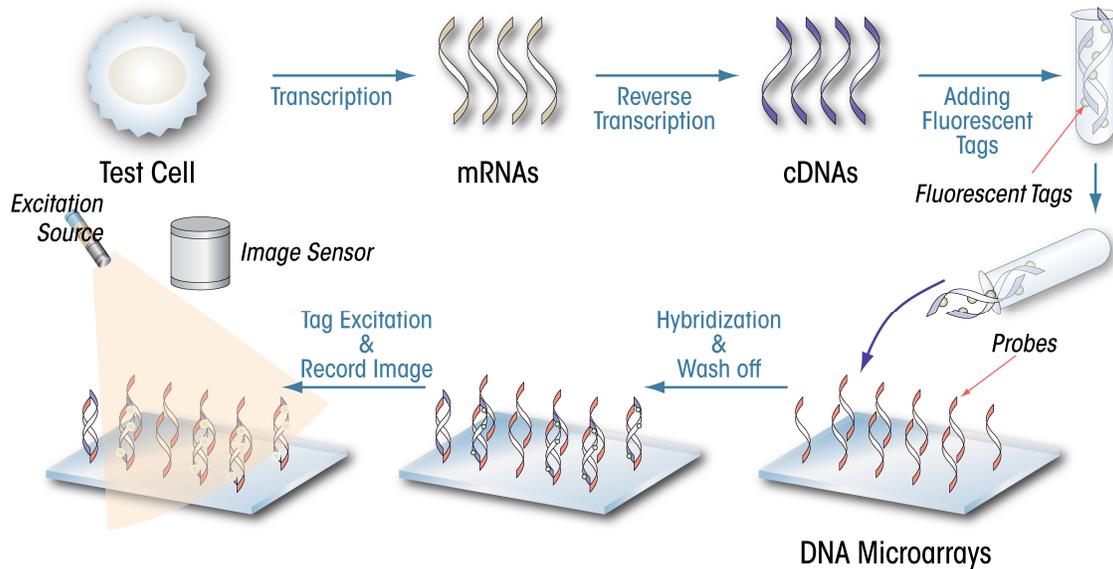


Figure 1-1: An abridged diagram illustrating the gene expression profiling process using high throughput DNA microarrays. The microarray fabrication process is not included in this figure.

Figure 1-1 shows a simplified illustration of the gene expression profiling process using the DNA microarray. The profiling experiment starts with the extraction of mRNAs from test cells. Due to the fragility of mRNAs, they are often reverse-transcribed to the more stable cDNA form. They are

typically referred to as targets. The targets are subsequently tagged with fluorescent dyes and washed over the prepared microarray. Hybridization then occurs over a time interval when the genes are expressed. That is, the fluorescently-tagged targets are bonded to the immobilized probes on the microarray. The unbonded targets are washed off so that only sites with hybridized probes remain on the microarray. The fluorescent tags on the remaining targets are energized and the illuminated assay sites are photographed by a camera. The photograph is subsequently analyzed by computer software packages to determine the intensity of the spots, which correlates to expression levels. This research work targets the imaging technology used in the final stage of the assay process.

1.2 *Current Detector Systems*

The discussion of HTS platform emphasizes that the speed per assay is an important figure of merit. Features of microarrays and macroarrays that dictate the assay performances are not limited to speed alone; substrate material, immobilization resolution of oligonucleotides, and scanner sensitivity are also crucial parameters. In keeping with the relevance of this research work, the discussions in this section focus on the detector systems used in the final imaging stage of the assays, which is used in all high throughput fluorescence-based bio-assay processes.

The components of the current commercial detector systems include: 1) an excitation source to activate the bonded fluorescent molecules 2) sophisticated optical assemblies to provide a means of scanning the

samples at desired resolution 3) image sensors and complementing software package for evaluating the magnitude of the fluorescence signals 4) mechanical framework to orient the microarray plates and optical system during scanning.

1.2.1 Excitation Sources and Strategies

Table 1-1 compares the common light sources used in microarray scanners. Solid-state lasers are favoured due to their smaller size and simpler integration with control electronics. Depending on the specifications of the tagging molecules used, excitation strategies are also important to reduce photobleaching. Table 1-2 lists some of the commonly used excitation strategies for microarray detectors.

Table 1-1: A comparison between common light sources used to excite the fluorescent tags in microarrays; compiled from [4].

Light Sources	Description	Advantages	Disadvantages
Gas Laser	<ul style="list-style-type: none"> ▪ Electric current is discharged through gas to produce light ▪ Helium-Neon, 635nm 	<ul style="list-style-type: none"> ▪ Commonly available ▪ Available in specific wavelengths 	<ul style="list-style-type: none"> ▪ Large, hot, and fragile
Solid-state and Semiconductor Laser	<ul style="list-style-type: none"> ▪ A laser that uses a solid crystal as the gain medium ▪ Fixed wavelength ▪ Yttrium Aluminium Garnet (YAG), 532nm 	<ul style="list-style-type: none"> ▪ Small, efficient, and controllable ▪ Long life 	<ul style="list-style-type: none"> ▪ Wavelength choices are restricted to a limited set
White Light Source	<ul style="list-style-type: none"> ▪ Xenon arc light source ▪ Range of wavelengths from 350nm to 750nm or more 	<ul style="list-style-type: none"> ▪ Single source is adequate for multiple excitations 	<ul style="list-style-type: none"> ▪ Large, hot and fragile ▪ Needs filters to isolate wavelengths ▪ Lower intensity than laser source

Table 1–2: A comparison between common excitation strategies used in microarray scanners; compiled from [4].

Excitation Strategy	Description	Advantages	Disadvantages
Simultaneous Excitation	<ul style="list-style-type: none"> Light sources excite multiple dyes in the same pixel at the same time 	<ul style="list-style-type: none"> Increased scanning speed 	<ul style="list-style-type: none"> Increased crosstalk Reduced SNR
Pixel Shifting	<ul style="list-style-type: none"> Light sources excite multiple dyes at different pixels at the same time 	<ul style="list-style-type: none"> Reduced crosstalk Increased SNR 	<ul style="list-style-type: none"> Misalignment Require image registration
Fiber Optics	<ul style="list-style-type: none"> Fiber optic cables direct light from external light source to scanning optics 	<ul style="list-style-type: none"> Allow large lasers and alternative light sources 	<ul style="list-style-type: none"> Reduced optical power delivery Reduced resolution
Gated Laser	<ul style="list-style-type: none"> Light sources are toggled One light source excite one pixel at a given time 	<ul style="list-style-type: none"> Laser lifetime extended Eliminated crosstalk 	<ul style="list-style-type: none"> Reduced scanning speed

1.2.2 Image Sensors

The two types of sensors currently used in microarray scanners are *charge-coupled devices* (CCD) and *photomultiplier tubes* (PMT). Invented in 1969 by Bell Laboratory, CCDs dominated the digital imaging market for over 25 years [5]. CCD image sensors are built as a matrix of light-sensitive capacitors where the photogenerated charge are stored and sequentially read. Even though the rival *complementary metal-oxide-semiconductor* (CMOS) sensors have replaced many of the mainstream applications due to their lower power consumptions, faster imaging speed, simpler clocking scheme, and better system integration, CCDs remain to be the preferred sensor for HTS applications due to its superior image quality in terms of noise, uniformity, and dark current levels [6]. In contrast, PMTs are

extremely sensitive photon detectors. Their operation is based on the multiplication of photogenerated electrons via dynodes, where the amplification can be as large as 10^8 times. The ability for PMTs to amplify very faint light signals places them as the most sensitive detector type currently used for microarray readout.

1.3 Research Motivation

The aspiration of this doctoral research stems from the necessity to address critical issues that is inherent in the current state-of-the-art high throughput bio-assay detectors. The goals of this research are three folds. There is an immediate need to assess the feasibility of using *hydrogenated amorphous silicon* (a-Si:H) photodiodes as the underlying sensor for fluorescence-based bio-assays. Doing so would address issues in terms of excessive cost, low throughput, and poor efficiency that haunt the current imaging systems. Then it is necessary to cultivate the underlying technology elements needed to realize such sensor systems. Finally, it is necessary to develop a compact model for a-Si:H photodiode suitable for circuit-level simulations. The model should be compatible with current circuit simulators used for *crystalline silicon* (c-Si) devices and technologies. The discussion in this section focuses on some of the critical issues inherent in the current CCD and PMT detector systems. At the same time, it presents some of the benefits offered by a-Si:H photodiodes which address these issues. It thus serves as a justification for the research conducted.

1.3.1 Benefits of a-Si:H-based Detection Systems

Hydrogenated amorphous silicon can be fabricated in large areas due to relaxed deposition environment requirements. Although a-Si:H can be manufactured to yield better spatial uniformity in comparison with c-Si, it is much inferior in terms of temporal stability. Nevertheless, such technology has already been demonstrated in commercialized large-area *flat-panel displays* (FPD). The seventh generation process for example, allows fabrication of electronic backplanes based on a-Si:H *thin-film transistors* (TFT) on 1.87×2.2m² sized glass substrates [7], which are found in large-area widescreen *high-definition* (HD) *liquid crystal displays* (LCD) televisions and computer monitors. Large area fabrication capabilities have several implications in bio-assay detector technologies in terms of throughput, costs and detection efficiency.

Throughput

Even though assay detector systems with PMTs as the underlying sensor technology can only detect a single site each time, the fast response time allows them to complement detection systems with very competitive scanning speed as high quality CCD systems. The average time required for CCD systems to scan a 25×75mm² area is ~10 minutes [8]–[11], which translates to a scan rate of 3mm²/sec. Depending on the spatial resolution of the assay sites, a throughput of one million genotypes per day using 20,000 *single nucleotide polymorphism* (SNP) substrates is common [8]. Given that each assay site is ~2×2mm², large-area detectors based on a-

Si:H photodiodes can potentially perform $\sim 10^6$ assays per run; therefore, improving the assay throughput by multiple magnitudes.

Cost

CCD sensors are costly to fabricate; 17"×17" TFT array introduced recently for the *digital radiography* (DR) application costs over \$218,000 [12]. The relaxed environmental constraints allow a-Si:H to be deposited at lower cost and higher yield. The lower deposition temperatures (120–260°C) delivers the possibility of fabricating photodiodes on flexible and robust substrates such as aluminum foils, providing the possibility of accelerated production at fractions of the cost with high throughput manufacturing processes. Large imaging areas also ease the resolution requirements for manufacturing microarrays and liquid dispensing systems for microwells where the area per assay can be increased by three orders of magnitude. It also eliminates the use of high-cost precision instruments, yielding an overall lower cost assay system.

Efficiency

The large area capability allows a-Si:H systems to be used as contact-type sensors; therefore, avoiding the use of any optical couplers such as lenses or optical fiber. The laws of optics dictate that the efficiency of the lens coupling is determined largely by the solid angle subtended by the collecting optics. For a single lens system, best possible light collection efficiency is $\sim NA/(m^2 + 1)$ [13] where NA is the numerical aperture of the relay lens and m is the demagnification factor [14]. Even with an expensive

1"×1" CCD, the practical collection efficiency from an 8×8cm² area would not exceed 1%. Contact-type sensors eliminate the enormous losses due to optical coupling; therefore, increases the overall detection efficiency. This is especially important since faint signals emitted from fluorescent dyes require very sensitive detectors. An added benefit of a-Si:H based detectors is the promising possibilities of fabricating sensors with <1pA/cm² dark current density levels at room temperature. Together with the elimination of optical losses, it is possible to build a detector system that does not rely on bulky and expensive cryogenic cooling equipments. Cryogenic assemblies are usually implemented in CCD and PMT detector systems to reduce the background dark current; doing so increases the sensitivity of these systems required for drug and gene discovery assays.

1.3.2 Readout with a-Si:H *n-i-p* Photodiodes

The low photon count produced by the fluorescent dyes emphasizes the need for highly sensitive detectors. Hydrogenated amorphous silicon *n-i-p* photodiodes offers itself as a promising candidate for low photon flux detection applications in views of its low dark current and high absorption efficiency in the visible spectrum. Oligonucleotides and PCR products typically have base counts ranging from 25b to 20kb; proteins molecules may have even higher counts. Binding the long chains with fluorescent dyes typically result in photon flux in the range of 10³–10⁶ph/mm²/sec. Since not all photons received by the photodiode are successfully collected, a conversion efficiency of ~80% brings the photo-induced current density between 10fA/cm² to 10pA/cm².

Table 1-3: A comparison of the performances of various image sensors utilizing a-Si:H technology. *p-i-n* and *n-i-p* photodiodes offer one of the lowest dark current levels.

	Photoconductor	Schottky	<i>p-i-n</i> & <i>n-i-p</i>	Photo TFT
Sensitivity	High	Low	Low	High
Response Time [μ s]	Slow ~500	Fast ~50	Fast <5	Slow ~500
Dark Current [A/cm ²]	~10 ⁻⁶	10 ⁻⁷ ~10 ⁻⁹	10 ⁻¹⁰ ~10 ⁻¹¹	10 ⁻⁷ ~10 ⁻⁸
Stability	Good	Good	Good	Marginal
Large Area Capability	Yes	Yes	Yes	Yes

Table 1-3 compares the performances of various a-Si:H sensors; among them a-Si:H *n-i-p* photodiodes offers the lowest dark current levels, surpassing other sensor structures. The 10–100pA/cm² current density level at room temperature for typical a-Si:H *n-i-p* device indicates that at low illumination range the photocurrent falls below the dark current level required for these types of sensors. Therefore, charge integration time of 60–600 seconds is needed. This time requirement is comparable to that offered by CCD and PMT detector systems.

The intrinsic material properties of a-Si:H allow them to be used in thin-film detectors to produce high absorption efficiency in the green spectrum. Fluorophores such as *fluorescein isothiocyanate* (FITC), rhodamine, and cyanine can be attached to molecules such as proteins. Depending on the molecular configuration, they can emit maximally between 510nm and 570nm when excited. Cy3 dye for example, emits maximally at 550nm which is close to the peak quantum efficiency of 500nm thick a-Si:H *n-i-p* photodiodes. The maximal excitation wavelength is shorter than the emission wavelength, some of which falls in the *ultraviolet* (UV) spectrum.

In the case where the excitation wavelength is close to the emission wavelength, optical filters can be implemented to reduce signal crosstalk. Optical filters with very high transmittance (>90%) and narrow spectrum selection (<10nm) are not prohibitively expensive (~\$300). These benefits place a-Si:H *n-i-p* photodiodes as a competitive candidate to use as the underlying detector in high throughput fluorescence-based bio-assay applications.

Chapter 2: Hydrogenated Amorphous Silicon $n-i-p$ Photodiodes

The positive assessment of employing a-Si:H $n-i-p$ photodiodes as the assay detectors prompt for a more in-depth discussion on the device. This chapter outlines some of the recent advancements of the ongoing research of a-Si:H $n-i-p$ photodiodes. The discussion first focuses on the electronic properties of the a-Si:H material to establish the necessary foundations required to examine the photodiodes. The physics and electronic characteristics of a-Si:H $n-i-p$ photodiode are subsequently delivered. The results of the discussions form an important basis for the design of the assay sensors presented in Chapter 6.

2.1 *Hydrogenated Amorphous Silicon*

For a-Si:H $n-i-p$ photodiodes, the electronic properties of the intrinsic layer (i -layer) play critical roles in the device performances. Table 1-1 compares the typical material parameters between c-Si:H and a-Si:H. Amorphous silicon is often regarded as a derivative of crystalline silicon where the existing disorder degrades its electronic properties. Even though amorphous silicon poses no long range structural periodicity, short range order is still present; the resulting structure is a random atomic network full of dangling bonds and voids. A comparative illustration between c-Si and a-Si:H bonding structures is shown in Figure 2-1.

Table 2-1: A comparison of the typical material parameters between crystalline silicon (c-Si) and hydrogenated amorphous silicon (a-Si:H).

Electrical Properties	c-Si	a-Si:H
Energy Gap (E_g) [eV]	1.12	1.7–2.0
Conductivity (σ) [S/cm]	4×10^{-6}	$10^{-8} - 10^{-12}$
Relative Permittivity (ϵ_r)	12.0	~11.8
Electron Mobility (μ_{de}) [$\text{cm}^2/\text{V}\cdot\text{sec}$]	10^3	~1.0
Hole Mobility (μ_{dh}) [$\text{cm}^2/\text{V}\cdot\text{sec}$]	10^2	$10^{-3} - 10^{-2}$
Electron Diffusion Length [μm]	300	<10
Hole Diffusion Length [μm]	200	~0.1
Defect Density [cm^{-3}]	$<10^7$	10^{15}
Hydrogen Concentration [at.%]	—	10

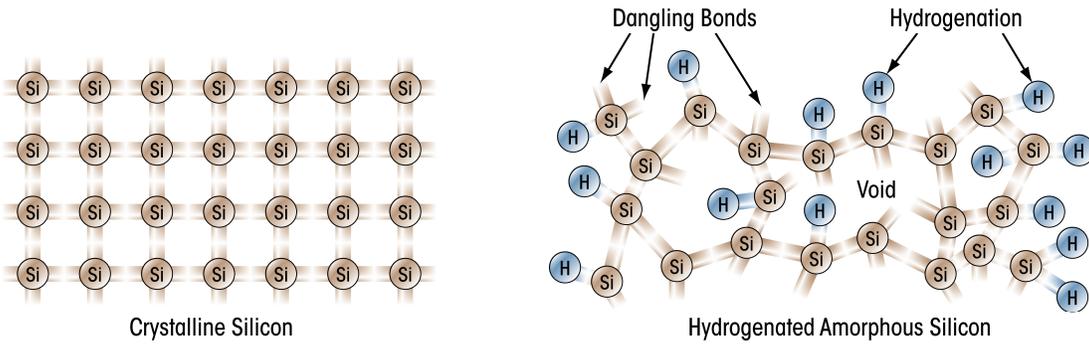


Figure 2-1: An illustration of the atomic bonding structures of crystalline silicon (c-Si) and hydrogenated amorphous silicon (a-Si:H). Coordination defects such as voids and dangling bonds are shown along with hydrogenation for a-Si:H.

Early fabrication processes for amorphous silicon led to very high defect densities, which cause severe degradations in its electrical properties. The carrier mobility and temporal stability stands far from that of crystalline silicon, which rendered amorphous silicon as an impractical material for most electronic devices [15]. Hydrogenation of amorphous silicon provided the much needed improvements in electronic properties [16]. The hydrogen atoms are responsible for lowering the defect densities by passivating the dangling bonds; this is critically important in terms of

carrier transport since the dangling bonds often behave as effective recombination centers for electrons and holes.

2.1.1 Device Quality *a*-Si:H

Figure 2-2 shows a timeline for the development of device quality *a*-Si:H [15]–[21]. The first breakthrough occurred in 1970 when it is discovered that *a*-Si:H deposited via silane (SiH_4) plasma greatly improved its electronic properties. The second breakthrough came around 1975 with the discovery of substitutional doping, where *n*-type and *p*-type conduction can be respectively achieved with the addition of phosphine (PH_3) and diborane (B_2H_6) into the plasma during growth.

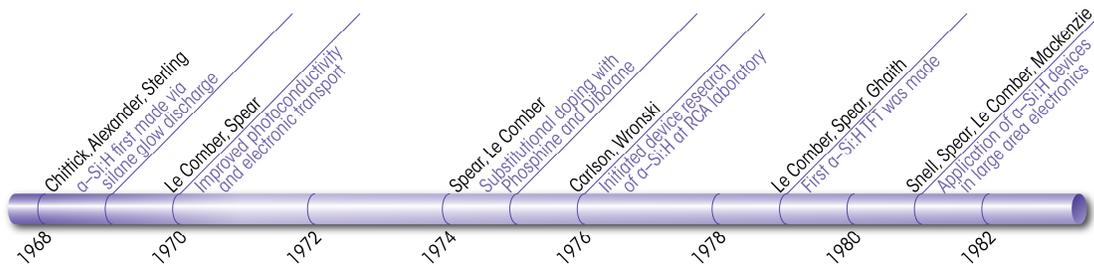


Figure 2-2: An abridged timeline of the *a*-Si:H material development between 1969 and 1981. Exploration of different fabrication techniques within the twelve year period has delivered device quality *a*-Si:H found in current electronic backplanes of large area displays. Timeline compiled from reference [15] to [21].

Although deposition system design has evolved since its initial conception, the growth of device quality *a*-Si:H films are still commonly done by the *plasma enhanced chemical vapour deposition* (PECVD) technique. In the absence of plasma, silane gas decomposes at $\sim 450^\circ\text{C}$; this temperature is too high for the grown film to retain hydrogen yielding low quality materials. Plasma in PECVD systems offers the required energy source to

dissociate silane at much lower temperatures so permitting the growth of films. The electronic structure of the films is mostly influence by defect reactions taken place within the material after growth, independent of the growth process details. Low defect density a-Si:H in the range of 10^{15} – 10^{16}cm^{-3} can be fabricated with $\sim 260^\circ\text{C}$ substrate temperature and low RF power ($<5\text{W}$), at growth rate of $1\text{--}3\text{\AA}/\text{s}$.

2.1.2 Density of States Distribution

The energy-dependent *density of states* (DOS), $g(E)$, can efficiently describe the electronic characteristics of a-Si:H. Figure 2–3 shows a crude depiction of the DOS distribution of a-Si:H and c-Si. For c-Si material, energy band formation is a consequence of the periodicity of the crystalline lattice where the separation of the bonding and anti-bonding states yields the forbidden energy gap. For an ideal crystal, there are no states within the energy gap, and the edges of the energy gap are well defined. The energy bands are strongly influenced by the short range order which also exists in a-Si:H; therefore, the overall shape and framework of the c-Si energy gap can still be applied for a-Si:H with small perturbations.

The long range disorders of a-Si:H, represented by the deviations in the bond lengths and bond angles (Figure 2–1), yield broadened tails of states extending into the forbidden energy gap. The width of the band tails depend on the degree of disorder. Structural defects such as dangling bonds and voids are not split by the interactions of the bonding orbitals; therefore, introduces electronic states deep within the band gap. The

disorder in a-Si:H leads to the presence of localized states for which the carrier mobility vanishes at zero temperature ($T=0\text{K}$). The localized tail states are separated from the extended band states by the mobility edge as shown in Figure 2-3. Hydrogen bonds in a-Si:H also introduces extra states in the valence band and causes shifting of the band edge [22].

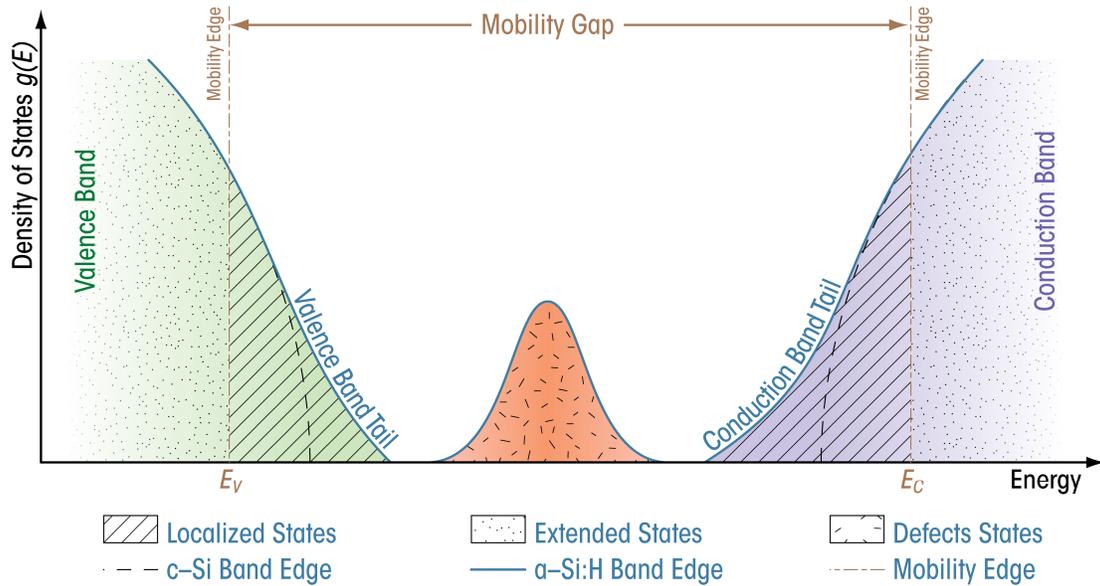


Figure 2-3: A rough schematic of the density of states (DOS) distribution for a-Si:H and c-Si material. The density of states for a-Si:H is divided into three different energy ranges; the main conduction and valence bands, the band tails, and the defect states in the forbidden energy gap.

The distribution of localized states in a-Si:H has pivotal importance on its carrier transport properties; therefore, it has been extensively studied by using various experimental techniques [23]–[28]. The results of the studies suggest that the distribution of localized states in the mobility gap (E_μ) of a-Si:H can be approximated by exponential distributions of the deep tail

states for both the acceptor-like and donor-like states [29]–[30]. This DOS approximation is calculated and plotted in Figure 2–4.

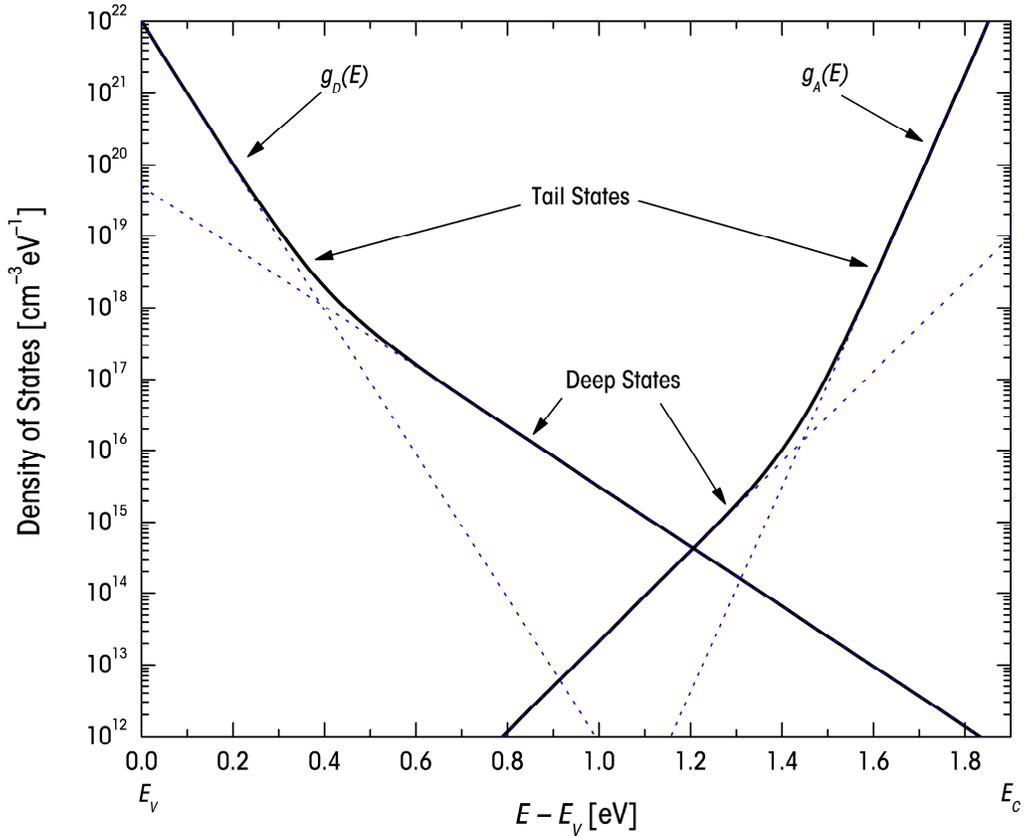


Figure 2–4: A plot of the density of states in the mobility gap of device quality a-Si:H. The asymmetry of the distribution bends the Fermi energy of intrinsic a-Si:H slightly towards the conduction band. Characteristic parameters are adopted from [30].

The mobility gap of a-Si:H, defined as the difference between the conduction band edge (E_C) and valence band edge (E_V), is estimated to be in the range of 1.85–1.9eV [15]. The localized states close to the conduction band edge above the Fermi energy level behave as acceptor-like states ($g_A(E)$). The states closer to the valence band edge below the Fermi energy level behave as donor-like states ($g_D(E)$). Acceptor-like states

are neutral when they are empty and negatively charged when occupied by an electron. Donor-like states are positively charged when they are empty and neutral when they are occupied by an electron. Based on the exponential DOS distribution approximation, $g_A(E)$ and $g_D(E)$ can be written as

$$g_A(E) = g_{tc} \exp\left(\frac{E}{k_B T_{tc}}\right) + g_{dc} \exp\left(\frac{E}{k_B T_{dc}}\right) \quad (2.1)$$

$$g_D(E) = g_{tv} \exp\left(\frac{E_V - E}{k_B T_{tv}}\right) + g_{dv} \exp\left(\frac{E_V - E}{k_B T_{dv}}\right). \quad (2.2)$$

Here, energy E is defined negative for states in the mobility gap with respect to the conduction band edge, E_C . k_B is Boltzmann's constant and T is temperature. g_{tc} , g_{dc} , g_{tv} , g_{dv} , T_{tc} , T_{dc} , T_{tv} , T_{dv} represents the tail and deep acceptor-like states at the conduction band edge, the tail and deep donor-like states at the valence band edge, the slopes of the tail and deep acceptor-like states, the slopes of the tail and deep donor-like states. Typical values of these characteristic parameters are given in Table 2-2.

Table 2-2: Typical values for the characteristic parameters of the exponential density of states model for intrinsic a-Si:H (compiled from [30]).

Parameters	Tail States	Deep States
Density of States at E_C [$\text{cm}^{-3}\text{eV}^{-1}$]	$g_{tc} \sim 5 \times 10^{22}$	$g_{dc} \sim 1 \times 10^{19}$
Density of States at E_V [$\text{cm}^{-3}\text{eV}^{-1}$]	$g_{tv} \sim 1 \times 10^{22}$	$g_{dv} \sim 5 \times 10^{19}$
Exponential Slope for E_C [K]	$T_{tc} \sim 350$	$T_{dc} \sim 800$
Exponential Slope for E_V [K]	$T_{tv} \sim 500$	$T_{dv} \sim 1200$

It is important to note the asymmetry of the valence and conduction band tails. This asymmetry is caused by the fact that the conduction band edge is made of s -like states while the valence band edge is made up of p -like states. Since the bonding disorder influences the p states more than the s states, the valence band exhibits a wider band tail than the conduction band. This asymmetric distribution of DOS bends the Fermi energy (E_F) of intrinsic a-Si:H slightly towards the conduction band, giving a-Si:H material slight n -type characteristics [15].

2.1.3 Trapped and Free Carrier Densities

The DOS distribution presented provides the means of expressing the trapped and free charge densities, which in turn aid in the concept development of the dispersive transport. The density of trapped and free electrons can be obtained as a function of E_F by integrating the product of DOS and the probability of electron occupancy $f(E)$ over the mobility gap.

$$n_t = \int_{E_V}^{E_C} g_A(E) f(E) dE \quad (2.3)$$

$$n_f = \int_{E_C}^{+\infty} g_A(E) f(E) dE \quad (2.4)$$

where n_t and n_f are the densities of the trapped and free electrons, respectively. In the same fashion, the density of the holes can be found by

$$p_t = \int_{E_V}^{E_C} g_D(E) [1 - f(E)] dE \quad (2.5)$$

$$p_f = \int_{-\infty}^{E_v} g_D(E)[1 - f(E)]dE \quad (2.6)$$

p_t and p_f are the densities of trapped and free holes, respectively. In dynamic equilibrium, the probability of electron occupancy is described by the Fermi-Dirac function,

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{k_B T}\right)} \quad (2.7)$$

Under non-equilibrium conditions, the occupation function depends on both the electron and hole concentrations [31]. The solutions for Equation (2.3) and (2.5) can be computed numerically or approximated as a sum of exponentials with the assumption that E_F moves no closer than a few $k_B T$ from the mobility edge; the assumption is valid by virtue of the high density of tail states that tends to constrain the Fermi level movement for a broad range of bias voltages. The trapped electron density in localized states is well approximated by:

$$n_t(E_F) = N_{tc} \exp\left(\frac{E_F - E_C}{k_B T_{tc}}\right) + N_{dc} \exp\left(\frac{E_F - E_C}{k_B T_{dc}}\right) \quad (2.8)$$

Here, N_{tc} and N_{dc} are the total densities of the tail and deep states, respectively. The typical parameter values for Equation (2.8) are shown in Table 2–3. The density of electrons excited to the conduction band is

$$n_f(E_F) = N_C \exp\left(\frac{E_F - E_C}{k_B T}\right) \quad (2.9)$$

where N_C is the effective density of states of the band and is estimated to be $\sim 10^{21} \text{cm}^{-3} \text{eV}^{-1}$ [32]. The asymmetry of DOS in the mobility gap, discussed in Section 2.1.2, renders the electron mobility much higher than the hole mobility. Consequently, electrons are the dominant carriers in intrinsic a-Si:H.

Table 2-3: Typical values of the characteristic parameters for trapped electron density at $T=300\text{K}$ (compiled from [30]).

Parameters	Tail States	Deep States
Carrier Density at E_C [cm^{-3}]	$N_{tc} \sim 1 \times 10^{21}$	$N_{dc} \sim 5 \times 10^{18}$
Characteristic Temperature [K]	$T_{tc} \sim 350$	$T_{dc} \sim 800$

2.1.4 Carrier Transport in a-Si:H

Electronic transports in a-Si:H is partitioned into three regions [15]: extended states conduction, band tail conduction, and hopping conduction at E_F .

Extended states conduction is due to the thermal activation of carriers from E_F to above the mobility edge. Electrons in the extended states can move freely with finite mobility. The activation energy is the separation between E_F and mobility edge, which is $\sim 1.0\text{eV}$ for intrinsic a-Si:H. Since the carriers are thermally activated, extended states conduction vanishes at low temperatures. The conductivity for extended states follows the relation

$$\sigma_{ext} = \sigma_{oe} \exp\left(-\frac{E_C - E_F}{k_B T}\right) \quad (2.10)$$

σ_{oe} is the average conductivity above the mobility edge ($\sim 100\text{S/cm}$). Carriers excited to the localized states in the band tail transport via hopping conduction at elevated temperatures. Hopping conduction in the band tail is given by

$$\sigma_{tail} = \sigma_{ot} \exp\left(-\frac{E_{CT} - E_F}{k_B T}\right) \quad (2.11)$$

where E_{CT} is the average energy of the conduction path, and σ_{ot} is an exponent prefactor that is generally much smaller than σ_{oe} . Hopping conduction at E_F occurs when the DOS is large enough for significant tunnelling of electrons, analogous to impurity conduction in heavily doped c-Si. This mechanism can be described by

$$\sigma_{hop} = \sigma_{oh} \exp\left(-\frac{W}{k_B T}\right) \quad (2.12)$$

where W is the hopping energy, and σ_{oh} is the hopping prefactor usually in the range of $10^{-1}-10^{-2}\text{S/cm}$. This transport mechanism dominates at very low temperatures [15].

Carrier mobility is an alternative measure of the conductivity related through

$$\sigma(E_F) = qg(E_F)\mu(E_F)k_B T \quad (2.13)$$

Due to the high density of tail states in a-Si:H, the frequent trapping and releasing of carriers lead to dispersive transport in the band tails. As a

result, the effective carrier mobility is lower than the free carrier mobility (μ_o). The effective carrier mobility, also termed the drift mobility (μ_d), can be measured from the time-of-flight experiment [32]. The drift mobility can be expressed as a fraction of the free carrier mobility where the fraction is dictated by the time the carrier spends in the traps

$$\mu_d = \mu_o \frac{n_f}{n_f + n_t} \quad (2.14)$$

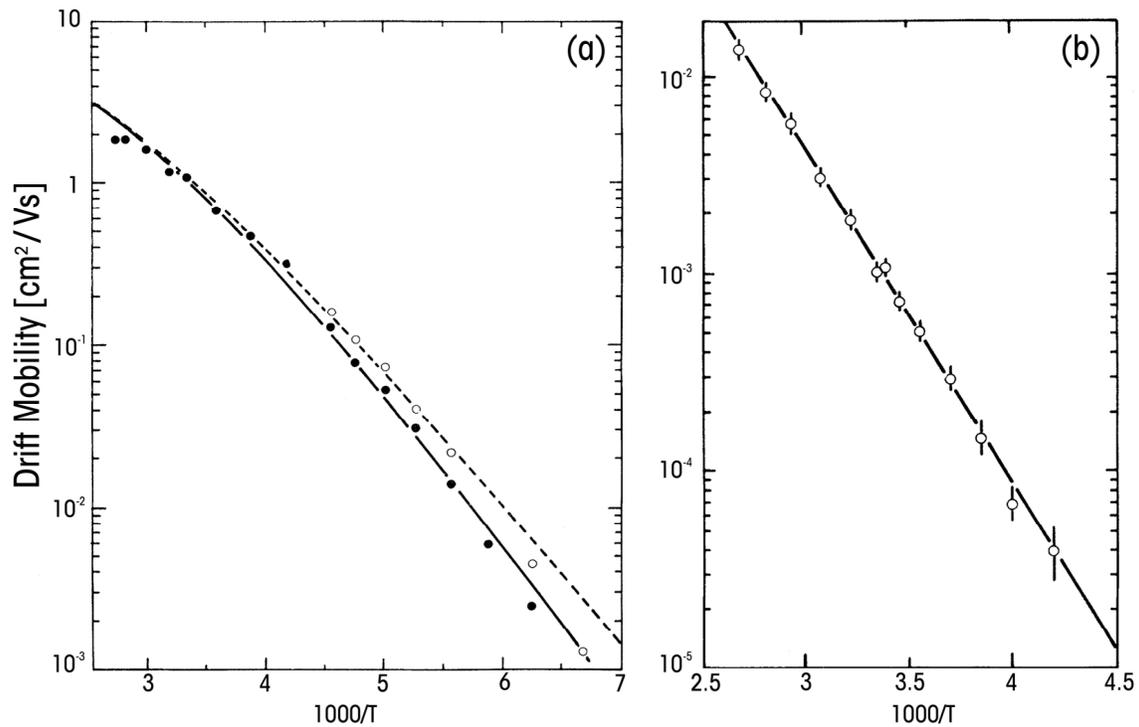


Figure 2-5: Drift mobility data for electrons (a) and holes (b). The electron data are measured for electric field strengths of 1×10^4 V/cm (solid circles) and 2×10^4 V/cm (hollow circles). The hole drift mobility data are measured for electric field strength of 5.8×10^4 V/cm [33].

Figure 2–5 shows the measured drift mobilities of intrinsic a–Si:H [33]; the hole mobility is almost two orders of magnitude lower than the electron mobility due to enhanced dispersive transport in the wider valence band tails.

2.1.5 Optical Properties of a–Si:H

The absorption of photons in intrinsic a–Si:H has pivotal implications in determining the performance of the a–Si:H photodiodes. This is quantified through the specification of its optical absorption coefficient. Optical absorption coefficient (α) provides the fractional loss in intensity per unit depth into the material and is governed by the relationship

$$\frac{dI(z)}{dz} = -\alpha I(z) \quad (2.15)$$

$I(z)$ is the intensity of the beam defined as the optical power per unit area, and z is the depth from the surface of a–Si:H where z is zero. The solution to equation (2.15) is

$$I(z) = I_o \exp(-\alpha z) \quad (2.16)$$

where I_o is the optical intensity at the surface ($z=0$). The optical absorption can be classified into three regions [34] depending on the energy of the photon ($\hbar\omega$). In the high energy regime, transitions of charge carriers take place between the extended states across the forbidden gap. For photon energy equal or below the optical band gap energy, the absorption is dominated by transitions of carriers either from the localized states of the

valence band across the band gap into the extended states of the conduction band, or from the extended states of the valence band across the gap into the localized states of the conduction band [35]. In this region, $\alpha(E)$ follows an exponential described by

$$\alpha(\hbar\omega) = \alpha_o \exp\left(\frac{\hbar\omega - E_g}{E_o}\right) \quad (2.17)$$

where E_g is the optical band gap and E_o is the Urbach energy typically in the range of 50–100meV. The optical band gap is an extrapolation of the Urbach edge in Tauc plots and typically falls in range of 1.7–1.8eV. The optical band gap of a-Si:H is generally smaller than the mobility gap. At even lower photon energies, absorption takes place through the deep defect states located in the middle of the gap as shown in Figure 2–3. This absorption region is generally characterized by a plateau in the absorption coefficient between ~0.9eV and ~1.2eV. The absorption coefficient of intrinsic a-Si:H as a function of photon energy is shown in Figure 2–6 [36].

Aligning with the bio-assay application specification, if the common green Cy3 fluorescent dye is used to tag the samples, they would emit maximally around 550nm; that is 2.2eV ($E_{ph} = \hbar\omega \approx 1240/\lambda_{nm}[\text{eV}]$). Near room temperature, this energy corresponds to an absorption coefficient around $2 \times 10^4 \text{cm}^{-1}$. The absorption depth (δ), defined as α^{-1} , is approximately 500nm. This value has important implications when designing the a-Si:H *n-i-p* photodiode where the thickness of the intrinsic layer, the region where the photons are converted to electrical carriers, is chosen.

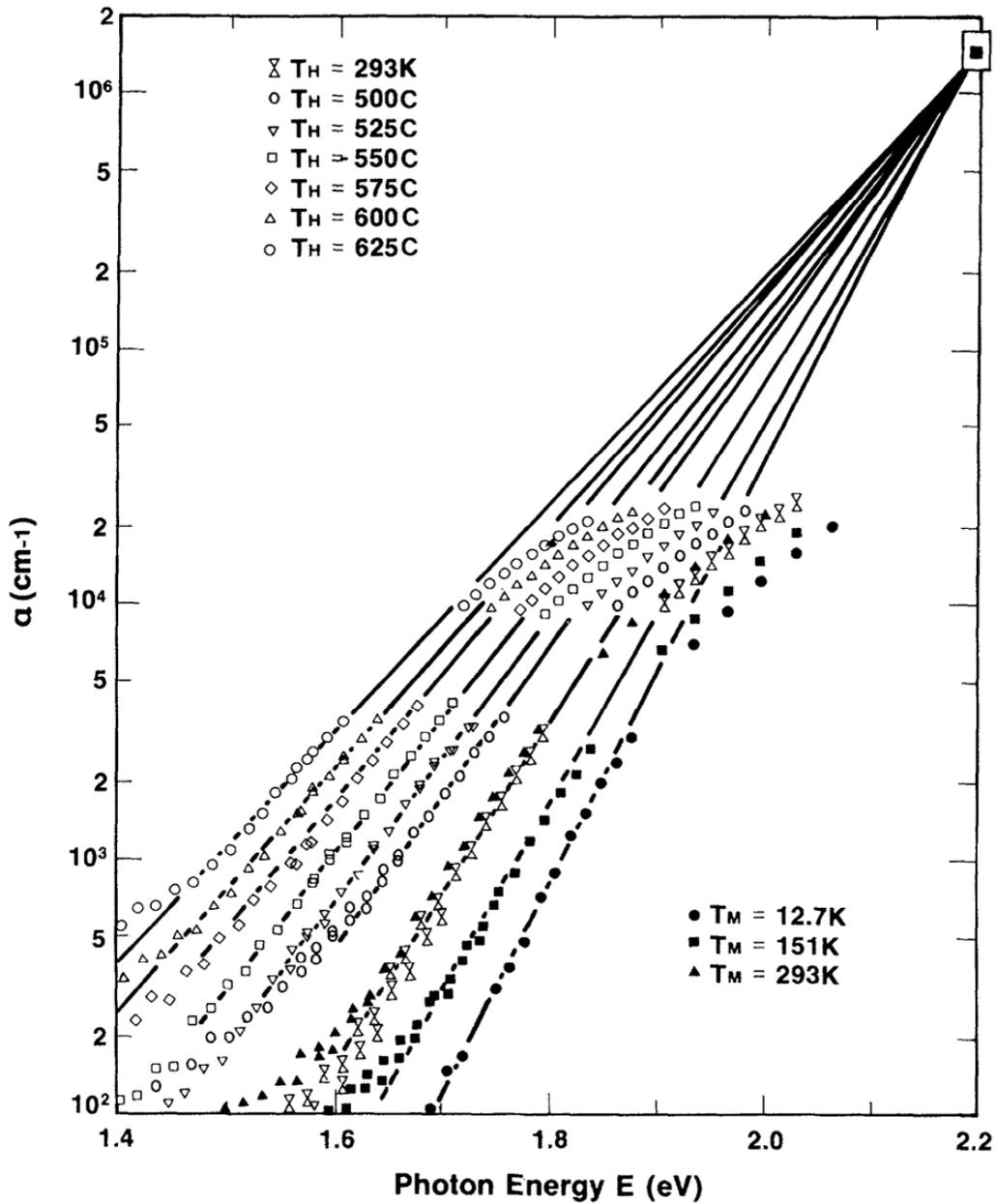


Figure 2-6: Absorption coefficient of intrinsic a-Si:H as a function of the photon energy. Solid symbols refer to data obtained at different measurement temperatures while hollow symbols refer to film that has been isochronally heated to introduce structural disorder [36].

Photoconductivity occurs when carriers are optically excited from non-conducting states to conducting states. This is marked by an increase in conductivity. There are two types of photoconductivity noted as primary and secondary photoconductivity [15]. For primary photoconductivity, the only current contribution in the device is from the optically excited carriers achieved with blocking contacts. Secondary photoconductivity occurs when the electrons and holes that are absorbed at the contacts are replaced by carriers injected from the other contact.

The primary photocurrent of thin a-Si:H sample is

$$I_{ph} = \eta_g \eta_c \varphi_{ph} \quad (2.18)$$

Here, φ_{ph} is the photon flux. η_g is the quantum efficiency for generating mobile holes and electrons. Since experiments suggest that there is no geminate recombination in a-Si:H at room temperature [37], η_g is usually close to unity [15]. η_c is the charge collection efficiency and its value approaches unity when deep trapping time is longer than the carrier transit time. The secondary photoconductivity is given by

$$\sigma_{ph} = q\varphi_{ph} (\mu_{de}\tau_e + \mu_{dh}\tau_h) \approx \varphi_{ph} q\mu_{de}\tau_e \quad (2.19)$$

where $\mu_{de}\tau_e$ and $\mu_{dh}\tau_h$ are the mobility-lifetime products of electrons and holes, respectively. The approximation is made under the assumption that the transport in a-Si:H thin-film is dominated by electrons, evident in Figure 2–5.

2.1.6 *Metastability and Defect Creation*

Discussions of the electronic properties conclude with the metastability phenomenon inherent in even the best quality a-Si:H. When a-Si:H is placed under stress such as prolonged illumination or voltage biases, reversible changes occur in the DOS within the energy gap. Defects are created in a-Si:H whenever the quasi-Fermi level is shifted from the equilibrium point. Introduction of these defects reduce the carrier lifetimes and affect the electrical characteristics. Recovery of the defects creation can usually be achieved by annealing the material above 150°C.

Such phenomenon is best demonstrated through either the Staebler-Wronski effect [38] or threshold voltage (V_T) shift in a-Si:H TFTs [39]. The physics of defect states creation and removal processes are based on the breaking of weak Si-Si bonds to form Si dangling bonds [40], [41]. With such weak bonds broken, the new Si dangling bond must be resolved into stability; otherwise, adjacent Si dangling bonds would form another Si-Si bond. It has been proposed that some of the hydrogen motion is involved in the kinetics and stabilization of the metastable defects [42]. Evidence supporting the involvement of hydrogen in the metastable changes of a-Si:H is justified through a number of observations [43]–[47].

The diffusion-mediated metastable changes suggest that hydrogen bonded to Si is either released interstitially with subsequent trapping, or reallocated from one Si atom to another to create and anneal dangling bonds [43]. Consequently, there is a time dependence of the defect

creation process which is determined through the diffusion of hydrogen atoms towards these defect formation sites [44]. The hydrogen atom must leave the Si–H bond to occupy a transport state before bonding to another Si–H bond. These transport states can be an unbonded hydrogen interstitial state, a state in which two hydrogen atoms are paired, or a state in which the hydrogen atom is partially attached to the silicon atom before bonding to another [15]. The hydrogen diffusion process has been found to be dispersive in nature where the diffusion coefficient is time-dependent [44]. This accounts for the stretched exponential decay of excess carriers in doped a–Si:H [45], the annealing of light induced defects [46], and carrier-induced creation of defects [47]. The stretched exponential behaviour suggests that there is a near exponential energy barrier for the creation and annealing processes.

The threshold voltage shift of a–Si:H TFTs may be an important issue if they are used in electronic backplane drivers; however, clever circuit design techniques can be employed for compensation. Metastability phenomena may also manifest itself as a time-dependent reverse current for a–Si:H detectors, which ultimately limits its sensitivity. In views of the specifications for fluorescence-based bio-assay application presented in Section 1.3.2, the light-induced defects creation of such faint signals does not place serious constraints on the employment a–Si:H photodiodes; although, such phenomenon is evident during the characterization and measurements of the fabricated sensors.

2.2 *a-Si:H n-i-p Photodiodes*

The discussion on the electronic properties of *a-Si:H* paves the way for the understandings of *a-Si:H* photodiodes. This section presents the current technology and physics of *a-Si:H n-i-p* photodiodes used as the underlying assay sensor for this research work.

Amorphous silicon *n-i-p* photodiodes have high quantum efficiency and low reverse bias leakage current, which renders them as the preferred photosensor structure for high-sensitivity imaging applications compared to other commonly studied structures such as *metal-insulator-semiconductor* (MIS) and Schottky photodiodes [48]. Figure 2-7 shows the general device structures for both *a-Si:H n-i-p* and *p-i-n* photodiodes.

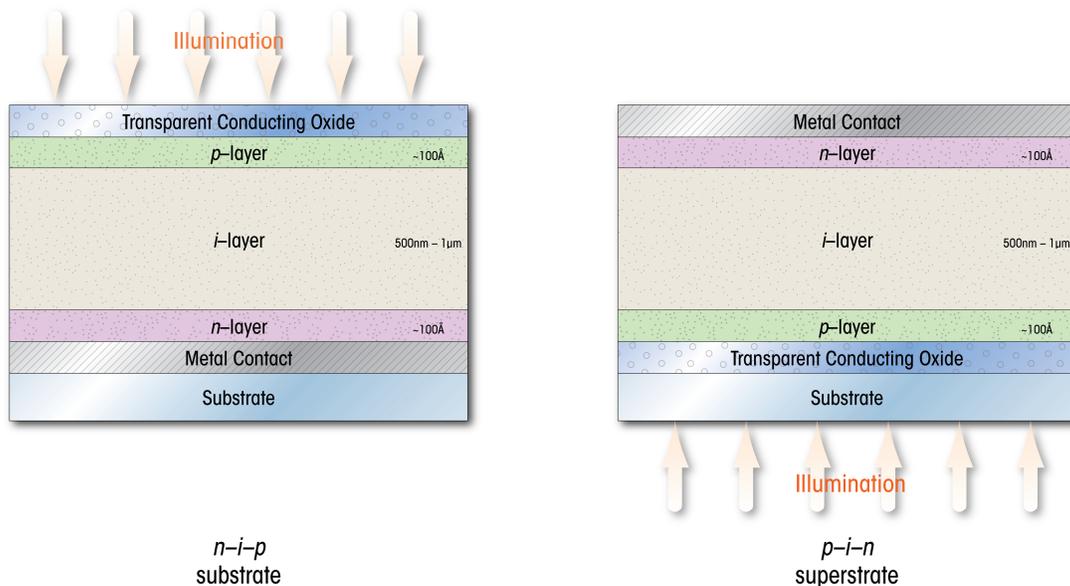


Figure 2-7: Illustration of the cross-sectional diagram for *n-i-p* and *p-i-n* photodiodes. Depending on the intended illumination direction, the photodiodes are referred to as superstrate and substrate structures.

The letters n , i , and p represents the deposition order of n -doped, intrinsic, and p -doped layers, respectively.

2.2.1 Principle of Operation

Despite of the fundamental differences between a-Si:H and c-Si photodiodes, their dark *current-voltage* (I_D - V) characteristics look similar. Figure 2-8a shows the typical electrical characteristic of a-Si:H p - i - n photodiodes. The reverse current increases by orders of magnitude under illumination favouring the photon conversion mode performed while photodiodes are placed under reverse biases. The magnitude of the illumination signal is usually taken as the difference between the total current under illumination to that of the dark conditions. During photovoltaic operations, a-Si:H n - i - p photodiodes are placed in reverse bias with the cathode of the diode connected to a relatively positive potential source and the anode of the diode connected to a relatively negative potential. Usually, the strength of the built-in potential (V_{bi}) only yields partial depletion of the i -layer. The enhanced *electric field* (E-field) caused by the reverse bias results in full depletion of the i -layer.

As shown in Figure 2-8b, the *electron-hole pairs* (EHP) generated due to impinging photons are separated and swept by the internal electric field in opposite directions. Depending on the external electrical connection, these photogenerated carriers are either stored in the internal junction capacitance of the photodiode (C_j) for delayed readout or appear as photocurrent (I_{ph}).

The photocurrent can be calculated by

$$I_{ph} = \varphi_{ph} \eta_{qe}(V, \lambda) \quad (2.20)$$

$\eta_{qe}(V, \lambda)$ is the external quantum efficiency, which includes the wavelength-dependent absorption that generates the EHP and bias-dependent charge collection efficiency. The mean free path (d) of the carriers is given by

$$d = \mu_d \tau \xi \quad (2.21)$$

where ξ is the electric field and τ is the recombination lifetime. Smaller τ translates to a higher trapping probability and hence a lower collection efficiency. Higher collection efficiency is achieved with higher applied bias as well as larger $\mu\tau$ product. Typically, $\mu_{de}\tau = 3 \times 10^{-7} \text{cm}^2/\text{V}$ and $\mu_{dh}\tau = 5 \times 10^{-8} \text{cm}^2/\text{V}$ for low defect density a-Si:H [15].

It is worth noting that for both types of photodiodes shown in Figure 2-7, it is preferred to have the illumination shone through the p -type contact. This illumination scheme is used to achieve better carrier collection efficiency by reducing the distance travelled by the photogenerated holes, which have much lower mobility than that of electrons. The thicknesses of the n - and p -layers are only on the order of a few hundred angstroms. The i -layer, which acts as the principal absorption layer, has a thickness of few hundred nano-meters. This thickness is much less than the average required for c-Si photodiode due to the high optical absorption coefficient of a-Si:H. The n - and p -layers are not used for absorption due to very high defect densities in doped a-Si:H. The high defect densities lead to

very small minority carrier lifetimes. The strong built-in field across the thin i -layer in $n-i-p$ photodiodes helps to separate the photogenerated carriers so that they can be collected at their corresponding contacts. This field-assisted separation is critical since practically, even for device quality a -Si:H, the carrier diffusion length is shorter than the thickness of the i -layer.

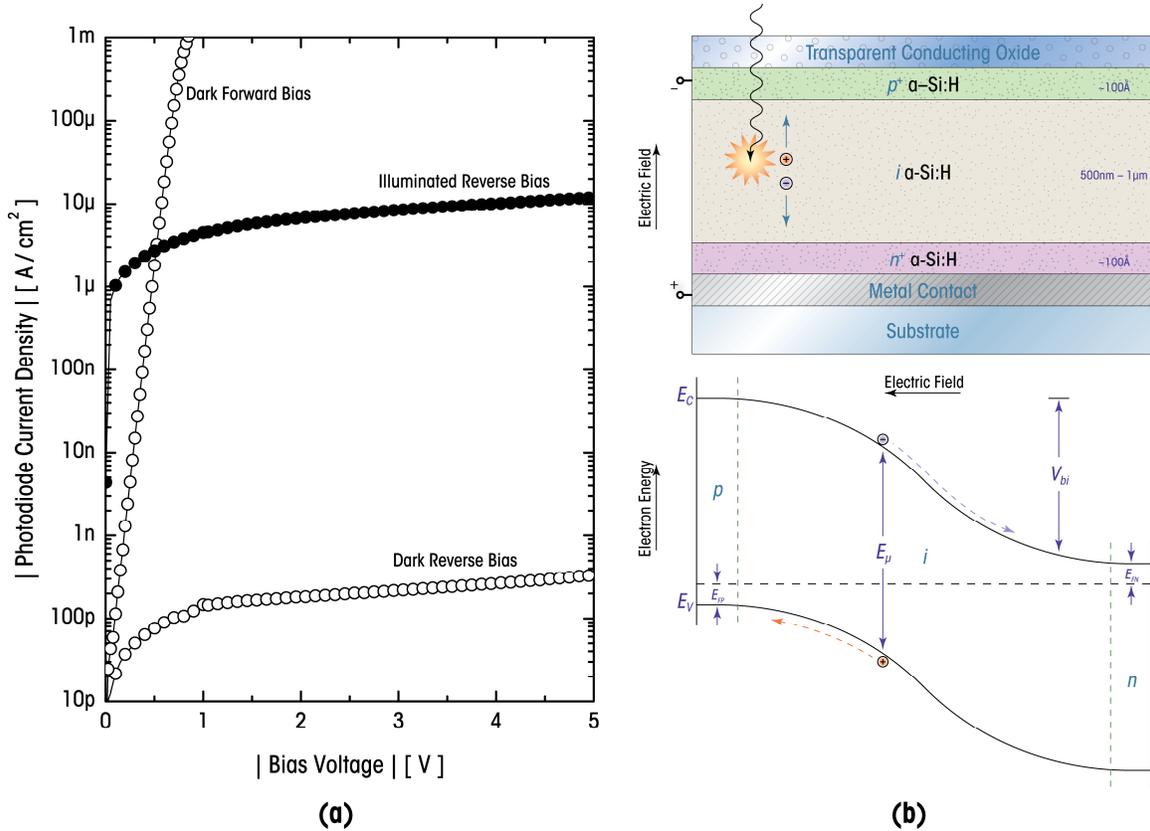


Figure 2-8: (a) Typical current-voltage characteristics of a -Si:H $n-i-p$ photodiodes. In reverse biases, the diode current increases by orders of magnitude with illumination. (b) the structure and band diagram of typical a -Si:H $n-i-p$ photodiodes illustrating the generated electron-hole pair with incident photons.

2.2.2 Quasi-static Dark Current–Voltage Characteristics

The energy band diagram of the i -layer for an a-Si:H n - i - p photodiodes under thermodynamic equilibrium is illustrated in Figure 2–9. The potential drop across the bulk of the i -layer (V_i) is the build-in potential (V_{bi}) reduced by the presence of potential barriers V_p and V_n . The heights of these potential barriers are determined by the space charge in the i -layer, which originates from the trapped carriers in the defect states. The exact magnitude of V_p and V_n are difficult to determine as the densities and distributions of the trapped charges are complex functions of carrier density, energy distribution of the defect states, and positions of the quasi-Fermi levels.

For the case of uniform distribution of defect states across the i -layer, more electrons are trapped in the region close to the n contact where the electron concentration (n_o) is the highest; similarly, more holes are trapped in the region close to the p contact where the hole concentration (p_o) is the highest. The space charge density is lower in the middle of the i -layer where both carrier concentrations are low. Consequently, a-Si:H i -layer with relatively low defect densities confines the relatively low V_p and V_n potential barriers to regions close to the contacts, leaving an approximately uniform E-field distribution across the bulk of the i -layer. Typically, one would expect higher defect density in the region close to the contacts than those near the middle of the i -layer. With optimized processes however, the densities of defect states can be relatively homogeneous across the i -layer [50].

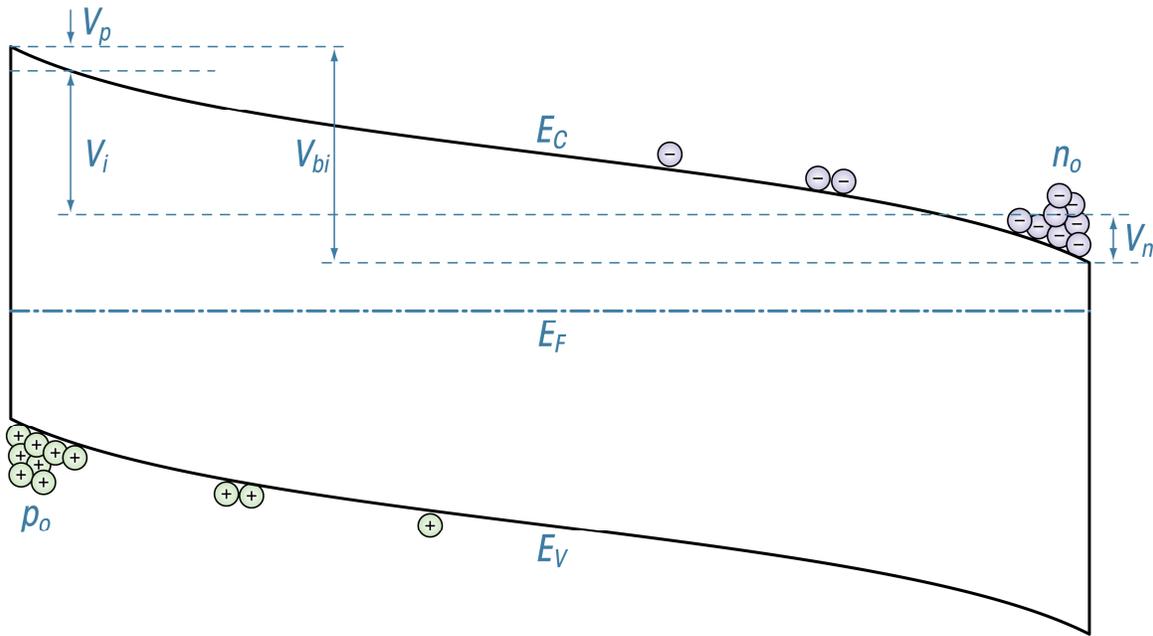


Figure 2-9: Energy band diagram of the *i*-layer in a-Si:H *n-i-p* photodiodes under thermodynamic equilibrium condition; adopted from [49].

Forward Bias Characteristics

Even though a-Si:H *n-i-p* photodiodes are placed under reverse bias during photon detections, carrier recombination through carrier injection obtained under dark forward biases provide a means of probing the defect states in the *i*-layer [49]. Furthermore, forward characteristics are important if the diodes are used as switching elements in sensor arrays where the switching performance depends partially on the forward characteristics [51].

Figure 2-10 shows a typical forward characteristics of a-Si:H photodiode. Under forward bias conditions, excess electrons and holes are injected into the bulk *i*-layer from the contacts. The carrier recombination through defect states is described by the *Shockley-Read-Hall* (SRH) recombination

mechanism [52] which leads to an exponential dependence of photodiode current on its applied voltage. The recombination rate is directly related to the electron and hole quasi-Fermi levels, E_{Fn} and E_{Fp} . As shown in Figure 2-11, E_{Fn} and E_{Fp} are spliced by the applied bias (V_a).

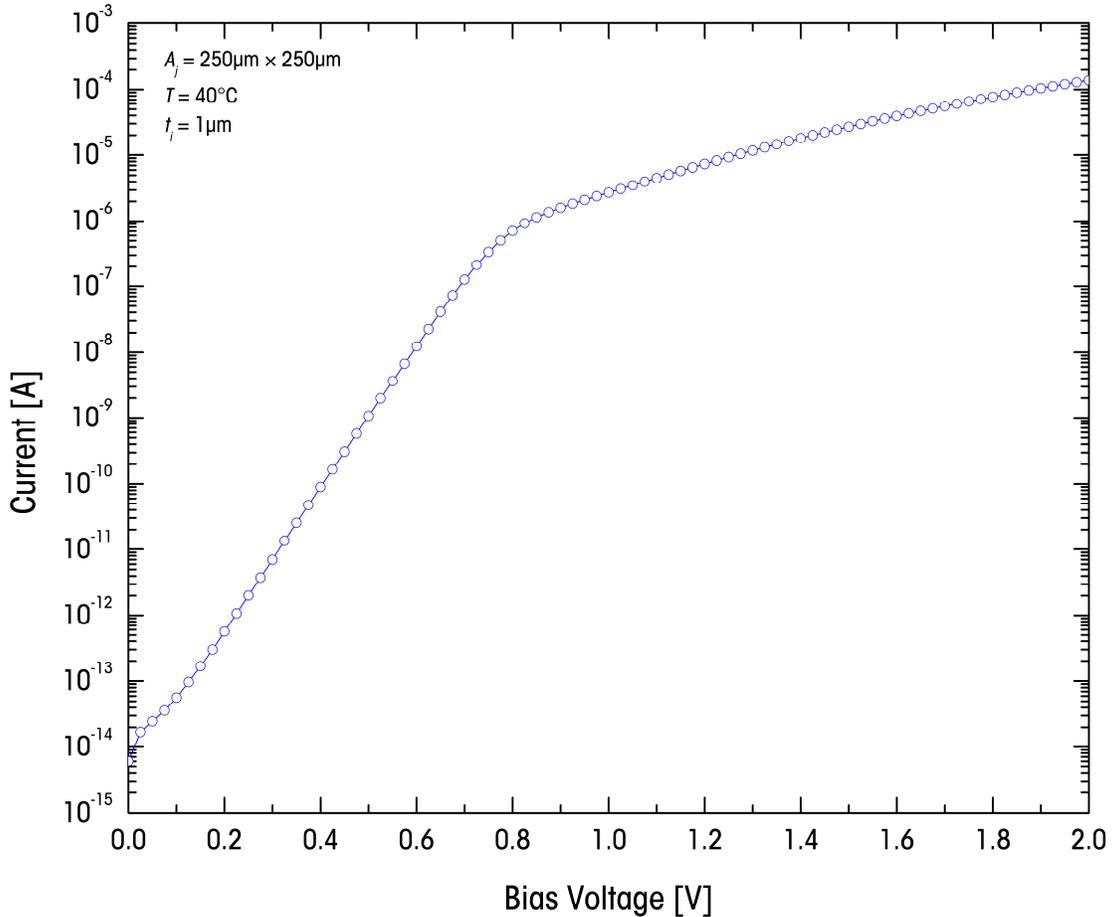


Figure 2-10: Measured forward I_D - V characteristics of a $250 \times 250 \mu\text{m}^2$ a-Si:H $n-i-p$ photodiode operated at 40°C . The forward characteristic distinctly shows two different carrier transport regimes.

The quasi-Fermi levels not only determine the concentrations of electrons and holes, but also dictate the number of recombination centers. The

effective recombination center consists of defects lying only between the two quasi-Fermi levels [53]. Evident in Figure 2-10, the forward characteristics can be demarcated into two main regimes. The differences in the two regimes are due to the dissimilar carrier transport mechanisms [54]–[55].

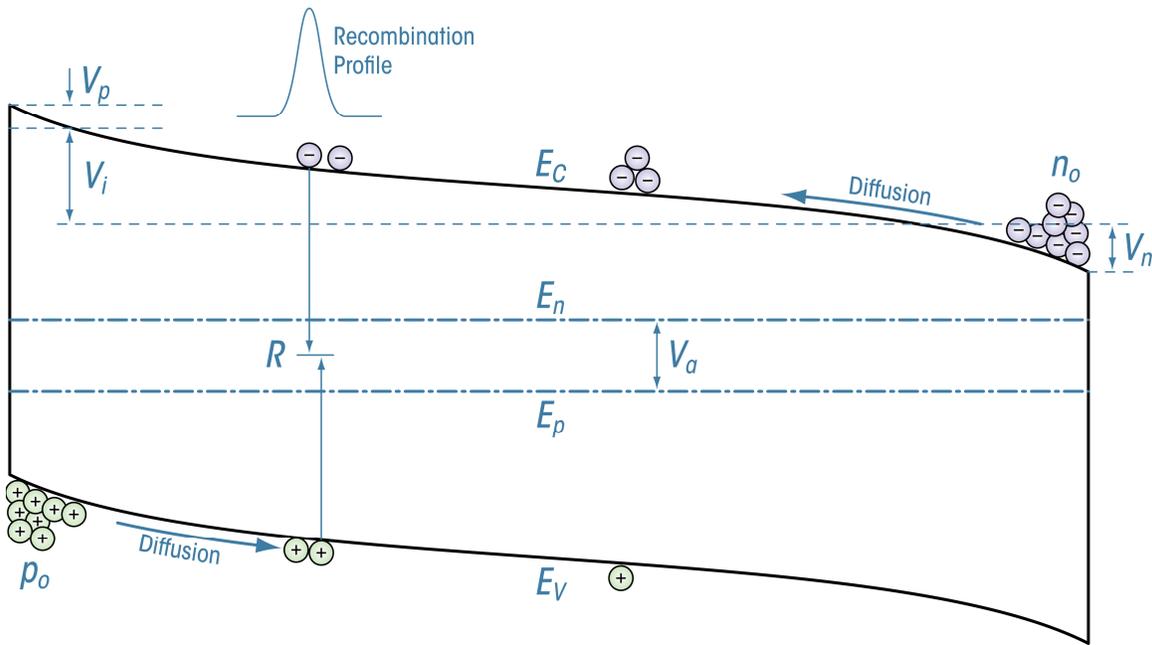


Figure 2-11: Energy band diagram of the *i*-layer in a-Si:H *n-i-p* photodiode under low forward bias condition; adopted from [49].

The forward current increases exponentially at low voltage biases, dominated by the diffusion and subsequent recombination of excess carriers injected into the *i*-layer from the *n* and *p* contacts. At high biases, current increases at a much slower rate via power-law relationship. The current flow changes from diffusion and recombination to carrier injection limited and drift-driven transport. Figure 2-11 shows the energy band diagram of the *i*-layer under low forward bias conditions. In this

exponential regime, the I_D - V characteristics are either characterized with the classic diode ideality factor (n) with values between 1 and 2 [56], or a voltage dependent differential ideality factor, $n(V)$ [49]. Carriers that diffuse over the potential barrier and recombine in the doped layers yield quality factors close to unity, while carriers that recombine in the i -layer via SRH process give quality factors near 2. Investigation through numerical methods indicates that the total current is dominated by the recombination in the i -layer and that there is very little contribution of the diffusion current [57]. The carrier recombination occurs both in the bulk i -layer as well as at the n - i and i - p interfaces. In the case where recombination occurs at the i - p interface, the concentration of holes adjacent to the p -layer is much greater than that of the electrons, which render electrons the minority carriers there. Therefore, the recombination rate is determined by the electron concentration at the i - p interface. Likewise, the recombination rate at the n - i interface is determined by the minority hole concentration there. In the case of recombination in the bulk i -layer, electrons and holes recombine through the defect states lying between E_{Fp} and E_{Fn} , as shown in Figure 2-11. The two quasi-Fermi levels are essentially constant across the i -layer in high quality a-Si:H materials with their separation equal to V_a . The total recombination current is obtained by integrating across the thickness of the i -layer (t_i) and the states across the energy gap [49], [53], [57],

$$J_D \propto \int_0^{t_i} \left[\frac{rnp}{rn + p} \int_{E_{Fp}}^{E_{Fn}} g(E) dE \right] dz \quad (2.22)$$

J_D is the dark current density and r is the ratio of electron and hole capture cross sections. Due to variations in the positions of E_{Fn} and E_{Fp} relative to E_C and E_V , respectively across the i -layer, n and p also vary with the position of the i -layer. The np products however, remain essentially constant according to,

$$np \approx n_i^2 \exp\left(\frac{qV_a}{k_B T}\right) \quad (2.23)$$

The SRH term, $rn p / rn + p$, is maximum when $rn + p$ is at minimum; this occurs in the i -layer where $rn = p$ [57]. The SRH term tails off rapidly at locations away from the maximum as shown in Figure 2-11. Consequently, the bulk recombination is confined to a relatively narrow region of the i -layer. Although the $g(E)$ integral between E_{Fp} and E_{Fn} depends on the location of the i -layer, it does not vary as rapidly as the SRH term. Therefore, the integral of $g(E)$ can be approximated as constant evaluated at z_o where SRH is maximum. This leads to

$$J_D \propto \int_0^{t_i} \frac{Rnp}{Rn + p} dz \left(\int_{E_{Fp}}^{E_{Fn}} g(E) dE \right)_{z=z_o} \quad (2.24)$$

The resulting integral can be evaluated with the assumption that the local electric field around z_o (E_o) is constant [57]:

$$J_D \propto \frac{1}{E_o} \exp\left(-\frac{E_g}{2k_B T}\right) \exp\left(\frac{qV_a}{2k_B T}\right) \left(\int_{E_{Fp}}^{E_{Fn}} g(E) dE \right)_{z=z_o} \quad (2.25)$$

Equation (2.25) shows that there are two major contributions to the current increase with applied voltage. The first contribution, $\exp(qV_a/2k_bT)$, comes from the increase of the carrier concentration by carrier injection from the n and p contacts, which for recombination through a single defect level results in the classic diode ideality factor 2. The second contribution, in the form of an integral, is due to the increase in the number of defect states that contributes to the recombination process with increase in applied bias. In the case of a purely exponential distribution of gap states, the J_D - V characteristics merge in the form [57]

$$J_D \propto \exp\left(\frac{qV_a}{nk_bT}\right) \quad (2.26)$$

with constant n valued between 1 and 2. High quality a-Si:H n - i - p photodiodes possess such DOS distributions in its i -layer as discussed in Section 2.1.2. However, in more general cases, the DOS distribution in the energy gap is more complex; therefore, the I_D - V relationship can no longer be described by a voltage independent ideality factor, but instead [49]

$$n(V) = \frac{q}{k_bT} \left(\frac{d \ln J_D}{dV} \right)^{-1}. \quad (2.27)$$

Reverse Bias Characteristics

The reverse bias dark current level of a-Si:H n - i - p photodiode is arguably one of the most important parameters that dictates the performance of a sensor. Decreasing the dark current level improves the sensitivity and

dynamic range of the sensor, which facilitate the detection of faint signals with low photon flux. It is for this reason that the origin and optimization of reverse dark current level for a-Si:H *p-i-n* and *n-i-p* photodiodes have been actively studied since its initial conception. This merit is especially important for the fluorescence-based assay applications for its heightened requirement in sensitivity.

Table 2-4 shows a compilation of reported reverse dark current density (J_D) values for a-Si:H *p-i-n* and *n-i-p* photodiodes deposited via PECVD [56], [58]–[70]. The fundamental lower limit of the dark current level in a-Si:H *n-i-p* photodiodes is determined by the thermally-induced carrier emission from deep levels in the bulk a-Si:H layer [71]. Additional sources that increase the dark current level may include emissions of carriers from defect states at the *i-p* and *n-i* interfaces [58], [63], [72], contact injection [61], edge leakage [62], and macrostructural shunt paths [73].

Macrostructural shunt paths can be caused by contaminations and imperfections with photolithography masks used extensively during the fabrication process. Quality of the contact materials can also be important; the average distance between point defect distributions, for example, is larger for tin oxide (SnO_2) than zinc oxide (ZnO). Section 3.1.2 discusses such issues in more detail. Generally, photodiodes with areas greater than 20mm^2 are more prone to this source and the increase in reverse current can be catastrophic. The contribution of this source towards the total leakage current diminishes for small photodiodes fabricated with optimized processes.

Table 2-4: A summary of reported reverse dark current levels for a-Si:H $p-i-n$ and $n-i-p$ photodiodes, listed in chronological order [56], [58]–[70]. Results for both segmented and non-segmented structures are presented.

Source	Descriptions	$J_D @ V_a$ [A/cm ²]
McMahon et. al. [58]	<ul style="list-style-type: none"> ▪ 1984 ▪ segmented a-Si:H $p-i-n$ ▪ at -1V ▪ room temperature 	$\sim 4 \times 10^{-10}$
Matsuura et. al. [56]	<ul style="list-style-type: none"> ▪ 1985 ▪ segmented a-Si:H $p-i-n$ ▪ at -1V ▪ room temperature 	$\sim 1 \times 10^{-10}$
Street [59]	<ul style="list-style-type: none"> ▪ 1991 ▪ segmented a-Si:H $p-i-n$ ▪ at -2V ▪ room temperature 	$\sim 3 \times 10^{-11}$
Kramer et. al. [60]	<ul style="list-style-type: none"> ▪ 1994 ▪ segmented a-Si:H $p-i-n$ ▪ at -5V ▪ 30°C 	$\sim 2 \times 10^{-11}$
Chevrier et. al. [61]	<ul style="list-style-type: none"> ▪ 1994 ▪ segmented a-Si:H $p-i-n$ ▪ at -5V ▪ room temperature 	$\sim 1 \times 10^{-9}$
Schiff et. al. [62]	<ul style="list-style-type: none"> ▪ 1996 ▪ segmented a-Si:H $n-i-p$ ▪ -2V ▪ room temperature 	$\sim 1 \times 10^{-10}$
Morrison et. al. [63]	<ul style="list-style-type: none"> ▪ 2002 ▪ segmented a-Si:H $n-i-p$ and $p-i-n$ ▪ room temperature 	$\sim 2 \times 10^{-11}$
Tchakarov et. al. [64]	<ul style="list-style-type: none"> ▪ 2003 ▪ segmented a-Si:H $p-i-n$ ▪ at -2V ▪ room temperature 	$\sim 2 \times 10^{-11}$
Mulato et. al. [65]	<ul style="list-style-type: none"> ▪ 2003 ▪ segmented a-Si:H $n-i-p$ 	$\sim 2 \times 10^{-10}$

	<ul style="list-style-type: none"> ▪ at -1V ▪ room temperature 	
Theil [66]	<ul style="list-style-type: none"> ▪ 2003 ▪ non-segmented a-Si:H <i>p-i-n</i> ▪ at 5V/μm ▪ room temperature 	$\sim 2 \times 10^{-11}$
Wyrsh et. al. [67]	<ul style="list-style-type: none"> ▪ 2003 ▪ non-segmented a-Si:H <i>p-i-n</i> ▪ at -1V ▪ room temperature 	$\sim 2 \times 10^{-12}$
Servati et. al. [68]	<ul style="list-style-type: none"> ▪ 2004 ▪ segmented a-Si:H <i>n-i-p</i> ▪ at -1V ▪ room temperature 	$\sim 1 \times 10^{-11}$
Tchakarov et. al. [69]	<ul style="list-style-type: none"> ▪ 2004 ▪ segmented a-Si:H <i>p-i-n</i> ▪ at -3V ▪ room temperature 	$\sim 1 \times 10^{-10}$
Chang et. al. [70]	<ul style="list-style-type: none"> ▪ 2004 ▪ segmented a-Si:H <i>n-i-p</i> ▪ at -1V ▪ room temperature 	$\sim 1 \times 10^{-11}$

A significant contribution of the reverse dark current for a-Si:H *n-i-p* photodiodes under 4mm^2 is from the edge leakage component. This arises from the enhanced conduction path along the edges of the photodiode due to band bending and added defects created during dry etching. The magnitude of this contribution is affected by the details of the sensor design and fabrication processes such as etching and passivation. For small photodiodes with areas under $100 \times 100 \mu\text{m}^2$, this contribution usually dominates the reverse dark current level.

For high quality a-Si:H $n-i-p$ photodiodes, the contact injection current component is usually negligible. This source depends greatly on the barrier height of the contacts. Good quality blocking contacts in a-Si:H $n-i-p$ photodiodes renders this source less important than those in Schottky photodiodes. With that said, the quality of the $i-p$ interface is important and plays a critical role in determining the electrical and photovoltaic performance for these types of photodiodes [56], [74]. One key issue is the diffusion of the boron atoms from the p -layer into the first few hundred angstroms of the i -layer. This significantly decreases the carrier lifetime and lowers the electric field strength at the interface.

Ideally, thermal generation current would be the dominant contributor for the reverse leakage current. Thermal generation current arises from carriers excited via deep states in the energy gap of the i -layer to the band edges, and subsequent collection by the depletion field. The process can be described by the SRH formalism where current is the sum of the electron and hole emission rates (dQ_e/dt and dQ_h/dt , respectively),

$$J_{th} = \int_0^{t_i} \left(\frac{dQ_e}{dt} \frac{t_i - z}{t_i} + \frac{dQ_h}{dt} \frac{z}{t_i} \right) dz \quad (2.28)$$

Here, J_{th} is the thermal generation current density, z indicates the distance from the p contact and t_i is the total thickness of the i -layer. The dependence on z is due to the dependence of the displacement current from the excited carrier on the distance it moves during collection [75].

Equation (2.28) assumes that all the excited carriers are collected without significant recombination. Such condition is usually satisfied if

$$\begin{aligned}\lambda_d &< \mu_d \tau \xi_i \\ \lambda_d &< \mu_d \tau \frac{V_i}{t_i} \\ \mu_d \tau &> \frac{t_i^2}{V_i}\end{aligned}\tag{2.29}$$

λ_d is the drift length and ξ_i is the uniform field across the i -layer. For a $t_i = 500\text{nm}$ photodiode biased at -1V , $\mu_d \tau > 2.5 \times 10^{-9} \text{cm}^2/\text{V}$ is required. This condition is easily satisfied as device quality a-Si:H usually have $\mu\tau$ product greater than $10^{-7} \text{cm}^2/\text{V}$ [76], [77].

Equation (2.28) can be solved analytically,

$$J_{th} = \frac{1}{2} \frac{dQ_e}{dt} t_i + \frac{1}{2} \frac{dQ_h}{dt} t_i\tag{2.30}$$

The rate of thermal emission of electrons and holes from a distribution of localized states can be written as

$$\frac{dQ_e}{dt} = \int g(E) f(E, t) \omega_{oe} \exp\left(-\frac{E_C - E}{k_B T}\right) dE\tag{2.31}$$

$$\frac{dQ_h}{dt} = \int g(E) [1 - f(E, t)] \omega_{oh} \exp\left(-\frac{E - E_V}{k_B T}\right) dE\tag{2.32}$$

where ω_{oe} and ω_{oh} are the electron and hole excitation rate prefactors, respectively. The excitation rate prefactors are related to the carrier cross sections by [77]

$$\omega_{oe} = N_C k_B T \sigma_e \nu_f \quad (2.33)$$

$$\omega_{oh} = N_V k_B T \sigma_h \nu_f \quad (2.34)$$

where σ_e is the electron capture cross section, σ_h is the hole capture cross section, and ν_f is the free carrier velocity. In the steady-state condition, the electron and hole excitation rates are equal [78],

$$\frac{dQ_e}{dt} = \frac{dQ_h}{dt} \quad (2.35)$$

Equation (2.30) consequently simplifies to

$$J_{th} = t_i \frac{dQ_e}{dt} = t_i \frac{dQ_h}{dt} \quad (2.36)$$

Equating the electron and hole emission rates shows that the steady-state electron occupancy factor is [75]

$$f(E, \infty) = \frac{1}{1 + \exp\left(2 \frac{E - E_{FD}}{k_B T}\right)} \quad (2.37)$$

E_{FD} is the quasi-Fermi energy describing the occupancy,

$$E_{FD} = \frac{1}{2} E_\mu + \frac{1}{2} k_B T \ln\left(\frac{\omega_{oh}}{\omega_{oe}}\right) \quad (2.38)$$

The difference in the capture cross sections shifts E_{FD} away from the midgap ($\frac{1}{2}E_{\mu}$). Since σ_e/σ_h is the order of 0.1 [71], E_{FD} shift towards E_C by roughly 20–40meV. Figure 2–12 shows an illustration of the DOS indicating the origin of the thermal generation current through gap states as well as annotating various energy levels.

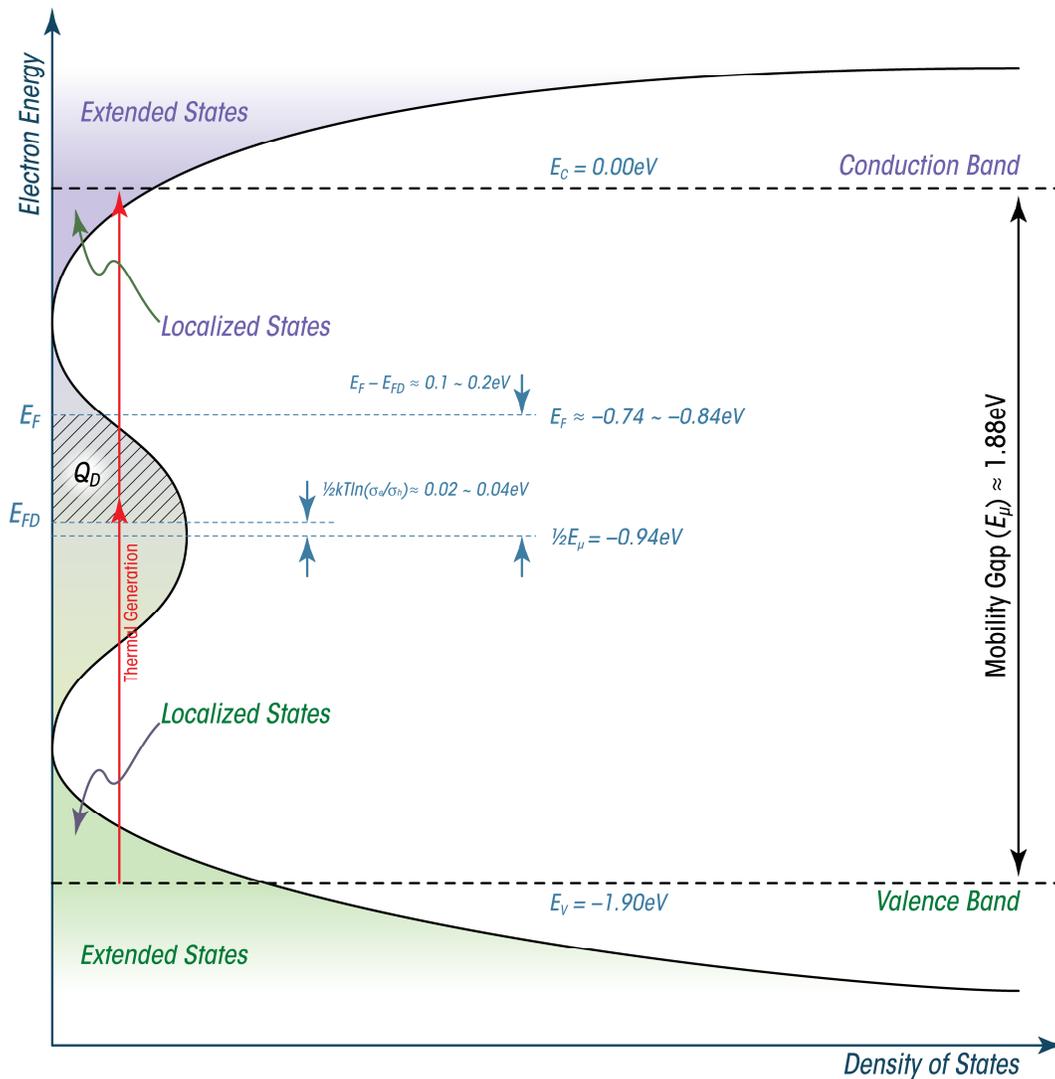


Figure 2–12: An illustration of the density of states showing the origin of the thermal generation current through gap states. The hatched region in the middle of the energy gap represents the depletion charge.

E_F is the equilibrium Fermi energy of undoped a-Si:H at zero bias. For a continuous distribution of traps, the generation current is dominated by the emission from those traps within $k_B T$ energy of E_{FD} [78]. Since neither E_F nor E_{FD} is within the band tails, $g(E)$ can be approximated as constant [71] and the occupancy factor can also be approximated, in this case as the Boltzmann function. The thermal generation current per unit area evaluated via Equation (2.31) and (2.36) is therefore [71]

$$J_{th} = t_i g(E_{FD}) k_B T \omega_{oe} \exp\left(-\frac{E_C - E_{FD}}{k_B T}\right) \quad (2.39)$$

In the case of low reverse biases, the condition stated in Equation (2.29) may not be satisfied. The quasi-Fermi energy moves away from E_{FD} near the contacts and the contribution to the current is lower [75]; therefore, full generation current is not observed. For such circumstances, the current can be approximated by multiplying the full generation current by a reduction factor: $V_a / (V_a + V_{bi})$.

2.2.3 Photodiode Capacitance

The capacitance of photodiode is an important parameter in determining the response time and maximum operating speed of the circuits it connects to. For charge readout scheme, the photodiode capacitance also dictates the maximum amount of photogenerated charge it can store before readout. Furthermore, C - V measurements of a-Si:H n - i - p photodiodes can be designed to characterize the gap states of a-Si:H depending on the voltage bias, frequency, and temperature [79].

Under moderate reverse bias, the $n-i-p$ structure behaves similar to a parallel plate dielectric capacitor where the depleted i -layer is sandwiched between two contacts. The geometric junction capacitance is given by

$$C_j = \frac{\epsilon_o \epsilon_r A_j}{W_d} \quad (2.40)$$

where ϵ_o is the permittivity of free space, ϵ_r is the relative permittivity of a-Si:H (~ 11.8), A_j is the photodiode junction area, and W_d is the depletion width. In general, the capacitance rises with decreasing frequency and increasing temperature due to more effective charge transfer from and to the localized states. At high frequency only a few shallow traps can exchange charge within the energy gap. In particular, the band-tail contribution to capacitance decreases slowly with frequency, while deeper defect states are only effective below 100Hz. At higher frequencies, trapping phenomena plays a lesser role in the measurement while depletion charge becomes relevant and the measured capacitance tends to its asymptotic junction value.

For a-Si:H $n-i-p$ photodiodes with a thin ($< 1\mu\text{m}$) and low defect density ($< 10^{15}\text{cm}^{-3}$) i -layer, the space charge is insufficient to cause the electric field to change significantly across the region. The depletion widths extend into the n - and p -layers. Therefore, the total depletion width (W_d) is given as the sum of the i -layer thickness and the depletion width in the n and p doped layers (W_n and W_p , respectively).

$$W_d = t_i + W_n + W_p \quad (2.41)$$

Finding these depletion widths require the straightforward application of the Poisson's equation [80]. Assuming an idealized model with abrupt junctions and the space charge densities uniformly distributed through the various layers [81],

$$W_d = t_i + \frac{(\rho_n + \rho_p)qV_a}{\rho_n\rho_p\varepsilon_o\varepsilon_r t_i} + \frac{\rho_n\rho_i\rho_p t_i}{\rho_n - \rho_p} \quad (2.42)$$

where ρ_n , ρ_i , and ρ_p are the space charge densities in n -, i -, and p -layers, respectively.

Since under moderate reverse bias, the i -layer is fully depleted, a small decrease in the photodiode capacitance with increasing applied voltage is due to the expansion of the depleted region into the doped contacts. The doping level in the n -layer is usually much higher than that of the p -layer; therefore, most of the contribution of this expansion occurs in the p -layer. The acceptor density (N_A) can be easily estimated from the C - V plot. From Poisson's equation, it can be concluded that a voltage variation ΔV induces a change in the depletion width in the p -layer (ΔW_p) via

$$\Delta W_p = \frac{C_j(V)}{qN_A A_j} \Delta V \quad (2.43)$$

By differentiating Equation (2.40) and applying the result to Equation (2.43), the acceptor density is obtained as

$$N_A = C_j^3 \left(q\varepsilon_o\varepsilon_r A_j^2 \frac{dC_j}{dV} \right)^{-1} \quad (2.44)$$

For fluorescence-based bio-assay applications, the photodiode is usually biased between -1.5V and -3.5V . Low reverse bias ensures full depletion of the i -layer while suppressing leakage current level. The unit area capacitance under this operation condition for a $t_i = 500\text{nm}$ photodiode is $\sim 20\text{nF/cm}^2$ and decreases slightly with increase in voltage.

2.2.4 Spectral Response

The spectral response of the photodiode directly relates to the optical absorption of the material of which it is composed. For a-Si:H $n-i-p$ photodiodes, the absorption characteristics of intrinsic a-Si:H is discussed in Section 2.1.5. Photodiode quantum efficiency (η_{qe}) and responsivity (R) provides two means of measuring the efficiency of the detector. The internal quantum efficiency (η_g) is the ratio of the number of photogenerated electron-hole pairs to the number of impinging photons of a given energy that the photodiode receives. The external quantum efficiency on the other hand, depends on the photon absorption, charge collection efficiency, and optical losses such as transmission and reflection. In an experiment, the photocurrent and optical power are usually measured instead of the number of electrons and photons. The ratio of the electrical output current (I_{ph}) in Amperes to the optical input power (P_{ph}) in Watts is termed responsivity and can be thought of as the transfer function for the photodiode.

$$R = \frac{I_{ph}}{P_{ph}} = \eta_{qe} \left(\frac{q}{\hbar\omega} \right) \quad (2.45)$$

Equivalently, quantum efficiency which is expressed as a percentage value relates to responsivity by

$$\eta_{qe} = R \left(\frac{1240}{\lambda_{nm}} \right) \times 100\% \quad (2.46)$$

where λ_{nm} is the wavelength of the impinging photon in nano-meters. The quantum efficiency is therefore

$$\eta_{qe} = \frac{n_e}{n_{ph}} = \left(\frac{I_{ph}}{q} \right) \left(\frac{\hbar\omega}{P_{ph}} \right) \quad (2.47)$$

It has been shown that an optimized design of a-Si:H *n-i-p* photodiodes can achieve a quantum efficiency of ~80% in the wavelength range of 500–600nm [82]. The photodiode quantum efficiency is degraded in practical systems and this is mainly caused by recombination where some photogenerated carriers do not survive crossing the junction and are not collected, and optical reflection losses where some photons simply do not reach the photodiode. The recombination effect can be minimized by reducing the number of recombination centers. This can be achieved by tailoring the defects during device fabrication. The reflection losses can be minimized by introducing additional layer of *anti-reflection* (AR) coating. Optical reflection occurs at the photodiode surface due to the differences in the index of refraction (n_r) of the semiconductor ($n_{si} \approx 3.4$) and air ($n_{air} = 1$). The Fresnel's equation can be applied to calculate the reflection losses if the interface between the semiconductor surface and air is flat and

planar over many wavelength distances. The reflection coefficient is given by

$$R_r = \frac{(n_{air} - n_{si})^2}{(n_{air} + n_{si})^2} \quad (2.48)$$

Therefore, more than 25% of the incident photons are reflected. A thin layer of amorphous silicon nitride ($n_{sin} \approx 2$) can be used as an anti-reflection coating. The thickness of the coating (t_{ar}) should be selected such that [83]

$$t_{ar} = \frac{1}{4} \frac{\lambda}{n_{sin}} \quad (2.49)$$

Proper use of the anti-reflection coating will enhance the quantum efficiency at specific photon wavelength while attenuating efficiency values at other spectrum range. In the case of fluorescence-based bio-assays, the desired quantum efficiency behaviour depends on the specific fluorescent dye used and is subjected to optimization.

2.2.5 Noise of *a-Si:H* Photodiodes

Noise is a random process that degrades the signal of interest. While the instantaneous value of noise cannot be predicted, a statistical model provides information on some of the important properties that is useful for analysis. In electronic devices, common sources of noise include thermal noise, flicker noise, and shot noise. Thermal noise is due to the random variation of current and voltage caused by the Brownian

movement of carriers in the semiconductor. The noise power spectral density of this source can be expressed as

$$v_{nth}^2(f) = 4k_B TR \quad (2.50)$$

where R is the resistance value of the material. Flicker noise, also referred to as $1/f$ noise due to its frequency dependence, is evident in most electronic devices operated at low frequencies. The noise power spectral density of this source can be written as

$$i_{nf}^2(f) = \frac{I_D^a}{f^b} \quad (2.51)$$

a and b are fitting parameters. The value of a and b are typically ranged between 1.5–2 and 0.8–1.4, respectively. While the origin of flicker noise is still a matter of discussion, there are different proposed models to describe this phenomenon including the fluctuation in the number of carriers [84] and mobility [85], trapping at interface states, trapping or recombination at a distribution of localized states, or even quantum effects [86]. Shot noise arises from the fact that current, despite its apparent constant value, is composed of a large number of independent random movements of charge carriers. The different arrival times of the electrons contributes to different impulses of charge, which translates to a wideband noise in the frequency domain. The shot noise power spectral density can be written as

$$i_{ns}^2 = 2qI_D \quad (2.52)$$

The studies on the noise of a-Si:H photodiodes suggests that flicker noise is the main contributing noise source at low frequencies [86]–[89]. The thermal noise is the dominant source at low biases and is due to the series resistance of the p and n contacts [90]. This component is not dependent on the current level through the photodiode as is the case for shot noise, where the contribution increases with increase in current. At high reverse bias, an expected amount of shot noise is seen. At low reverse biases, shot noise diminishes and flicker noise appears. The flicker noise is found to be dominant at low frequencies. At lower biases, the $1/f$ dependence changes to $1/f^2$ dependence with increasing frequency. At higher biases, this change in slope occurs at higher frequency value and is generally less pronounced. Flicker noise power is also found to scale exactly with the photodiode area. It is also influenced by the i -layer thickness. Thicker photodiodes show higher $1/f$ noise than thinner ones when the current value is comparable.

There are a number of models that could explain the frequency dependence of the flicker noise. From experimental evidences, the most plausible origin is argued to be the fluctuation of the charge carrier density due to trapping and releasing of carriers via the distributed trapping centers in the energy gap. Current filaments through the interface layers mediate the trapping traffic at the localized states, and the charge of localized and thermally emitted carriers switches on and off isolated current filaments through the doped contact layer and modifies the current injection into the diode whereby causing noise [91].

2.2.6 *Current Transients and Illumination*

The discussion of a-Si:H *n-i-p* photodiode concludes with the current stability issue delimited by the inferior material properties discussed in Section 2.1. The current transient decay that occur with the perturbation of the operating environment such as bias voltage forces the need for frequent correction of obtained signals to reflect this time-varying current. Furthermore, transient decay due to trapping and releasing of carriers in the deep states limits the operational speed of the sensor where small durations in between consecutive readout may lead to serious memory issues such as image lag phenomenon.

For fluorescence-based bio-assay applications, current instability caused by the Staebler-Wronski effect as described in Section 2.1.6 does not play an important role since the total illumination of sensors under normal operation conditions is much less than the magnitude needed to create defects. Actual sources of leakage current instability are all related to conduction mechanisms. The strong temperature dependence of the leakage current is an example where the variation of current is mapped from temperature fluctuations. Another example is the bias dependent reverse current which indirectly causes the leakage current of the photodiode to change for different illumination durations. Consequently, the leakage current correction measured in the dark may not apply precisely to an illuminated sensor. Current stability is less important when the dark current level is low; therefore, low leakage devices are again desirable. For high sensitivity applications such as protein function

assessment, a-Si:H *n-i-p* photodiodes offers lower leakage current and very stable dark current level near room temperature at moderate biases. The efforts of the discussions are therefore placed on the transient current of the sensor.

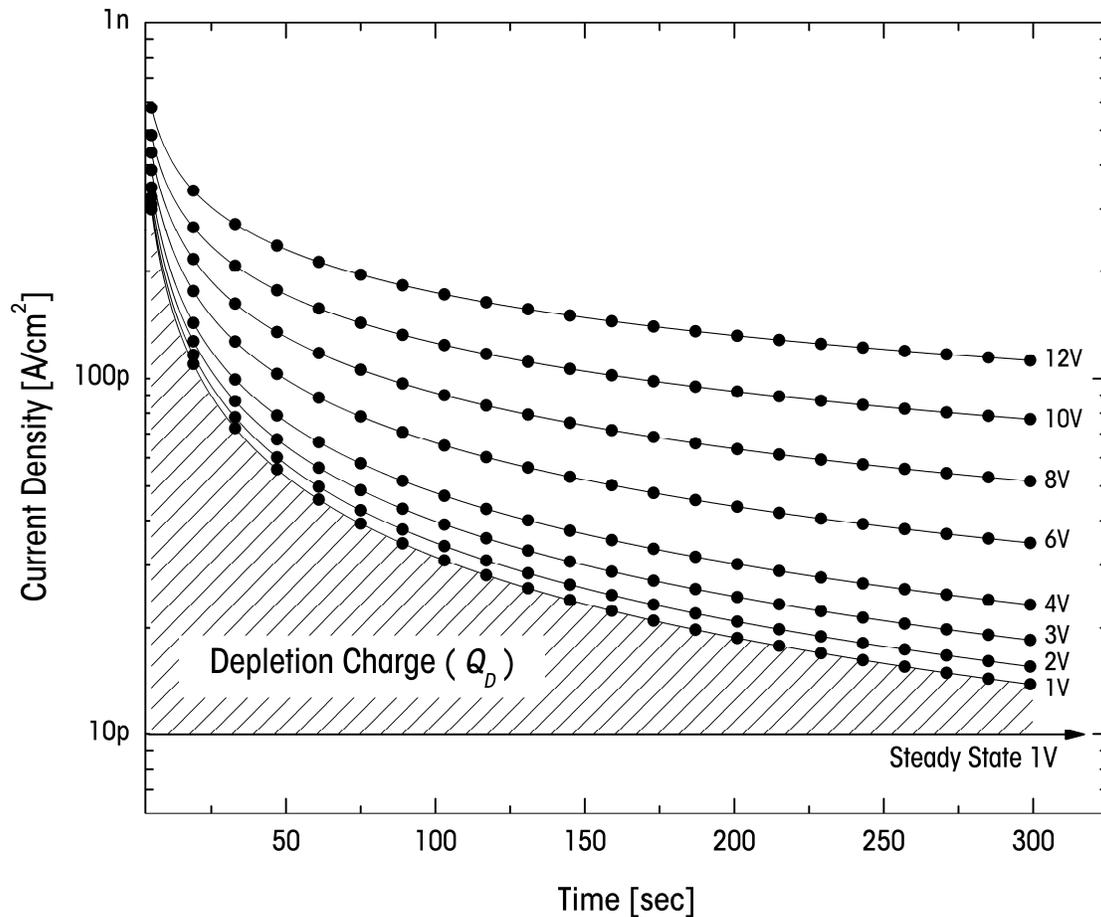


Figure 2-13: Time dependence of the dark current after a reverse bias is applied. The steady-state current level at -1V is indicated. The shaded region represents the depleted charge (Q_D) from the bulk *i*-layer.

Figure 2-13 shows the dependence the dark current on time (t) immediately follows an applied voltage bias for different reverse biases.

The dark current decreases after the reverse bias is applied from its initial value of $I_{th}(0)$ to the steady-state value $I_{th}(\infty)$. The current level decreases by about an order of magnitude over a 300sec period and continues to decay with the voltage bias maintained; the current level eventually reaches a steady-state value after an additional ~ 1500 sec. The steady-state current level for $-1V$ reverse bias is indicated in Figure 2-13 and its value is given by Equation (2.39).

The current decay transient is a phenomenon indicating a shift in E_F from its equilibrium position at zero bias to E_{FD} . In the short-time range (< 0.1 sec), the decay transient is most sensitive to the position of E_F , while in the intermediate time range (0.1–10sec), the current is mostly sensitive to the DOS distribution in the deep states. For a uniform DOS, the current decays approximately by $1/t$; the decay is faster if $g(E)$ decreases towards E_{FD} . Eventually, the current approaches its steady-state value which depends on the position of E_{FD} . The estimated values of various parameters for a typical device are indicated in Figure 2-12. Zero-bias data indicates that $g(E)$ in the deep states falls in the range of $10^{15} \text{cm}^{-3} \text{eV}^{-1}$ [71], which is close to what is approximated for intrinsic a-Si:H shown in Figure 2-4.

The equilibrium electron occupancy before applying the reverse bias is different from the steady-state value. Since intrinsic a-Si:H is slightly n -type, the equilibrium Fermi-energy lies above E_{FD} and there is an enhanced electron emission. Figure 2-12 shows that E_{FD} lies very close to the midgap in satisfying the condition of equal electron and hole generation. During the current transient, electrons are removed from the states between E_F

and E_{FD} and the occupancy factor changes. The depletion charge (Q_D), due to the release of trapped charge in the states between E_F and E_{FD} , is

$$Q_D = q \int g(E) [f(E,0) - f(E,\infty)] dE \approx qg(E)(E_F - E_{FD}) \quad (2.53)$$

The approximation in Equation (2.53) stems from the assumption that the DOS deep in the energy gap between E_F and E_{FD} is independent of energy and that there is no special dependence of the occupancy factor [71]. It is important to note that since band bending does occur in the device, the latter approximation should be taken with caution; nevertheless, the result allows simple comparisons between the measurement results. The depletion charge can be obtained from experiments by

$$Q_D = 2 \int_0^\infty [I(t) - I_{th}] dt \quad (2.54)$$

The integral is indicated by the shaded region in Figure 2–12 and Figure 2–13. A factor of two accounts for the fact that electrons contribute only a fraction of their charge to the integral as discussed in Section 2.2.2. The steady-state thermal generation current given in Equation (2.39) can be found if the depletion charge is known; J_{th} is then given by [71]

$$J_{th} = \frac{Q_D t_i}{\ln \left(\frac{I_{th}(0)}{I_{th}(\infty)} \right) \tau_{max}} \quad (2.55)$$

τ_{max} is the time constant that is inverse of the carrier release rate from E_{FD} . Its value is usually between 200sec to 300sec, which can be found by

$$\tau_{max} = \frac{1}{\omega_{oe}} \exp\left(\frac{E_C - E_{FD}}{k_B T}\right) \quad (2.56)$$

Under pulsed illumination, a-Si:H *n-i-p* photodiodes experiences similar current transient phenomenon. The photocurrent rises slowly when the photodiode is illuminated under the mechanisms discussed in Section 2.2.1, and reaches a value that corresponds to the level of illumination. When the illumination is turned off, there is a relatively fast current decay followed by a long-lasting residual current transient. Examination of the rise and decay curves indicate that the charge missing in the photocurrent rise is equal to the charge extracted from the photodiode current decay. Therefore, there is a strong indication that the delayed photocurrent rise and decay is due to the trapping and subsequent release of photogenerated carriers in the photodiode; these charges are trapped during the illumination phase and later swept out forming the residual photocurrent. Consequently, the amount of trapped charge is influence by the defect density of a-Si:H in the *i*-layer. The number of traps that can be occupied by the carriers is limited. At the start of the illumination, there are a large number of unoccupied traps in the reverse-biased photodiode; therefore, many of the photogenerated electrons are trapped. Assuming a homogenous electric field, trapping takes place everywhere in the *i*-layer. The photocurrent therefore will initially have a value much lower than the stationary photocurrent value. Moments after when a considerable number of traps are occupied, the trapping rate for the carriers slows down and the photocurrent increases towards the stationary current value.

When illumination is turned off, the trapped carriers deep in the energy gap are released from the states slowly.

Illumination with short light pulses yields a faster current decay while longer term illumination results in a higher residual current level as well as a slower current decay. The transient photocurrent also depends on the illumination intensity. At low illumination intensity, the residual current reaches a fairly constant value in the time span of seconds. At higher illumination intensity, the initial slow current decay changes over to $1/t$ dependence within one second. After a few seconds, all decay curves merge into the same line which indicates that the occupation of deep traps is not influenced by the illumination intensity if the light pulses are long enough.

For low-level photon flux fluorescence-based bio-assay applications, small changes in the band bending due to lessened amount of trapped charge yields a relative homogenous electric field in the i -layer of a-Si:H $n-i-p$ photodiodes. When there is a stationary photocurrent flowing in the photodiode, the electron occupation function for localized states at energy E in the energy gap is given by

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_{Fn}}{k_B T}\right)} \quad (2.57)$$

$$E_{Fn} = E_C - k_B T \ln \frac{N_C}{n_f} \quad (2.58)$$

The occupation of the localized states changes with illumination level, and the equilibrium states are described by the rate equations for trapping and emission of electrons. The probability for electron emission is proportional to the trap density $n_t(E)$, the occupation function $f(E)$, and the exponential factor describing the energy dependence of the thermal emission. Changes in the illumination level will prompt a corresponding response of the occupation at all energy levels given by [91]

$$\frac{df(E)}{dt} = af_{ph}(E) - af(E) \quad (2.59)$$

$$a = \omega_{oe} \left[\exp\left(-\frac{E_C - E}{k_B T}\right) + \exp\left(-\frac{E_C - E_{Fn}}{k_B T}\right) \right] \quad (2.60)$$

The differential equation can be solved analytically,

$$f(E, t) = f(E, 0)\exp(-at) + f_{ph}(E)[1 - \exp(-at)] \quad (2.61)$$

The switchover from the occupation in the dark and under stationary illumination is seen to take place by the simultaneous trapping of electrons at all energy levels. It takes increasingly longer time intervals to trap more and more electrons until the occupation function under illumination is reached. When all the traps lying between the two states are reached, the number of trapped electrons would remain constant. After the stationary level of illumination is turned off, the electrons trapped in localized states that are normally unoccupied are thermally emitted. The emission starts with the localized states and continues to reach the deep state.

An example measurement of the photodiode current transients due to the two perturbations, bias and illumination, are shown in Figure 2-14.

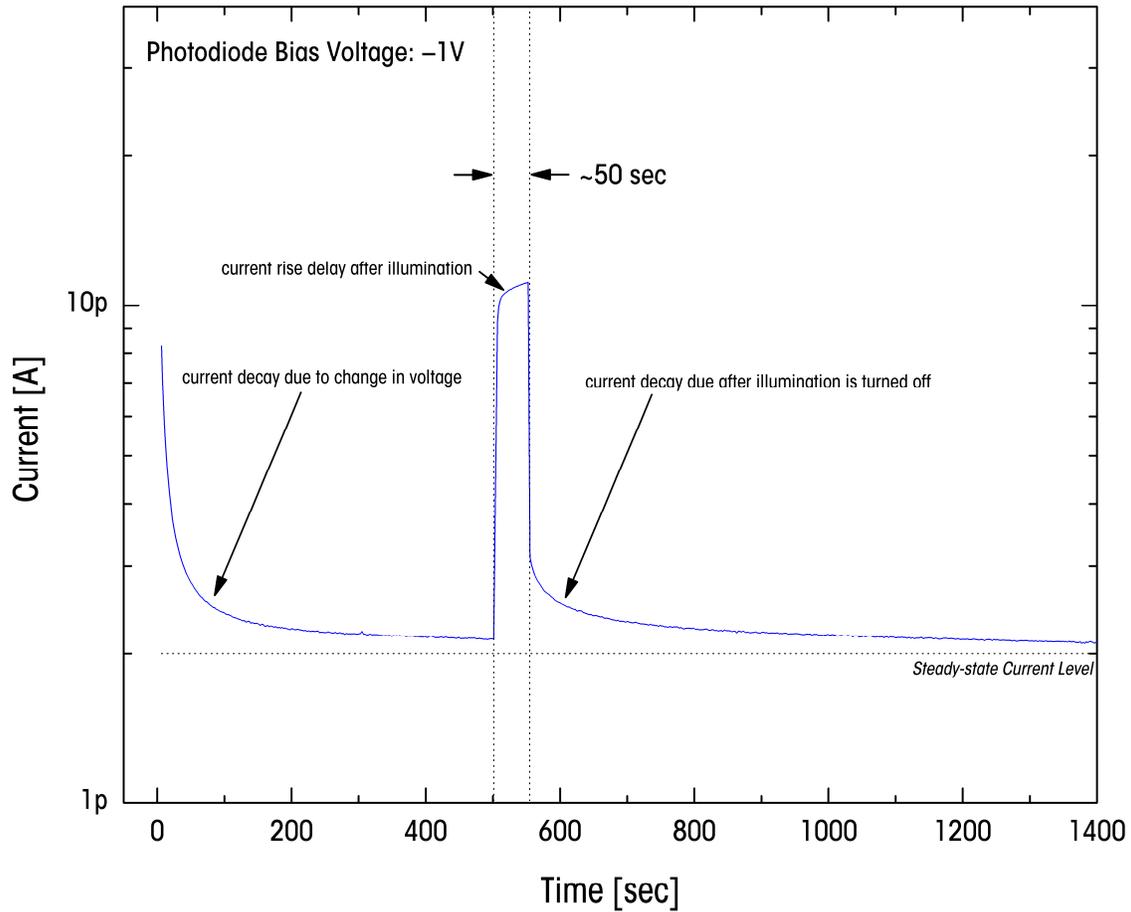


Figure 2-14: Measured current transients for an a-Si:H *n-i-p* photodiode. The photodiode is placed under continuous -1V reverse bias. The first current decay is due to bias perturbation while the second current decay is due to ~50sec illumination. The charges missing during the current rise, measured by integrating the measured current is equal to the charge released after illumination source is turned off.

The first current decay occurs after -1V reverse bias is applied to an a-Si:H *n-i-p* photodiode at $t = 0$ sec. The bias is continuously held to deplete the trapped charges. After 450s, most of the relatively shallow traps are

emptied and an illumination source is shone over the photodiode for ~50s. There is a noticeable delay for the current to reach the maximum photocurrent level. The current rise is fast immediately after the illumination is applied and gradually slows down with the continuing application of the illumination source. After the illumination source is turned off, the current decays towards the steady-state current level. The charge missing during the current rise when the illumination source is turned on reflects the transient charge release after the illumination source is turned off.

The readout time requirement for fluorescence-based bio-assays reduces the photocurrent constrains since the time between successive readout is relatively long and the intensity of the fluorescent signal is low. Nevertheless, the current transient phenomenon should be suppressed by keeping the defect state density of *i*-layer a-Si:H as low as possible. This is accomplished by carefully controlling the processing conditions and passivating the sensors to tailor the defects. The recipe in crafting such sensor as the underlying assay detector is presented in the next chapter.

Chapter 3: Fabrication of a-Si:H *n-i-p* Photodiodes

The fabrication technology incorporated to produce high quality segmented a-Si:H *n-i-p* photodiodes for this research followed the conventional PECVD processes to obtain a-Si:H materials with low defect densities. This chapter provides a full disclosure of the fabrication techniques and consolidates the details of the optimization process for the photodiodes. All a-Si:H sensors are fabricated in-house at the University of Waterloo which featured low reverse dark current optimized for low light level detection. The spectral response of the photodiode is also optimized with peak wavelength of 560nm to target the maximum emission wavelength of Cy3 fluorescent dyes. The steps involved in optimizing the devices are justified through a large number of measurements on prototype devices; the results of these measurements are also selective presented.

3.1 *Device Structure and Materials*

A number of fabrication sequences are performed to seek the preferred device structure and material for low dark current photodiodes. Different materials for contact metals, photodiode junction passivation, and transparent electrodes are experimented to obtain a good quality device. This section provides the necessary overview of the sensor structure and materials used in fabricating the prototype photodiodes.

3.1.1 Geometries

The selected sensor structure followed the $n-i-p$ substrate configuration shown in Figure 2-7, taking into account various factors such as adhesion of the contacts and quality of the interfaces. Using the same processing conditions and equipments, a-Si:H $n-i-p$ photodiodes produced in-house generally yielded one order of magnitude lower reverse dark current than a-Si:H $p-i-n$ photodiodes [63]. The photovoltaic actions of the sensors depend strongly on the interface quality between the p contact and i -layer, as discussed in Section 2.2.1. The deposition sequence of the device dictates the amount of additional defects at the $i-p$ interface. When an i -layer is deposited on top of the p -layer, the growth morphology yields a device with inferior interface quality than devices deposited in the opposite sequence. This is attributed to the fact that for $p-i-n$ structures, the p -layer is retained longer in the vacuum chamber for the entire duration of the i -layer deposition resulting in an enhanced boron diffusion process. The thick i -layer also places mechanical stress on the atomic structure of the thin p -layer, giving additional strain to the bonds of the random network. Furthermore, the $p-i-n$ structure places constraints on the selection of the substrate material the thin-film structures reside on since it needs to be transparent to the wavelength of interest. Robust substrates such as metal foil would fail this requirement which leads the choice back to the $n-i-p$ structure design. For the reasons mentioned above, the $n-i-p$ photodiode structure is therefore chosen for the bio-assay sensor system.

Figure 3–1 shows a detailed illustration of the device structure cross-section for an a-Si:H *n-i-p* photodiode. Segmented photodiodes do not share a common *n-i-p* stack when they are placed side-by-side; the neighbouring photodiodes are isolated by a thick layer of non-stoichiometric hydrogenated amorphous silicon nitride (a-SiN_x:H) passivation. The bottom electrode is formed with *n*-layer deposited on top of a thin metal layer. The top electrode is formed with the combination of *p*-layer, *transparent conducting oxide* (TCO), a-SiN_x:H, and contact metal.

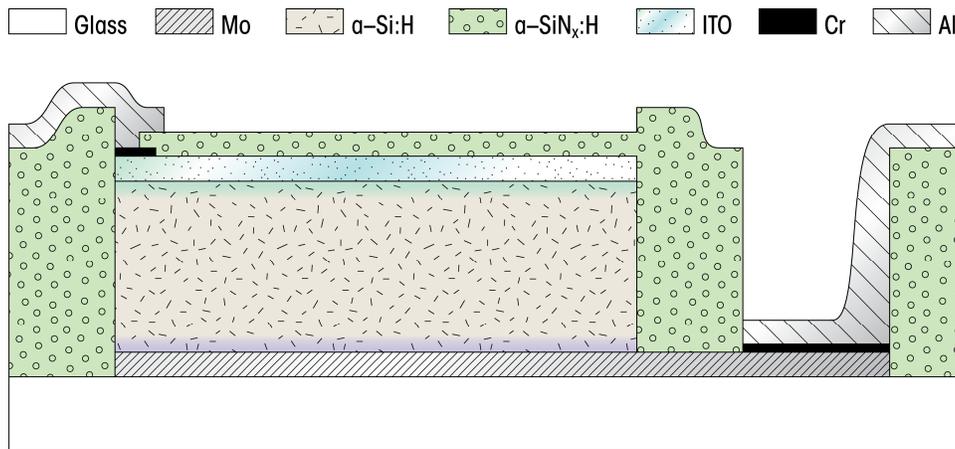


Figure 3–1: A detailed illustration of the device cross-sectional diagram of segmented a-Si:H *n-i-p* photodiode built on top of glass substrate.

3.1.2 Thin Film Layers

Hydrogenated amorphous silicon used for the *n-i-p* stack deposition is discussed in Section 2.1. Therefore, this subsection focuses on the materials used in other parts of the a-Si:H *n-i-p* photodiode, which include metal contacts, silicon nitride passivation, and transparent contacts.

Metals Contacts

Chromium (Cr) and molybdenum (Mo) are typically used as bottom metal layers for a-Si:H *n-i-p* photodiodes, while aluminum (Al) is commonly used for top metal contacts and pad metallization. These metals are often prepared through conventional sputtering processes. Even though Mo has a lower resistivity than Cr (Mo: $10^{-5}\Omega\cdot\text{cm}$, Cr: $10^{-6}\Omega\cdot\text{cm}$), it is not as widely used as Cr due to its poor selectivity with a-Si:H wet etching and higher stress. The heavy metal Cr forms a good interface to a-Si:H with its lower diffusion; therefore, a good ohmic contact can be formed between Cr and the bottom n^+ a-Si:H layers. Furthermore, Cr is stable at high temperatures and is resistant to the a-Si:H etchant, which renders it an excellent candidate for bottom electrodes. Photodiodes with Al bottom electrode generally have higher dark current level since Al diffuses more easily into n^+ a-Si:H at their interface. Al also has an order of magnitude higher thermal expansion coefficient which would cause undesirable stress when deposited in large areas. The stress brings in the tradeoffs on the metal film thickness. A thicker film yields a lower resistance but causes higher stress. Typically, a bottom metal layer has a thickness in the range of tens of nanometers, while a top metal layer has a thickness of a fraction of a micrometer.

Silicon Nitride Passivation

Amorphous silicon nitride is commonly used as a passivation material in segmented a-Si:H photodiodes owing to its good interface properties with a-Si:H. Silicon nitride is also frequently used as gate insulators in a-Si:H

TFTs. Using PECVD, a-SiN_x:H can be prepared by mixing silane gas with ammonia (NH₃) in the deposition chamber. When a-SiN_x:H changes stoichiometry from a silicon rich to nitrogen (N) rich film, the defect state density decreases due to the reduced number of dangling bonds. Thin a-SiN_x:H films can also be utilized as part of an antireflective coating. By varying the ratio of the deposition gases, the band gap of a-SiN_x:H can be controlled. Typical deposition conditions yield a band gap value of ~5.3eV; the value is larger if the a-SiN_x:H film is N rich and smaller if it is Si rich. For example, if N to Si ratio is changed from 0.9 to 1.6, the band gap would change from 1.7 to 5.6eV [92]. Therefore, due to the aforementioned merits, a-SiN_x:H is used exclusively as the passivation and AR coating material for the photodiodes used in this research work.

Transparent Conducting Oxide

The substrate photodiode structure requires at least one electrode to provide both optical access and low-resistance electrical connection. This is achieved with either a very thin metal film or a degenerately doped wide band gap oxide or nitride semiconductor. Indium-based TCO materials such as indium tin oxide (ITO) and indium zinc oxide (IZO) are most popularly among sensors for imaging applications. They are commonly fabricated by magnetron sputtering deposition techniques. Even though both amorphous ITO and IZO can be deposited at room temperature, at present, ITO offers the lowest resistivity ($\sim 10^{-4}\Omega\cdot\text{cm}$) [93]. Low-temperature deposition of ITO also leads to highly planar amorphous thin films. Such film can be etched relative rapidly with HCl-based etchants.

The lower fabrication cost of IZO and high chemical and thermal stability renders them as an attractive replacement for ITO. However, such a replacement is still not feasible for large area imaging applications due to its increased resistance. For this research work, ITO is used as the top TCO for the photodiode sensors.

3.2 *Fabrication and Characterization*

Having presented the structure and materials for the a-Si:H *n-i-p* photodiode sensor, this section discloses in full detail the fabrication recipe for low reverse dark current a-Si:H *n-i-p* photodiode. Selected characterization techniques and measurement results including I_D - V characteristics, spectral response, and defect density obtained from current transients are also presented. They are used to partially examine and improve the processing technology. The last portion of this section presents some of the steps taken to optimize the photodiode.

3.2.1 *Fabrication and Photolithography*

A set of photolithography masks is made for patterning the materials used during each processing steps. Details of these processing steps are given in Table 3-1. Illustrations of the device cross-sections for each step are provided in Figure 3-2 through to Figure 3-6. All a-Si:H *n-i-p* photodiode samples are fabricated on Corning 7059 glass substrates utilizing standard processing steps that includes sputtering of contacts, multi-chamber PECVD, as well as wet and dry etching.

Table 3-1: Detailed process sequence for a-Si:H *n-i-p* photodiodes deposited on Corning 7059 glass substrates. Sequences are compiled from reference [70] and [82].

	Process	Description	Remarks
1	Clean glass substrate	Clean with RCA	10 minutes RCA: H ₂ O ₂ + NH ₄ OH + H ₂ O
2		Hot wash	10 minutes
3		Rinse in DI water	2 minutes
4		Spin dry	2 minutes
5	Mo deposition	Sputter ~50nm (Mo)	Edwards sputtering system
6	Mask 1: Mo	Spin-on photoresist	
7		Pre-bake	
8		Expose to Mask 1	
9		Develop	
10	Mo etch	Wet etch Mo in PAN	40°C for 5 minutes PAN: H ₃ PO ₃ + HNO ₃ + CH ₃ COOH + H ₂ O
11		Wet strip resist	20°C for 5 minutes
12		Clean	Rinse in DI water and spin dry
13	a-Si:H <i>n-i-p</i> stack deposition	Preheat	PECVD Not breaking vacuum a-SiN _x :H is used as a mask to pattern the <i>n-i-p</i> stack TMB: B(CH ₃) ₃
14		Deposit 30nm <i>n</i> ⁺ a-Si:H	
15		Deposit 500nm <i>i</i> a-Si:H	
16		Deposit 4nm a-SiC:H	
17		Deposit 20nm <i>p</i> ⁺ a-Si:H	
18	Deposit 100nm a-SiN _x :H		
19	Mask 2: a-Si:H <i>n-i-p</i> stack	Spin-on photoresist	
20		Pre-bake	
21		Expose to Mask 2	
22		Develop	
23	Nitride etch	Wet etch a-SiN _x :H	20°C, 30 – 60 seconds
24		Clean	Rinse in DI water and spin dry
25	a-Si:H <i>n-i-p</i> stack etch	RIE etching	Dry etch with SF ₆ + O ₂ plasma Etching condition and parameters are subjected to optimization
26		Wet strip photoresist	20°C, 5 minutes
27		Clean	Rinse in DI water and spin dry
28	Passivation deposition	Deposit 500nm a-SiN _x :H	PECVD
29	Mask 3: Nitride window	Spin-on photoresist	
30		Prebake	
31		Expose to Mask 3	
32		Develop	
33	Nitride etch	Wet etch a-SiN _x :H in BHF	BHF: HF + NH ₄ F

34		Wet strip photoresist	20°C, 5 minutes
35		Clean	Rinse in DI water and spin dry
36	ITO deposition	Deposit ~65nm ITO	Sputter deposition Thickness is subjected to optimization
37	Mask 4: ITO	Spin-on photoresist	
38		Pre-bake	
39		Expose to Mask 4	
40		Develop	
41	ITO etch	Wet etch ITO	ITO etchant: HF solution + HCl
42		Wet strip photoresist	
43		Clean	Rinse in DI water and spin dry
44	Cr deposition	Deposit 30nm Cr	Sputter deposition Increases ITO and Al adhesion and barrier ITO from BHF etchant
45	Mask 5: Cr	Spin-on photoresist	
46		Pre-bake	
47		Expose to Mask 5	
48		Develop	
49	Cr etch	Wet etch Cr	20°C, 1 minute
50		Wet strip photoresist	20°C, 5 minutes
51		Clean	Rinse in DI water and spin dry
52	Anti-reflection coating deposition	Deposit 100nm a-SiN _x :H	Thickness of AR coating is subjected to optimization
53	Mask 6: AR	Spin-on photoresist	
54		Pre-bake	
55		Expose to Mask 6	
56		Develop	
57	AR etch	Wet etch a-SiN _x :H	Etch stop at Cr
58		Wet strip photoresist	20°C, 5 minutes
59		Clean	Rinse in DI water and spin dry
60	Al deposition	Deposit 500nm Al	Sputter deposition
61	Mask 7: Al	Spin-on photoresist	
62		Pre-bake	
63		Expose to Mask 6	
64		Develop	
65	Al etch	Wet etc Al in PAN	
66		Wet strip photoresist	20°C, 5 minutes
67		Clean	

The deposition of the thin metal films for bottom and top metallization is performed in an Edwards sputtering system. The parameters used for these processes are given in Table 3–2. a–Si:H, a–SiN_x:H, and ITO layers are deposited using a computer controlled multi-chamber PECVD and sputtering system, design and built by MVSystems Inc. As shown in Figure 3–2, a thin ~50nm molybdenum layer is first sputtered on a Corning 7059 glass substrate and patterned with the first photolithography mask to form the bottom contact pads for the segmented *n-i-p* junctions.

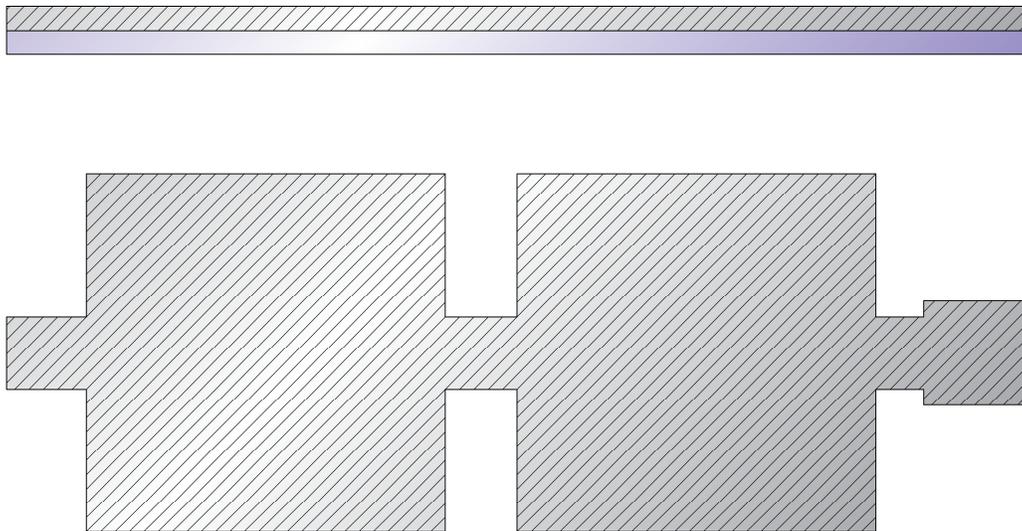


Figure 3–2: An illustration of the device cross-section and top view after the first photolithography step.

Table 3-2: Optimized process parameters for depositing Mo, Cr, and Al films in the Edward sputtering system.

Metal	Argon Flow Rate [sccm]	Process Pressure [mTorr]	RF Power [W]	Growth Rate [Å/sec]
Mo	25	4	320	1.7
Cr	25	3	240	1.5
Al	30	5	360	1.2

Following that, a $n-i-\delta_i-p$ hetero-structure is deposited using PECVD and patterned by *reactive ion etching* (RIE). In order to avoid cross contaminations, the doped and undoped a-Si:H layers are deposited in separate chambers without breaking vacuum. The base pressure is set to $\sim 2 \times 10^{-7}$ Torr. The n - and i -layers are deposited at a stabilized substrate temperature of 220°C. The substrate temperature is subsequently lowered to 180°C to deposit a thin layer of a-SiC:H film. This is done to prevent possible impurity diffusion and preserve the integrity of the $i-p$ interface. The n -type a-Si:H (~ 30 nm) is prepared by the decomposing the $\text{SiH}_4 + \text{PH}_3$ ($\sim 1\%$ in H_2) gas mixture. The intrinsic a-Si:H layer (~ 500 nm) is deposited in another chamber using silane gas. The flow rates of the silane and dopant gases are 20sccm and 10sccm, respectively. The process is carried out at a pressure of 400mTorr and RF power of 2W. The thin (~ 2 nm) graded layer is deposited by gradually increasing the flow rate of CH_4 up to 40sccm while keeping the SiH_4 flow rate constant at 20sccm. This is followed by the deposition of ~ 4 nm a-SiC:H buffer layer at a processing pressure of 500mTorr. Finally, a p -type a-SiC:H layer with optical band gap of ~ 2.1 eV is prepared using the doping gas *trimethylborane* (TMB) ($\sim 1\%$ in H_2). The deposition for this layer is done

with processing pressure of 600mTorr, RF power of 2W, SiH₄ flow rate of 20sccm, CH₄ flow rate of 40sccm, and B₂H₆ (~2% in H₂) flow rate of 10sccm. The *n-i-p* stacks are formed by etching the amorphous silicon layers in SF₆ plasma via Trion Phantom II RIE system, operated at 13.56MHz. The dry etch experiments are carried out with a base pressure 10^{-5}Torr at room temperature. The etching conditions are: RF power of ~50W, process pressure of 120mTorr, and SF₆ flow rate of 30sccm.

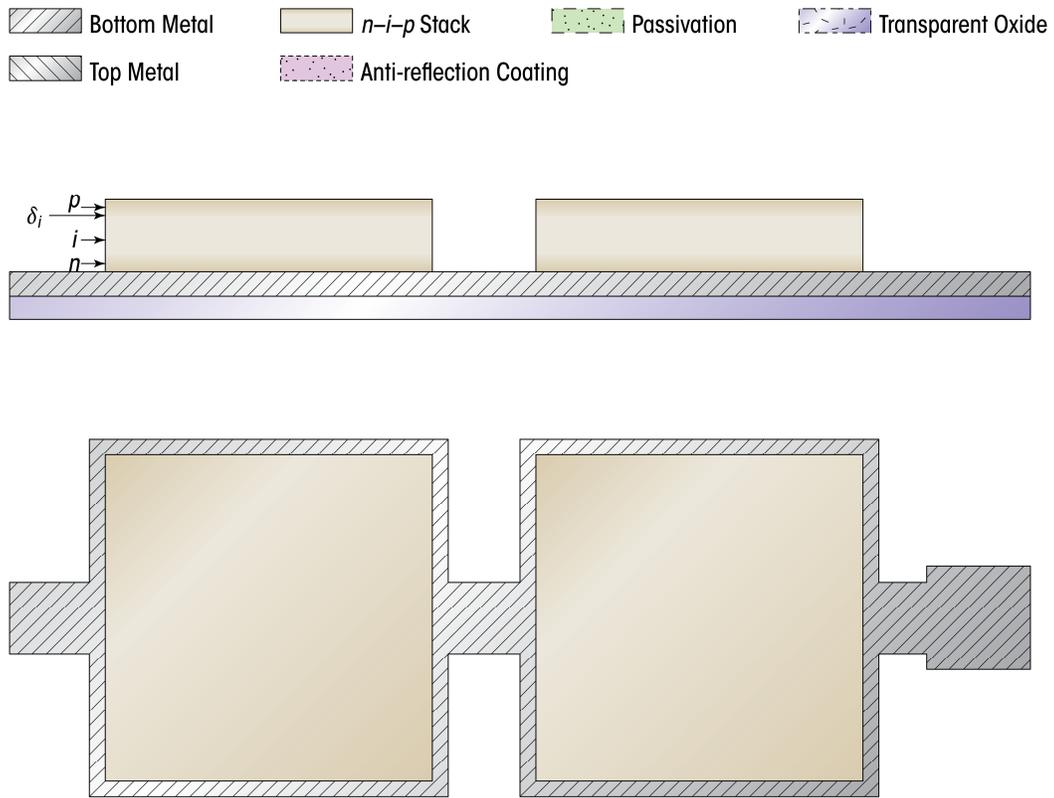


Figure 3-3: An illustration of the device cross-section and top view after the second photolithography step. The *n-i-p* stacks are separated with RIE. The a-SiN_x:H is used as a masking layer.

Two *n-i-p* stack formation methods are tested. In the first method, the sample is patterned by positive photoresist and loaded into the RIE

chamber for processing. After etching, the resist is stripped with acetone and the wafer is cleaned in *deionized* (DI) water and subsequently dried. The use of photoresist as a mask is a concern due to the frequent occurrences of polymer grass formation under the given etching conditions. In the second method, a 70–100nm a-SiN_x:H film is deposited on top of the *n-i-p* structure. The a-SiN_x:H is patterned with photoresist and etched in *buffered hydrofluoric acid* (BHF) solution, followed by resist stripping. During RIE, the a-Si:H *n-i-p* stack etches much faster than a-SiN_x:H in the plasma; therefore, rendering a-SiN_x:H as an effective masking layer. After dry etching, the wafer is quickly reloaded into the PECVD system for the deposition of the passivation layer. The second method is more advantageous in terms of achieving lower reverse leakage current since it avoids the contamination of the junction sidewalls, which happens during the etching operation described for the first method. Therefore, the second photolithography method is used for the optimized photodiodes. Table 3–3 lists some of the parameters measured for the layers used for the *n-i-p* stack.

Table 3–3: A list of measured parameters for various types of layers of the *n-i-p* stack. The thin film samples used the same processing parameters and are deposited on glass.

Layer	Deposition Rate [Å/sec]	Sheet Resistance [Ω/□]	Dark Conductivity [S/cm]
<i>n</i>	1.3	8.9×10^7	8.78×10^{-4}
<i>i</i>	1.8	1.42×10^{14}	1.94×10^{-10}
<i>p</i>	2.6	1.2×10^{10}	1.59×10^{-6}

After the formation of the *n-i-p* stack, a ~500nm a-SiN_x:H passivation layer is deposited over the segmented *n-i-p* structures from a mixture of

silane (3sccm) and ammonia (100sccm) (Figure 3–4). The deposition conditions are as follows: 400mTorr processing pressure, 7W RF power, and 180°C substrate temperature. This stage can also be considered as a post-etch annealing step to help in reducing the edge leakage caused by defects on the photodiode edge. After patterning and etching the silicon nitride to open windows for the underlying photodiodes, a ~65nm ITO film is deposited using RF sputtering (Figure 3–5). The sputtering conditions are: 80W RF power, 15sccm argon (Ar) flow rate, 5mTorr process pressure, and 120°C substrate temperature.

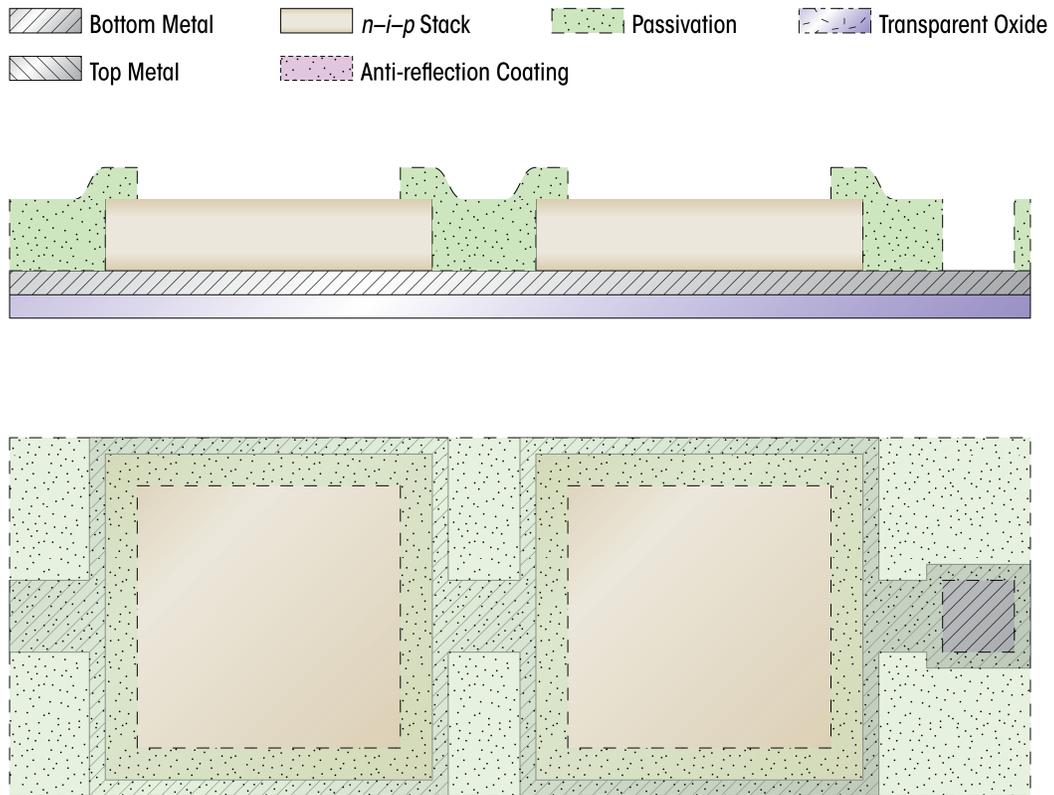


Figure 3–4: An illustration of the device cross-section and top view after the third photolithography mask. The a-SiN_x:H passivation helps to reduce the leakage caused by defects on the silicon sidewalls.

The growth rate of the ITO film is $\sim 1.2 \text{ \AA/s}$. The ITO layer is patterned with photoresist and etched using an HCl/HNO_3 solution to form the top photodiode electrodes.

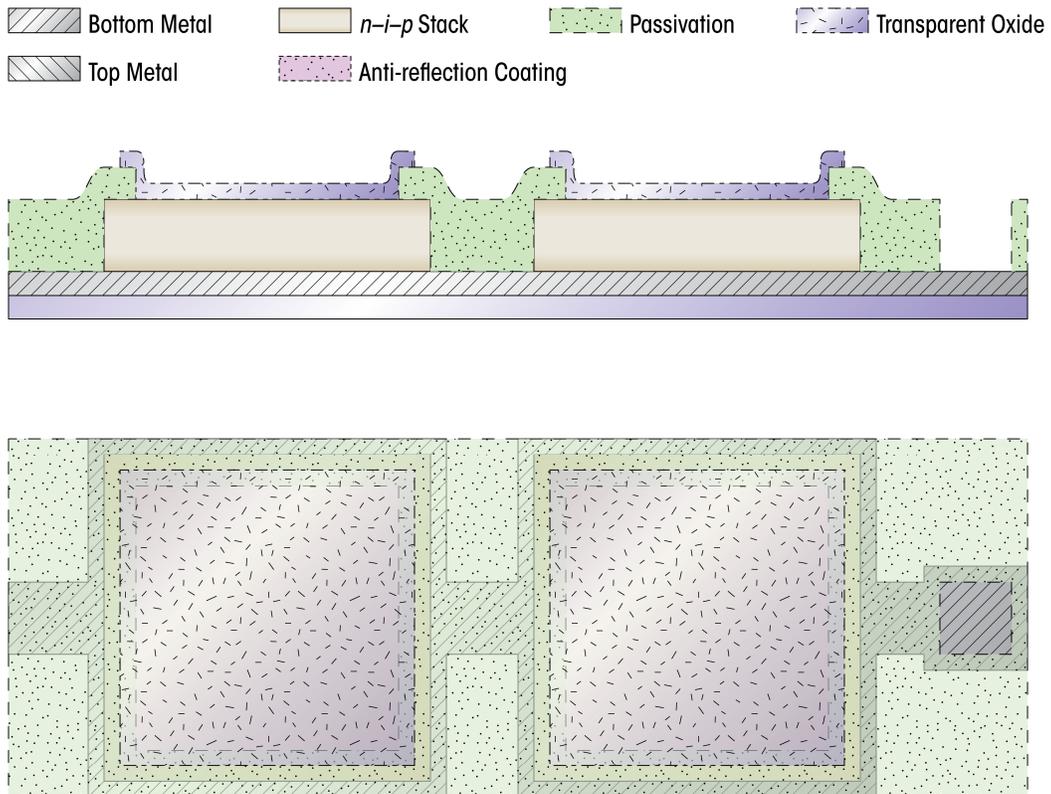


Figure 3-5: An illustration of the device cross-section and top view after the fourth photolithography mask. The thickness of the ITO layer is subjected to optimization.

To create an excellent adhesive contact to the ITO, a $\sim 30 \text{ nm}$ thick Cr layer is sputtered. This film also serves as a protective layer in the wet-etch process since *phosphoric-acetic-nitric* (PAN) etchant used for Al also etches ITO. Afterwards, a $\sim 100 \text{ nm}$ a-SiN_x:H film is deposited over the entire wafer at 150°C substrate temperature (Figure 3-6). The nitride layer

not only serves as an AR coating for the photodiodes, but also protects the ITO contact from environmental degradations.

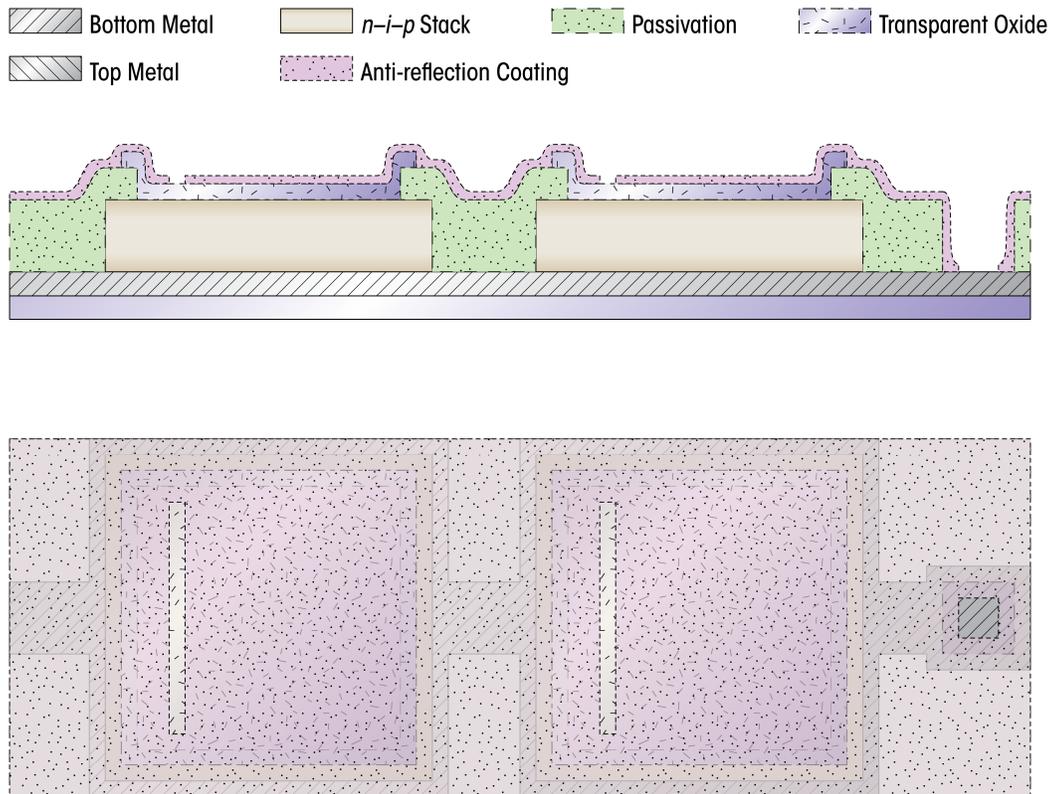


Figure 3-6: An illustration of the device cross-section and top view after applying the fifth and sixth photolithography masks. The thickness of the anti-reflection coating is subject to optimization.

The thickness of the nitride layer is subjected to optimization to maximize the amount of photons available to the *i*-layer of the photodiode. The silicon nitride is selectively etched to open top contact vias for the photodiodes. Finally, the photodiode fabrication is completed with the sputtering and patterning of Al as its top metallization (Figure 3-7). The specifics of the above process recipe can be slightly adjusted to vary the

performance of the photodiode. Such characterization and modification cycle is discussed in Section 3.3.

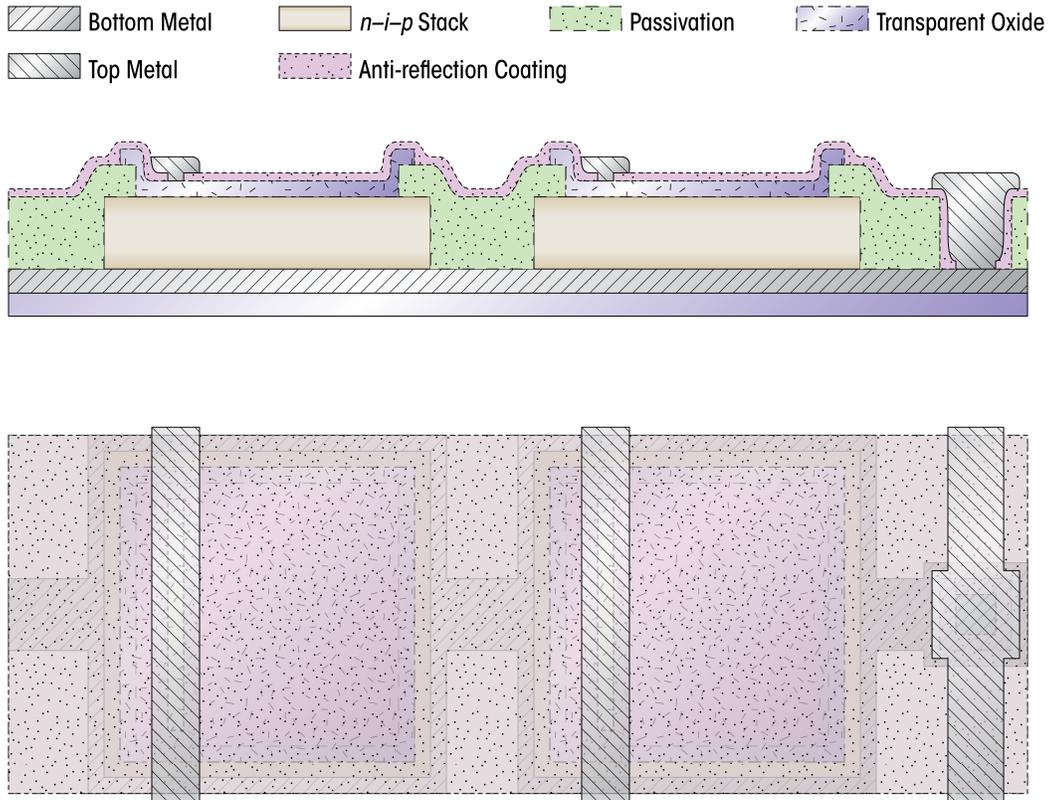


Figure 3-7: An illustration of the device cross-section and top view after applying the final photolithography masks. Aluminum is patterned as the top metallization layer for photodiode electrodes and bonding pads.

3.2.2 Device Performance

The fabricated devices are characterized to evaluate their performances as well as to tweak the fabrication recipe. Selected results are presented in this subsection along with a brief description of the test setup constructed for the measurements.

Quasi-static Dark J_D - V Characteristics

The electrical measurements are performed with a Keithley 4200-SCS semiconductor characterization system accompanied by four 4200-PA remote pre-amplifiers. An illustration of the test setup is given in Figure 3–8. In order to measure the dark characteristics, the viewing window on the MicroChamber is covered by a metal plate. The fabricated photodiodes are extremely sensitive; even with the metal plate cover in place, some light still enter the chamber from side openings caused by uneven surfaces of the metal plate cover. Therefore, a layer of black electrical tape is placed around the plate cover to completely seal the top. Stray light from the side of the chamber is blocked by black cloth covering the platform completely.

The remote pre-amplifiers are crucial for the reverse bias measurements since current levels for some of the photodiodes are in the sub-pA range. Environmental noise sources can be coupled into the cables in-between the probes and the measurement computer. With remote pre-amplifiers installed, current level in the range of ~ 10 fA can be confidently measured without severe degradations.

Figure 3–9 shows two typical quasi-static J_D - V characteristics of large and small photodiodes measured in the dark at room temperature. In order to minimize the transient current induced by the release of the trapped charge, an initial six minutes delay is placed to allow the Fermi level to reach its equilibrium position. Following that, a ten second hold time is given between each measurement points. The bias voltage is varied from 1V to -5 V with a 25mV interval.

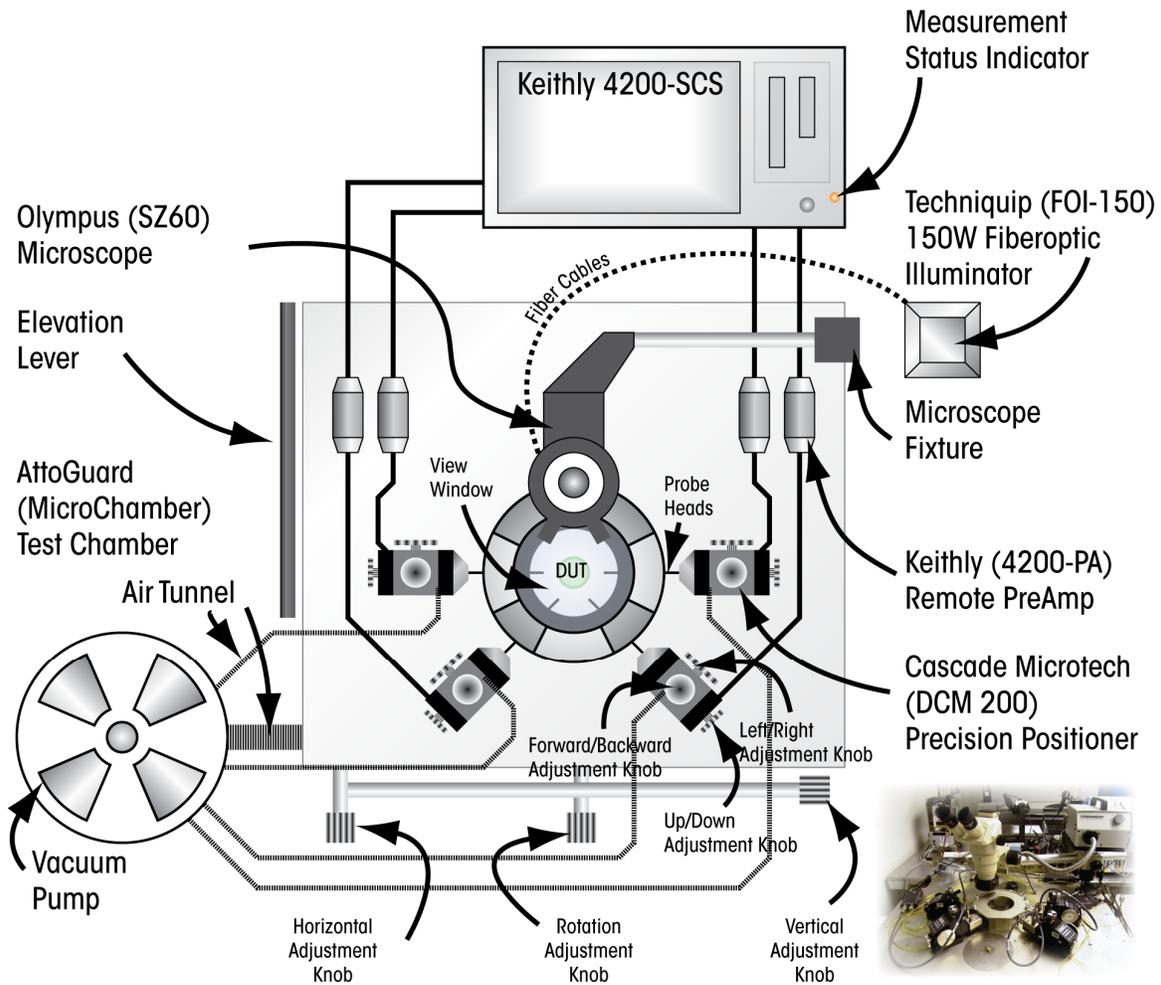


Figure 3-8: An illustration of the equipment setup used for measuring the quasi-static J_D - V characteristics. The setup is used extensively during the optimization phase of the photodiode fabrication.

For large photodiodes, the $\log|J_D|$ - V plots are precisely linear in the forward bias range of 0.15–0.6V. Through a curve fitting procedure, the diode ideality factor (n) and saturation current density (J_0) are extracted and are 1.4 and 0.6pA/cm², respectively. The equivalent shunt resistance (R_0) is $\sim 400\text{G}\Omega$ at a bias of $\pm 50\text{mV}$. At biases higher than 0.75V, the J_D - V

dependence is non-exponential and the forward current is space charge limited [94].

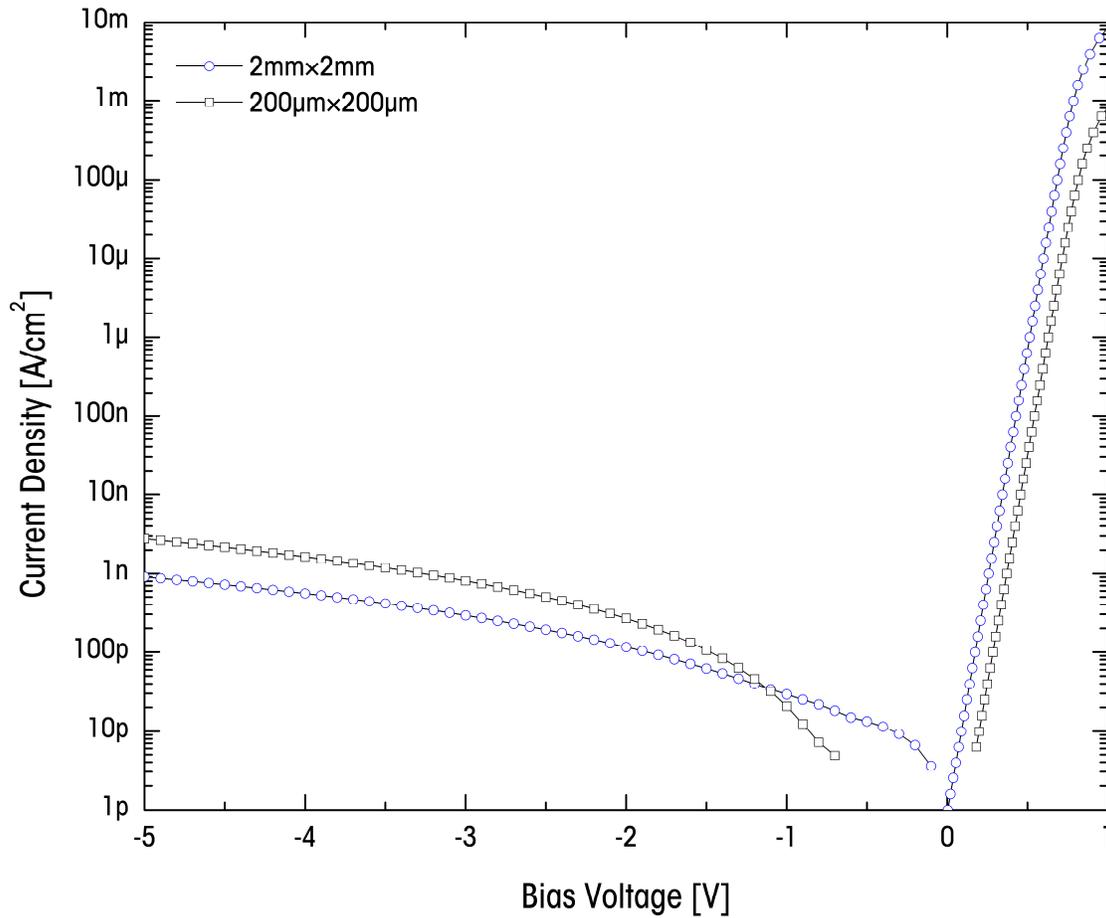


Figure 3–9: A plot of the quasi-static J_D - V characteristics for two non-optimized a-Si:H n - i - p photodiodes fabricated in-house. The measurements are conducted in the dark, at room temperature.

The reverse bias leakage current is one of the most important characteristics of the photodiode sensor since it determines the lowest detectable light level. As shown in Figure 3–9, the reverse dark current density level of non-optimized photodiodes fall in the range of 1nA/cm^2 at -5V bias. This is only slightly higher than the junction leakage reported for

non-segmented a-Si:H *p-i-n* photodiode arrays with continuous intrinsic layers [95], [96]. The leakage current mechanisms must be identified to minimize its contributions during device design and fabrication. It is subjected to optimization which is discussed in more detail in Section 3.3.

Spectral Response

The spectral response measurements are performed with a PC controlled setup based on Oriel's 77200 grating monochromator, Stanford Research System's SR540 light chopper, and SR530 DSP lock-in amplifier. A block diagram of the test setup is illustrated in Figure 3-10.

The Oriel illuminator (model 66181) with halogen lamp is used as the initial light source for the spectral response measurements. The light chopper effectively modulates the beam at a given frequency. The modulation frequency, set to 40Hz for most of the measurements, is controlled by the SR540 chopper controller. The modulated polychromatic light beam enters the Oriel monochromator (model 77200). The monochromator uses diffraction gratings to spatially separate light beam to different wavelengths. From the theory of optics, the incident light and the reflected light from the gratings need to be an integer multiple of each other to result in constructive interference. By shifting the location of the grating surface, narrow spectrum light beam of a given central wavelength can be obtained. An Oriel step motor controller (model 20025) is used to change the output wavelength, which is controlled by computer via a parallel port. The resulting chopped quasi-monochromatic beam is passed through a second lens. This focused beam is then divided by an Oriel fused

silica beam splitter to illuminate the sample. The system is calibrated between 300nm and 1100nm using a Newport 818-UV photodetector. A 1.5V reverse bias is applied to the a-Si:H *n-i-p* photodiode under test.

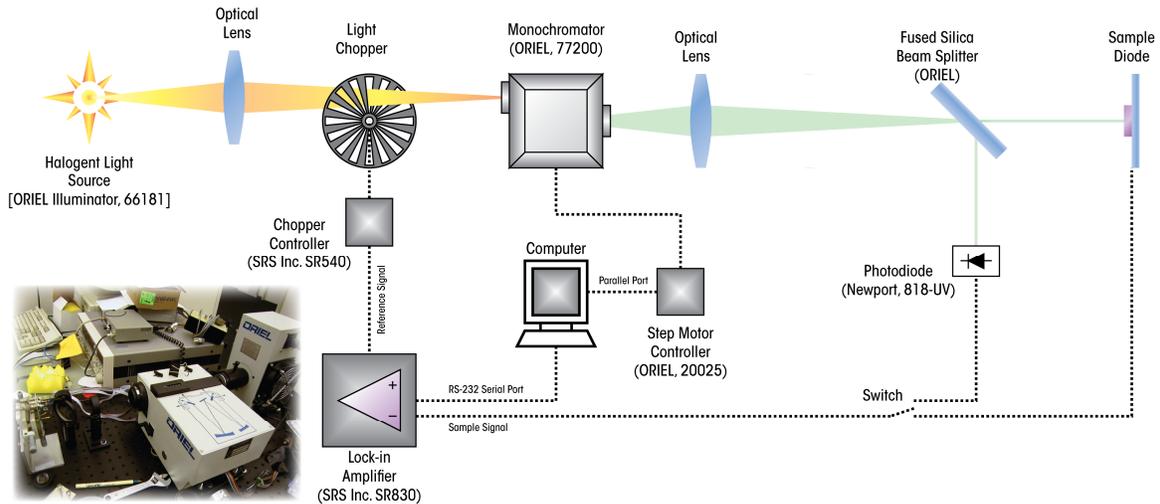


Figure 3–10: An illustration of the equipment setup used in measuring the spectral response of the photodiodes. The manufacturer and model of the important equipments are listed in brackets.

The heart of the spectral response system is the SR830 DSP lock-in amplifier. Lock-in amplifiers can detect very small AC signals, often down to few nano-Volts. Accurate measurements can be achieved even if the small signal is obscured by noise sources many thousand times greater. It uses phase-sensitive detection technique to single out the component of the signal at a specific reference frequency. Noise signals at frequencies other than the reference frequency are discarded. The reference frequency in this case is the frequency of the light chopper, set and controlled by the SR540 chopper controller. The control signals of the light chopper and the photodiode current are both fed into the lock-in amplifier.

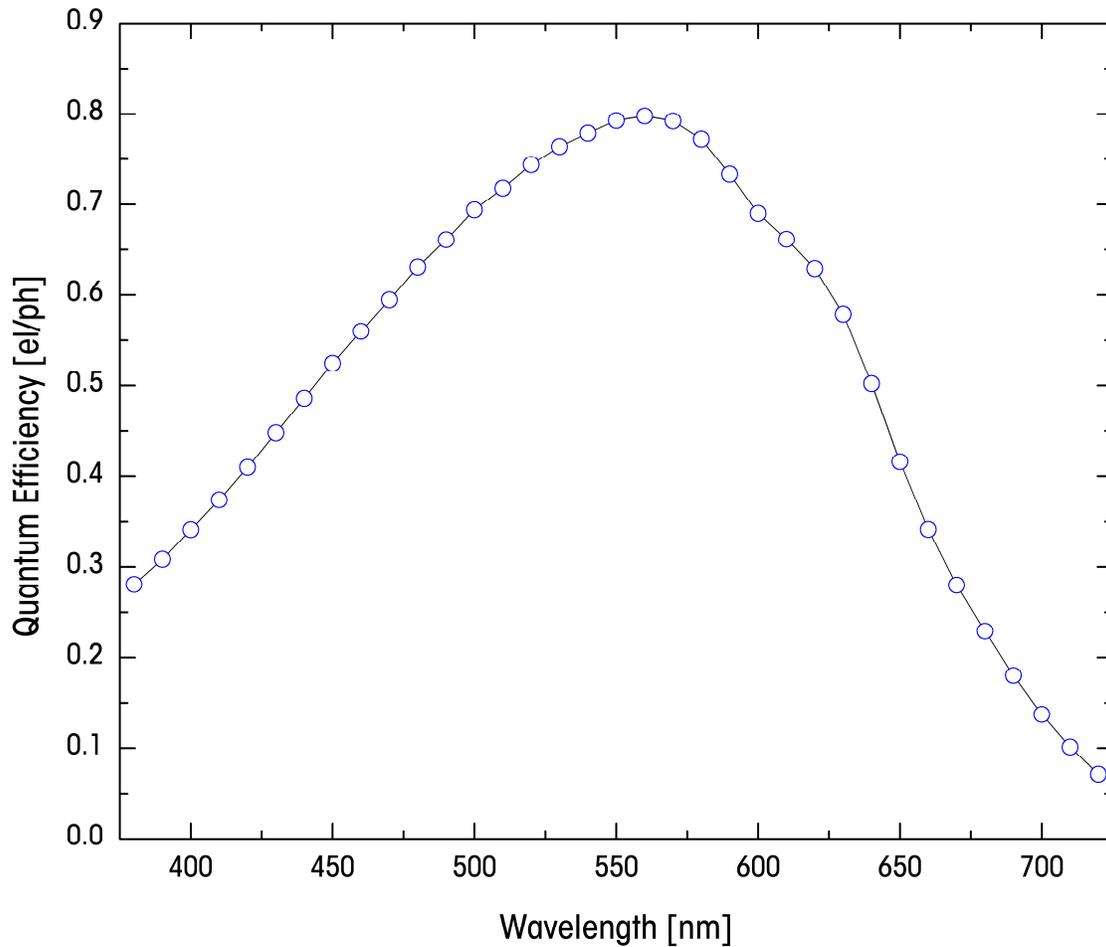


Figure 3–11: The spectral response characteristics of large a-Si:H *n-i-p* photodiodes. Peak quantum efficiency is achieved at ~560nm.

Figure 3–11 shows the measured spectral response of large photodiodes. The spectral response peaks around 560nm. In the short wavelength region, the quantum efficiency is limited by optical absorption and free carrier recombination in the doped layer; therefore, minimizing the *p*-layer thickness is important in device optimization. Thinning the contact layer excessively is an issue since the contact layer should contain enough dopant charge to deplete the *i* layer and compensate for the work function

difference between the TCO and a-SiC:H. In the long wavelength region, the photodiode is insensitive to photons with absorption depth larger than the thickness of the *i*-layer; therefore, causing the quantum efficiency to drop again.

Illumination Induced Degradation

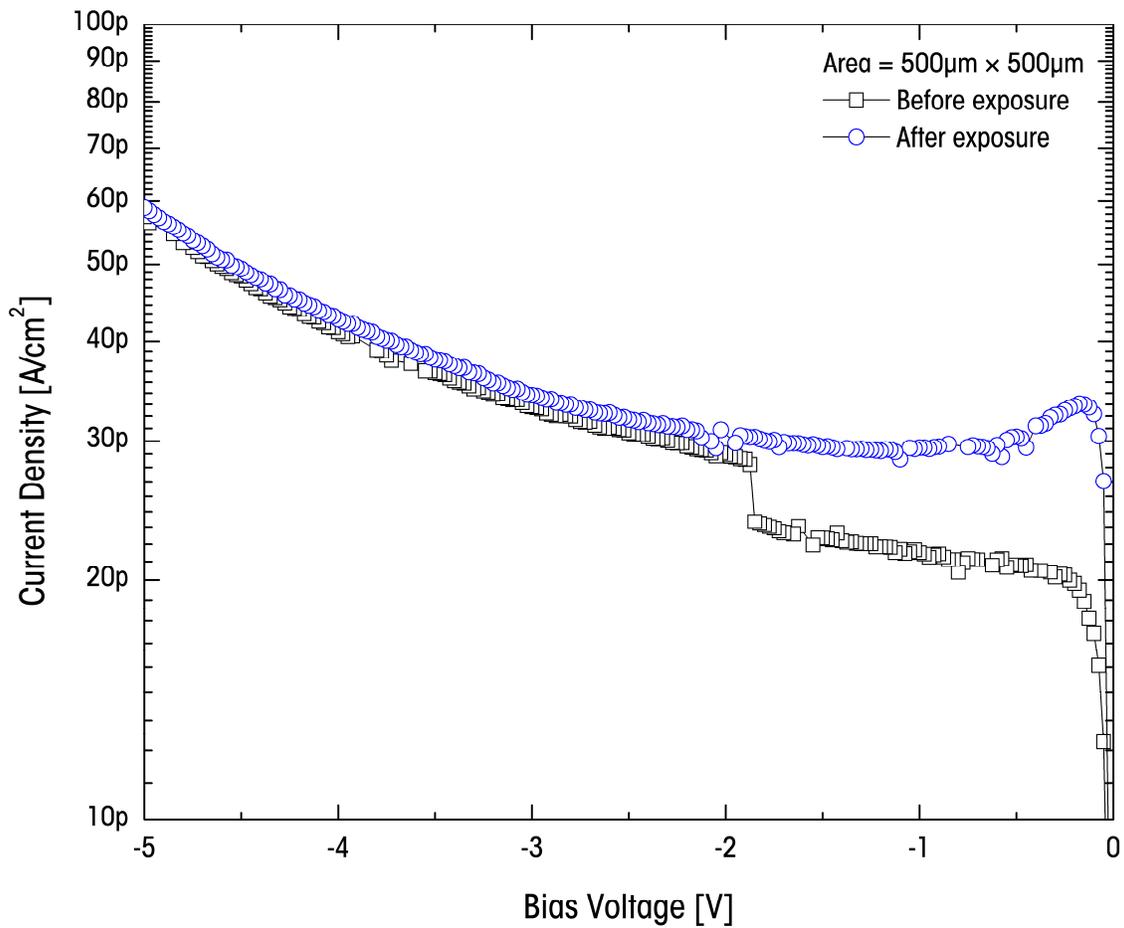


Figure 3-12: Reverse leakage current degradation test with UV light exposure on a 500×500μm² a-Si:H *n-i-p* photodiode. The sudden jump in the measurement is a measurement error due to relay switching.

The metastability effect discussed in Section 2.1.6 concluded that light-induced defect creations for faint signals are unlikely for the fluorescence-based bio-assay applications. Faint fluorescence signals do not provide enough energy to cause structural changes in the photodiode material. The higher energy UV light used to excite the fluorescent tags does not cause problems either. This issue is investigated by exposing $\sim 1.6\text{J}/\text{cm}^2$ of UV light on a $500\times 500\mu\text{m}^2$ photodiode. The measurement results are shown in Figure 3–12. Aside from the sudden jump at the lower bias region, there is no significant change in the leakage current level before and after exposure. The sudden jump at the lower bias region before exposure is caused by the feed-through charge of the switching relays inside the measurement system, which occurs when the range of measurement system is shifted. The small differences at higher reverse biases are due to measurement errors caused by slightly elevated room temperature. The higher current level at lower reverse bias region is due to the incomplete release of the trapped charge prior to the start of the measurement.

Current Transients and Illumination

The transient response of fabricated photodiodes under reverse bias is investigated, which provides information on the trap states. Short time experiments ($10^{-9}\sim 10^{-5}\text{sec}$) reflect the shallow states in the band-tails, while long time measurements are used to investigate deep states located in the midgap. The equipments used for transient analysis parallels those used for the quasi-static J_D-V characteristic measurements shown in Figure 3–10. The variation is in the necessity to incorporate a light source

as the stimulus with corresponding setup adjustments of the measurement system. The light source used is a 556nm green *light-emitting diode* (LED).

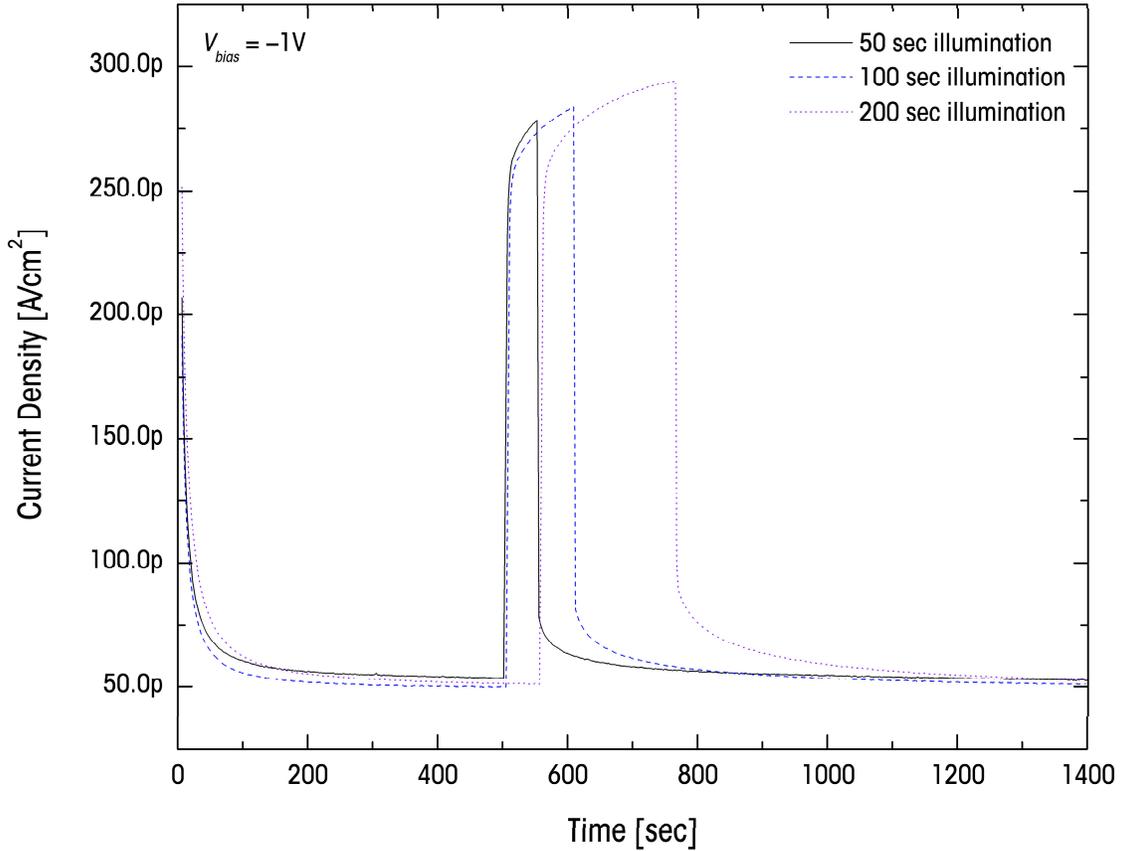


Figure 3-13: A plot showing the photocurrent transient for different illumination durations. The a-Si:H *n-i-p* photodiode is biased at -1V constantly.

The LED is mounted on a special cover built to fit the viewing window of the MicroChamber while having an opening for fixating an external controlled light source. The current through the LED is controlled by a set of resistances. A battery is used as the power source to minimize noise introduced by power fluctuations. The series resistances can be adjusted easily following the need of the experiment to obtain different luminosities.

The measurement system is also configured to run in sampling mode instead of sweeping mode to continuously acquire the diode currents at different times. A plot of the measurements obtained by the setup is shown in Figure 2-14.

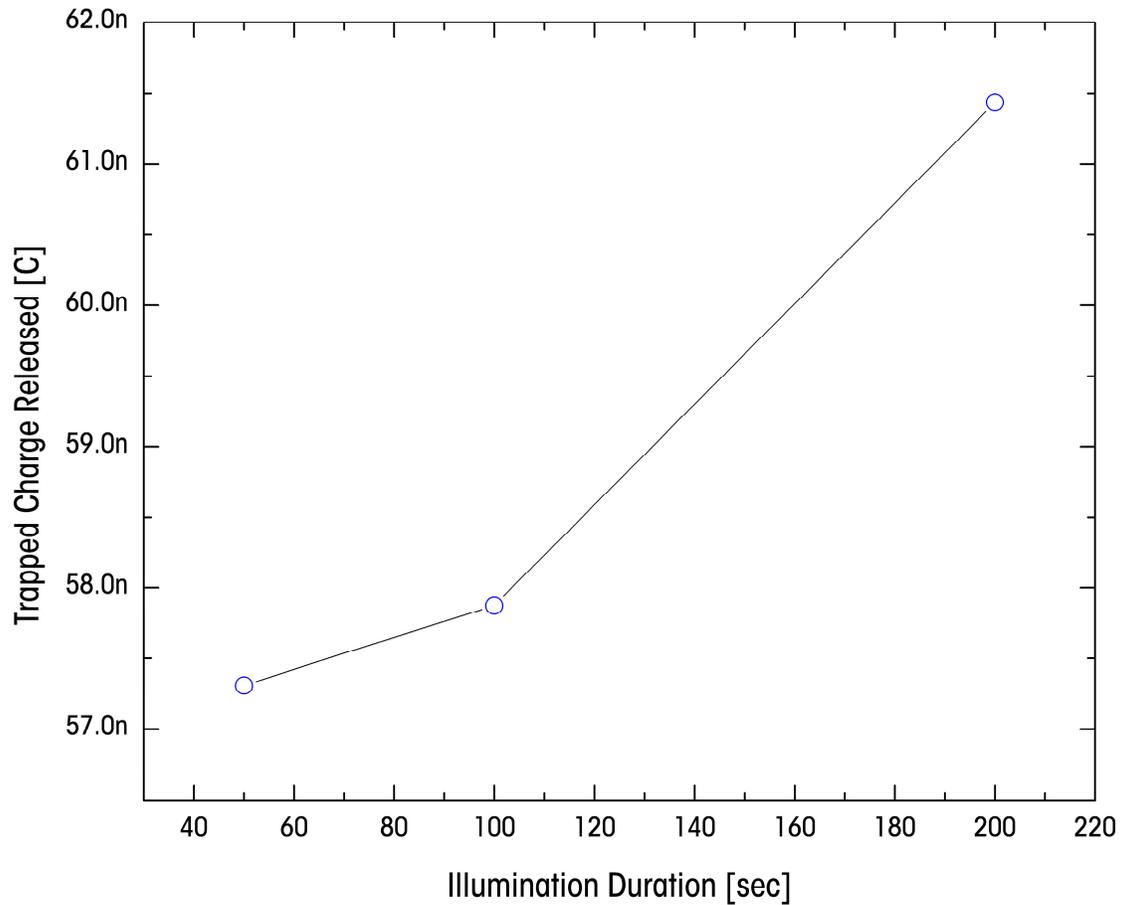


Figure 3-14: A plot of the released trap charge as a function of the illumination duration. The trapped charge increases with the increase in illumination time.

Figure 3-13 shows a plot of the transient response of the photodiode at different illumination periods biased at $-1V$. During the short period of time after the switch-on and switch-off of the LED, the photodiode current

changes rapidly. The rate of change during illumination and after illumination is indicated by the ramp-up and ramp-down of the photodiode current. At a given light intensity, the amount of trapped charge depends on the illumination time. As shown in Figure 3–14, the amount of trapped charge increases with an increase in illumination time.

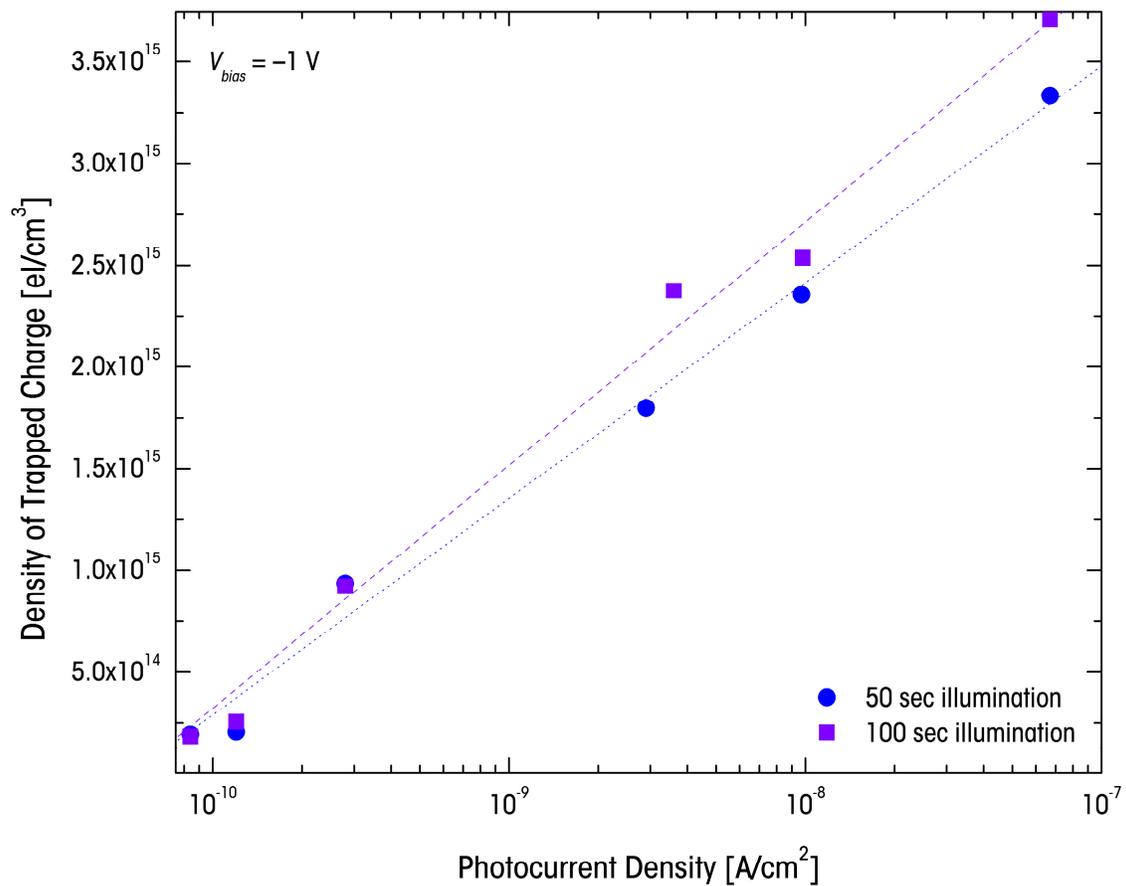


Figure 3–15: A plot of the density of trapped charge as a function of photocurrent. The photodiode is biased at -1V .

Figure 3–15 shows the density of the trapped charge as a function of photocurrent amplitude for two illumination durations. The density of

trapped charge is calculated by Equation (2.54). The density of trapped charge depends logarithmically on illumination intensity.

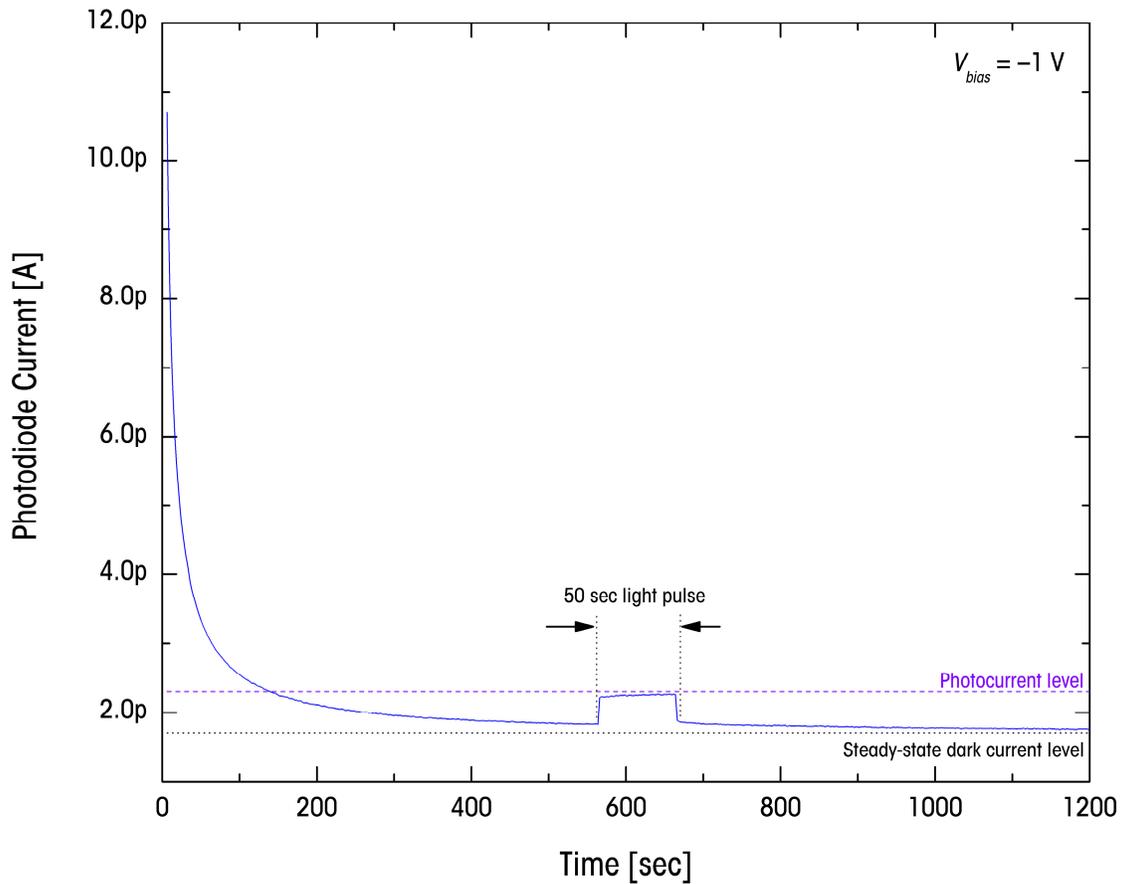


Figure 3–16: A plot of the photodiode transient response at very low illumination intensity. The photodiode is biased at $-1V$. The a-Si:H $n-i-p$ photodiode can potentially detect photocurrent lower than its dark current levels at zero bias.

An interesting result discovered from the intensity variation measurement is that at very low intensity illumination, charge trapping occurs quickly in the shallow states, indicated by the fast rise in photocurrent, shown in Figure 3–16. It differs from the graph shown in Figure 2–14 in that there is virtually no ramp-up time for the photodiode to reach the saturated

current levels. Furthermore, it falls back to the previous dark current level almost as quickly after the illumination is removed. The result shows that the fabricated a-Si:H *n-i-p* photodiodes are excellent for low light level detections. It can potentially detect photogenerated current levels that are even lower than the initial dark current levels. An important point to note here is that the photodiodes must first be initialized by placing them in reverse bias for some time to deplete all the initial trapped charge.

3.3 *Optimization*

The promising characterization results of non-optimized segmented a-Si:H *n-i-p* photodiodes indicate that using such device as the underlying detector for drug assays is definitely possible. This section unveils some of the further efforts placed in optimizing the a-Si:H *n-i-p* photodiodes. Two aspects of the photodiode characteristics are targeted: the reverse bias leakage current level and quantum efficiency. Results of only selected samples are reported since only a fraction of fabricated photodiode samples are functional. While optimizing the photodiode dark current, the fabrication parameters and device geometry parameters are assumed to be independent of each other to reduce the number of process runs. Such assumption is valid from experimental results since different photodiode sizes fabricated under the same process conditions yielded similar reverse dark current density. Therefore, the geometry of the device does not possess strong influences under the crucial dry etch process. Sequential

optimization was undertaken such that the parameter configuration yielding the best result is used for the subsequent steps.

3.3.1 Reverse Leakage Current

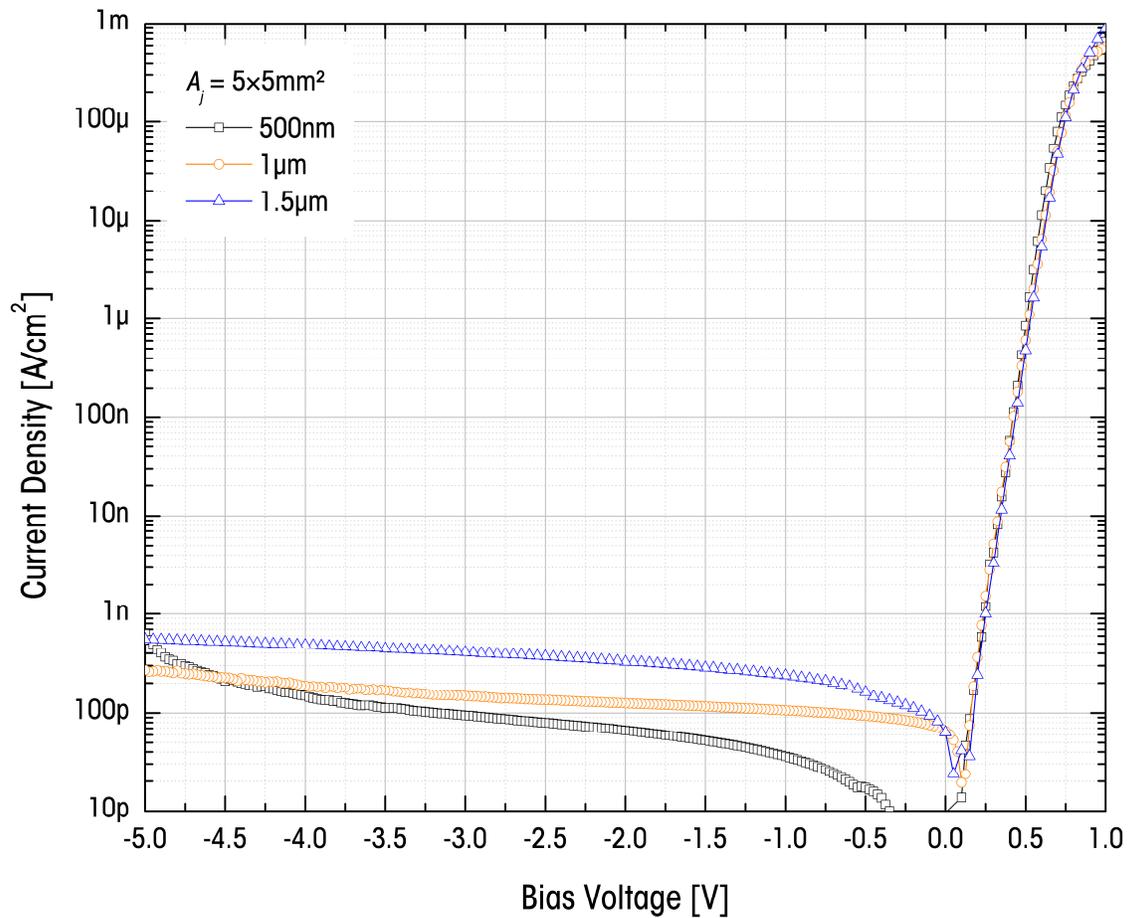


Figure 3–17: A plot of the quasi static J_D - V characteristics of large photodiodes with different intrinsic layer thicknesses. n - and p -layer thicknesses are 80nm and 50nm, respectively.

The motivations behind minimizing the photodiode leakage current have already been stressed, and the resulting efforts published from different groups are chronologically summarized in Table 2–4. The sources that

contribute to the reverse dark current are first introduced in Section 2.2.2. The fundamental lower limit of the dark current level is determined by the thermally-induced carrier emission in the bulk a-Si:H layer. Therefore, a-Si:H $n-i-p$ photodiodes with thinner i -layer is expected to have lower thermal generation current.

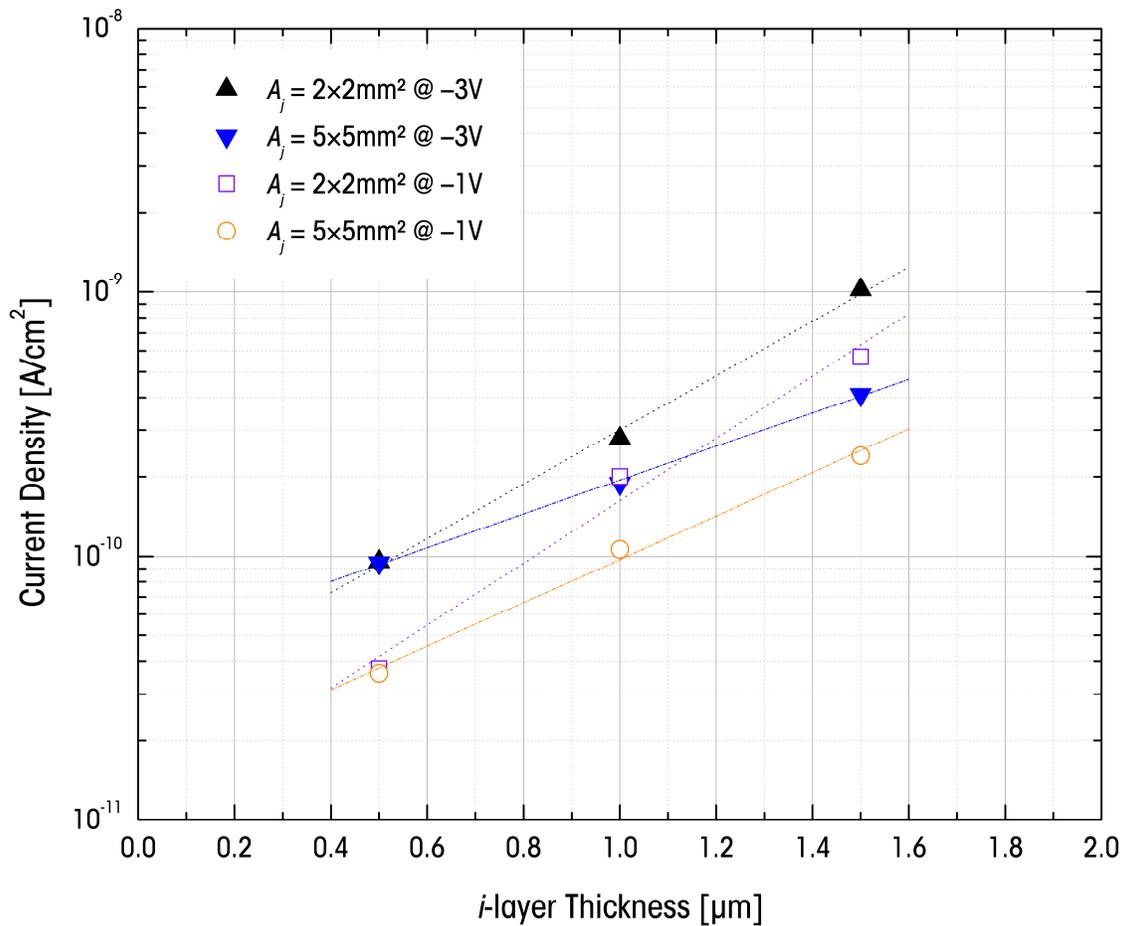


Figure 3-18: Extracted dark current levels at different biases for different intrinsic layer thicknesses. Dark current level varies monotonically with thickness.

Figure 3-17 shows the quasi-static J_D - V characteristics of photodiodes with three different intrinsic layer thicknesses. Large photodiodes are

chosen for the measurements to minimize the contribution of edge leakage sources toward the total dark current level. The plot shows that reverse bias current are indeed higher for thicker photodiodes. The increase in current level is less noticeable for larger photodiodes. Thinner photodiodes are also more prone to the change in electric field strength across the intrinsic layer; this is shown by the stronger bias dependence of the reverse dark current.

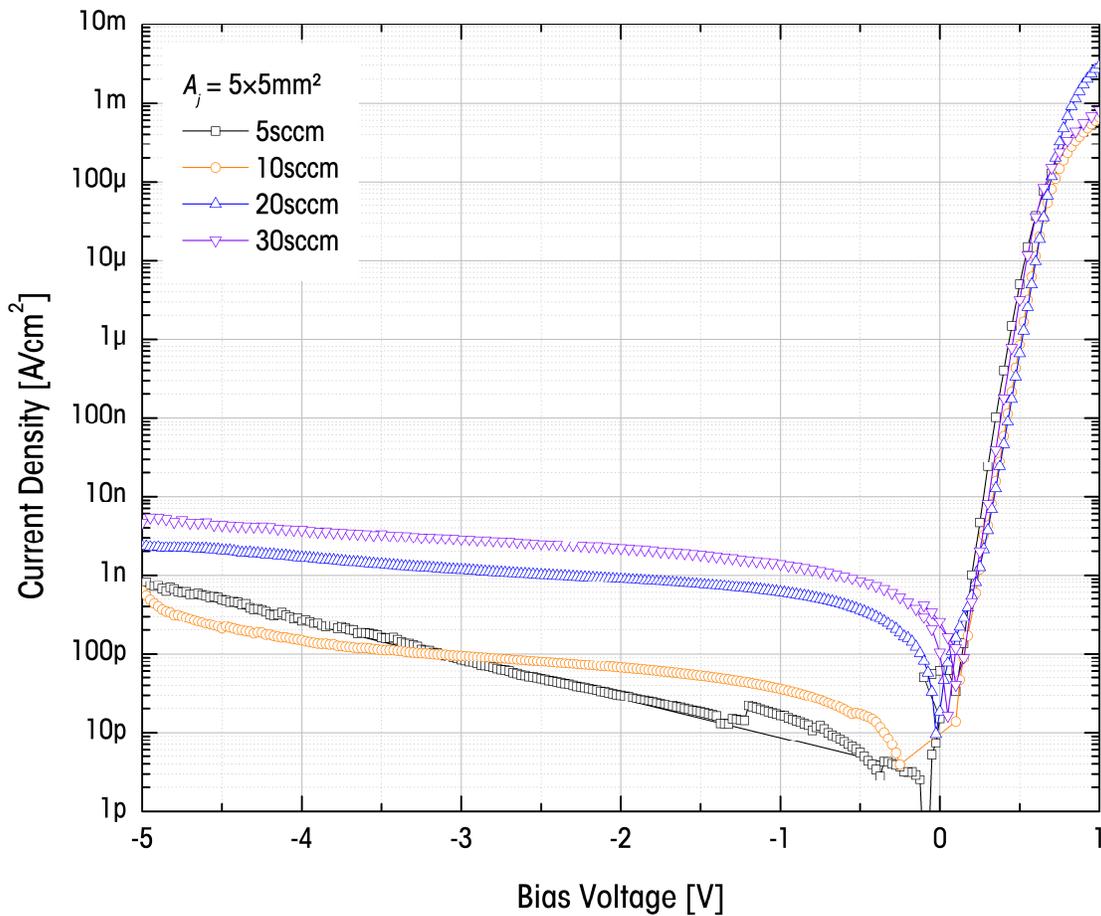


Figure 3–19: A plot of the quasi-static J_D - V characteristics of a-Si:H n - i - p photodiodes with different TMB flow rates during deposition. n -, i -, and p -layer thicknesses are 80nm, 500nm, and 20nm, respectively.

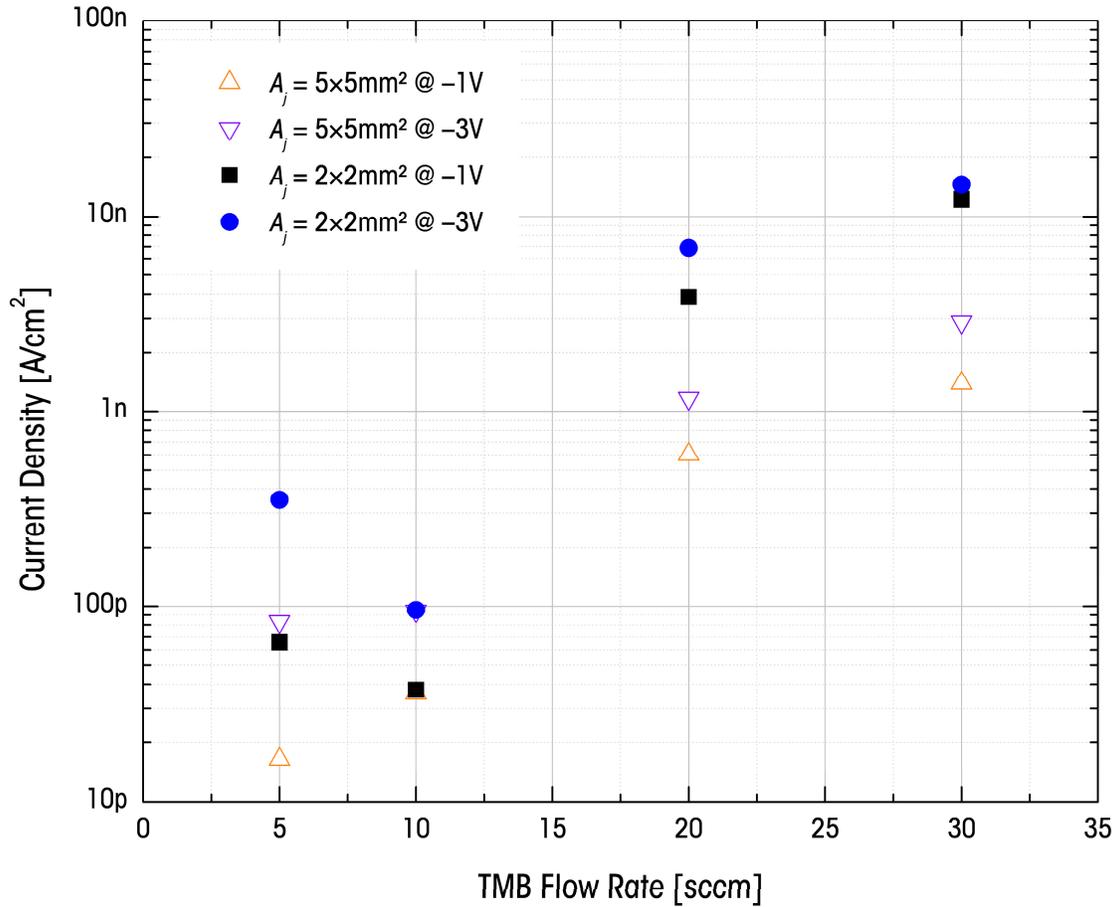


Figure 3-20: Extracted dark current levels at different biases for different TMB flow rates. Dark current is at the lowest level with 10sccm TMB flow rate during deposition.

The reverse bias dark current levels at two different voltage biases for two different photodiode sizes are extracted. The data displayed in Figure 3-18 indicates a non-linear dependence of dark current level on the thickness of the intrinsic layer. The quality of the $i-p$ interface also plays an intricate role on the dark current level of the sensor [56], [74]. The variation in the flow rate of the dopant gas, for example, can result in orders of magnitude difference in dark current level. Figure 3-19 shows the measured quasi-

static J_D - V characteristics of photodiodes deposited with different TMB flow rates. The plots indicate that the dark current level increases with increase in TMB flow rates. Lower flow rates also yield an inferior interface which again increases the dark current level at moderate reverse bias. Optimum TMB flow rate appears around 10sccm. Such trend is readily shown in Figure 3-20 where the dark current levels at particular biases are extracted for different TMB flow rates.

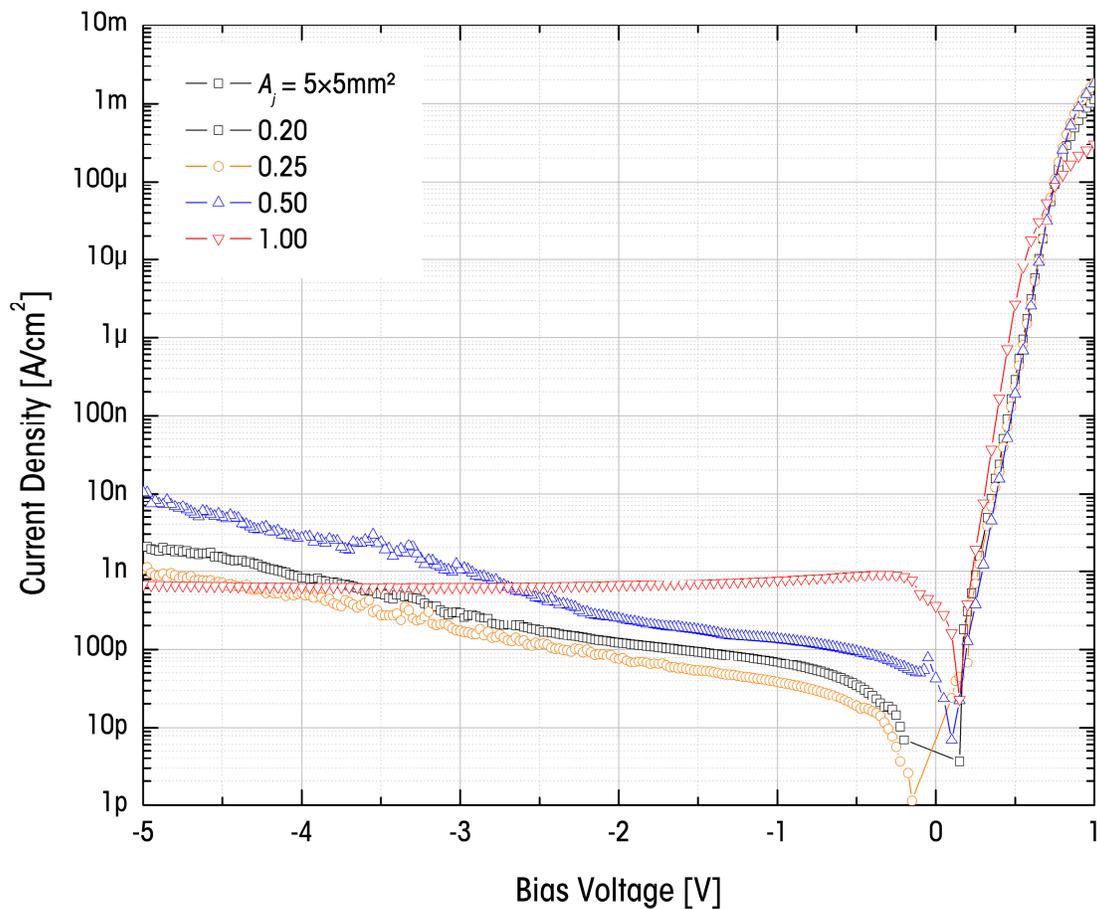


Figure 3-21: A plot of the quasi-static J_D - V characteristics of a-Si:H n - i - p photodiodes with different $\text{SiH}_4/(\text{H}_2+\text{SiH}_4)$ flow rate ratios during deposition. n -, i -, and p - layer thicknesses are 30nm, 500nm, and 20nm, respectively.

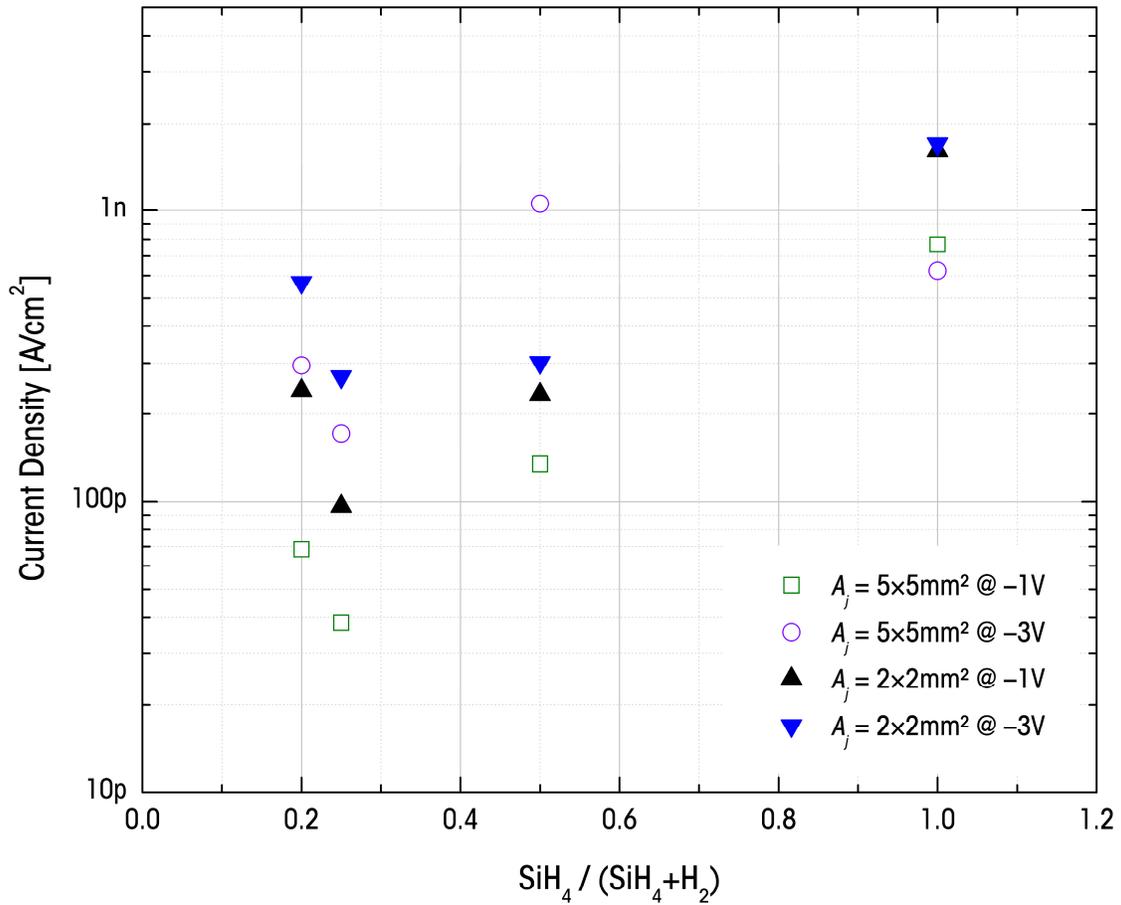


Figure 3–22: Extracted dark current levels at different biases for different silane and hydrogen flow rate ratios. Lowest dark current level is obtained with a ratio of 0.25 for low reverse biases.

The hydrogen and silane flow ratio also controls the dark current level of the photodiode. The role of hydrogen during deposition is to mediate the formation of the silicon random networks by removing weak bonds while terminating dangling bonds. Flow ratio ultimately affects the growth morphology of the photodiode material layers and their quality. Figure 3–21 shows a plot of the J_D - V characteristics of photodiodes with different

deposition gas ratios and Figure 3–22 shows the extracted data to obtain the trend. The results indicates that $\text{SiH}_4/(\text{H}_2+\text{SiH}_4)$ ratio of 0.25 yields the lowest dark current level at low biases. An increase in the flow ratio increases the dark current exponentially.

As photodiode sizes decrease, the leakage current contribution from the edges of the photodiode increases. For a-Si:H *n-i-p* photodiode sizes below $1\times 1\text{mm}^2$, the edge leakage current contribution may hold a non-negligible portion of the total current. To minimize this effect, the processing conditions during RIE dry etching are extremely important. The trade-off is on the power provided to the RIE chamber. Higher power RIE yields a faster etching rate to minimize the amount of time the sample spends in the plasma. However, higher power plasma also implicates heavier ion bombardments on the sample. The quality of the segmented *n-i-p* stack sidewall suffers significantly where heavier bombardments create additional defect states. Therefore, RIE etching process should be done at lower power and low base pressure to achieve desired anisotropic etch and impose minimum damage on the photodiode sidewalls. The leakage mechanisms caused by unavoidable damages on the photodiode sidewalls can be reduced by passivating the dangling bonds with silicon nitride with follow-up annealing processes.

3.3.2 *Quantum Efficiency*

Optimizing the quantum efficiency of the photodiode withhold a slightly different goal than leakage current level optimization. While it is desired to

have the lowest leakage current level for any input signal, the quantum efficiency ought to be maximized at the targeted wavelength of the impinging photons while suppressing signals from other wavelength ranges. For the fluorescence-based bio-assay applications, the optimization criteria depends on the tagging material. Cy3 is a commonly used dye for proteomics which emits maximally at ~550nm while Cy5 tags emits maximally around ~670nm. Therefore, the device needs to be optimized to respond maximally at the desired wavelength.

Generally, the quantum efficiency of a-Si:H *n-i-p* photodiode depends on factors such as the optoelectronic properties of the doped and intrinsic layers, the corresponding layer thicknesses, and the quality and optical properties of the front and backside interfaces. Partial optimization is achieved by adjusting the layer thicknesses of the top contact where the light signal enters. The top contact include the *p*-type a-Si:H layer, the ITO TCO layer, and the a-SiN_x:H AR coating layer.

Figure 3-23 shows a plot of the quantum efficiency measured from a-Si:H *n-i-p* photodiodes with different *p*-layer thicknesses [70]. The plot shows that the short wavelength quantum efficiency is limited by the optical absorption in the doped layer. By thinning the *p*-layer from 45nm to 25nm, short wavelength response at 400nm can be enhanced from 14% to 30% while keeping the leakage current level unchanged. The peak efficiency at 560nm also changes from 76% to 82%. Therefore, to improve the overall quantum efficiency, the *p*-layer should be made as thin as

possible while still retain enough dopant charge to compensate for the work function difference at the contact.

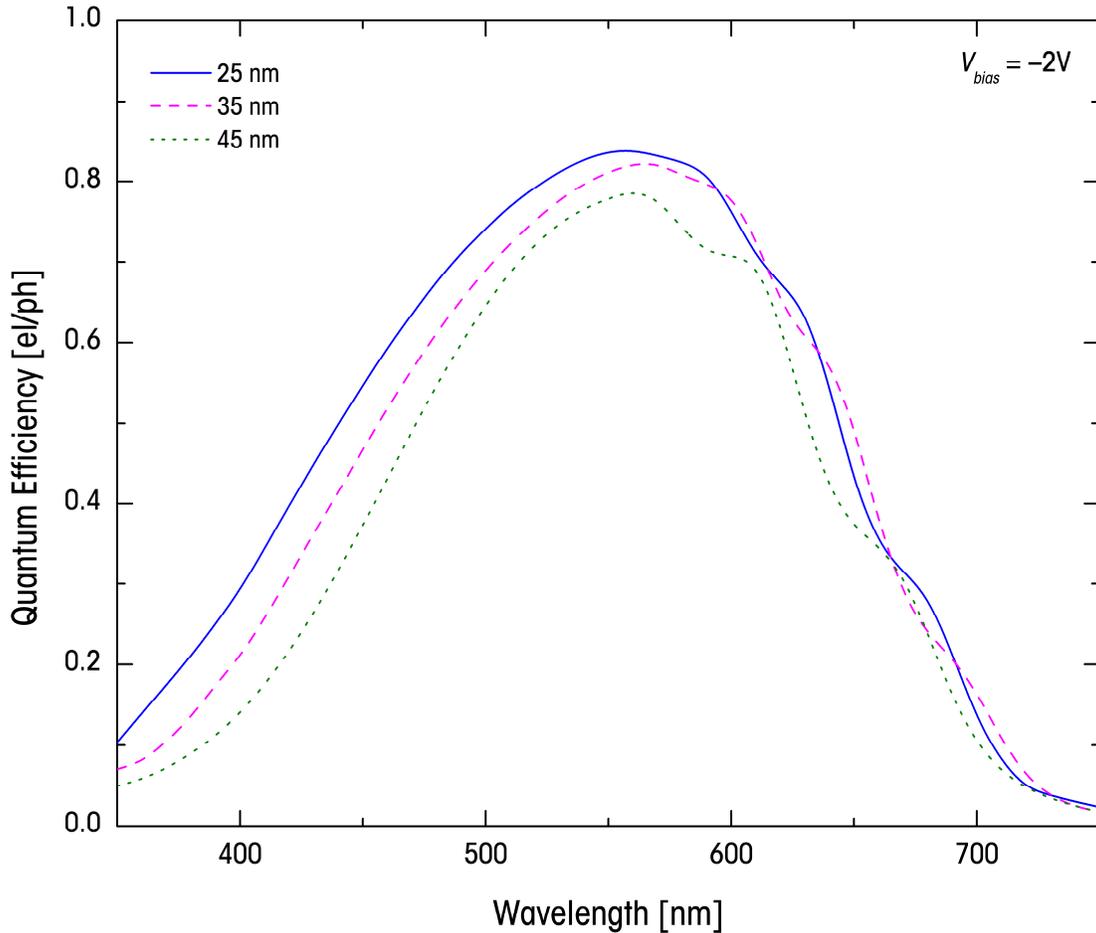


Figure 3–23: Quantum efficiency plot of the a-Si:H *n-i-p* photodiodes deposited with different *p*-layer thicknesses. The peak efficiency at 560nm improves from 76% to 82% by thinning the *p* layer from 45nm to 25nm [70].

The combination of the transparent a-SiN_x:H and ITO film also serves as an AR coating where the spectral response of the photodiode can be controlled by adjusting the thicknesses of these films. Alteration to the thickness of the ITO film is restricted to a limited range. In practice, the

thickness of the ITO layer can only be varied between 50nm and 90nm. Thinner ITO layers yield undesired high resistances that hinders the performance of the device if it is integrated into a large area array. Thicker ITO layers on the other hand yield photodiodes with cracks due to stress. Therefore, the desired option is to keep the thickness of the ITO layer fixed and change the thickness of the a-SiN_x:H AR coating to minimize reflection losses. To tackle this issue, the optical properties of the device interface are analyzed using an IMD computer program [97]. The optical constants used for numerical simulations are determined from ellipsometry data of thin films deposited on Corning 7059 glass and crystalline silicon substrates. Measurements are performed using the J. A. Woollam Co. ellipsometer and the collected data are analyzed with the WVASE32 software.

Figure 3–24 shows the calculated reflectance (R_x) and transmittance (T_x) as a function of wavelength in the range of interest [98]. Calculations are performed for a-SiN_x:H film thickness between 80nm and 110nm, while the thicknesses of the ITO and *p*-layer are kept constant at 70nm and 25nm, respectively. Numerical calculations show that the reflectance loss can be minimized to 1–2% at a given wavelength by adjusting the thickness of the a-SiN_x:H film; however, the light absorption in the *p*-layer film remains to be the main limiting factor for reduced transmittance below 500nm.

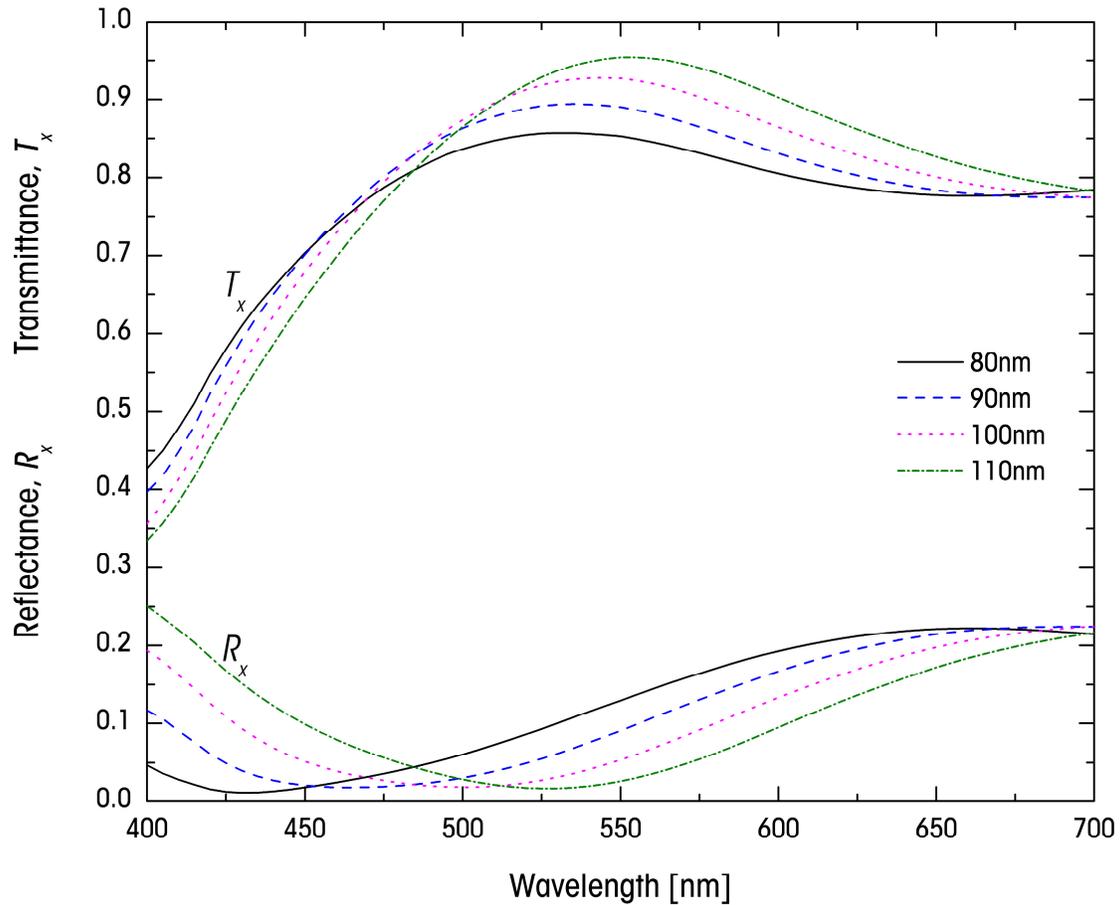


Figure 3-24: Calculated reflectance and transmittance of the a-SiN_x:H/ITO(70nm)/p-a-SiC:H(25nm)/a-Si:H interface for different a-SiN_x:H film thicknesses [98].

Figure 3-25 shows the quantum efficiency spectra measured for two different a-Si:H *n-i-p* photodiodes with a-SiN_x:H AR layer thicknesses of 80nm and 110nm. The photodiodes are deposited with the same process sequence. Photodiodes with 110nm thick a-SiN_x:H layer have an overall higher efficiency in the long-wavelength region and lower efficiency in the short-wavelength region. The efficiency peak also shifts toward shorter wavelength with decreasing a-SiN_x:H thickness. The short-wavelength section of the curve correlates well with the corresponding transmission

spectra in Figure 3–24. The quantum efficiency of 34% at $\lambda=400\text{nm}$ is close to the calculated transmittance (36%) at the same wavelength.

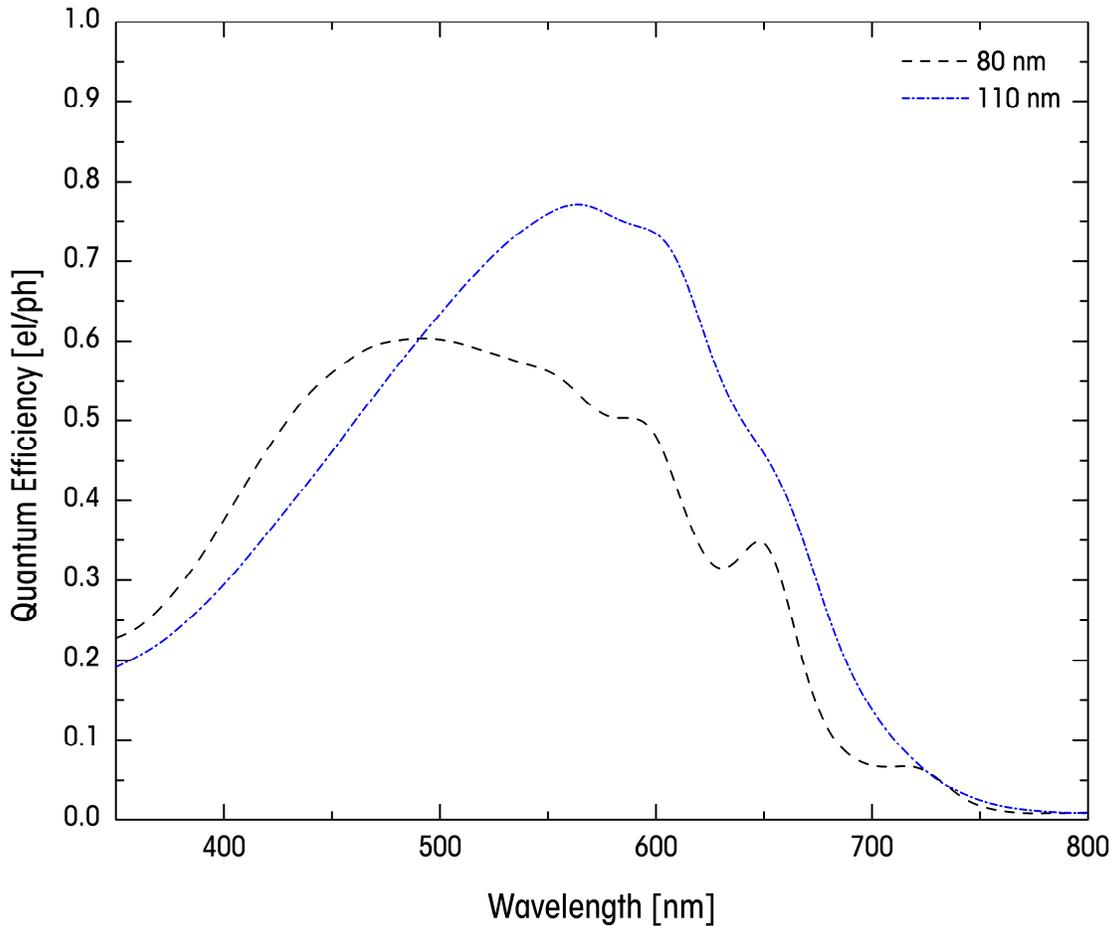


Figure 3–25: Quantum efficiency plot of the a-Si:H *n-i-p* photodiodes deposited with two different a-SiN_x:H layer thicknesses.

At longer wavelengths, increase in the difference between the quantum efficiency and transmittance is probably due to changes in the collection efficiency. The quantum efficiency reaches a peak value of 80% at $\lambda=558\text{nm}$ and subsequently degrades due to decreasing absorption in the *i*-layer. Coarse adjustments of the peak efficiency wavelength cannot be

done without compromising the overall quantum efficiency, but fine adjustments can be done by calculating layer thicknesses using computer software.

Chapter 4: Compact Model of a-Si:H *n-i-p* Photodiodes

It is evident that during the design phase of a detector system, an accurate model of the detector can play an imperative role in determining the performances of the detector system and ascertain design issues before production. The level of abstraction of the model may range from parameter extractions with measured empirical data to pure theoretical models formulated with device physics concepts. Numerical solutions are often based on different assumptions on the material parameters and on the structures themselves, thus preventing conclusions with general validity and unified view of the results. Furthermore, the complexity of the model and time consuming computations inhibits the possibility of discriminating the exact effect of large number of parameters on the overall photodiode behaviour [99]. Analytical model, which also falls in the category of theoretically modeling, offer a deeper comprehension of the structure; therefore, achieving a complete control on the various parameters and on defining their role of the device operation. The limitations of the analytical models, however, lay in the need for simplified assumptions in the model physics, which may only be accepted in order to reduce complexity in calculations.

Many a-Si:H photodiode numerical and analytical models have been presented [99]–[106]. These models require the simultaneous solution of a complete set of transport equations, which includes the one-dimensional electron and hole continuity equations,

$$\frac{1}{q} \frac{dJ_n}{dz} = G(z) - R(z) \quad (4.1)$$

$$\frac{1}{q} \frac{dJ_p}{dz} = G(z) - R(z) \quad (4.2)$$

and the Poisson's equation,

$$\frac{d\xi}{dz} = \frac{\rho(z)}{\varepsilon} \quad (4.3)$$

$G(z)$ and $R(z)$ are the respective generation and recombination rate along the thickness axis (z) of the photodiode. J_n and J_p are the electron and hole conduction current densities expressed as

$$J_n = q\mu_{de} \left(n\xi + \frac{k_B T}{q} \frac{dn}{dz} \right) \quad (4.4)$$

$$J_p = q\mu_{dh} \left(p\xi + \frac{k_B T}{q} \frac{dp}{dz} \right) \quad (4.5)$$

To find the space charge density $\rho(z)$ and the recombination rate, one must consider the electron and hole concentrations n and p as well as the distribution of localized states, given in Equation (2.1) and (2.2).

In contrast, empirical models sometimes lack the elucidation of the underlying theory of operation provided by the theoretical models. Despite this frailty, empirical models can be authored quickly and is sufficiently accurate for matured fabrication processes. They are often

preferred with its faster simulation time and simpler parameter extraction processes.

This chapter presents the formulation and implementation of a physical-based compact model for a-Si:H *n-i-p* photodiodes fabricated in-house. The photodiode model may be used for simulating the high throughput bio-assay detector system. The parameter extraction processes of the physical model parallels those of the empirical models while still implicate the physical phenomena of the device with equations formulated via device physics. Verifications of the model are given in the final section of this chapter to demonstrate its integration with the widely used Cadence Spectre circuit simulator.

4.1 *Photodiode Model Formulation*

This section presents the formulation of the photodiode model, independent of its implementation method. It must be emphasized that the parameter extraction procedures, rather than the data themselves, are important. The immediate objective is to create a black-box model with all the necessary input parameters. Figure 4-1 annotates the schematic symbol for the model. Note that although the physical photodiode is a two-terminal device (shown on the left of the figure), two additional terminals are needed in the model to account for illumination on the photodiode (shown on the right of Figure 4-1). The behaviour of the black-box is improved in four different stages; each stage includes additional features to fine tune the accuracy of the model. In the first stage,

an empirical model is implemented for the quasi-static dark I_D - V characteristics of the fabricated photodiodes. In the second stage, the photodiode capacitance is incorporated as well as photocurrent generation effects. In the third stage, the charge-trapping behaviour of dark current is implemented. The final stage models the temperature dependence of the photodiode characteristics.

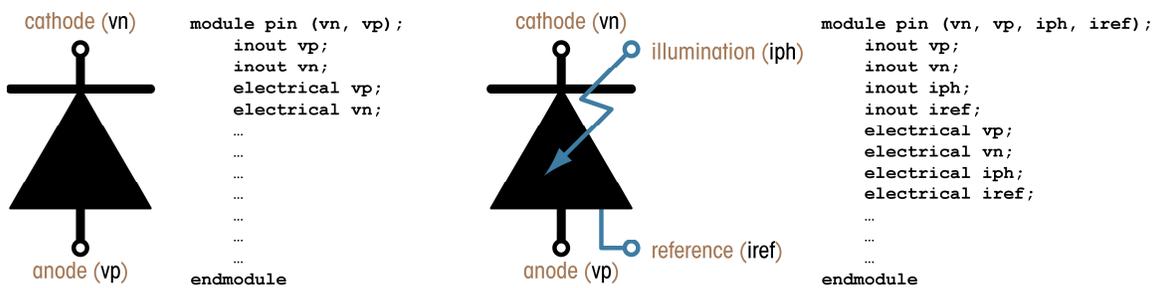


Figure 4-1: Schematic symbols and Verilog-A syntax for a-Si:H p - i - n photodiode models. The right symbol has an extra terminal for illumination simulation.

The dark quasi-static J_D - V characteristics model require a number of measurements on fabricated a-Si:H n - i - p photodiodes of various sizes. The measurement system parallels those used for the preliminary characterizations to fine tune the photodiode fabrication: a Keithley SCS2000 semiconductor characterization system with remote pre-amplifiers. The system can measure current level down to ~ 10 fA. An open probe test is done to measure the noise of the probes and integrated test environment; the result is shown in the inset graph of Figure 4-2.

Due to the notorious time-dependent dark current behaviour, care is taken while performing the measurements. An initial delay of 10–600sec is given before the initial bias. In between each measurement point, a 2–10sec

delay is also introduced. The integration time for the remote amplifiers and the internal *complex programmable logic device* (CPLD) is placed in low-noise settings to suppress unwanted noise. One result of the measurements performed on $250 \times 250 \mu\text{m}^2$ photodiode is shown in Figure 4-2. To simplify the modeling task, the forward and reverse bias characteristics are modeled separately, and then combined after.

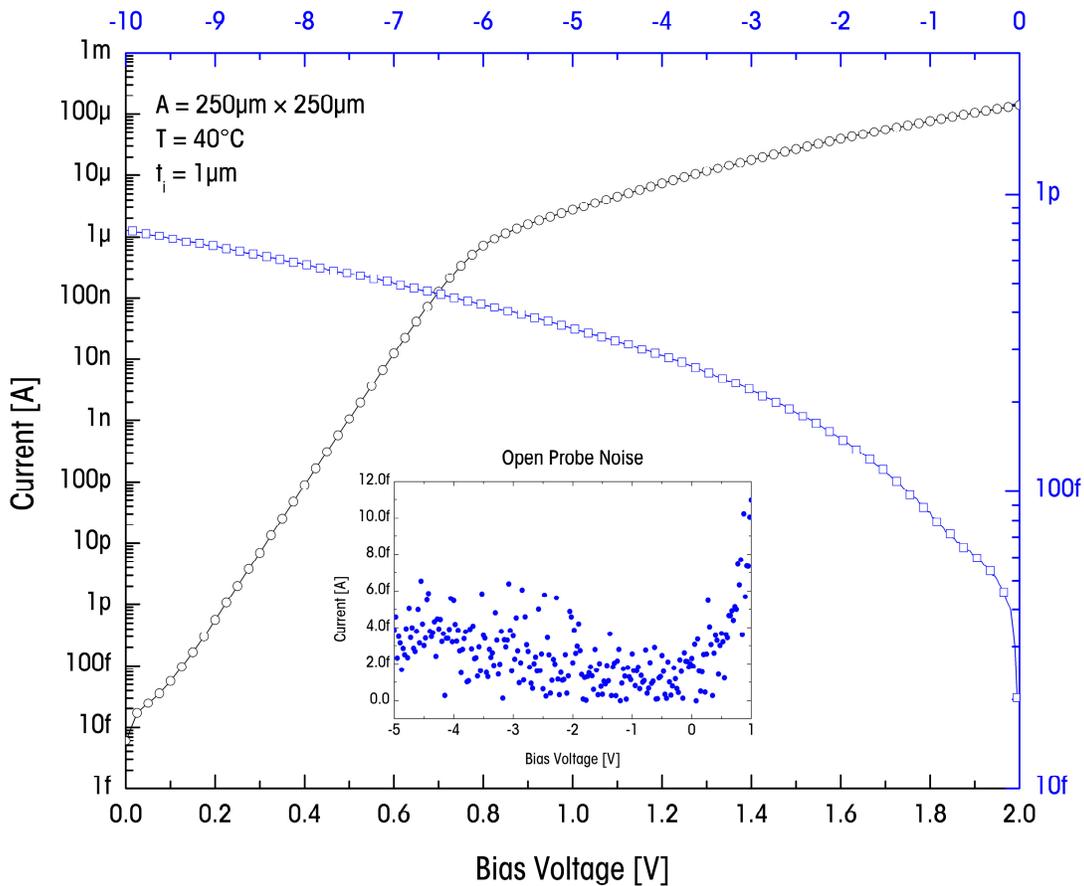


Figure 4-2: Current-voltage characteristics of a $250 \times 250 \mu\text{m}^2$ a-Si:H *n-i-p* photodiode, plotted in a semi-logarithmic scale. The inset graph shows the result of the open probe test to evaluate the instrumentation noise of the measurement setup.

4.1.1 Forward Bias

Figure 4–3 shows the forward J_D - V characteristics of square photodiodes with sizes ranging from $1 \times 1 \text{ mm}^2$ to $126 \times 126 \mu\text{m}^2$. The well matched curves indicate that the forward current scales with the photodiode size (A_j); that is $I_D = A_j J_D$. If an equation can be found to describe the current density of the photodiode, the photodiode current for any sizes can also be readily calculated.

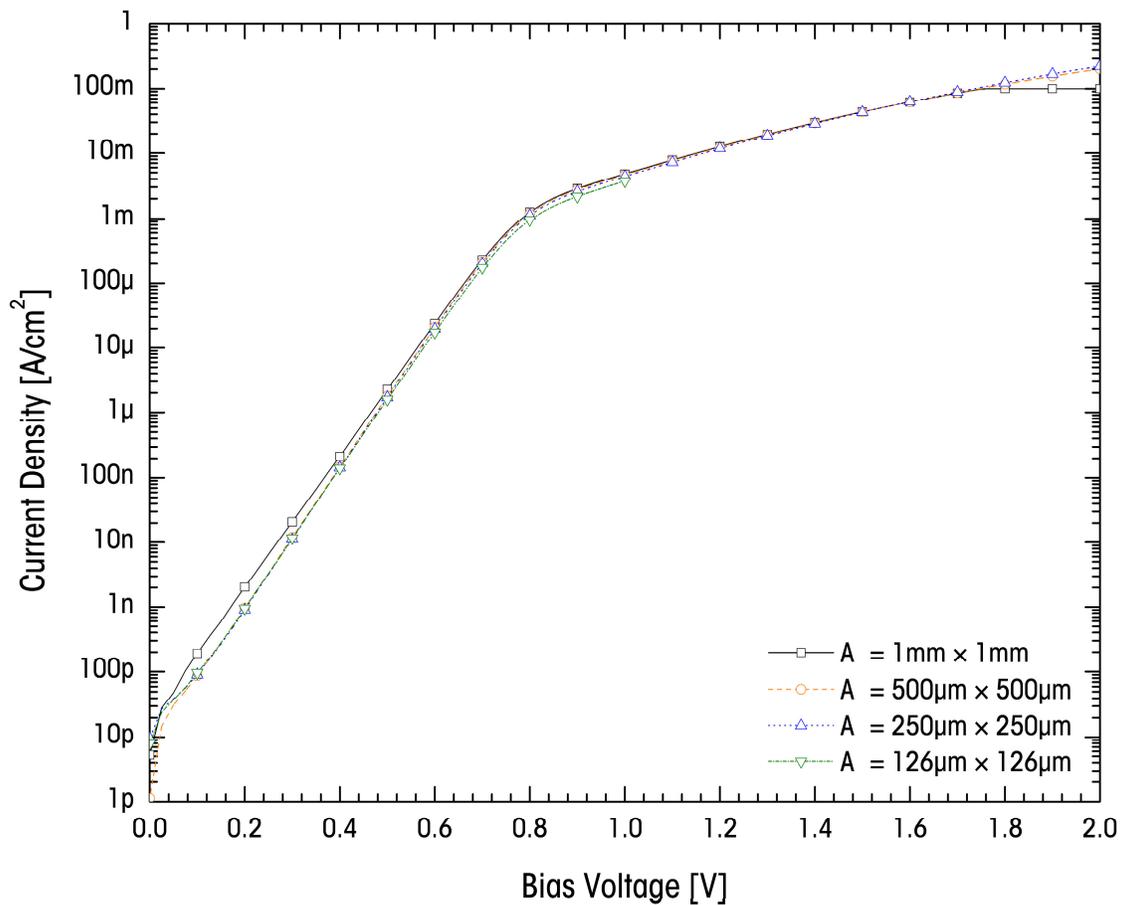


Figure 4–3: Forward current-voltage characteristics of a $250 \times 250 \mu\text{m}^2$ a-Si:H n - i - p photodiode, plotted in semi-logarithmic scale.

It is apparent in Figure 4–3 that the forward bias current density falls into three regions of operations: low, medium and high forward biases. At low forward biases (0.05–0.60V), the photodiode current increases exponentially with voltage since it appear as a straight line in the semi-logarithmic plot. This confirms the physics presented in Section 2.2.2; in particular, Equation (2.26). Due to series contact resistance however, this relationship is not maintained and the current starts to deviate from the ideal exponential behaviour at moderate bias voltages (0.60–0.80V). The photodiode current continues to increase at high forward bias voltages, but at a much slower rate. The recombination mechanism becomes apparent since the large trapped spaced-charge density often exceeds free-carrier density by orders of magnitudes [107].

Low Forward Biases

In this region, the J_D - V relationship follows the ideal junction equation in the form of an exponential

$$J_D(V_a) = J_{ol} \left[\exp\left(\frac{qV_a}{n_l k_B T}\right) - 1 \right] \quad (4.6)$$

J_D is the photodiode current density, V_a is the voltage applied to the photodiode terminals, q is the elementary charge, and k_B is the Boltzmann's constant. J_{ol} and n_l are the saturation current density and photodiode diode ideality factor, respectively; the subscript l indicates that these parameters are valid only in the low biasing regime.

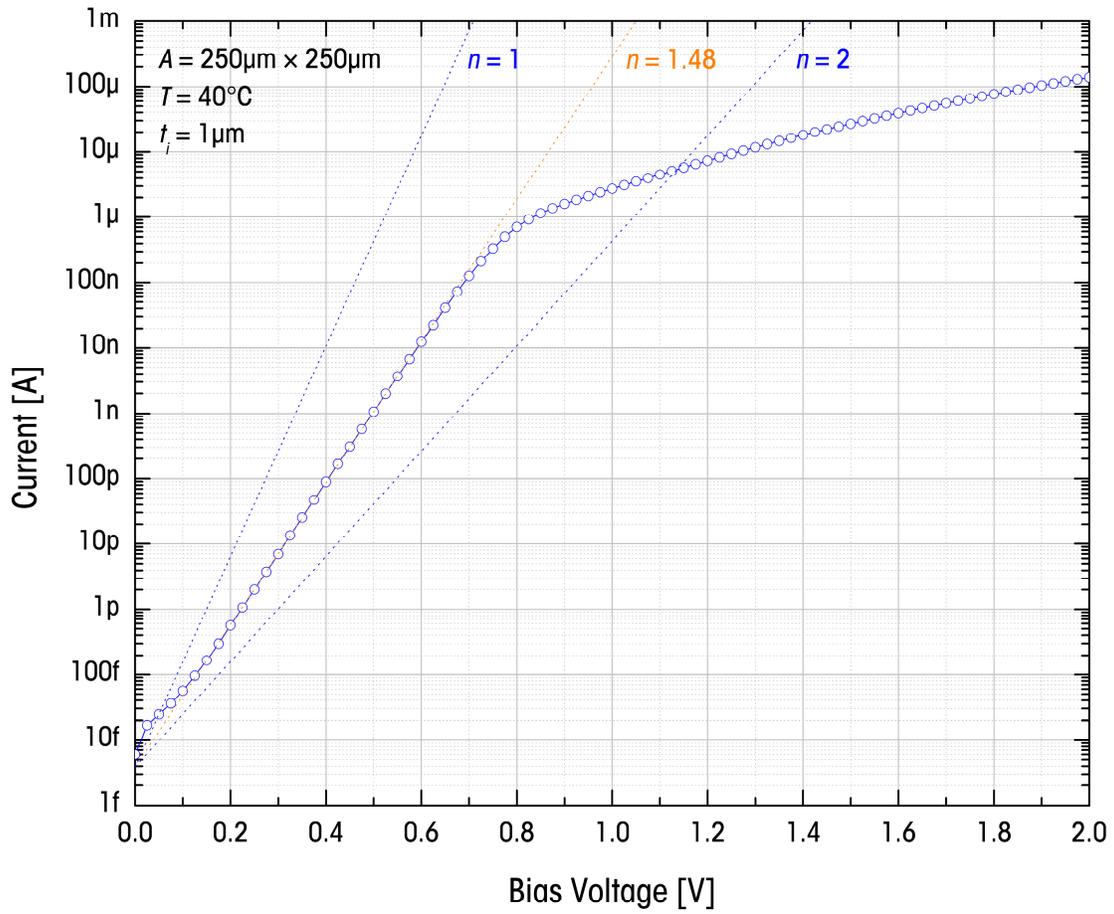


Figure 4-4: Parameter extraction for low forward bias region. Ideality factor of $n=1$ (thermionic emission) and $n=2$ (recombination) are also plotted with the extracted ideality factor n_i .

To extract J_{ol} and n_i , the measured values are first plotted in semi-logarithmic graphs, as shown in Figure 4-4. The exponential equation (4.6) consequently modifies to

$$\underbrace{\log|J_D(V_a)|}_Y = \underbrace{\log|J_{ol}|}_B + \underbrace{q \log e (n_i k_B T)^{-1}}_M \underbrace{V_a}_X \quad (4.7)$$

With the appropriate substitutions, the equation now deals with linear parameters which can be extracted via linear regression on the measured values. B is the y -axis intercept and M is the slope. Note that at zero bias, the diode current is zero; therefore, the offset current should be subtracted prior to the extraction of the parameters. The extracted parameters need to be mapped back to the original exponential equation. The combination of Equation (4.6) and (4.7) gives

$$\begin{aligned} J_{ol} &= 10^B \\ n_l &= \frac{q \log e}{k_B T M} \end{aligned} \quad (4.8)$$

Figure 4-4 shows a result of such extraction for a $250\mu\text{m} \times 250\mu\text{m}$ photodiode. Extracted parameters B and M , and diode parameters J_{ol} and n_l are lists in Table 4-1.

Medium Forward Biases

For medium forward biases, the series contact resistance (R_s) reduces the effective voltage across the photodiode. The current reduction ratio is

$$\exp\left(\frac{qI_D R_{\square}}{n_l k_B T A_j}\right) \quad (4.9)$$

where R_{\square} is the square series contact resistance and $R_s = R_{\square}/A_j$. With the measured current, the series resistance can be extracted by

$$R_{\square} = R_s A_j = \frac{A_j}{I_D} \left(V_a - \frac{q}{n_l k_B T} \ln \left| \frac{I_D}{I_{ol}} \right| \right) \quad (4.10)$$

for different bias voltages. The extracted values near the medium bias region are averaged. Figure 4–5 shows two I_D - V characteristics: one with extracted R_s and the other without. One can see that between 0.6V and 0.7V, the equation that incorporated R_s matches closer to measured results.

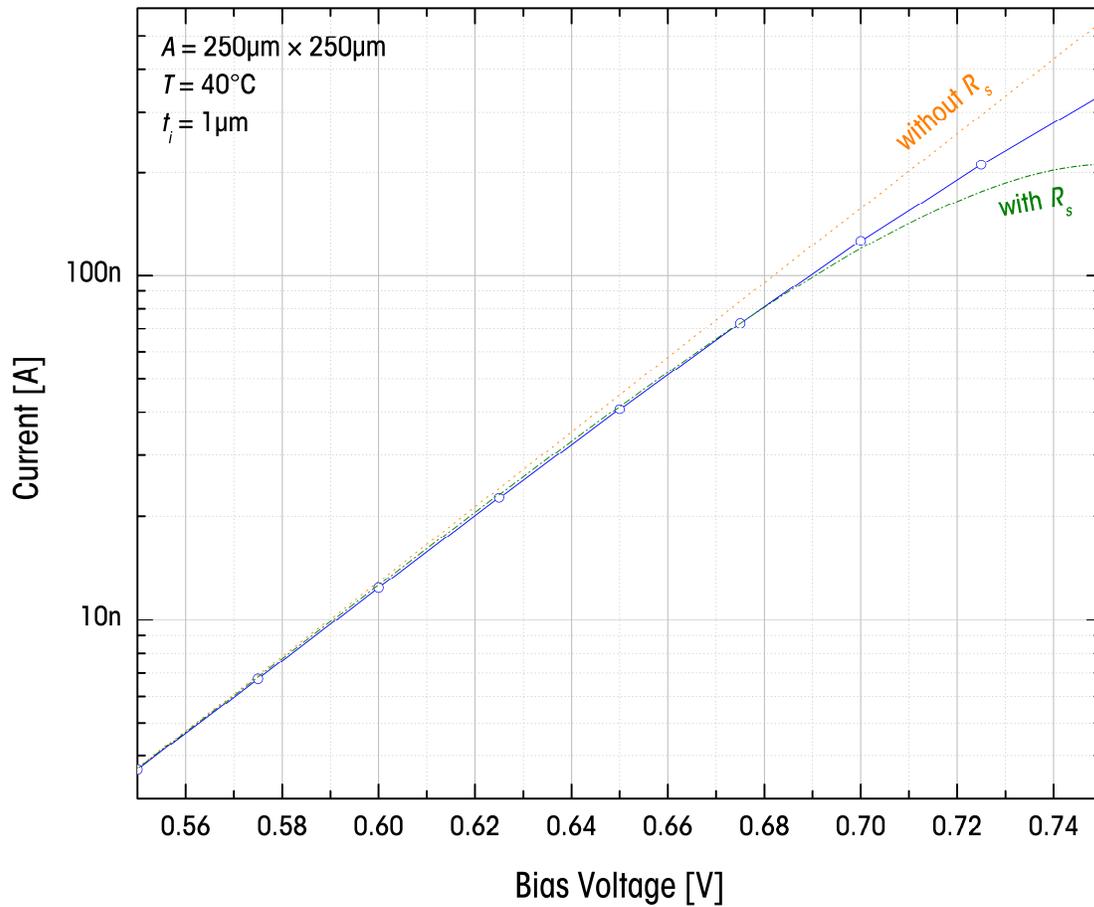


Figure 4–5: I_D - V characteristics near medium forward bias region deviates from the ideal exponential characteristics due to series contact resistance. Equations that incorporated R_s give better matches to the measured results.

High Forward Biases

In the high forward bias regime ($>1.0\text{V}$), the current-voltage characteristics follows a power relationship in the form of

$$J_D = J_{oh} V_a^{n_h} \quad (4.11)$$

J_{oh} and n_h are power-law factors that can be extracted graphically for I_D - V data measured larger than 1.0V, as shown in Figure 4-6.

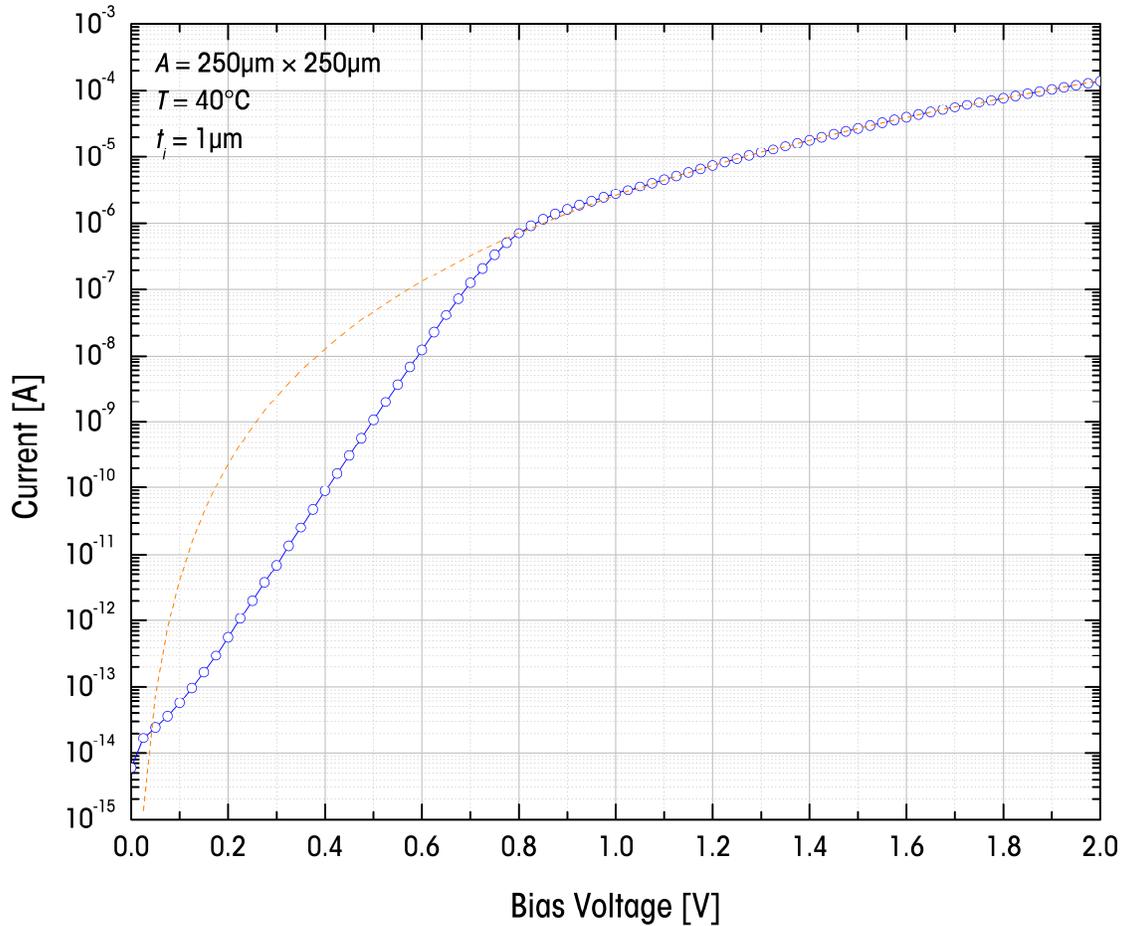


Figure 4-6: Parameter extraction for high forward bias region. The I_D - V plot follows a power law relationship.

The measured data are plotted in a double-logarithmic graph. The model equation consequently modifies to

$$\underbrace{\log|J_D|}_Y = \underbrace{\log|J_{oh}|}_B + \underbrace{n_h}_M \underbrace{\log|V_a|}_X \quad (4.12)$$

Linear regression is performed again on the graph to yield parameters B and M . They translate back to the power-law parameters via

$$\begin{aligned} J_{oh} &= 10^B \\ n_h &= M \end{aligned} \quad (4.13)$$

Region Weighting Function

Table 4-1: A list of parameters extracted from J_D - V characteristics in different forward bias regimes.

Regions	Parameters	Extracted Value
$0 < V < 0.60$	B	-14.407
	M	10.863
	J_{ol}	6.259×10^{-12} [A/cm ²]
	n_l	1.481
$0.60 < V < 1.00$	R_{\square}	40.745 [Ω -cm ²]
$1.00 < V$	B	-5.590
	M	5.789
	J_{oh}	4.106×10^{-3} [A/cm ²]
	n_h	5.789

Table 4-1 consolidates the results of the parameter extractions for the data shown in Figure 4-3. Even though the region selection process for some simulators can be done using available software constructs, the extremity values of different biasing regions still change abruptly. It is generally a good practice to program smooth continuous functions whose derivatives are also continually differentiable. To achieve this for the model, an appropriate weighting function is used to combine all three regions. The weighting function is chosen to be in the form of

$$f(V_a) = \frac{1}{1 + \exp[f_p(V_a - f_q)]} \quad (4.14)$$

f_p and f_q are the scaling parameter and center parameter of the weighting function, respectively. f_p governs the smoothness of the transitions between different regions, and f_q governs the center voltage where the transition actually occur.

Combining the aforementioned equations, the quasi-static forward I_D - V characteristics can be described by

$$J_D = \frac{J_{ol} \exp\left(\frac{qV_a}{n_l k_B T}\right)}{1 + \exp[f_{pl}(V_a - f_{ql})]} + \frac{J_{oh} V_a^{n_h} \exp[f_{ph}(V_a - f_{qh})]}{1 + \exp[f_{ph}(V_a - f_{qh})]} \quad (4.15)$$

The subscripts l and h of the weighting function parameters f_p and f_q indicates the respective low and high bias regime. The typical values of the weighting function parameters are listed in Table 4-2.

Table 4-2: A list of weighting function parameter values used in Figure 4-7. Small variations of f_p do not affect the precision of the model.

Regions	Parameters	Value
Low and Medium Bias	f_{pl}	30
	f_{ql}	0.74
High Bias	f_{ph}	40
	f_{qh}	0.785

The final result of this empirical model for forward bias is plotted in Figure 4-7 against the measured values. The results calculated by the model matches very well with the measured data in all bias regimes.

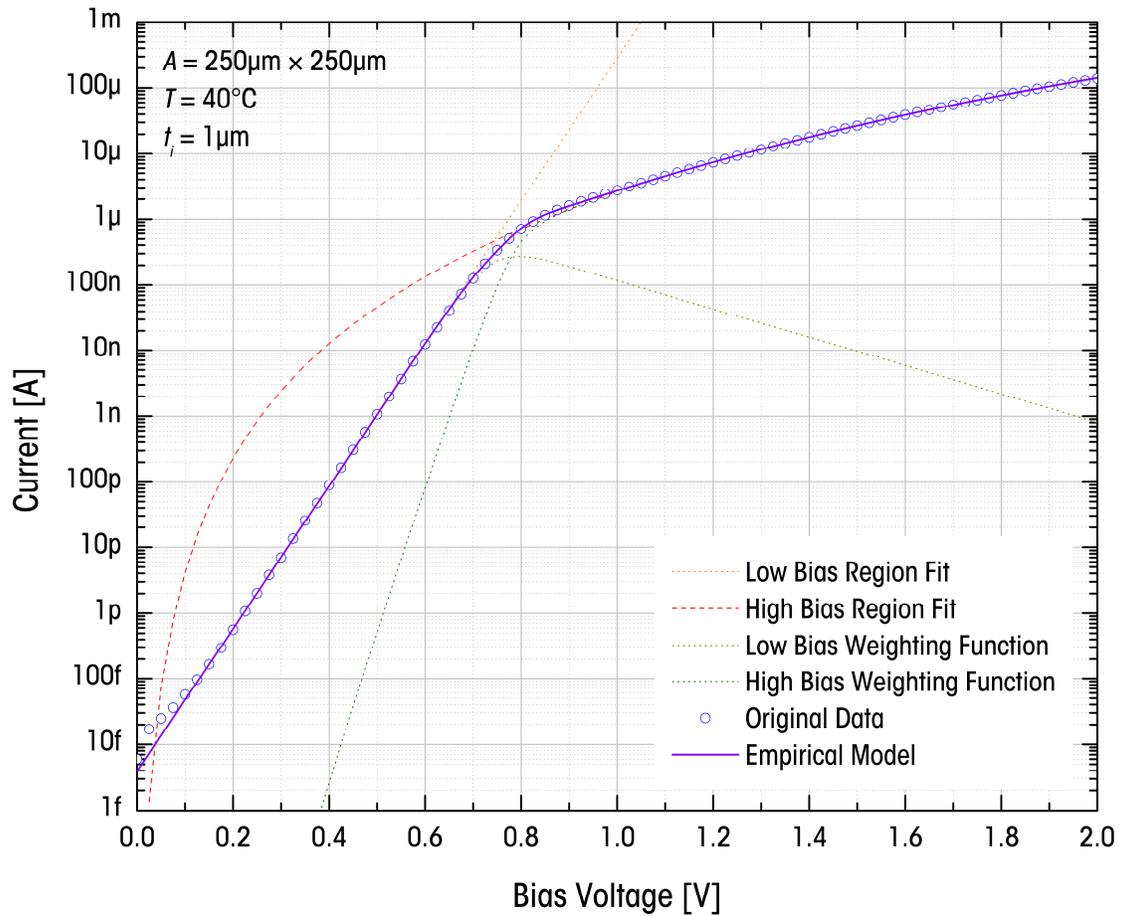


Figure 4-7: A plot showing the modeling result for a forward biased a-Si:H $n-i-p$ photodiode. The model curve is plotted along with the measured values to show that differences are very small. Results of the weighting functions are also plotted for reference.

4.1.2 Reverse Bias

For segmented a-Si:H $n-i-p$ photodiodes formed by patterning the a-Si:H films, the reverse bias dark current can be decomposed into a number of components. The origins of these components are discussed in Section 2.2.2. For good quality photodiodes, central and peripheral current components are the most important as they hold the majority portions of

the measured current values. Figure 4–8 illustrates these two components with respect to the geometry of the photodiode. There are also contributions from the corners of the photodiode as shown in the figure; however, its magnitude is much less than the central and peripheral components. This can be proved by measuring I_D - V characteristics at various temperatures for photodiodes with various sizes, which is presented later in this section.

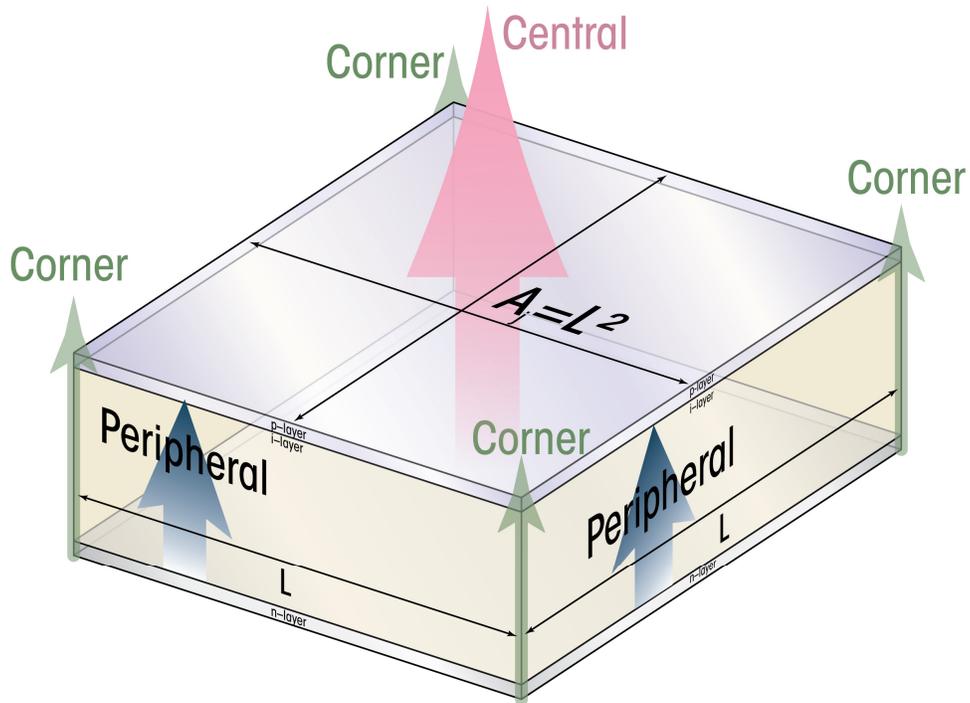


Figure 4–8: An illustration of the leakage current components of a-Si:H n - i - p photodiodes. The central, peripheral, and corner current components scale with the photodiode area, perimeter, and number of corners, respectively.

Consequently, the reverse bias dark current can be represented as the sum of central bulk generation current component and the peripheral edge leakage current component. As indicated in Figure 4–8, the central leakage

current component scales with the photodiode area while the peripheral component scales with the photodiode perimeter [108]. For a square a-Si:H $n-i-p$ photodiode with junction side length L , the reverse bias dark current can be expressed as

$$I_D = J_B L^2 + 4J_P L \quad (4.16)$$

where J_B and J_P are the central and peripheral current density, respectively. The peripheral current can be extracted if the I_D - V characteristics of two photodiodes with distinctly different sizes are available. Current of the large photodiode would be dominated by the central current component while current for the small photodiode would be governed by the peripheral components. In such case, J_P can be found by [98]

$$J_P = \frac{I_l A_s - I_s A_l}{A_s P_l - A_l P_s} \quad (4.17)$$

A_l and A_s are the large and small photodiode areas, respectively; P_l and P_s are the respective photodiode perimeters, and I_l and I_s are the respective measured current values. Using this method, any reverse bias I_D - V characteristics, such as the one shown in Figure 4-2, can be decomposed into central and peripheral components. Figure 4-9 shows the two leakage current component curves of the measured reverse current presented in Figure 4-2. Due to only partial current component dominances for both large and small photodiodes measured, small error exists for both extracted current components. The temperature measurement data presented in Section 4.1.3 provides a means of alleviating this error.

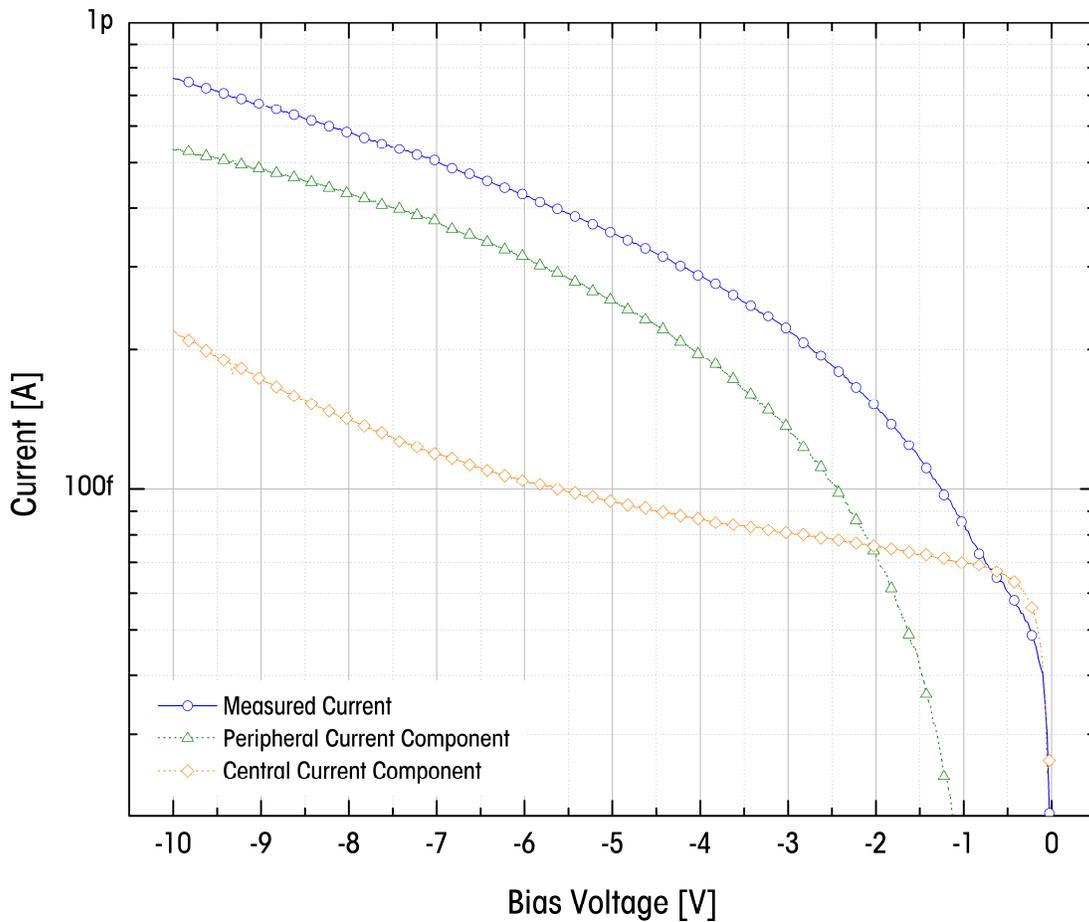


Figure 4-9: Decomposition of the two major current components of reverse biased a-Si:H $n-i-p$ photodiode with I_D-V characteristics shown in Figure 4-2. Error in low bias region is caused by the extraction process.

Variable Size Photolithography Mask Set

A full set of high quality metal photolithography masks is designed and fabricated to extract the central and peripheral current components. The mask set allows the fabrication of segmented a-Si:H $n-i-p$ photodiode structures of various sizes between $L=50\mu\text{m}$ to $L=2000\mu\text{m}$. For small photodiodes, leakage current level falls below the femto-Ampere range. It

is too low for the characterization system to measure accurately. Therefore, these photodiodes are connected in parallel and the measured values are the divided and averaged. This and other connection configurations are shown in Figure 4–10. Of course, the technique relies on the uncertainties that one of the photodiode connected in parallel may have shunts, which would increase the overall current value. Forward I_D - V measurement are done to discern these defects before reverse bias measurements.

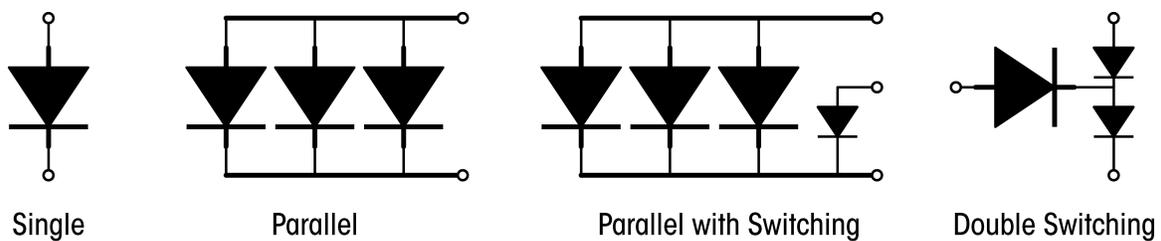


Figure 4–10: Different connection configurations included in the mask set. Single and double switching connections are available for large photodiodes. Parallel connections are done for small photodiodes where the current level of a single photodiode is too low for the measurement instruments even with remote amplifiers.

The complete design process of the mask set is lengthy; therefore, it is only presented briefly here. A document is written to detail the specifics for this topic [109]. The designed wafer is divided into three regions. The top portion of the wafer is mainly given to small area dies. The middle portion is reserved to deflection experiments, prepared for photodiodes fabricated on robust substrates such as stainless steel or plastic. The bottom portion of the wafer is given to large area dies. A screenshot of the wafer layout is shown in Figure 4–11.

Some selected die configurations included in the layout are shown in Appendix A. Different layout design rules are applied depending on the

size of the photodiodes; they are given in Appendix B. The dies are designed so that they can be readily packaged into a standard 28-pin *dual inline package* (DIP). A number of measurements are taken with die configuration 8 (Figure A-8). This configuration has a common bottom electrode with top metallization patterned. Large photodiodes have dedicated bonding pads for packaging, while smaller photodiodes are connected in parallel with internal probing pads. The photodiodes are also placed in close vicinity of each other to ensure similar processing conditions and lower temperature variations during temperature I_D - V characteristic measurements.

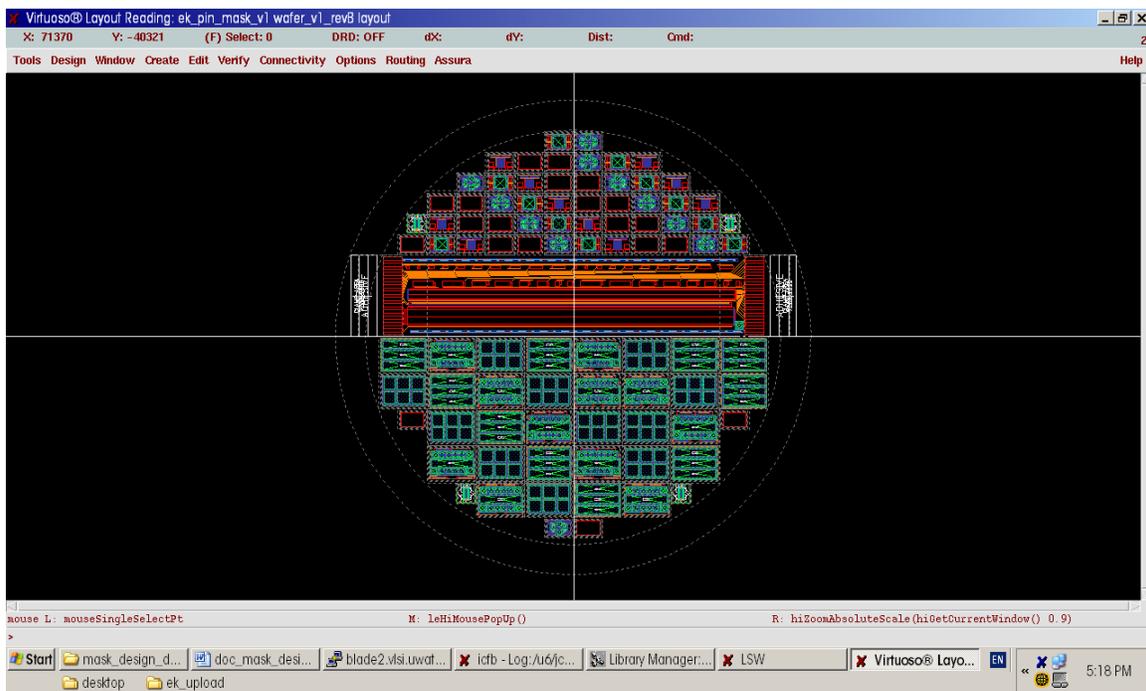


Figure 4-11: A screenshot of the variable size photodiode wafer mask set. The top portion and bottom portion are given to small and large sized die configurations, respectively. The middle portion is reserved for experiments with flexible substrates. Selected screenshots of the die configurations can be found in Appendix A.

Central Leakage Component

For large a-Si:H $n-i-p$ photodiodes ($A_j > 1 \times 1 \text{ mm}^2$), the dominating leakage current mechanism is the central current (I_B). This component arises from the excitation of electrons from the valence band to the empty gap states, and from the filled gap states to the conduction band [110]. The thermal generation current is discussed in Section 2.2.2. The estimated magnitude of the thermal generation current is given by [71]

$$I_{th} = t_i g(E_{FD}) k_B T \omega_{oc} \exp\left(-\frac{E_C - E_{FD}}{k_B T}\right) A_j \quad (4.18)$$

Referring to the measured values shown in Figure 4-9, the calculated value is not only smaller but also lacks the voltage dependence that is apparent from the measured results.

A number of explanations are given to describe this bias dependence including field-enhanced emission process [60], increase in generation centers [72], and electron-lattice interactions [111]. Detailed analysis of the field dependence is complicated since both carriers may be excited from the same defect level in the localized states in the band tail. Kramer et al. argues that the bias dependence on the width of the i -layer is small compared to the field-enhanced conduction and can be ignored to simplify analysis. Since most relevant generation centers are located in proximity of E_{FD} , the activation energy of the reverse current should be bias independent. The generation center theory would work if the depletion charge has similar bias dependence as the photodiode current.

However, this is not the case; the bias dependence of the depletion charge is much weaker than the photodiode current. Therefore, field-assisted excitation is a more plausible cause for the bias dependence of reverse dark current. There are two field-dependent emission mechanisms that need to be considered: *thermally assisted tunnelling* (TAT) and *Poole-Frenkel* (PF). For electrons, if the particle is from an initially negative defect ($D^{0/-}$), then the field enhancement is attributed to TAT. In contrast, if the defect state is initially neutral ($D^{+/0}$), the enhancement is described by PF mechanism. For holes, the situation is reversed. The probability for TAT to occur is given by [111]

$$P_{TAT}(E_T, \xi) = \omega_{oe} \exp\left(\frac{E_C - E_T}{k_B T}\right) + \int_{E_C}^{E_T} \frac{\omega_{oe}}{k_B T} \exp\left(\frac{E_C - E_T + \delta E}{k_B T}\right) g(\delta E, \xi) d(\delta E) \quad (4.19)$$

The first term refers to thermal emission as described before. The second term refers to the enhancement due to escape probability via states located δE below the conduction band; $g(\delta E, \xi)$ is the density of these states, which calculates the penetration of the conduction band electron wave function through a triangular potential barrier. The probability for PF field-enhanced mission to occur is given by [111]

$$P_{PF}(E_T, \xi) = \omega_{oe} \exp\left(\frac{E_C - E_T + \Delta E_{PF}}{k_B T}\right) + \int_{E_C}^{E_T + \Delta E_{PF}} \frac{\omega_{oe}}{k_B T} \exp\left(\frac{E_C - E_T + \Delta E_{PF} + \delta E}{k_B T}\right) g(\delta E, \xi) d(\delta E) \quad (4.20)$$

Here, ΔE_{PF} describes the energy barrier reduction due to interactions between electric field and charge traps; it can be expressed as [111]

$$\Delta E_{PF} = 2 \sqrt{\frac{q\xi}{4\pi\epsilon_0\epsilon_r}} \quad (4.21)$$

Considering these two mechanism simultaneously, the field assisted enhancement from a charged defect can be described by TAT with an enhancement factor of $\exp(-\beta_t\xi)$. Similarly, if the particle is from an initially neutral defect, the enhancement can be described by PF mechanism with a factor of $\exp(-\beta_{pf}\sqrt{\xi})$. Assuming a uniform field across the i -layer, both field assisted mechanisms are possible contributors for the observed voltage dependence of the thermal generation current. The bulk generation current density equation can therefore be modeled by

$$J_B(\xi) = J_{th} \exp(-\beta_t|\xi|) \alpha_{pf} \exp(-\beta_{pf}\sqrt{|\xi|}) \exp(-\beta_{pd}\sqrt{|\xi|^3}) \quad (4.22)$$

β_t is the exponential factor for modeling TAT; α_{pf} and β_{pf} are the pre-exponential factor and exponential factor for modeling PF mechanism; β_{pd} is the exponential factor to account for the partial depletion at low reverse biases where the mean electric field strength is not adequately established across the i -layer. To extract these parameters, a variable substitution is first made for the electric field ξ ,

$$X = \sqrt{|\xi|}, \quad Y = \ln \left| \frac{J_B(\xi)}{J_{th}} \right| \quad (4.23)$$

Equation (4.22) therefore becomes a polynomial in terms of X .

$$Y = \beta_{pd}X^3 + \beta_t X^2 + \beta_{pf}X + \ln|\alpha_{pf}| \quad (4.24)$$

The coefficients of this polynomial can be extracted using linear regression analysis. Given $i = 1, 2, \dots, n$ measured value pairs (I_i, V_i) ,

$$I_i = \beta_{pd}V_i^3 + \beta_t V_i^2 + \beta_{pf}V_i + \ln|\alpha_{pf}| + \varepsilon_i \quad (4.25)$$

The error term ε_i takes into account the unpredicted variations from measurements. ε_i is assumed to be uncorrelated for each data point with a mean value of zero. Equation (4.25) can be rewritten in matrix form,

$$\underbrace{\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_n \end{bmatrix}}_{\mathbf{Y}} = \underbrace{\begin{bmatrix} V_1^3 & V_1^2 & V_1 & 1 \\ V_2^3 & V_2^2 & V_2 & 1 \\ \vdots & \vdots & \vdots & \vdots \\ V_n^3 & V_n^2 & V_n & 1 \end{bmatrix}}_{\mathbf{X}} \underbrace{\begin{bmatrix} \beta_{pd} \\ \beta_t \\ \beta_{pf} \\ \ln|\alpha_{pf}| \end{bmatrix}}_{\hat{\boldsymbol{\beta}}} + \underbrace{\begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \vdots \\ \varepsilon_n \end{bmatrix}}_{\hat{\boldsymbol{\varepsilon}}} \quad (4.26)$$

Using least-squares estimator, the parameter matrix $\hat{\boldsymbol{\beta}}$ is given by

$$\hat{\boldsymbol{\beta}} = (\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T \mathbf{Y} \quad (4.27)$$

The residuals, representing the difference between the measured value and the fitted quantities, can be found by

$$\hat{\boldsymbol{\varepsilon}} = \mathbf{Y} - \mathbf{X}\hat{\boldsymbol{\beta}} \quad (4.28)$$

Using this method, the extracted parameter values for the central current component shown in Figure 4–9 is given in Table 4–3. Figure 4–12 shows the extraction process with the variable substitution; it plots the calculated values with the extracted parameters against the measured values. Excellent matching is found for most regions of the curve.

Table 4–3: A list of parameters and their corresponding values used for calculating the field-enhanced carrier generation of bulk current component.

Parameters	β_{pd}	β_t	β_{pf}	α_{pf}
Extracted Values	-1.535×10^{-7}	6.731×10^{-5}	-0.011	1.174

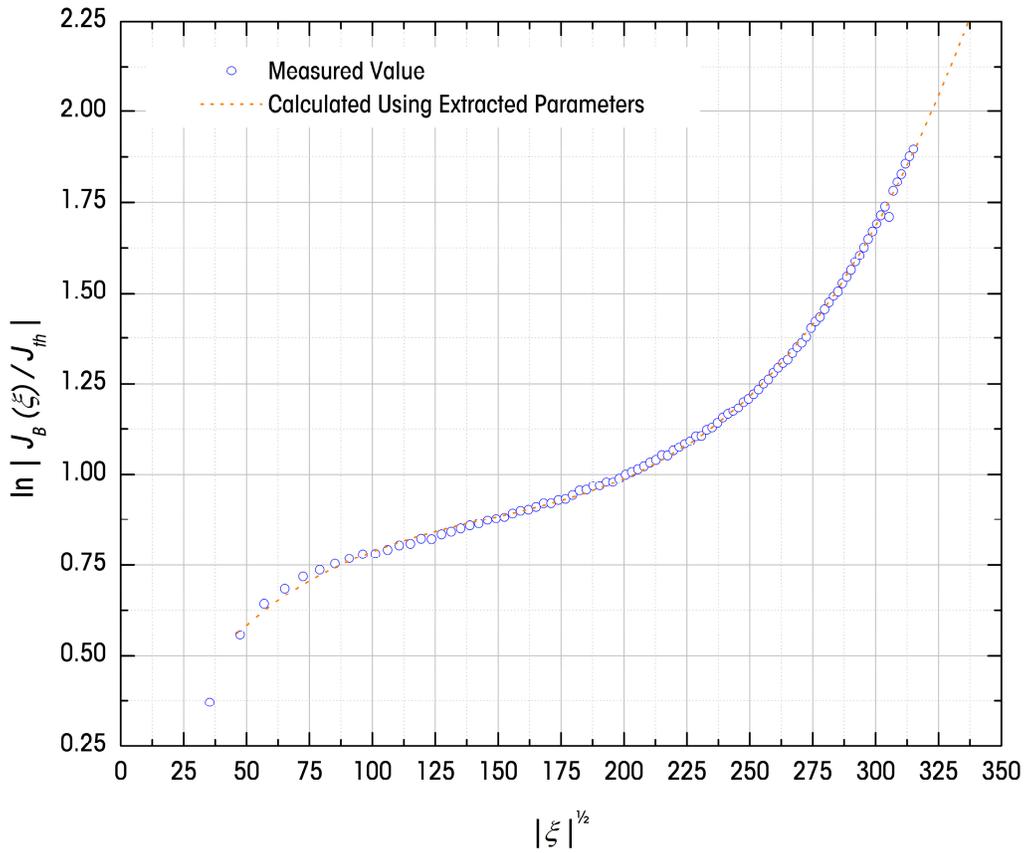


Figure 4–12: A plot of calculated current for field-enhanced generation using the extracted parameter values. The measurement data are shown in hollow circles.

With the new found parameters, the central current component can be easily modeled by Equation (2.39) and (4.22). Figure 4–13 shows the result of the central current component model in relation to the measured values. The model matches well in the low and medium bias regions, which is where the photodiode would be operated for the fluorescence-based bio-assay application.

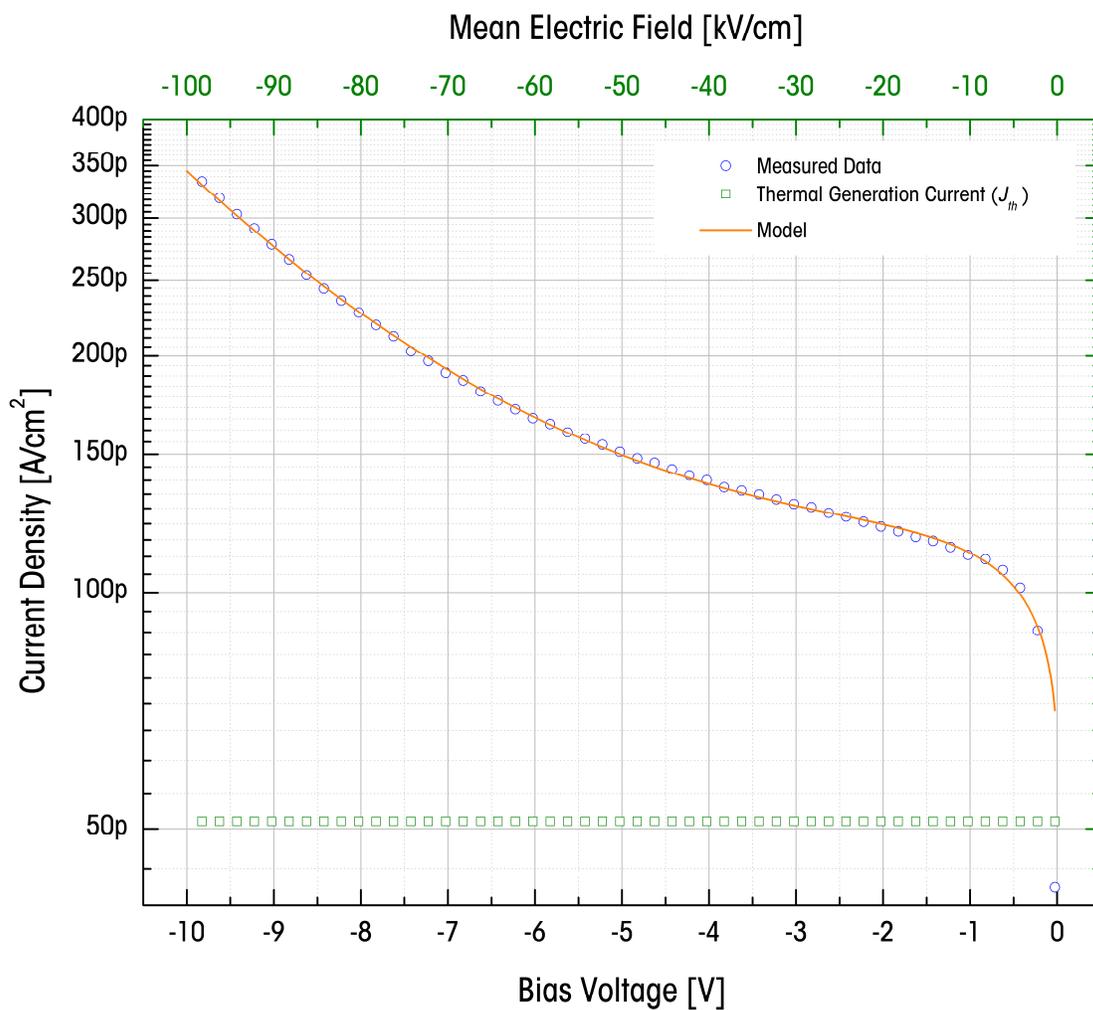


Figure 4–13: A plot of the central current component with the calculated model that includes field-enhanced generation phenomenon. Estimated J_{th} is also included.

Peripheral Leakage Component

While a major portion of the total leakage current in large a-Si:H *n-i-p* photodiodes is attributed to central leakage component, the peripheral leakage component (I_p), affected by the details of the sensor structure and fabrication process, may very well dominate the total leakage current level for small photodiodes ($A_j < 100 \times 100 \mu\text{m}^2$). This would limit the practical dimensions of such devices.

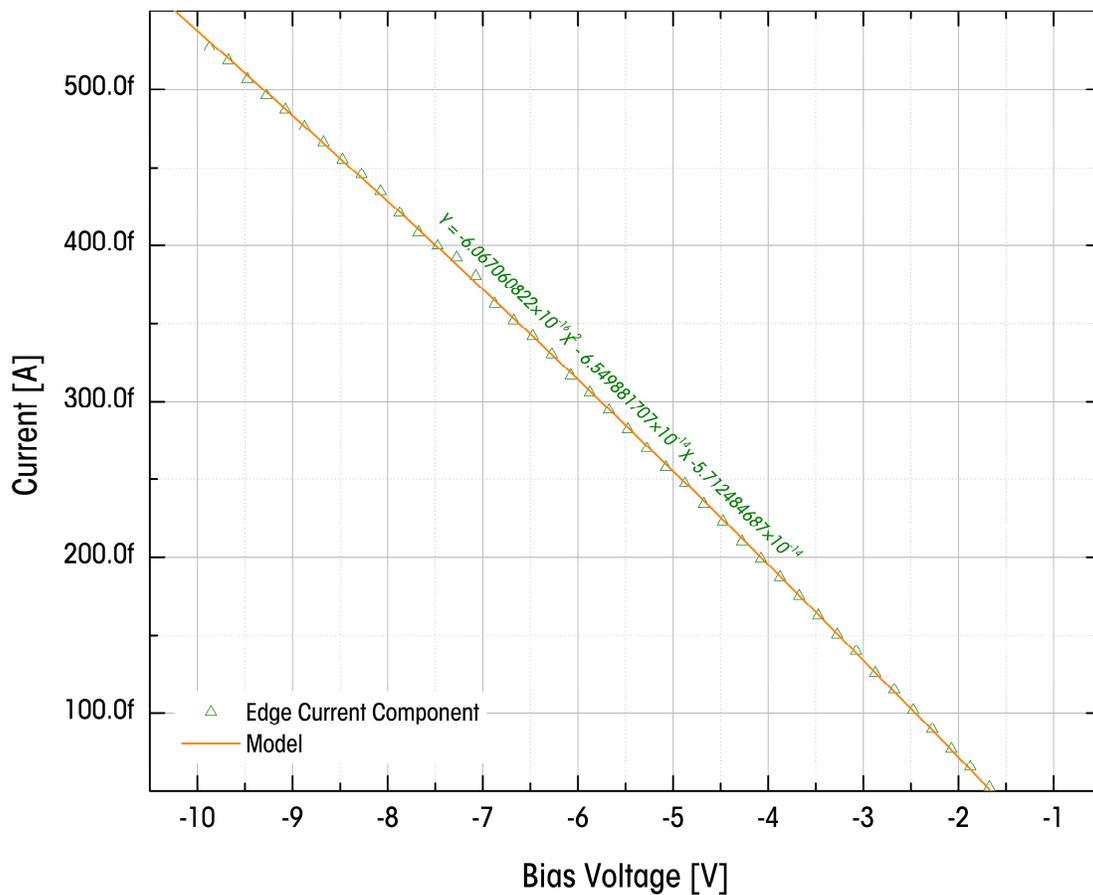


Figure 4-14: A graph of the measured peripheral current component plotted against the calculated model. The second order effect of this component is only evident at elevated temperatures.

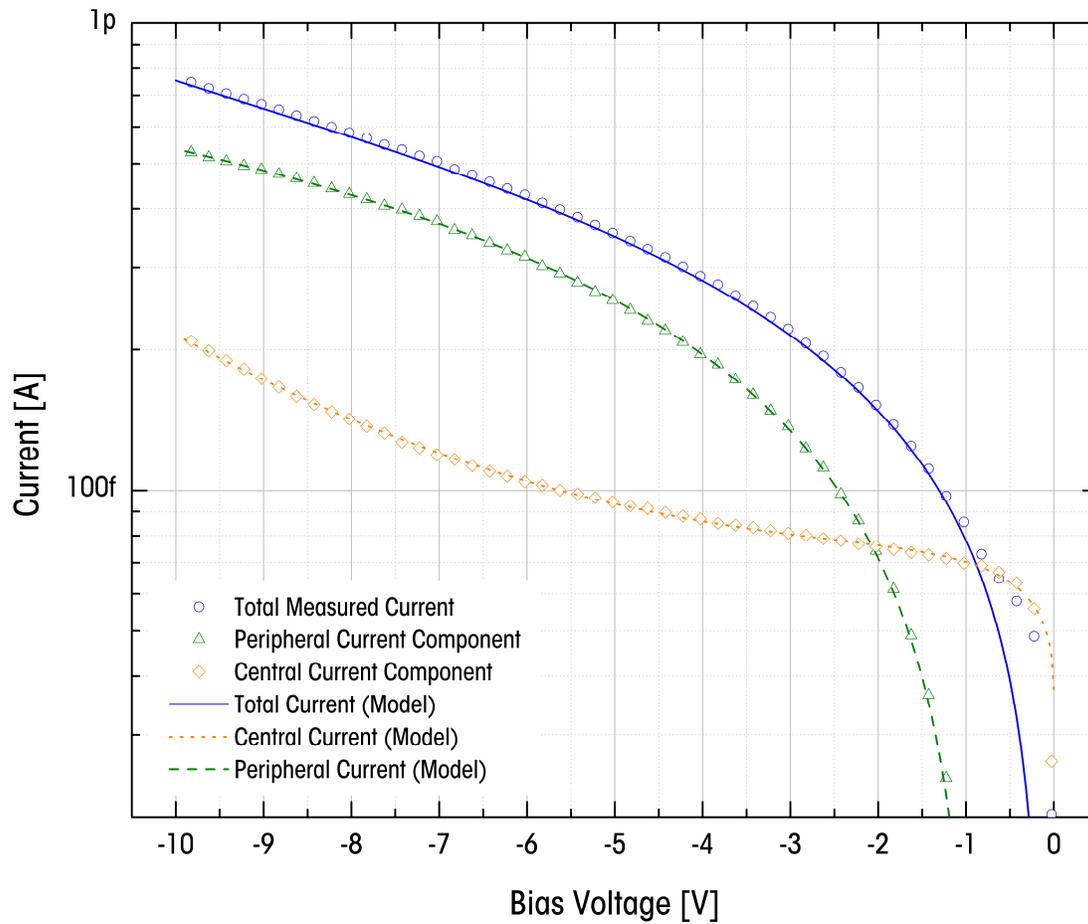


Figure 4-15: A plot of the measured current and its corresponding model components. The original measurement data is from a $250 \times 250 \mu\text{m}^2$ a-Si:H segmented *n-i-p* photodiode. The calculated model fits very well for reverse bias voltage beyond -1V .

Peripheral component may be caused by the increased defects at the photodiode junction sidewalls where the intrinsic a-Si:H interfaces with the a-SiN_x:H passivation. For this reason, the peripheral edge leakage current conductance is proportional to the photodiode junction perimeter. The increased defects can be attributed to damages due to intense ion bombardment during the RIE process. Surface states may also exist due to

changes at the interface. Therefore, the peripheral current component has a much larger and less predictable variation compared to the central leakage component.

The decomposed peripheral current component shown in Figure 4–9 also indicates a strong bias dependence. In general, this component can be modeled by a second order polynomial. The result of this model is shown in Figure 4–14. It may seem that in this plot the second order term is not necessary in providing a good fit; a linear equation would have also given a good match. However, the second order effects are more pronounced in elevated temperatures. At room temperature, the coefficient of the high order term is indeed small. This phenomenon is discussed in the proceeding section. The combined model for reverse current is shown in Figure 4–15. The measured reverse current and the calculated current from the model matches very well beyond $-1V$.

4.1.3 Temperature Dependence

The majority of studies of the leakage components is performed at room temperature for various photodiode sizes, deposition temperature, and etching processes in attempt to separate the central and peripheral components [62], [65]. Even though temperature dependence of the reverse dark current for large area photodiodes is previously analyzed [60], there is a need to determine the temperature dependences of various current components. This subsection presents findings of the temperature dependence study of dark current characteristics for segmented a-Si:H n -

i-p photodiodes, allowing a more accurate separation of different leakage components at various temperatures. The results also establish the foundations necessary to model the temperature effects of the I_D-V characteristics.

Square segmented a-Si:H *n-i-p* photodiodes with side length L ranging from 125 μm to 2000 μm are fabricated using the variable size photolithography mask set (Section 4.1.2). The I_D-V characteristics are measured in the range of 40–80°C. The forward and reverse dark current characteristics are measured separately in the range of 0V to –5V and 0V to 1V at 50mV steps. To minimize temperature drift during measurements, half an hour is given to the measurement system for it to ramp up and stabilize to the targeted temperature.

Figure 4–16 plots the measured J_D-V characteristics of an $L=1000\mu\text{m}$ square photodiode at each measurement temperature [112]. For clarity, only one data set is shown; though, other sizes have seemingly identical behaviours. As expected, the forward bias characteristics follow an exponential behaviour in the bias range of 0.1–0.6V. Figure 4–17 plots the measured J_D-V characteristics for various photodiode sizes at 40°C. J_D matches very well for photodiodes with different L indicating that there is no current shunt path created during deposition. The same conclusion is reached by comparing the forward current characteristics. The exponential region can be fitted using Equation (4.6) with the modification of a temperature dependent saturation current density $J_{D_0}(T)$ and ideality factor $n(T)$:

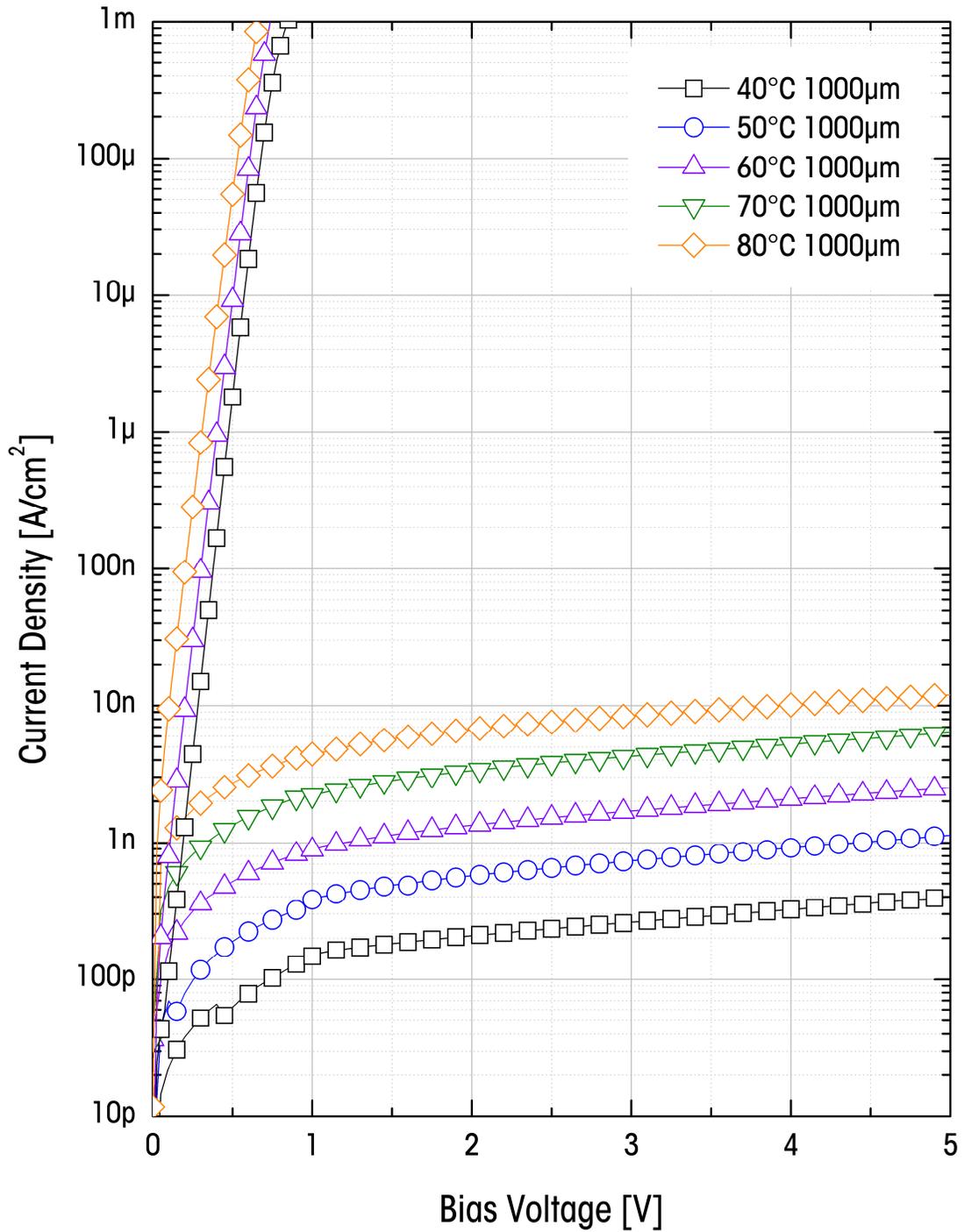


Figure 4-16: Measured J_D - V characteristics for $L = 1000\mu\text{m}$ square photodiode at various temperatures [112]. The J_D approximately doubles every 10°C .

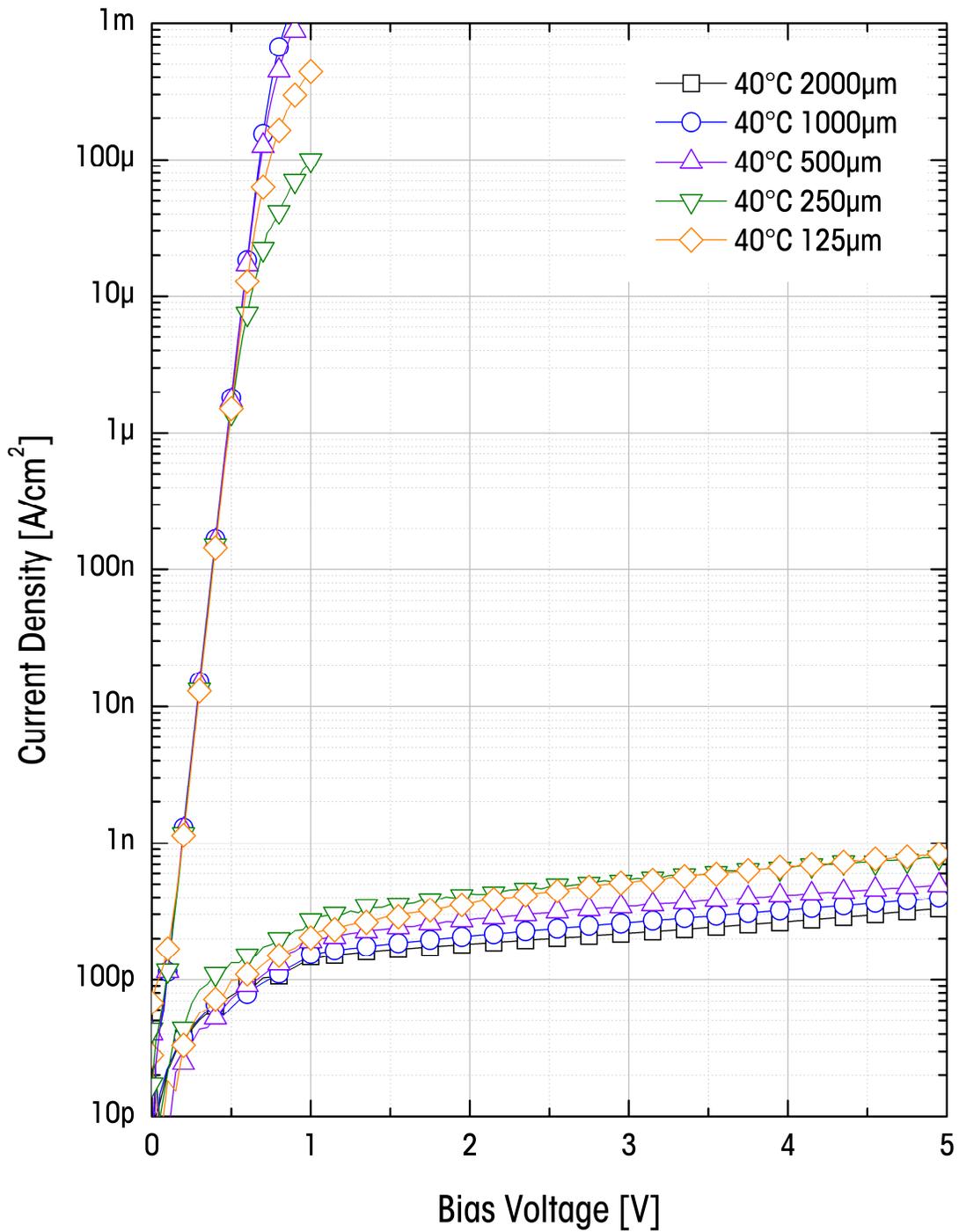


Figure 4-17: Measured J_D - V characteristics at 40°C for photodiodes with various sizes [112]. Smaller photodiodes have slightly higher current density level as expected.

$$J_D = J_{D_o}(T) \left[\exp\left(\frac{qV_a}{n(T)k_B T}\right) - 1 \right] \quad (4.29)$$

The parameters can be extracted for each temperature and size using the same method presented in Section 4.1.1. Figure 4–18 shows the temperature dependence of $J_{D_o}(T)$ and $n(T)$ obtained from the measurement data. $J_{D_o}(T)$ follows the Arrhenius relationship

$$J_{D_o}(T) = A_o \exp\left(-\frac{E_a}{k_B T}\right) \quad (4.30)$$

A_o is the pre-exponential factor dependent on the processing conditions, and E_a is the forward bias activation energy. The activation energy, averaged to be $\sim 0.85\text{eV}$ from the extraction, is shown in Figure 4–18 inset. It matches very well with the previous reported values [56]. The change for the photodiode ideality factor is very small. The diode ideality factor at 40°C is ~ 1.4 and decreases linearly with temperature at the rate of $\sim 0.003\text{K}^{-1}$. This can be modeled with a linear equation,

$$n(T) = n_0 + \delta n T \quad (4.31)$$

n_0 is the value of the ideality factor interpolated at 0K; δn is the rate of change per Kelvin.

For high forward biases, a similar procedure is performed to extract the power-law constant. The activation energy in the high forward bias region is approximately half of the value extracted for the exponential region.

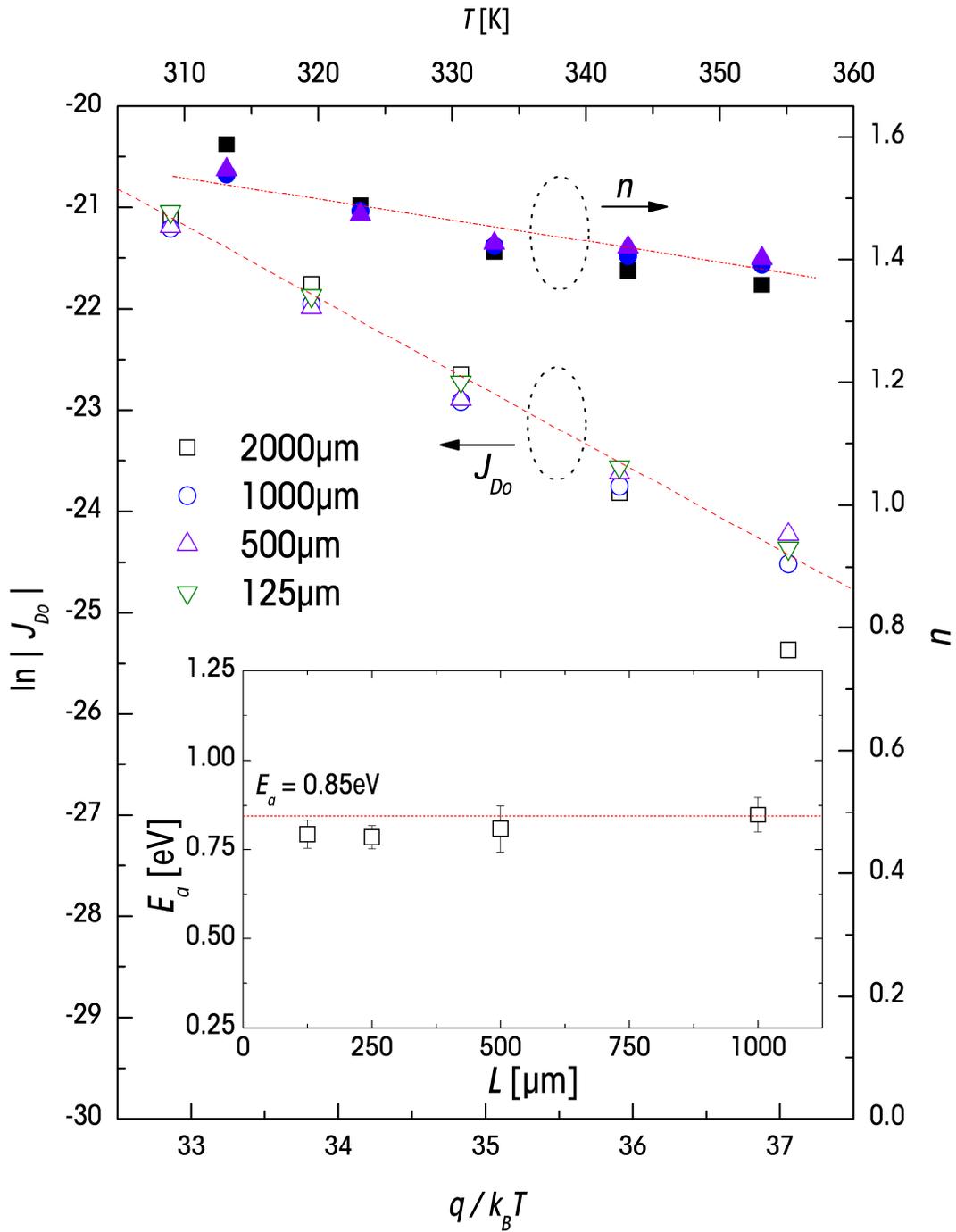


Figure 4-18: Extracted parameters $J_{D0}(T)$ and $n(T)$ from measured forward J_D - V characteristics [112]. Inset shows the extracted forward activation energy averaged to be ~ 0.85 eV.

Changes for the power constant remain small, similar to that of the behaviour of the photodiode ideality factor. These parameter values are summarized in Table 4-4.

Table 4-4: A list of parameters extracted from the temperature dependence measurements for forward biased a-Si:H *n-i-p* photodiodes.

	A_o	E_a	n_o	δn
Low Bias	15.577×10^3	0.85eV	1.48	-0.003K^{-1}
High Bias	37.019×10^3	0.45eV	5.79	-0.003K^{-1}

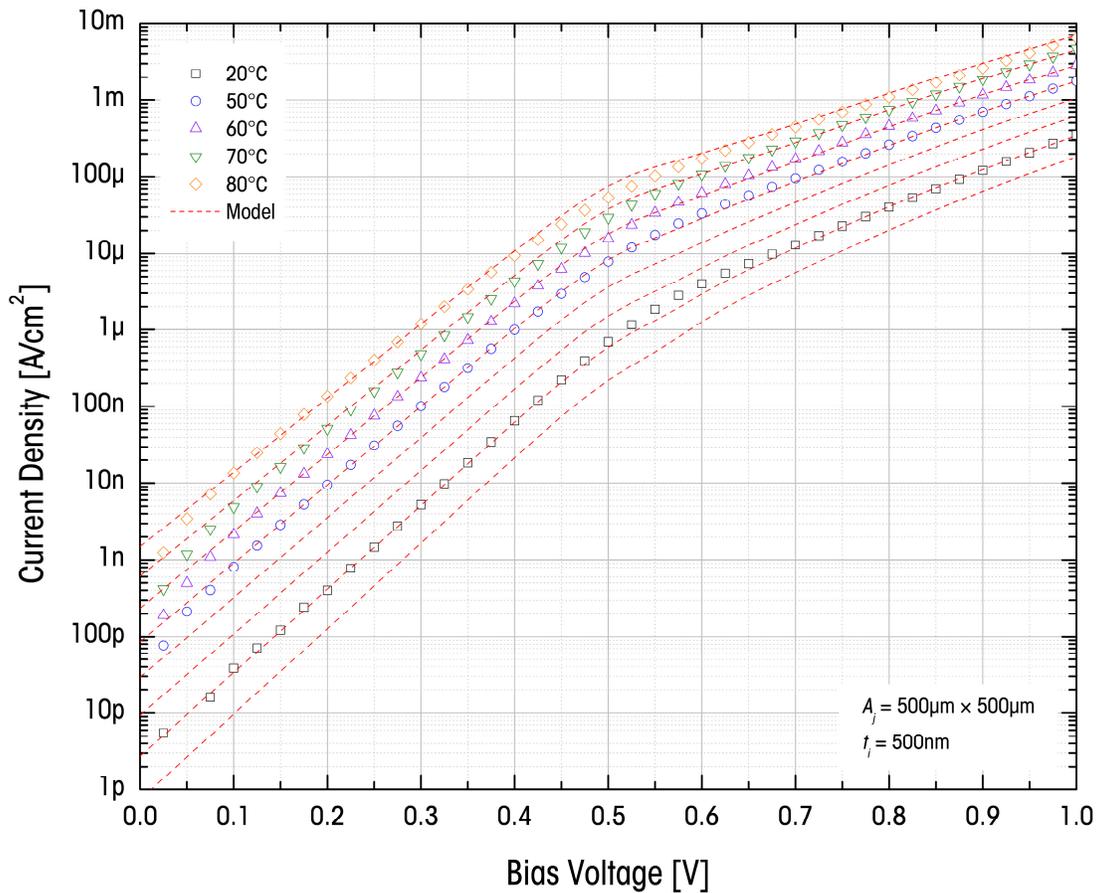


Figure 4-19: A plot of the measured data against the calculated model built from the extracted parameters. The hollow symbols are part of the measured data. The model fits well for both the low bias exponential region and high bias power-law region.

Incorporating these temperature dependent parameters into Equation (4.15) gives the forward bias modeling equation

$$I_D = A_j A_{ol} \frac{\exp\left[\frac{qV_a}{(n_{ol} + \delta n_l T)k_B T} - \frac{qE_{al}}{k_B T}\right]}{1 + \exp\left[f_{pl}(V_a - f_{ql})\right]} + A_j A_{oh} \exp\left(-\frac{qE_{ah}}{k_B T}\right) V_a^{(n_{oh} + \delta n_h T)} \frac{\exp\left[f_{ph}(V_a - f_{qh})\right]}{1 + \exp\left[f_{ph}(V_a - f_{qh})\right]} \quad (4.32)$$

This equation is calculated and plotted against the measured data at different temperatures, shown in Figure 4–19. The model matches the experimental data well in both the low bias exponential region and high bias power-law region. The model does not account for the shift of the center parameters of the weighting function; thus, causing slightly larger variations in the transition regions.

For reverse bias leakage current, the temperature dependence measurements are not only used for the separation of the main central and peripheral components, but also used to extract their individual temperature dependences. From the measurement data of photodiode samples baring the same L , the observed reverse photodiode leakage current level is fairly consistent. In addition to the two components inferred in Equation (4.16), an additional parameter I_o is included to account for the current contribution from photodiode corners and instrumentation leakage. Therefore, the quintessential representation of the reverse leakage current is

$$I_D = J_B L^2 + 4J_P L + I_o \quad (4.33)$$

To extract the central and peripheral component graphically, Equation (4.33) is rearranged to

$$\frac{I_D}{L} = J_B L + 4J_P + \frac{I_o}{L} \quad (4.34)$$

$$\frac{I_D}{L^2} = J_B + \frac{4}{L} J_P + \frac{I_o}{L^2} \quad (4.35)$$

Figure 4–20 shows the I_D/L and I_D/L^2 (inset) plots with respect to L at 40°C, for different voltage biases. Since I_D/L varies linearly with L for $L > 500\mu\text{m}$, J_B and J_P can be respectively obtained from the slope and intercept values, via linear regression. The magnitude of I_o is comparable with the total leakage current for photodiodes with $L < 250\mu\text{m}$. This is apparent from the I_D/L^2 plot where the sudden reduction of current below $L=250\mu\text{m}^2$ indicates that the I_o/L^2 term dominates in that region. The question may rise as to why the I_D/L^2 term is not used for the extraction of J_B . In the inset of Figure 4–20, the I_D/L^2 plot shows that even for $L = 1000\mu\text{m}^2$, there are still traces of non-negligible peripheral current component; otherwise, the curves would be completely flat for large area photodiodes. Obtaining the slope of I_D/L avoids using extrapolation of curves on the y -axis which would otherwise give a larger error of extraction. Furthermore, this extraction process yields better precision compared to the method given in Equation (4.17) [98] where no assumption is made for the dominating current component for large and small area photodiodes.

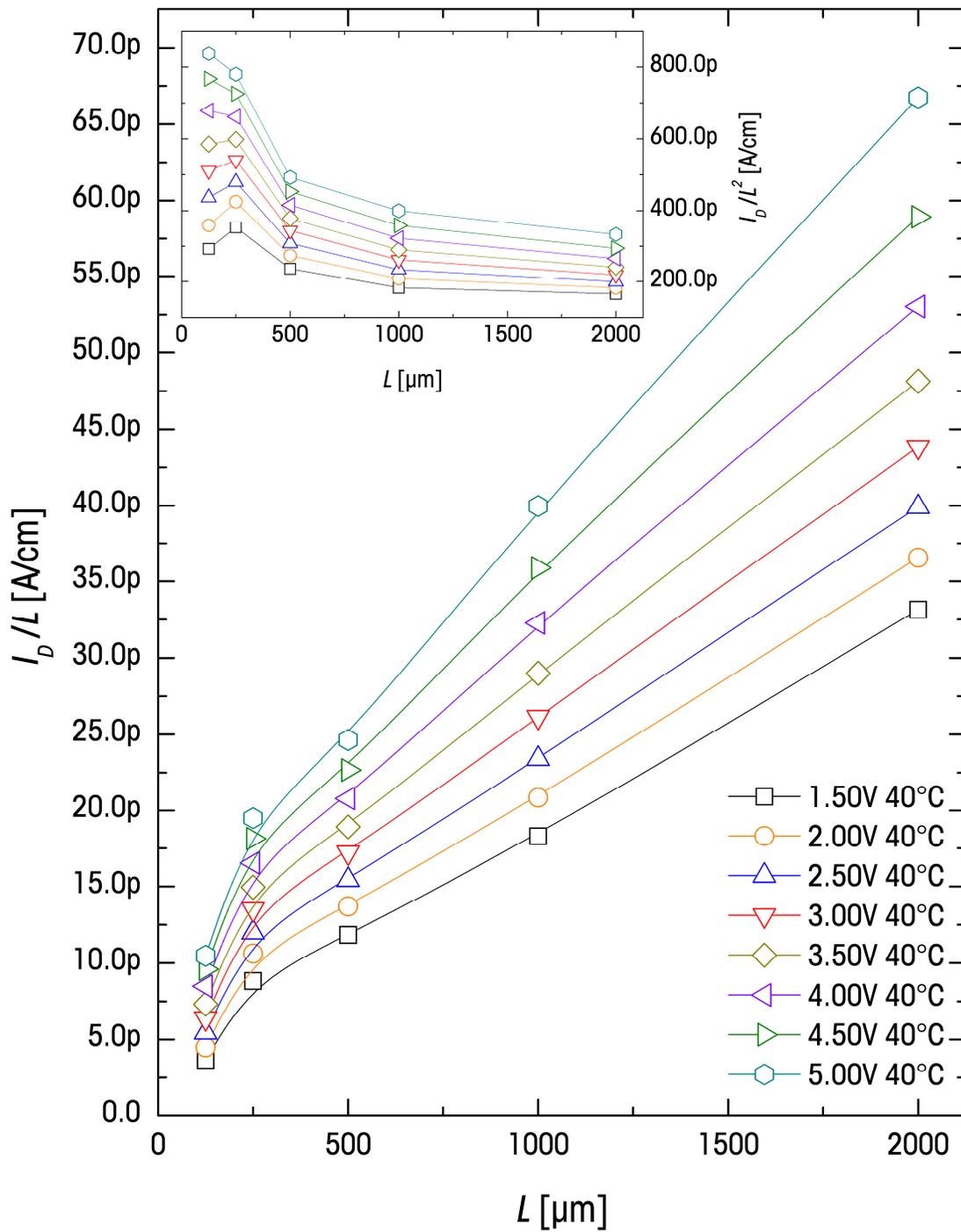


Figure 4-20: I_D/L and I_D/L^2 (inset) as functions of the photodiode side length (L) measured for different voltage biases at 40°C [112].

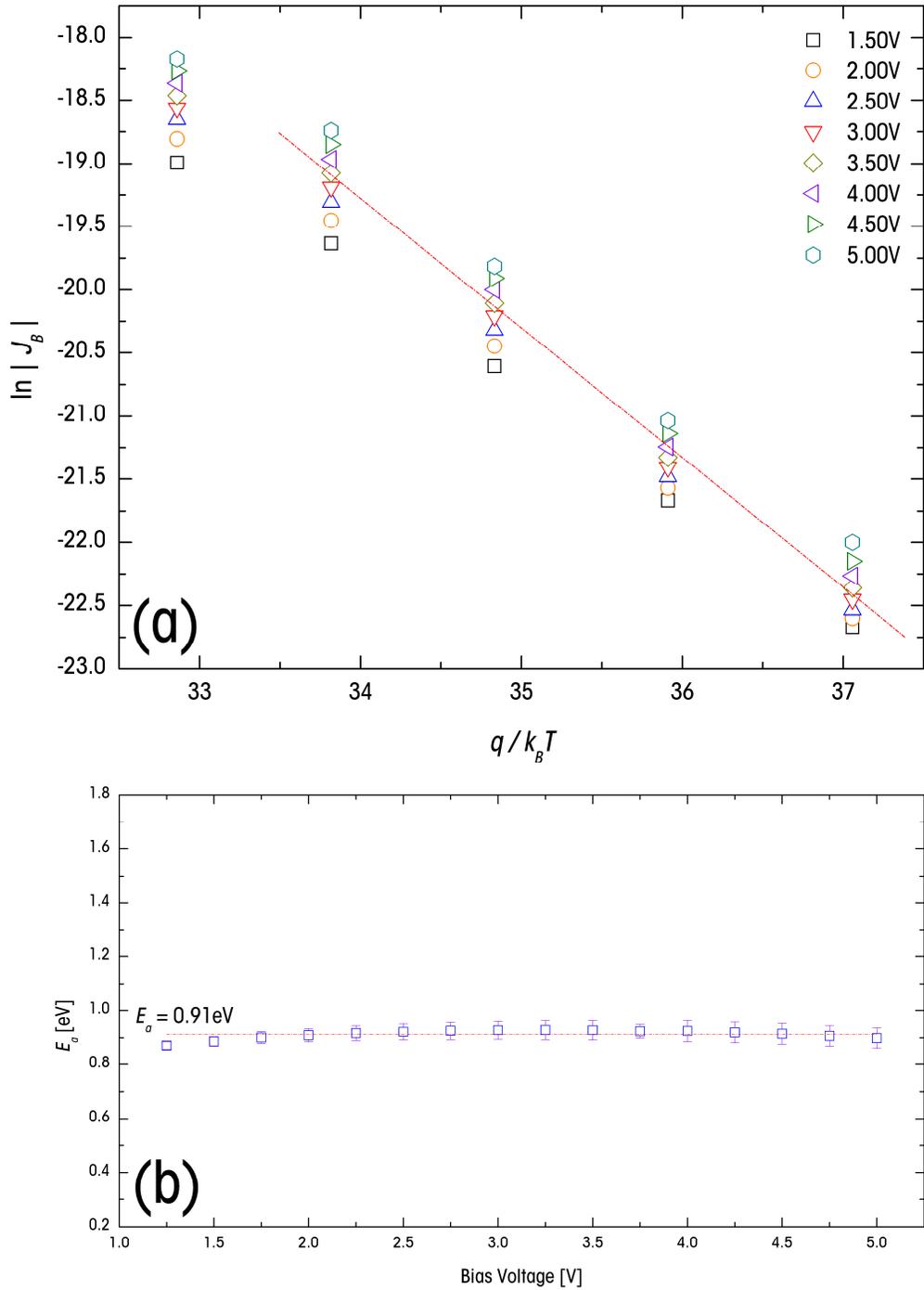


Figure 4-21: Temperature dependence of (a) extracted central leakage current density and (b) activation energy for different reverse bias voltages [112].

To investigate the temperature dependence of the central current component, the Arrhenius plot of the extracted J_B is shown in Figure 4–21a. The central current component increases exponentially with temperature. The activation energies, extracted from the Arrhenius plot at different reverse biases, are shown in Figure 4–21b. There is no noticeable bias dependence of E_a . The average value of E_a is $0.91\pm 0.03\text{eV}$, which is approximately half of the reported mobility gap for device quality a-Si:H [15]. Since the dependence of E_a on the bias voltage is weak, the field and thermal component of J_B can be decoupled and modeled separately. J_B at various temperatures and bias voltages can therefore be described by

$$J_B(V, T) = J_{B0} \exp\left(-\beta_v \frac{V}{t_i}\right) \exp\left(-\frac{E_a}{k_B T}\right) \quad (4.36)$$

J_{B0} is the pre-exponential constant for the bulk component model; from measured data, it is estimated to be $\sim 5.8 \times 10^4 \text{A/cm}^2$. β_v is the voltage dependence exponential constant estimated to be $\sim 1.03 \times 10^{-5} \text{cm/V}$, assuming the field is uniform across the i -layer with thickness t_i . This value is very similar to the TAT exponential factor β_t extracted via Equation (4.22).

Figure 4–22 shows the modeled I_B plotted with measured I_D for an $L=1\text{mm}$ square photodiode. It is evident from the plot that as temperature increases, I_p contribution towards I_D diminishes [112]. The thermal generation current in the photodiode bulk surpasses the leakage current sourced at the edges of the photodiode.

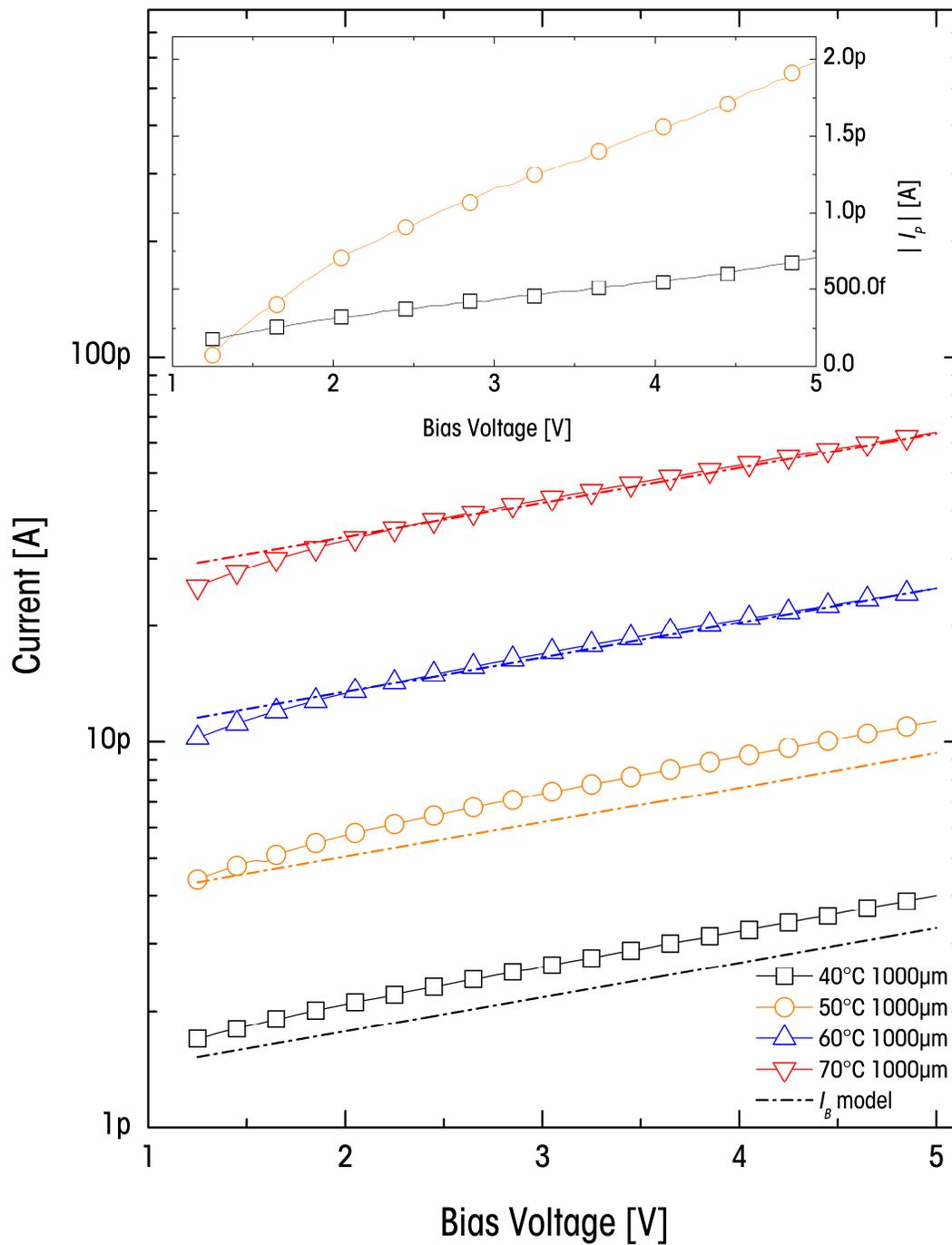


Figure 4-22: Reverse I_D - V plot of $L=1000\mu\text{m}$ segmented $a\text{-Si:H } n\text{-i-p}$ photodiode at various temperature. The measurement results are shown with hollow symbols. Dotted lines are the modeled I_B using extracted activation energy.

At low voltage biases, the noticeable deviation of the experimental curves from values calculated via Equation (4.36) is owed to the incomplete depletion of the i -layer.

Figure 4-22 inset shows the plot of peripheral current component extracted for 40°C and 50°C. At higher temperatures, the I_p component is much smaller than I_B . Therefore, this prevents accurate extraction of I_p beyond 50°C. The issue is apparent in the inset plot of Figure 4-20 where data for large photodiode is no longer flat for measurement temperatures higher than 50°C. The perimeter current component increases linearly with voltage, giving the valued opportunity to model this leakage component as a shunt resistor. The peripheral unit conductances $G = (dI_p/dV)/4L$ are estimated to be $\sim 0.3\text{pS/cm}$ and $\sim 1.0\text{pS/cm}$ at 40°C and 50°C, respectively. This mounts to a peripheral shunt resistance of $64\text{T}\Omega$ for an $L=125\mu\text{m}$ photodiode at 40°C. From the presented equations and parameter extraction methods, the temperature dependent reverse leakage current can be modeled empirically.

4.1.4 Capacitance

For a reverse biased a-Si:H $n-i-p$ photodiode, the capacitance value stays fairly constant, indicating that the depletion region spans across the intrinsic layer of the photodiode even at low biases. Therefore, the photodiode capacitance can be approximated as parallel plate capacitor with its i -layer as the dielectric (Equation (2.40)). There is however, a minor voltage dependence on the capacitance due to the expansion of the

depletion region in the doped contacts (Equation (2.41)) [113]. Figure 4–23 shows a plot of the measured C – V characteristics for an $L=1\text{mm}$ square photodiode deposited on glass substrate.

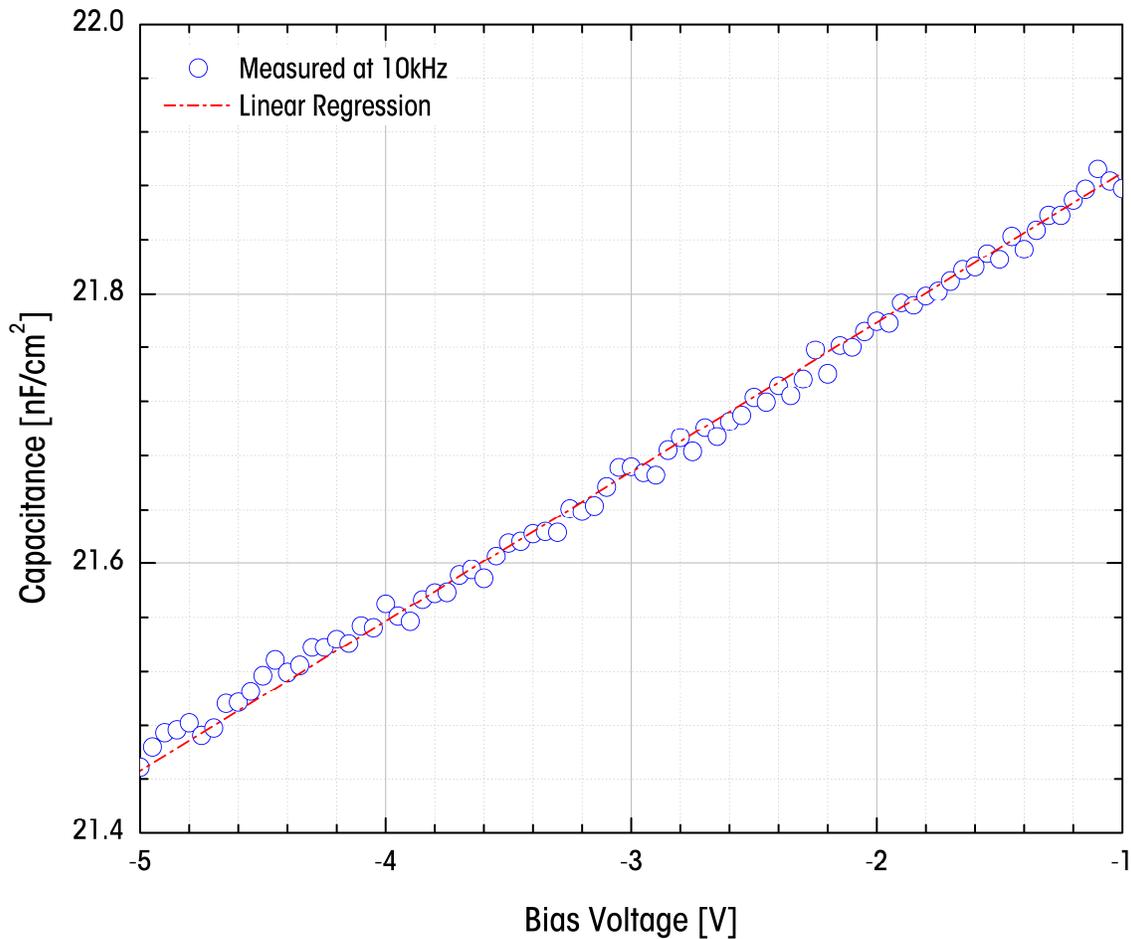


Figure 4–23: Capacitance–voltage characteristics of a $1\times 1\text{mm}^2$ a-Si:H n – i – p photodiode deposited on glass substrate measured at 10kHz.

The near linear voltage dependence shown in Figure 4–23 can be modeled with the addition of an extra voltage dependence term in Equation (2.40),

$$C_j(V) = \frac{\epsilon_o \epsilon_r A_j}{W_d} + \gamma_c A_j V \quad (4.37)$$

γ_c is the voltage dependence proportionality constant extracted as $\sim 0.11 \text{ nF/V}\cdot\text{cm}^2$. The γ_c parameter is also dependent on the photodiode size: γ_c decreases with photodiode junction area.

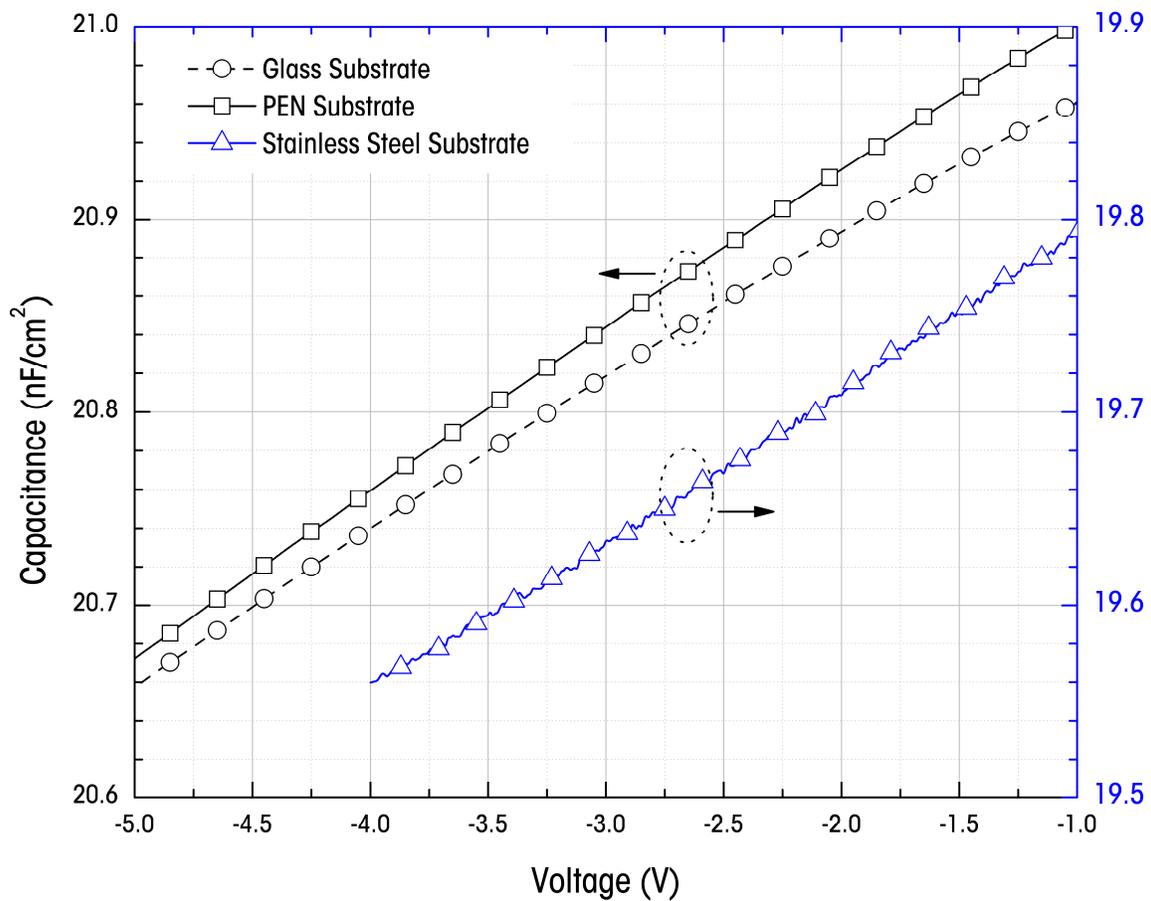


Figure 4-24: Capacitance–voltage characteristics of $1\times 1\text{mm}^2$ a-Si:H *n-i-p* photodiode deposited on various substrate materials. The measures are conducted with 10kHz signals.

The capacitances for photodiodes fabricated on robust substrates are also measured. The results are shown in Figure 4–24. The stainless steel substrate samples seem to yield a slightly lower capacitance; however, the bias dependence of the measured capacitance does not vary. In other words, the value of γ_c appears to be independent of the substrate materials.

Even though the voltage dependence of the capacitance can be modeled easily, it may cause significant increase in the simulation runtime due to coupling of the voltage variable. As the variation of the capacitance due to voltage is small (<1%), the voltage dependence of photodiode capacitance can be ignored, or best implemented as a selectable option for simulators.

4.1.5 Quantum Efficiency

The quantum efficiency of the segmented a-Si:H $n-i-p$ photodiode depends on a number of processing parameters such as the thickness of the intrinsic a-Si:H i -layer, thickness of the p -layer, and thickness of the AR coating. The quantum efficiency can be estimated by

$$\eta_{qe}(\lambda) = \eta_c T_{ITO} \exp(-\alpha_\lambda t_n) [1 - \exp(-\alpha_\lambda t_i)] \quad (4.38)$$

T_{ITO} is the transmittance of the ITO film, t_n is the thickness of the n -layer, and α_λ is the extinction coefficient of the n -layer. The extinction coefficient and the absorption coefficient are related by

$$\alpha = \frac{\lambda_c}{4\pi} \alpha_\lambda \quad (4.39)$$

where λ_c is the wavelength of the *electromagnetic* (EM) wave in vacuum. The thickness of the contact layers may only be estimated and the parameters for the films also need additional measurements. An easier approach is to model the measured quantum efficiency with a polynomial.

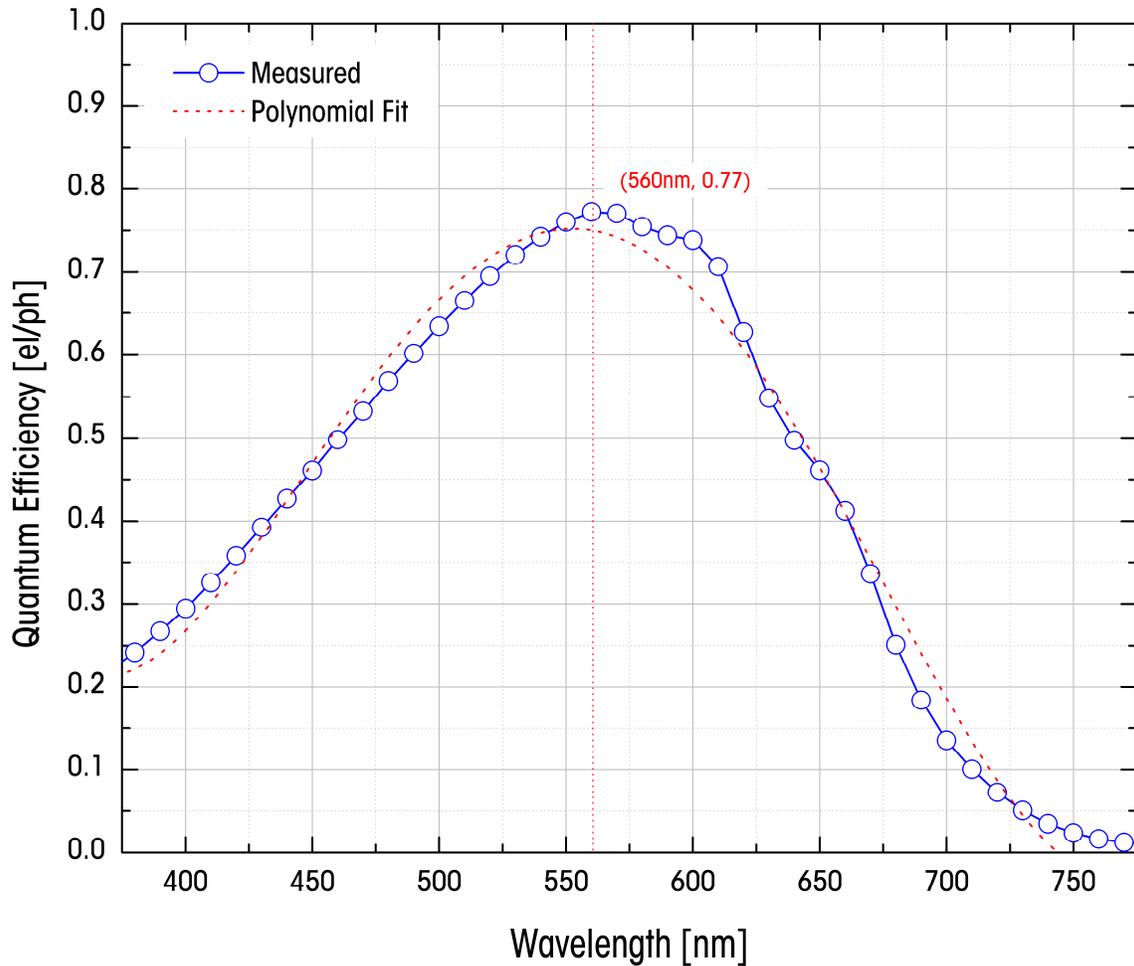


Figure 4–25: Measured quantum efficiency of a large photodiode with *i*-layer thickness of 500nm and *p*-layer thickness of 10nm, plotted against a fourth-order polynomial.

Figure 4–25 shows a typical spectral response curve where the behaviour can be approximated by a fourth-order polynomial. Lower order polynomial generally results in very poor fittings. Higher order

polynomials may provide a more precise fit but with more parameters. Fourth order polynomial is a fair compromise; therefore, the spectral response is modeled by

$$\eta_{qe}(\lambda) = A_4\lambda^4 + A_3\lambda^3 + A_2\lambda^2 + A_1\lambda + A_0 \quad (4.40)$$

The approximate parameter values for $A_0 - A_4$ are listed in Table 4-5.

Table 4-5: A list of parameters and their corresponding values used for the polynomial model of the photodiode quantum efficiency shown in Figure 4-25.

Parameters	A_4	A_3	A_2	A_1	A_0
Values	4.141×10^{-10}	-9.306×10^{-7}	7.512×10^{-4}	-0.257	31.934

The model is also plotted in Figure 4-25 along with the measured values; it is only valid for photon wavelengths between 400nm and 750nm. With the spectral response formulated, the generated photocurrent can be found by

$$I_{ph}(\lambda) = q\eta_{qe}(\lambda)\phi_{ph}A_j \quad (4.41)$$

4.1.6 Current Transients

The physics of the transient current phenomenon for a-Si:H *n-i-p* photodiode is discussed in Section 2.2.6. The evidence of this feature is also observed from device characterization measurements presented in Section 3.2.2. Due to filling and releasing of the trapped charge in the intrinsic layer, there is a finite amount of time needed before the photodiode reaches steady state after illumination. Even though this phenomenon is well observed in many experiments, there is still a need for the development of a simulation model.

On logarithmic plots, the transient current decays are approximately linear, indicating that the trapped charge release through time is governed by a power-law relationship:

$$I_{PD}(t) = A_{ill}t^\beta + I_D \quad t > 0 \quad (4.42)$$

$I_{PD}(t)$ is the time dependent photodiode current; A_{ill} and β are power-law parameters to be extracted from experimental results. The extraction process is similar to those performed for the forward bias I_D - V characteristics where a logarithmic plot of Equation (4.42) prompts its modification to

$$\underbrace{\log|I_{PD}(t) - I_D|}_Y = \underbrace{\log|A_{ill}|}_B + \underbrace{\beta}_{M} \underbrace{\log|t|}_X \quad (4.43)$$

Linear regression would yield the values of B and M , which can be referred back to the power-law parameters. Equation (4.42) does have a singularity at $t=0$ sec however, where current $I_{PD}(t=0$ sec) is evaluated to be zero. This is obviously not the observations from the measurements. The initial value of the current transient is not zero; it depends on the illumination conditions. To compensate for this singularity, the transient current of the diode is empirically modeled by

$$I_{PD}(t, I_{ill}, \tau_{ill}) = I_{ill} \left(\frac{t}{\tau_{ill}} + 1 \right)^\beta + I_D \quad (4.44)$$

I_{ill} is the maximum output current of the photodiode during illumination, τ_{ill} is the illumination duration in seconds, and β is the trapped charge

release power constant. The extraction of β can be done for $t \ll \tau_{ill}$ using Equation (4.43). τ_{ill} can be extracted through charge integration:

$$Q_D = \int_a^b (I_{PD}(t) - I_D) dt = \int_a^b I_{ill} \left(\frac{t}{\tau_{ill}} + 1 \right)^\beta dt \quad (4.45)$$

a and b are the start and end time of the integration. If the speed of the decay is fast enough ($\beta < -1$), Q_D is bounded for $0 < t < \infty$. Otherwise, Q_D is only bounded for $0 < t < b$. In other words,

$$Q_D = \begin{cases} -\frac{I_{ill}\tau_{ill}}{\beta+1} & \beta < -1 \\ \frac{I_{ill}\tau_{ill}}{\beta+1} \left[\left(\frac{b}{\tau_{ill}} + 1 \right)^{\beta+1} - 1 \right] & \beta \geq -1 \end{cases} \quad (4.46)$$

Bias Dependence

The bias dependence of the trapped charge release phenomenon is investigated under dark conditions. Figure 4–26 shows the transient current decay after different reverse bias voltages are applied. $t = 0$ sec marks the initial application of the bias, which is held for $t \geq 0$ sec. At low reverse biases ($< 3V$), the extraction of the parameters can be done easily since the transient current decays monotonically. However, for higher reverse biases, the decay no longer follows a power-law relationship, thus complicating the extraction process. The current increases with time after the initial decay, and eventually reaches a larger steady-state value. Figure 4–27 shows current transient measurement results at various bias voltages

plotted in logarithmic scale. The steady-state current level has been removed. As expected, the current decay follows a power-law relationship.

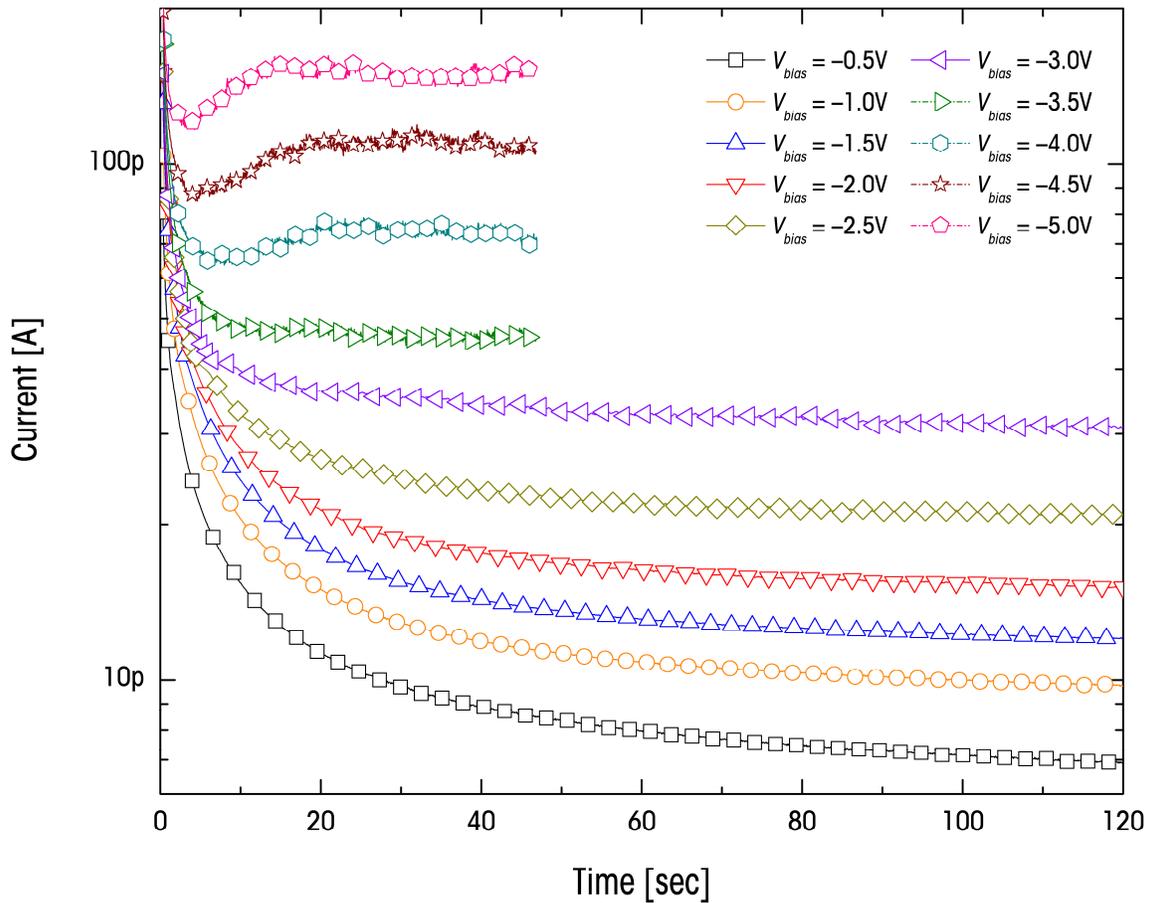


Figure 4-26: Measured current transients at different reverse bias voltages. Low reverse bias voltages result in monotonic power-law decay while high reverse bias voltages cause higher than expected steady-state current levels.

An important conclusion derived from the plot is that the initial current decay constant β is independent of the bias voltage. That is, at different reverse biases, the difference in the trapped charge release rate is negligible. Consequently, there are no advantages to elevate the magnitude of the

reverse bias voltage since that would increase the dark current level while does not decrease the amount of time to sweep out the trapped charge.

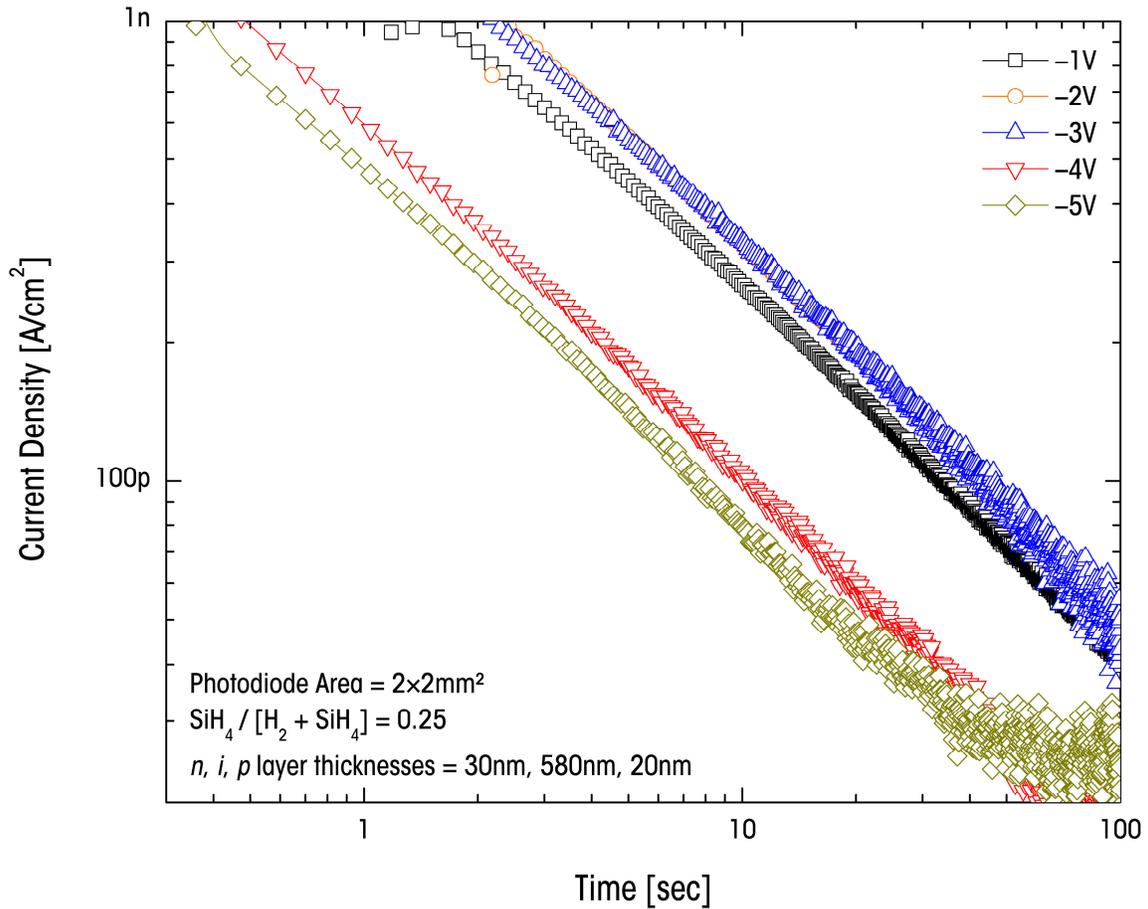


Figure 4-27: Current transient measurement data plotted in double-logarithmic scale. The rate of decay for all reverse biases is equal, indicating that trapped charge release rate is independent of voltage bias.

This answers the question of what the appropriate biasing voltage for the photodiodes should be when used for the HTS applications. Depending on the thickness of the *i*-layer, a sufficient bias must be applied to fully deplete the bulk layer. Meanwhile, the magnitude of the reverse bias should also be as low as possible to achieve low steady-state current level.

These constraints place the appropriate biasing voltage for the a-Si:H *n-i-p* photodiodes between -1.0V and -3.0V.

Illumination Intensity

The transient current decay measurement is also performed under different illumination intensities. The light source is a green LED ($\lambda \approx 550\text{nm}$) energized for two seconds. The variation of the LED intensity is monitored by adjusting its current, under the assumption that the response is linear. The trapped charge release immediately following the removal of the light excitation is recorded and plotted.

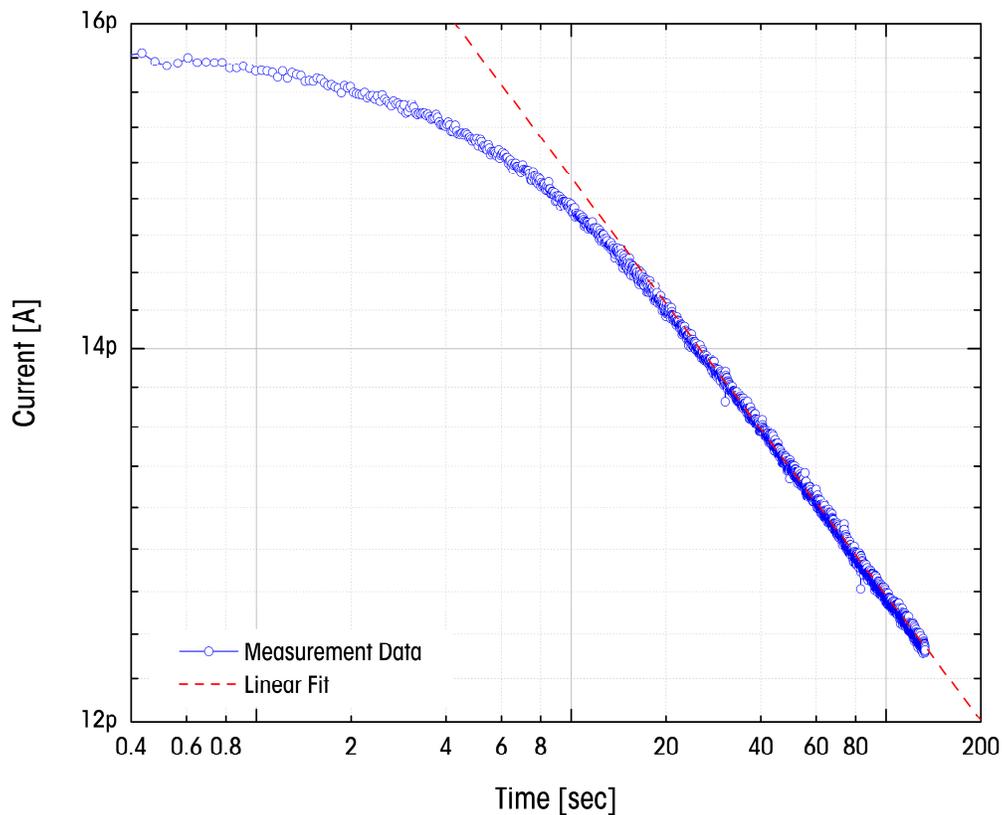


Figure 4-28: Transient current decay due to trapped charge release immediately following low illumination intensities.

Figure 4-28 and Figure 4-29 respectively shows the current transient decay for low and high illumination intensities. Comparing between the two plots, charge trapping of photogenerated carriers in the shallow states are more prominent for high illumination intensities. This is demonstrated by the reduced number of trapped charge released during the initial 10sec, shown in Figure 4-28.

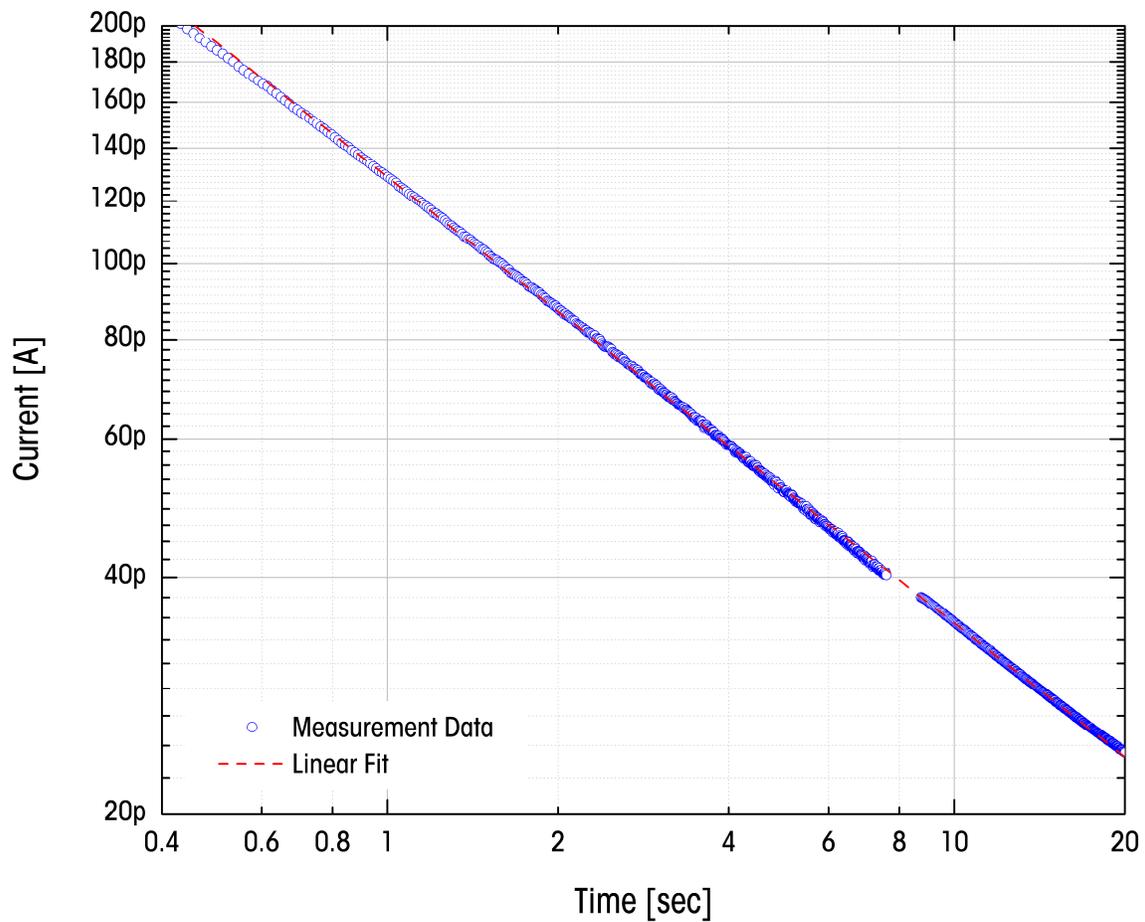


Figure 4-29: Transient current decay due to trapped charge release immediately following high illumination intensities. More trapped charge are released in the initial 10sec indicating that more carriers are trapped in the shallow states.

In contrast, for high illumination intensity, the power-law current decay occurs almost immediately, as shown in Figure 4-29. Once the current decay is measured for different illumination levels, a family of curves can be generated, such as the one shown in Figure 4-30. From the curves, it can be concluded that the fractions of filled traps increases with light intensity, though the total number of trapping center is finite where higher illumination would only yield the same $1/t$ decay.

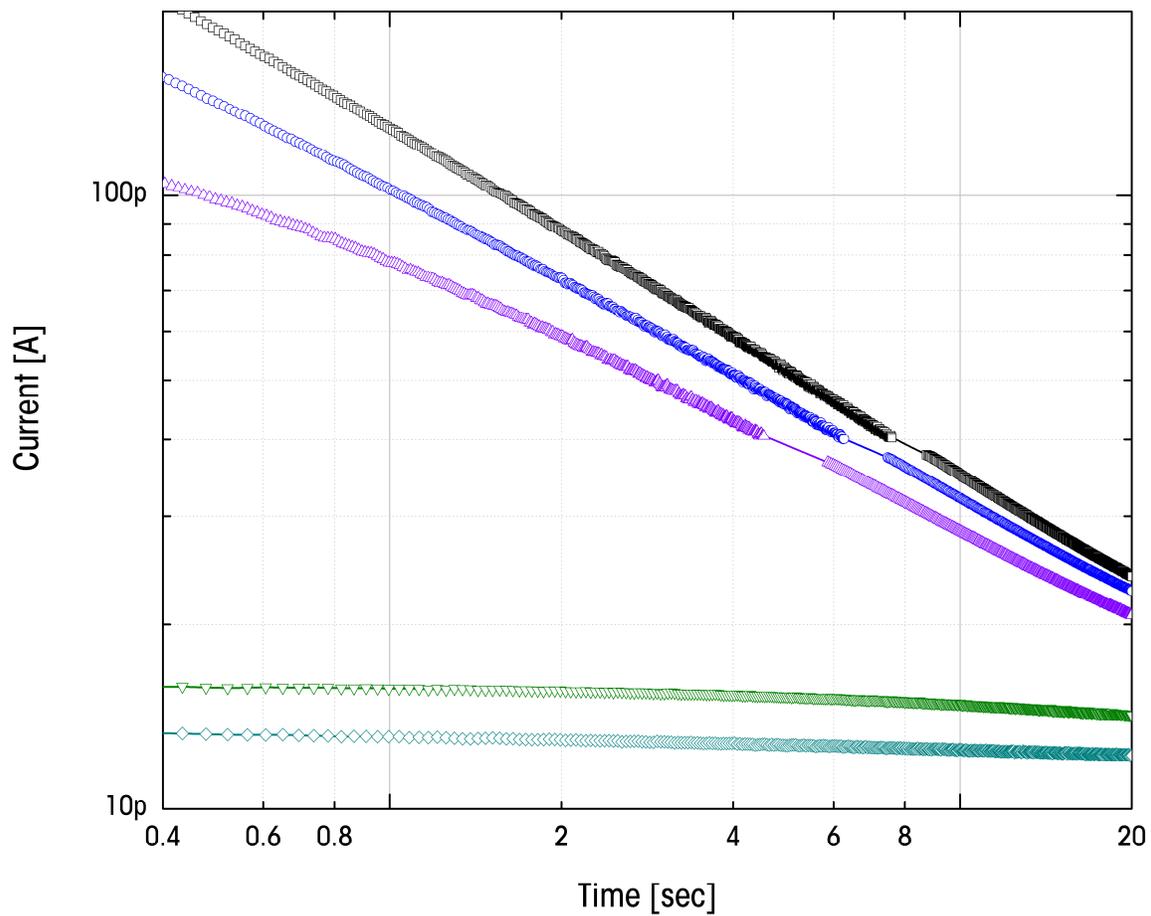


Figure 4-30: Transient current decay due to trapped charge release immediately following various illumination intensities.

The parameters for different illumination current are extracted and plotted in Figure 4–31. Both parameters fit well with a stretched exponential relationship:

$$A_{ill} = B_{A1} \exp\left(-\frac{t}{B_{A2}}\right) + B_{A3} \quad (4.47)$$

$$\tau_{ill} = B_{\tau1} \exp\left(-\frac{t}{B_{\tau2}}\right) + B_{\tau3}$$

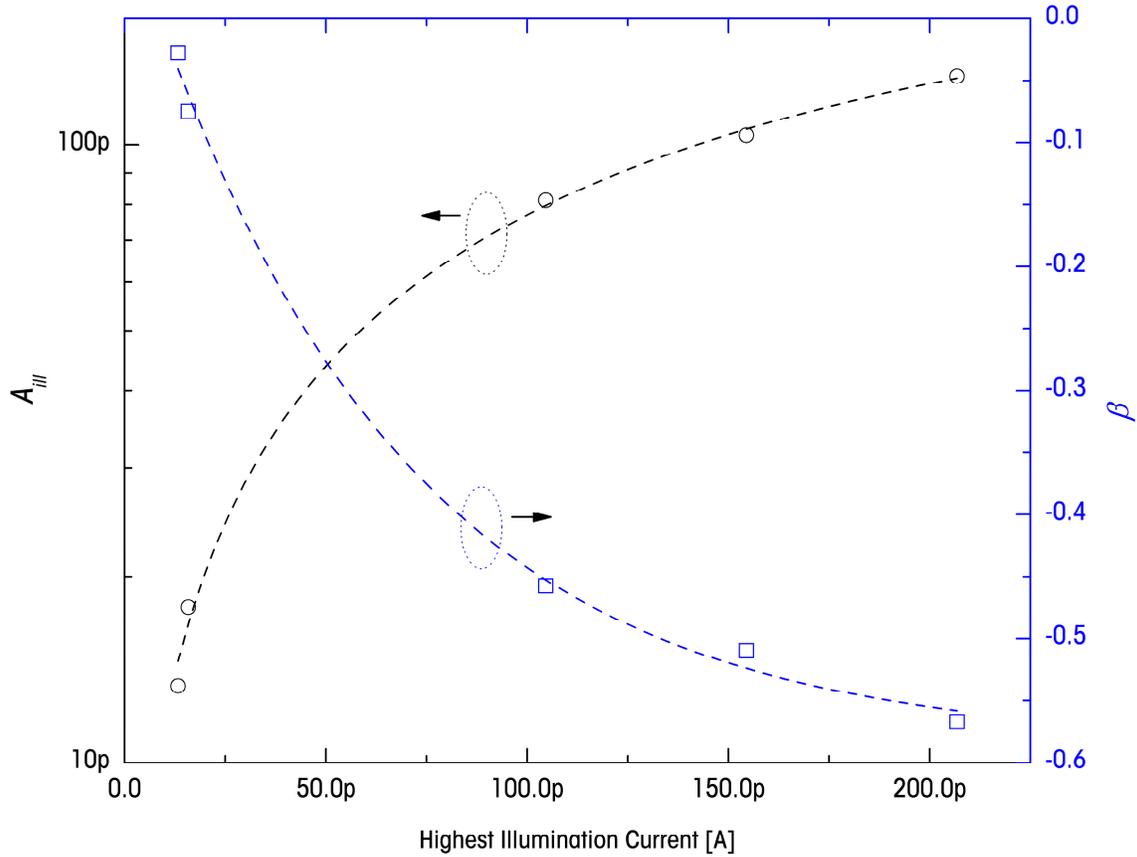


Figure 4–31: Current transient parameters extracted from different impinging photon flux, generating different initial maximum photocurrent.

The extracted values are also shown in Table 4–6 for reference. The calculated values using the current transient model equations are plotted along with the measured values in Figure 4–31.

Table 4–6: A list of parameters extracted from the illumination intensity dependence of the current transient parameters.

Parameters	B_{A1}	B_{A2}	B_{A3}	$B_{\tau1}$	$B_{\tau2}$	$B_{\tau3}$
Values	-2.146×10^{-10}	2.36×10^{-10}	2.174×10^{-10}	0.669	6.475×10^{-11}	-0.586

The light intensity experiment suggests a very important merit for a-Si:H $n-i-p$ photodiodes. If the illumination intensity is low enough, the rate of trapped charge release is drastically reduced for the initial few seconds. This simplifies the needed calculations for number of released trapped charge released through time to compensate for the image lag phenomenon. This is especially important for the fluorescence-based bio-assay application where the emitted light intensity per assay site is low.

4.2 Model Implementation and Verification

The presented formulation of the a-Si:H $n-i-p$ photodiode model is largely independent of its implementation method. This section utilizes the results of the previous section to present a Verilog-A *Hardware Description Language* (HDL) implementation of the photodiode model. The verification of the model is demonstrated through successful simulations on the popular *Analog Design Environment* (ADE) simulation platform by Cadence [114]. The *Simulation Program with Integrated Circuit Emphasis* (SPICE) based Spectre circuit simulation engine is used.

4.2.1 Verilog-A Photodiode Model

The photodiode model is implemented in Verilog-A HDL primarily due to the constraints introduced by platform integration. Even though popular scientific programming languages such as Matlab and C++ can be used to describe the behaviour of isolated photodiode just as easily, they lack the underlying integration platform needed to simulate along with other circuit elements. Furthermore, these languages are limited by the lack of explicit notations for syntax and semantics to express time dependence and concurrency, which are fundamental attributes needed to describe hardware devices. These attributes holds pivotal importance for describing the current transient behaviours of the a-Si:H *n-i-p* photodiodes. Therefore, analog HDLs such as Verilog-AMS and VHDL-AMS are best suited for the task.

Verilog-A HDL, the continuous-time subset of Verilog-AMS [115], is the industry standard modeling language for analog circuits. Verilog-AMS is a derivative of Verilog HDL that includes a much needed *analog and mixed-signal* (AMS) extension to the original pure digital description language. Verilog-AMS can be used to define the behaviours of an entire analog/digital mixed-signal system. A similar but non-equivalent language, VHDL-AMS (the AMS version of *VHSIC Hardware Description Language* (VHDL)), can also be used to implement the photodiode model. It has the added advantage of strict structuring which aids in documenting the model implementation. In fact, the first implementation of the a-Si:H *n-i-p* photodiode model was done with VHDL-AMS. Due to compatibility

issues with the Cadence ADE however, the modeling task is eventually completed with Verilog-A HDL.

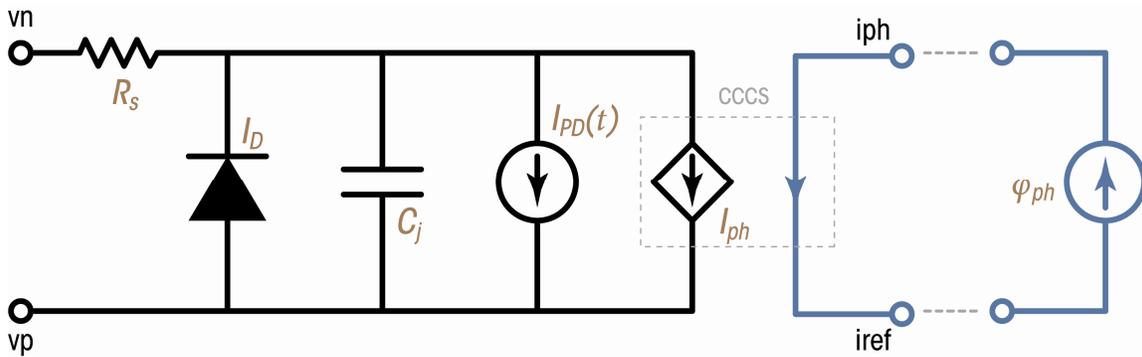


Figure 4–32: A simplified schematic of the equivalent circuit model for the a-Si:H $n-i-p$ photodiode model. The CCCS is used to model the illumination effect.

Figure 4–32 shows the simplified schematic of an equivalent circuit used for the a-Si:H $n-i-p$ photodiode model implementation. The series resistance models the lumped contact resistance of the photodiode. The ideal diode provides the dark quasi-static I_D - V characteristics. The shunt capacitor models the photodiode capacitance that can be used to store the photogenerated carriers. The time dependent current source is used to model the current transient behaviour of the photodiode after a perturbation. As shown in Figure 4–1, appending two extra terminals to the model is one method to incorporate the illumination effects. The *current controlled current source* (CCCS) is used to model the illumination effect of the photodiode. To illustrate this physical phenomenon, an input current is used instead of an input voltage. The input current reflects the physical process of the impinging photon flux towards the photodiode and the generation of the carriers. This current source is placed between terminal i_{ph} and i_{ref} ; current flows into i_{ph} and out from i_{ref} .

The model is integrated into the Cadence ADE by compiling the Verilog-A HDL code followed by instantiation. To start the import process, a library must be created with a unique name containing the Verilog-A cell view. Default VI-based text editor [116], [117] is automatically launched with an empty template, shown in Figure 4–33. The content of the template must be completely replaced by the model code. Upon closing, the code is compiled automatically. Based on the port names specified in the model file, a schematic symbol is automatically generated to map the available ports (Figure 4–34). The properties of each photodiode instances can be adjusted similar to SPICE based components, shown in Figure 4–35.

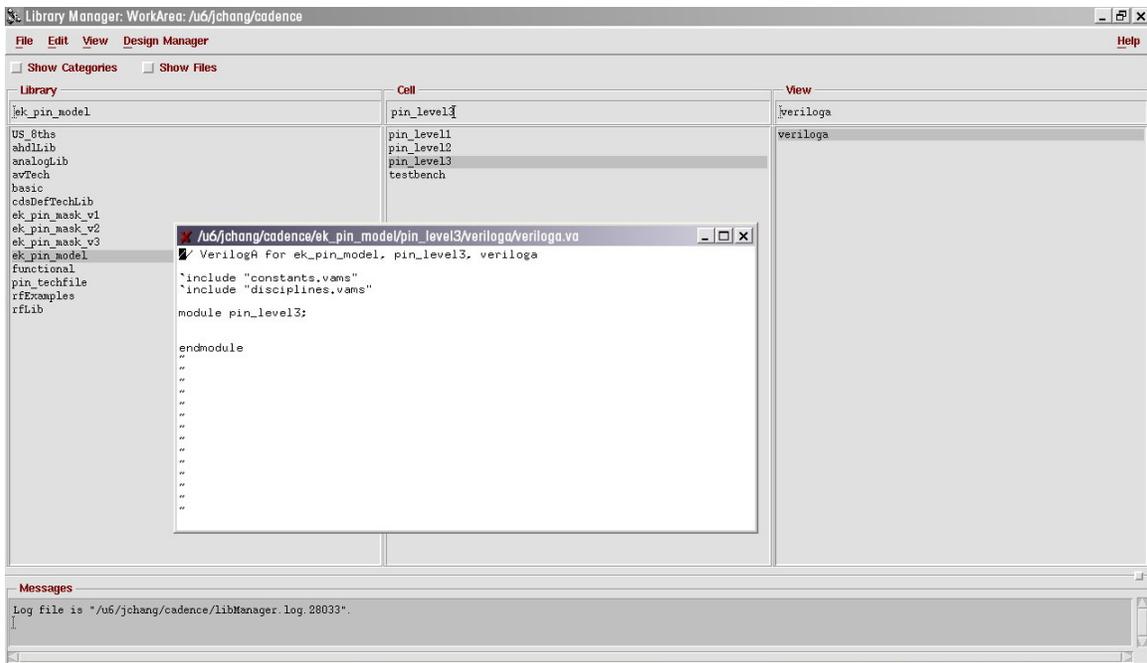


Figure 4–33: A screenshot capturing the VI editor and empty Verilog-A template [118]. The library and necessary cell views are also shown.

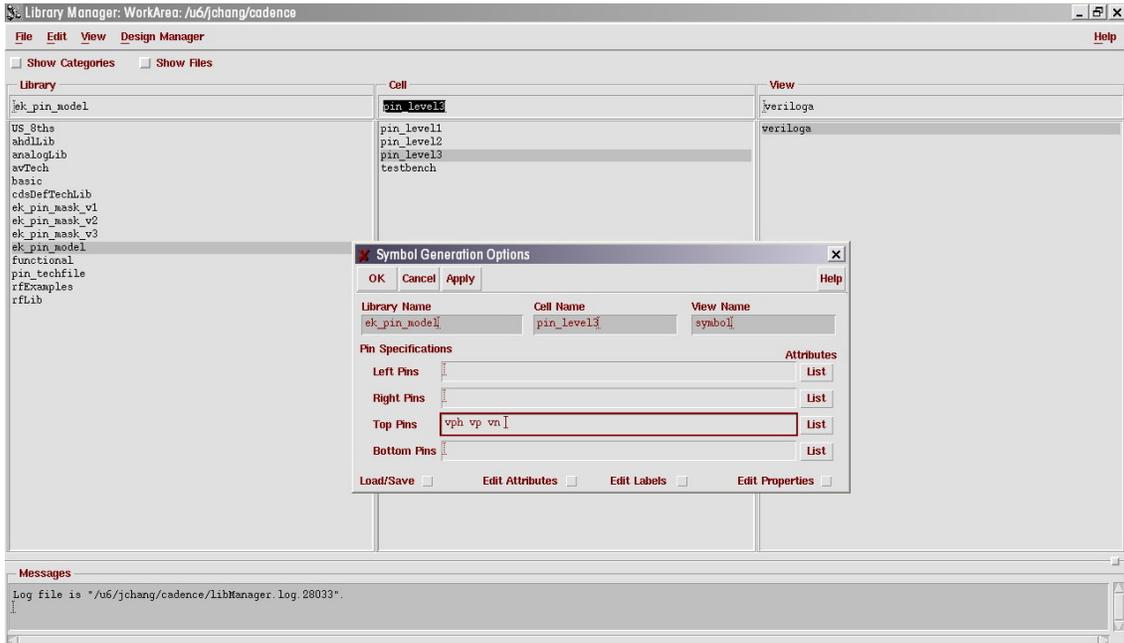


Figure 4-34: A screenshot capturing the automatic symbol generation process [118].

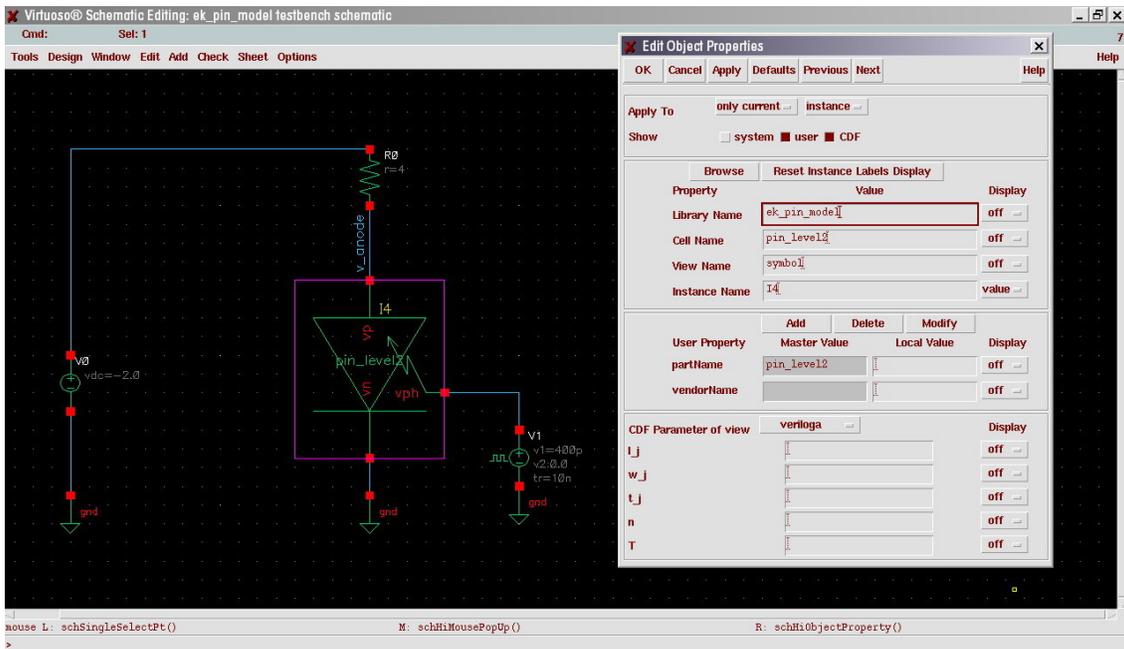


Figure 4-35: A screenshot of the photodiode property panel [118]. All modeling parameters can be adjusted for each instantiation from its default values for specific simulation needs. The parameters can also be changed during simulation.

4.2.2 Simulating Current–Voltage Characteristics

To verify the functionality of the model, a testbench is created to simulate the quasi-static I_D – V characteristics. Figure 4–36 shows a screenshot of the testbench, which includes an instantiation of the model symbol; the `iph` and `iref` terminals are grounded to ensure the resulting characteristics are simulated under dark conditions. A set of default values for the model parameters are included in the model file [118]; therefore, it is not necessary to key in all the values during instantiation. The parameters can be easily adjusted for devices fabricated under different processes.

To ensure that the model behaviour is continuous, the biasing source is first varied from 2V to –10V. Figure 4–37 shows a screenshot of the simulation results executed at 25mV intervals. The photodiode size is set to $250 \times 250 \mu\text{m}^2$ with $1 \mu\text{m}$ i -layer thickness. The solver engine of the simulator did not encounter any singularities. An excellent match is obtained between the simulated values and the measured values from the probe station, confirming the accuracy of the photodiode model.

Taking one step further, a parametric sweep is performed to vary the simulation temperature for each voltage biases. This provides response based on the temperature dependence of the model. Figure 4–38 and Figure 4–39 respectively shows the simulated forward and reverse I_D – V characteristics of the instantiated photodiode in the range of the measurement temperatures. The simulation results also show good matching for characteristics between 20°C and 80°C.

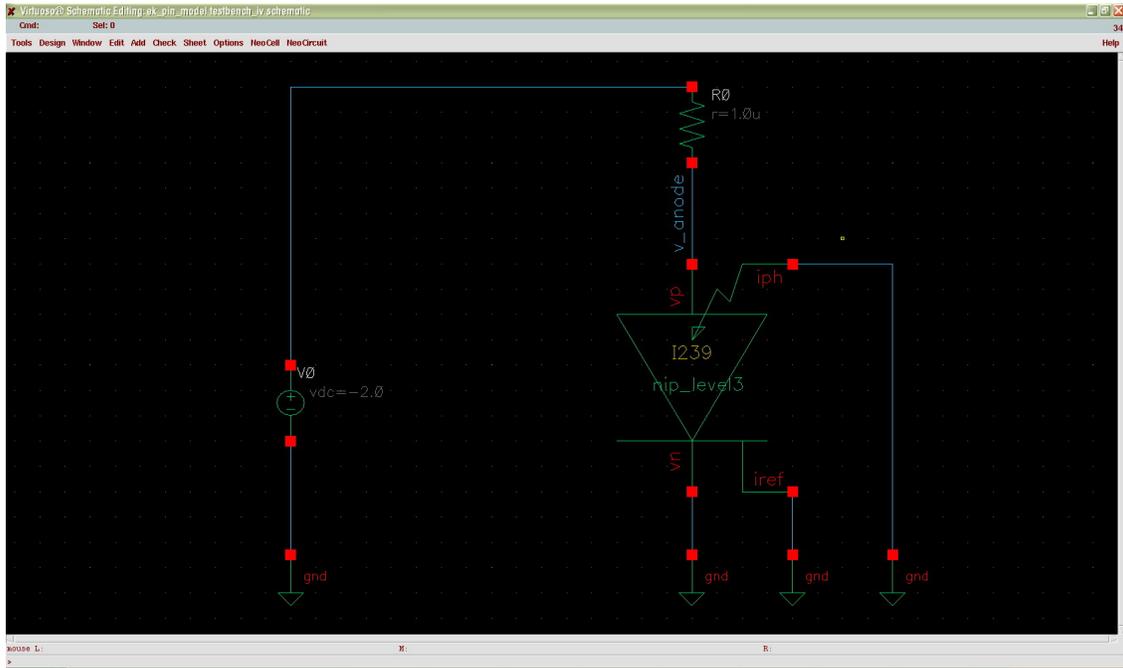


Figure 4–36: A screenshot of the testbench used for quasi-static I_D - V characteristics simulations [118].

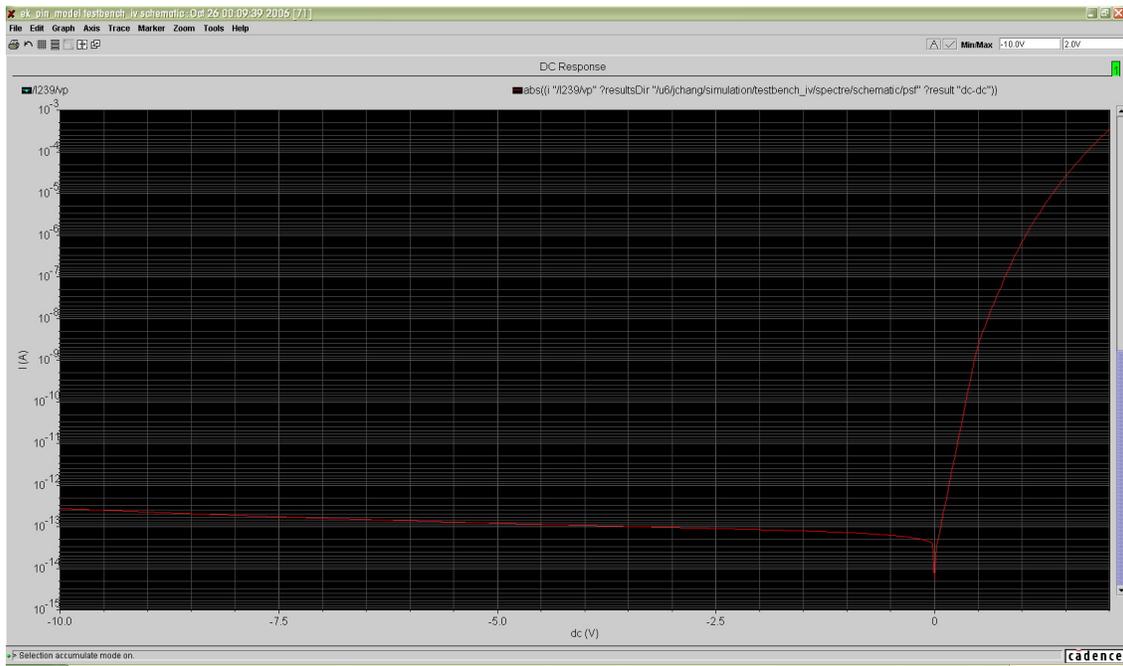


Figure 4–37: A screenshot of the simulation results for quasi-static I_D - V characteristic.

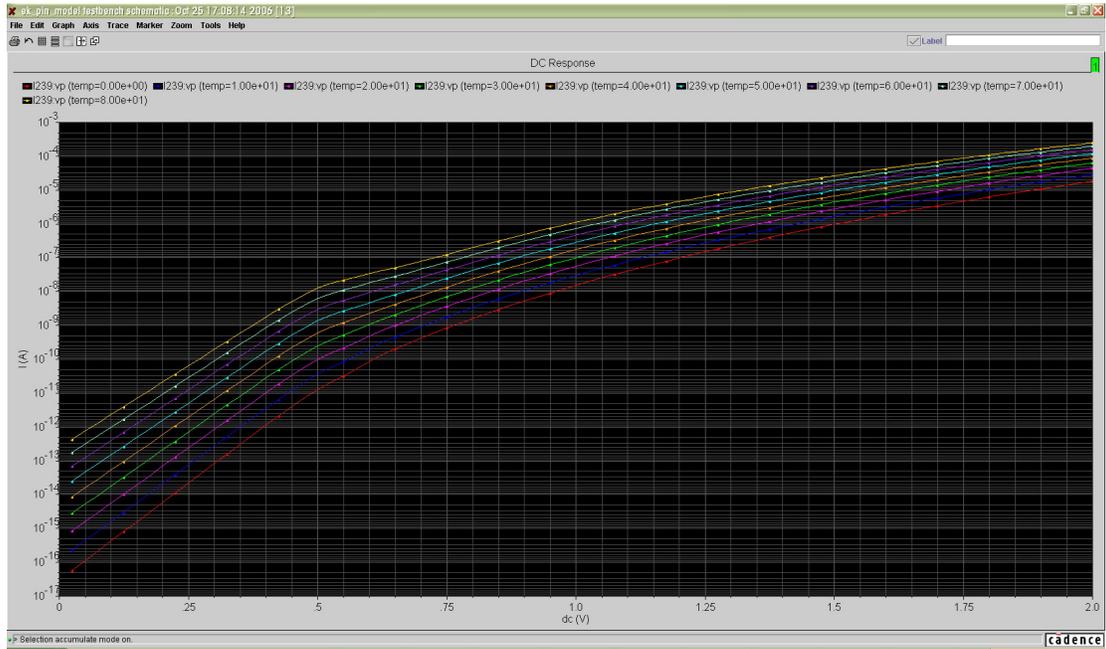


Figure 4-38: A screenshot of the simulation results for forward I_D - V characteristics executed at various temperatures [118].

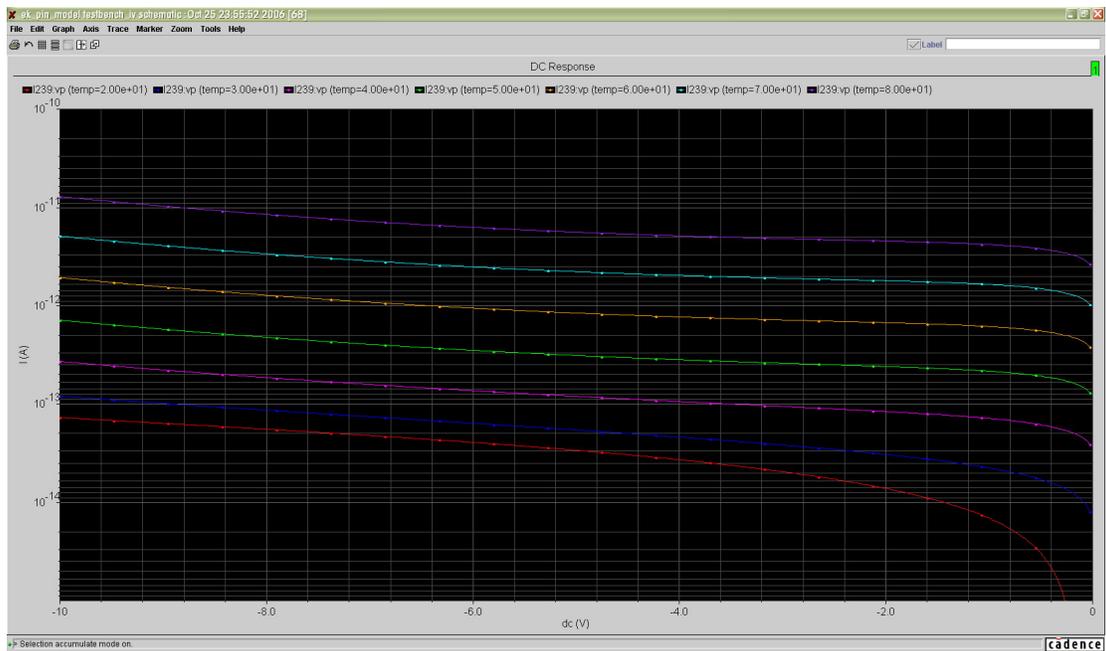


Figure 4-39: A screenshot of the simulation results for reverse I_D - V characteristics executed at various temperatures [118].

4.2.3 Illumination Response of Photodiode

As part of the photodiode illumination response simulation, the quantum efficiency embedded in the model may be evaluated. Figure 4–40 shows the testbench configuration used for such task. A constant photon flux source is placed in the testbench. Since virtually all parameters of the photodiode model can be varied during simulation, the impinging photon wavelength may be adjusted without exception. The photon wavelength parameter is swept from 400nm to 700nm. The spectral response is then given by the total current of the photodiode divided by the total photocurrent value. Figure 4–41 shows the result of the simulation and the resulting curve matches the calculated data given previously.

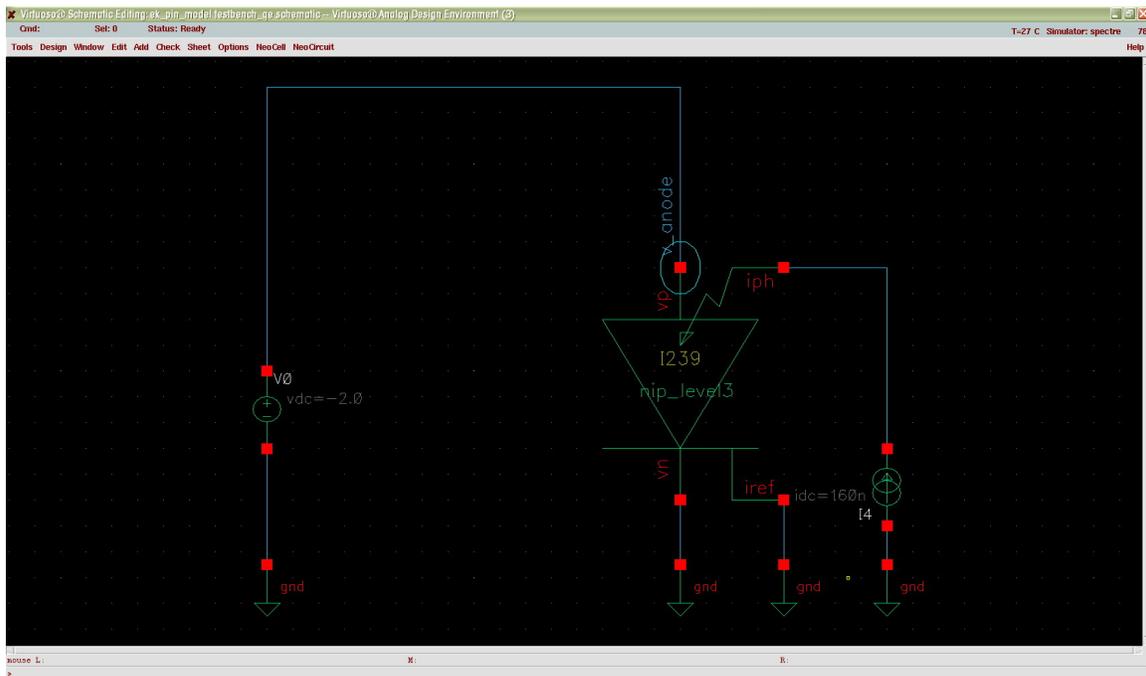


Figure 4–40: A screenshot of the testbench used for spectral response simulations. A total input photon flux of 1 billion photons per cm^2 per second is used as the photocurrent source [118].

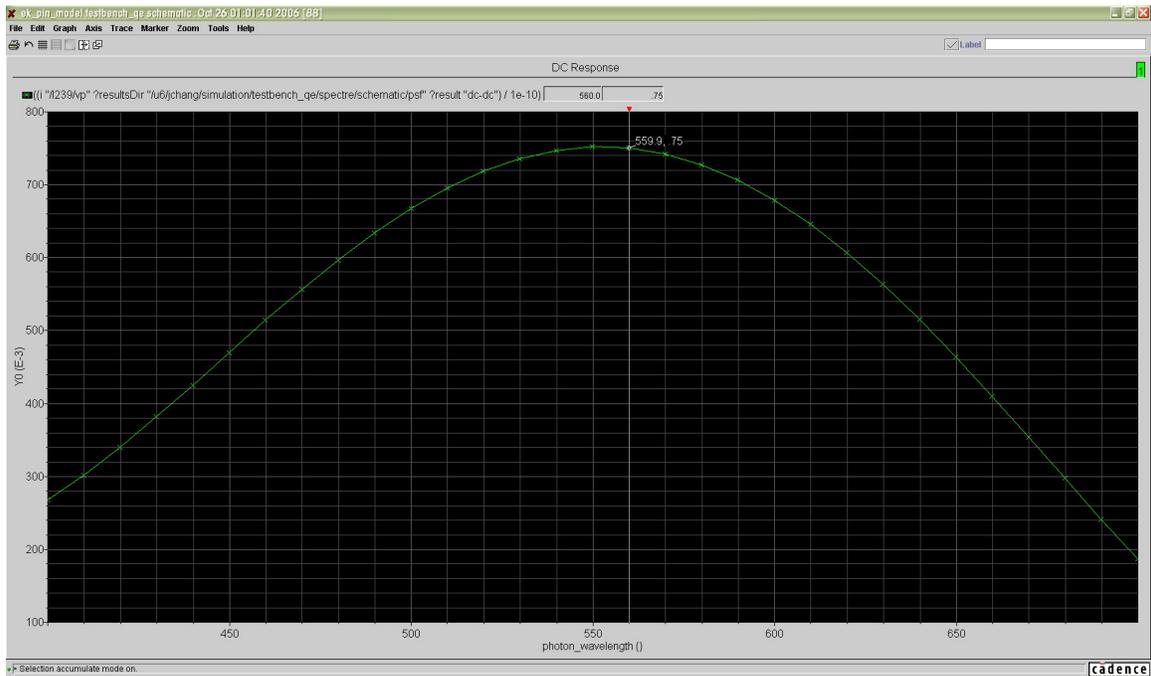


Figure 4–41 A screenshot showing the simulation result of the photodiode quantum efficiency at different wavelength, much like the modeled curve shown in the previous section [118].

If the constant photon flux source is changed to a current pulse train, the testbench would then emulate a flashing light source. Figure 4–42 shows the testbench used for illumination excitation of the photodiode model. The photodiode is illuminated for a short duration (2ms) in between large intervals. The transient simulation result is shown in Figure 4–43. The transient current decay closely approximates what is measured from the probe station. To better illustrate the rate of decay, the transient current is plotted in double logarithmic scale. As shown in Figure 4–44, the current follows the approximate $1/t$ relationship as discussed in the previous section, closely approximate what is measured from the photodiode samples using a probe station.

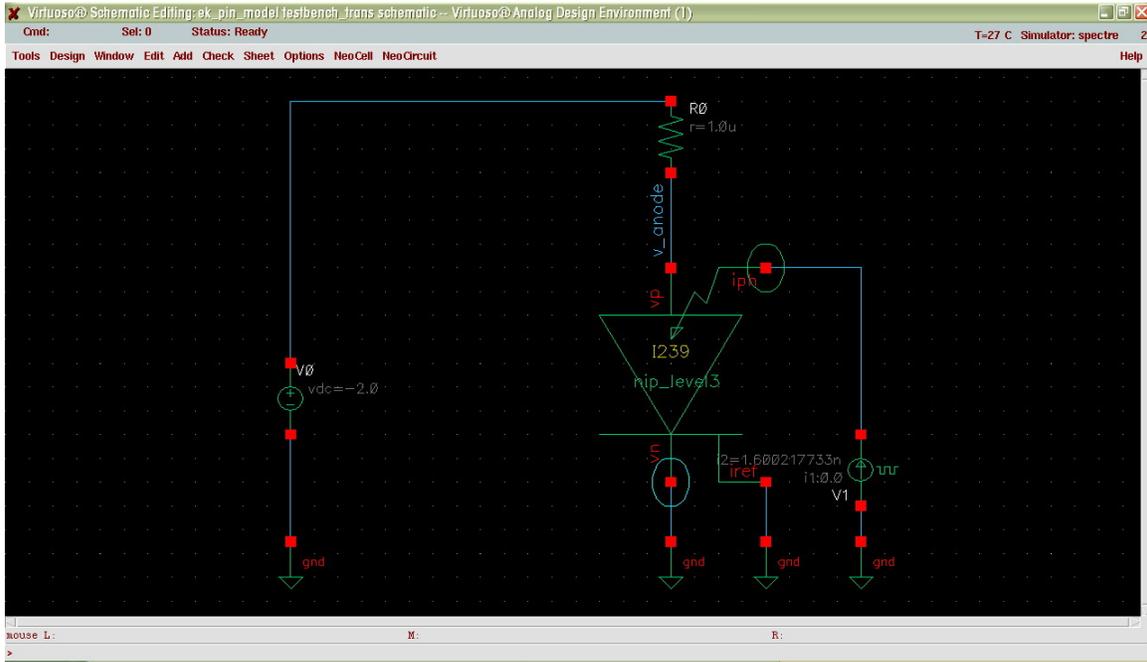


Figure 4-42: A screenshot of the testbench used to demonstrate photodiode transient current simulation [118]. The input photon flux is driven by a current pulse train.

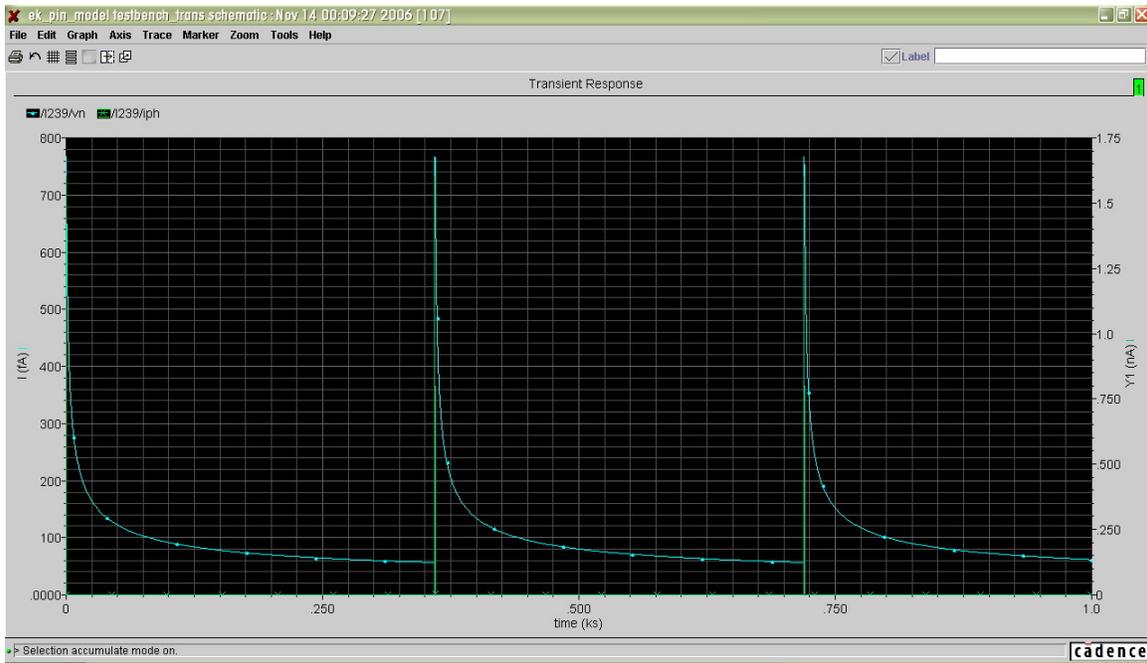


Figure 4-43: Simulated photodiode current transient with periodic excitation [118].

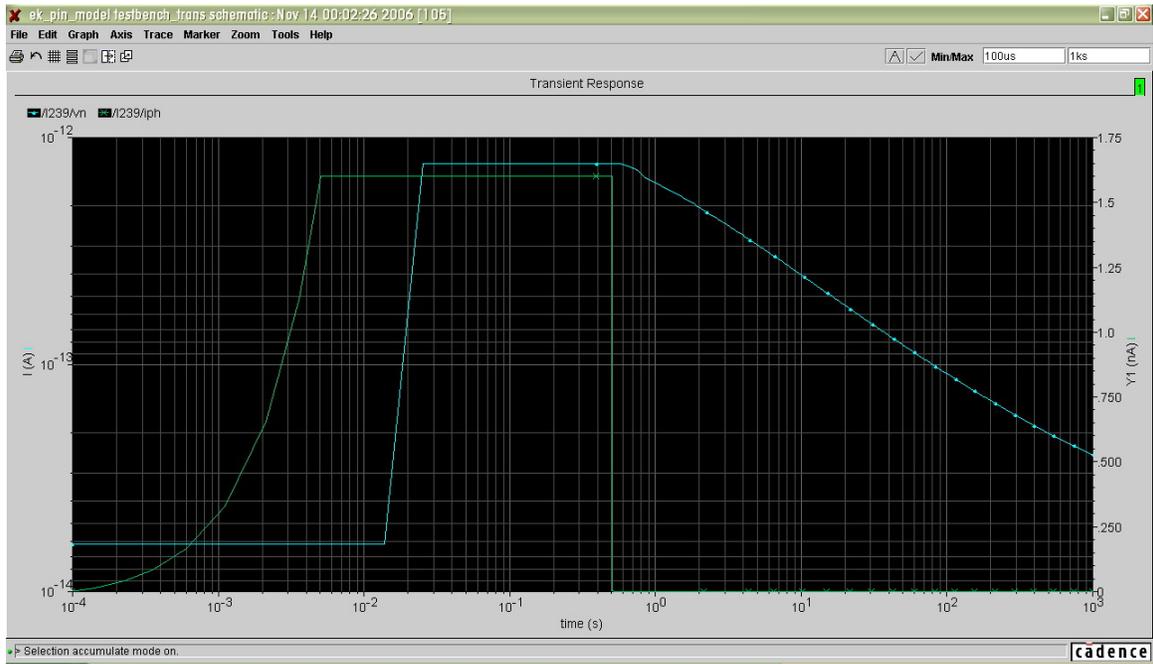


Figure 4-44: Simulation result of a single illumination pulse plotted in double logarithmic scale [118].

4.2.4 System Level Integration

Perhaps the best way to test the a-Si:H $n-i-p$ photodiode model is to simulate its integration with a transimpedance charge amplifier. The amplifier can be constructed using a low input current operation amplifier instance with a single switch-capacitor network as its feedback element. The schematic diagram of this testbench is shown in Figure 4-45. The switch is non-ideal and has an on resistance of $1.5\text{k}\Omega$. Two independent voltage sources are used to drive the reset and the input switches. One pulsed current source is used to simulate the photon flux current. Figure 4-46 shows one of the simulation results. The driving waveform for the charge amplifier and the illumination source is shown on top, while the driving waveform and charge amplifier output are shown on the bottom.

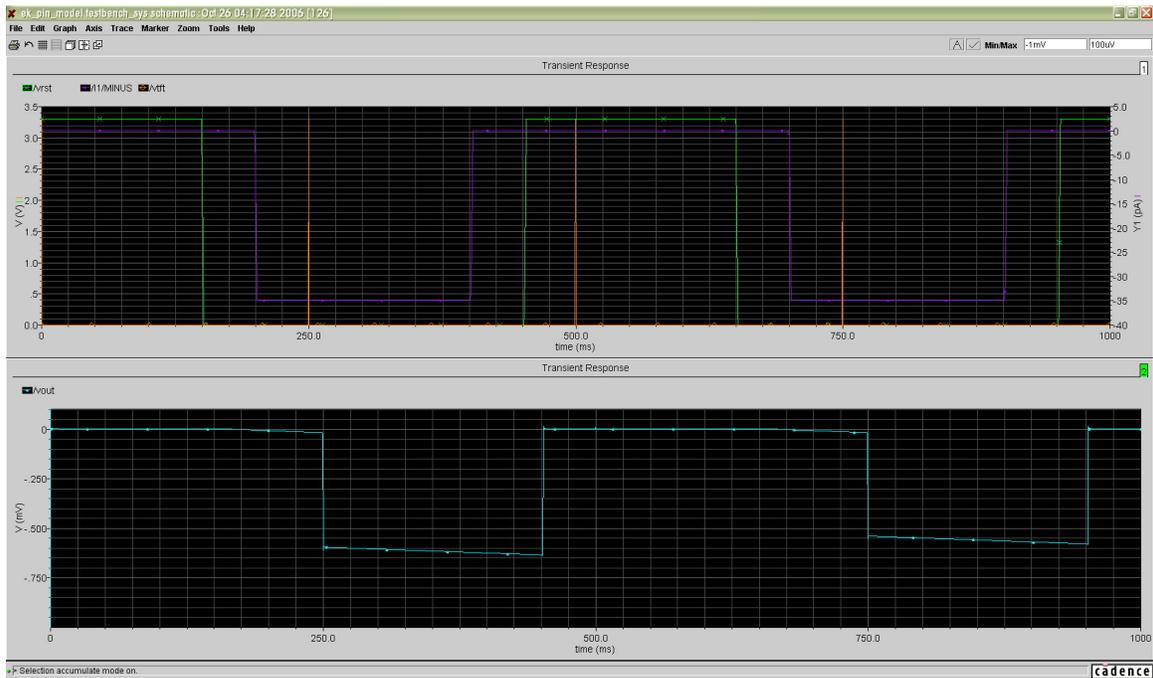


Figure 4–47: Simulation output for short pulsed illumination. The charge stored in the photodiode is read.

As expected, the slope of the charge amplifier output is different for dark and illuminated conditions. The shallow decay is due to the photodiode dark current while the steeper descent is due to photogenerated carriers.

To further demonstrate that the photodiode retains the photo-induced charge in its internal capacitance, a switch is placed between the photodiode and the charge amplifier input (hold switch). The simulation results are shown in Figure 4–47. Similar to previous cases, the driving waveforms are placed on top while the output is placed at the bottom of the figure. The voltage spike on the top graph indicates when the hold switch is closed, such that the charge stored in the photodiode is transferred to the charge amplifier.

The output of the charge amplifier indicates that after applying the illumination with the hold switch open, only small amount of photo-induced charge is leaked though to change the output voltage of the charge amplifier. Upon closing the hold switch, the stored charge floods through and dramatically increases the output voltage. The presented simulations indicate that the photodiode model can be easily integrated with circuit systems to evaluate their performances. Furthermore, it can be easily modified to accommodate characteristic changes due different fabrication conditions.

Chapter 5: a-Si:H *n-i-p* Sensor System for Bio-assays

The gene profiling process presented in Chapter 1 is among the many bio-assays performed routinely. To fulfill the high throughput requirement of HTS, optimized a-Si:H *n-i-p* photodiodes must be integrated together in large numbers to perform massively-parallel detections. This chapter bridges the research work presented in previous chapters with the application requirements of the bio-assays by consolidating the design efforts into a sensor system based on state-of-the-art a-Si:H *n-i-p* photodiodes to detect the emitted fluorescence from common tagging molecules. The design of the system is discussed first followed by its implementation.

5.1 *Sensor Array Design and Fabrication*

The design specifications of the sensor system stem from repertoires of equipments available currently for HTS experiments. Experiment samples are placed side-by-side in an array fashion commonly referred to as microarrays and microwells. Microarrays are typically used for experiments that do not require biological reagents to be continuously immersed in fluids; otherwise, microwells are used. Microwells tend to have larger site areas and inter-site spacings due to constraints of the currently available liquid dispensing systems. Standard microarray plates have dimensions no larger than $\sim 26 \times 76 \text{mm}^2$, limited by the field of view and scanning speed of the CCD or PMT sensor systems. Each assay site is

typically allocated with an area of $50 \times 50 \mu\text{m}^2$, although this number has been shrinking rapidly with the advancement of placement technologies. The analyses provided in previous chapters indicate that the dark current level of segmented a-Si:H *n-i-p* photodiodes near and under this size have significant amount of peripheral contributions that would drown the signal current. This hinders the photodiodes to be useful under low photon flux conditions. The sensor system ought to be designed to target assays performed with microwells where the inter-site spacings are larger, in the range of millimetres.

Figure 5-1 shows an illustration of the microwell plate used to hold sample tissues for drug screening applications. The wells are made of indented grooves on polystyrene, *cyclo-olefin co-polymer* (COC), or glass marked alpha numerically. Standard microwell plates (ANSI-SBS 2004) typically have dimensions of $86 \times 128 \text{mm}^2$, featuring four array sizes; they are 96 (8×12), 384 (16×24), 1536 (32×48), and 3456 (48×72) wells plates. Well depths vary depending on the assay requirements as they dictate the maximum allowable sample volume per site. They typically fall in range of 3.25mm and 4.85mm. Well pitch is manufactured to be precisely 2.25mm for 1536 well plates and 1.5mm for 3456 well plates. Larger well pitch may go as high as 9mm found mostly on 96 well plates. They are been slowly replaced by 1536 and 3456 well arrays due to improved dispensing technology and throughput requirements.

The challenge of the array design is to fully satisfy the requirement constraints while minimizing conflicts between performance parameters.

The size of the a-Si:H *n-i-p* photodiodes are most suited for the 1536 and 3456 well assays. Photodiode arrays with pixel sizes larger than $5\times 5\text{mm}^2$ may suffer yield issues due to macroscopic shunts and stress cracks. Pixel sizes smaller than $50\times 50\mu\text{m}^2$ possesses high dark current density levels due to peripheral leakages, thus prohibiting measurements. Therefore, the physical size of the detectors is designed to be in congruence with the 1536 well plate specifications.

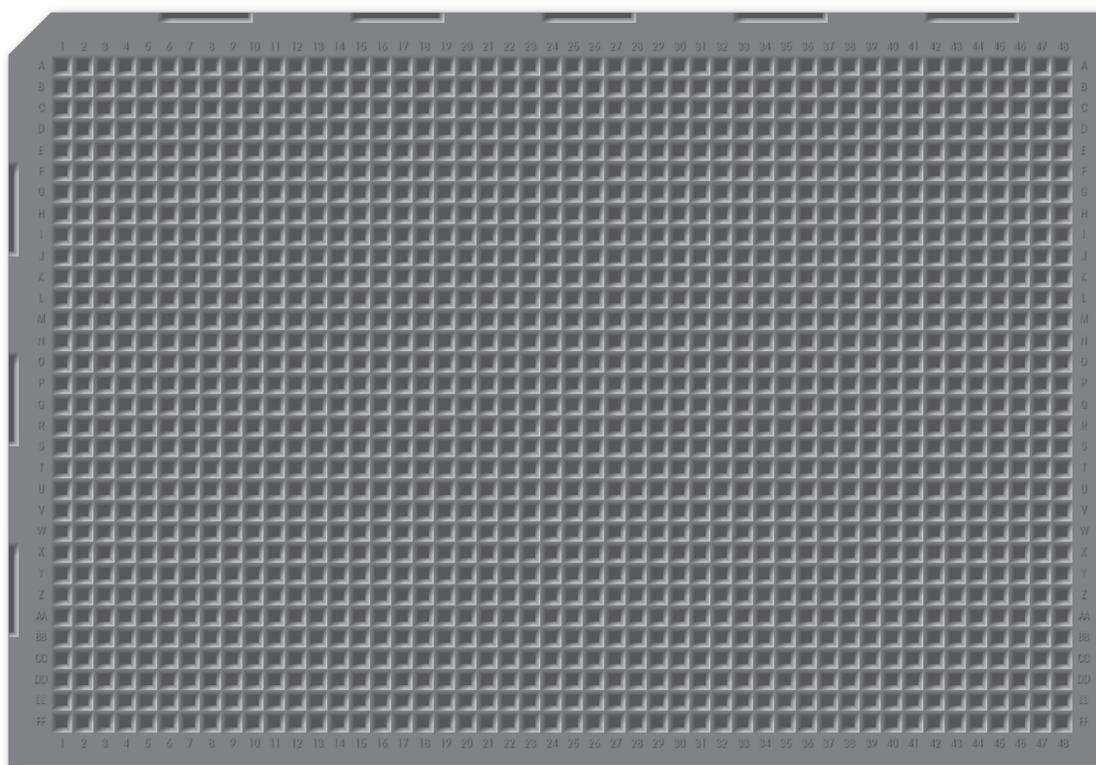


Figure 5-1: An illustration of the 1536 (32×48) wells microwell plate used for fluorescence-based drug screening applications.

The photodiodes are arranged in a two-dimensional rectangular matrix fashion with one a-Si:H *n-i-p* photodiode per assay site. Ideally, the fabricated sensor array would align directly on top of the microwell plates

during readout. Depending on the tag excitation mechanisms, optical filters may be required to isolate the wavelength of interest. The detected signals are stored within each pixel of the array until they are retrieved by readout electronics. This technique also nullifies the need to perform pattern recognitions, such as spot edge detection critical for the current CCD systems, since the detection location for each site is predetermined.

5.1.1 Pixel

Each sensor pixel is designed to hold one a-Si:H sensor and one pixel switch. The pixel switch restricts the photogenerated charge to reside in the sensor during detection phase while providing the path to transfer these signals out from the pixel during readout phase. Figure 5–2 shows two pixel architectures included in the fabricated prototype sensor arrays; they are the single and double switching diode architectures [70], [94], [98], [119].

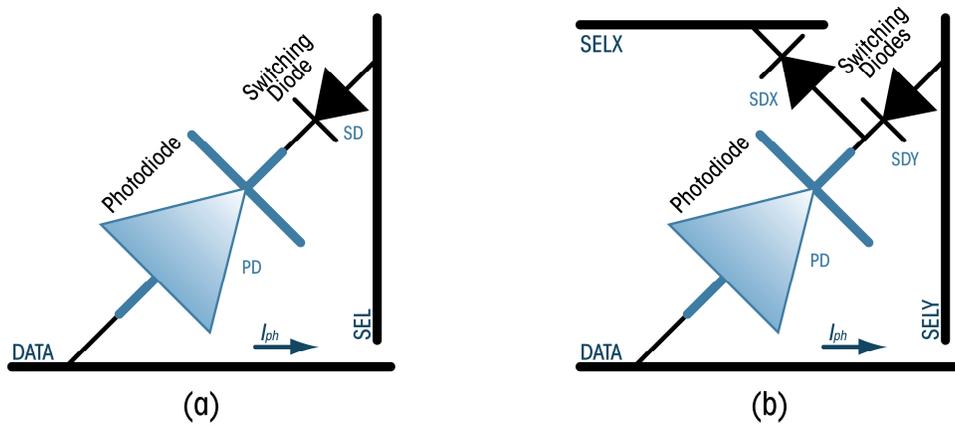


Figure 5–2: Schematic diagram of the single switching diode architecture (a) and double switching diode architecture (b). The switching diodes are physically smaller than the photodiodes to reduce leakage current and improve fill factor.

The diode switching architecture is an attractive alternative for the commonly used TFT switching architecture for *flat-panel imagers* (FPI) [120] since both the switching diode and the photodiode can be simultaneously fabricated. Fabricating the sensor and switching element concurrently reduces the cost and complexity of fabrication, which consequently improves yield. Drawback of using single switching diode architecture is implied through its I_D - V relationship. The exponential increase of the forward bias resistance with decreasing applied voltage affects the charge transfer efficiency between the sensing element and external electronics. Inefficient signal transfer is a significant source of image lag phenomenon. This problem is not critical however if the readout time is long, which is indeed the case for the microwell assays where the frame time is often large. Diode switches also have higher capacitance compared to TFTs resulting in greater signal crosstalk between neighbouring pixels and greater charge transients during switching. To reduce capacitance and signal leakage, the switching diodes are designed much smaller in size than the photodiode. Furthermore, they are also covered with metallic light shield to prevent increase in their reverse current due to incident light when they are in the off state.

The pixel operation principle for the single diode switch architecture parallels that of the TFT-switched pixels. Referring to Figure 5-2a, pixel reset prior to illumination is done by forward biasing the switching diode with a positive pulse on the array addressing line (SEL). This essentially transfers the bias voltage on SEL to the internal node (cathodes of the

photodiode and switching diode). Removal of the addressing pulse holds the internal node voltage since the switching diode would now be in reverse bias. The data line (DATA) is pinned to a reference voltage at all times to ensure the photodiode is continuously placed in reverse bias. During illumination, the charge collection process decreases the floating node voltage while holes accumulate at the anode of the photodiode. The signal readout and reset of the pixel is done simultaneously; while resetting the internal node voltage again with a voltage pulse on the addressing line, the charge held by the photodiode capacitance is released through the data line. Since the bias voltage across the switching diode decreases throughout the reset process, the rate of charge transfer from SEL to the floating node also slows down drastically. The rate of signal charge released to the data line is directly proportional to this rate; therefore, duration needed for complete pixel reset is large.

The double switching diode pixel architecture, shown in Figure 5-2b, alleviates this issue by maintaining high forward current during reset. During pixel reset and signal charge transfer, SELY address line is pinned to the same reference voltage as the DATA line (usually 0V); the SELX address line is held at twice the photodiode biasing voltage. The series resistance of the switching diodes places the floating node voltage at half of the SELX line voltage. During illumination, the voltages on SELX and SELY addressing lines are interchanged to ensure both switching diodes are reverse biased. The capacitance feed-through charge is also eliminated in this configuration as the charge transfer from one diode is offset by an

equal and opposite charge from the other. The trade-off for these improvements is the requirement of an additional biasing line that complicates layout routing and reduces pixel fill factor. Both pixel architectures are built to evaluate their performances. Figure 5–3 and Figure 5–4 shows the top view of the single and double switching diode pixel layout, respectively.

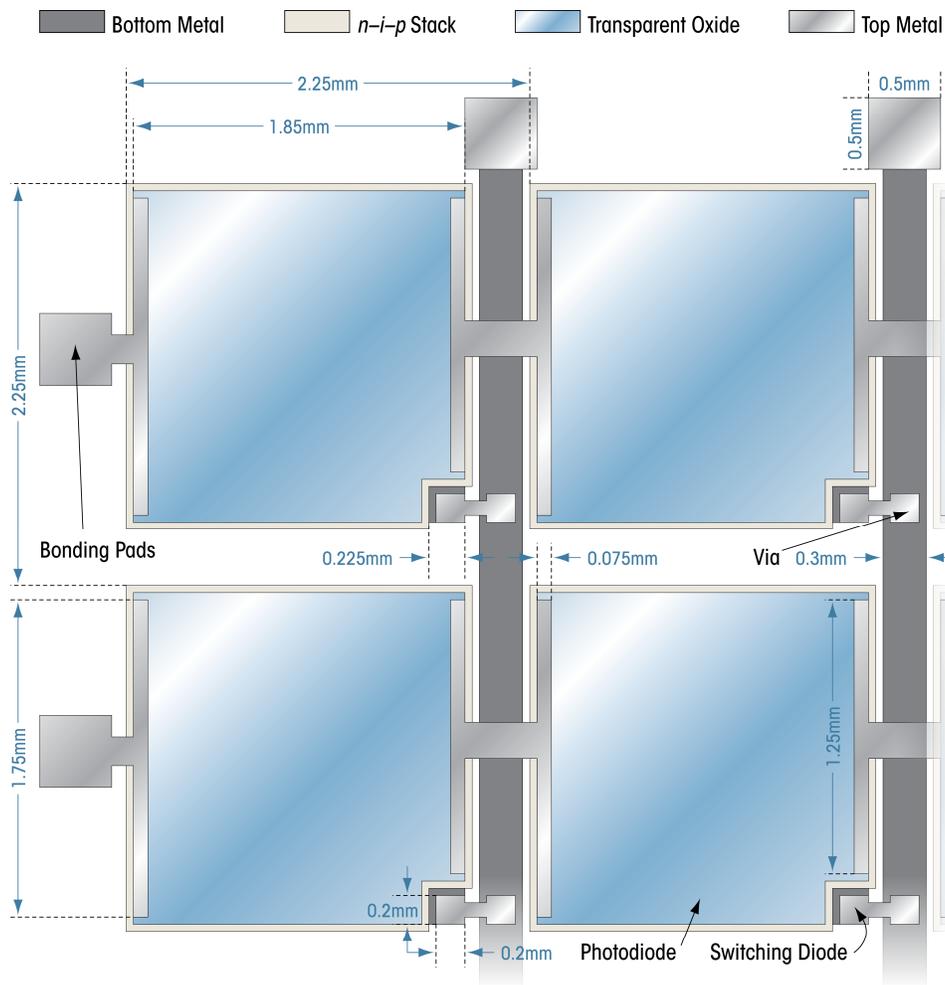


Figure 5–3: Top view illustration of the single switching diode sensor pixel design. Four pixels are shown to mark the critical design rule dimensions which followed the processing rules presented in Appendix B.

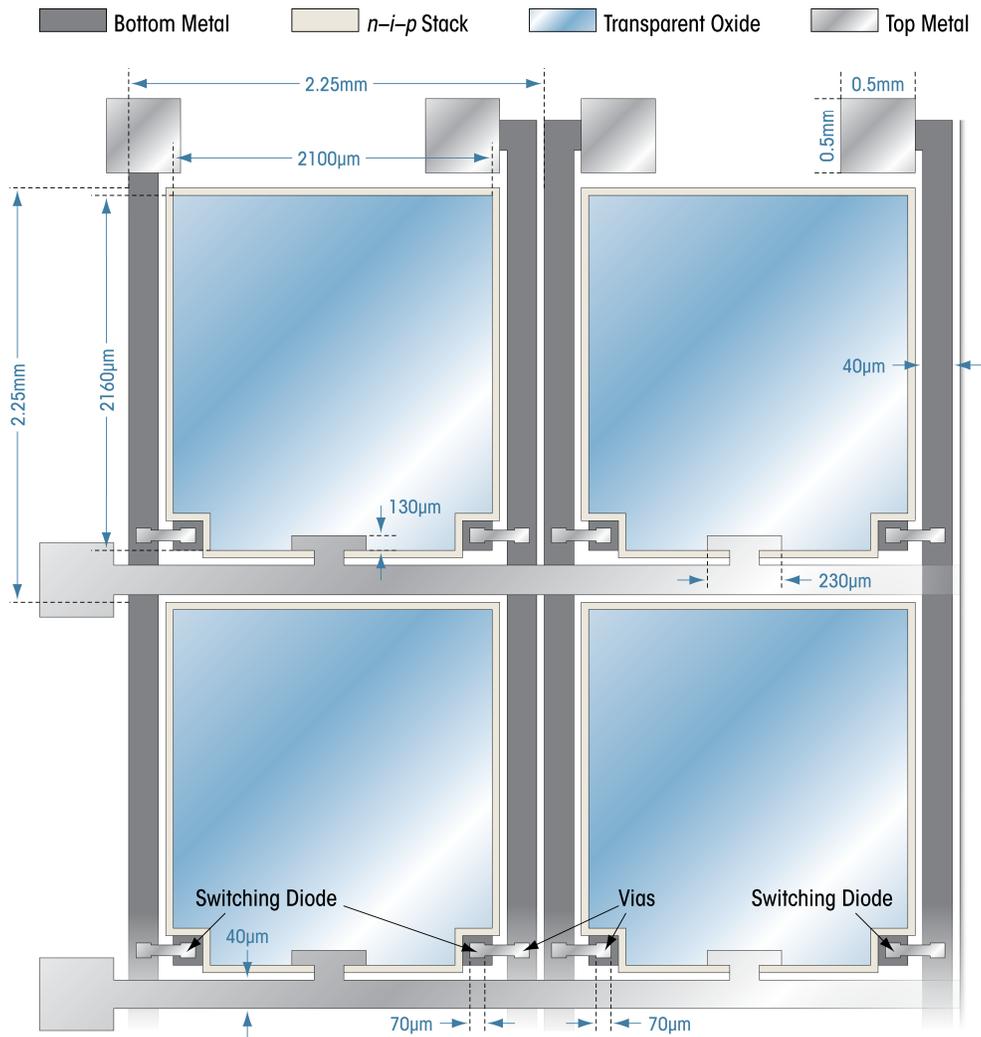


Figure 5-4: Top view illustration of the double switching diode sensor pixel design. Four pixels are shown to mark the critical design rule dimensions which followed the processing rules presented in Appendix B.

The pixels are designed to occupy an area of $2.25 \times 2.25 \text{mm}^2$, matching the well size of the 1536 well plates. The geometric fill factor for the single and double switching diode architectures are $\sim 67\%$ and $\sim 88\%$, respectively. The addressing lines, switching diodes, and vias for the single switching diode architecture design are larger than the double switching diode

architecture to compensate for the inferior charge transfer efficiency. The photodiode capacitances for the single and double switching pixel architectures are $\sim 700\text{pF}$ and $\sim 940\text{pF}$, respectively. Under moderate reverse biases, they are large enough to host carriers generated by even the highest assay signals for minutes; therefore, there is no need to include additional capacitances in the pixel design.

Matrix addressed array, commonly found in large area LCD panels, can be adopted for the sensor array system. Matrix addressing reduces the number of contacts required to access all sensor pixels. The data lines and address lines are placed orthogonal to each other, where their intersections mark the locations for each pixel. Figure 5–5 shows the schematic diagram of an a-Si:H $n-i-p$ photodiode-based sensor array with double switching diode pixel architecture. It is designed for assays with the 1536 well plates.

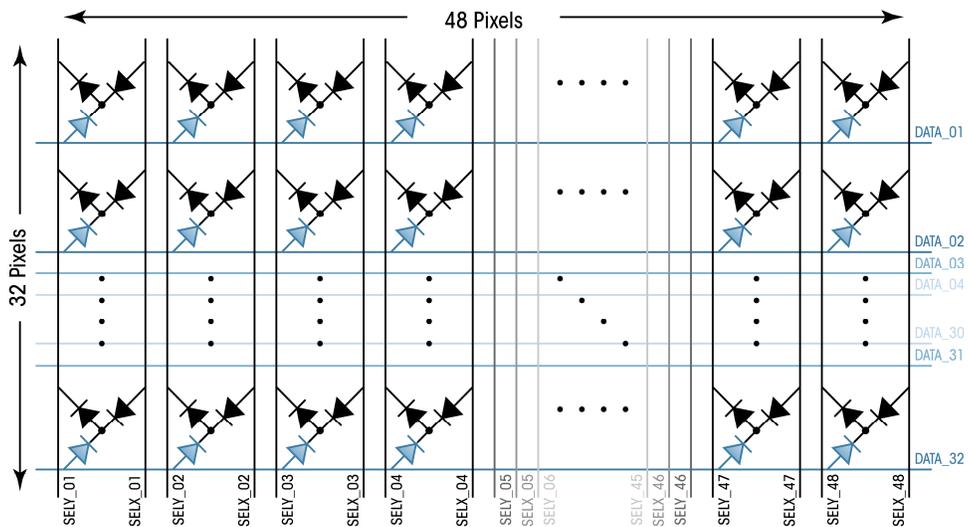


Figure 5–5: Schematic diagram of the sensor array system with double switching diode pixel architecture, targeted for fluorescence-based bio-assays with 1536 well plates.

Due to size constraints imposed by the fabrication system, a 32×48 full-size sensor array cannot be made in-house. Therefore, photolithography mask sets are designed with smaller arrays for both diode switched pixel architectures. The design and layout of the arrays are highly modularized; therefore, the pixel count and individual pixel design can be modified with ease. Figure 5–6 shows a top view diagram of the two prototype arrays. In both array designs, the data lines and addressing lines are orthogonal to each other, providing the matrix formation. The data lines are shared by photodiodes on the same row while address (select) lines are shared by photodiodes on the same column. During charge readout, each column is addressed sequentially; the charge stored in each addressed photodiode is also transferred to the corresponding data line sequentially.

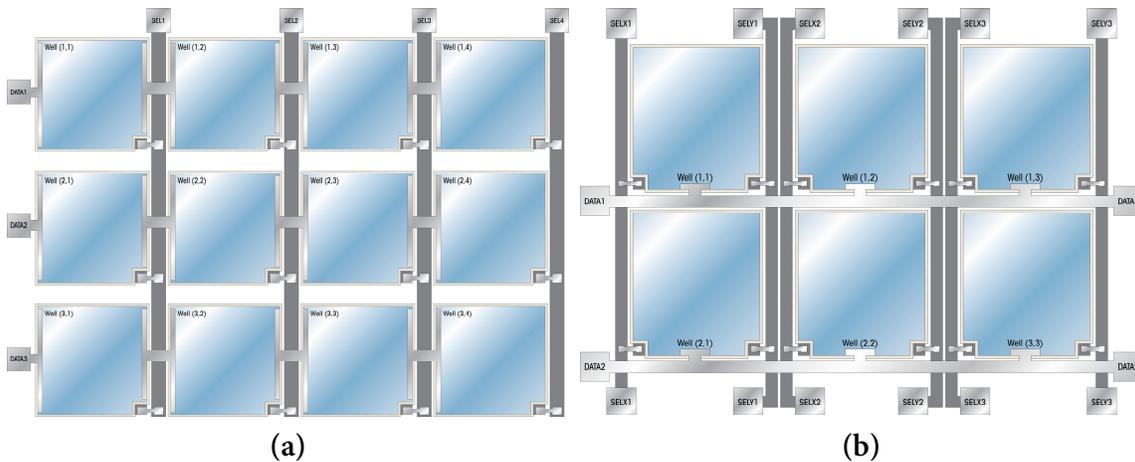


Figure 5–6: Top view illustration of prototype array with single switching diode architecture (a), and double switching diode architecture (b).

Aside from pixel count, one significant difference between the two arrays is the data line routing. For the single switching diode architecture, the data lines are routed with the interchanging Al/ITO top contacts.

Preliminary testing results shows that the data line resistivity is too high ($\sim 150\Omega/\text{pixel}$) for this configuration to be used in large area arrays with high pixel count. The high resistivity is primarily due to the thin ITO film. Therefore, the data lines for the double switching diode architecture are routed with Al only.

5.1.2 Fabrication

The layout task of the sensor arrays is completed using Cadence Virtuoso LE. A screenshot of the double switching diode array layout is shown in Figure A-5. Switching diode architectures allow the switching elements to be fabricated along with the photodiode without any additional photolithography masks. An illustration of the pixel cross-sections for both of the architectures is shown Figure 5-7. The fabrication process follows the recipe for optimized a-Si:H *n-i-p* photodiode which is presented in Section 3.2.1; therefore, they are not discussed here. Perhaps it is worth mentioning that the $\sim 30\text{nm}$ thin Cr sheet deposited to improve adhesion between ITO and Al also reduces the switching diode contact resistance by forming a thin layer of silicide on top of the switching diodes [121].

The fabricated prototype arrays are diced into individual dies and packaged into 28-pin DIP packages. The contact pads of the DIP package are gold plated to provide excellent conductivity. A diagram marking relevant dimensions of the DIP package as well as a photograph of the packaged array is shown in Figure 5-8.

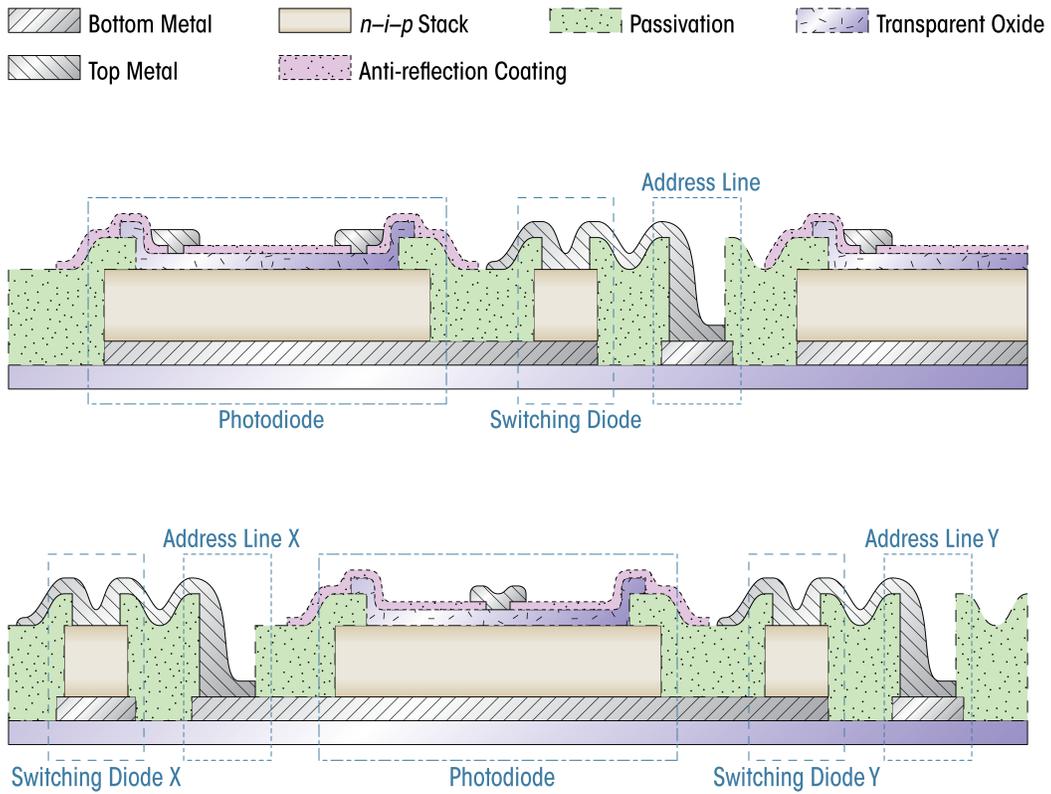


Figure 5-7: An illustration of the pixel cross-section for the single and double switching diode architecture. The fabrication steps are presented in Section 3.2.1.

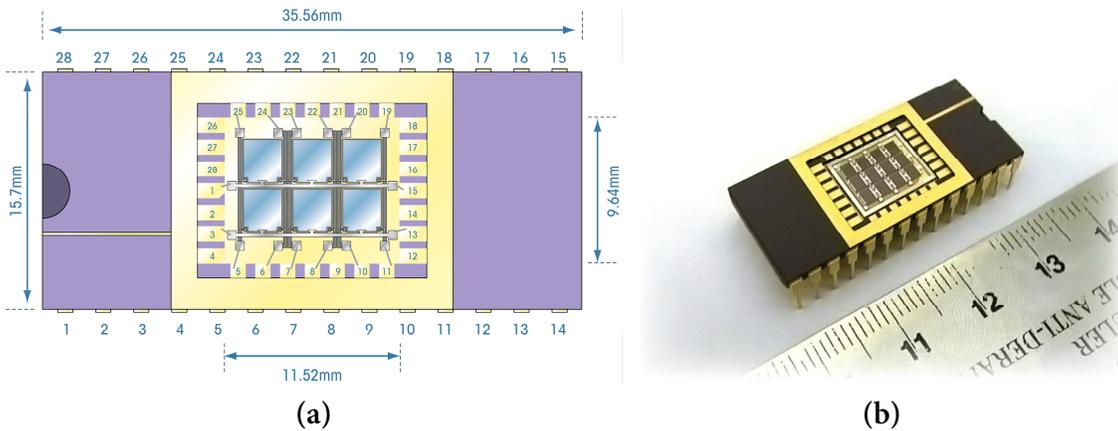


Figure 5-8: Packaging diagram annotating relevant dimensions (a) and a photograph of packaged prototype array with very thin bonding wires.

Fabricated sensor arrays are probed for defects. Over 90% of the fabricated arrays are functional. Arrays with defective pixels typically contain photodiodes that exhibit extremely large reverse dark current values. The quasi-static I_D - V characteristics of the a-Si:H n - i - p photodiodes are selectively measured. Excellent dark current uniformity is demonstrated across different pixels for the functional arrays. The measured values are within 100fA of each other at the same bias voltage. Reverse dark current measurement of the switching diodes are prohibited by its low current level (<10fA). However, forward current of the switching diodes show ideal exponential behaviour between 0.2V and 0.8V with an average ideality factor of 1.42. The rectification current ratio at $\pm 1V$ is approximately $\sim 10^9$, which surpasses the level required for such devices.

Figure 5-9 plots the quasi-static I_D - V characteristics of an in-pixel photodiode. Measured data matches very well with those collected for standalone photodiodes fabricated with the variable-size photolithography masks. The plot shows that central leakage component dominates at very low reverse biases, while peripheral leakage component dominates at bias magnitude larger than 1.5V. The central leakage current level achieved ~ 500 fA at $-1.5V$ bias and remains steady until $-4V$ where slight field dependence is evident. The measured dark current level corresponds to a minimum detectable photon flux of 1.7×10^6 ph/mm²/sec at 560nm without charge integration. For large protein functional assays, 100ms integration time is sufficient to reliably detect fluorescence from each well, while several seconds is needed for smaller oligonucleotides samples.

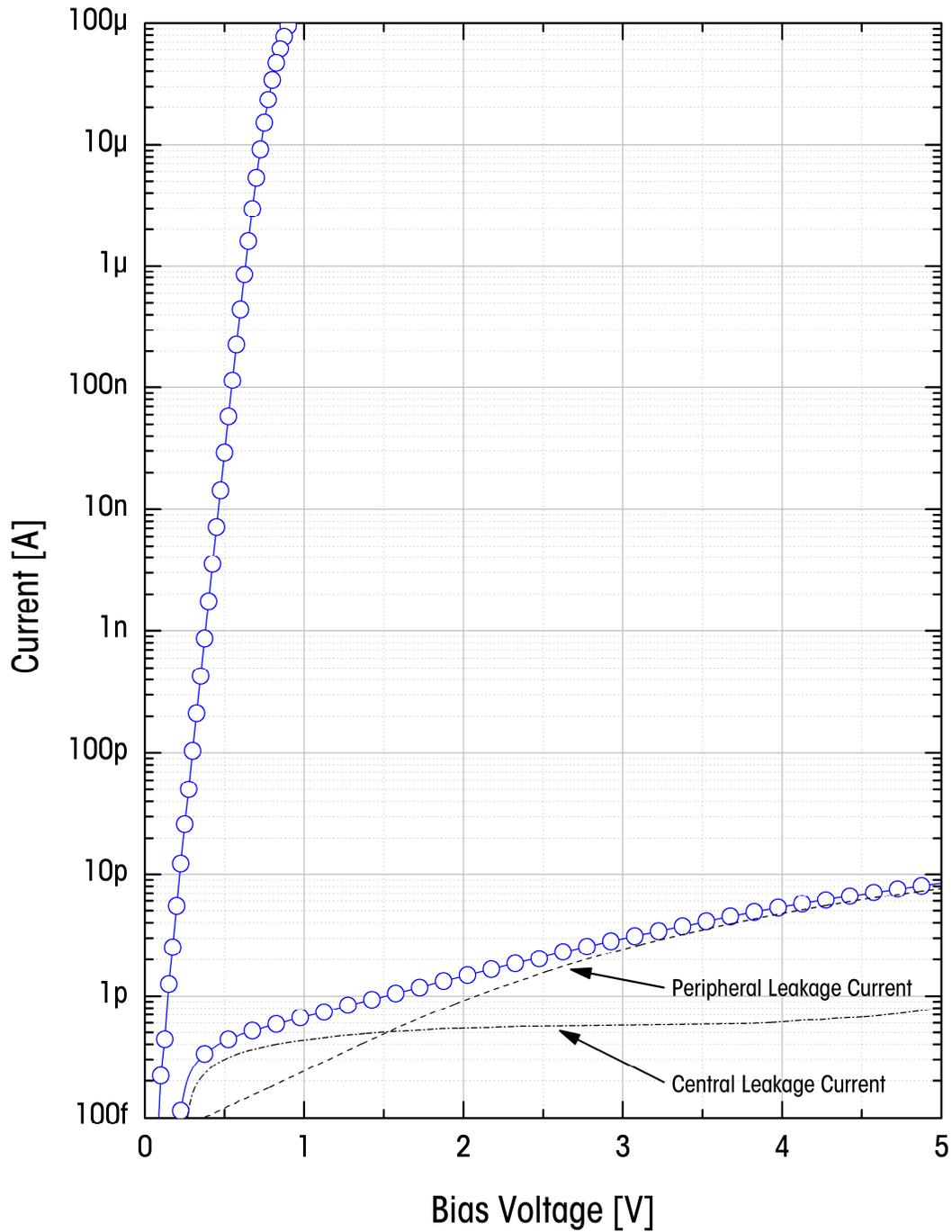


Figure 5-9: The measured quasi-static I_D - V characteristics of a photodiode residing in a sensor array pixel. The central leakage current level at -1V is ~ 300 fA. All measurements are taken at room temperature.

A number of problems were encountered during the fabrication of the arrays. Out of the forty test arrays fabricated, only twenty or so arrays were functional. The first set of arrays experienced adhesion problems with top ITO contact where stress cracks and peeling are commonly found viewing from microscope. Some pixels also have apparent ITO voids although they do not seem to affect the functionality of the sensor. The reduction of the ITO layer thickness resolved this problem at the expense of line resistance. While designing the second pixel configuration, this problem was avoided by using direct Al roughing while sacrificing geometric fill factor. Problem with packaging surfaced when the arrays are bonded to the 28-pin DIP package. The Al layer was not thick enough to provide proper adhesion with the bonding wire. Visual inspection from the microscope showed missing bonding wires after handling of the bonded packages.

5.2 *Peripheral Electronics*

Peripheral electronics are necessary to examine the functionality of the prototype arrays. The peripheral electronics tailor the need in two areas. First, it provides the circuitry needed to readout the photogenerated charge stored in the each of the array pixels. Secondly, it provides the necessary driving waveforms for both the charge readout circuits and the prototype arrays themselves. This section provides relevant information on the design and implementation of the peripheral readout electronics for the fabricated prototype arrays.

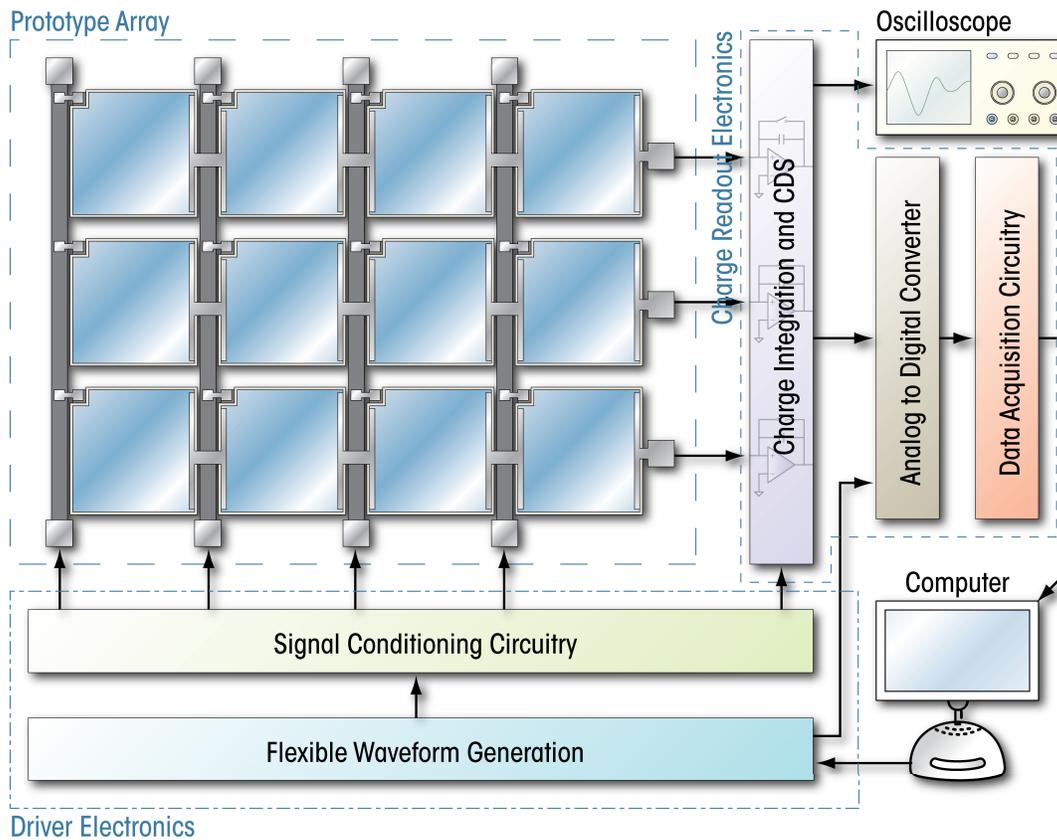


Figure 5–10: A block diagram of the sensor system elements. The arrows indicate the direction of the signal path.

Figure 5–10 shows a simple block diagram of the sensor system, indicating the relationships between each element. Even though the underlying design of the charge readout electronics did not change significantly, the driver electronics have gone through a number of revisions. A low-noise *printed circuit board* (PCB) is built to host the charge readout electronics.

5.2.1 Charge Readout

The charge readout process is performed in two stages. First, the photogenerated charge transferred from the array pixel is converted into

output voltage via a switch capacitor transimpedance amplifier. Then using *correlated double sampling* (CDS) [122], any stray leakage charge that gets on the data line, including the photodiode leakage, is removed.

Figure 5–11 shows the circuit schematic for a single readout channel. The anode of the photodiode is pinned to AGND ($\approx 0V$) by the charge amplifier. When the feedback *RESET* switch of the charge amplifier is closed, the feedback integration capacitor (C_{int}) is discharged, thus successfully resetting it. The charge released by the photodiode is converted into voltage when the *RESET* switch is open. The output voltage of the charge amplifier (v_{amp}) is given by

$$v_{amp}(t) = -\frac{1}{C_{int}} \int_0^{\tau_{int}} i_{ph}(t) dt = \frac{1}{C_{int}} \int_{\tau_{int}}^0 dq_{ph}(t) \quad (5.1)$$

τ_{int} is the duration of charge integration; $i_{ph}(t)$ and $q_{ph}(t)$ are the released photodiode current and charge, respectively. If $i_{ph}(t)$ remains constant throughout τ_{int} , the output voltage equation simplifies to

$$V_{amp} = -\frac{I_{ph}\tau_{int}}{C_{int}} \quad (5.2)$$

It is important to note that the line capacitance (C_{line}) cannot be ignored for large area sensor arrays since its value can be comparable to C_{int} .

Taking this into account,

$$Q_{ph} = C_{int} V_{in} (G_{amp} - 1) + C_{line} V_{in} \quad (5.3)$$

where G_{amp} is the gain of the amplifier. G_{amp} is usually large enough for C_{int} to dominate so that the charge sharing effect between these two capacitances is minimized.

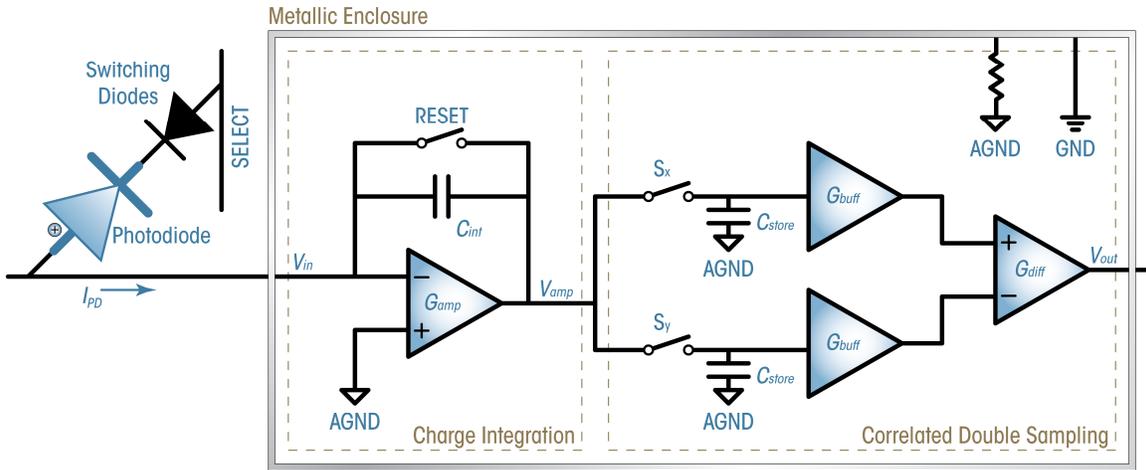


Figure 5–11: Schematic diagram for the charge readout electronics for a single readout channel. The circuit is duplicated for every row of the array with common driving signals. The node annotations are variable names.

The readout can be ameliorated with the addition of CDS circuitry, where the stray leakage currents inevitably integrated along with the signal current (I_{ph}) can be subtracted. To elucidate the readout process, the driving waveform for the schematic shown in Figure 5–11 is provided in Figure 5–12. When switches S_x and S_y are closed, the voltage at the output of the charge amplifier is duplicated across the respective storage capacitors (C_{store}). Therefore, during the reset stage both C_{store} are discharged to AGND. The output of the differential amplifier (V_{out}) is approximately GND (0V) since there are no voltage differences between the two storage capacitors. During the sampling stage, the input current is integrated twice. The first integration attempts to collect all the current

components not due to the impinging photons. The photogenerated carriers remain in C_{ph} , held by the reverse biased switching diode. The second integration attempts to capture all the current components. The addressing line SELECT is pulsed during integration to reset the floating node, concurrently releasing the photogenerated charge. At the end of each charge integration cycle, V_{amp} is sampled to the respective C_{store} . The differential amplifier finds the difference between the two sampled voltages thus yielding the voltage only due to I_{ph} . The same driving scheme can be applied to the double switching diode pixel architecture where the logic of the address lines is complemented.

It is apparent that the timing of the driving waveforms is crucial in ensuring an accurate readout. Since the output voltage is directly proportional to the integration time, τ_{int} for both integration periods must be the same. Otherwise, current component aside from I_{ph} will not be completely cancelled by subtraction. The photodiode leakage current level are also slightly different for the two integration periods due to the differences in photodiode bias before and after the release of the signal charge. This again indicates that the dark current component cannot be completely cancelled by subtraction. The period for both the integration time and sampling time (τ_{sam}) must be long enough to ensure most if not all the charge are successfully transferred.

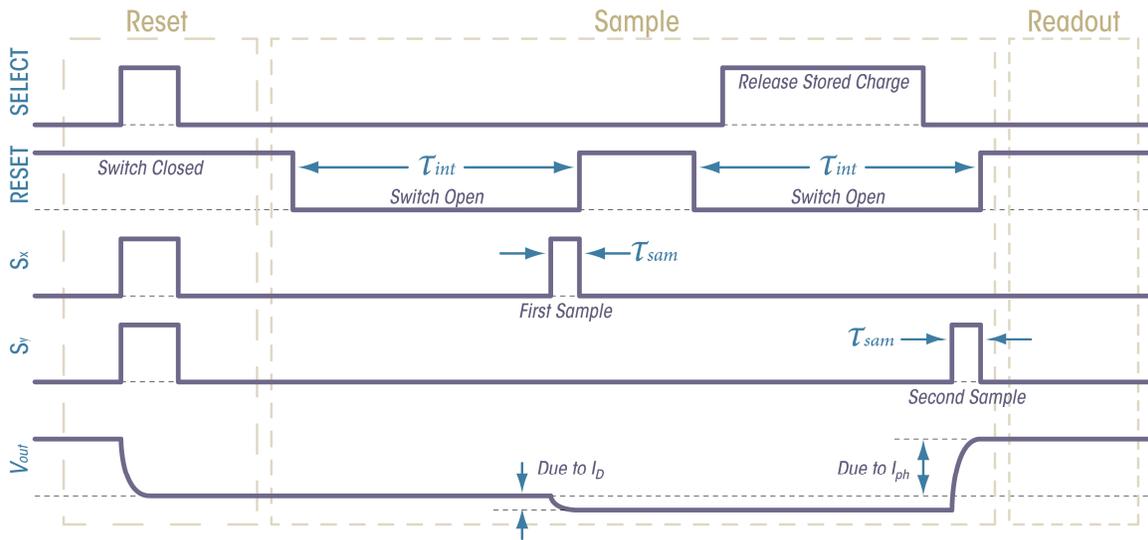


Figure 5–12: The timing diagram used for the readout electronics shown in Figure 5–11. For RESET, S_x , and S_y , the switches are closed when the signal level is high, open when the signal level is low.

As shown in Figure 5–10, the output voltage of the differential amplifier can be measured using an oscilloscope; though more often, the signal is collected and converted to binary numbers via *analog-to-digital converters* (ADC). These numbers are subsequently transferred to a computer via *peripheral component interconnect* (PCI) *data acquisition* (DAQ) modules. Commercially available ADC and DAQ modules are adopted for array tests. The outputs of the CDS electronics are connected to an *input/output* (I/O) board (OME-DB-1825). The I/O board provides the necessary interface for the 110kS/s 12-bit ADC PCB (OME-PCI-1002). Both boards are built by Omega Engineering [123]. The functionality of the ADC and the data manipulation is controlled by a program written in Microsoft Visual Basic using software drivers provided by the vendor.

5.2.2 Driver

The configuration of the driver electronics has undergone several revisions mainly due to performance issues. Initially, the entire waveform generation process is done by Tektronix GaGe CompuGen signal generator [124]. The generator board interfaces with a host computer via PCI, capable of producing 32 channels of *transistor-transistor logic* (TTL) level waveforms. The factory software provides a *graphic user interface* (GUI) platform to manipulate the waveform design with time resolution of 10 μ s.

Figure 5–13 shows a screenshot of waveforms produced by an oscilloscope. The output of the charge amplifier for one readout channel is probed. Evidently, the lack of proper shielding and power supply fluctuations from the host computer yields a very noisy readout. Noisy driving signals also compromise the array operation. Since the addressing lines are connected directly to the driver bus, fluctuation of the driving signals is also coupled into each rows of the array, causing non-uniformity issues during readout. Furthermore, manipulation of the waveform with the provided GUI is a cumbersome and laborious task. Therefore, there is a strong incentive for an alternative implementation of the driver electronics.

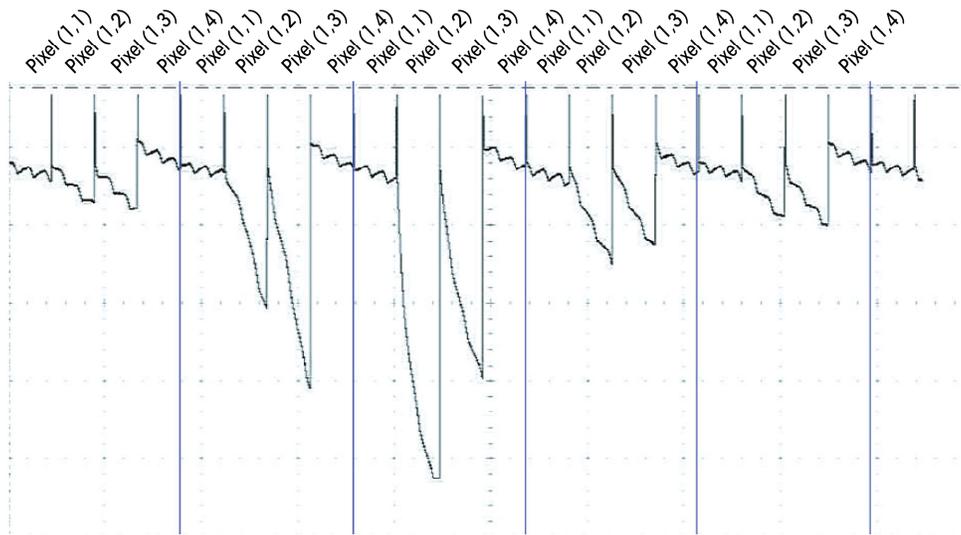


Figure 5–13: Screenshot from the oscilloscope showing the output waveform of the charge amplifier for a single channel. The waveforms show ripples due to external noise sources.

One alternative implementation used extensively in array testing is based on a *field-programmable gate array* (FPGA) circuit board. The array driver waveform is written in VHDL. The VHDL code can be simulated with ModelSim SE from Mentor Graphics for debugging and analysis [125]. A screenshot of the simulated driving waveform is shown in Figure 5–14.

After successful simulation, the VHDL code is compiled and synthesized using Quartus II software by Altera [126]. The synthesized circuit is realized on a NIOS development board, design and manufactured by Altera [127]. Figure 5–15 shows a photograph of the development board. The board hosts the APEX20K series FPGA that is capable of driving more than 80 CMOS logic I/O pins. Therefore, the use of multiplexers is not necessary for driving the small prototype arrays. The onboard clock provides 30ns of time resolution for the programmed waveforms, which is

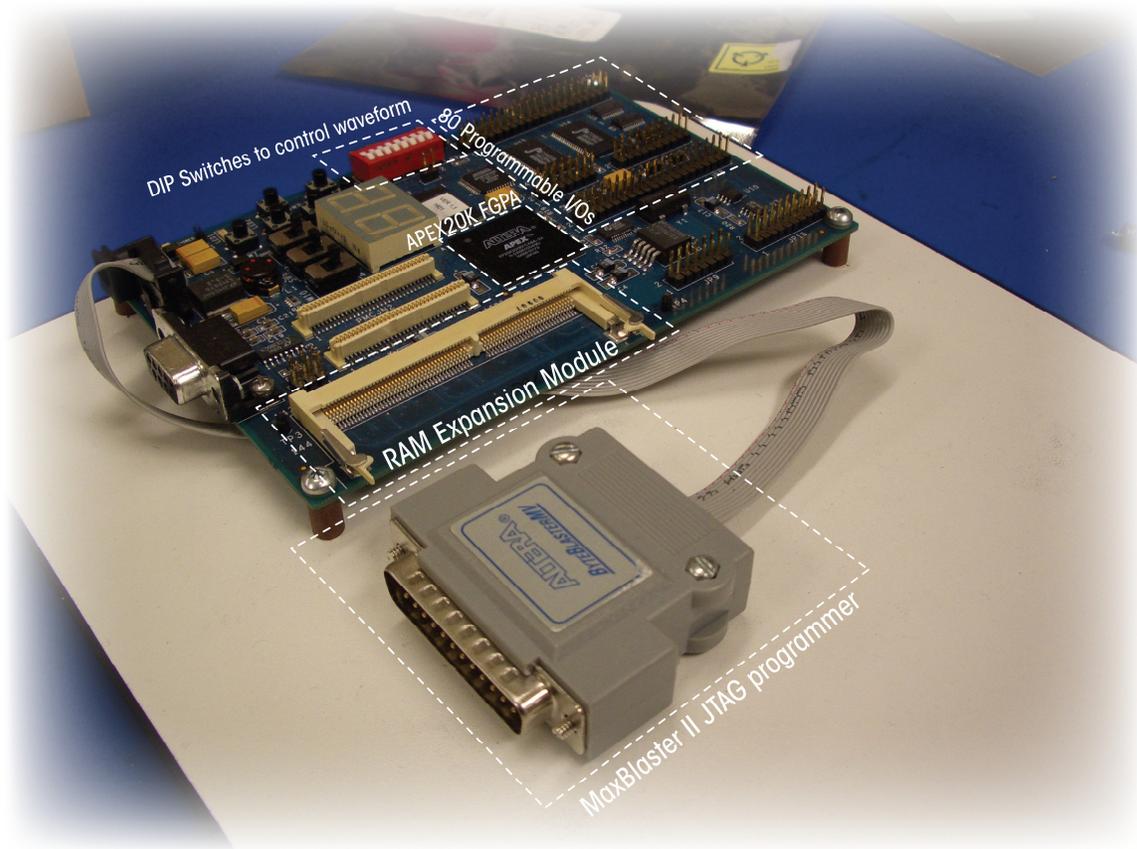


Figure 5–15: A photograph of the NiOS development kit hosting the APEX 20K series Altera FPGA.

Other alternatives for waveform generation have also been investigated. RCM3720 RabbitCore [128], which hosts the Rabbit 3000 microcontroller from Rabbit Semiconductors, is programmed with waveforms intended to drive multiple packaged array samples. Figure 5–16 shows a photograph of the RCM3720 RabbitCore PCB hosting the Rabbit 3000 microcontroller. Such implementation is preferred for full-size sensor arrays as the programmed microcontroller can be soldered directly on the same PCB as the readout electronics. This eliminates the need for signal bus cables and improves the driving signal integrity.

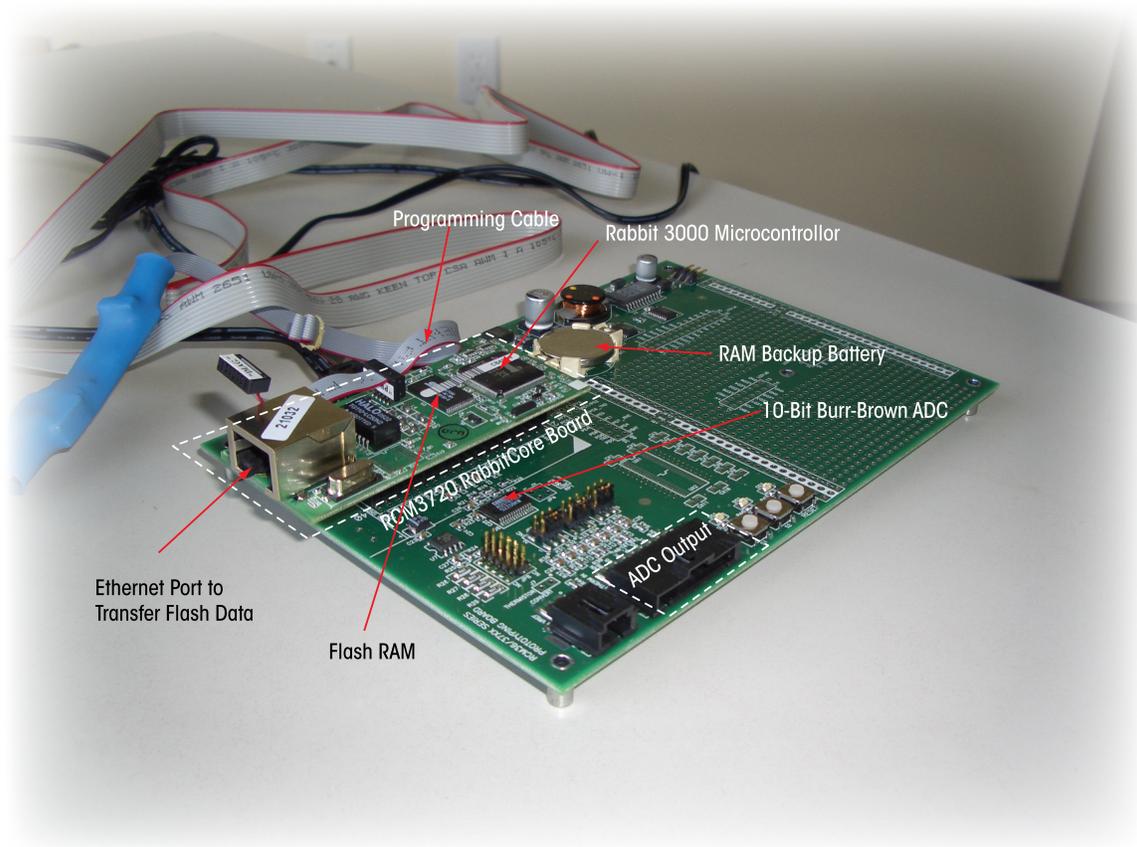


Figure 5–16: A photograph of the RCM3720 RabbitCore development board which hosts the Rabbit 3000 microcontroller.

5.2.3 Low-noise Printed Circuit Board

The original GaGe waveform driver interfaces with a multipurpose electronic board to test the prototype arrays. A photograph of the test board is shown in Figure 5–17. The PCB contains a 28-pin DIP socket to host the prototype arrays, power regulation circuits, signal conditioning circuits, and charge readout circuits. The charge amplifiers used for this board is the popular IVC102 from Burr-Brown [129]; the CDS circuitry is built with components from Analog Devices [130]. Due to numerous

necessary modifications done on the PCB, proper *electromagnetic interference* (EMI) shielding could not be put in place. As the driving signal from the GaGe generator is noisy, optical couplers are placed in the signal condition circuitry. However, the leakage current from the PCB is still large enough to drown the photodiode signals from weak illuminations.

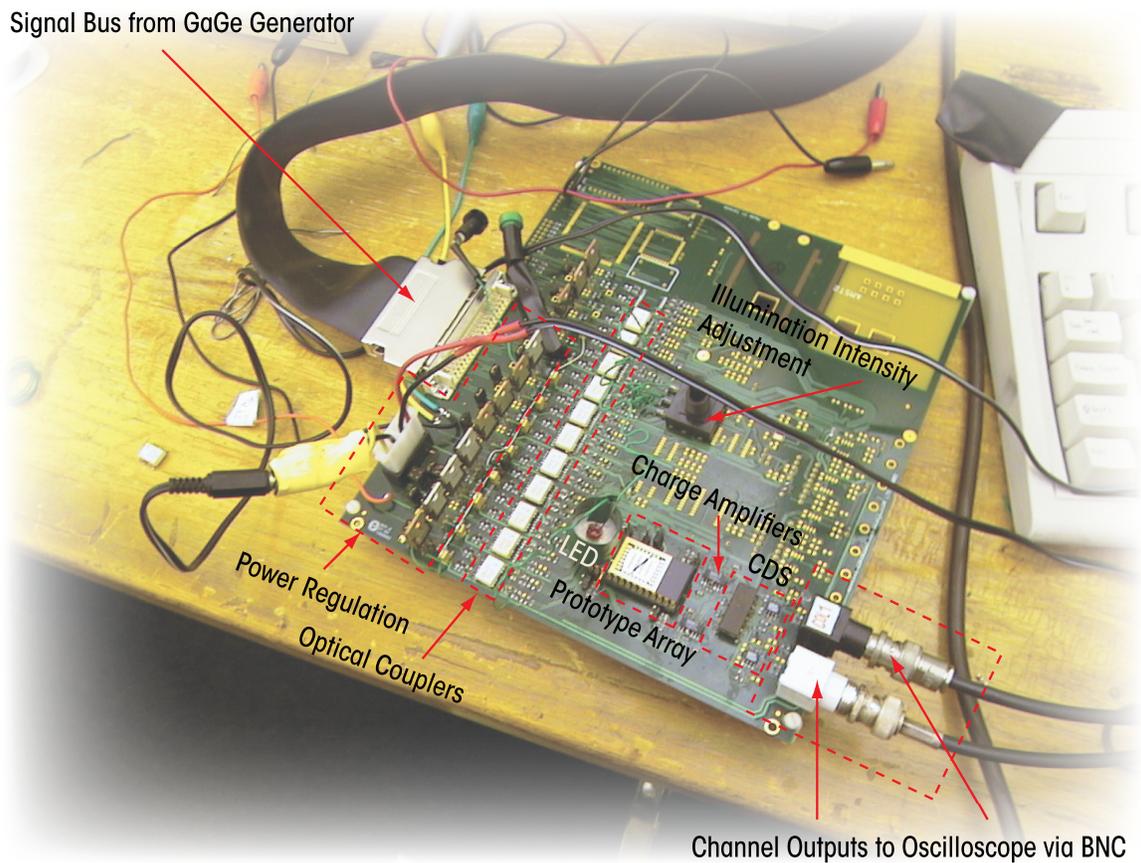


Figure 5-17: A photograph of the readout electronics PCB used to interface with the GaGe signal generator.

In order to properly test the fabricated arrays, a low-noise readout PCB is built to accompany the FPGA driving board. The PCB features four readout channels with each channel incorporating the readout schematic

shown in Figure 5–11. Both circuit schematic capturing and PCB layout are completed with the Altium Designer software [131]. The readout PCB is designed as a daughter board to provide synchronous sample and reset pulses for each channel. The readout board can be cascaded to expand to any number of readout channels; however, only one PCB is necessary to test the prototype array. Figure 5–18 shows a photograph of the partially populated 4-layer FR4 PCB. Preliminary tests of the PCB indicates that pre-amplifiers are not necessary for high photon flux conditions.

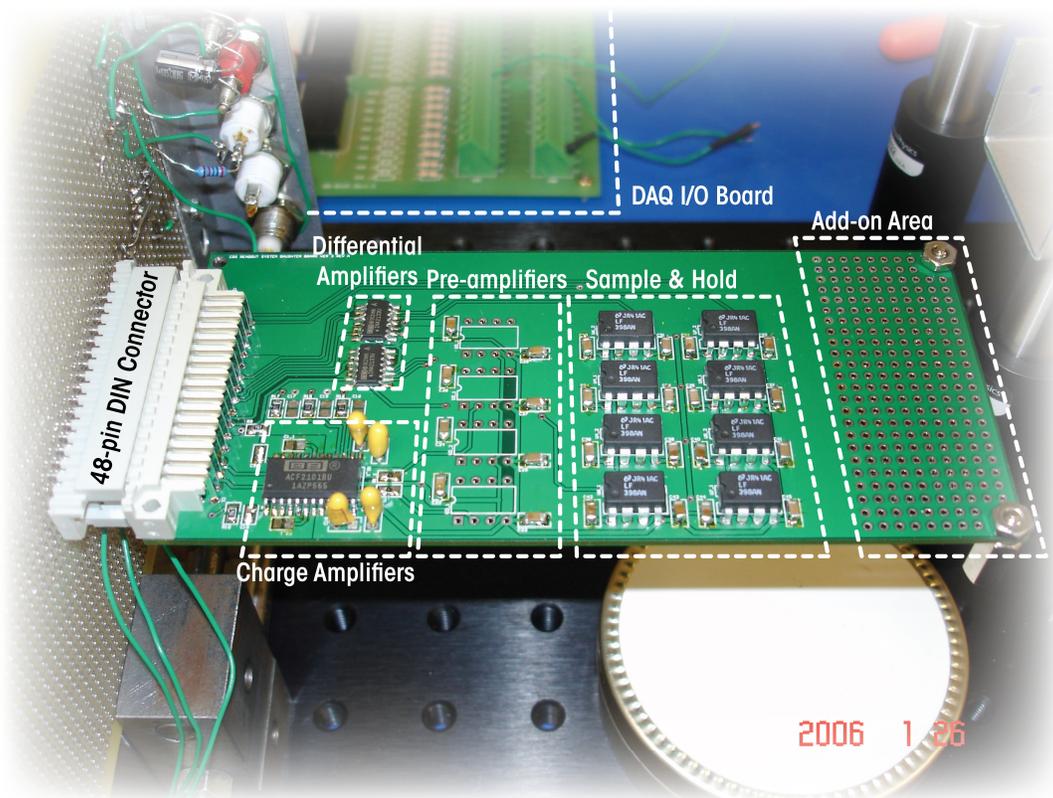


Figure 5–18: A photograph of the populated low-noise readout PCB. Each board consists of four individual readout channels with synchronous sample and reset.

The readout PCB interfaces with the driver electronics and test array through a 48-pin DIN connector [132]. The shielded data lines are routed

directly to the charge amplifier with short trace distances. The driving signals are routed to the signal conditioning circuitry then disturbed to the on-board components. The charge amplifier module employs the high-precision dual switched integrator ACF2101 from Burr-Brown [133]. The CDS circuitry is implemented with the LF398 sample-and-hold amplifier from National Semiconductors [134] and INA2133 high-precision differential amplifier from Burr-Brown [135]. A number of steps are taken to ensure the desired performance of the PCB. The 4-layer PCB allows the ground and power planes to be sandwiched between the top and bottom routing layers. This eliminates the need to route the power signals to the components and also ensures uniform potential across the board. The critical data lines are properly shielded and are completely decoupled from the driving signals to ensure signal integrity. The critical charge amplifiers also have a separate quiet ground from the rest of the components. Inputs to the ACF2101 are properly guarded to ensure low input noise and low input leakage current. The charge readout circuits are powered by six 6V rechargeable batteries to reduce power supply noise.

5.2.4 Array Characterization

The arrays are tested with photodiodes biased at -1.5V to ensure full depletion while minimizing the dark current level. Figure 5-19 shows the measured waveform at the output of the charge amplifier performed for an array with the single switching diode pixel architecture. The *HOLD* and *SELECT* switch for the ACF2101 are kept open. The laser-trimmed internal feedback capacitor ($C_{int}=100\text{pF}$) is used. The charge amplifier

output voltages of the corresponding data lines are simultaneously probed with a four channel Tektronix TDS2024B digital oscilloscope [136].

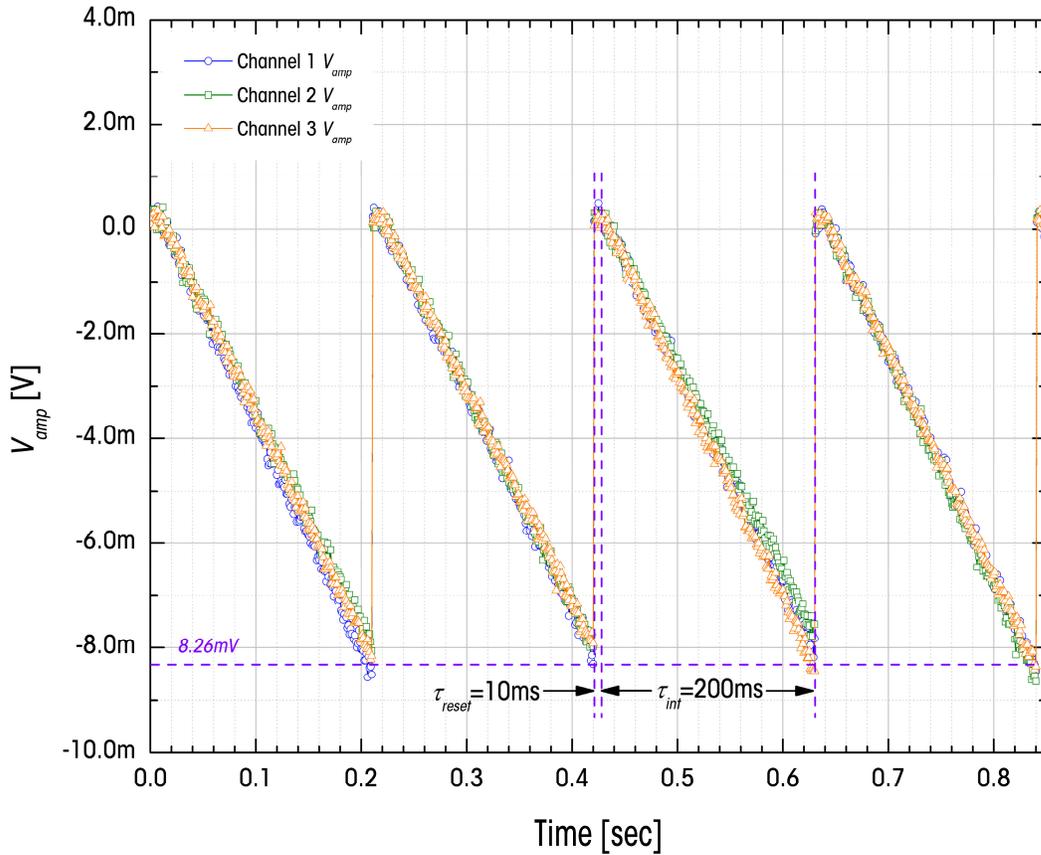


Figure 5–19: The output of the charge amplifier for three different channels. The array contains single switching diode pixel architecture.

The line current is integrated for 200ms while the RESET switch of the ACF2101 is kept open. The output voltage drops linearly according to Equation (5.2). The average output magnitude of 8.26mV indicates a reverse leakage current of 1.03pA for the photodiodes, which matches very well with I_D - V measurement results. Figure 5–20 shows the measurement results of the same array under green LED illumination. It is evident that a

finite amount of time is needed to transfer all of the photogenerated charge from each pixel due to increasing resistance of the switching diode.

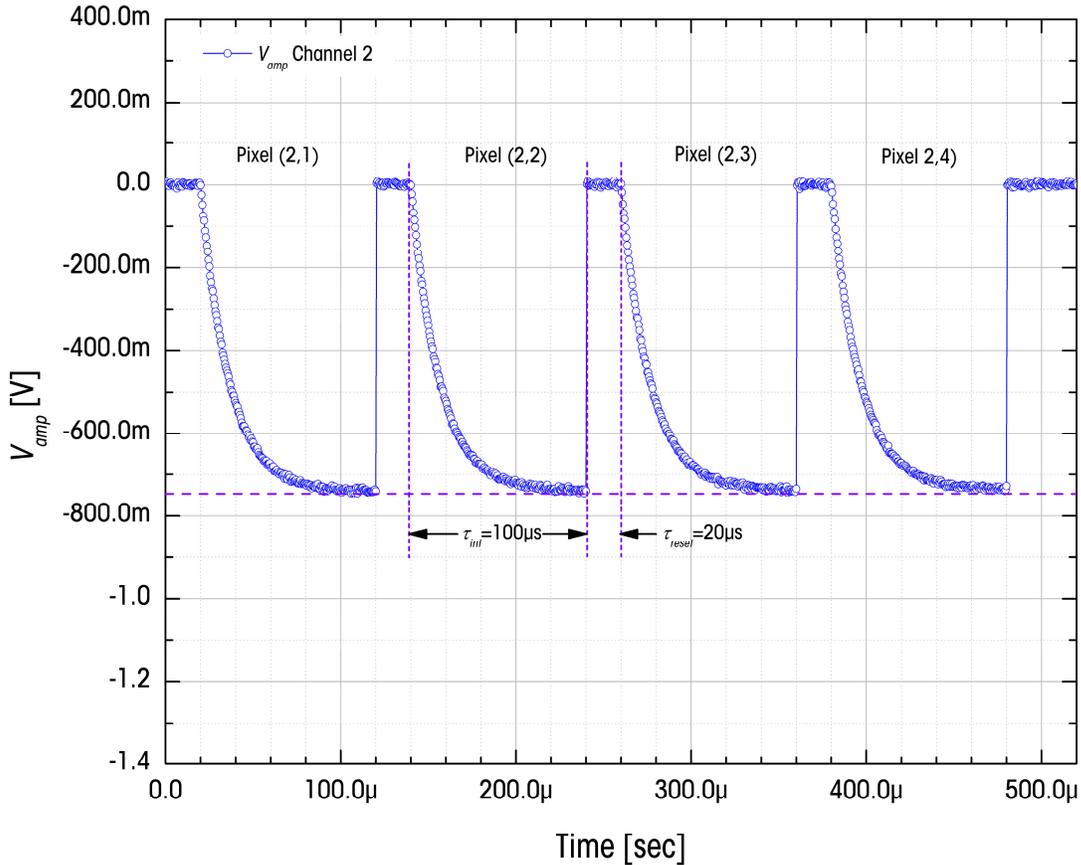


Figure 5–20: The output of the charge amplifier after the illumination of the array. The green LED illumination flux is $\sim 1.12 \times 10^{12}$ ph/mm²/sec.

The duration of the address line pulse (τ_{select}) dictates the amount of time given for the charge to transfer. Figure 5–21 investigates this issue by plotting the relative pixel signal as a function of τ_{select} . It can be seen that τ_{select} between 60–80 μ s is a good trade-off between charge readout time and charge transfer efficiency. Comparing to arrays with TFT switches [137], this measured charge transfer time is roughly twice as long.

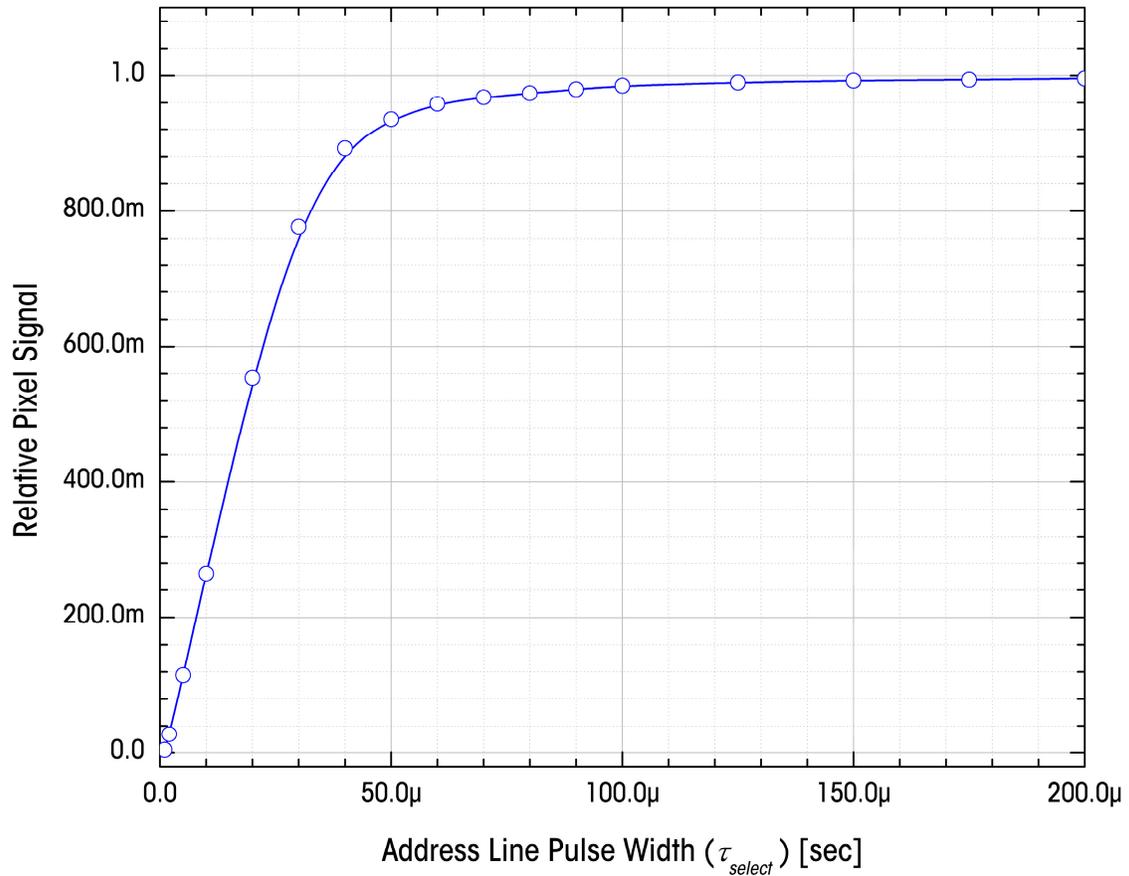


Figure 5–21: A plot of the output signal as a function of the select pulse width. Optimum transfer time is between 60–80 μ s.

Figure 5–22 shows the output signals of the differential amplifier for two different LED intensities. The measurements are conducted with a test array containing the double switching diode pixel architecture. The LED intensity is controlled by tuning the potentiometer connected in series. The impinging photon flux for high and low illumination level is calculated to be $\sim 68.45 \times 10^6 \text{ph/mm}^2/\text{sec}$ and $\sim 643.09 \times 10^3 \text{ph/mm}^2/\text{sec}$,

respectively. Different integration time are used for the high and low photon flux level; they are 500ms and 10sec, respectively.

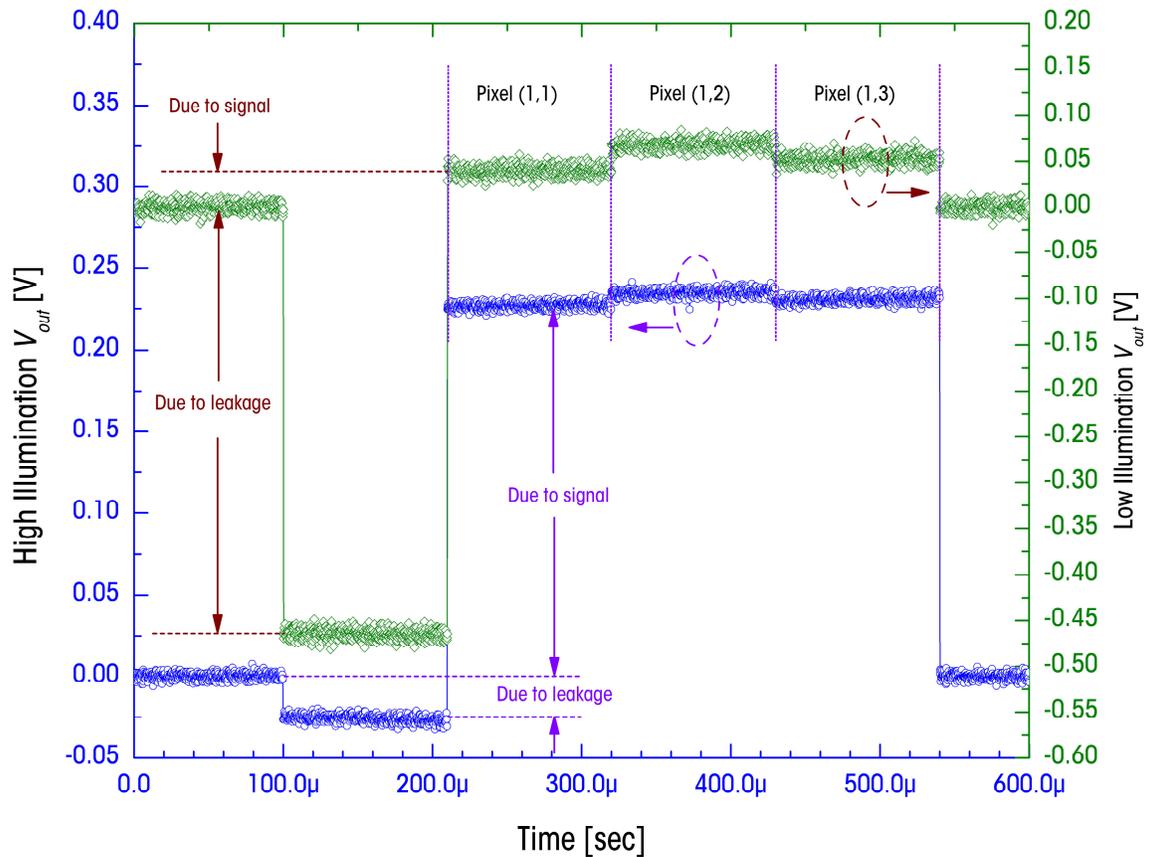


Figure 5–22: The output of the differential amplifier with two different illumination levels. Low light level illumination seems to show larger voltage variations between pixels.

The output voltage for each column directly infers the emission signal received by the pixels. The low flux illumination seems to yield greater voltage variations, which may cause problems if the microwells are used with low sample counts. The linearity of the detector is examined by measuring the system response to the released charge. The address line pulse width is set to 70μs. The amount of charge held by the photodiode is

varied by changing the frame time (τ_f) under controlled pixel illumination. Figure 5–23 shows the result of the experiment where the output voltage is plotted against the voltage drop across the photodiode (Q_{ph}/C_{ph}). The detector system shows excellent linearity over three orders of magnitude. This provides the accurate evaluation for the amount of fluorescence present at each site, which is important in determining the degree of expressions; for example, the degree of hybridization of RNAs or the degree of protein expressions.

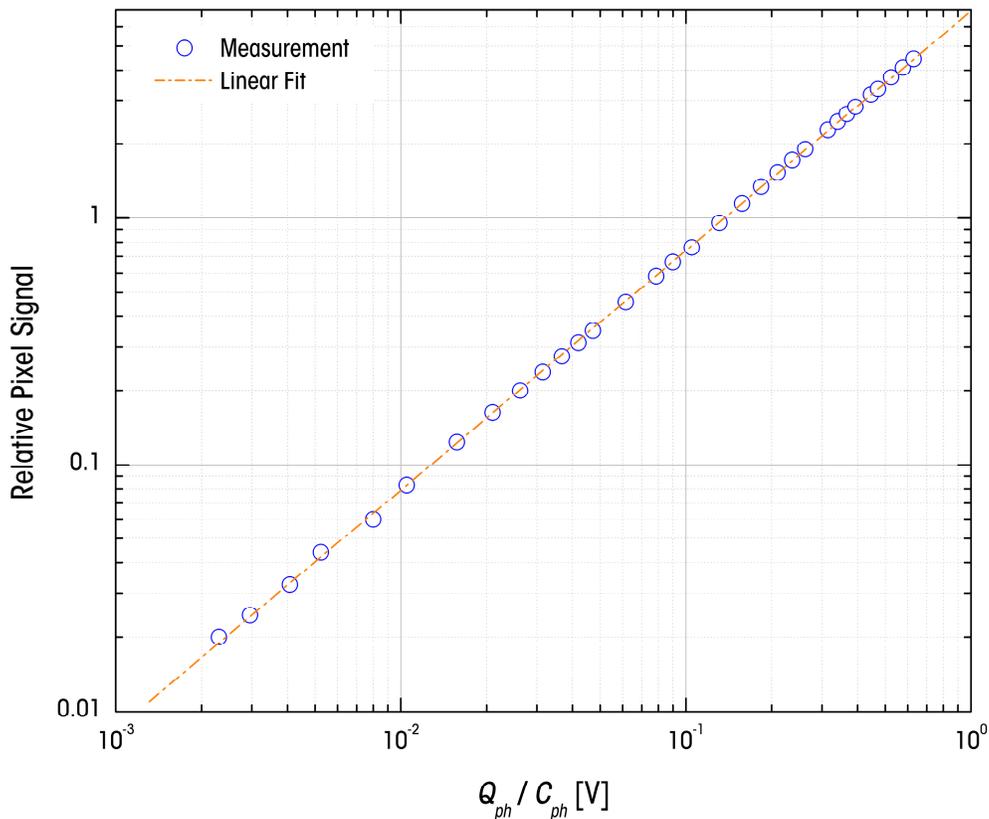


Figure 5–23: A plot of the output signal with injected charge normalized by pixel capacitance.

Chapter 6: Conclusions and Outlook

Novel contributions of this research work can be summarized in several areas. The development of the fabrication technology and optimization process enables the production of segmented a-Si:H photodiodes featuring pico-Ampere level dark current density. This sensor technology is essential for massively-parallel bio-assays where the incident photon count is low. For the first time, a physical-based a-Si:H $n-i-p$ photodiode model is developed in Verilog-A HDL. Such model is favored by design engineers as they are suitable for circuit level simulations and is completely compatible with existing SPICE models using mainstream circuit simulators. While modeling the temperature dependence of the photodiodes, a novel technique is also developed to extract the two major components of the photodiode reverse bias current. Such technique provides improved extraction accuracy for different photodiode sizes. Finally, small diode-addressed imaging arrays for bio-assay application are demonstrated for the first time to address the issues concerning the current bio-assay scanner systems.

Several important investigations remain to be conducted where issues may surface with the integration of the sensor system. Since the fabricated contact-type sensor array will inevitably come into direct contact with fluid agents used to immerse the bio-samples, it is uncertain how the behaviours of the sensors would change with prolonged exposure to moisture. Furthermore, when undertaking biological tests, it is best to

employ large protein molecules first which provides sufficient illumination to the array sensors pixels. Aside from possible integration issue, there are also factors that may hinder the commercialization of the sensor system. The current sensor deposition rate is very low and is not sufficient to produce such sensor array in full production scale. The fabrication speed needs to be increased without compromising the dark leakage current level. Without dedicated manufacturing facilities for large scale production, the cost of the sensor array would not offer any advantage compared to the current sensor systems.

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Appendix A — Die Configurations

There are eight different die configurations available for placement on the wafer. Each wafer is able to produce 52 small area dies and 32 large area dies, or roughly 10 sets of small dies and 3 sets of large dies. Two different die sizes are determined from the area to bonding pad ratio. The small die has a dimension of $3300\mu\text{m}\times 4700\mu\text{m}$ while the large die has a dimension of $5800\mu\text{m}\times 7800\mu\text{m}$; both include a $200\mu\text{m}$ boundary tolerance for dicing saw. A portion of the wafer area is allocated for the deflection experiments, providing important information for photodiode under compressive and tensile stresses.

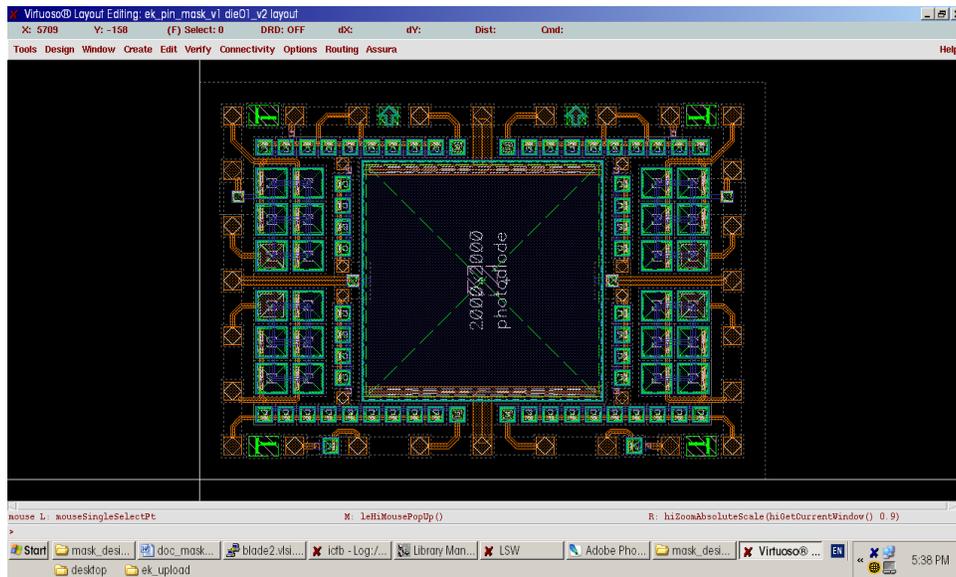


Figure A-1: A screenshot of die configuration 1. This die contains photodiodes of various sizes connected in parallel.

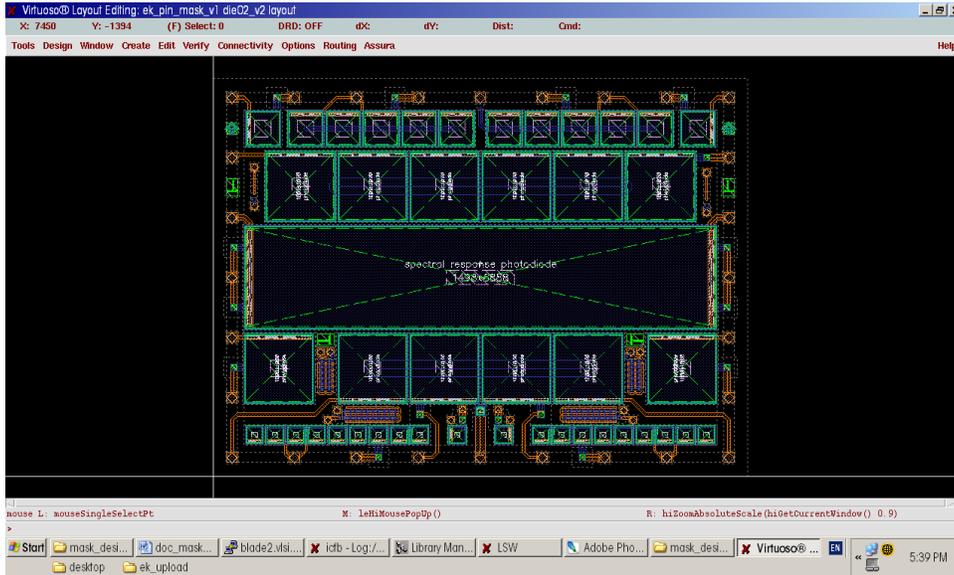


Figure A-2: A screenshot of die configuration 2. This die contains a large photodiode for spectral response.

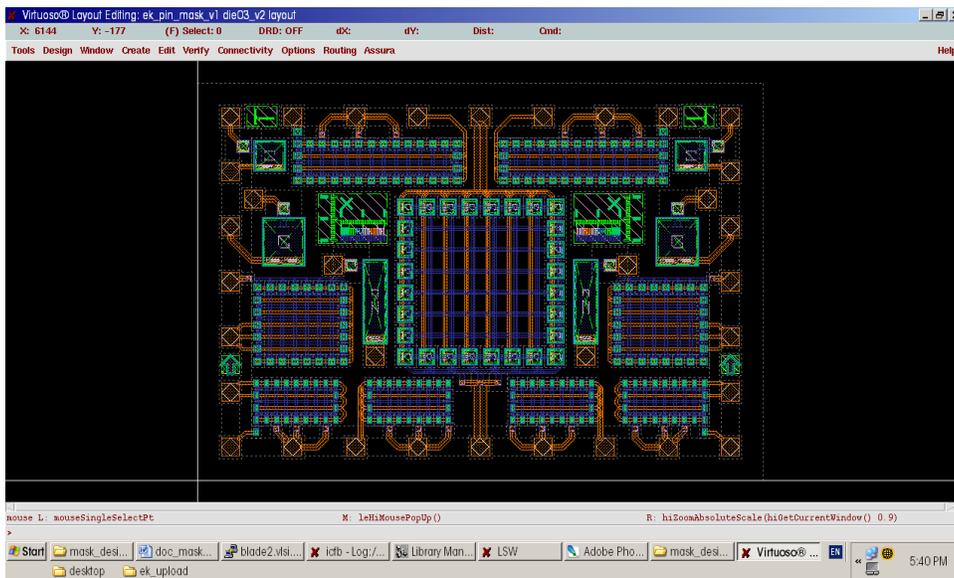


Figure A-3 A screenshot of die configuration 3. This die configuration contains mostly arrays of small photodiodes connected in parallel.

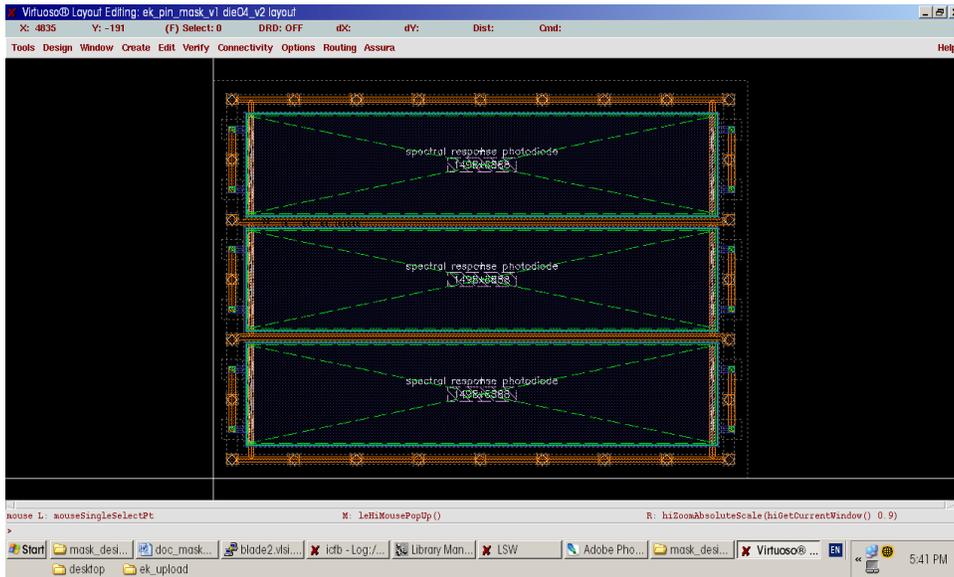


Figure A-4: A screenshot of die configuration 4. This die contains single photodiodes for spectral response tests.

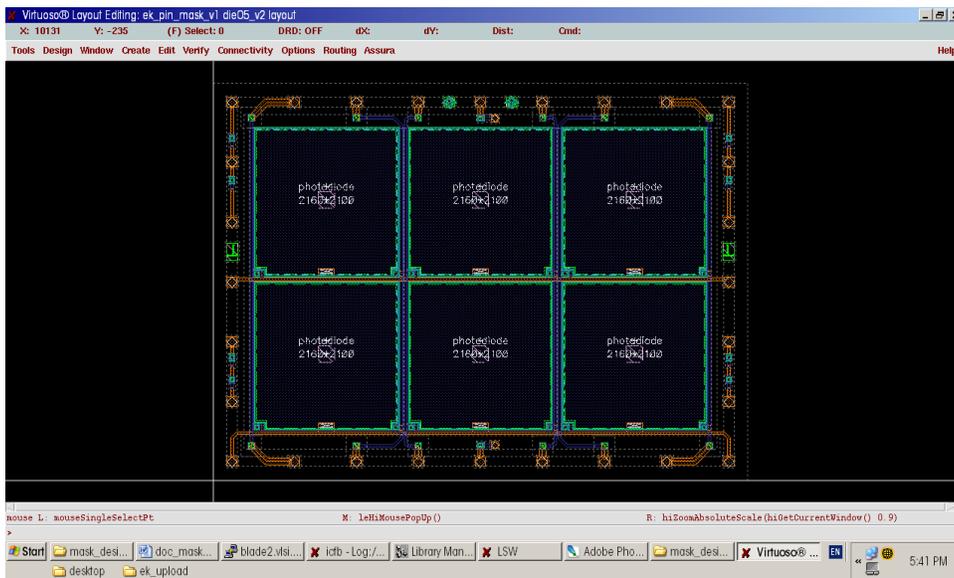


Figure A-5: A screenshot of die configuration 5. This die contains a 2x3 photodiode array with double switching diodes.

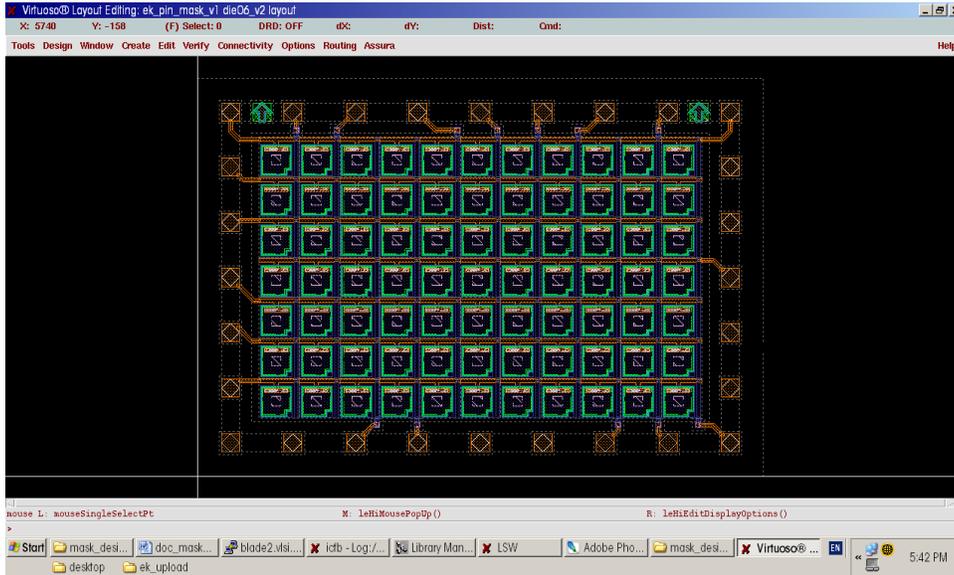


Figure A-6: A screenshot of die configuration 6. This die contains a 7×11 photodiode array with single switching diodes.

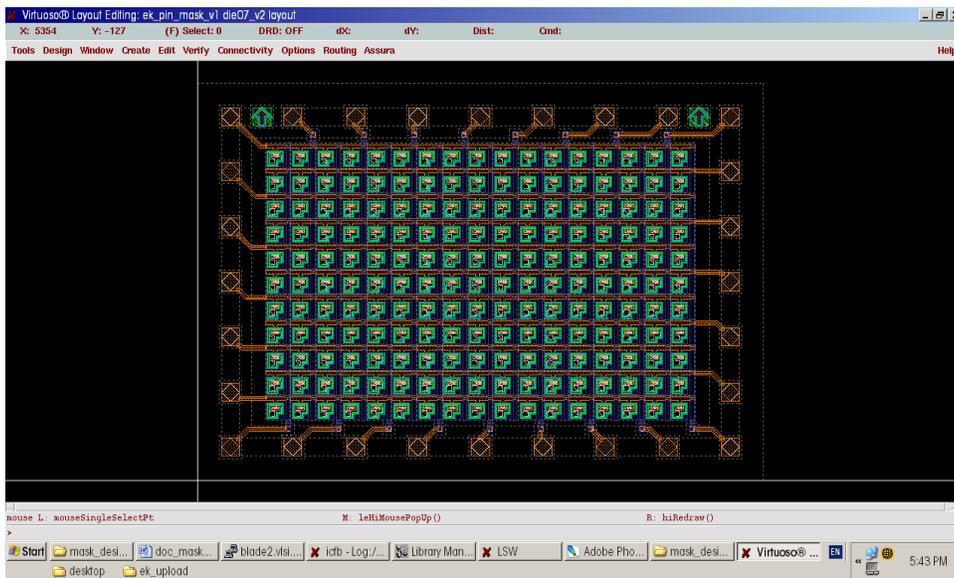


Figure A-7: A screenshot of die configuration 7. This die contains an 11×17 photodiode array with single switching diodes.

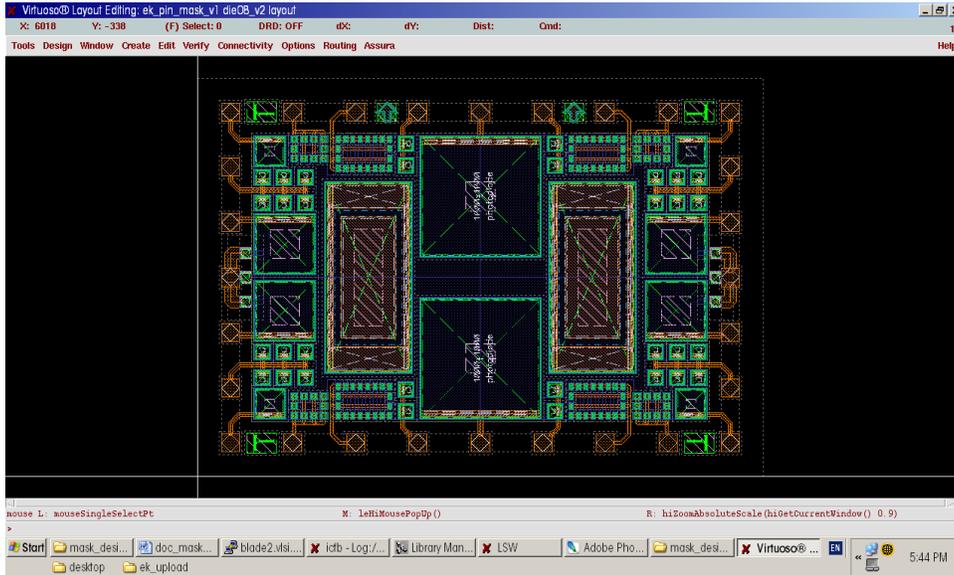


Figure A-8: A screenshot of die configuration 8. This die contains single photodiodes of various sizes. It also has a photodiode with guard rings for top metallization.

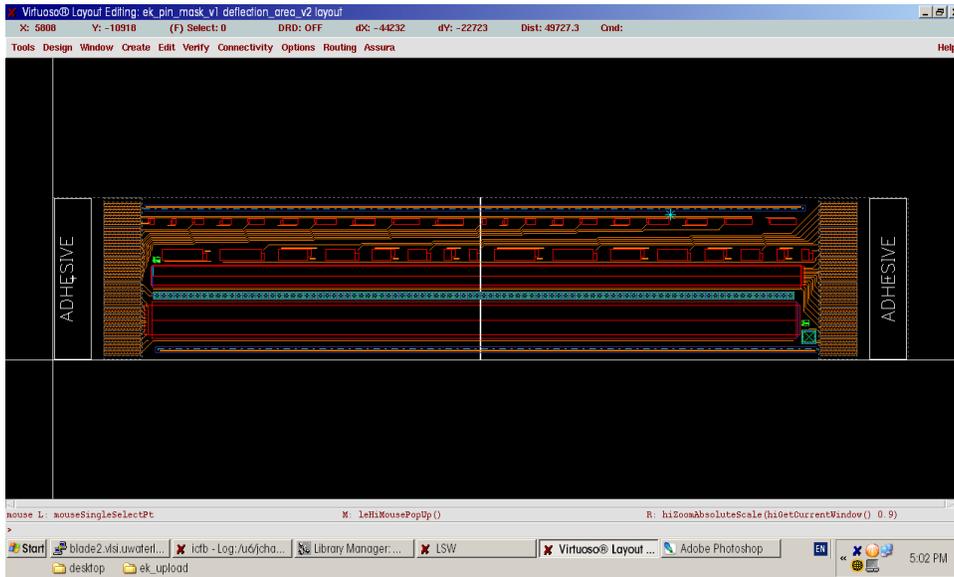


Figure A-9: A screenshot of the deflection experiment area. Arrays and single photodiodes of various sizes are included in this area.

Appendix B— Photolithography Design Rules

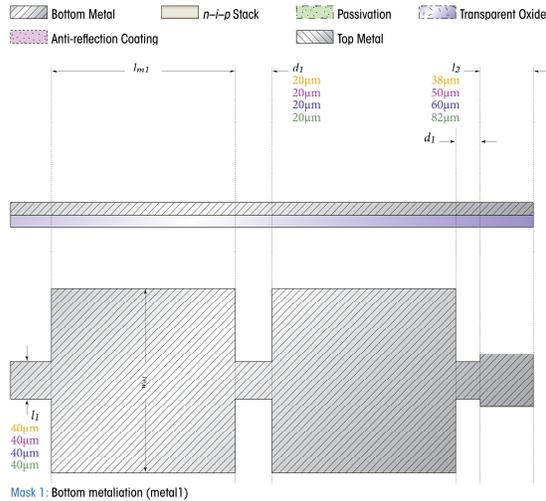


Figure B-1: Critical design rule dimensions corresponding to mask 1.

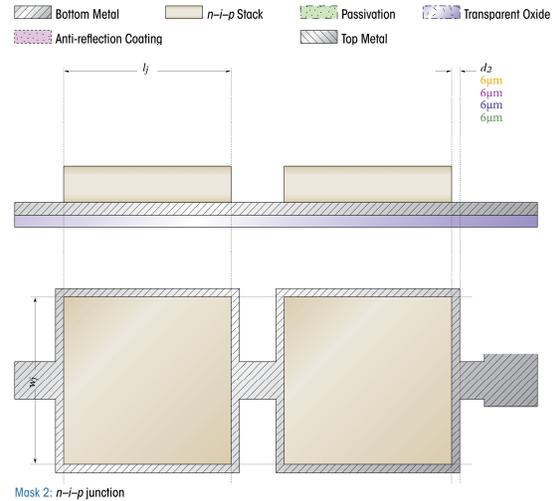


Figure B-2: Critical design rule dimensions corresponding to mask 2.

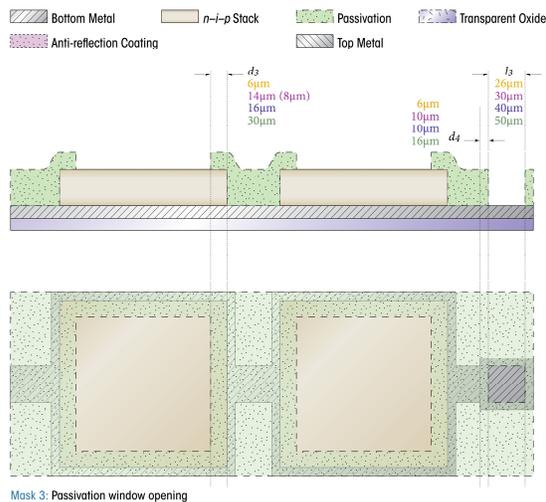


Figure B-3: Critical design rule dimensions corresponding to mask 3.

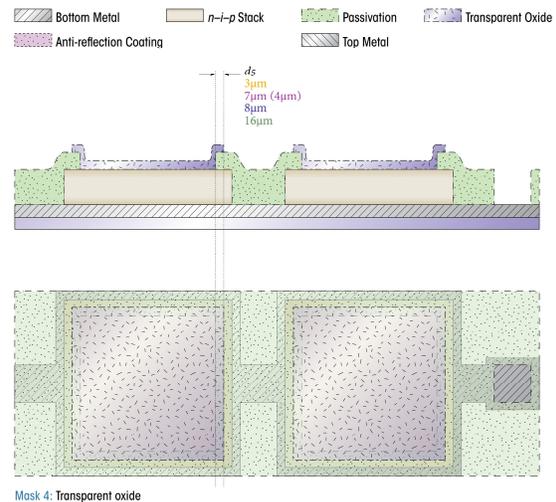


Figure B-4: Critical design rule dimensions corresponding to mask 4.

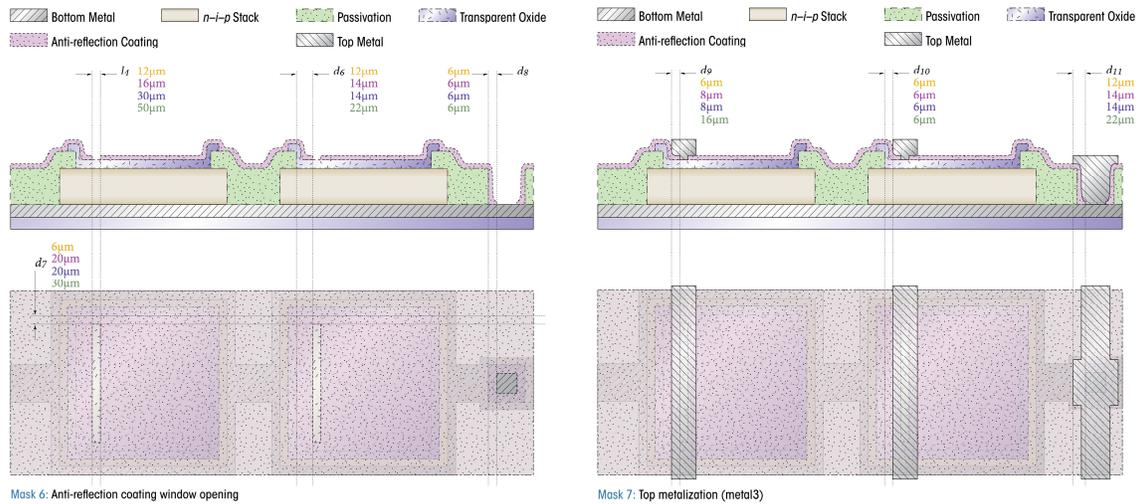


Figure B-5: Critical design rule dimensions Figure B-6: Critical design rule dimensions corresponding to mask 6. Mask 5 (metal2) is not corresponding to mask 7. included in this illustration.

The labels are color coded: orange refers to photodiodes with junction size between $30\mu\text{m}\times 50\mu\text{m}$ to $50\times 50\mu\text{m}^2$, magenta refers to junction sizes between $126\times 126\mu\text{m}^2$ to $250\times 250\mu\text{m}^2$, blue refers to junction sizes between $500\times 500\mu\text{m}^2$ to $1\times 1\text{mm}^2$, and green refers to junction sizes greater than $2\times 2\text{mm}^2$.