Design and Development of a Power Modulator for Insulation Testing

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Variable speed drives allow for more precise speed control of induction motors, are of high power factor, and offer fast response characteristics, compared to older technologies, such as motor-generator sets and eddy current clutches. However, due to the high switching frequencies as well as the high dV/dt in the output increased dielectric stresses are produced in the insulation system of the motor they supply. Due to the use of these solid state drives there have been concerns of premature failure in large, medium and high voltage, motors. To fully understand and deal with these concerns requires studying the degradation mechanisms, in the insulation system, caused by these drives; which, on an actual motor is both extremely costly as well as impractical. Therefore, coil samples which accurately represent the construction of the actual insulation system, must be aged and studied instead. In addition, to ideally replicate the aging process, the same waveform that the motor is subjected to must be applied to these samples. As a result of this requirement, a low power, two-level, high voltage PWM inverter has been built to replicate the most important characteristics of the output waveform of a variable speed drive. This power modulator allows for testing the insulation systems considering a real PWM waveform in which both the fast pulses and the fundamental low frequency are included. The results of these tests show that the effects of PWM waveforms cannot be entirely replicated by a unipolar pulse generator.

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Table of Contents

List of Tables

List of Figures

Chapter 1
Introduction

The introduction of the first medium-voltage drive in 1983 [1] ushered in a new era in the operation and control of medium voltage (MV) induction motors. These new drives quickly began to supersede devices such as gearboxes and eddy-current clutches, which had been previously used for these applications. In addition, rapid development of technology and manufacturing processes in the electronics industry has allowed for the development of semiconductor products, such as switches, with ever increasing current and voltage ratings. This in turn has allowed for the development of higher voltage solid state drives. Currently, solid state based medium voltage drives with operating voltages of 2.3 to 13.8 kV are available on the market. As such, it is possible to increase the operating voltage; hence the power ratings of these drives continue to increase, while, keeping the current at a reasonable level, so as to keep the physical size of the components reasonable and allow for good thermal performance [2].

The new drives have applications in a diverse array of industries such as oil and gas, mining, metals, and marine sectors [3]. Initially, the first MV drives produced were used in lighter loads such as fans and compressors [4]. As the technology further developed, higher power and voltage ratings were implemented in these solid state drives. For example, one of the emerging applications being investigated for MV drives is for use in marine applications such as propulsion systems [5]. The market for medium voltage drives has shown 20% growth in the last 2 years and continues to rapidly grow [6].

Many MV drives are designed and installed to run continuously. For example, in many oil and gas applications, where the drives are used for pumps and compressors, these installations must run continuously 24 hours a day, 365 days a year. Refineries operate continuously and any stoppages due to maintenance or equipment failure are costly. To prevent these costly repairs and potential work

stoppages motor manufacturers must continue to develop and improve the magnetic and insulation systems used in inverter duty motors.

The newer solid state drives provide obvious advantages over the older methods of speed control. For example, they are much less prone to equipment breakdown [1], and offer significant energy savings over their mechanical alternatives for variable torque applications [1,7]. For constant torque applications, while it has been shown that the energy savings are not significant enough to justify the capital cost of a solid state MV drive, there are other reasons which support the application of solid state MV drives. As mentioned previously, these reasons include increased reliability, as mentioned previously, as well as poor support available for legacy technologies [1].

1.1 Types of Medium Voltage Drives

Presently, there are two main types of drives available in the market, current source converters (CSCs) and voltage source converters (VSCs). As the name implies, CSCs require a constant DC link current to operate. As a result, a reactor is required in between the line rectifier and the inverter, which for high power/torque applications can become quite large, and potentially increase the size of the drive greatly. CSCs offer the advantage of being more rugged and reliable compared to VSCs [8]. For VSCs, a capacitor is required in the DC link to provide a constant DC voltage regardless of the load connected to the converter. VSCs advantages over CSCs include better efficiency, superior transient response, lighter weight, lower price, and the flexibility of operating with either open loop (which is not possible with CSI) or closed loop control [8]. As a result of these advantages, the majority of manufacturers utilize the voltage source converter topology in their designs. CSCs have been slowly squeezed out of the market by VSCs [9], leaving CSCs to be used solely in very high power applications [8].

In the low voltage drive designs, the 2-level voltage source inverter topology has become the dominant configuration [10]. This is mainly due to the fact that these products have been in use for quite a while, which allowed the technology to mature. Differentiation between manufacturers is mainly based on smaller aspects like packaging, efficiency, and controller features as well as the improvement of the actual power semiconductors used in these drives [10]. Currently, there is no dominant drive topology in the medium voltage (MV) range [11]. However, a common branch between all manufacturers is the use of some form of multi-level inverter in the designs of all the voltage source converters (VSC) in this class. There are three main types of multi-level inverters: diode clamped, capacitor clamped, and cascade [12]. The diode clamped inverter utilizes additional diodes to clamp the voltage exposed to the switches. One of the main advantages of the diode, and the capacitor clamped inverters, is that each switch is only exposed to a fraction of the DC-link voltage. The size of this fraction is dependent on the number of levels. The use of this topology allows for higher operating voltage compared to a 2-level inverter, when using switches with the same voltage rating. The cascade type inverter has a number of possible implementations. One method utilizes the series connection single phase inverters, while another method utilizes the series connection of three phase inverters.

The main advantage of multilevel inverters, from an insulation standpoint, is that they produce much more motor friendly waveforms as compared to a standard 2-level inverter. The multiple levels reduce the overall dV/dt in the output which occurs at the motor terminals, this in turn reduces the stress on the insulation. Another advantage of multilevel converters is that because of their higher voltage outputs, due to the stacking of switching devices, the use of output transformers for large induction motor applications can be negated [13]. While multilevel inverters have a number of obvious advantages they also have some weaknesses; the increased number of components required can reduce the overall reliability of the system [14] as well the control algorithms required for

multilevel converters are much more complex, for example it is difficult to maintain equal voltage balance between all the DC link levels [13].

1.2 Insulation Problems

The application of solid state PWM drives for use with induction motors has created concerns with regards to the negative impact that these drives have on the insulation system of the motor [15,16]. This is mainly due to the fact that the insulation systems are not designed to cope with the impulse like voltages produced by the drive, as they have been mainly designed to operate solely at power frequency (50/60 Hz). Most of the problems that occur due to the use of these drives result from the steep front pulses (high dV/dt) and added harmonic content of the output waveforms. These problems include large overshoots at the motors terminals [17], increased motor heating [18], and bearing currents [19].

The large overshoots that occur at the terminals result from using longer feeders to supply the motor. These overshoots, shown in Figure 1.1, occur because there is a mismatch between the cable impedance and the motor impedance [17]. This mismatch causes the travelling wave produced by the inverter to be reflected back upon itself. The superposition of the reflected wave and the incoming wave can cause a spike of up to two times the nominal voltage to appear at the motor terminals [17].

The increased motor heating is a result of the additional harmonic content found in the PWM waveform compared with that of a sinusoidal 60Hz waveform. These harmonics do not contribute to the output power of the motor and are simply converted to heat, which may speed up the thermal degradation of the insulation.

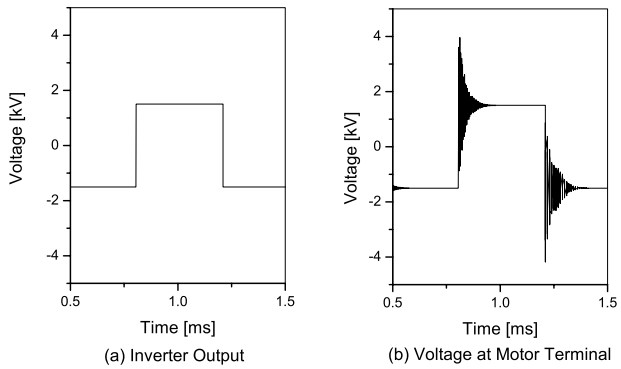


Figure 1.1: Inverter output voltage (a) and motor terminal voltage (b) of a motor connected by a long feeder

Common mode voltages induce currents to flow through the parasitic capacitances coupling the shaft and the stator through the bearings. These currents conducted through the bearings gradually degrade the surface of the bearings and eventually enough degradation occurs to cause a mechanical failure. One of the recent solutions proposed to solve this problem was the use of less conductive lubricants as well as insulating ball bearings [20].

To combat the problems associated with these drives, there are currently two potential solutions, to either use an inverter duty motor or to use an filter between the motor and the converter [21]. Often this inverter duty motor is simply a standard motor with improved cooling and added groundwall and turn-to-turn insulation [4,22]. This solution has not completely eliminated the aging and degradation problems found in the insulation system. It has simply lengthened the aging process before any serious problems or failures develop. Further increasing the insulation thickness is not an acceptable solution as it increases the size and cost of the motor. Instead of focusing on this type of solution motor manufacturers need to focus on developing and qualifying insulation systems that are much more resilient to the operating conditions produced by VFD's.

Filters may be an appropriate solution for a variety of situations however they are not always applicable. For example, the weight and space saving gained in ships by replacing the conventional gear box speed control with an adjustable speed drive is negated by the weight and size of a filter [5]. Filters can also be unappealing due to the fact that the resonant frequency of the filter can potentially limit the fundamental frequency of the output, limiting the operating modes of the drive [23].

One trend that maybe especially problematic for motor manufacturers is the increasing voltage ratings of the semiconductor devices. These higher voltage ratings will allow manufacturers to achieve the same operating voltage levels, while simultaneously reducing the number of levels in their designs. This would reduce the complexity, as well as the number of the components required in the design and as a result, will reduce the cost while potentially increasing the reliability. This trend, towards simpler designs such as 3-level inverters, would be beneficial for drive manufacturers, but it may create an added insulation problem for motor manufacturers [24].

Currently, there is very little available literature in regards to the effects of PWM inverters on medium voltage insulation systems [25,26,27,28]. Correspondingly, there is a lack of research in developing improved insulation materials for medium voltage induction motors. There has only been a small focus on developing improved magnet wire coatings [29,30]. The lack of research in this area may be attributed to a number of reasons; namely, inverter fed medium voltage induction motors have only recently become widespread, and, due to the large capital cost and limited market for these motors, manufacturers may be wary of publishing reliability studies and test results that generate unfavorable publicity. As a result, researchers attempting to study the reliability of medium voltage inverter-fed motors and their insulation systems are left to look at the low voltage class of inverter-fed induction motors and to make inferences on medium voltage class inverter-fed motors.

One example of this is in determining the rise time (and the dV/dt) of the pulses produced by these converters. For low voltage drives it is relatively easy to determine the rise times as the dynamic characteristics of low voltage IGBT's are well known. As well, low voltage low power drives are quite economical and so easy to obtain, allowing researchers to easily measure and empirically determine the rise time of the pulses that appear at the motor terminals. For medium voltage drives this is not the case. These drives are very expensive to acquire and install. As well there are few simulation models available of IGBT modules [31]. As a result of these conditions, researchers are left with either basing the estimates on the data sheet values of the power semiconductor devices being used and the few output waveforms that manufacturers make available. A survey of current IGBT modules, which are the switches used in the majority of MV drive designs, available with ratings from 1.7 to 6.5kV show turn-on and turn-off times between 0.4 to 2.4μs [32,33,34]. The turn-on time relates to the time required for the collector emitter voltage to drop from its steady state off value to the devices' on state value. The turn-off relates to the converse of the turn-on.

While the insulation problems discussed previously can be found in both low voltage and medium voltage motors, the solutions developed to combat these problems in low voltage insulations systems cannot be directly applied to their medium voltage counter parts because they have different constructions. As well, medium voltage drives have only become more widespread recently as compared with low voltage drives. The differences in the insulation system between low and medium voltage will be briefly covered in Section 1.3.

1.3 Medium Voltage Induction Motor Insulation Systems

There are two types of stator windings used in the construction of induction motors namely; random wound, and form wound coils. In addition, random wound stator coils are usually found in smaller

induction motors with operating voltages of less than 1000V [35]. Random wound coils are constructed using rounded copper conductors that are wound either by hand or by machine. The name random wound comes from the fact that the arrangement between turns is not exactly defined and can vary between coils of the same design.

Form wound stator coils are mainly used in larger machines with operating voltages above 1000V. The construction and design of these coils is much more complex and involved, making them much more expensive than their random wound counterparts. Form wound coils are constructed using rectangular magnet wire, which is wound in a precise fashion to form the coil. These coils are then treated using global vacuum-pressure impregnation (VPI). In the VPI process, the untreated coil is first placed in a vacuum chamber and dried for up to 8 hours [35]. Then, after vacuum treatment, the coil is immersed in a resin inside a pressurized tank. The resin under pressure is forced into the voids within the coil. Finally, the coil is removed from the tank and heated at a temperature of 120-150°C to cure the resin [35].

The insulation system of a form wound coil consists of three main parts namely; strand insulation, turn insulation, and the groundwall insulation [35,36]. The strand insulation consists of a thin layer of polyamide coating that is on the surface of the magnet wire. The turn insulation is designed to electrically isolate adjacent turns from each other. At lower operating voltages, the strand insulation can also be used as the turn-to turn-insulation. For higher voltages, mica tape is wrapped around the conductors to provide the turn-to-turn insulation. The purpose of the groundwall insulation is to provide electrical insulation between the stator coils and the grounded stator core, of the induction motor. The groundwall insulation is the most critical of the three types of insulation within the motor. Should the groundwall insulation fail a ground fault will occur, which would result in catastrophic consequences.

At operating voltages above 4.16kV, a special modification is made to the groundwall insulation because as the operating voltage increases, the electric stress, at different interfaces between the grounded stator core and the energized coil, increases. Above 4.16kV, the electric stress on coil surfaces begins to reach the inception voltage for partial discharge (PD) activity. As a result, a stress grading/control coating is applied to certain sections of the coil, specifically at the slot exit as well as the end windings, to prevent this from occurring. The purpose of the stress grading is to grade the electric field along the surface of the coil and so decrease the field strength thus preventing PD. This grading allows for a smooth transition in the voltage from the grounded stator core to the energized coil voltage, thus avoiding any both sharp changes in the voltage and high concentrations of electric field [36].

1.4 Aim of the Present Work and Thesis Organization

As stated previously, there is little published work on medium voltage inverter-fed motor insulation. Currently, the majority of the research in this area utilizes unipolar square waves or exponentially decaying pulses as test waveforms in insulation tests. This waveform doesn't expose the insulation under test to the full effects that the converter output produces; namely, the fundamental component, the high dV/dt, and the large harmonic content. As a result a comparison between the ageing effects under conventional test waveforms and an actual PWM test waveform would prove to be very beneficial. To address this need, the objective of this thesis is to construct a pulse modulator capable of producing a high voltage bipolar pulse width modulated (PWM) output suitable for use in insulation testing. The requirements of this device are as follows:

- High voltage output with low power consumption;
- The output should attempt to replicate the output of a MV PWM-VSC as close as possible;

- Based on the previous criteria and the study of current IGBT modules the rise time of the output pulses should be between 0.5μs and 1μs; and
- The device should be able to operate with a capacitive load connected.

With respect to the previous objectives this thesis is organized as follows:

- Chapter 2 covers the design process and construction of the pulse modulator. This will encompass component selection and important design considerations, as well as the software used in the controller.
- Chapter 3 presents the results of building the modulator. This includes the output waveforms, as well as some of the limitations, and weaknesses of the device.
- Chapter 4 presents and discusses the preliminary results from the insulation tests that were conducted using the constructed pulse modulator. Tests were performed on turn insulation, groundwall insulation, as well as stress grading.

Chapter 2
Design, Development and Construction of the Modulator

2.1 Introduction

This chapter covers the design, development, and construction of the pulse modulator. Due to the high voltage operation and the need to test the suitability of individual components, this device was constructed in two stages. First, a smaller unipolar pulser was designed, and constructed. This allowed the basic design to be tested on a smaller scale, to determine whether the selected components would be able to handle the voltages required by the modulator, and to determine the best way for connecting multiple switches in series. Once all these problems and concerns had been addressed the final pulse modulator could be constructed. After which it could be used to test insulation systems of inverter fed medium voltage induction motors.

The topology of the pulse modulator is based on a simple single phase PWM inverter [37]. Because this pulse modulator will primarily be used to test insulation samples, the device should attempt to accurately replicate the waveforms produced by a MV PWM-VSC. One important constraint on this design is the fact that the majority of power semiconductor products designed for high voltage operation are also designed with correspondingly high current ratings. For insulation testing only high voltage but low current (1-2A average) is required. This problem is highlighted in Figure 2.1.

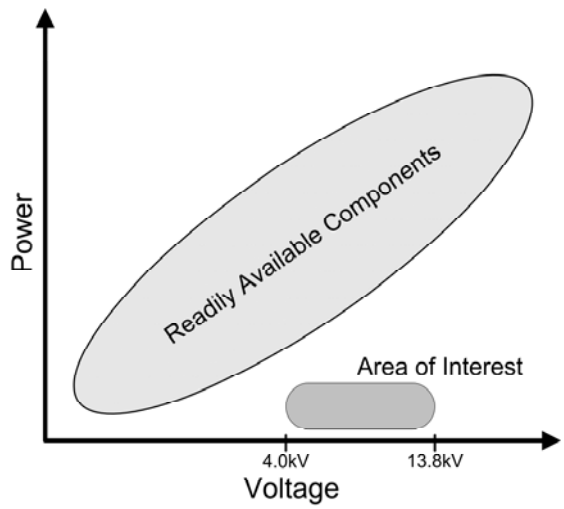


Figure 2.1: Components available on market and area of interest of this project

2.2 Unipolar Pulser

The basic design that was used in the unipolar pulser as well as the bipolar pulse modulator is shown in Figure 2.2.

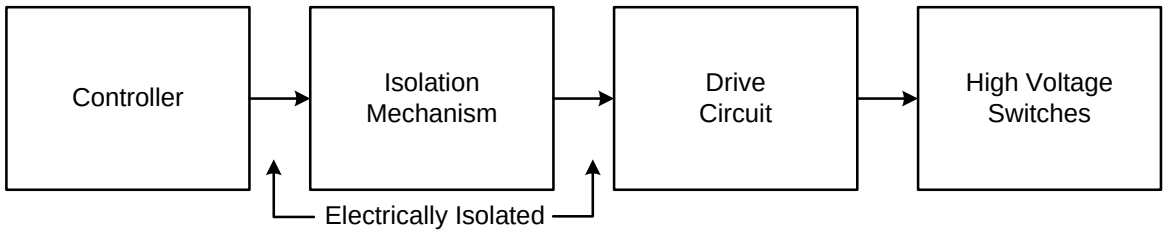


Figure 2.2: Block diagram of the basic configuration used in both devices

The four main parts of the pulser are: the controller, the isolation mechanism, the drive circuit, and the high voltage switches. The controller sends the gating signal through the isolation mechanism to the driver circuit, which then provides the current to properly drive the switches. This pulser was built in stages, starting with the controller and a single switch. After this configuration was verified

to be operating properly, another switch was added in series. This process was repeated until the pulser was operating with four switches in series to obtain the required voltage amplitude.

2.2.1 Controller

The control circuit controls all aspects of the pulser's operation. Because the unipolar pulser and bipolar modulator do not need any advanced control features or computations, a simple controller with a basic instruction set will suffice. As well, because of the high voltage nature of the circuit and the inherent incompatibility of low voltage digital electronics with high voltage, it is essential to use a lower cost component in the initial prototyping, where parts are often destroyed due to design oversights and flaws. The PIC16F73 was selected for the controller due to its low cost, useful instruction set, and its robust construction. The circuit schematic for the controller used in the unipolar pulser is shown in Figure 2.3.

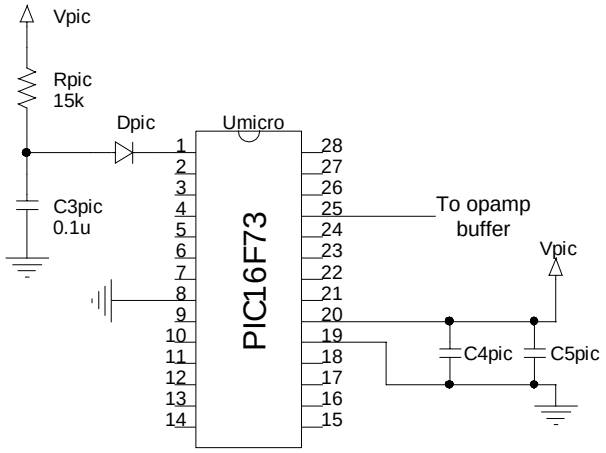


Figure 2.3: Circuit schematic for the controller of the unipolar pulser

Initially, the controller was used to provide the input to the gate circuit of only one switch. As a result the highest current drawn from pin 25, which was connected to the input of the optocoupler,

was less than the maximum supply current of the microcontroller. The current drawn by the optocoupler was measured using a differential probe across a 1Ω resistor connected to the optocoupler input. The captured waveform is shown in Figure 2.4.

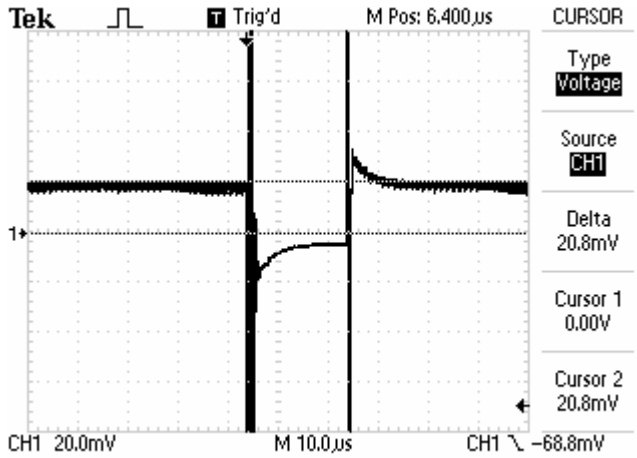


Figure 2.4: Voltage measured across a 1Ω resistor connected to optocoupler input

The current drawn by the optocoupler was measured to be 20mA. According to the PIC16F73 data sheet [38] any single input/output (I/O) pin is only able to source 25mA maximum. To increase the operating voltage of the unipolar pulser, more switches would need to be connected in series. This meant that if 4 switches were connected in series around 80mA would be drawn, which would exceed the current rating of the PIC™ microcontroller. To address this, a buffer stage had to be used. A simple op-amp voltage follower using high slew-rate op-amp has been implemented. The final configuration of this buffer stage is shown in Figure 2.5.

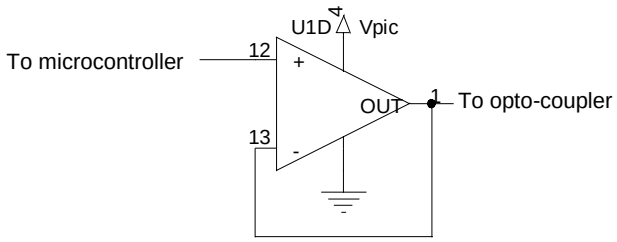


Figure 2.5: Op-amp buffer connected in between the microcontroller output and the optocoupler

This buffer stage was tested using two decade resistor boxes to determine the optimal resistance values for the feedback loop. It was found that the best performance was achieved with the use of zero resistance, in the feedback loop. The TLC2274 was selected because it has a high bandwidth as well as a high slew rate [39]. The slew rate of the op-amp was initially assumed to be adequate but observation of the output waveform from the PIC™ microcontroller and the output of the buffer stage, shown together in Figure 2.6 proved otherwise.

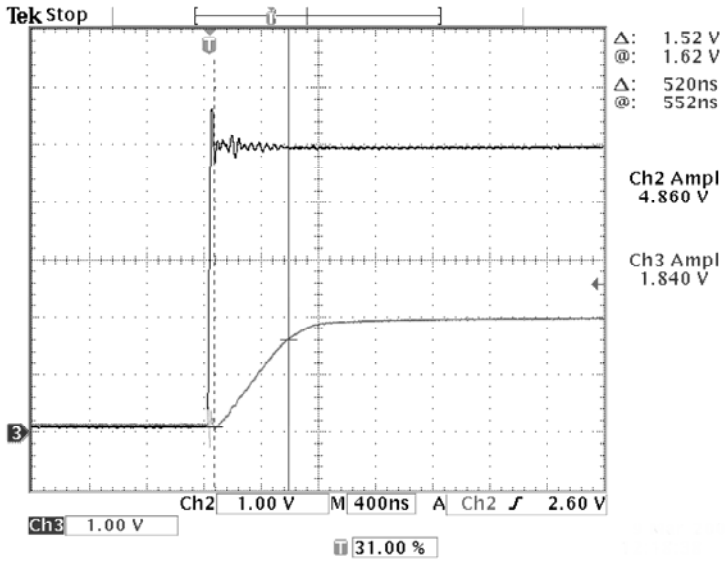


Figure 2.6: Captured output of the microcontroller (CH2 - top) and the buffer stage (CH3 - bottom)

Figure 2.6 shows that the op-amp slew rate is a limiting factor in the dV/dt of the gating signal. To verify this observation, the slope of the buffer output is calculated in (1) and compared with the slew rate specified on the datasheet of the op-amp.

$$\frac{dV}{dt} \approx \frac{\Delta V}{\Delta t} = \frac{1.52V}{520ns} = 2.9V / \mu s \tag{1}$$

The slew rate calculated from the actual waveform is quite close to the value specified on the datasheet (3.6V/µs); the variation in values could be attributed to measurement error. This limitation of the op-amp maybe one of the limiting factors of the control circuit, and is addressed in Chapter 5.

2.2.1.1 Firmware

The software to control the unipolar pulser was written in the assembly language of the PIC™ microcontroller. For the unipolar pulser the program simply needed to produce a chain of pulses which would be used to drive the power switches ON and OFF. A flow chart of the program is shown in Figure 2.7.

To generate the repeating pulse train, the program utilizes one of the built-in timer modules that are integrated in the microcontroller. For this program the TIMER2 module was used. This module works by incrementing a counter, at a user set frequency, and when the value of this counter equals the period programmed into TIMER2 an interrupt is generated. The program, shown in Figure 2.7, first begins by disabling all other interrupts, so they do not interfere with the TIMER2 interrupt. Next, pin 4 on Port B, which drives the switches, is set as an output by clearing its respective data direction (TRIS) bit, after which the timer module must be initialized. This initialization will enable the timer's interrupt as well as set the timer interrupt frequency which will in turn set the switching frequency of the pulse train. The timer interrupt frequency is controlled by the crystal oscillator

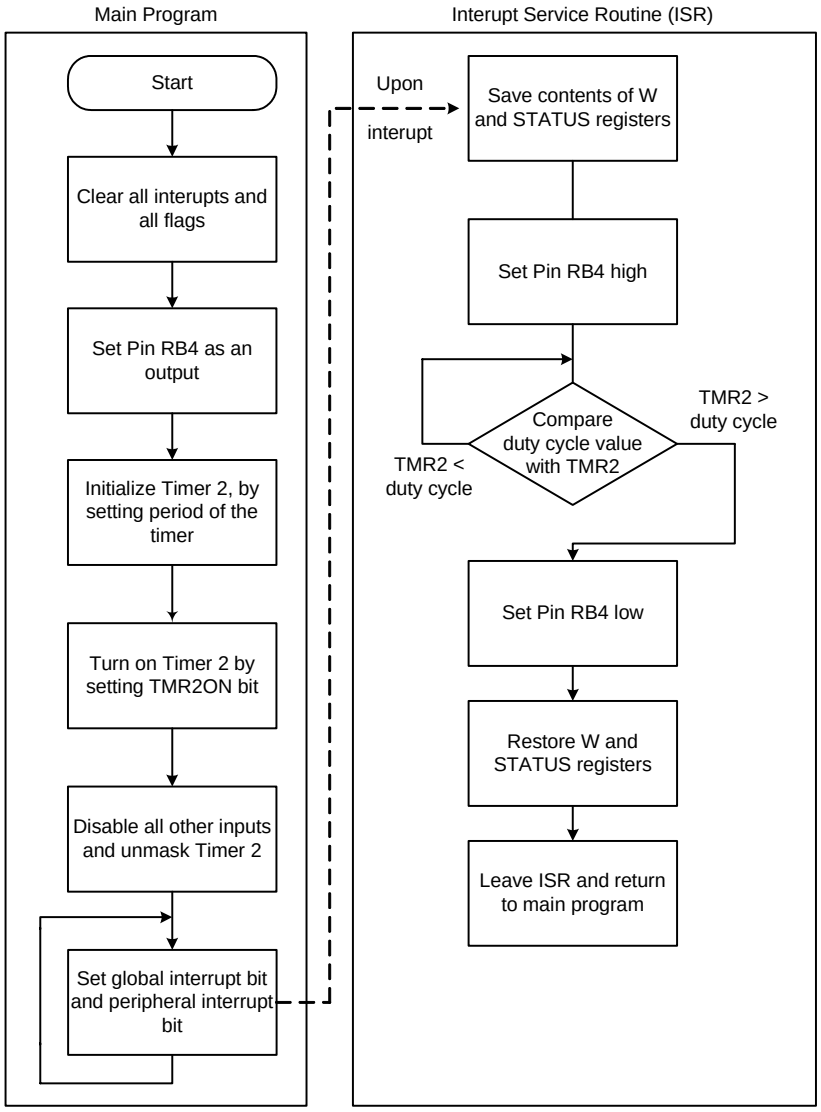


Figure 2.7: Program flow chart for the unipolar pulser firmware

frequency, the prescaler value, and the timer period register (PR2). The steps for calculating and setting the interrupt frequency are discussed below.

$$\text{Timer increment frequency} = \frac{f_{osc}}{4} \times \frac{1}{(prescaler \times postscaler)} \tag{2}$$

The crystal oscillator frequency, in (2), is divided by 4 because 1 instruction is executed for every 4 clock cycles [40]. For replicating the effects of a MV solid state drive the switching frequencies are usually between 1kHz to 3kHz [41]. The crystal oscillator frequency is 20MHz. This value is kept quite high to minimize the delay that is generated during the execution of each instruction. To reduce the frequency of the timer increment, the largest value for the postscaler (16) was used.

$$\therefore \text{Timer increment frequency} = \frac{20MHz}{4} \times \frac{1}{16 \times 1} = 312.5kHz \tag{3}$$

The timer increment frequency calculated in (3) represents the rate at which the timer will increment the counter. As stated previously the timer interrupt is generated when the timer counter (TMR2) equals the timer period register (PR2). So the interrupt frequency will be dependent upon how long it takes for TMR2 to increment from 0 to the value stored in PR2. For the unipolar pulser a switching frequency of 1.25kHz was selected for testing.

$$\text{Interupt period} = \left(\frac{1}{\text{Timer increment freq}}\right) \times PR2 \tag{4}$$

$$\text{Interupt period} = \frac{1}{\text{Interrupt freq}} \tag{5}$$

Combining (4) and (5),

$$\therefore PR2 = \frac{\text{Timer increment freq}}{\text{Interrupt freq}} = \frac{312.5kHz}{1.25kHz} = 250 = \text{0xfa (hexadecimal)} \tag{6}$$

When PR2 is set to 0xfa, an interrupt will be generated at a repetition rate of 1.25kHz. When the interrupt is generated, the PIC™ will leave the main program and execute the interrupt service routine. Within this routine the output pin which controls the switches is turned ON or OFF, based on the comparison between the timer counter and the duty cycle value set by the user. The full source code of the program for the unipolar pulser can be found in Appendix C.

2.2.2 Switch Selection

The proper selection of components for this design will require a balance between a high voltage and low current rating. Currently, MOSFETs are readily available with voltage and current ratings of 1200V and 3A respectively. For low power/low voltage pulse applications, where the current is very small, these switches are an excellent choice. For this design because the operating voltage is so high, a series connection of switches must be used. This aspect constrains the design between two opposite goals. The requirement for higher operating voltages results in the use of more switches in series. However, the use of more switches is limited by the need to keep the overall size of the device at a reasonable level.

Another important characteristic with regards to MOSFETs is that their turn on/off times are on the order of tens of nanoseconds. This makes for very sharp pulses with turn on/off times which are much faster than those found in IGBT modules. As a result these pulses will have much higher dV/dt compared to the pulses produced by a MV VSC. This aspect can be corrected by increasing the gate resistance connected to the MOSFET. This increase in the turn on/off times (reduction of dV/dt) will be at the expense of increasing the switching losses. These increased switching losses will result in additional heating which may reduce the reliability of the switching device as well as making the thermal management design more complex. Based on these considerations and the need to limit the number of series stages to a reasonable level, MOSFETs are deemed unsuitable for this application.

Turn on/off times for discrete IGBTs are on the order of hundreds of nanoseconds, which is much closer to the switching behaviour of power IGBT modules, making them the best choice. Currently, discrete IGBT units available in the market have voltage ratings of up to 1700V and current ratings up to 75A [42,43]. An IGBT switch, manufactured by IXYS Inc., model number IXBT16N170 with voltage and current ratings of 1700V and 16A respectively, was selected for use. This higher voltage

rating allows for the use of fewer switches in the series chain thus reducing the overall size of the pulse modulator.

2.2.3 Gate Circuit Requirements

Once the appropriate switches had been selected, the next part of the design was to estimate the peak current that would be required, from the gate circuit, during turn-on of the switch. The gate circuit is a very integral part of the overall design. If the gate circuit is poorly designed then the switching performance of the IGBTs will be poor. The gate circuit must be able to supply enough peak current so as to turn on the switch by fully charging the input capacitance, putting the switch into the low impedance operating mode.

During turn-on, when voltage is applied to the gate terminal, a gate current flows into the device charging this input capacitance. A very rough estimate of the peak current can be determined using the peak gate voltage and the value of the gate resistance. The gate resistance for the selected IGBTs is specified as 33Ω on the data sheet [44].

$$I_{peak} \approx \frac{V}{R_{gate}} = \frac{15}{33} = 0.45A \tag{7}$$

The above calculated value is much higher than the actual gate current and only serves to provide an estimate. This rough estimate for the peak gate current can be further refined through computations using either the gate charge value or the gate capacitance values specified for the device on the datasheet. Using the gate charge value on the data sheet, the current can be estimated by dividing the gate charge by the turn-on time of the device.

$$I_G \approx \frac{Q_G}{t_{on}} = \frac{65nC}{500ns} = 0.13A \tag{8}$$

Using the gate capacitance, the gate current can be separated into two components, one that will charge C_{GE} and the other which will charge C_{GC}, the Miller capacitance [45]. The data sheet for the device specifies three values for the capacitance: the input capacitance which consists of C_{GE}+C_{GC}, the reverse transfer (Miller) capacitance which is C_{GC}, and the output capacitance consisting of C_{GC}+C_{CE}. Using the fundamental relation, which relates the current in a capacitor with the rate of change of the voltage, and an estimated switching time of 500ns, the current component which charges the gate-emitter capacitance, I_{G1}, can be calculated as follows:

$$I_C = C\frac{dV}{dt} \approx C\frac{\Delta V}{\Delta t} \tag{9}$$

$$I_{G1} = \frac{V_{GE} \times C_{GE}}{t_{sw}} = \frac{15V \times (1400-31)pF}{500ns} = 0.0411A \tag{10}$$

Next, the current which charges C_{GC} is calculated. It is assumed that under normal operating conditions the collector emitter voltage (V_{CE}) will not exceed 1500V. The IGBTs used in this design are rated for 1700V but they will be operated at no more than 1500V to allow for a safety factor.

$$I_{G2} = \frac{V_C \times C_{GC}}{t_{sw}} = \frac{(1500-15)\times 31pF}{500ns} = 0.0921A \tag{11}$$

Summing the results of (10) and (11) the total estimated gate current can be computed.

$$I_G = I_{G1} + I_{G2} \tag{12}$$

$$\therefore I_G = 0.0.0411 + 0.0921 = 0.13A \tag{13}$$

Based on the previous calculations the gate circuit will be required to provide around 150 mA during the turn on of the switch.

2.2.4 Isolating Mechanism/Gate Drive Circuit

The operation of the proposed pulser requires the use of a series chain of switches to allow the device to operate safely at higher voltages. This means that the gate terminal of all the switches except the bottom one in the chain must be supplied with floating gate signals. To accomplish this, the controller must be electrically isolated from the switches. Another advantage of electrically isolating the controller from the high voltage switches is that it protects the controller from any spikes, surges, or interference that may occur on the high voltage side. There are three potential ways of accomplishing this electrical isolation either through the use of optical isolation, gate drive transformers, or passive triggering of the series chain.

Passive triggering a series chain of IGBTs requires that the bottom switch be actively triggered and then all the other switches in the chain are then capacitively coupled to that switch. When the bottom switch turn's on, the switches above also begin to turn-on. This arrangement has a very low component count, and is in theory able to balance the turn on voltage of each device [46]. The results that have been published using series IGBTs are not very promising. During turn off, it is found that each switch in the chain turns off sequentially [46]. This means that each switch may be exposed to voltages exceeding its rating during turn off, potentially damaging the switch. Another limitation of this design is the fact that during long duty cycles, the coupling capacitors can become fully discharged [45] which may result in the switch turning off prematurely.

The next option was the use of gate drive transformers. This option, like the previous one, has the advantage of being very compact. The main problem with this solution is that currently the majority of gate drive transformers available on the market are only compatible with switching frequencies of 10 kHz and above. As stated previously the purpose of this device is to replicate the waveform found in a MV drive so the switching frequency must stay between 1 and 3 kHz. As a result it is very difficult to find any commercial units compatible with the previously specified switching frequency.

Several commercial units as well as a lab built unit were tested to examine if they could potentially work in the current application. The test results obtained with the commercial units were poor and so a lab built gate drive transformer was constructed using a ferrite core. The test results for the lab built transformer are shown in Figure 2.8.

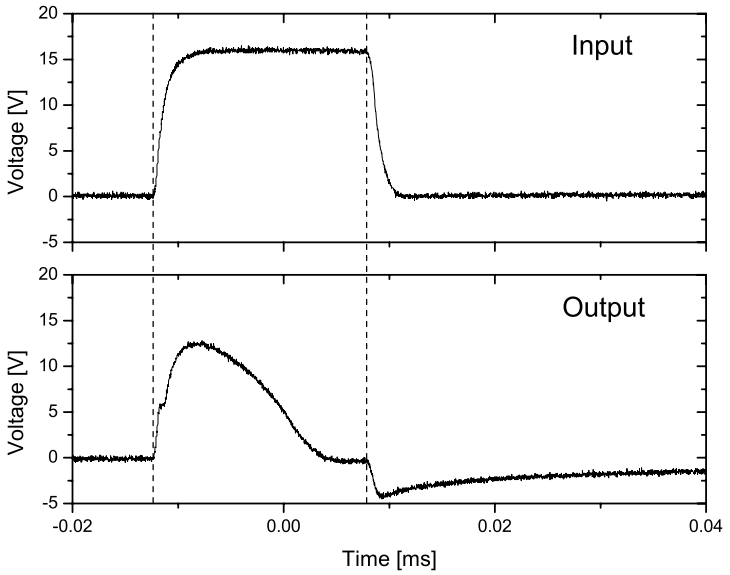


Figure 2.8: Input pulse from controller to the gate transformer (top) and the output signal from the transformer to the gate of the switch (top)

The gate drive transformer was tested by connecting it to the controller, the recorded waveform from the controller is shown in Figure 2.8. The output of the gate drive transformer was connected to the gate of an IGBT switch, the waveform observed at the gate terminal of the switch is shown in the bottom of Figure 2.8.

The voltage waveform captured in Figure 2.8 shows that with the transformer the gate voltage did rise above the threshold required to turn on the switch, and the plateau during the charging of the

Miller capacitance can even be observed. While the turn on behaviour of the switch is acceptable, the distortion in the gate signal and its premature drop before the turnoff of the input causes the switch to turn-off early. This type of behavior may be tolerable in a unipolar pulser where the duty cycles can be kept extremely short, but for a PWM inverter this characteristic is unacceptable. The pulse widths in PWM are specifically set so that the signal contains a low frequency fundamental component. As a result of the incompatibilities of the previous two methods, optical isolation techniques were utilized.

The major downside of using optocouplers to drive every switch in the chain is that each optocoupler requires an isolated DC power supply. This will occupy a lot of space on a circuit board as compared to the previously discussed solutions. This increased component count makes the overall size of the pulse modulator larger, and potentially reduces the overall reliability of the device. This reduced reliability can be attributed to the fact that with more components in the design, there are more components which could fail. To use the optocouplers in this application four important criteria must be met: high insulating voltage, high transmission speed and bandwidth, low propagation delay, and being readily available. The HCNW4504, manufactured by Agilent, was selected because it was found to meet all these criteria. There are a number of other optocouplers which offer better performance as well as higher insulating voltages, but they were not readily available at the time and so could not be used in the design. The major limitation of the HCNW4504 is that its output current is limited to 16mA peak [47]. This makes the device unable to supply enough current to properly latch the IGBT switch on. To remedy this problem a buffer stage is required to supply the needed current.

Initially, a MOSFET based buffer stage, shown in Figure 2.9, was selected for use. The advantage of this buffer is that it can produce very fast outputs with extremely short rise times. In this way the gate signal from the optocoupler is not affected like the output from the PIC was affected by the op-amp buffer stage used in the controller. Simulations of the buffer stage, in PSPICE, showed that it

operated normally and was able to properly drive the IGBT switches on and off. Next, the buffer was implemented on a prototype board with the controller and the preliminary results showed lots of noise and instability in the output, periodically. This instability may have been due to other problems such as a flaw in the construction of the board, or a bad solder joint. Due to these problems and time constraints, a transistor based buffer stage, shown in Figure 2.10, was selected for use.

The transistor based buffer uses two matched bipolar transistors and is recommended in many application notes produced by IGBT manufacturers [48,49,50]. The MPS8099 and MPS8599 transistors were selected for use because they have high sufficiently high peak current ratings and are capable of high switching speeds.

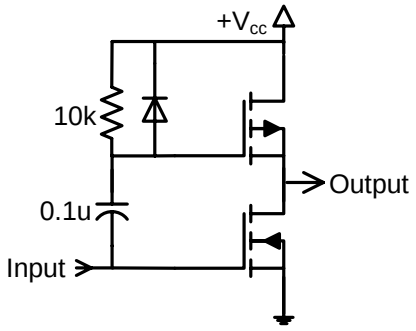


Figure 2.9: MOSFET based push-pull buffer stage for use in the driver circuit of the IGBT

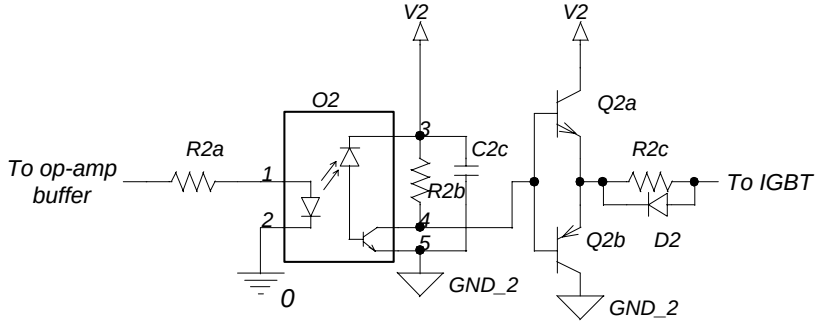


Figure 2.10: Circuit schematic of the drive circuit for an IGBT

In Figure 2.10, resistor R2a was inserted in the input of the optocoupler to limit the peak current into the device. The output voltage of the op-amp buffer stage varies between 0 and 5V, and the maximum rated input current into the optocoupler is 40 mA [46]. Based on these two criteria, the value of the current limiting resistor can be calculated as follows:

$$\therefore R_{\lim it} = \frac{V}{I_{in(peak)}} = \frac{5V}{40mA} = 125\Omega \tag{14}$$

Tests on the actual circuit using a decade resistor box showed that a resistance of 200Ω provided improved performance and hence 200Ω was substituted for the initially calculated value of 125Ω.

One modification to the gate circuit which was investigated was the use of "reverse biasing" on the gate terminal of the switch. This simply means that a negative voltage is applied to the gate terminal during turn off. Some of the literature suggests that applying a negative voltage during turn-off of the IGBT can reduce the turn-off time, by speeding up the discharge of the gate capacitance [49]. Alternatively it has been observed that the reverse biasing has no effect on the speed of the turn off, rather it serves to only make sure that the device remains turned off should any noise be induced at the gate terminal [47,51].

To determine whether this reverse bias would improve the turn off performance of the IGBT, a negative supply was added to one of the drive circuits. No improvement was observed when applying -5V to the gate terminal during turn off of the switch. As a result, the idea was not implemented in the final design of the pulse modulator.

The capacitor, C2c, is connected across the power and ground terminals of the optocoupler, in Figure 2.10, to remove any ripples in the +15V supply, its value of 0.1μF was adopted from the datasheet [46]. A 20kΩ resistor, R2b, was connected between the power and output terminal of the optocoupler as per [46,52]. Finally, a fast diode (1N4148) is connected in parallel with the gate

resistor to provide a low impedance path for the gate capacitance of the switch to discharge through during turn off [51].

Once the gate circuit was assembled, it was tested and several measurements were made to verify that the design was adequate and that the switch was able to properly turn-on. Using an oscilloscope, the gate current, the gate voltage, and the collector emitter voltage of the IGBT switch were recorded.

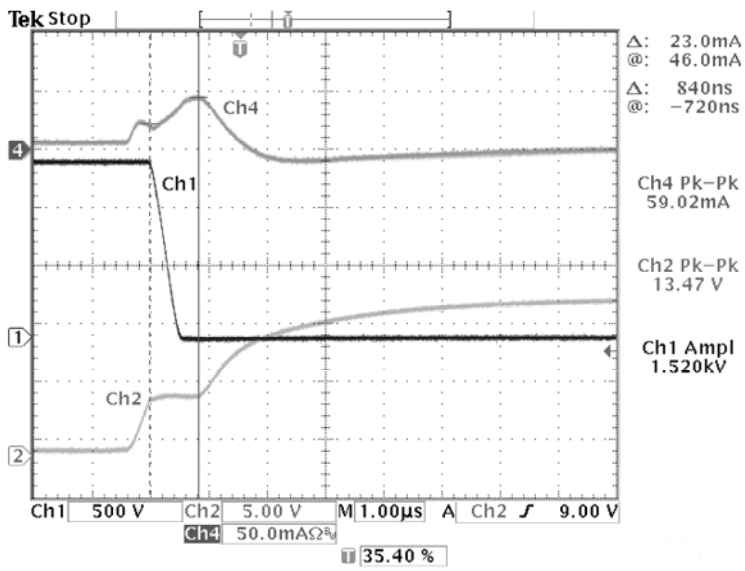


Figure 2.11: Switching waveforms during turn on: V_{CE} (CH1), gate voltage - V_{GE} (CH2), gate current - I_G (CH4)

Figure 2.11 shows the relevant switching waveforms with a collector voltage of 1.5kV applied to the IGBT switch. At peak the gate current is measured to be 59mA, which is about half the initially estimated value from Section 2.2.3, and significantly lower than the 130mA that was calculated in the previous section. The gate current, in Figure 2.11 was recorded using a current probe connected around the gate lead. The negative dip in the gate current could be attributed to measurement error in the probe.

Figure 2.11 shows that the IGBT properly turns on when the gate signal is applied. It is observed that when the gate voltage rises and reaches a threshold value, the collector emitter voltage begins to drop. Then the gate voltage reaches a plateau, which is where the Miller capacitance is charged, and just at the end of this plateau, the peak gate current occurs. In many publications, the location of the peak gate current is often found at the beginning of the current pulse [53], the distorted gate current could be due to the characteristic of the selected IGBT switches. Once the Miller capacitance is charged, the voltage smoothly rises up towards the applied 15V.

Next, the turn off behavior is recorded to make sure that the drive circuit is functioning normally during turn off.

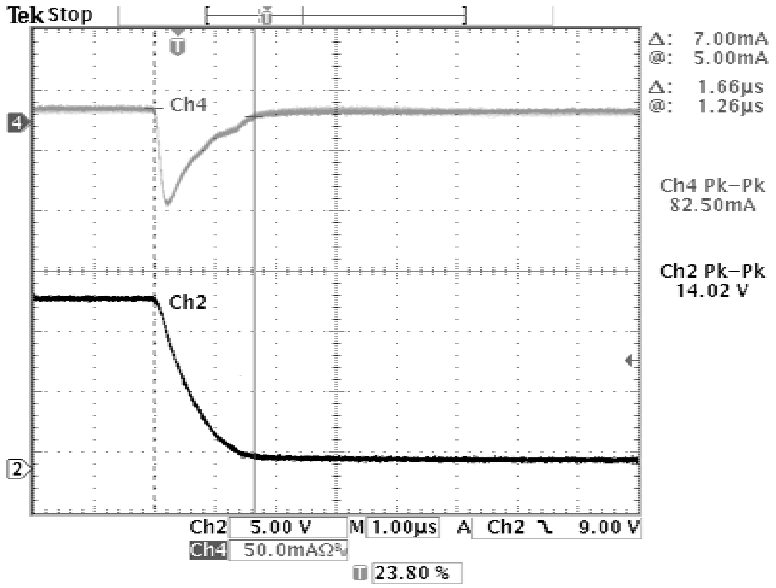


Figure 2.12: Switching waveforms during turn off: gate voltage - V_{GE} (CH2), gate current - I_G (CH4)

The gate current captured during turn off in Figure 2.12 closely resembles the typical waveform expected during the turn off of the IGBT.

2.2.5 Snubber Design

Under ideal circumstances a simple series chain of switches with no voltage sharing scheme may be acceptable, but in reality device variation and other factors must be considered and so some form of voltage sharing must be utilized to keep the switches operating within their safe operating areas (SOA). These voltage sharing techniques can be divided in two main groups: passive (snubbers) and active which involves controlling the gate signal to control the voltage sharing [54]. Due to the limited functions available in the controller and to keep the design and construction of the pulser as simple as possible, only passive snubbers will be utilized to control the voltage sharing. The most common voltage sharing technique is the use of parallel resistors for steady state voltage sharing in a series chain of switches. Here the design criteria for the selection of the resistor value is simply based on the shunt current in the resistors being ten times larger than the largest leakage current of the switches in use [37]. For this design, 2MΩ shunt resistors were selected based on the 50μA leakage current specified for the switch. Initial operation of the chain of switches demonstrated that this snubber was suitable to operate the chain safely, without damaging any components, and the resulting waveform can be seen in Figure 2.13.

Measurements with a differential probe demonstrated that while the steady state voltage was indeed equalized, the transient voltage across each switch was different. This is observed in Figure 2.14, which shows that the top switch is subjected to most of the transient voltage during turn off. To correct this problem, snubbers were tested to equalize the transient voltage across each switch during

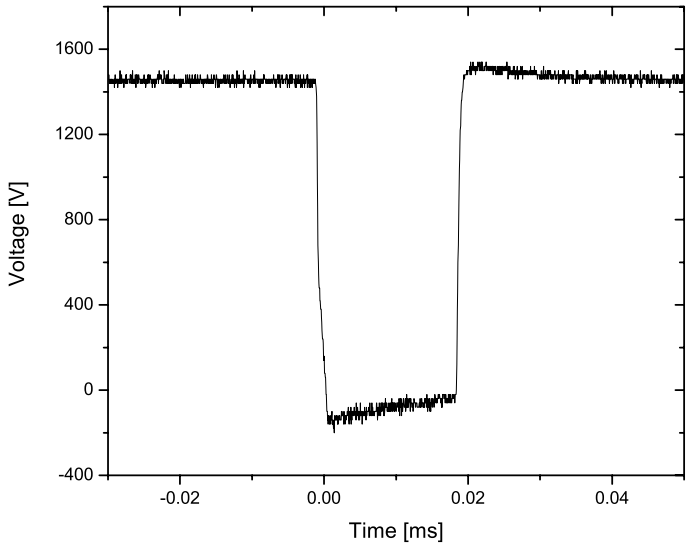


Figure 2.13: Output waveform observed using two switches connected in series with resistive snubbers only

turn off. The simplest solution for transient voltage sharing was through the use of capacitors placed in parallel with the switches [55,56]. The size of the capacitors was determined from the collector-emitter capacitance, and through experimentation with different values. Using this criterion, 1nF capacitors were found to be the smallest capacitance that had a noticeable impact on the transient voltage sharing. This solution equalized the transient voltage but created another concern instead; the turn off time of the switch became much longer distorting the pulse shape. This is shown in Figure 2.15 which compares the pulse shape with and without snubber capacitors installed.

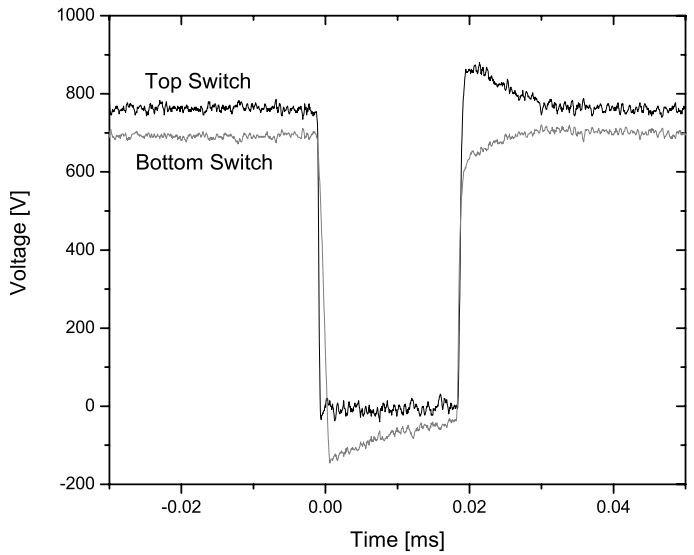


Figure 2.14: Voltage measured across each switch in a series chain of two switches with resistive snubbers only

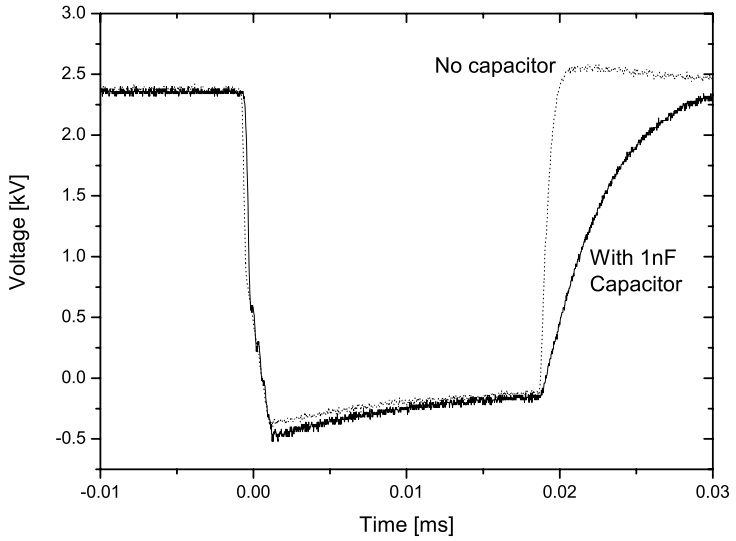


Figure 2.15: Comparing the effect of RC snubbers with resistive snubbers

For switching resistive loads, a gradual turn off in the pulse shape may be acceptable but for use with insulation testing, where loads are predominantly capacitive, the capacitive snubber will only serve to further increase the turn off time. If the turn off time of the output becomes too long this will limit the applications of this pulser. One initial application this pulser was used for was for characterizing the dielectric properties of dielectric materials under pulse conditions using the techniques specified in [57,58]. This would not be possible because the long turn off (low dV/dt) makes the current conducted through the sample very small, due to I=C*dV/dt. As a result, when using capacitive snubbers, it was difficult to obtain all the required measurements to carry out the computations. After much testing with different snubber values coupled with different loads it was determined that it was best not to use the capacitive snubber.

2.3 Bipolar Pulse Generator

The 2-level inverter topology was selected because it offers the simplest control algorithm as well as the simplest construction. As discussed previously, completely replicating a MV VSC would require a multi-level inverter. Due to constraints such as size and the need for multiple high voltage DC sources and capacitors, which were not available, a multi-level topology was not used. The 2-level inverter will replicate the most important aspects of a MV VSC's waveform: the rise time (high dV/dt), the fundamental component (50/60 Hz), and the high frequency components (harmonics). The major weakness of the 2-level inverter as discussed previously is the fact that each leg of the inverter will be exposed to the full DC-link voltage, which will limit the maximum operating voltage.

2.3.1 Controller

The controller constructed for the bi-polar pulser, shown in Figure 2.16, is very similar to the one that was previously discussed for the unipolar pulser. The major changes are the use of 4 I/O pins for each leg of the H-bridge, the use of a keypad for added user functionality, and a new firmware. By controlling the 4 separate legs accordingly, the required waveform can be produced at the load. Because each I/O pin would be driving multiple switches (due to the series connections) the voltage follower buffer found in Section 2.2.1, was implemented for each switch.

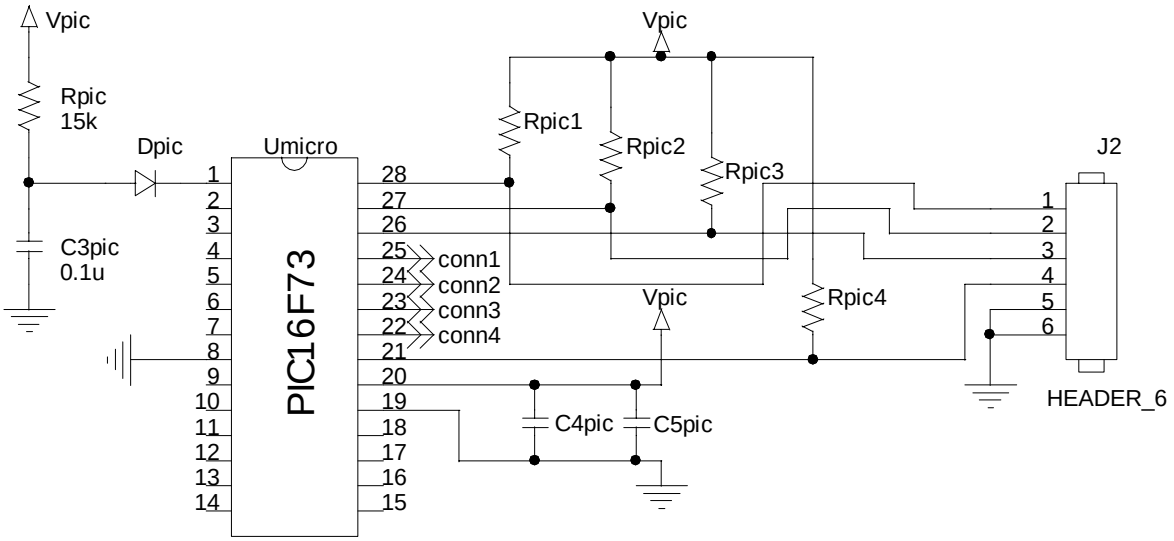


Figure 2.16: Circuit schematic for the controller in the bipolar pulse modulator

2.3.1.1 Firmware

The firmware used in the bipolar pulse modulator adopts the same basic framework as the one used in the unipolar pulser. The main differences are the additional use of the capture, compare, PWM (CCP) module, and the use of the ROM to store the PWM duty cycle data. A simplified flow chart for the bipolar firmware is shown in Figure 2.17.

In this firmware a keypad was built into the controller circuit to allow the user to control the program during the operation of the pulse modulator. The keypad has 4 buttons: start, stop, increase fundamental frequency, and decrease fundamental frequency. The current settings in the firmware allow the user to vary the fundamental frequency from 1 to 60Hz. This was accomplished by either increasing or decreasing the step size of the counter which was used to determine the address of the appropriate sine value stored in the ROM. The lookup table was stored starting at address 0x100. Then as the counter incremented during program execution, the counter was added with the base address to get the location for the required sine value. As the step size of the counter is increased, the fundamental frequency was increased. The opposite would occur as the step size was decreased.

One of the settings in the firmware that had to be carefully considered was the insertion of a dead time between when the currently conducting switches of the inverter are turned off and when the opposite switches are turned on. This is especially important with capacitive loads, because as discussed previously, the turn off time of the pulse increases with the capacitance of the load. Experimentation with the unipolar pulser has shown that turn off times on the order of 5 to 10 μs are possible depending on the magnitude of the capacitance of the test object. Initially, the PIC was programmed with a dead-time of 8 μs, shown in Figure 2.18. For smaller capacitive loads such as, small magnet wire samples and stress grading systems [10], this dead time was adequate.

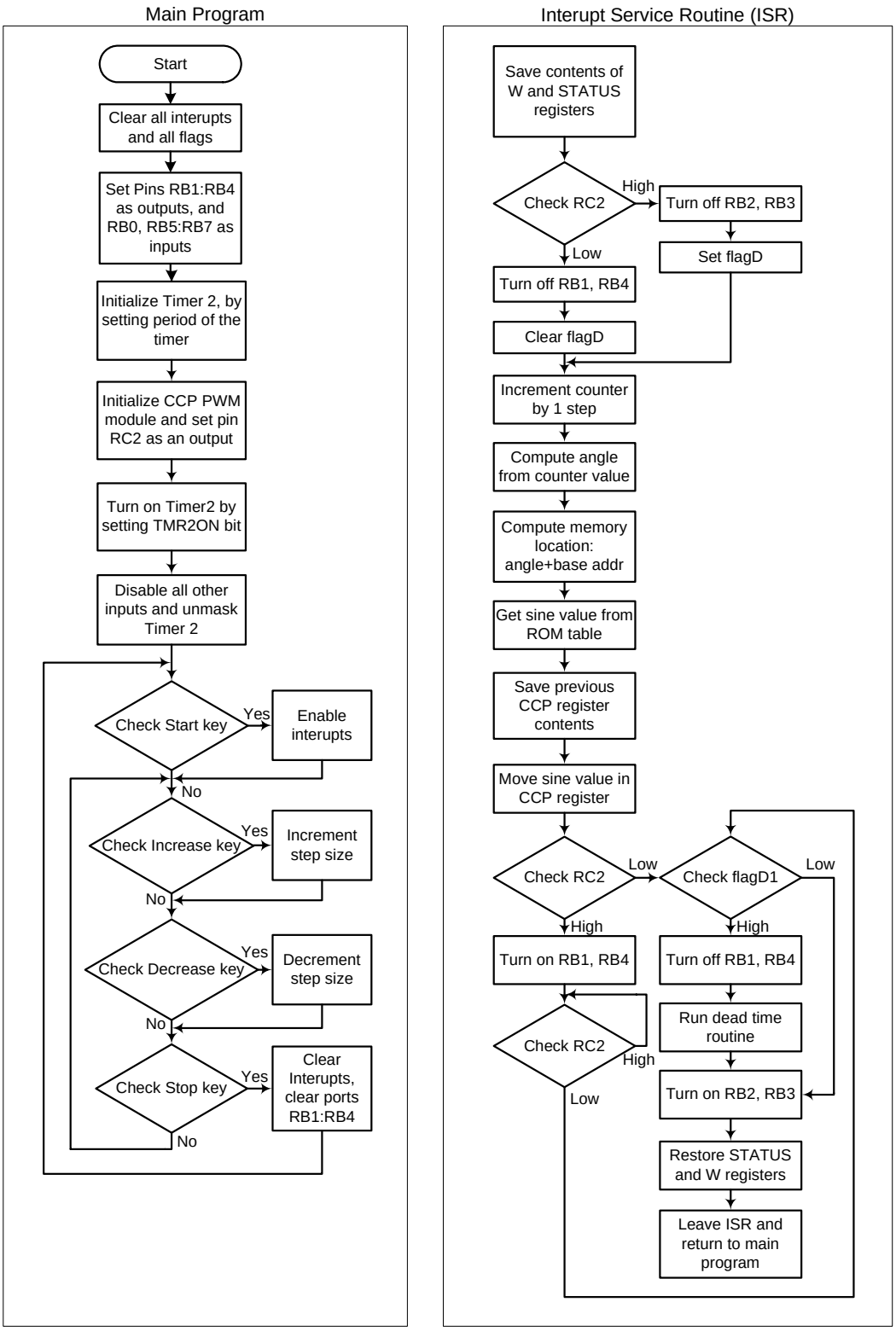


Figure 2.17: Program flow chart for the bipolar pulse modulator firmware

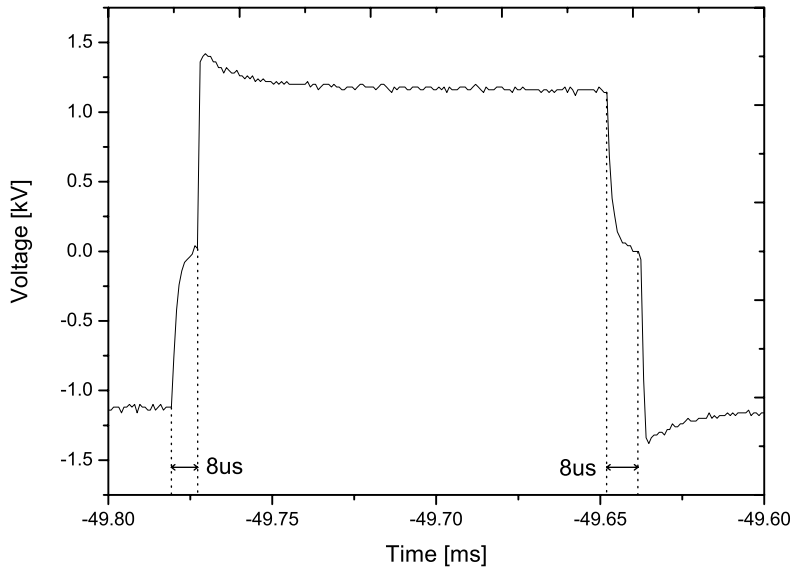


Figure 2.18: Dead time inserted in the bipolar pulse modulator output

2.3.2 Isolating Mechanism/Drive Circuit

The optocoupler was again selected for use in this application, and its discussion can be found earlier in Section 2.2.4.

2.3.3 Printed Circuit Board (PCB)

After testing the unipolar pulser and planning the layout for the bipolar pulse modulator it was decided that 4 switches would be used in each section of the inverter. This would allow a DC link voltage of 6000V, while allowing for each switch to be de-rated by 200V. Using a DC link voltage of 6000V would produce a 12kV peak to peak output. Using 4 switches per section would keep the overall size of the device practical while allowing for reasonably high voltage operation. To make

sure that all the circuits were consistently identical, a printed circuit board (PCB) was designed and manufactured for use in the modulator. The designed circuit board is shown below in Figure 2.19.

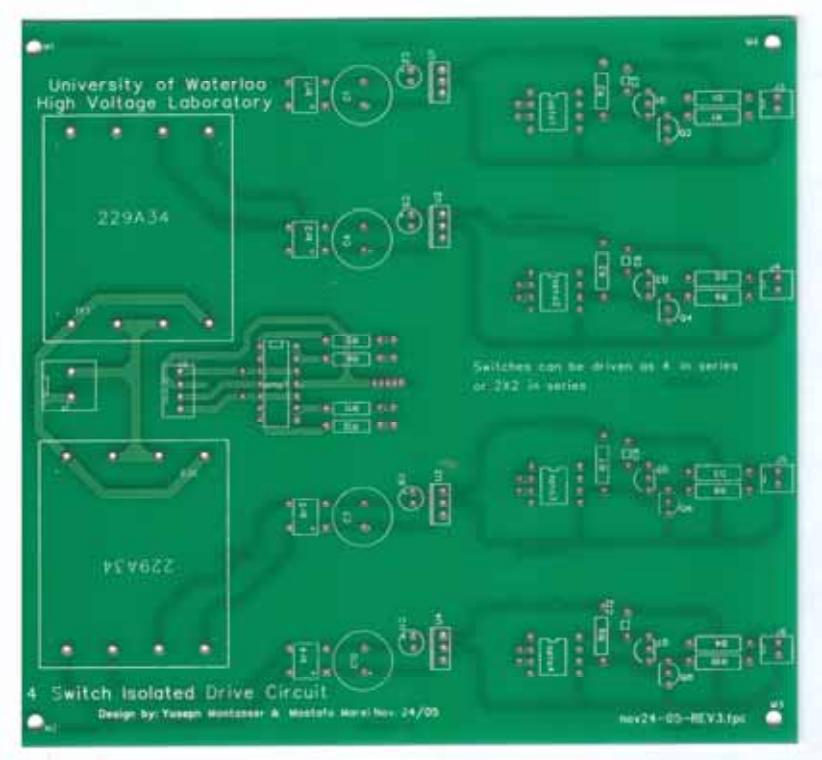


Figure 2.19: PCB designed for high voltage inverter

The actual Gerber file for this design, with all the layers can be found in Appendix G. When routing the PCB, several parameters such as trace width and clearance must be carefully considered. This is especially important because the board will be exposed to differential voltages up to 5kV. IPC standard 2221 contains all the relevant information with regards to electrical clearances and trace widths for printed circuit boards. A trace width of 1.27mm (50 mils), which is suitable for up to 3A, was selected to make sure that all connections between parts were of extremely low impedance. This was also done to ensure that if a short or spike occurs, only the components on the board are damaged the traces in the board would still survive. The value of the electrical clearance required for a voltage

difference of 2kV, which would be the maximum voltage difference between adjacent gate drive circuits, was determined to be around 20.32mm (800 mils). This value was extrapolated from the data available in the IPC standard. The use of these circuit boards greatly simplified the construction of the bipolar pulser. As well the use of these boards will allow for the construction of identical gate circuits for each switch. This will make the propagation delays of all the gate signals identical, which makes it much easier to trigger all the switches together at the correct time. The identical construction of all the gate circuits removed the slight bend that is apparent in the pulse shown in Figures 2.13 and 2.15.

2.4 Completed Modulator

Once all the design aspects and all the details had been planned out, the device was constructed. The completed modulator, shown in Figure 2.20, was initially built on a flat sheet of plastic without an enclosure.

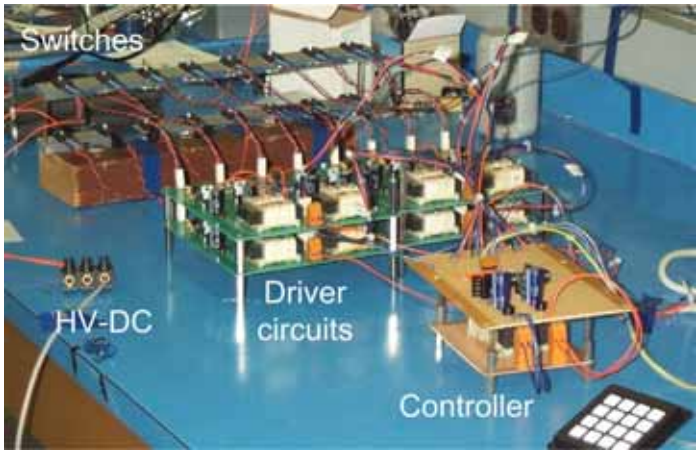


Figure 2.20: Completed high voltage low power inverter

2.5 Conclusion

This chapter covered the design and development process of the bipolar pulse modulator. Some of the important component choices as well as important milestones were discussed. Schematics of both the unipolar pulser and the bipolar pulse modulator can be found in Appendices A and D, respectively. While the bill or materials' for each unit can be found in Appendices B and E, respectively. The firmware for the unipolar pulser can be found in Appendices C and the Gerber file for the PCB designed is given in Appendix F.

Chapter 3
Results

3.1 Introduction

Once the pulse modulator had been constructed, it had to be tested to verify that it produced the outputs it had been designed for. As well, the limits of the device must be determined to understand the maximum load that can be connected to the output. This section briefly discusses the possible output waveforms that can be produced by the pulse modulator. Depending on the firmware programmed in the PIC™ microcontroller there are 3 possible operating modes for this device. These modes will be covered in the sections below along with a study of the performance of specific sections of the modulator.

3.2 Controller Performance

The PIC16F73 which was selected as the controller for use in the pulse modulator, proved to be more than adequate in normal operation. The outputs of all four channels of the controller are captured in Figure 3.1.

Upon initially testing the device everything worked as expected. As the DC link voltage was increased above 1kV the controller began to sporadically reset itself. This problem was attributed to the electromagnetic interference (EMI) produced by the switches. As the voltage increased so did the magnitude of the current. The controller board is not built on a printed circuit board and so does not have a ground plane to make it more resistant to EMI.

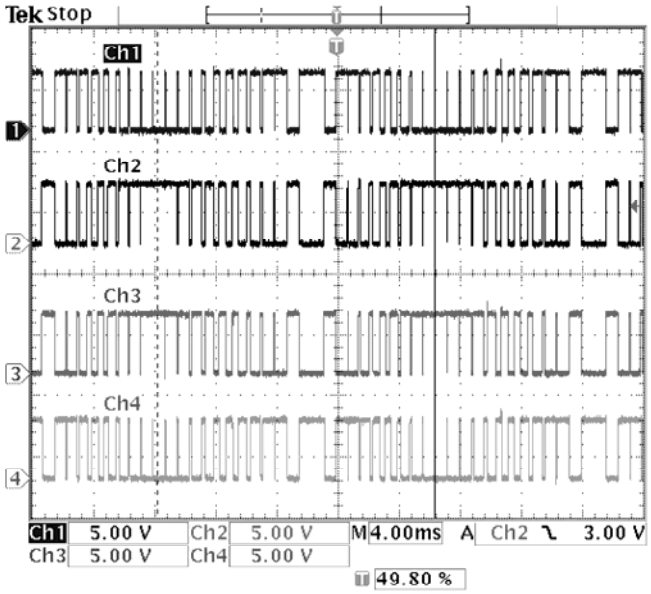


Figure 3.1: Outputs for the 4 sections of the inverter from the microcontroller

To combat this problem, the switches as well as the drive circuits were mounted in a grounded enclosure, shown in Figure 3.2, while the controller was mounted in another grounded enclosure, shown in Figure 3.3. This reset condition was also observed when "noisy" test samples were connected at the output of the modulator. Noisy in this case refers to excessive PD and corona activity due to the geometry and construction of the sample.

After the addition of the two enclosures the effects of the EMI only became noticeable at DC-link voltages above 4kV.

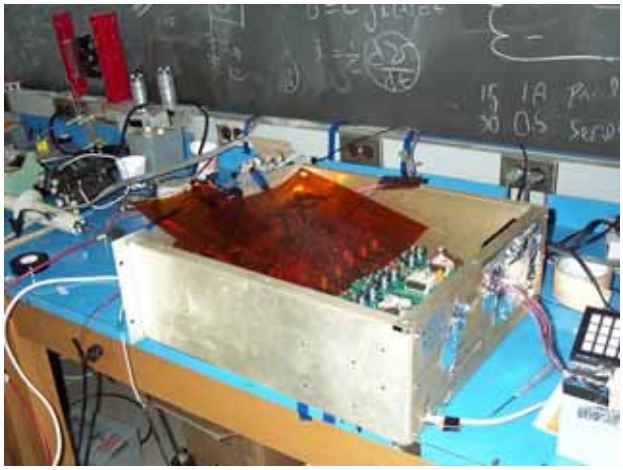


Figure 3.2: Pulse modulator being mounted into a grounded enclosure

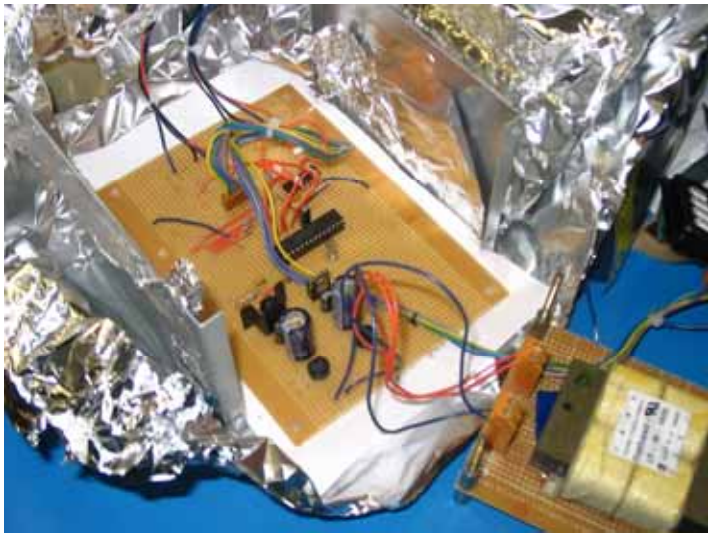


Figure 3.3: Control circuit of the modulator being mounted into a grounded enclosure

3.3 Driver Circuit Performance

As was discussed in Section 2.2.4 the performance of the driver circuit was shown to be adequate. On the previously captured gate voltage waveform it was shown that at the application of the gate signal, the gate voltage began to ramp up until it plateaus during the charging of the Miller capacitance. After the Miller capacitance the voltage continues to rise until it settles at the steady on

state value of +15V. This charging of the Miller capacitance indicates that the switch is being properly driven from its off state to its full on low impedance state.

One phenomena, which was observed during the construction of the modulator, was that as the collector emitter voltage increased, the shape of the gate current waveform also began to change. This is shown in Figures 2.12, 3.4, 3.5, and 3.6. As V_{CE} increases, a second peak appears and continues to grow until it reaches half the magnitude of the first current peak. The reason for this current peak may be attributed to the device characteristics of the IGBT device.

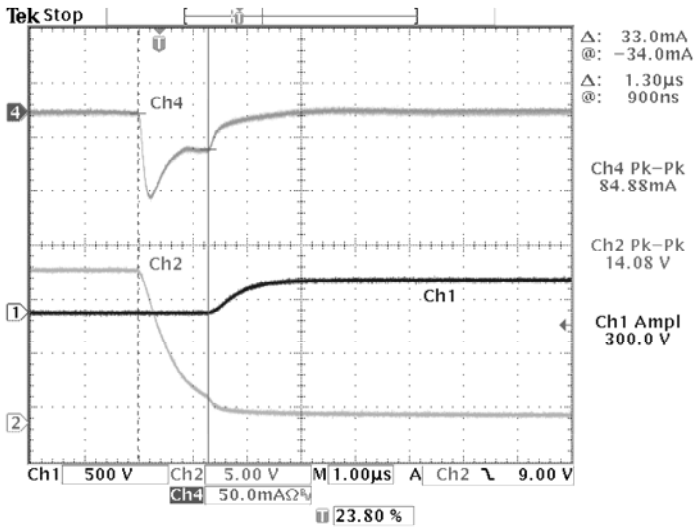


Figure 3.4: Switching waveforms during turn off: V_{CE} (CH1)=300V, gate voltage - V_{GE} (CH2), gate current - I_G (CH4)

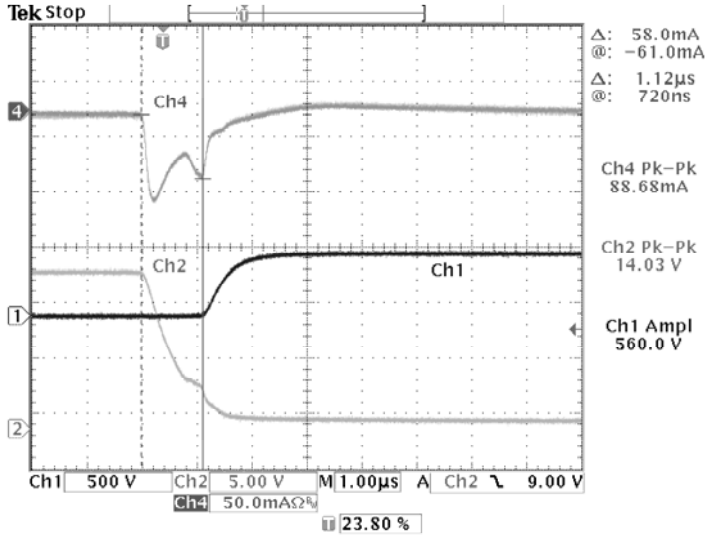


Figure 3.5: Switching waveforms during turn off: V_{CE} (CH1)=560V, gate voltage - V_{GE} (CH2), gate current - I_G (CH4)

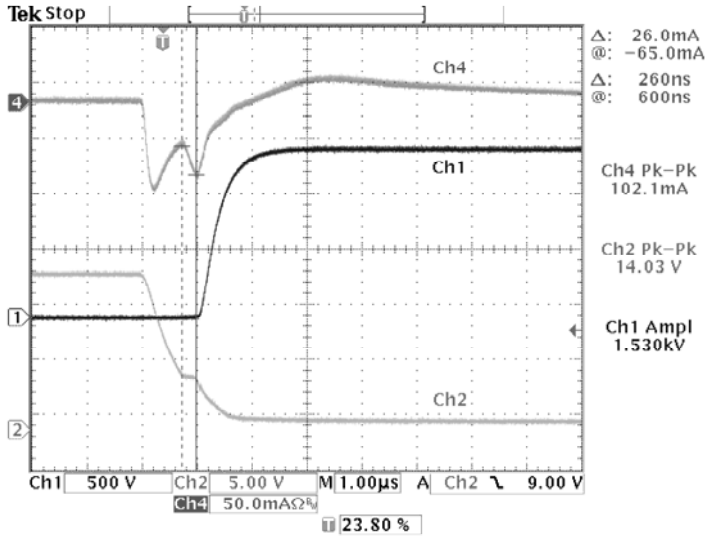


Figure 3.6: Switching waveforms during turn off: V_{CE} (CH1)=1.5kV, gate voltage - V_{GE} (CH2), gate current - I_G (CH4)

3.4 Output Waveforms

Depending on the firmware programmed in the PIC™ microcontroller, there are three possible output waveforms that can be produced by the pulse modulator which are summarized in Table 3.1. It should be noted that for all three operating modes the connection of the load remains the same.

Table 3.1: Comparison of all output waveforms which can be produced by the modulator

Firmware		Type	Switching Frequency	Carrier Frequency	Fundamental Frequency	Number of Pulses	Duty Cycle
1	Unipolar	Squarewave	1Hz-25kHz	N/A	N/A	1-infinity	1%-100%
2	Bipolar	Squarewave	1Hz-25kHz	N/A	N/A	1-infinity	1%-100%
3	Bipolar	Sinusoidal PWM	N/A	1.25kHz	0.1-60Hz	N/A	N/A

3.4.1 Unipolar Square Wave

In this mode the pulser produces a train of unipolar pulses with a switching frequency and duty cycle based on what the user specifies in the firmware. The magnitude of pulse is controlled by the external HV-DC source. The switching frequency is limited by the maximum switching frequency of the IGBTs in use. The datasheet for these devices does not specify a maximum switching frequency, but based on the observed turn on and turn off times as well as the minimum possible duty cycle, the switching frequency could be as high as 20kHz.

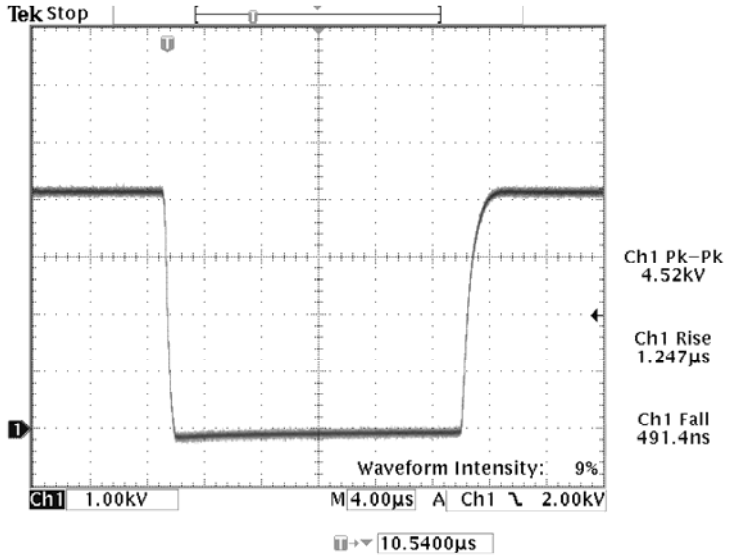


Figure 3.7: 4.5kV unipolar pulse with a fall time of 490ns, turn off time of 1.2us and a very low duty cycle

Figure 3.7 shows a single pulse. A turn-on time of 300ns can be obtained depending on the collector current in the IGBTs. The length of the turn-off time is dependent on the capacitance, and was discussed in detail in Chapter 2. The switching times while not extremely fast compared to MOSFET switching times, this turn on time is perfectly acceptable for insulation testing applications and matches the initial requirements that were set out in Chapter 1.

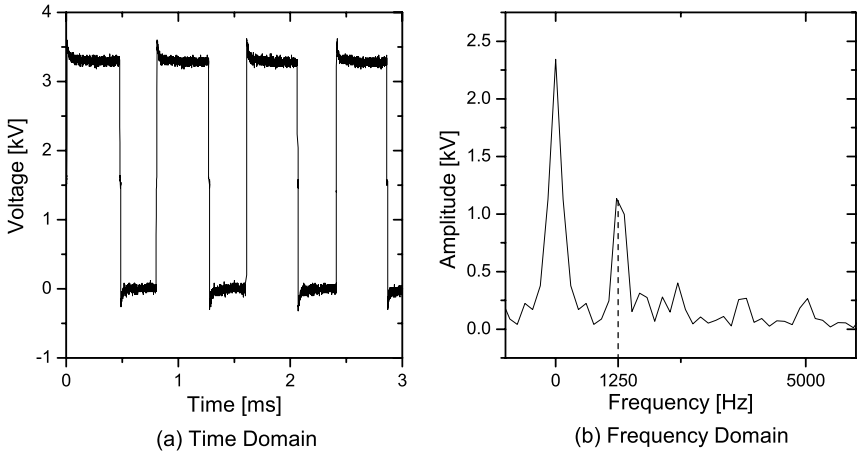


Figure 3.8: Captured train of unipolar pulses with 65% duty cycle (a) Fourier spectra of the captured signal (b)

Figure 3.8(a) shows a train of unipolar pulses, which was recorded with a magnet wire sample connected in parallel with the load resistor. The overshoots in the voltage are due to the inductance in the leads used to connect the sample to the pulse generator. The captured waveform was then analyzed and its Fourier spectrum generated, which is shown in Figure 3.8(b). The Fourier spectrum shows that the two major components of the unipolar pulses occur at 0Hz and the switching frequency, which is unlike a PWM signal which has large harmonic content. The component at 0Hz represents the DC average of the voltage which is inherent in any unipolar signal. This value can be significantly reduced by reducing the duty cycle of the pulse. For most unipolar pulse systems the duty cycle is kept very small either to keep the pulse transformer from saturating or due to the limited size of the energy storage capacitor. As a result the DC component is very small and so does not have much of a contribution when unipolar pulses are used in insulation testing, meaning that the majority

of the stress is produced by the component at the switching frequency. The effects of this reduced harmonic are investigated and compared with the effects of an actual PWM signal in Chapter 4.

3.4.2 Bipolar Square Wave

Operation in this mode simply requires the firmware for the unipolar pulser to be modified by inserting some code to turn-on the opposite switches when the currently conducting switches are turned off. This mode was never utilized in any tests and so was never implemented. The reason this mode is mentioned is because many pulse power applications currently utilize unipolar pulses in their present implementations, due to the ease with which a unipolar pulse power source can be constructed. This stands out in contrast to some of the literature which states that bipolar pulses are much more effective than unipolar pulses [59].

3.4.3 Sinusoidal Pulse Width Modulation

This output waveform was the main focus of this work. As discussed previously, there is no literature comparing the aging effects of an actual PWM waveform with unipolar square wave pulses that are used in the majority of the work done on insulation systems. The construction of this bipolar pulse modulator and its PWM output will now allow for subsequent testing and comparison of the aging effects of both waveforms. The output that was produced by the modulator is in Figure 3.9. The fundamental component is superimposed onto the voltage waveform to show that the output is in fact a sinusoidal PWM voltage with a peak-to-peak magnitude of nearly 7kV.

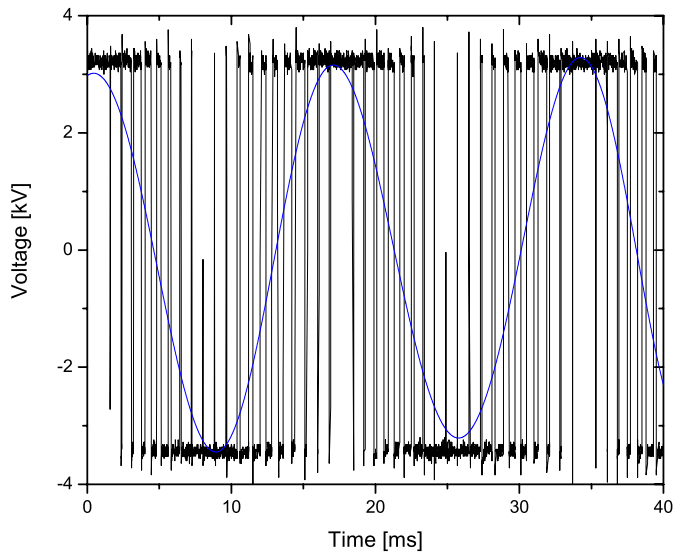


Figure 3.9: PWM output, showing a superimposed fundamental frequency, measured using two high voltage probes which were then subtracted using the math function

Due to the nature of the connection of the load in the inverter, both connections to the load are floating. As a result, to properly capture the output wave form, a differential probe should be used. Due to the lack of a differential probe with high enough ratings, two high voltage probes were used instead. Then the math function in the scope was then used to subtract the two waveforms, this is shown in Figure 3.10. The maximum DC-link voltage with which this modulator was operated was 3.6kV. This produced an output voltage with a peak-to-peak voltage of 7.2kV. In theory the modulator should be able to operate with a maximum DC-link voltage of 6.8kV. But due to safety and operating issues with regards to such high voltages this value was never reached.

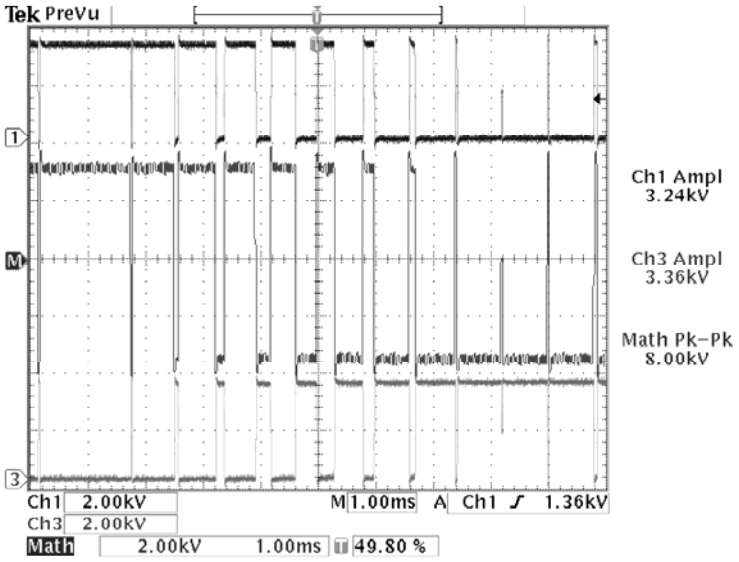


Figure 3.10: Zoomed in capture of the PWM output, showing each channel for the two high voltage probes used in capturing the bipolar PWM signal

The PWM voltage waveform was then analyzed and Figure 3.11 shows the Fourier spectrum of the captured signal. The Fourier spectrum show the numerous high frequency components clustered around multiples of the switching frequency (1.25 kHz) as well as the low frequency fundamental component. In reality the insulation system of an inverter fed induction motor is exposed to a similar waveform. By testing with unipolar square wave pulses to recreate the stresses that insulation is exposed to, the significant heating contribution of the fundamental is not being considered. By using a PWM waveform, the insulation can be exposed to the effects of both the fundamental component as well as the harmonics.

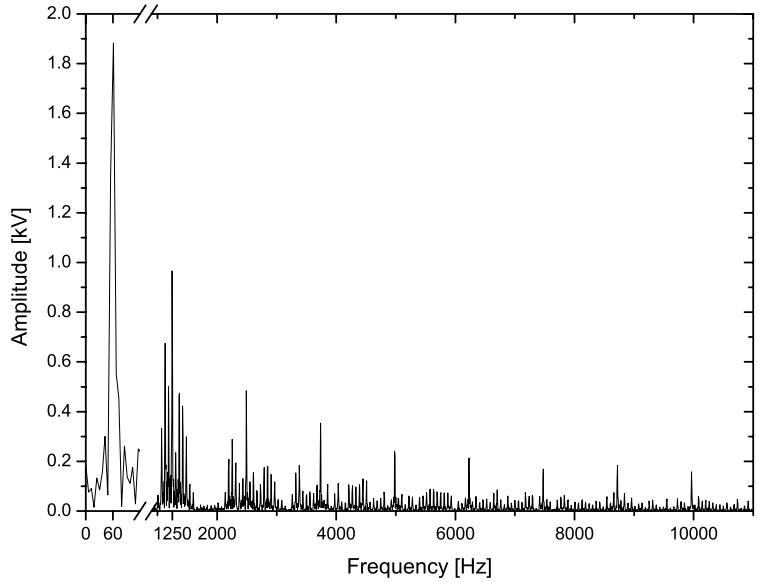


Figure 3.11: Fourier spectrum of captured signal shown in Figure 3.9

To determine whether the bipolar pulse modulator would be able to be used in testing a full coil, a short test was run with a coil connected at the output.

3.5 Modulator Limitations

3.5.1 Capacitance Limitations

To attempt to determine the maximum load capacitance of the test object that could be connected to the output of the pulse modulator, a variety of capacitances were tested. It was initially hoped that the final modulator would be capable of testing full coils. To determine whether this would be possible, a 4.16kV coil was connected to the output. One connection was made to the steel plate which would simulate the stator core and the other connection was to the first turn of the coil. Then the system was energized and the DC-link voltage was slowly increased. Because the currents drawn by the load

were so high, the maximum DC-link voltage which could be applied was around 400V. The voltage and current waveforms in the coil are shown in Figure 3.12.

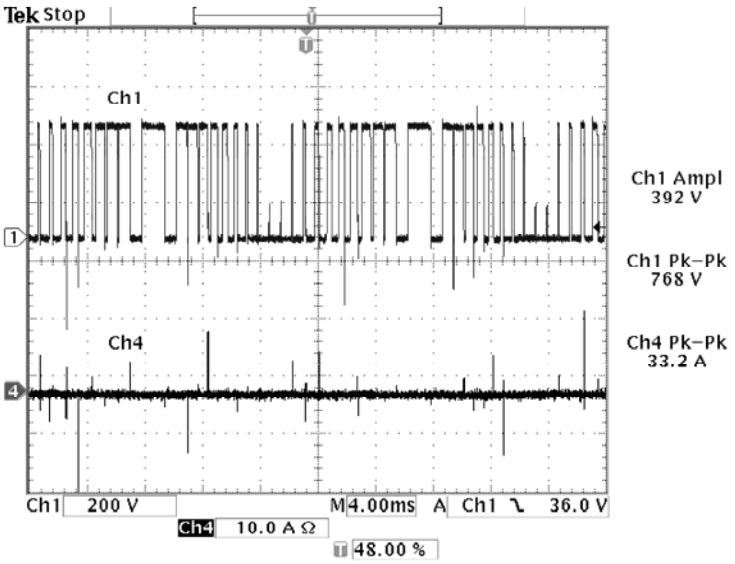


Figure 3.12: Captured output voltage (CH1) and current (CH4) with a 4.16kV coil connected at the output

The very large irregular high currents that were induced were assumed to be due to the very large inductance of the coil. In an attempt to rectify this problem all the turns within the coil were shorted together. This reduced the current that was drawn by the load and allowed the DC-link voltage to be increased up to around 600V, as shown in Figure 3.13. In this figure the current waveform shows that the capacitance of the coil is not the dominant component. This is apparent from the fact that there is only current when there is a transition in the voltage. This is because the current in the capacitor is dependent on dV/dt. When the voltage is constant such as during a longer pulse, the current through the load becomes zero because $dV/dt \approx 0$.

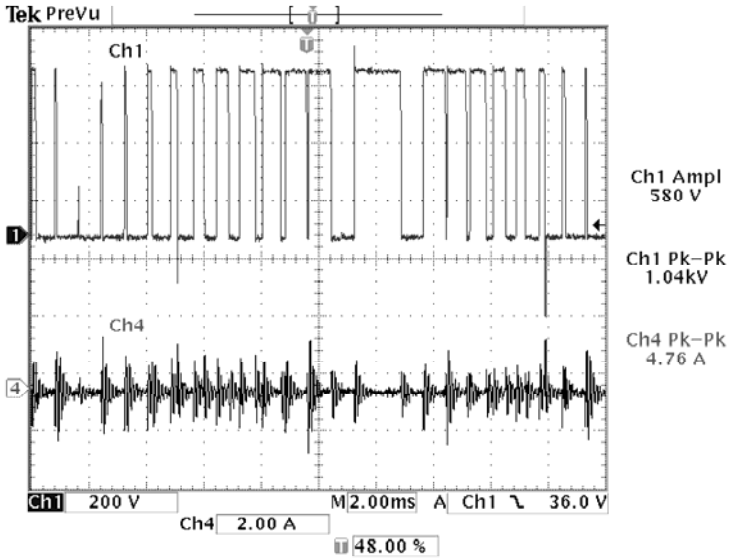


Figure 3.13: Captured output voltage (CH1) and current (CH4) with a 4.16kV coil connected at the output with all its internal turns shorted together

3.5.2 Thermal Limitations

The current waveform in Figure 3.13 showed that during the testing of insulation samples, most of the current that flows in the modulator is during the voltage transitions, which is when the IGBT switches are turning on and off. There is very little heating effect when the switch is either fully turned on or off. During the initial design and construction of the modulator, it was assumed that since the average currents in each switch were so low, there would be very little heating of the device. As a result it was decided to mount all the devices on two large aluminum bars; one bar for each leg of the inverter. This way the connection between consecutive switches could be made as short as possible reducing the inductance in the circuit. As well because the TO-247 case is not completely isolated, an isolation pad must be inserted between the case and the heat sink reducing the thermal performance of the heat sink. Based on the maximum possible DC-link input, which is 6000V, and the isolation pad having an isolation voltage of 4000V, two pads were used for mounting each switch. This further reduces

the thermal performance of the heat sink and is required for the modulator to safely operate. During turn-on it is assumed that the capacitive currents dominant in the losses and the switching losses will be neglected in the calculations which follow. During turn-on and turn-off it is assumed that the collector-emitter voltage ramps up/down in a linear fashion during the transition period,

$$V_c = \frac{Vt}{T_r} \quad 0 \le t \le T_r \tag{15}$$

as well the current through the capacitive load is defined by (16).

$$i_c = C\frac{dV_c}{dt} \tag{16}$$

As the voltage across the load ramps up the collector emitter voltage across the IGBTs ramps down,

$$v_{ce} = \frac{V(T_r - t)}{nT_r} \quad 0 \le t \le T_r \tag{17}$$

Using (15) and (16) the power dissipated in each device can be calculated.

$$P = i_c v_{ce} = \frac{CV^2(T_r - t)}{nT_r{}^2} \quad 0 \le t \le T_r \tag{18}$$

Based on (18) the peak power dissipated in the switches occurs at t=0s.

$$\hat{P} = \frac{CV^2}{nT_r} \tag{19}$$

Using (19) and assuming the maximum junction temperature cannot exceed 150°C (T_{jmax}), otherwise the switching device will be damaged [60] a relation between the peak power dissipated and the case temperature can be written using the transient thermal impedance.

$$\hat{P} = \frac{T_{j\max} - T_c}{Z} \tag{20}$$

The transient thermal impedance can be approximated by (21), where δ is the duty cycle, which is the turn-on time of the switch over the period [61].

$$Z \cong R_{jc}\delta \tag{21}$$

$$\delta = \frac{T_r}{T} \tag{22}$$

Combining (19), (20), (21), and (22) a relation is obtained relating the capacitive load with the DC-link voltage and the switching frequency.

$$C = \frac{n(T_{j\max} - T_{case})}{R_{jc}V^2 f} \tag{23}$$

As was stated previously, each switching device is mounted on 2 isolation pads and then the heat sink. Because the case temperature does not fluctuate like the junction temperature, the steady state thermal resistance values can be used in the following calculations. The thermal impedance of the 2 isolation pads and the heat sink are calculated in (24).

$$R_{ca} \approx 2R_{c-pad} + R_{HS-amb} = 2 \times 4 + 3 = 11 \tag{24}$$

Integrating (18) gives the average power dissipated in the device per cycle.

$$\overline{P} = \frac{CV^2 f}{2n} \tag{25}$$

Using the average power dissipated in the device, a relation can be written between the ambient temperature and the case temperature.

$$\overline{P} = \frac{T_c - T_a}{R_{ca}} \tag{26}$$

Combining (23), (25), and (26) gives an equation which can be used to determine the maximum capacitive load that can be connected at the output based on the operating voltage and frequency.

$$C = \frac{2n}{fV^2 R_{ca}} \frac{(T_{junc-\max} - T_{amb})}{(1 + \frac{R_{jc}}{R_{ca}})} \tag{27}$$

Plotting equation (27) for a variety of frequencies and DC-link voltages provides a series of maximum operating conditions. This series of plots is shown in Figure 3.14.

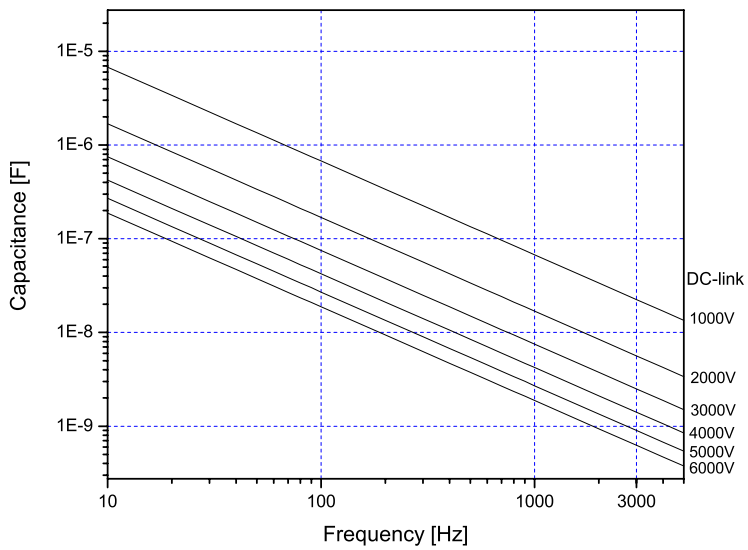


Figure 3.14: Maximum capacitance for a variety of operating conditions to maintain the maximum junction temperature of the IGBTs at or below 150°C

Subsequent operation of the modulator for long periods of time showed that there was significant temperature increases. Using the graph in Figure 3.14, at a switching frequency of 1250Hz, and a DC-link voltage of 4000V the maximum capacitive load possible is around 80nF. In reality the maximum capacitance will be less than this value because the above calculations have neglected the conduction losses which are due to the resistor connected in parallel with the capacitive load as well as the switching losses of the IGBT.

3.6 Conclusion

The chapter presented and discussed the performance of a number of subsystems within the modulator. The performance of the controller was found to be adequate for the application selected. The only major drawback was the high degree of sensitivity that the controller exhibited to EMI. This problem is attributed to the circuit board used to mount the microcontroller. As well, the three potential output waveforms (unipolar square wave, bipolar square wave, and bipolar sinusoidal PWM) were discussed as well as their potential applications. Finally, the major limitations of the designed modulator were presented.

Chapter 4
Applications

4.1 Introduction

As discussed previously the majority of studies conducted with regards to motor insulation systems utilize unipolar pulses or high frequency AC as the test waveforms. In reality the motor insulation is exposed to a much more complex voltage waveform. To gauge whether the current testing methodologies are adequate, the ageing effects of these conventional test waveforms must be compared with the effects of using an actual PWM waveform. Using the newly constructed modulator, an assortment of tests were performed on a variety of insulation samples. The results of these tests are then compared with the test results using conventional test waveforms.

4.2 Strand Insulation Test

The strand insulation in a motor coil consists of an enamel coating on the surface of the magnet wire. This enamel coating consists of a polyimide resin, which may contain fillers depending on the manufacturer and application of the wire. Most enamel coatings used in magnet wire applications were designed for operation under 60Hz AC conditions [62] and as a result these coatings are often unable to handle the transient pulse conditions found in PWM waveforms. Under 60Hz AC steady state operation, the potential throughout the coil is uniform which means there will be no nonlinear voltage distribution between turns. As a result there are no high electric fields created within the enamel coating. Under pulse however, a nonlinear voltage distribution has been proven [63] to exist between turns. This potential difference between turns will create an electric field inside this enamel coating, which can cause degradation of the insulation. To test these coatings several samples were

made using the geometry shown in Figure 4.1. Two pieces of magnet wire were placed against each other inside a clamp system. Then voltage is applied between the wires, to age the enamel insulation on the wires.

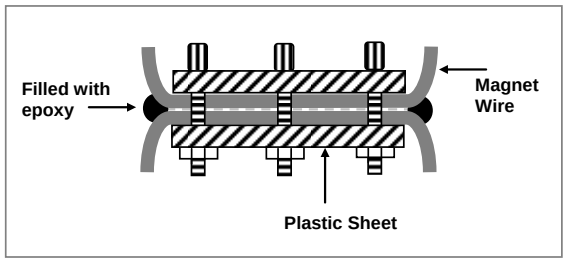


Figure 4.1: Geometry of magnet wire samples that were tested [62].

Several different ageing tests were performed. Depending on the number of layers present in the enamel insulation and the DC breakdown voltage of each type of wire, an appropriate ageing voltage level was determined. First a number of samples were aged at their specific voltage level and the time to failure was recorded. Other samples were aged at the same voltage but for only one hour; then, the affected areas were observed using a scanning electron microscope (SEM). Next the un-aged samples were compared with their aged counterpart to observe the changes that occur to the surface of the sample during ageing under a PWM waveform.

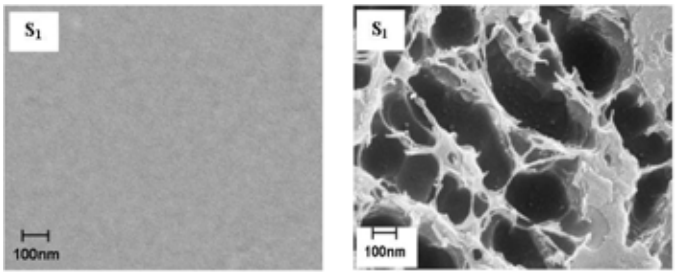


Figure 4.2: SEM photo of the surface of un-aged (a) and aged (b) surface of a commercial magnet wire sample with only a polyimide coating

Figure 4.2 shows extensive damage to the surface of the polyimide coating under PWM ageing. The polyimide, which is an organic compound, has been almost completely eaten away due to the partial discharge (PD) activity. To correct this problem, manufacturers have begun to use inorganic fillers, with high PD resistance, in their polyimide compounds, so as to try and reduce the effects PD has on the polyimide insulation. To test this, two commercial wires with improved PD resistance were also aged. The results of these tests are shown in Figure 4.3 and Figure 4.4.

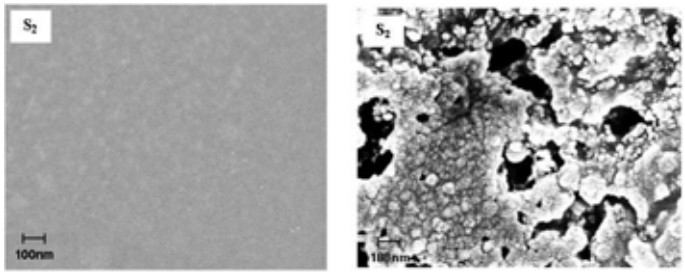


Figure 4.3: SEM photo of the surface of un-aged (a) and aged (b) surface of a commercial magnet wire sample with polyimide+THEIC coating

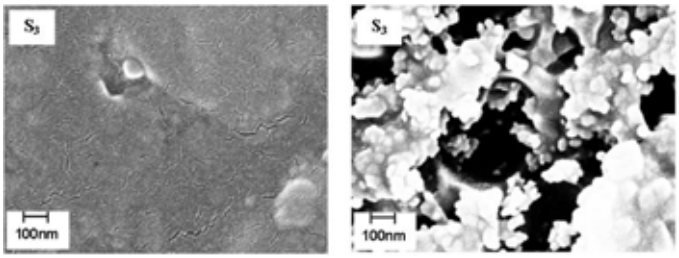


Figure 4.4: SEM photo of the surface of un-aged (a) and aged (b) surface of a commercial magnet wire sample with Alumina filler

The samples shown in Figure 4.3 and Figure 4.4 show increased resistance to PD activity. In both figures the polyimide has been eaten away exposing the inorganic filler, which due to its high PD

resistance is not affected. To contrast the performance of these corona resistant wires, three other filler materials were tested using prepared samples for other studies [62]. The fillers tested were fumed silica (S4), titanium oxide (S5), and alumina (S6). The results of the ageing test are shown in Figure 4.5.

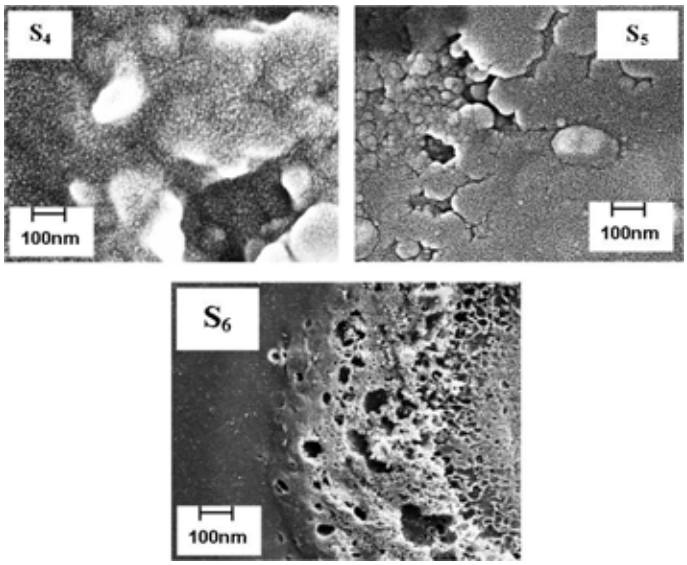


Figure 4.5: Aged samples of the laboratory developed enamel coatings [62]

The use of nano-fillers under PWM aging seems to greatly improve the performance of the polyimide coating. There is much less surface degradation present in Figure 4.5 compared to Figure 4.3 and Figure 4.4. Further discussion on the degradation mechanisms involved in the strand insulation can be found in Appendix H.

The strand insulation tests have shown that the current materials used show a great amount of degradation under PWM waveforms. The performance of these coatings can be improved through the use of nano-fillers.

4.3 Groundwall Insulation Test

For groundwall insulation testing miniature samples representing a stator coil section were used. These samples replicated the construction of the insulation system found on an actual form wound coil but their physical size is much smaller, decreasing the capacitance, and making them suitable to test with the lab built pulse modulator. These samples are prepared by taking several pieces of uncoated magnet wire and first wrapping them with mica tape, which is shown in Figure 4.6(c). Next these bar samples are vacuum dried in an oven for 6-8 hours, after which they are immersed in resin in a pressurized container. The pressurized container is used so as to force resin into all the voids of the insulation making it much more difficult for PD activity to occur. These samples, after the VPI treatment, are shown in Figure 4.6(b). After the samples have fully cured, some semi-conductive graphite paint (also called conductive paint) is applied to the central section of the bar. At the edge of the black paint, some stress grading material is applied, shown in Figure 4.6(a). For high frequency and pulse aging, this stress grading is not really required. A more detailed description of the preparation process can be found in [27,64].

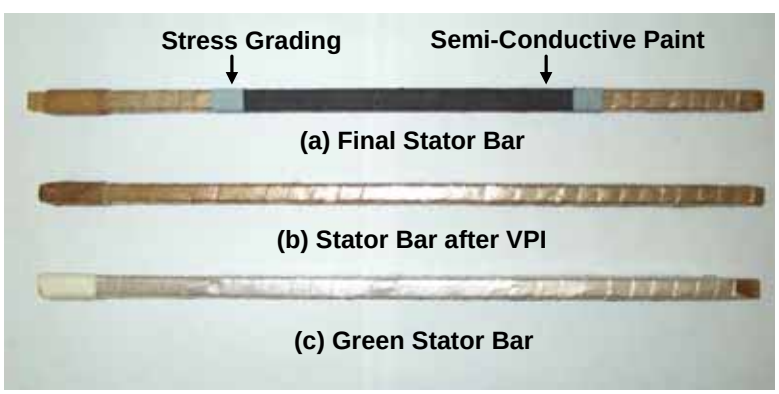


Figure 4.6: Preparation of the groundwall insulation samples [64]

After the paint and stress grading material have cured, a piece of conductive foil tape is placed in the middle of the area painted with the black paint. This piece of foil will represent the grounded stator core of an induction motor. A comparison between the smaller samples and an actual stator core is shown in Figure 4.7.

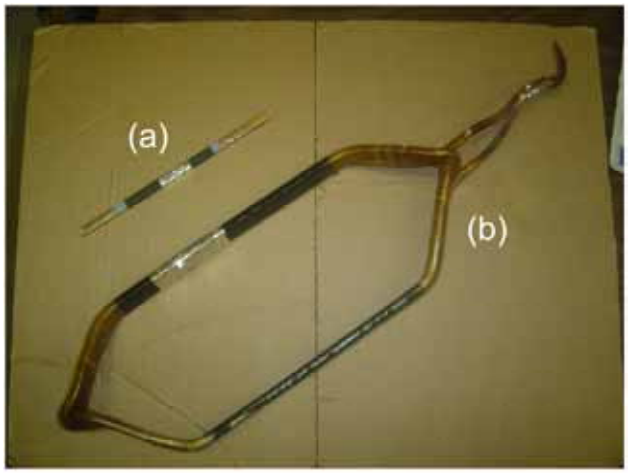


Figure 4.7: Comparison between the smaller groundwall sample (a) and an actual MV motor coil (b)

To test the insulation system, voltage is applied between the conductive tape and the magnet wire conductors inside the sample. These tests were used to observe the failure mechanism as well as study the breakdown strength of the groundwall insulation under different test waveforms. The breakdown voltage was determined by slowly increasing the voltage applied to the sample until failure, which was indicated by a short circuit and the voltage collapsing, was observed. A number of samples were tested using a variety of waveforms to produce a valid data set. The observed breakdown strength comparing the different waveforms is shown in Figure 4.8.

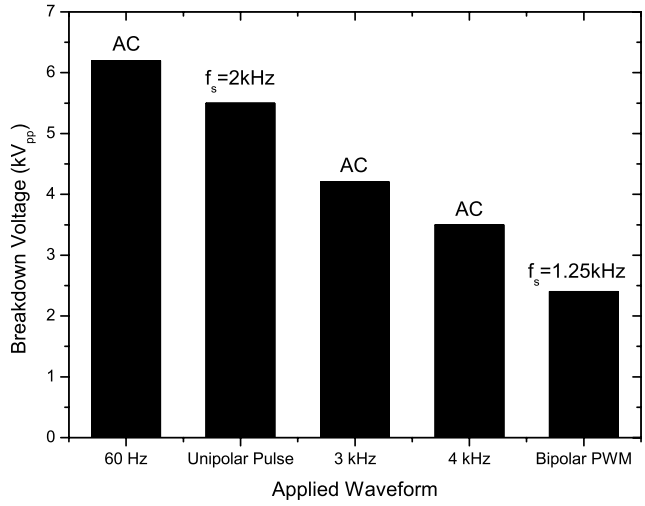


Figure 4.8: Observed breakdown strength of groundwall insulation samples [64]

Figure 4.8 demonstrates that as the fundamental/switching frequency of the AC waveform increases, the breakdown strength of the sample decreases. This holds true for both sinusoidal and unipolar waveforms. The data set for the bipolar PWM waveform indicates that the combined effect of the fundamental frequency coupled with the harmonics are much more stressful on the insulation system than either high frequency AC or unipolar pulses. This would indicate that current methods used for testing insulation systems may not be able to adequately represent the effects that a MV VSC produces.

In most of the samples, the insulation failed in one of two general areas. Either the failure occurred right at the edge of the foil tape, which on an actual coil would be the slot exit, or in the area covered by the semi-conductive paint. In the first failure area, shown in Figure 4.9, the failure occurred at the edge of the foil tape because of a concentration of the electric field at that point. The purpose of the semi-conductive paint, as discussed earlier, is to keep the surface of the coil at a ground potential

identical to that of the stator core. This minimizes the electric field concentration, possible PD, and potential surface degradation. Under 60Hz AC operation, this paint functions as it is designed and the electric field concentration is moved away from the slot exit and into a stress grading area. Under pulse operation, it has been shown that the conductive paint is no longer able to stay at ground potential and the electric field actually concentrates right at the slot exit [26]. Experimental results showing this are briefly covered in Section 4.4. As a result of this field concentration, the insulation becomes much more susceptible to degradation and in extreme cases can rupture, which is shown in Figure 4.9.

Figure 4.9: Rupture in the groundwall insulation at the edge of the simulated slot exit under PWM ageing

This field concentration is verified from studying the thermal profile of the bar sample shown in Figure 4.10. The high field concentrations cause increased dielectric heating which is shown by the brighter areas in the thermal image.

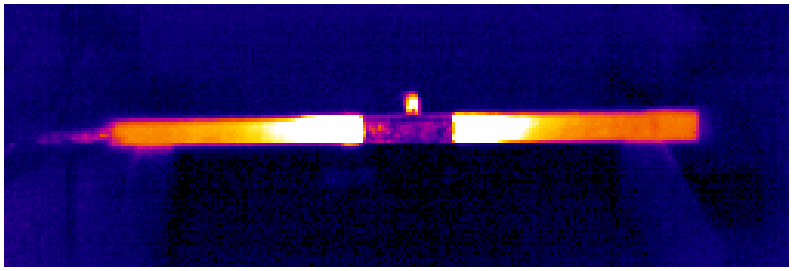
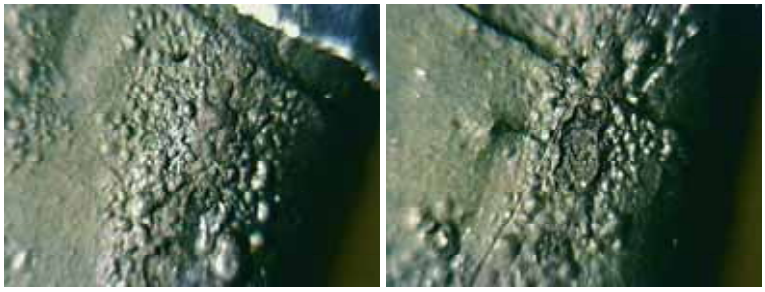


Figure 4.10: Infrared image of a groundwall insulation sample under pulse conditions

The second failure type is most likely due to voids existing within the groundwall insulation. These voids have a lower permittivity than the surrounding insulation causing a concentration of the electric field which eventually may lead to partial discharge. This PD can erode the insulation eventually creating a short between the conductive black paint and the magnet wire inside the sample; when this occurs a current flows between the rupture in the insulation, shown in Figure 4.11(b), and the foil tape. This creates a track, shown in Figure 4.11(a), on the black paint due to the high current being conducted on the surface of the sample.



(a) *(b)*

Figure 4.11: Surface damage on the graphite paint from the surface current (a) the rupture in the insulation due to a void (b)

4.4 Novel Stress Grading System Test

As discussed earlier, stress grading (SG) coatings are applied to coil ends and slot exits of electrical machines in order to both the high concentrations of the electric field that can occur without a SG coating [36], and the PD damage caused by the high concentrations of electric field. The stress grading system utilizes materials that have field dependent conductivities. As a result, as the field concentration increases, the conductivity increases causing the electric field to spread out more. Current stress grading systems have been designed to operate under power frequency conditions (50/60 Hz) and as a result, their performance rapidly degrades under pulse conditions, such as the case when the motor is fed by a PWM-VSC. This is demonstrated with a coil that was tested in Figure 4.12. Currently there are no electrostatic voltmeters capable of measuring the electric field under pulse conditions, so an alternate method will be used to determine field concentrations. Areas of high electric field concentration will show increased dielectric heating, and so a thermal image of the test object will indirectly show the areas of high field concentration.

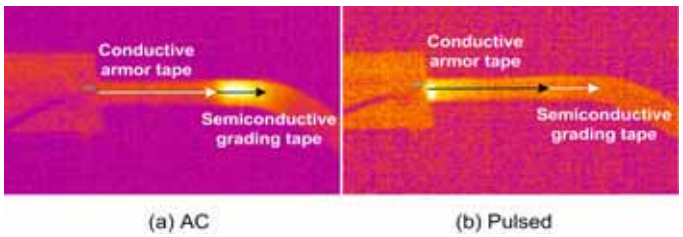


Figure 4.12: Thermal images of the stress grading system of a MV induction motor coil under both AC and pulse conditions [57]

When 60Hz AC is applied to the coil, the heating, shown in Figure 4.12(a) is concentrated in the stress grading area. This shows that the stress grading system is functioning normally. Figure 4.12(b) shows heating at the slot exit under pulse conditions meaning that the electric field concentration is also there. This indicates that the stress grading system is no longer effective. This means that under

PWM conditions the 60Hz component of the electric field will be graded by the stress grading while the high frequency components will remain at the slot exit.

To correct this problem a new SG coating was developed that would be able to function under sinusoidal PWM conditions. Using a special two layer system, the stress grading would grade the 60Hz and high frequency components of the electric field to different locations on the coil. The fundamental and high frequency components of the electric field are graded to two different locations to reduce the heating of the insulation compared with if both components had been graded to the same point. This will reduce the thermal stress on the insulation and so increase its operating life. To be able to test this SG system properly and see if the stress grading is actually able to grade both the fundamental as well the pulse electric fields, some sort of high voltage PWM source will be required source.

The SG samples were tested using a circular geometry because it produces an electric field in the sample that is very similar to that found at the slot exit. As well it allows for better control of the coating thickness and easy application. A more detailed description of the geometry and preparation process can be found in [57]. This new stress grading was tested separately, first under pulse conditions, shown in Figure 4.13(a), and then at 60 Hz, shown Figure 4.13(b).

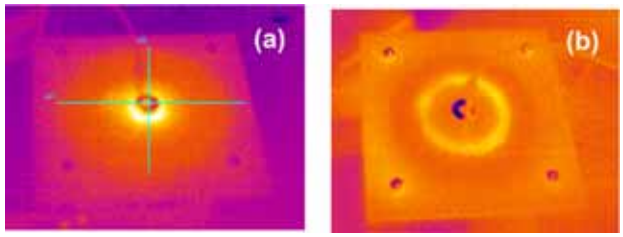


Figure 4.13: Thermal image of the new stress grading system in lab separately under: (a) pulse and (b) 60Hz AC [57]

In this stress grading system it is observed that under pulse the heat concentrates in the inside ring, showing that the electric field is concentrated there, while at 60 Hz the heat is observed in the outer region. Both these results are promising and show that this stress grading system is able to control the electric field for both 60Hz and pulse conditions. Next the system was tested to show whether the stress grading will function as designed when both conditions are present. To do this the specimen is tested using the lab built pulse modulator. Under PWM two hot spots are observed on the SG coating. Figure 4.14 demonstrates that the SG coating does in fact work as it should. It shows that the 60Hz continues to concentrate in the outer region while the inner region grades the pulse electric field. The verification of whether this design would actually work or not was only possible using the lab built PWM inverter.

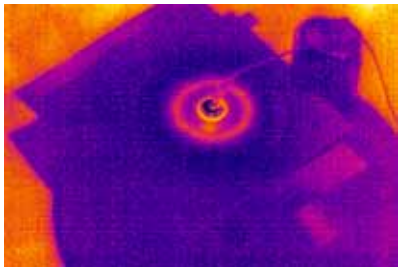


Figure 4.14: Thermal image of the new stress grading system with an actual sinusoidal PWM waveform to show that the system is able to grade both the 60Hz AC and pulse electric fields [57]

4.5 Conclusion

This section has covered the different insulation systems that were tested using this pulse generator. The preliminary results for test on groundwall, turn, and stress grading insulation systems have been covered. The majority of the results seem to indicate that testing with an actual bipolar pulse width modulated waveform may be more effective than simply using unipolar pulses. Further investigation contrasting the effects of unipolar pulses, bipolar square wave and bipolar PWM is required to

conclusively determine the total impact the PWM waveform has on the insulation systems in MV induction motors.

Chapter 5
Conclusions and Future Work

5.1 Conclusions

The literature survey conducted in Chapter 1 showed that the majority of work which studied the effects of solid state VSC's almost exclusively used either high frequency AC or unipolar pulses as the test waveforms. While both these waveforms are components of the actual waveform produced by a VSC, in reality the insulation in an induction motor is exposed to a voltage with a multitude of components. The Fourier spectrum of a basic 2-level PWM signal, shown in Figure 3.11, showed that the output contains both a low frequency fundamental harmonic component as well as numerous high frequency components. To solely use high frequency AC as a test waveform neglects the effects of that the high dV/dt of the converter pulses have on the insulation. This high dV/dt creates high currents as well as electric stresses within the insulation that can cause degradation and eventual failure. Using only unipolar pulses neglects the contribution of the fundamental component mainly in the form of heating, which is a thermal stress on the insulation.

The work discussed in this thesis has attempted to explore the use of sinusoidal PWM as a test waveform in insulation testing. Chapter 2 covered the design and construction of the pulse modulator capable of producing a sinusoidal PWM output. Chapter 3 discussed some of the associated problems and challenges in constructing the device, while Chapter 4 presented some of the preliminary test results using the modulator.

The construction of this modulator has demonstrated that it is possible to produce a voltage waveform similar to that produced by a MV VSC using readily available low voltage/low power components. As well due to the use of low power components the overall size of the device is much smaller than an actual drive, making the device easy to deploy and work with. Tests were

successfully performed on groundwall insulation, strand insulation, and stress grading systems. For groundwall insulation samples, a failure mechanism specific to inverter fed motors was documented and discussed. As well, the breakdown test results indicate that under sinusoidal PWM voltage the stress on the insulation system is greater than under unipolar pulse. Strand insulation test results showed that ageing under pulse is much more accelerated than under 60Hz AC. The results also showed that as the frequency of the waveform increased the aging process further accelerated. These results all indicate that using a PWM waveform in insulation testing may provide a better indication of the failure mechanisms and weaknesses in current insulation systems.

Using the modulator, a novel double layer stress grading system able to operate under PWM conditions was tested. To be able to validate and conclusively prove that this new design would work as specified a high voltage PWM source is required. This fact allows for the use of actual PWM waveforms to validate new insulation system designs without having an actual medium voltage drive.

One of the main weaknesses of the modulator is the controller used, because it is extremely susceptible to noise. As a result samples that produce excessive amounts of PD or corona are difficult to test, because they interfere with the operation of the controller forcing it to reset. For short term ageing tests of only 2 or 3 hours, the device has performed quite well without problems. For longer duration tests, better thermal management of the heat produced is required; as well, some type of feedback must be installed to automatically turn off the device when the test object fails.

With smaller capacitance test objects, the modulator is capable of producing pulses with rise times around 500ns, the fall time is heavily influenced by the capacitance and is usually around 2-5 µs. The modulator has been successfully operated at output voltages up to 8kVpp. Based on the IGBTs selected for use, this device should in theory be able to operate at voltages up to 12kVpp, but due to the problems with packaging, this voltage has not been attempted.

While the current modulator design is fully functional, as with any circuit design, improvements can always be made. Suggested improvements to this design are discussed Section 5.2.

5.2 Suggestions for Future Work

Currently, the only protection scheme implemented for the switching devices in the modulator is the current limiter which comes built-in the high voltage DC source. The effectiveness of this limiter is negated when external DC-link capacitors are connected in parallel with the HV-DC source, due to the fact that the limiter only controls the output current of the DC source and has no effect on the discharge rate of the capacitors. Due to the nature of the loads connected to the device, which was discussed earlier, to improve the durability of the modulator some form of protection for the switches is required. To protect against surge currents which can potentially damage the switches, the use of metal oxide varistors (MOVs) or a high voltage fuse with a rating of 15A should be investigated. An added benefit of using a MOV over a fuse is that during a surge or impulse, the varistor also clamps the voltage across its terminals to a maximum level that can be selected through proper design. To protect against overvoltages, the use of spark gaps connected in parallel with the switches could be studied.

Another area of improvement would be the packaging of this device. At lower operating voltages (below 2 kV_{pp}) the packing and shielding is a non issue. As the voltage increases towards the maximum operating value, the current correspondingly increases and so does the EMI. This EMI interferes with the operation of the controller and causes it to periodically reset. To correct this problem better packaging, with improved shielding of the switches and controller is required.

An improvement related to the previously discussed issue is the design and use of a proper controller board; which, would be manufactured on a 4-layer PCB. Using a 4-layer design for the board would allow for a ground plane, which would improve the noise resiliency of the controller.

The PCB which was designed and discussed previously, in Section 2.3.3, can be improved in a number of ways:

- Mounting the actual switches and any required snubbers directly on the PCB instead of the external heat sink;
- Repositioning the optocouplers on the PCB to eliminate the use of jumpers;
- Moving the op-amp buffer stage to the controller board, potentially reducing the size of the driver board;
- Installing a Hall effect current sensor which would monitor the current supplied to the test object. When the test object fails then the controller would be able to automatically shut the modulator off.
- Investigating the use of commercial implementations of isolated DC-DC converters for powering the individual drive circuits. If a suitable part can be found this would eliminate the transformer, diode bridge, and 7815 regulator currently used in the design. This would result in a significant reduction in the size of the device.

To increase the operating voltage of the modulator while using the same number of switches this device could be converted from a 2-level inverter to a 3-level diode clamped inverter. This would require the use of a number of high voltage diodes as well as significant modification of the firmware. This modification would make the output waveform of the modulator more closely resemble the output produced by a MV VSC. The main limitation of this idea is that it requires two high voltage DC sources to implement.

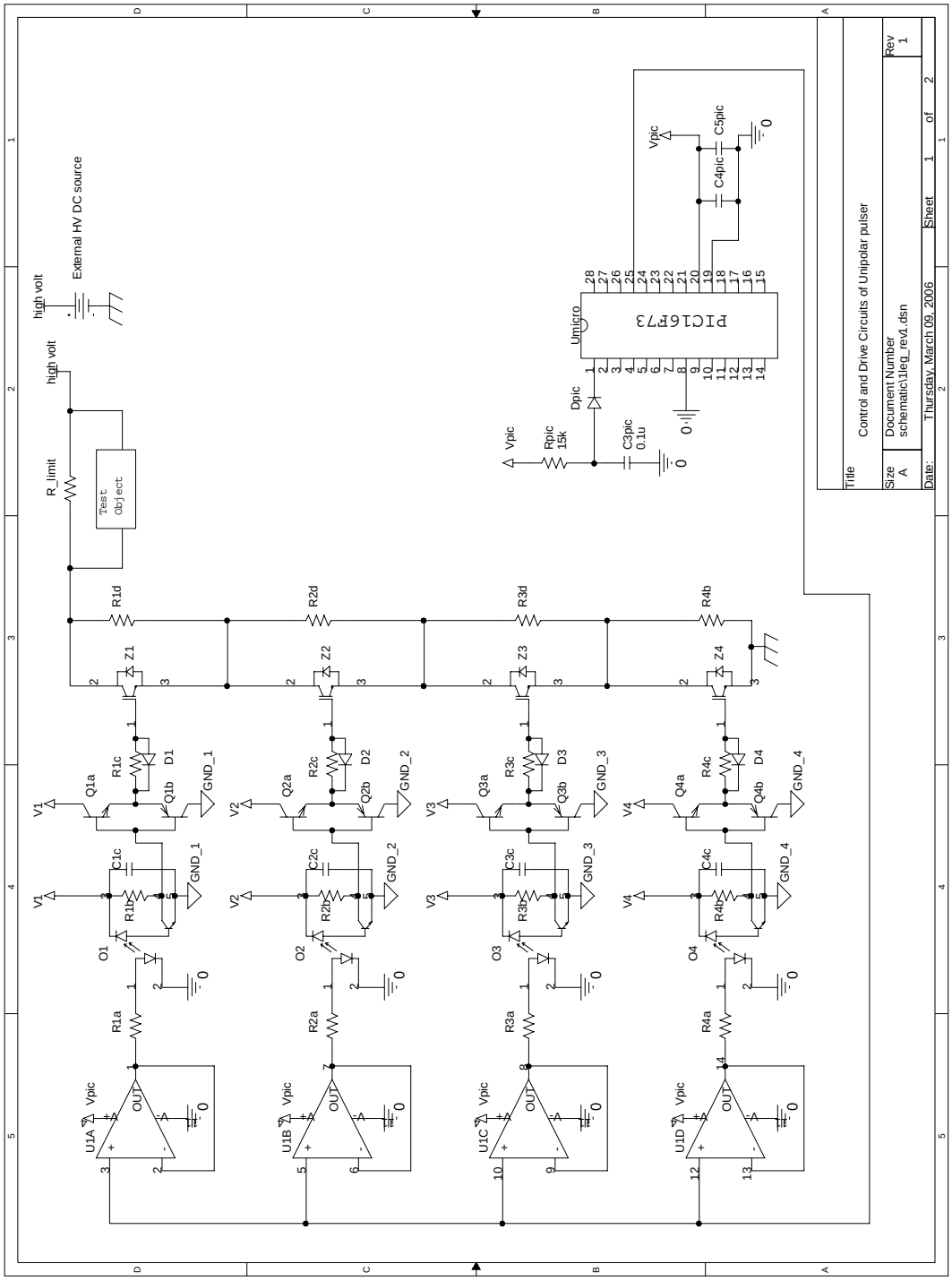
This modulator has been successfully used to test a variety of insulation samples. The results of these tests have shown that the device does have a number of limitations. One of these limitations was clearly demonstrated during the testing of the groundwall insulation of a full 2.2kV induction motor coil. Current spikes with magnitudes in excess of 20A were recorded by the current probe during switching of the IGBTs. As a result of these high currents the maximum voltage that could be applied during the test was greatly limited. As well, because the capacitance was so large the resistor

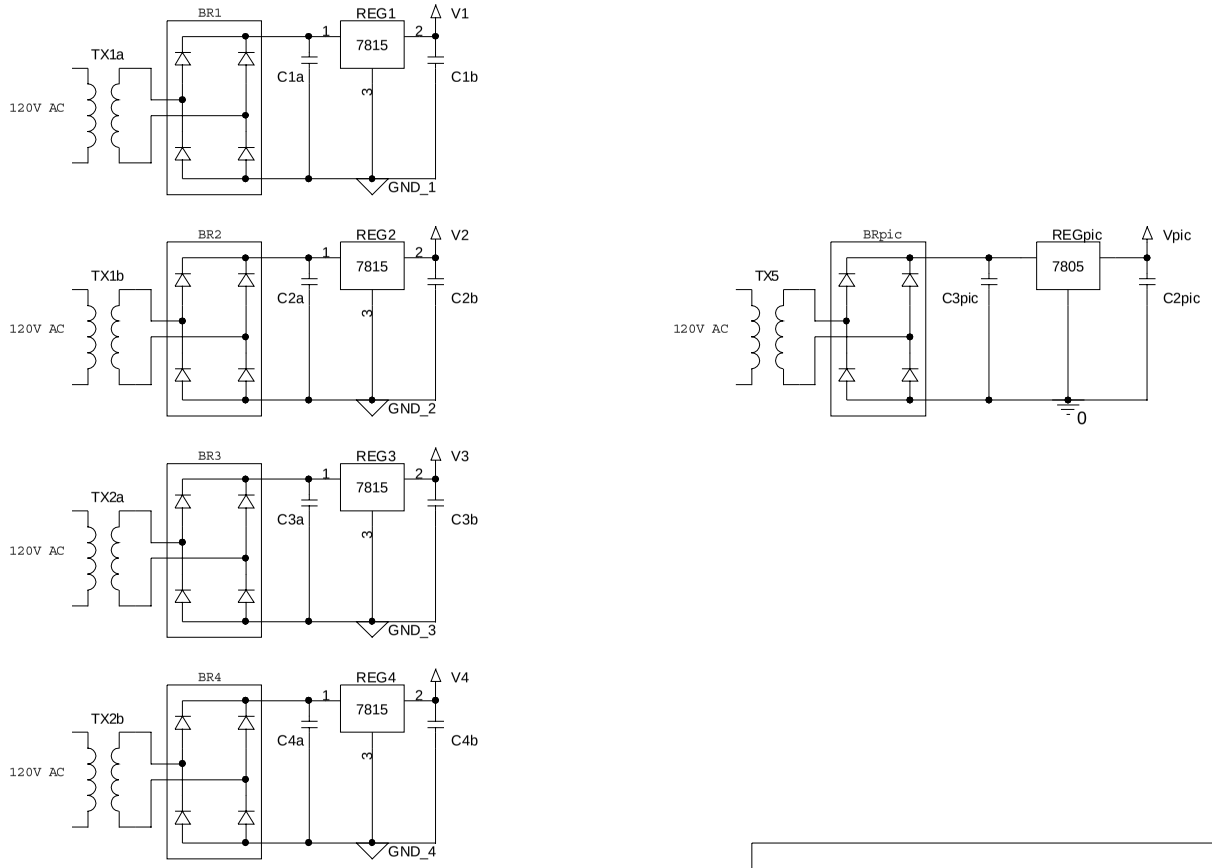
connected in parallel to the coil was not able to discharge the load capacitance fully during turn off, creating some distortion in the output waveform. This could be corrected by using a resistor with a lower impedance, but this is constrained by the very limited current the external HV-DC source is able to supply along with the very small DC-link capacitors used.

To be able to conduct tests on a full coil (larger capacitive load), the current design for the modulator would have to be scaled up. This would require a larger high voltage DC source with higher output current rating as well as larger DC link capacitors. With these alterations a smaller resistor can be connected in parallel to the test object allowing faster discharge, thus maintaining the square pulse shape with larger capacitive loads. The reduction of the shunt resistance and use of larger capacitive loads will cause the current spikes during turn on to be higher; as a result, IGBTs with higher pulsed current ratings may have to be utilized.

Appendix A

Unipolar Pulser Schematic





Title	Power Circuits for Unipolar Pulser	
Size A	Document Number schematic\1leg_rev1.dsn	Rev 1
Date: Thursday, March 09, 2006	Sheet 2 of 2	

Appendix B

Unipolar Pulser Bill of Materials

Item	Quantity	Reference	Part	Description
1	5	C1a,C2a,C3pic,C3a,C4a	1000u	Electrolytic Capacitor
2	6	C1b,C2b,C3b,C4b,C2pic,C4pic	10u	Electrolytic Capacitor
3	6	C1c,C2c,C3c,C4c,C3pic,C5pic	0.1u	Ceramic Capacitor
4	5	D1,D2,D3,D4,,Dpic	D1N4148	Fast Diode
5	4	O1,O2,O3,O4	HCNW4504	High Speed Optocoupler
6	4	Q1a,Q2a,Q3a,Q4a	MPS8099	NPN transistor
7	4	Q1b,Q2b,Q3b,Q4b	MPS8599	PNP transistor
8	1	REGpic	uA7805C	5V 1.5A Linear Regulator
9	4	REG1,REG2,REG3,REG4	uA7815	15V 1A Linear Regulator
10	1	R_limit	8.3k	6 parallel 50k 100W resistor
11	1	Rpic	15k	1/4 Watt Resistor
12	4	R1a,R2a,R3a,R4a	1k	1/4 Watt Resistor
13	4	R1b,R2b,R3b,R4b	20k	1/4 Watt Resistor
14	4	R1c,R2c,R3c,R4c	33	1/4 Watt Resistor
15	4	R1d,R2d,R3d,R4d	2M	1 Watt Resistor
16	1	Umicro	PIC16F73	PIC microcontroller
17	1	U1	TLC2274ACN	High speed 4 Op-amp IC
18	4	Z1,Z2,Z3,Z4	IXBT16N170	1700V discrete IGBT switch
19	5	BR1,BR2,BR3,BR4,Brpic	DB102	Rectifier bridge
20	3	TX1,TX2,TXpic	229A34	Low profile PCB transformer
21	1	CR	200ECSD	20 MHz oschillator

Appendix C

Firmware for Unipolar Pulser

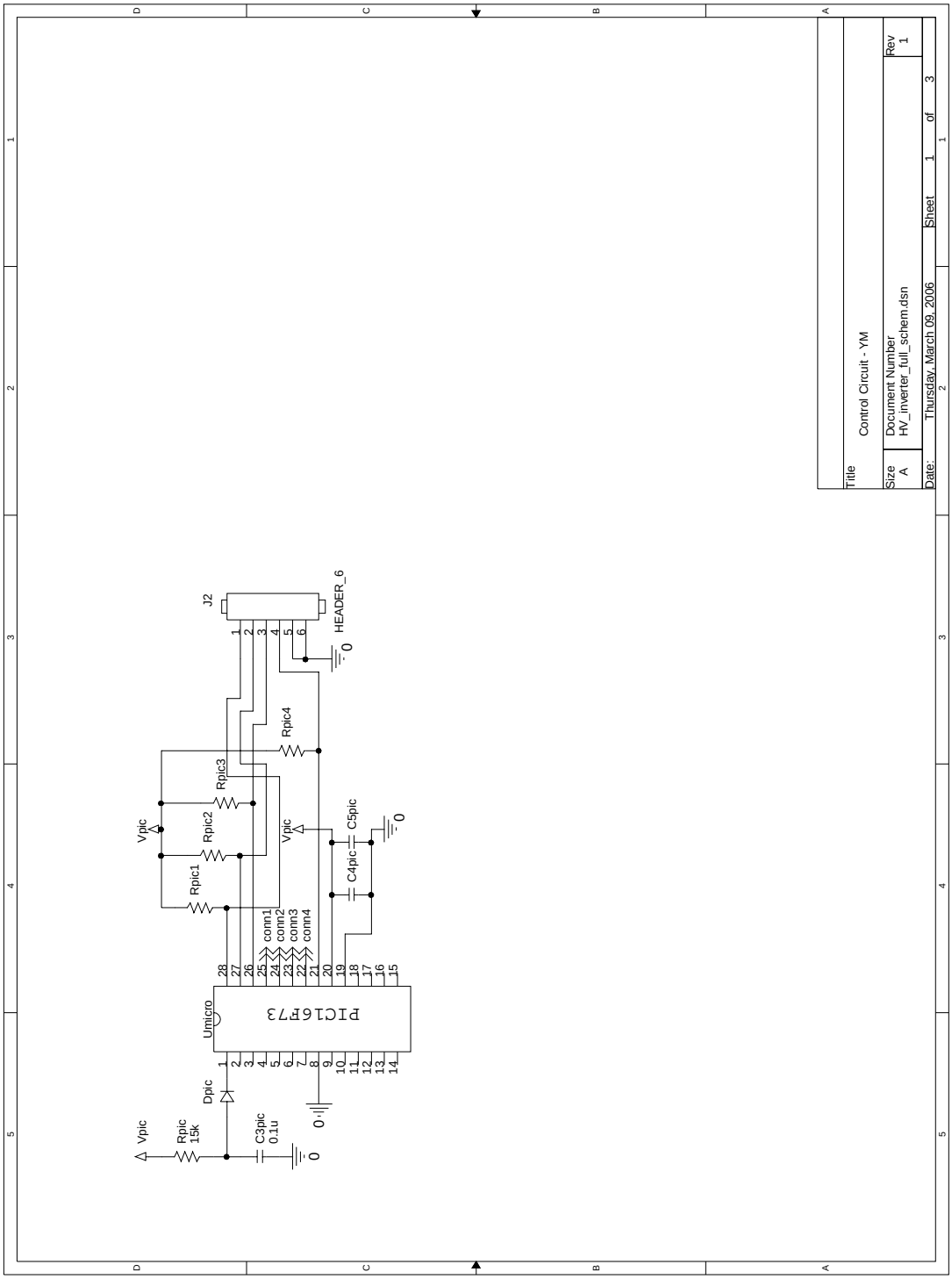
```
      title "PIC16F73 counting program"
      list P=PIC16F73 ;p=16f73,f=inhx32
      #include <p16f73.inc>  ; This “header file” contains all
                                          ; the PIC16F73 special function
                                          ; register names and addresses.
                                          ; This file is located in the
same
                                          ; directory as MPASMWIN.EXE.

; variable declaration
;--------------------
DVAR  equ 0x21
DVAR2 equ 0x22
duty  equ 0x23
w_temp0 equ 0x70  ; temp store for W in banks 0 & 2
w_temp1 equ 0xf0  ; banks 1 & 3
st_temp equ 0x72 ; temp store for STATUS

; constant declaration
;--------------------
Dmax equ 0xf0
Dmin equ 0x01

      org 00h     ;place pointer at reset vector
      goto Start

;*****************************************
; Timer 2 ISR to generate 1 ms period (1KHZ)
;*****************************************
      org 0x04

      movwf FSR;w_temp0       ; save w
      swapf STATUS, w    ; swap STATUS
      bcf         STATUS, RP0  ; Bank 0
      movwf st_temp            ; sav STATUS

; T2 ISR main
onperiod
      bsf PORTB, 4
      movf TMR2, w      ; w = TMR2
      subwf duty,w    ; w = duty - TMR2
      btfsc STATUS, 0 ; if w>0, stay in the on period (borrow is active
low)
      goto onperiod
      bcf PORTB, 4
```

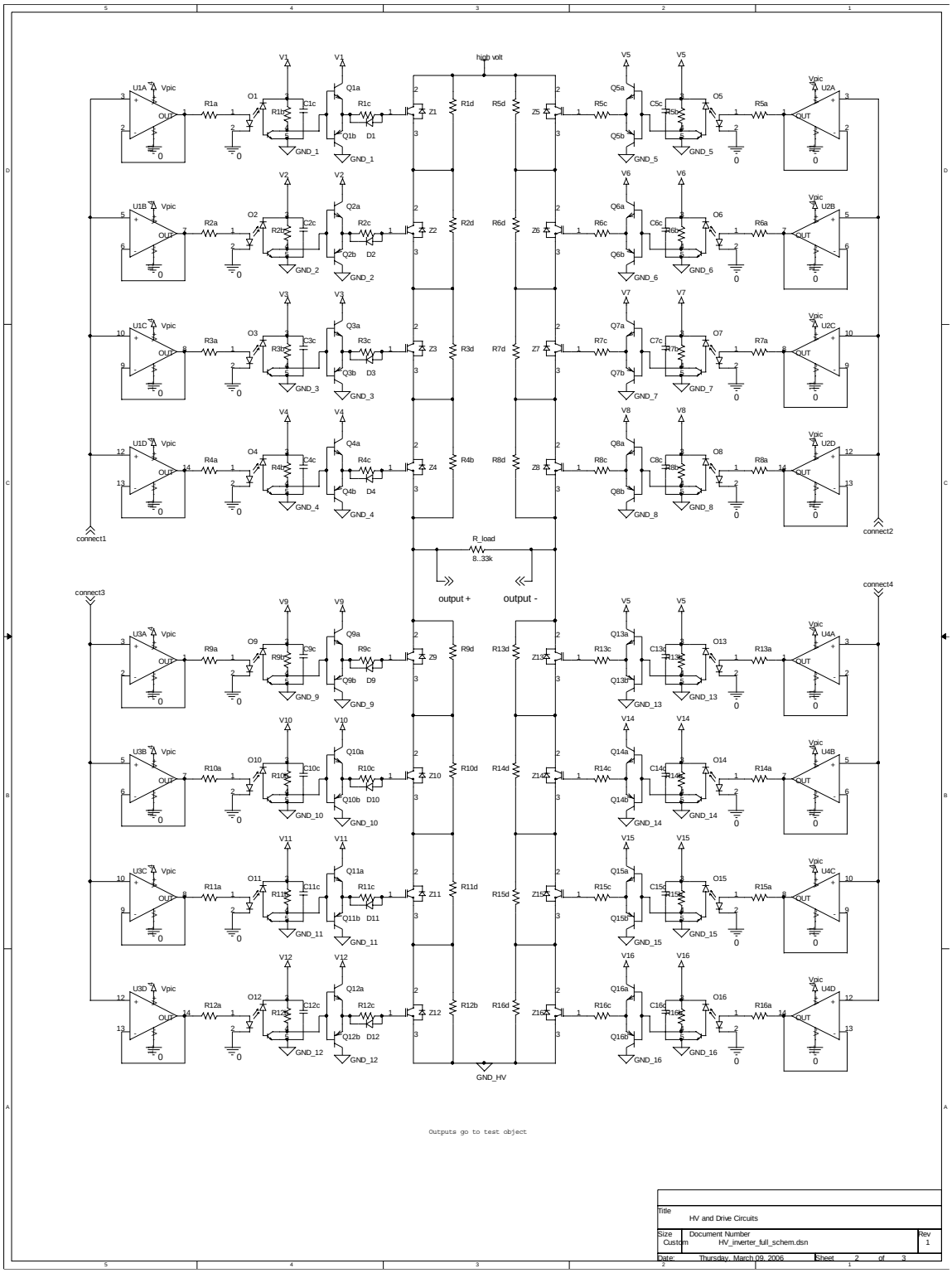
```
; POP
popout:
      clrf PIR1 ; clear int flags
      swapf st_temp, w ; swap status
      movwf STATUS ; restore status
      swapf FSR, f ; swap w
      swapf FSR, w ; restore w
      retfie
;*****************************************

      org 0x100
Start
; Initization
;-------------
      clrf STATUS ; Bank 0
      clrf INTCON ; disable interrupts
      clrf PIR1 ; clear flags

; Variable Initization
;----------------------
      movlw 0xf8;Dmin
      movwf duty ;initial duty cycle = 4/1000
;;    clrf flagD1

; I/O ports
;-----------
      clrf RCSTA ; disable serial port
      bsf STATUS, RP0 ; Bank 1
      movlw 0x00 ; RB4 and RB5 are outputs and the other pins are inputs
      movwf TRISB ;config PORTB as outputs
      clrf PORTB
      bcf STATUS, RP0   ; Bank 0
      bcf PORTB, 4

; T2 initialization for period generations
;----------------------------------------
      bsf STATUS,RP0 ; Bank 1
      movlw 0xfa ; 1/PR2=foc/4/250=20000Hz
      movwf PR2 ; Period of Timer 2
      bcf STATUS, RP0   ; Bank 0
      movlw 0x07
      movwf  T2CON ;prescale = 16, postscaler = 1, Enable T2; the T2 freq.
will be fsw=(1/PR2)/(postscale * prescale) = 1.25 KHZ

; Interrupt
;----------
      bsf STATUS,RP0 ; Bank 1
      movlw 0x02 ; T2
      movwf PIE1 ; unmask T2 and
      clrf  PIE2 ; disable other interrupts
      bcf STATUS, RP0 ; Bank 0

; Main program
```

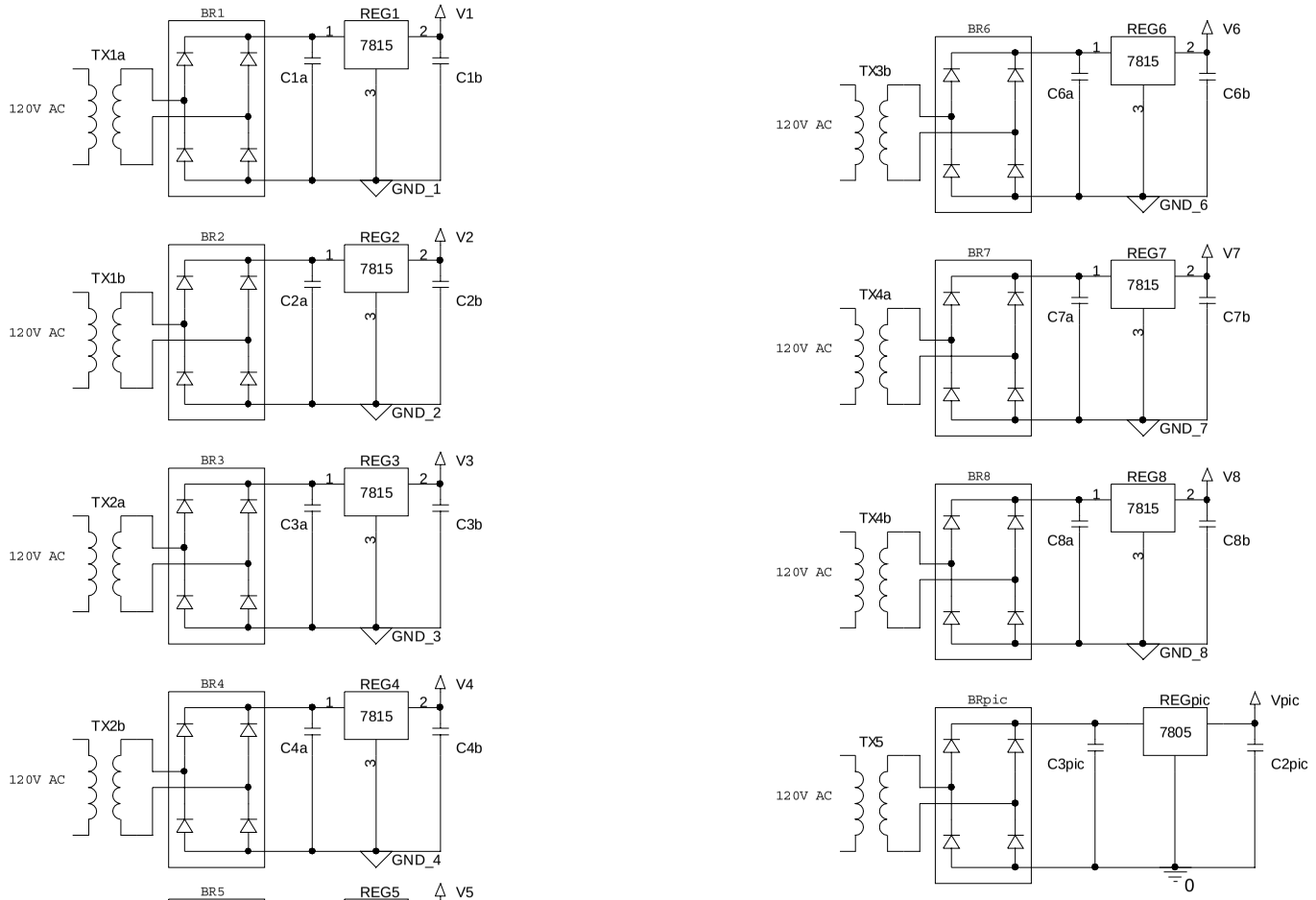
```
;-------------
loopin
      movlw 0xc0
      movwf INTCON ; enable interrupt

      goto loopin

      end
```

Appendix D

Bipolar Pulser Schematic




high volt
R_load
8..33k
output +
output -
connect1
connect2
connect3
connect4
GND_HV
Vpic
Outputs go to test object
Title
HV and Drive Circuits
Size
Custom
Document Number
HV_inverter_full_schem.dsn
Rev
1
Date:
Thursday, March 09, 2006
Sheet
2
of
3



Title	Power Suppy Circuits	
Size A	Document Number HV_inverter_full_schem.dsn	Rev 1
Date: Thursday, March 09, 2006	Sheet 3 of 3	

Appendix E

Bi-Polar Pulser Bill of Materials

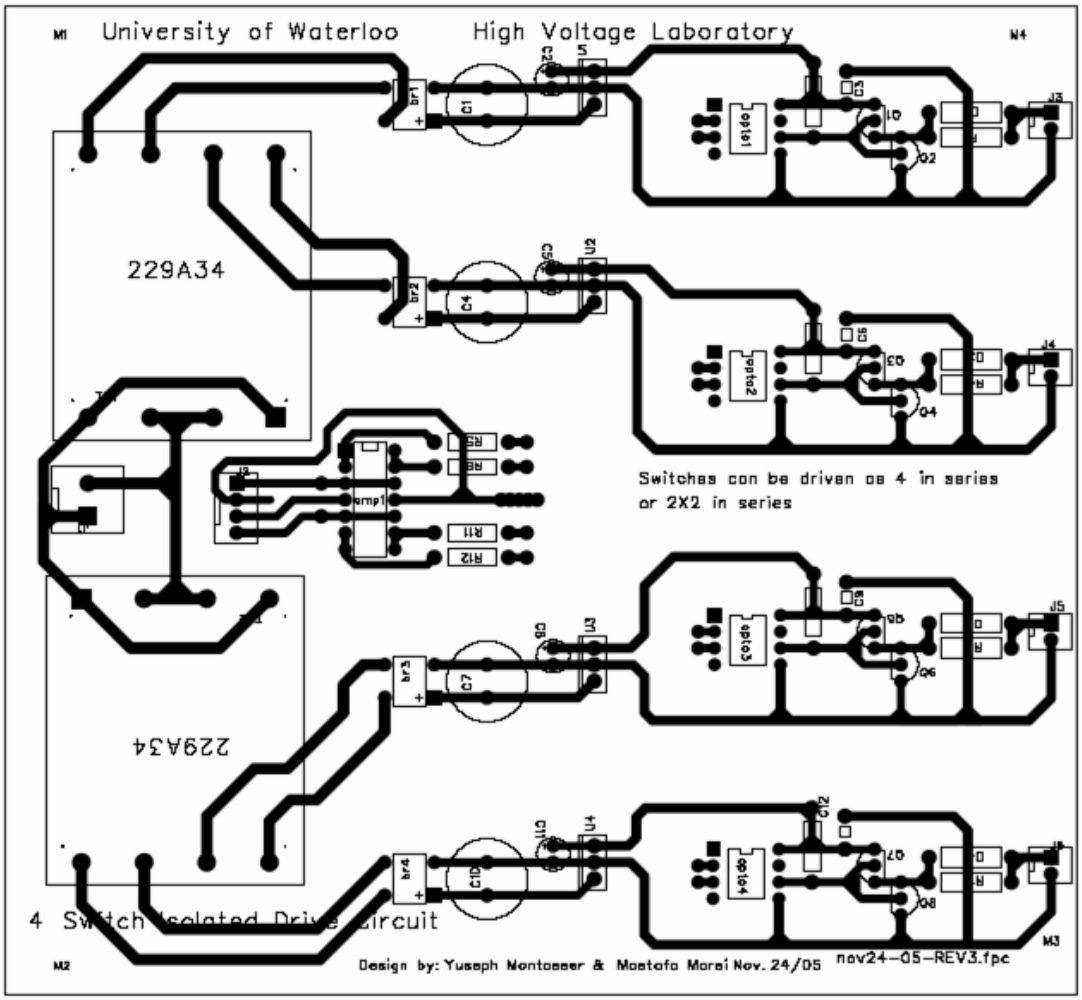
Item	Quantity	Reference	Part	Description
1	17	C1a,C2a,C3a,C4a,C5a,C6a,C7a,C8a,C9a,C10a,C11a,C12a,C13a,C14a,C15a,C16a,C3pic	1000u	Electrolytic Capacitor
2	18	C1b,C2b,C3b,C4b,C5b,C6b,C7b,C8b,C9b,C10b,C11b,C12b,C13b,C14b,C15b,C16b,C2pic,C4pic	10u	Electrolytic Capacitor
3	18	C1c,C2c,C3c,C4c,C5c,C6c,C7c,C8c,C9c,C10c,C11c,C12c,C13c,C14c,C15c,C16c,C3pic,C5pic	0.1u	Ceramic Capacitor
4	17	D1,D2,D3,D4,D5,D6,D7,D8,D9,D10,D11,D12,D13,D14,D15,D16,Dpic	D1N4148	Fast Diode
5	1	J2	HEADER_6	6 pin header
6	16	O1,O2,O3,O4,O5,O6,O7,O8,O9,O10,O11,O12,O13,O14,O15,O16	HCNW4504	High Speed Optocoupler
7	16	Q1a,Q2a,Q3a,Q4a,Q5a,Q6a,Q7a,Q8a,Q9a,Q10a,Q11a,Q12a,Q13a,Q14a,Q15a,Q16a	MPS8099	NPN transistor
8	16	Q1b,Q2b,Q3b,Q4b,Q5b,Q6b,Q7b,Q8b,Q9b,Q10b,Q11b,Q12b,Q13b,Q14b,Q15b,Q16b	MPS8599	PNP transistor
9	1	REGpic	uA7805C	5V 1.5A Linear Regulator
10	8	REG1,REG2,REG3,REG4,REG5,REG6,REG7,REG8	uA7815	15V 1A Linear Regulator
11	1	R_load	8.33k	6 parallel 50k 100W resistor
12	1	Rpic	15k	1/4 Watt Resistor
13	20	Rpic1,R1b,Rpic2,R2b,Rpic3,R3b,Rpic4,R4b,R5b,R6b,R7b,R8b,R9b,R10b,R11b,R12b,R13b,R14b,R15b,R16b	20k	1/4 Watt Resistor

Table Cont.

Item	Quantity	Reference	Part	Description
14	16	R1a,R2a,R3a,R4a,R5a,R6a,R7a,R8a,R9a,R10a,R11a,R12a,R13a,R14a,R15a,R16a	1k	1/4 Watt Resistor
15	16	R1c,R2c,R3c,R4c,R5c,R6c,R7c,R8c,R9c,R10c,R11c,R12c,R13c,R14c,R15c,R16c	33	1/4 Watt Resistor
16	16	R1d,R2d,R3d,R4b,R5d,R6d,R7d,R8d,R9d,R10d,R11d,R12b,R13d,R14d,R15d,R16d	SM104032004F	RES 2M OHM THICK FILM 1.5W 1%
17	1	Umicro	PIC16F73	PIC microcontroller
18	4	U1,U2,U3,U4	TLC2274ACN	High speed 4 Op-amp IC
19	16	Z1,Z2,Z3,Z4,Z5,Z6,Z7,Z8,Z8,Z9,Z10,Z11,Z12,Z13,Z14,Z15,Z16	IXBT16N170	1700V discrete IGBT switch
20	17	BR1,BR2,BR3,BR4,BR5,BR6,BR7,BR8,BR9,BR10,BR11,BR12,BR13,BR14,BR15,BR16,Brpic	DB102	Rectifier bridge
21	9	TX1,TX2,TX3,TX4,TX5,TX6,TX7,TX8,TXpic	229A34	Low profile PCB transformer
22	1	CR	200ECSD	20 MHz oschillator

Appendix F

PCB Board Schematic from Gerber File



Appendix G
Operating the Bipolar Pulse Modulator

To operate the bipolar pulse modulator an external DC source as well as an external load resistor must be connected to the device.

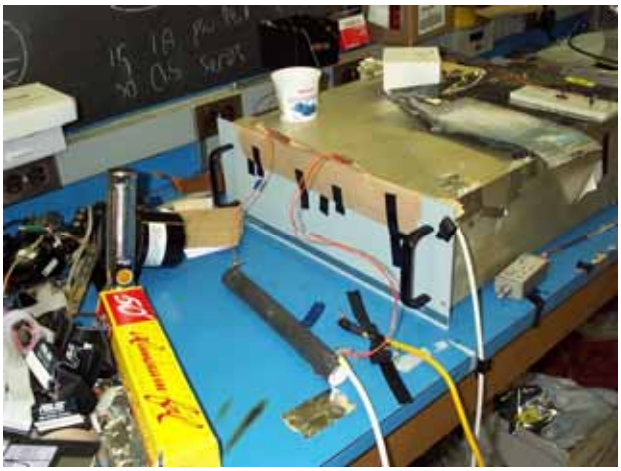


Figure H.1: Lab built modulator packaged in metal enclosure with an external resistor connected

Figure H.1shows the external resistor connected to the modulator by two leads exiting the front of the metal enclosure. The white high voltage cable coming off the side of the pulse modulator is for connection to the test object. If a test object was being used another lead would be connected to the other terminal of the resistor as well. As discussed previously the value of the resistor can be adjusted depending on the capacitance of the test object as well as the maximum DC-link voltage applied.

Next the DC source must be connected to the modulator. Because the DC source can only supply a limited amount of current the use of additional DC-link capacitors is recommended. The DC-link capacitors currently connected to the modulator are shown in the Figure H.2.

Figure H.2: Connections of the ground and HV-DC.

Now that all the required connections have been made the power for the controller and driver circuits can be turned on by plugging in the power cord into the wall socket.

Next the external high voltage DC source must be turned on. Now to turn activate the modulator the keypad shown in Figure H.3 must be used.

Figure H.3: Keypad used to control the modulator

To activate the pulse modulator output push key #1. This will start the program and there will be an output at the load. Next set the desired DC-link value on the DC source. To increase the fundamental frequency of the output waveform simply press key #3. To decrease the fundamental frequency simply press key #4. To turn off the output of the modulator press key #2 which will immediately stop the output. It should be noted that simply pressing the stop key does not mean that the load is safe to touch. The external DC source must be turned off and the DC-link capacitors must be fully discharged before the test object is safe for handling.

Appendix H
Further Discussion on Strand Insulation

During the aging process of the magnet wire samples two main degradation mechanisms occur within the enamel insulation. These two mechanisms are partial discharge (PD) and space charge formation [62]. This fact can be observed from the data collected from aging samples with the unipolar pulser at various frequencies. A residual life model, shown in Figure I-1, of two of the conventional wires can be constructed using the DC breakdown strength of various samples after aging at different frequencies.

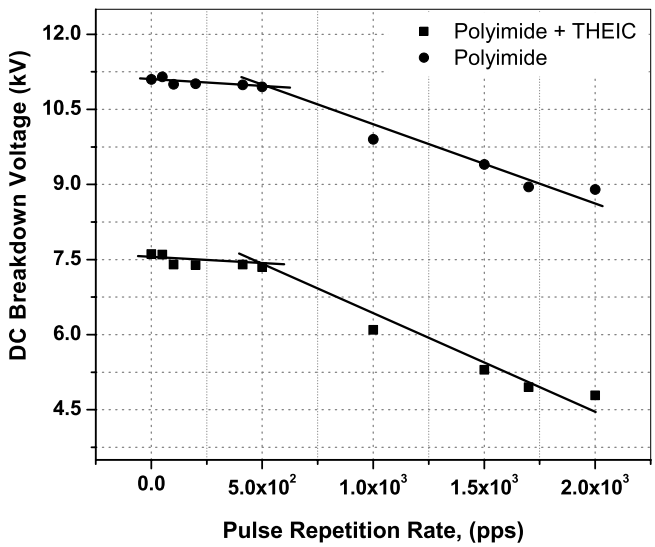


Figure I-1: Residual life of conventional wires based on the DC breakdown strength under unipolar aging [62]

The large difference in breakdown strength of the wires is due to the difference in thickness of the enamel coating. The number of layers applied to the wire during manufacturing varies with manufacturer. The two distinct slopes on the plot above indicates that there are two aging

mechanisms at work [65], which as mentioned previously are PD and space charge formation. The trend of breakdown strength decreasing as the frequency increases has been also shown under high frequency AC aging and again determining the residual DC breakdown strength of each sample. The same trend is observed, as the frequency increases the DC breakdown strength decreases.

Partial discharge is an extrinsic process which occurs either on the surface of the wire or within cavities in the bulk of the insulation. Because it occurs outside the bulk of the insulation it is called an extrinsic process. If the inception voltage is reached on the surface or inside a void in the bulk of the insulation, it can cause partial discharge (PD) activity. This discharge produces heat and radiation as well as chemical changes in the insulation material which degrades the insulation material.

The second mechanism space charge formation occurs when there is an accumulation of free charges within the insulation. When enough charges accumulate recombination of these charges may occur causing a discharge, producing a reaction similar that which occurred during the PD. These trapped charges can also cause electric field enhancements within the insulation reducing the PD inception voltage inside voids within the insulation, potentially creating increased PD activity.

The mechanism for how these charges currently accumulate within magnet wire insulation is currently being debated. There is currently two theories which have been published and attempt to explain these mechanisms. The first theory proposes that the charge accumulation occurs due to the high frequency nature of the changing electric field found inside the insulation. The authors suggest that because the switching time of this electric field, under PWM, is higher than the relaxation times of a number of the dipoles these dipoles are unable to synchronize with the field and so become stuck in one position. When the field reverses again this mechanism will again repeat itself, and over time charge accumulation will occur creating concentrations of charge within certain areas. Eventually enough charges will accumulate to cause a recombination which will create a discharge.

The second theory proposes that the charge accumulation occurs over time within impurities and defects within the bulk of the insulation. In this method internally trapped charges within the material can hop to the interface between layers of the insulation. Over time the more free charges begin to accumulate until there is enough for recombination to occur, creating a discharge. The amount of charge trapped is heavily dependent on the number of layers and as the number of layers increases so does the amount of trapped charge.

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