Silicon dry etching using fluorine-based gas for nanoscale cone and grating structure fabrication

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

Dry etching technique is widely used in creating high aspect ratio nanostructures currently. This pattern transfer process has better performance in the profile controlling compared with wet etching technique. For the plasma etching, fluorine-based plasmas are mainly used for rapid isotropic silicon etching process. To achieve an anisotropic profile, SF_6/C_4F_8 and SF_6/O_2 are generally used in the etching process. These anisotropic profiles, such as cones and pillars, are widely used in photovoltaic and optoelectronic devices. However, current research related to cone structure fabrication are a more random process. The size of the profile cannot be precisely controlled. Although there are some recipes can result in a taper profile, but large amount of C_4F_8 gas also inhibits further etching. In addition, the etching process with the mixture of C_4F_8 and SF_6 gases always raises the concern about chamber contamination issues.

In this thesis, some solutions are proposed to solve such problems. The traditional pseudo-Bosch process has been optimized by introducing a periodical oxygen clean step to remove the fluorocarbon polymer deposition during process. The cone array of a controllable size is fabricated by combining with optimized pseudo-Bosch process and maskelss etching. Another two ways of fabricating cone array are also introduced which are shrinking SiO_2 mask and photoresist mask. Unlike SiO_2 masks that spontaneously form a tapered structure when they are almost consumed, photoresist masks can be manually applied oxygen plasma to shrink periodically for a controllable cone array fabrication. In addition, the detailed investigation of near room temperature SF_6/O_2 etching is presented to prove it is possible to be an alternative way of pseudo-Bosch process in cone or grating structure fabrication.

Acknowledgements

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Chapter1. Introduction

1.1. Research goals and thesis organization

This research is mainly focusing on the silicon dry etching using fluorine-based gases with an aim to achieve the fabrication of nanoscale cone or grating structures of controllable size.

This thesis is divided into six chapters. This chapter gives an introduction to etching technique. The mechanisms and equipment including ICP-RIE system are introduced. A detailed description and some issues related to Bosch and cryogenic etching process is elaborated. Chapter 2 describes an optimized method to fabricate a controllable nano-cone array by combining pseudo-Bosch process followed by mask-less etching sharpening technique. Chapter 3 and 4 present a novel approach to fabricate microscale cone array by shrinking SiO_2 mask (Chapter 3) or photoresist mask (Chapter 4). Such microscale cone arrays may be utilized for AFM tip fabrication. Chapter 5 gives a detailed investigation of SF_6/O_2 etching at room temperature. It provides an alternative way to pseudo-Bosch process without any contamination issue. In Chapter 6, summary of this thesis work and future direction is presented.

1.2. Overview of etching

Etching is a main pattern transfer technology in semiconductor manufacturing process [1].Etching is divided into two main categories, which are wet etching and dry etching. The main difference between wet etching and dry etching is the phase of the etchants.

Wet etching technique is the earliest pattern transfer technique applied in semiconductor industry. It has many advantages which include but not limited to high

selectivity, high etch rate, low cost and easy operation. For wet etching, it usually uses liquid etchants. The wafer is often submerged in the solution where the etching process takes place. A common liquid etchant is buffer hydrofluoric acid (BHF) since it can be used to etch silicon dioxide at room temperature. It is worth noting that only chemical processes take place in wet etching.

However, it was gradually replaced by dry etching. Dry etching contains two different types: non-plasma based, and plasma based. For non-plasma based dry etching, it uses reactive gas to react spontaneously to achieve etching process. Two examples are listed here. First one is the reaction between chlorine gas and silicon wafer at about 800℃. The second example is the reaction of xenon di-fluoride (XeF_2) and silicon [2].This process can take place at room temperature. This process is often applied in micro electromechanical systems (MEMS). However, plasma-based etching is more popular currently. So, for dry etching, sometimes researchers just call it plasma etching since it mostly uses gaseous etchants in plasma. Distinct from wet etching, plasma etching consists of both physical and chemical processes.

1.2.1. Etching procedure

For a typical etching process, three processes are involved: First, the etchants will be carried to the surface of the substrate. Second, etchants will react with the film. Last step, the byproduct of the etching process will be removed. Diffusion and flow may happen in this step [3].

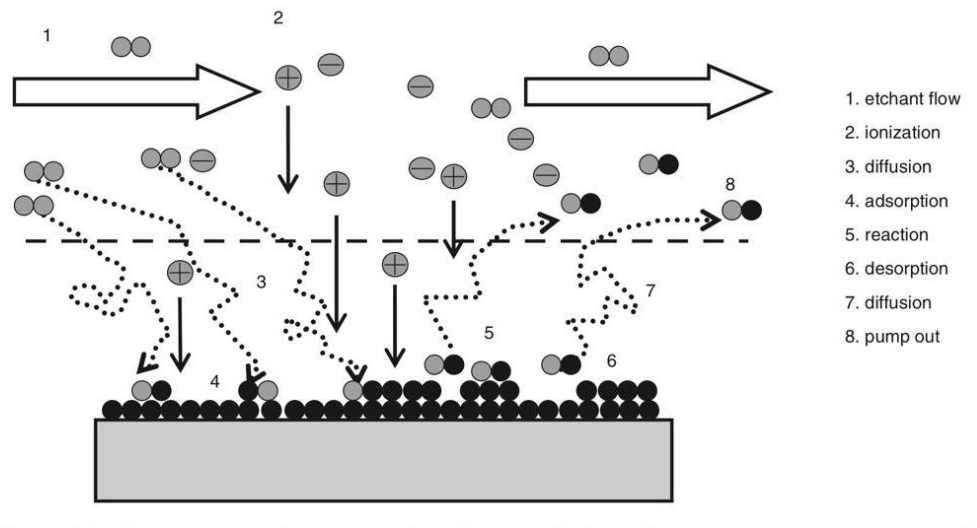

Fig. 1.1 Basic process in plasma etching [3].

Fig 1.1 gives an illustration of basic processes taking place in plasma etching. As Fig 1.1 showed, with the introduction of etchant flow, it will generate some active species such as radicals, ions, electrons and neutrals by ionization or other methods. Then, the active species can diffuse to the surface of the substrate which will be etched. The fourth step is called adsorption. In this step, the reactive species will adsorb onto the surface of substrate. After adsorption, the reactive species will react with the material which will be etched. This step is the reaction step. Ion bombardment enhances the reaction step. Taking chlorine atom as an example, with the help of ion bombardment, the adsorbed chlorine atoms strike silicon backbonds more effectively, resulting in the formation of a volatile silicon tetrachloride molecule. The desorption step happened after the reaction step. At high vapour pressure, the product of the reaction will desorb into gas phase. After that, diffusion often happens. The last step of plasma etching is called pump out. In this step, the desorbed species will be pumped out to prevent the redeposition [4].

1.2.2. Equipment of conventional reactive ion etching system

Such processes often happen in a reactive ion etching system. A schematic conventional reactive ion etching system, as shown in Fig 1.2, contains a RF power source. The reactive species such as fluoride atoms and carbon tetrafluoride molecules are excited with the help of RF power source. The etching gases such as SF_6, C_4F_8 and CHF_3 are introduced from the top side. In the vacuum reaction chamber, the wafer was put on the bottom side of the parallel plate. After the reaction steps, the volatile substances will be pumped out from the bottom side [4].

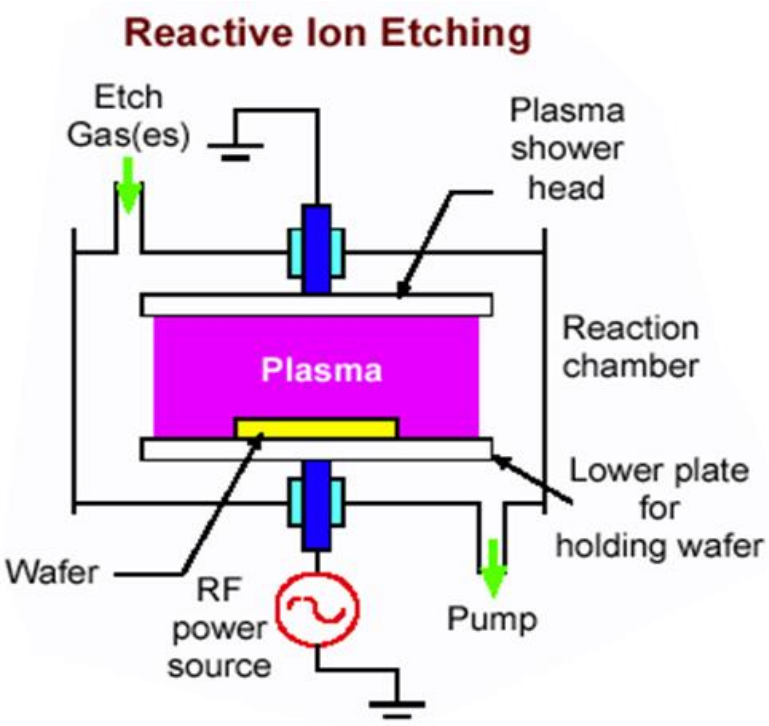

Fig. 1.2 Reactive ion etching system [5].

However, such conventional reactive ion etching system can only etch order of 100nm structures. This low etch rate limits the development of silicon etching technology. The etch rate is related to the plasma density. But it is not a simple task to solve by directly increasing the RF power. With the increasement of plasma density, which means the

increasement of RF power, the self-biasing voltage will also increase. This will result in the increasement of ion bombardment energy and affect the etching selectivity. The introduction of inductively coupled plasma (ICP) system can solve this problem. [1]

Fig 1.3 is the schematic of inductive coupling plasma source. In this system, the plasma generation is isolated from the bottom electrode. An induction coil from the outside couples RF power into the chamber. To accelerate the generated ions, it also has a second RF power source which is connected to the sample stage (bottom electrode). For the coil, it can generate high magnetic field. The electrons will be able to move in circles in the coil with long distance, which means a higher collision and ionization probability. Moreover, the AC magnetic field at RF frequency will generate circular electric field to greatly accelerate the electrons and further increase the plasma density. The self-biasing voltage can be regulated individually since now the sample stage has a separate power supply. As a result, compared to a traditional reactive ion etching system, an ICP system will generate higher plasma density while keeping low ion bombardment energy.

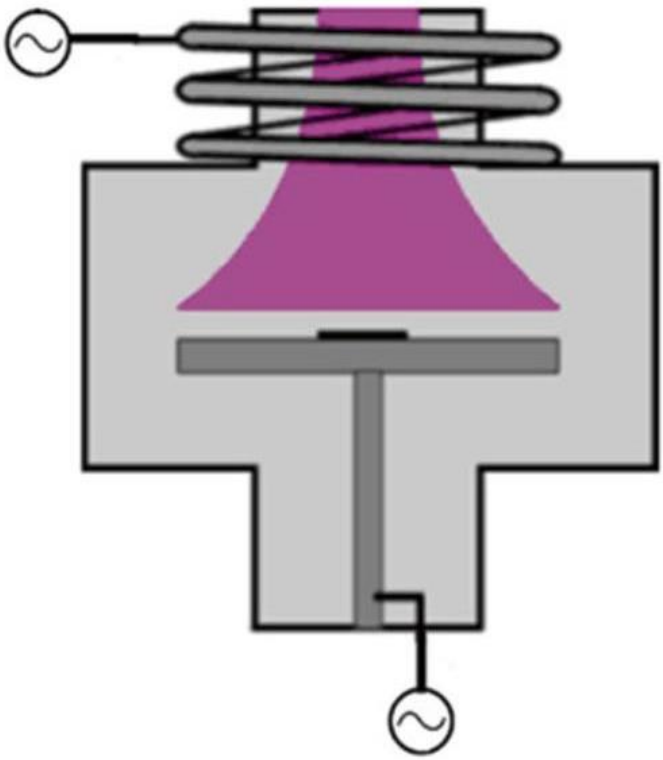

Fig. 1.3 Schematic of inductively coupled plasma source [1].

With the development of ICP system, it is now feasible to achieve high etch rate and deep reactive ion etching (DRIE). Deep reactive ion etching is an expansion of reactive ion etching. Compared to reactive ion etching, DRIE holds a better selectivity and controllability of the process. Thus, DRIE is typically used to fabricate a deep feature with high aspect ratio. To achieve high etch rate, halogen-based plasma is always applied to form the volatile products. Even though chorine and bromine-based plasma can generate anisotropic etch profile, chlorine and bromine-based plasma are gradually replaced by fluoride-based plasma because of their toxicity. As a result, it is highly recommended to use fluoride-based plasma in deep reactive ion etching process such as SF_6. In addition, the etching process is very sensitive to the temperature of the wafer surface. To maintain the temperature of the wafer surface, the equipment usually contains a helium backside cooling. In addition, sometimes to achieve a lower temperature like lower than -100℃, people also

apply liquid nitrogen in the system [6].

1.3. Silicon deep reactive ion etching processes

In general, there are two main categories of deep silicon reactive ion etching technique which are Bosch process and Cryogenic process.

1.3.1. Bosch process

Bosch process is the most widely used process of deep reactive ion etching. It is also named time-multiplexed etching since the cycle of Bosch process often consists of one etching step and one passivation step.

1.3.1.1. Bosch process cycle [1]

In the etching step, the etch gas is sulfur hexafluoride (SF_6), which is nontoxic. Since there are no other gases such as oxygen in this step, it will not result in any passivation film on the sidewall. The etching step will give an isotropic profile. However, in Bosch process, this step always takes just a few seconds per cycle, which means that an anisotropic profile can be obtained. The reason is that if SF_6 just etches for a few seconds, both vertical and lateral direction etching will be limited. After the SF_6 etching step, the deposition step immediately starts. In the deposition step, the process gas is octofluorocyclobutane (C_4F_8). It will react and create a thin passivation layer of fluorocarbon polymer on the sidewall. Such passivation layer will prevent the etching in lateral direction. Since the etching in lateral direction is limited, Bosch process can etch deep in vertical direction and result in a high aspect ratio feature. As mentioned above, after the deposition step, there will be again the SF_6 etching step. In this step, the deposited fluorocarbon layer at the bottom will be

sputtered away by the accelerated ions in the vertical direction. Then SF_6 gas will continue to etch in both vertical and lateral direction for a small period. By alternating the etching and deposition step, a high aspect ratio profile can be obtained.

The Fig 1.4 shows the process of a Bosch process from the first deposition step. Since the SF_6 etching is isotropic etching, even though the addition of passivation step can prevent the etching in lateral direction, the sidewall of the etching profile is not as smooth as anisotropic etching. As Fig 1.4 showed, it will result in a scalloping structure. It is easy to control the scalloping structure by adjusting the period of etching step and deposition step. If a smooth sidewall is required, the etching step duration should be decreased. But to meet the requirement of high etch rate, one should increase the period of etching step. Hence there is a trade-off between etch rate and sidewall smoothness.

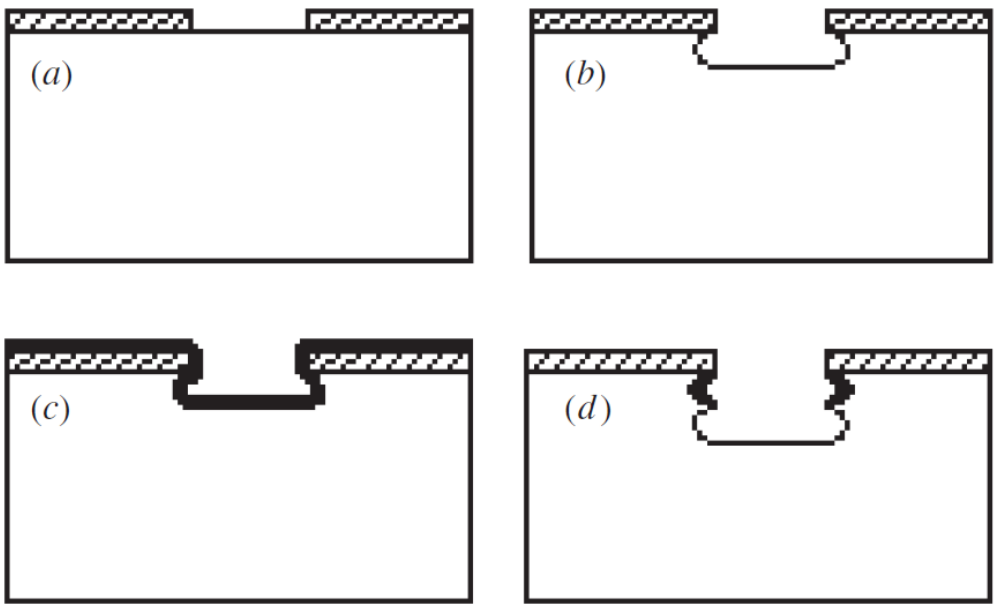

Fig. 1.4 Bosch process from the first deposition step [7].

For our Bosch process, for the etching step, it often uses 130sccm SF_6. The RF bias power is 12w and the ICP power is 600w. The duration of etching step is 9s. For the deposition step, it introduces 85sccm C_4F_8. The RF bias power is 0W and the ICP power

is 600w. The duration of the deposition is 7s. Bosch process is often set to run under this condition with the pressure of 20mTorr and temperature of 15℃. Fig 1.5 is the SEM image of a pillar array after 5 cycles Bosch. The etch rate of the process is about 260nm per cycle.

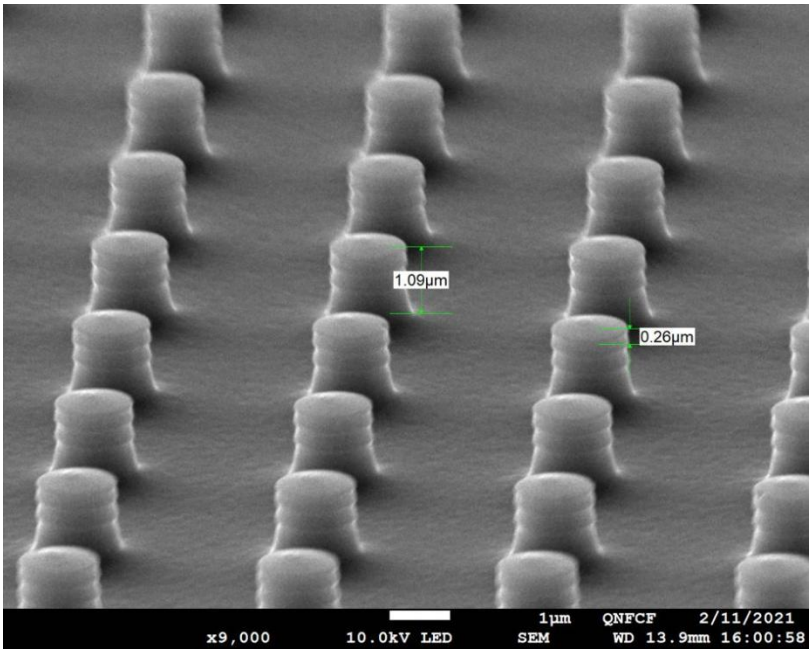

Fig. 1.5 SEM image of silicon pillars after 5 cycles Bosch etching.

1.3.1.2. Special issues related to Bosch process

1.3.1.2.1. Aspect ratio dependent etching

Aspect ratio dependent etching, also known as reactive ion etching lag, is a general phenomenon in etch process, where the etching depth depends on feature size. It is of particular concern when producing high aspect ratio structures. For certain applications, aspect ratio dependent etching may cause large features to be etched through before the small features do, causing etching of the layer underneath, or leakage of He cooling gas. Nevertheless, sometimes aspect ratio dependent etching is useful especially for the fabrication of slope features such as electrodes. [8]

As Fig 1.6 showed, there is a relationship between the aspect ratio and etch rate. Aspect

ratio dependent etching phenomenon can be directly observed through this figure.

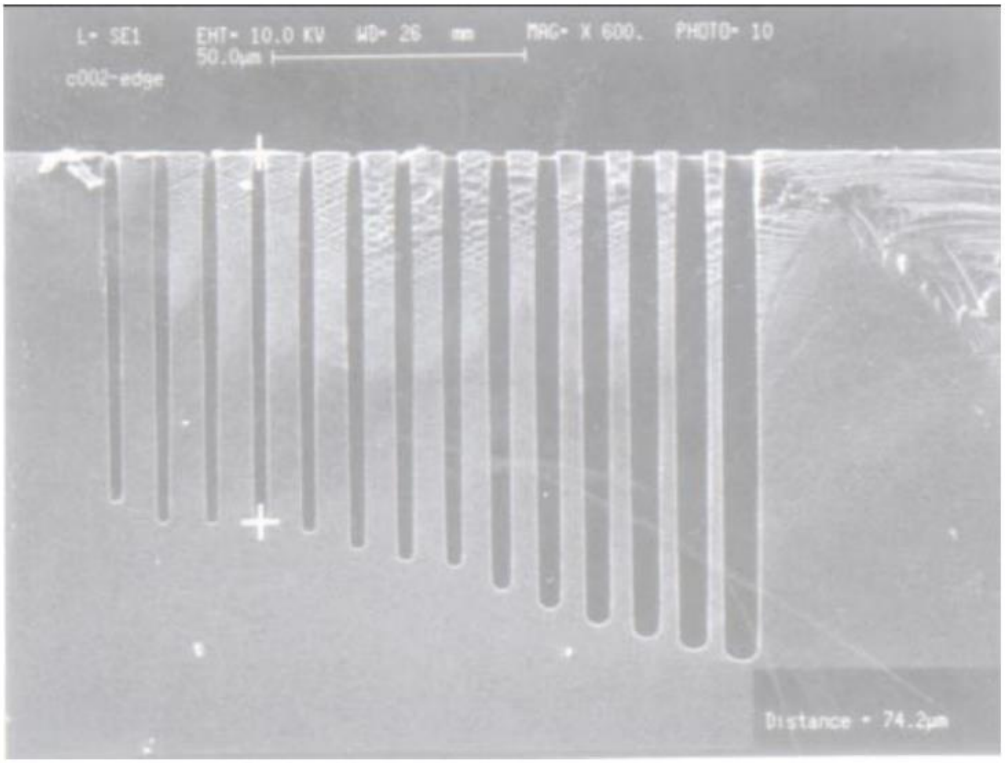

Fig. 1.6 ARDE phenomenon [9].

It has been studied that the major reason of aspect ratio dependent etching is the exhaustion of fluoride at the bottom of the trench [10].In addition, pressure and temperature are also two factors to control aspect ratio dependent etching. Furthermore, it has also been reported that aspect ratio dependent etching is due to the transport of radicals into trench/hole.

In this way, if it is required to optimize the aspect ratio dependent etching, it is possible to achieve it by adjusting the parameters of etching process. It has been summarized that with the increasement of bias voltage, the aspect ratio dependent etching effect will decrease [11].Aspect ratio dependent etching is also related to pressure. For low pressure, it will give a tight ion angular distribution which means aspect ratio dependent etching will

be improved [12].

Based on the research done by J. Tian and M. Bartek, the main factor which controls the etch rate for different trench dimensions is the width of the trench but not the length [13].It means the length contributes little to the etch rate.

Some researchers also did experiments to investigate the aspect ratio dependent phenomenon in three-steps Bosch process which are polymer deposition, polymer breakthrough etch and Si etching [14].They found that all the three steps are aspect ratio dependent. Additionally, for small features, the etch rate and deposition rate will be negatively affected. It is worthy to note that for the polymer etch step, the etch rate is slightly influenced by the dimensions of the feature.

1.3.1.2.2. Loading effect

The loading effect is a change in etch rate caused by variation of pattern density. It may happen to feature of the same size as well as features of varied sizes. The loading effect is caused by reactant depletion [8].

Microloading is defined as the variation of etch rates between features in a small region on the wafer. As mentioned before, the loading effect will happen due to the exhaustion of reactants. With the increasement of surrounding loading, it will result in a reduction of etch rate. It should be noted that the loading effect will result in a nonuniform etching. High density patterns require more reactive species and higher removal of etched byproducts than low density patterns. As a result, the pattern of higher density and lower density will get a different depth [8].

To solve this problem, one can introduce abundant source of reactants at low pressure, as the loading effect is less significant at low pressure [8].

1.3.1.2.3. Micrograss

Polymer residues may be generated on the surface during the etching process, leading to micro-masking and thus the phenomenon of micro-grass. Fig 1.7 shows the micro-grass phenomenon. The easiest way to solve this problem is increasing the DC bias voltage. However, when increasing the bias power, even though it can eliminate the grass formation, it may result in some other negative effects. For example, the passivation layer in vertical direction formed in deposition step may be affected under high bias power [15].

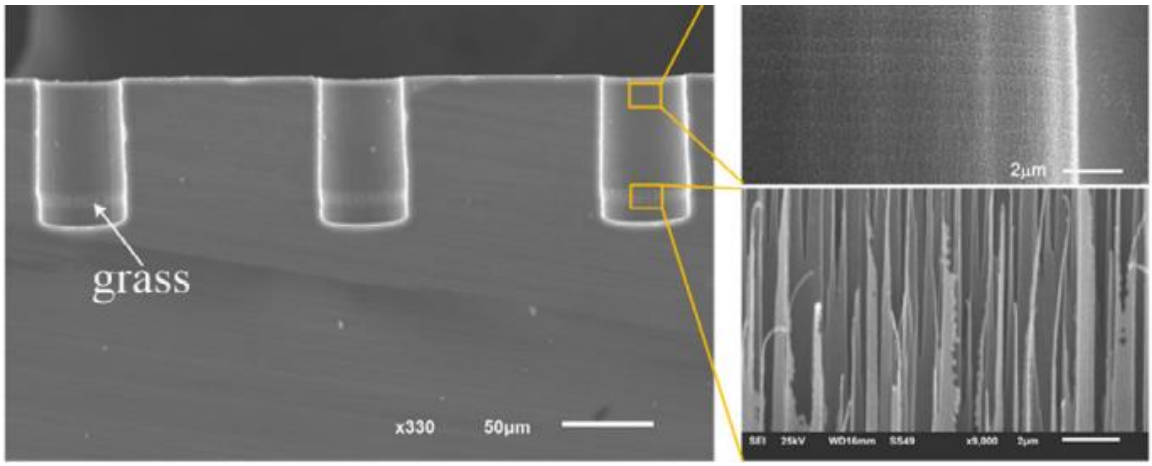

Fig. 1.7 Micro-grass phenomenon (right bottom: magnified image of the micro-grass at bottom of the holes) [16].

Similar to reactive ion etching lag issue, this problem can also be solved by adjusting the parameters of etching recipe. In addition, the micrograss formation is also related to the size of the feature. It has been shown that the micrograss is controllable. For example, if high temperature is applied, the micrograss can be reduced [11].

1.3.1.2.4. Notching

Notching is a general problem in Bosch process. As shown in Fig 1.7, the width of the lateral direction at the bottom is different from the width of the top of the structure. Such

notching effect always happens at the silicon-insulator interface when etching a SOI (silicon on insulator) wafer. The main reasons to notching are charge accumulation at the bottom oxide surface and the resulting electrical fields [13].

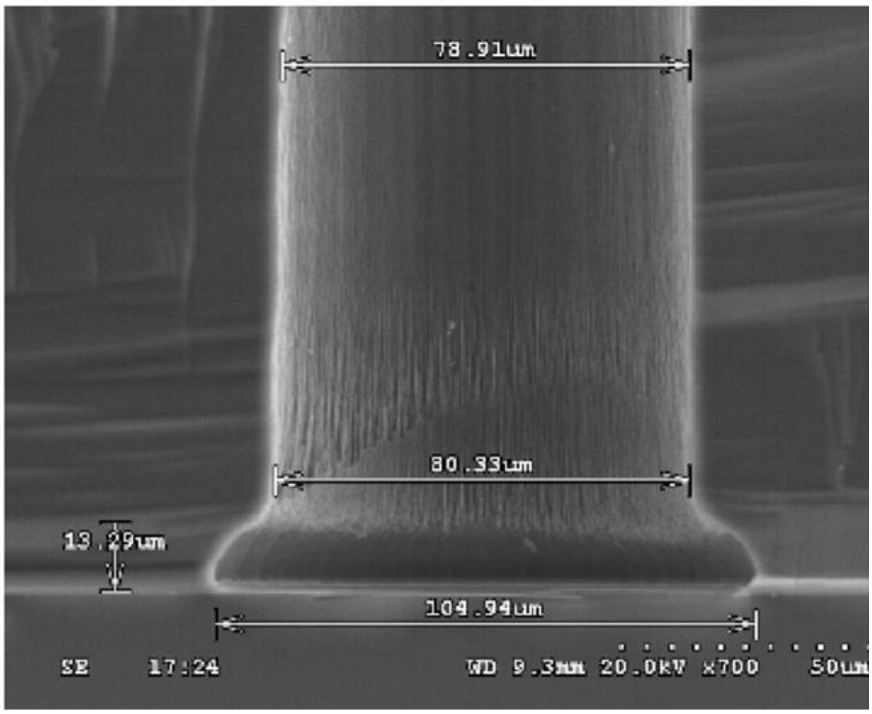

Fig. 1.8 Notching at the Si/SiO_2 interface [8].

As summarized in Wu, Kumar, and Pamrthy's review, since the loading and aspect-ratio dependent etching (ARDE) effect demands mild over etch, notching becomes more serious when there is substantial micro-loading or ARDE effect. It is suggested that notching can be avoided by enlarging the thickness of passivation layer by extending the duration of deposition step. It is also noted that the formation of notching is often influenced by pressure. As pressure is raised, ion energy decreases, leading to a low polymer sputtering rate, which minimizes the notching [8].

The notching effect can also be managed by applying a periodic pulsed RF power to the cathode. By enabling charge to disappear during the RF "off" stage, bias pulsing decreases ionic charging of the insulator under the silicon substrate, allowing for regulation

of bottom notching [17].There is no notching happening where a conductive material is applied to form the etch-stop layer [13].

There is also an alternative method to mitigating notching without applying pulsed bias to the cathode. It consists of two phases. The first phase employs a time-multiplexed etching method to achieve maximum depth without etching through. The second stage uses a continuous etch, which combines an etch gas SF_6 and a passivating gas C_4F_8 to finish the fabrication of the final small section of the trench [8].

1.3.2. Cryogenic etching

1.3.2.1. History

In the process of deep etching, low pressure plasma stands out because of its ability to direct the etching along the vertical direction and to form high-aspect-ratio structure. Additional gases are commonly needed to prevent the erosion caused by spontaneous chemical reactions. Of deep concern is finding an etching process that is fast, reproductible, and clean for industrial use, and cryogenic processes are good for achieving silicon high-aspect-ratio structures. The etching of silicon substrates at very low temperature was first introduced at the end of the 1980s [18].

To meet the demands of high etching rate, anisotropy, and high selectivity at the same time, it needs more research on cryogenic process. Even though as mentioned in Bosch process, SF_6 gas is possible to give a high etch rate, it is still an isotropic etching. Some people even add other gases such as CF_4, oxygen, HBr and CHF_3 to obtain recipes with higher etch rate [18].The anisotropy is the problem which needs to be resolved. From Tachi's suggestion, if it is possible to slow down even prevent the reaction happening in the sidewall but do not affect the reaction in the vertical direction, the anisotropic etching

should be achieved. Based on their research, they keep the temperature of the wafer below -100℃. The phase of SF_6 is a condensate state at <-130℃, thus no reactions happened on the sidewall [19]. This provides a good direction for cryogenic etching even though it did not show a deep etching profile.

Three years later, they do the research about the behaviour of different gases and materials at low temperatures. As shown in figure 1.9, it is obvious that the SF6 can give a high etch rate at the temperature higher than -130℃ [20].

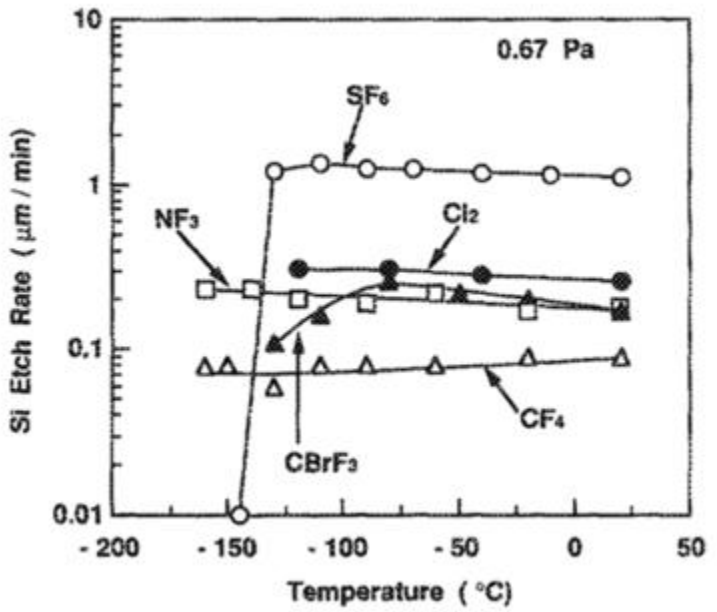

Fig. 1.9 Silicon etching rates for different gases at different temperatures [20].

In 1995, Bartha et al utilized a distributed electron cyclotron resonance (DECR) device as well as a helicon style plasma reactor to conduct several silicon cryogenic etching experiments. Unfortunately, even though they tried to cool the temperature of SF_6 gas to -120℃, they cannot get an anisotropic etching profile. However, when they introduced oxygen, the anisotropic structure is achieved. In addition, they also obtained a high etch rate and high selectivity. So, they proposed that the previous experiment done by pure SF_6

plasma is not reliable. In that experiment, SF6 gas will inevitably be introduced with a small oxygen flow. [21]

Jansen et al. published a new paper in 2001 about an adaptation of the black-silicon method for cryogenic etching. Figure 1.10 shows the relationship between the concentration of oxygen and temperature at specific condition. This figure gives a clear black silicon formation region. Black silicon is a very nonuniform silicon film that looks black when illuminated due to the micro-grass that scatters light at randomly directions. The proposed approach entails delineating the black-silicon area with a dummy silicon wafer and then operating in conditions very near to the etching/black-silicon forming border. Surprisingly, this border is not a straight line. There is a temperature at which black silicon is easier to form. [22]

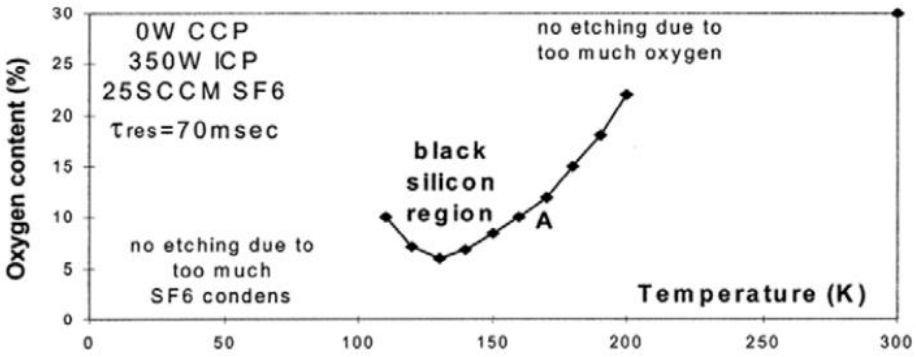

Fig. 1.10 The condition of the formation of black silicon [22].

1.3.2.2. Mechanism

In the cryogenic etching process, a high power is injected into the source to create a high-density plasma, which can be helpful to the independent control of ion flux and the ion energy (as shown in Fig 1.11). This can result in the increasement of etch rate. SF_6 and O_2 gases are introduced to the source part. SF_6 can provide abundant fluoride radicals and

oxygen is used to generate the passivation layer SiOxFy as mentioned before. The content of oxygen is controlled near 10%. In the diffusion chamber located in the reactor's lower portion, the wafer is laid on a substrate holder. SiO_2 is commonly used as suitable mask material since it holds the property of high selectivity and low contamination. Liquid nitrogen is used to achieve the low temperature. The temperature of the chuck is monitored and adjusted by a proportional-integral-derivative (PID) controlled heating system. With the adaption of this element, it is possible to keep the temperature at a relative low level approximately -100 ℃. A separate RF power supplies bias to the substrate. The introduction of helium is used to optimize thermal conductivity and promote the heat transfer to the cooling part [18].

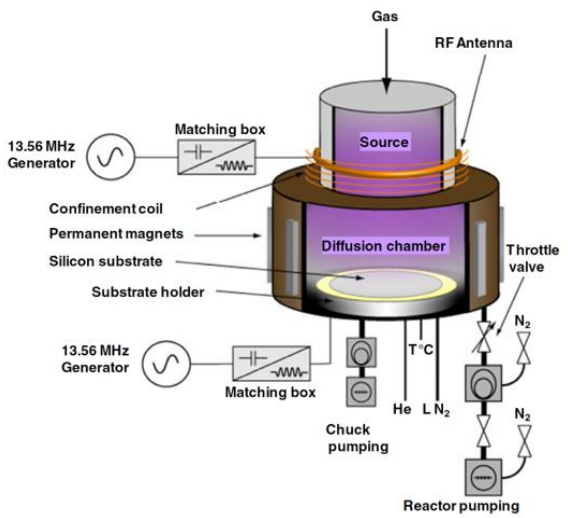

Fig. 1.11 Scheme of a typical ICP reactor dedicated to cryogenic etching [18].

Fig 1.12 gives a schematically illustration of etching mechanism of cryogenic etching. The plasma source generates fluorine, SF_x, and O radicals, which migrate to the surface of the substrate. SiFx molecules are obtained from the spontaneous reactions of fluorine radicals and silicon atoms at the surface. Fluorine will disperse across 2–5 monolayers before interacting with silicon in the absence of bias. SiF_4 is the main by-product of the reactions and is then either dissociated in the plasma or evacuated by the pumping system

because of its volatility. SiO_xF_y molecules can be formed because of oxygen-SiF_x reactions, obstructing the etching process. This siliconoxyhalide passivation layer is very fragile. Additional gases, such as HBr, may be used to boost the efficiency of ambient temperature processes and minimise undercut.

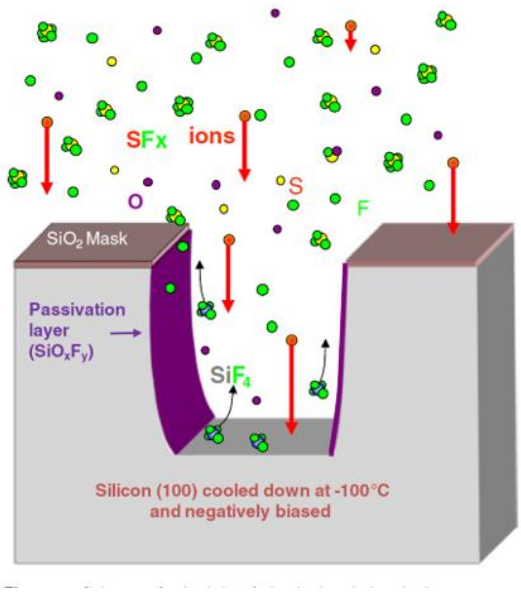

Fig. 1.12 Cryogenic etching mechanism [18].

1.3.2.3. Issues of cryogenic process

1.3.2.3.1. Bowing

Fig 1.13 is a SEM image which shows bowing formation. Boufnichel et al. presented the processes underlying the creation of bowing during silicon cryogenic etching. The bowing effect will be increasingly severe with the increasing of the length of the operation. Both ions and radicals contribute to the development of bowing. Increased self-bias will facilitate its growth. The side slope of the mask will also lead to the production of bowing. To avoid incident ions from being deflected, straight and vertical mask side slopes are favoured. By modifying the equilibrium between ion flux and F/O relative density, the appearance of bowing can be regulated. It was established that the time dependency of

lateral etching in SF_6/O_2 plasma at room temperature was caused by a rise in the scattering of ions reflected from the mask facets [18].

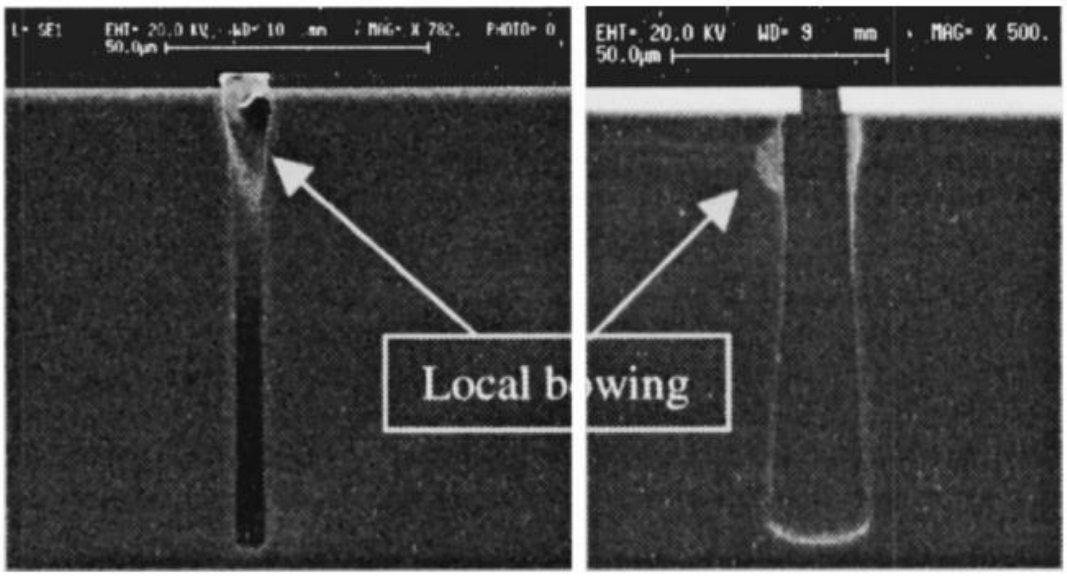

Fig. 1.13 Bowing phenomenon [23].

1.3.2.3.2. Undercut

Undercut is generated by fluorine radicals reacting spontaneously. It occurs at the very start of the etching phase, when the bias stabilises, as described in Boufnichel et al.' research. Additionally, plasma ignition will result in a temporary rise in the silicon surface temperature, which is detrimental to the passivation layer [24]. The size of undercut continues to evolve linearly with the increasing of the duration of operation. A strategy was proposed to eliminate the undercut and prevent its creation at the start of the process, involving the process of increasing the flow rate of SF_6 from 0 to a satisfied level in the first minute of the step. This mechanism is shown in Fig 1.14.

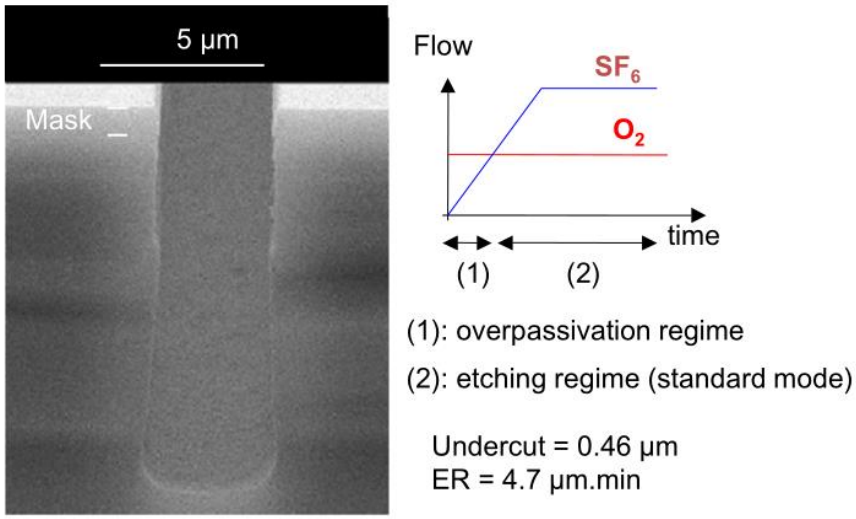

Fig. 1.14 Vertical trench without undercut by using over-passivation at the beginning [18].

1.3.2.3.3. Crystal orientation dependent etching

There is a crystal orientation dependent etching phenomenon when the substrate is at low temperature. Figure 1.15 gives the evidence of crystal orientation dependent etching phenomenon. At the bottom of the trench which is etched at -92°C, it is <111> plane. The negative slope of the sidewall is the evidence of crystal orientation dependent etching. Same as the reported issue about ARDE in Bosch process, crystal orientation dependent etching effect is not always bad. It can be used to fabricate patterns with different geometry shapes [18].

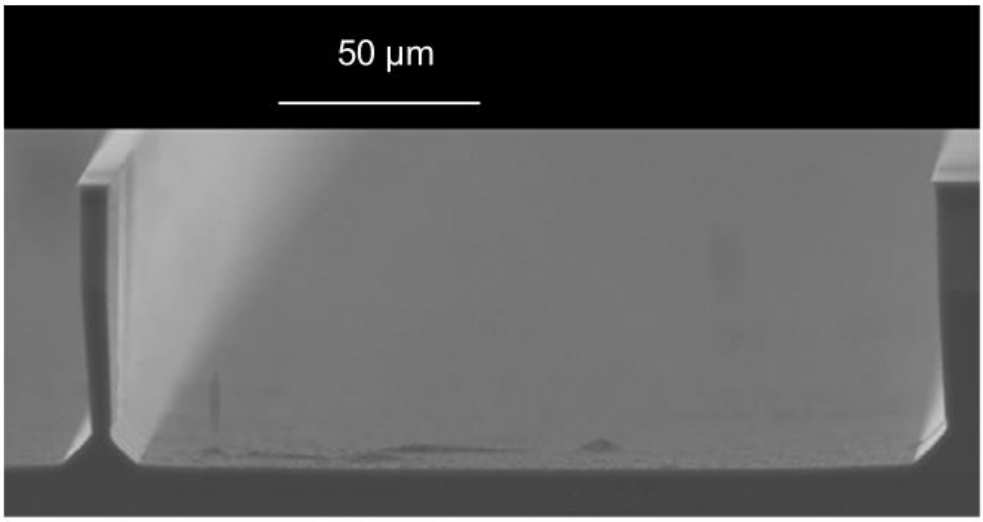

Fig. 1.15 Evidence of CODE [18].

It is reported that for different crystal orientation, the etch rate is different. But such diverse in etch rate for distinct crystal orientations becomes smaller at higher temperature. Thus, one way to prevent crystal orientation dependent etching is to increase the temperature [18].

Mekkakia-Maaza et al also provides alternative way to solve this problem. It requires an additional step called amorphization step. In this step, argon and oxygen plasma will be introduced. With this step, the argon can amorphized the surface. So, the effect will be eliminated. [24]

1.4. Comparison of Bosch process and cryogenic process

For both Bosch process and Cryogenic process, they use SF_6 to etch silicon which will produce volatile molecule SiF_4. Table 1.1 gives a detailed comparison for these two processes.

Table 1-1 Comparison of Bosch process and cryogenic etching process.

Terms	Bosch process	Cryogenic etching process
Working process	Cyclic mode	Mixed mode
Main gases	SF_6 and C_4F_8	SF_6 and O_2
Passivation layer	Fluorocarbon polymer	SiF_xO_y
Process temperature	Room temperature	Less than -80℃
Etching selectivity (Resist to Si)	Close to 70:1	Larger than 100:1
Sidewall roughness	Rough due to scalloping	Smooth

The major difference between these two techniques is the deposition step. As mentioned before, the formation of passivation layer is extremely important in the high aspect ratio fabrication process. In Bosch process, it uses C_4F_8 gases to generate the CF_2-species to form the passivation layer. But in cryogenic process, it introduces SF_6 and oxygen at the same time. As shown in the previous section, it will form a SiF_xO_y layer to prevent the etching in lateral direction. Furthermore, it can also avoid the scalloping structure which may appear in the Bosch process [15].

The second difference is that Bosch process is often operated at room temperature. But for cryogenic process, the temperature is always set to be below -80℃. It is suggested that at such relative low temperature, both requirements of high etch rate and high selectivity between silicon and resist can be met. In addition, the low temperature means the selection for mask is more difficult. The SiF_xO_y passivation layer can be dissociated at room temperature and volatilize. It means that it is not necessary to run a chamber cleaning process after cryogenic etching. Compared to Bosch process, it is much cleaner. [15]

The third difference is the gas injected to the chamber. Distinct from Bosch process, cryogenic process does not require the involvement of C_4F_8. Even though it is not toxic, it is still expensive. However, to cool the chiller temperature, cryogenic process often needs

to use liquid nitrogen [18].

Both Bosch process and cryogenic process can create desirable high aspect ratio features by adjusting the parameters of the process. A typical etching profile is always affected by the SF_6 flow, ICP power, etching and deposition duration, throttle position, substrate holder distance, temperature, and helium backside pressure. These effects are all summarized in the H V Jansen etc. ‘s research about black silicon method [6].

Chapter2. Cone shape fabrication by maskless etching and pseudo-Bosch process

2.1. Introduction

Nanotextures such as nanopillars, nanocones and nanowires have wide applications. Silicon nanowires can be applied in cancer detection and monitoring [25].Nano-texture such as nano-cones can improve the absorption of light by its anti-reflection or light trapping ability [26]. The application of nanocone array in solar cells has been reported for a long time [26]. In the case of ordered cone shape fabrication, the method of achieving tapered profile and controllable size of cone array received considerable attention.

Because of the development of nanofabrication technology, many methods to fabricate nano-textures has been reported. KOH wet etching can give a fixed tapered profile. Seeger, K., and R. E. Palmer fabricated silicon cones and pillars by using silver film as etching mask [27]. The combination of nanosphere lithography and RIE is also a possible way to fabricate nanocones [26].Some researchers also developed a method which combines colloid lithography and reactive ion etching to fabricate inverted nanocone arrays [28].

In this chapter, a combination of non-switching pseudo-Bosch process and maskless etching will be introduced. It is possible to control the size of nanocone arrays by adjusting reactive ion etching parameters and/or mask design.

2.2. Experimental

The experiment starts from bare Si wafer. The wafer is cleaned by acetone and isopropanol (IPA) rinse. Oxygen plasma cleaning is also performed to remove any organic contaminants on the surface. Afterward, a dehydration procedure is conducted at 180 °C.

Then a layer of e-beam resist (ZEP replacement from AllResist GmbH) is spin-coated at 1000 rpm for 1 minute followed by 3 minutes baking on a hotplate at 180 ℃. The lithography process is carried out using JOEL-EBL in QNFCF. In the next step, the sample is developed in ZED-N50 for 1 minute followed by IPA rinse for 1 minute. Subsequently, 30 nm Cr is deposited on the sample. Then, the sample is lifted-off in PG remover overnight. Finally, the sample is transferred into sonication bath of IPA and then oxygen plasma is used to remove remaining residues.

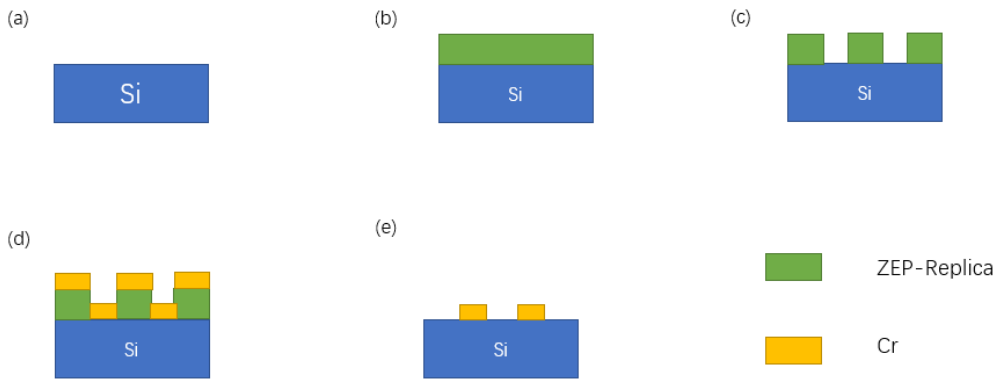

Fig. 2.1 Fabrication Process: (a) Bare Si Wafer; (b) Spin Coating of ZEP-replacement resist; (c) E-beam Lithography and Develop; (d) Cr Deposition; (e) Lift-off.

It has been reported that the recipe below can give a vertical profile in Oxford ICP-RIE system: C_4F_8 38 sccm, SF_6 22 sccm, RF power 20 W, ICP power 1200 W, pressure 10 mTorr and temperature 15℃ [29] (we named this recipe TempReza). Since SF_6 can etch Si isotopically and C_4F_8 can help to form the passivation layer to prevent lateral etching and make the etching profile more anisotropic, the gas ratio of C_4F_8/ SF_6 is associated with the profile especially the taper angle. It is reported that increasing the gas ratio of C_4F_8/ SF_6 will result in a more positively tapered profile, while decreasing it a negatively tapered profile could be obtained [30]. In this experiment, the gas ratio of C_4F_8/ SF_6 is increased to 56:4 to get an acceptable taper angle. However, since the gas of C_4F_8 is in high flow rate,

the chamber wall is coated by fluorocarbon polymer which may slow down the etch rate and affect the etching profile. Thus, a periodical oxygen clean step is added to maintain the etching profile and slightly speeds up the etching process [31].

There are two ways to fabricate a tapered profile as illustrated in Fig. 2.2. The first process is that the sample is firstly etched to have a vertical profile, then the mask is removed, and maskless etching is performed to make a tapered profile. For the maskless etching, the recipe can be either vertical profile etching recipe or tapered profile etching recipe. For vertical profile etching recipe, due to the lack of protection of mask, the silicon structure would be etched laterally and finally results in a tapered profile.

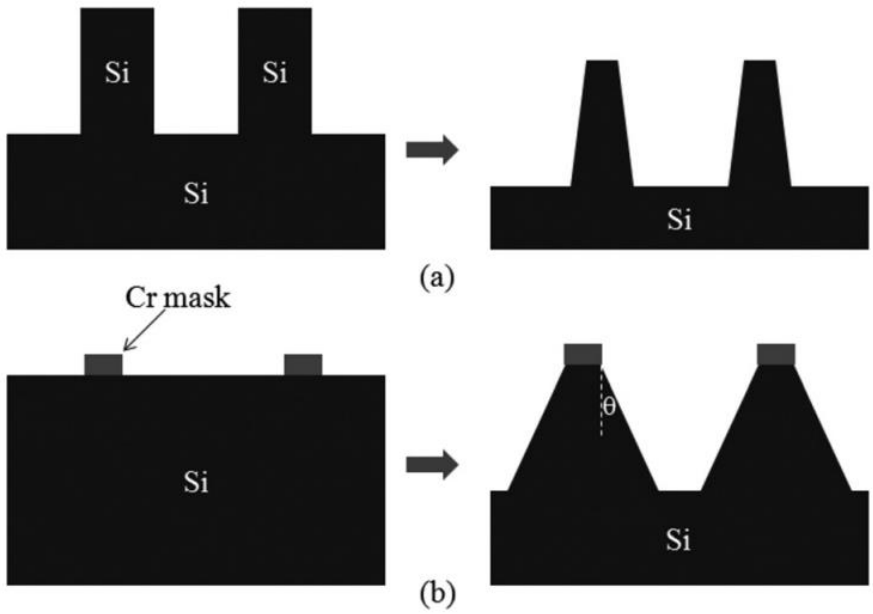

Fig. 2.2 Two processes for the fabrication of tapered structure. (a) Maskless etching of pre-etched silicon structures having a vertical profile, using a recipe that would give a vertical profile when masked. (b) Masked etching with a recipe that can give a tapered profile [32].

Fig 2.3 give an illustration of our etching process for cone shape etching. The sample is first etched with mask to get a primary height. Cr is selected as mask since it holds a good selectivity and has large undercut after etching [33].For the first etching process, the recipe can be either vertical profile etching or tapered profile etching. Then, the Cr mask

is removed by wet etching. Finally, the profile is converted to a cone shape by performing a maskless etching step using a modified non-switching pseudo-Bosch recipe with periodical oxygen clean step.

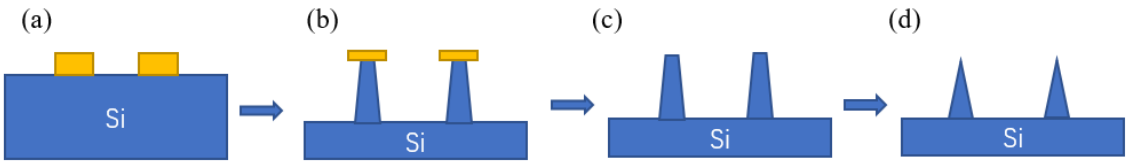

Fig. 2.3 Process flow for the cone shape etching.

2.3. Results and discussion

2.3.1. Tapered Si etching and tapered maskless Si etching

Table 2-1 Parameters for modified pseudo-Bosch recipe with periodical oxygen clean steps. Here the cleaning step is carried out after every 60 sec etching.

Etching step/half cycle		Oxygen cleaning step/half cycle	
C_4F_8 (sccm)	56	O_2(sccm)	20
SF_6(sccm)	4		
RF power(W)	15	RF power(W)	15
ICP power(W)	1200	ICP power(W)	1200
Time(s)	60	Time(s)	7
Temperature (℃)	15	Temperature (℃)	15
Pressure(mTorr)	10	Pressure(mTorr)	10

Table 2.1 shows the detailed parameters of this switching recipe we used to obtain a positively tapered profile. As mentioned before, the gas ratio of C_4F_8/ SF_6 is 56:4, so we

call it “56:4 recipe”. It can provide a 10° tapered profile. Even though it is possible to achieve a larger taper angle by changing the gas ratio of C_4F_8/ SF_6 or RF power, it may also slow down the etch rate. The way to gain a more tapered profile without changing the recipe is the introduction of maskless etching as we discussed before.

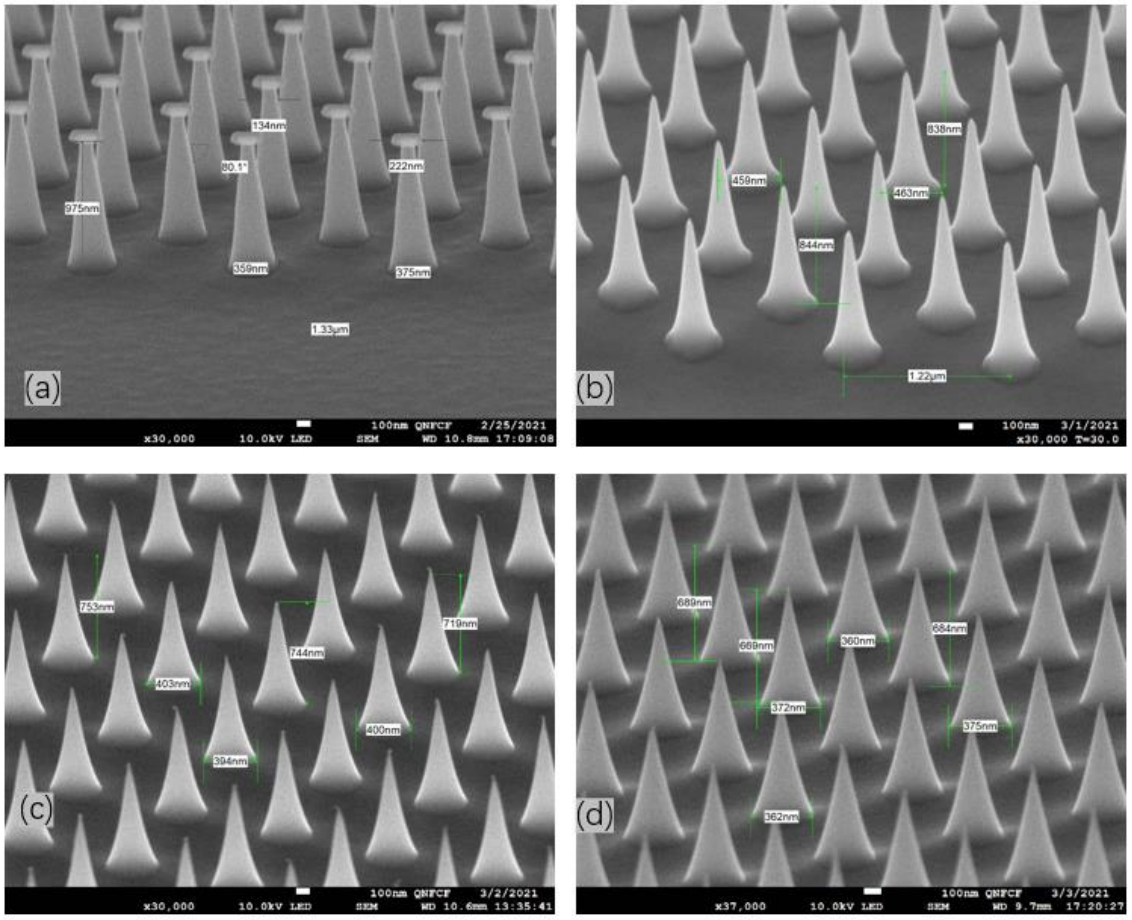

Fig. 2.4 SEM images of positively tapered Si nanostructures using the combination of tapered Si etching and tapered maskless Si etching; (a) 12 cycles 56:4 recipe; (b) Cr wet etching and 5 cycles 56:4 recipe; (c) 10 cycles 56:4 recipe; (d) 5 cycles modified 56:4 recipe @0℃.

Fig. 2.4 shows the results. Since SEM images are taken under 60 degrees tilt or 70 degrees tilt, the real height is slightly larger than measured on the images. Fig 2.4(a) shows the profile after 12 cycles of 56:4 recipe etching. The height of the cone array is aproximately 1040 nm and the taper angle is 10°. There is a large undercut which is close

to 45 nm. The top part is still a flat surface rather than a pointed end. After removing the Cr mask, maskless etching is performed. Fig. 2.4(b) is the results after 5 cycles of maskless etching using the 56:4 recipe shown in Table 2.1. The size of the sample decreased slightly after maskless etching. The top part of the sample is getting sharper. Accoring to the measurement, the taper angle increased from 10° to 12°. Then the sample was continuosly etched with another 10 cycles of 56:4 recipe (Fig 2.4(c)) and 5 cycles of 56:4 recipe@0℃ (Fig 2.4(d)). The top is further shaperned by etching. The taper angle is approximate 16°. For this recipe, the profile is not so sensitive to the temperature. At least, there are no obvious differences between the profile of 0℃ and 15℃. It can be concluded that a larger taper angle can be achieved by maskless etching with this modified pseudo-Bosch recipe.

2.3.2. Vertical Si etching and tapered maskless Si etching

Compared with traditional Bosch process, the above modified recipe has a low etching rate. When the target nanocone array requires a larger height, it is not cost-effective to use such a recipe. This can be achieved by using a vertical silicon etching recipe which holds a higher etch rate, and then do maskless silicon etching by using modified pseudo-Bosch recipe to achieve a sharp top part.

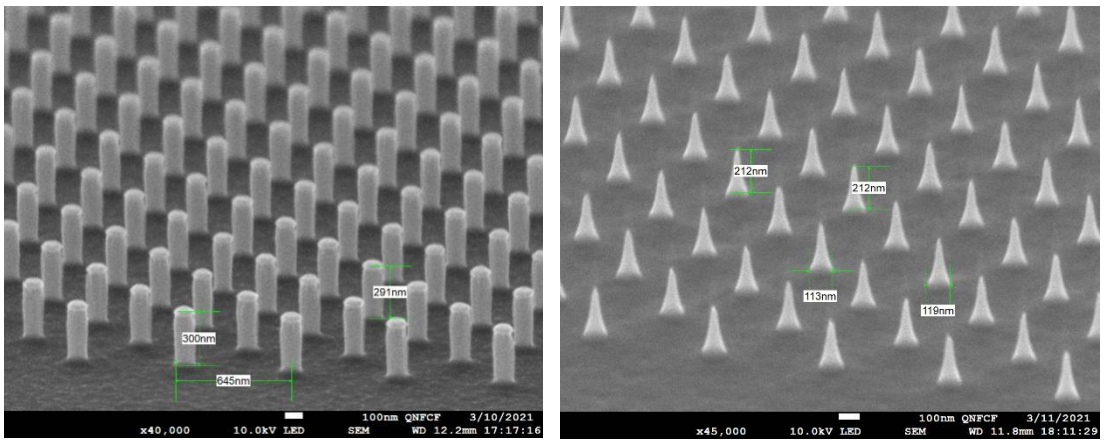

Fig. 2.5 SEM images of cone-shaped Si nanostructures using vertical Si etching followed by tapered maskless Si etching. Left: 1min TempReza Etching; Right: Addition of 2 cycles of 56:4 Etching as shown in Table 2.1.

As mentioned before, when the gas ratio of C_4F_8/ SF_6 is 38:22, it can give a perfect vertical sidewall. The etch rate for this recipe is close to 300 nm/min. The left image in Fig. 2.5 is SEM image of 1 minute etching using this recipe. To achieve a cone shape, the Cr mask is removed. A 2-cycle 56:4 recipe (as shown in Table 2.1) is applied after that. The right figure is SEM image after maskless silicon etching. The height decreases because the sample was etched without the protection of mask. It shows that final structure of the pattern has a taper angle of 15°. It should be mentioned that a cone array results from a wider pillar may require more maskless silicon etching.

2.3.3. The effect of oxygen cleaning Step

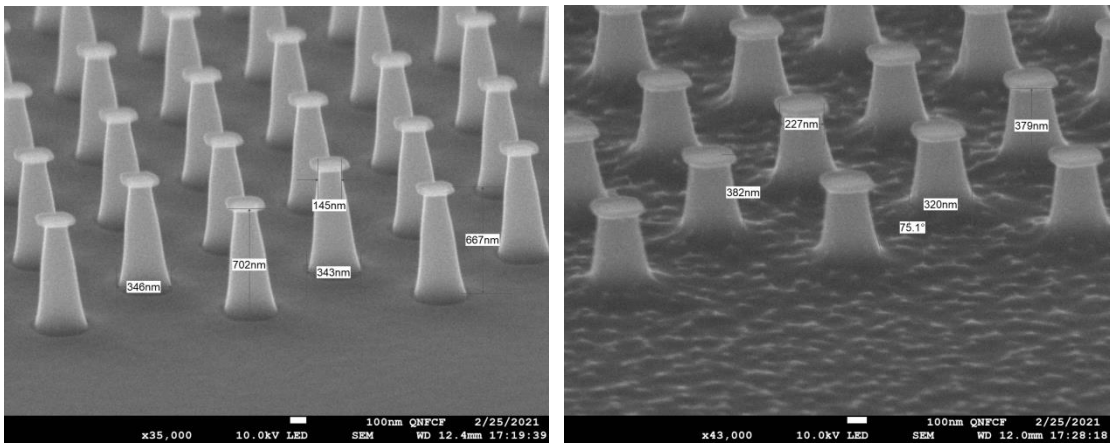

Fig. 2.6 SEM Images of Si pillars after 8 min etching using the recipe shown in Table 2.1. Left: with oxygen cleaning step. Right: without this step.

Figure 2.6 shows the SEM image of nanocone arrays. The left one is etched with 8 cycles of 56:4 recipe. It contains one oxygen clean step after every 1-minute silicon etching as mentioned in Table 2.1. The right one is the sample etched with 8 minutes 56:4 recipe. For this etching process, oxygen clean step is skipped, and only silicon etching step was applied. The silicon etching time for both samples is 8 min. Based on our investigation, oxygen plasma cleaning step of 7 sec will help reach a stabilized pressure during the etching process. Too long oxygen clean results in low slope while too short oxygen clean gives a rough surface.

As shown in Fig 2.6, the surface of the sample without oxygen clean is rough due to the fluorocarbon polymer deposition on the surface. Such fluorocarbon polymer also slows down the etching of the sample. The average etching rate for the recipe without periodical oxygen clean is about 50 nm/min. By introducing the periodical oxygen clean step, the etching rate is increased to 90 nm/min. The result shown in Fig 2.6 also indicates that 7 seconds oxygen clean step after every cycle is efficient to remove the deposited polymer.

In summary, the introduction of periodical oxygen clean step can speed up silicon etching while maintaining a smooth surface.

2.3.4. Effects of pattern density

For this experiment, the cone array has two different pitches: the pitch of sparse array of 1200 nm, and dense array of 600 nm.

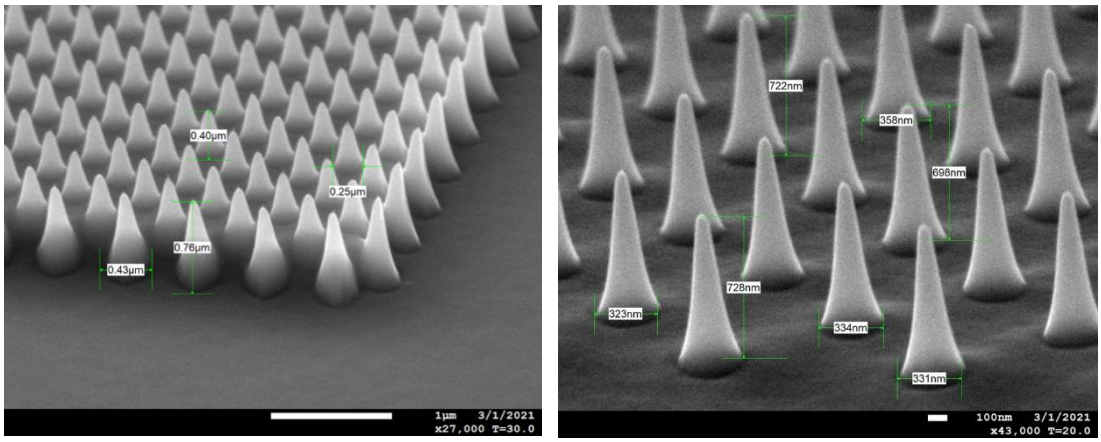

Fig. 2.7 SEM images of small pitch pattern (left) and large pitch pattern (right) after etching.

For these two samples, first they were etched with 12 cycles of 56:4 recipe. Then the Cr mask is removed, and 5 cycles of massless 56:4 recipe etching is applied. Fig 2.7 shows the result for dense and sparse pattern. The cone at the pattern edge of the dense array is taller than that at the central part - the central part for the dense array is not etched fully. A reasonable interpretation is the ARDE (aspect ratio dependent etching) effect. For the edge part, it has larger opening which allows more free radicals and ions to come inside to etch the silicon. If it is loading effect, then the cone at edge should be shorter (not taller) since it has large open etched area nearby that will compete and consume the etchants.

2.4. Summary

In this chapter, a novel way to fabricate an ordered nanocone array is investigated. The combination of taper angle silicon nanostructures etching and maskless etching is performed to obtain a perfect ordered cone array profile. The C_4F_8 gas flow is increased to 56 sccm to achieve an acceptable taper angle which is 10°. Further makless etching can help to make the top part pointier and increase the taper angle to 15°.However, the etching rate for this recipe is relatively low which is only about 50nm/min as etching proceeds. The chamber is contaminated due to large amount of fluorocarbon polymer formation during etching process. The introduction of oxygen plasma cleaning step can remove the polymers and increase the etching rate to 80nm/min. The density of the pattern also affects the etching profile. For 600nm pitch pattern, the inside was not etched completely. ARDE effect may be a potential problem when a dense cone array is needed.

Chapter3. Cone shape fabrication by using SiO_2 mask

3.1. Motivation

It should be stressed that when using chromium as mask during pseudo-Bosch etching, the undercut is very significant. One possible explanation is electric field perturbation effects [34].Thus, oxide masks such as Cr_2O_3 and SiO_2 or photoresists mask can be an alternative way to avoid large undercut. An interesting phenomenon is found that when SiO_2 mask is almost etched away, it will shrink rapidly, resulting in the desired cone shape [35].To investigate this idea, a dot array of SiO_2 mask was fabricated and followed by Si etch with pseudo-Bosch process.

3.2. Experimental

The fabrication step is illustrated in Fig 3.1. The fabrication process starts from bare Si wafer. Acetone and IPA rinse was performed for cleaning. First, one layer of 2 μm SiO_2 is deposited on the wafer by PECVD. Then HMDS coating is applied before resist spin coating. This process can coat substrates with adhesion promoter prior to photoresist coating. Next, one-layer PMGI was spin-coated at 5000rpm and baked at 180 ℃ for 1 minute. After that, S1805 photoresist was spin-coated at 3000 rpm and baked at 120℃ for 90 seconds. Photolithography process was performed using MLA (maskless aligner), for which the light source is 405 nm and dose is 100 mJ/cm^2. After lithography, the sample is developed in MIF 319 for 3 minutes. Then 100 nm Cr is deposited using e-beam evaporation. The sample is put in PG remover for lift-off overnight. After lift-off, the pattern is transferred from S1805 to Cr. Then, plasma etching of SiO_2 is performed to

transfer the pattern from Cr layer to SiO_2 layer. After that, Cr wet etching is preferred to assure that no Cr remains top.

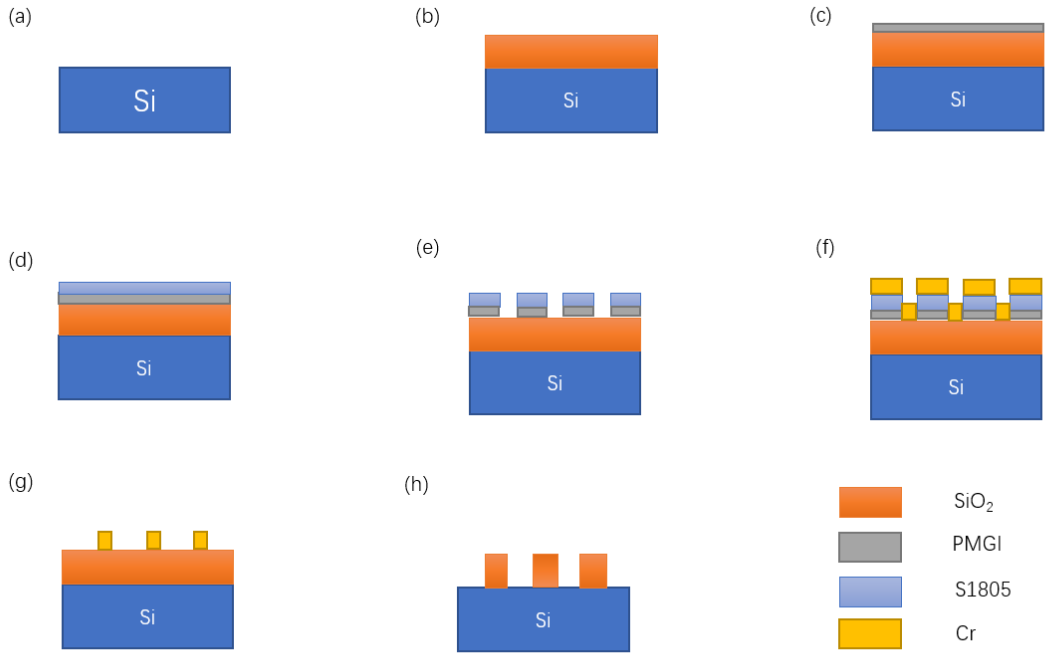

Fig. 3.1 Fabrication process of SiO_2 mask. (a) Bare Si wafer; (b) Deposit SiO_2; (c) Spin coat PMGI; (d) Spin coat S1805; (e) Photolithography and development; (f) Cr evaporation; (g) Lift off; (h) Etching.

The pattern is designed as shown in Fig 3.2. There are four different diameter dot arrays here, which are 0.5 μm, 0.8 μm ,1 μm and 1.2 μm. After development, the 0.5 μm dot array is not developed, and 0.8 μm dot array is only partly developed. Figure 3.3 is the image taken after lift-off process. The reason for the defects of 0.5 μm and 0.8 μm patterns may be the limitation of our MLA, as it is challenging to achieve such a high resolution. For the cone shape etching process, TempReza recipe is used, and some parameters are varied based on the results we have achieved.

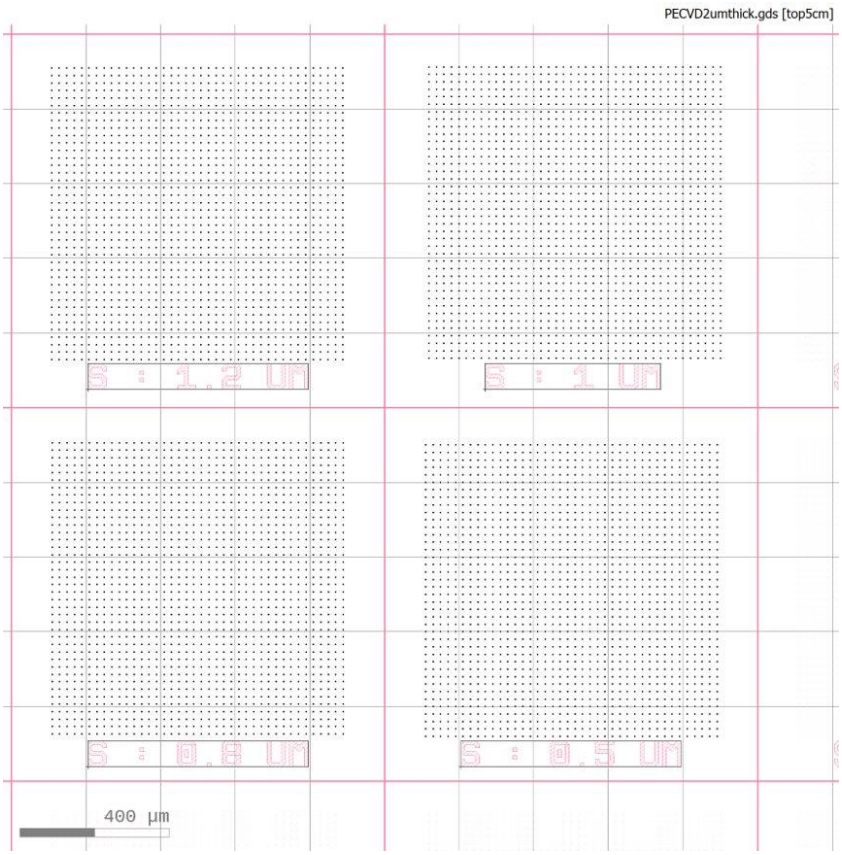

Fig. 3.2 Design of the dot arrays.

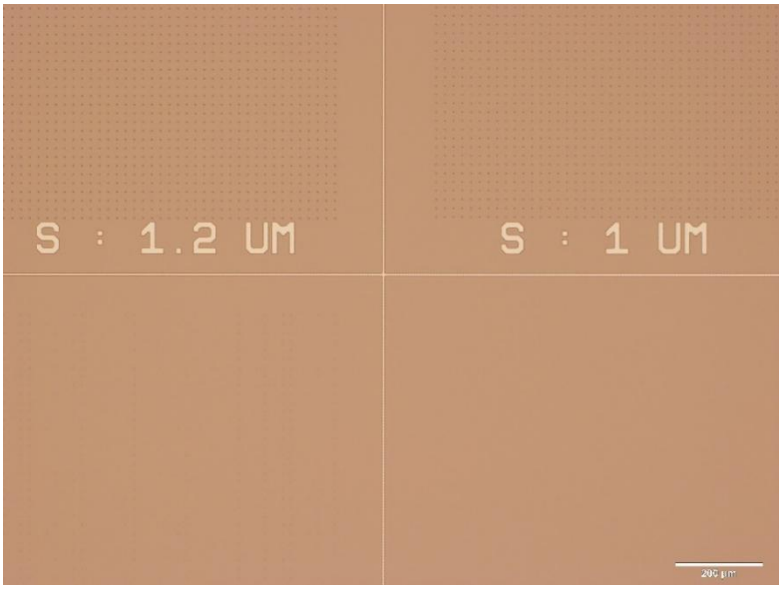

Fig. 3.3 Optical microscope image after Cr lift-off.

3.3. Results and discussion

Fig 3.4 shows the SEM images of silicon nanopillars etched using primary TempReza recipe for 15 minutes. The vertical structure is as expected. Since the remaining SiO_2 is about 500 nm, which is still a lot, SiO_2 mask doesn't shrink dramatically. The ideal situation is that the remaining SiO_2 is less than 100 nm so that it will shrink fast to a cone structure. To achieve such structures, this sample is continuously etched for 10 more minutes.

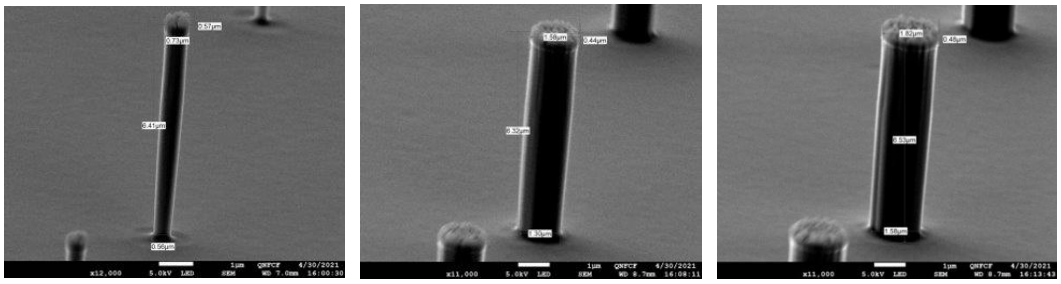

Fig. 3.4 SEM images of Si pillars after 15 minutes TempReza recipe etching. The designed diameters from left to fight: 0.8 μm, 1 μm, 1.2 μm. (The pillars appear tilted because the sample is not well aligned with the scanning direction during SEM imaging)

Fig 3.5 is the results of 25min TempReza etching. The SiO_2 is almost gone. However, the profile is still vertical. It means that the etching process is not as what we expected before.

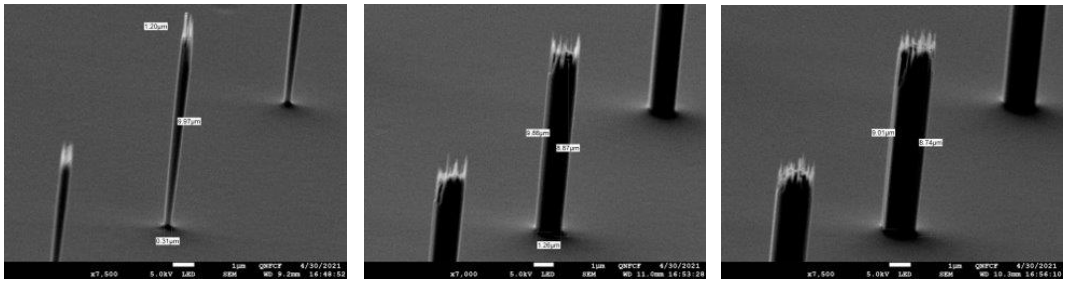

Fig. 3.5 SEM images of Si pillars after 25 minutes etching using TempReza recipe. The designed diameters from left to right: 0.8 µm.1 µm,1.2 µm. (The pillars appear tilted because the sample is not well aligned with the scanning direction during SEM imaging)

To obtain a cone shape, a more anisotropic etching is needed. The general way is to increase the RF power which means to increase the ion bombardment [36].Thus, the RF power is increased from 20 W to 50 W in the following recipe.

The sample is etched for 25 minutes by using the new recipe. As Fig. 3.6 showed, the top part of the pattern is now cone structure. The taper angle is about 40°, which is very large. It should be noted that based on SEM results, no SiO_2 remained on top. A reasonable explanation is that firstly the sample is etched with SiO_2 as mask, which gives a verticle sidewall as is the bottom part. When the SiO_2 mask is almost gone, it shrinks rapidly, and thus a cone structure is obtained at the end of etching. After all the SiO_2 was etched away, a maskless etching may be performed to smoothen the sidewall and tune the structure.

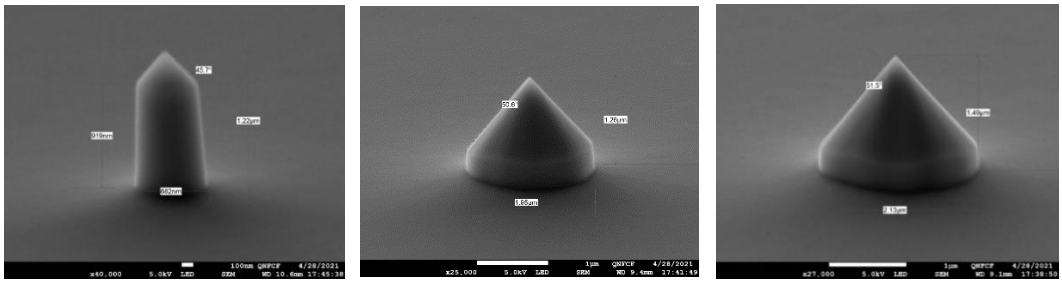

Fig. 3.6 SEM images after 25min TempReza (RF@50W). The designed diameters from left to fight: 0.8 μm, 1 μm, 1.2 μm.

We also tried to increase the ICP power from 1200 W to 2000 W, which can give a higher etch rate for Si and SiO_2. By maintaing RF power at 50 W, 2000 W ICP is used to etch for 15 minutes.

Fig 3.7 is SEM images of 1μm and 1.2μm patterns. It is now a completely cone shape. This result may be explained by the fact that here effectively longer maskless etching is performed due to higher etch rate that etched away all the masks.

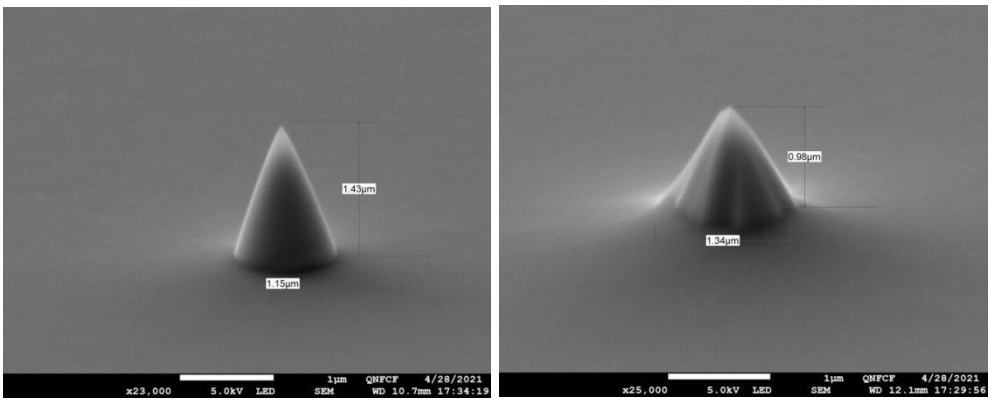

Fig. 3.7 SEM images of cone shape after 15 minutes TempReza (RF@50 W, ICP@2000 W). From left to right: 1 μm, 1.2 μm designed patterns.

3.4. Summary and conclusions

The increasement of ICP power can help with the generation of free radicals which can accelerate the etching process. RF power is associated with DC bias, and higher RF power means larger DC bias and more ion bombardment, which improves anisotropy of etching [1]. In this chapter, based on standard TempReza recipe, we increase the RF power or ICP power to etching the SiO_2 sample. By increasing the RF power to 50W, the final profile is a cone structure which the top part holds a taper angle about 40° and bottom part is little tilted. Increasing the ICP power to 2000W makes the consuming SiO_2 faster. Even the final structure is only 1μm, but the structure is completely cone shape. This section shows that it is possible to achieve a cone shape by optimizing RF power and ICP power. More investigations of the etch rate comparison with different recipes are required to make it more controllable. In addition, the plasma that can etch Si also etch SiO_2, so after the SiO_2 is all etched away, effectively maskless etching will continue, leading to a cone shape.

Chapter4. Cone shape fabrication by shrinking photoresist mask

4.1. Motivation

One can use modified pseudo-Bosch recipe to obtain a cone array by using Cr as mask as mentioned in Chapter 2. However, the etching rate is too low. For microscale cone etching, it is not cost-effective. In the last chapter, a possible way to fabricate cone shape by using SiO_2 as mask is introduced. But it is challenging to control the size and shrinkage. More work needs to be done to make it more repeatable. Since oxygen plasma etching of polymer is more available, one can also use oxygen plasma to shrink the resist mask. This shrinkage is controllable due to mature oxygen plasma etching for polymer; and more importantly, unlike SiO_2 etching that needs the assistance of physical bombardment, resist etching can be spontaneous and pure chemical, without the need of ion bombardment, and thus fast isotropic/lateral etching would be natural. It is worth noting that this way is different from the method which can obtain a tapered profile by controlling the silicon-etching selectivity with respect to the mask [37].The reports for shrinking mask to achieve a high aspect ratio nanocone array provides a good direction [36].The target for this project is to obtain an 8-10 μm high microstructure which top part having a taper angle, as needed for AFM tip fabrication.

4.2. Experimental

The experiment starts from 4-inch Si wafer. The wafer was cleaned in acetone and isopropanol (IPA). For the mask selection, one candidate is polystyrene and another

one is a negative photoresist nLof2035. Both of them have similar properties and the difference is that for polystyrene mask, it requires e-beam lithography, whereas for nLof2035 photoresist, it can be structured by photolithography. Since the pattern is microscale, photolithography is more convenient and can give an acceptable resolution for the features. Here is the illustration of the fabrication process of nLof2035 mask.

Fig. 4.1 Fabrication process of resist structure. (a) Bare Si wafer; (b) Spin-coat nLof2035 photoresist; (c) Exposure and development.

As shown in Fig. 4.1, one layer of nLof2035 is spin-coated on the Si wafer followed by a soft bake process at 110℃ for 1 minute. Then, the pattern is written using MLA with a light source of 375nm. Since nLof2035 is a negative photoresist, it requires post exposure bake to initiate the molecule crosslinking. Thus after exposure, the sample is baked at 110℃ for 1 minute. Next, the sample is developed in MIF 319 for 1 minute. The silicon is ready to be etched after development. The pattern is etched by combining pseudo-Bosch recipe and oxygen plasma shrinking step. There are three different size arrays, which are 2 μm, 2.5 μm and 3 μm in diameter.

Several groups of selectivity test are done before etching the real samples. The purpose of the selectivity test is not only to provide a direction for recipe selection but also to give a guideline for the size of initial resist structure. The recipes for selectivity tests are listed in Table 4.1. The temperature is fixed at 15 ℃ and pressure is 10 mTorr.

Table 4-1 Recipes for selectivity tests.

Recipes	RF power (W)	ICP power(W)	C_4F_8 (sccm)	SF_6 (sccm)
1	20	1200	38	22
2	20	2000	38	22
3	20	1200	50	10
4	50	1200	50	10
5	20	2000	50	10
6	10	1200	38	22

4.3. Results and discussion

4.3.1. Etching selectivity for different recipes

The samples for selectivity test are etched for 10 minutes. The etching rate is measured via profilometer. The etching rate for Si, SiO_2 and photoresist are listed in Table 4.2. From this table, it can be concluded that, by decreasing the RF power, it can decrease ion bombardment and thus increase the selectivity between Si and mask. The increase of ICP power can accelerate the etching process and enhance the selectivity between Si and mask. In addition, the increase of gas ratio C_4F_8/ (C_4F_8+ SF_6) will decrease the etch rate, as well as the selectivity, even though this may give a more tapered profile.

Table 4-2 Results for selectivity tests (ER – etching rate).

Recipes	ER for Si (nm/min)	ER for SiO_2 (nm/min)	ER for photoresist (nm/min)	Selectivity between Si and SiO_2	Selectivity between Si and PR
1	325	135	115	2.4	2.8
2	465	256	170	1.8	2.7
3	60	155	60	0.39	1.0
4	140	180	155	0.78	0.90
5	120	200	110	0.60	1.10
6	405	60	65	6.8	6.2

The thickness of photoresist is restricted between 2.5 μm and 3.5 μm. Even a thicker photoresist can be coated by decreasing the spin speed, the resist pillars were collapsed after lithography due to capillary force during development process [38]. In this case, Recipe 6 in Table 4.1 should be the only choice. It has been noted that this recipe can give a straight sidewall, so the shrinkage of mask is essential to reach a tapered profile.

4.3.2. Resist shrinking using oxygen plasma

For the resist shrinking step, it is favorable to get more laterally etch in order to shrink fast the photoresist pillar diameter. The general way is to increase chemical

etching and reduce ion bombardment that can be achieved under high pressure or low RF bias power [39]. The recipe is shown in Table 4.3.

Table 4-3 Primary recipe of oxygen shrinking step.

Temperature (°C)	Pressure(mTorr)	RF power(W)	ICP power (W)	O_2 (sccm)
15	10	0	1000	20

The original sample is etched for 4 minutes. As shown in Fig. 4.2, the diameter of the pillar decreased approximate by 1.5 μm and the height decrease by 0.8 μm after etching (the original height is 2.7μm). It means that the photoresist mask can be shrunk rapidly using this recipe.

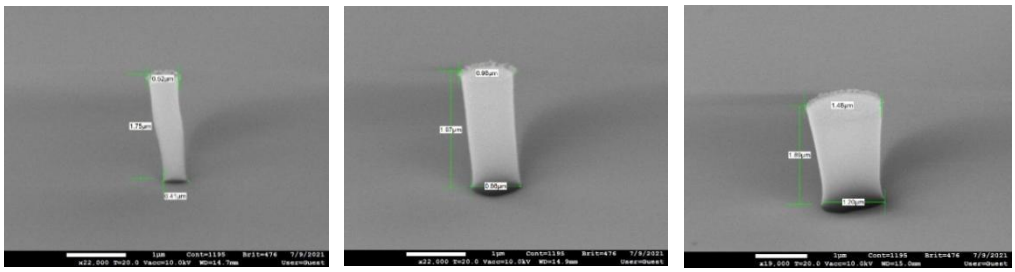

Fig. 4.2 SEM images after 4 min oxygen plasma shrinking. The designed diameters from left to fight: 2 μm, 2.5 μm, 3 μm.

However, when etching the sample by combining pseudo-Bosch Recipe 6 and this oxygen shrinking recipe, the profile is not perfect.

For the etching step, a manual mode is employed where the duration for each step is set manually. Here the etching sequence is: 10 minutes Recipe 6, 2 minutes oxygen shrinking, 5 minutes Recipe 6, 1 minute oxygen shrinking, 4 minutes Recipe 6, 1 minute

oxygen shrinking, 3 minutes Recipe 6, 40 seconds oxygen shrinking, 2 minutes Recipe 6, and finally 20 seconds oxygen shrinking.

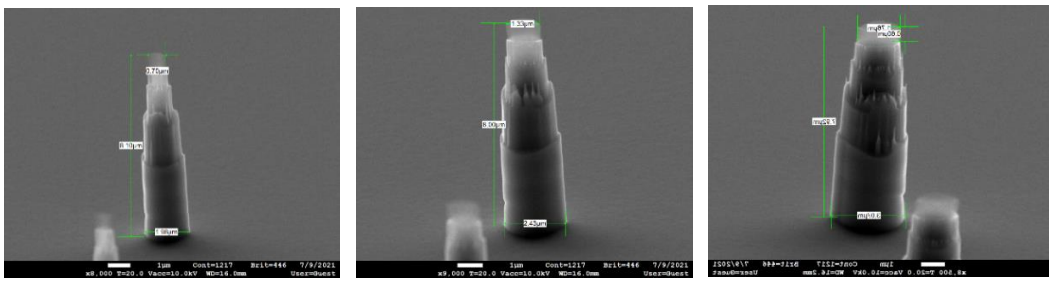

Fig. 4.3 SEM images of Si pillars after etching with manual combination of pseudo-Bosch and oxygen plasma shrinking steps. The designed diameters from left to right: 2 µm, 2.5 µm, 3 µm.

The profiles after etching are shown in Fig 4.3. It has many irregular steps which are caused by the manual control of the etching in different durations. Another serious problem is that there are many spikes/ “grasses” on the sidewall. This problem was solved by increasing RF power of the oxygen shrinking step. Thus, the RF power of oxygen shrinking step is increased from 0 W to 5 W. In addition, to solve the problem of irregular steps, the etching process was set to be a cyclic mode which is similar to Pseudo Bosch process discussed in Chapter 2, namely a main etching step followed by periodical oxygen shrinking step. The difference is that, in the previous recipe the oxygen plasma step is to clean the chamber wall and maintain the etch rate in an acceptable level, but the oxygen plasma step here is to etch and shrink the photoresist laterally. The optimized recipe (we named it “Si etching with periodical oxygen shrink”) is listed in Table 4.4. The temperature is 15 ℃ and pressure is 10 mTorr.

Table 4-4 Parameters for “Si etching with periodical oxygen shrink” recipe.

Etching step		Oxygen shrinking step	
C_4F_8 (sccm)	38	O_2(sccm)	20
SF_6(sccm)	22		
RF power(W)	10	RF power(W)	5
ICP power(W)	1200	ICP power(W)	1000

4.3.3. Etching with pure “Si etching with periodical oxygen shrink” recipe

The etching step is set to be 45 seconds and oxygen shrinking step is set to be 10 seconds. The sample is etched for 30 cycles.

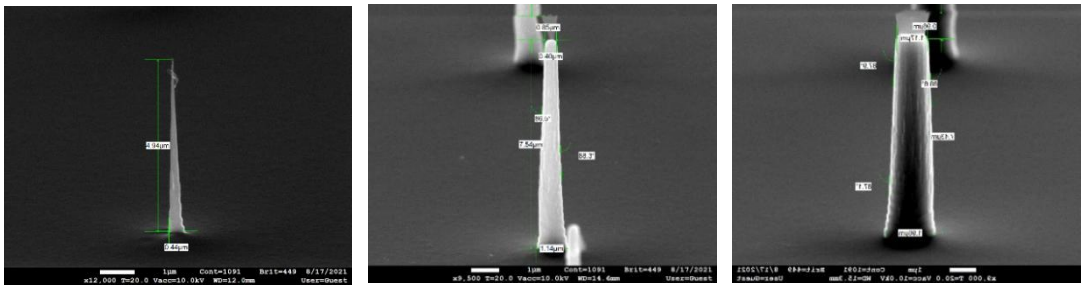

Fig. 4.4 SEM images of Si pillars after 30 cycles Si etching with periodical oxygen shrinking (etch 45 sec, oxygen 10 sec, per cycle). The designed diameters from left to right: 2 μm, 2.5 μm, 3 μm.

Fig 4.4 is the SEM images of Si pillars after 30 cycles etching. For 2 μm patterns, all photoresists on top were etched away. This might result from the severe lateral etch in oxygen shrinking step. The taper angle is not large with nearly vertical profile. One

plausible explanation is that, during the initial etching, the bottom part is protected very well. As etching proceeds, the silicon at lower part without mask protection is etched away laterally, leading to the fast reduction of diameter at pillar bottom.

4.3.4. Etching with Bosch recipe followed by "Si etching with periodical oxygen shrink" recipe

The Bosch recipe can provide a vertical profile, and selectivity between Si and photoresist is very high. For AFM tip fabrication, the positively tapered profile of the bottom part is not required. Thus, a Bosch recipe is employed to etch a vertical pillar for the bottom part. The Bosch recipe is listed in Table 4.5.

Table 4-5 Parameters of Bosch recipe.

Etching Step		Deposition Step	
C_4F_8 (sccm)	1	C_4F_8 (sccm)	160
SF_6 (sccm)	160	SF_6(sccm)	1
RF power(W)	20	RF power(W)	5
ICP power(W)	1000	ICP power(W)	1000
Pressure(mTorr)	25	Pressure(mTorr)	20
Temperature (℃)	15	Temperature (℃)	15
Duration(s)	5	Duration(s)	7

The etching rate for this recipe is close to 140 nm/cycle, and the sample is etched for 35 cycles. As shown in Figure 4.5, the profile is vertical. There is still 3 μm thick photoresist remaining on the top (the original thickness is 3.3 μm).

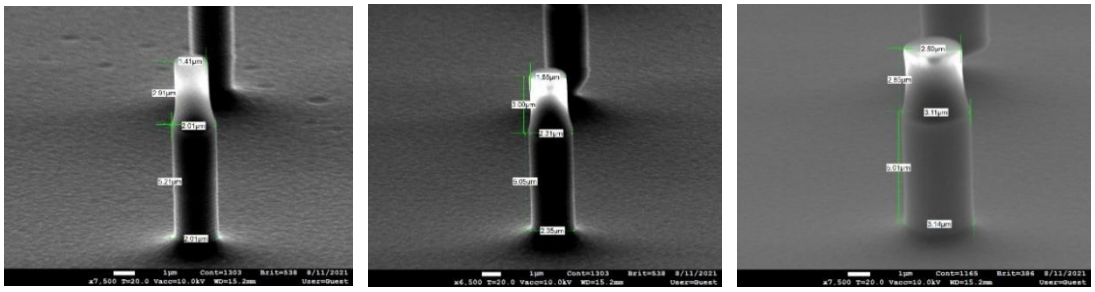

Fig. 4.5 SEM images of Si pillars after 35 cycles of Bosch recipe etching. The designed diameters from left to right: 2 μm, 2.5 μm, 3 μm. Here the resist mask on top is not removed.

After 35 cycles of Bosch recipe, the sample is further etched with “Si etching with periodical oxygen shrink” recipe. The etching time is 30 seconds and the oxygen shrinking time is 10 seconds. 30 cycles “Si etching with periodical oxygen shrink” recipe is applied to achieve a cone shape at top part.

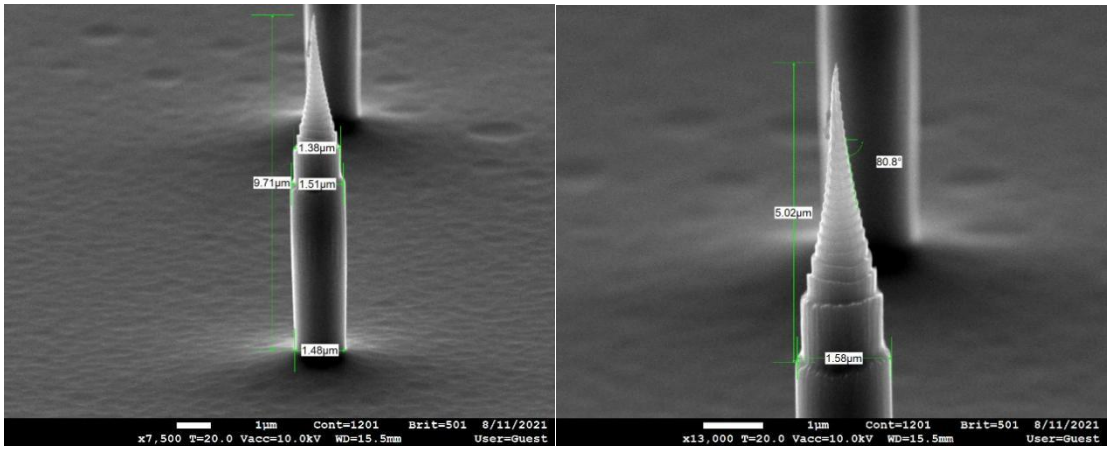

Fig. 4.6 SEM images of Si pillars after 35 cycles of Bosch + 30 cycles of Si etching with periodical oxygen shrinking (etch 30 sec, oxygen 10 sec, per cycle).

Figure 4.6 is the profile of 2 μm pattern. The overview of this pattern showed it has two different parts, the top part is cone shape, and the bottom part is vertical pillar shape, which is just as expected. The scalloping effect caused by Bosch process is eliminated after "Si etching with periodical oxygen shrink" recipe. It is notable that the "Si etching with periodical oxygen shrink" recipe can result in a significant reduction of the pillar diameter. For this pattern, all the photoresist is gone. The top part has a significant taper angle of 9.2°, which is impossible to achieve without the oxygen shrinking step. It can be concluded that the desired profile can be achieved by using the combination of Bosch recipe and "Si etching with periodical oxygen shrink" recipe. To optimize the profile, the adjustment of deposition and etching duration in Bosch recipe is a possible way. Accordingly, the etching duration and oxygen shrinking duration should be changed to maintain the height of the entire pillar.

4.3.5. Further sharpening and smoothening by thermal oxidation of silicon

As mentioned above, the top part etched by cyclic recipe has many steps. These steps can be minimized by dividing the etching process into more cycles. However, there is a limitation of total oxygen shrinking duration due to the lateral etch. One alternative solution is thermal oxidation sharpening [40] [41] [42]. This is a popular way to sharpen silicon tips. Thermal oxidation at atmospheric condition is applied on the sample. The temperature is set to be 1000℃ and the duration is set to be 2 hours. After thermal oxidation, the SiO_2 layer is etched in BOE (buffered hydrofluoric acid), resulting in a sharpening silicon cone structure.

Fig 4.7 is the SEM images of Si pillars before and after thermal oxidation sharpening. Before thermal oxidation, the taper angle is 7°; and after sharpening, it increased to 10°, which is sharper. In addition, thermal oxidation sharpening also help to reduce the top diameter because silicon is consumed and converted into SiO_2. Before thermal oxidation, the top diameter is 435 nm. After 2 hours thermal oxidation and BOE wet etch, the top diameter decreased to 161nm, which is a significant change in nanoscale. Moreover, the sidewall is smoother after the sharpening process.

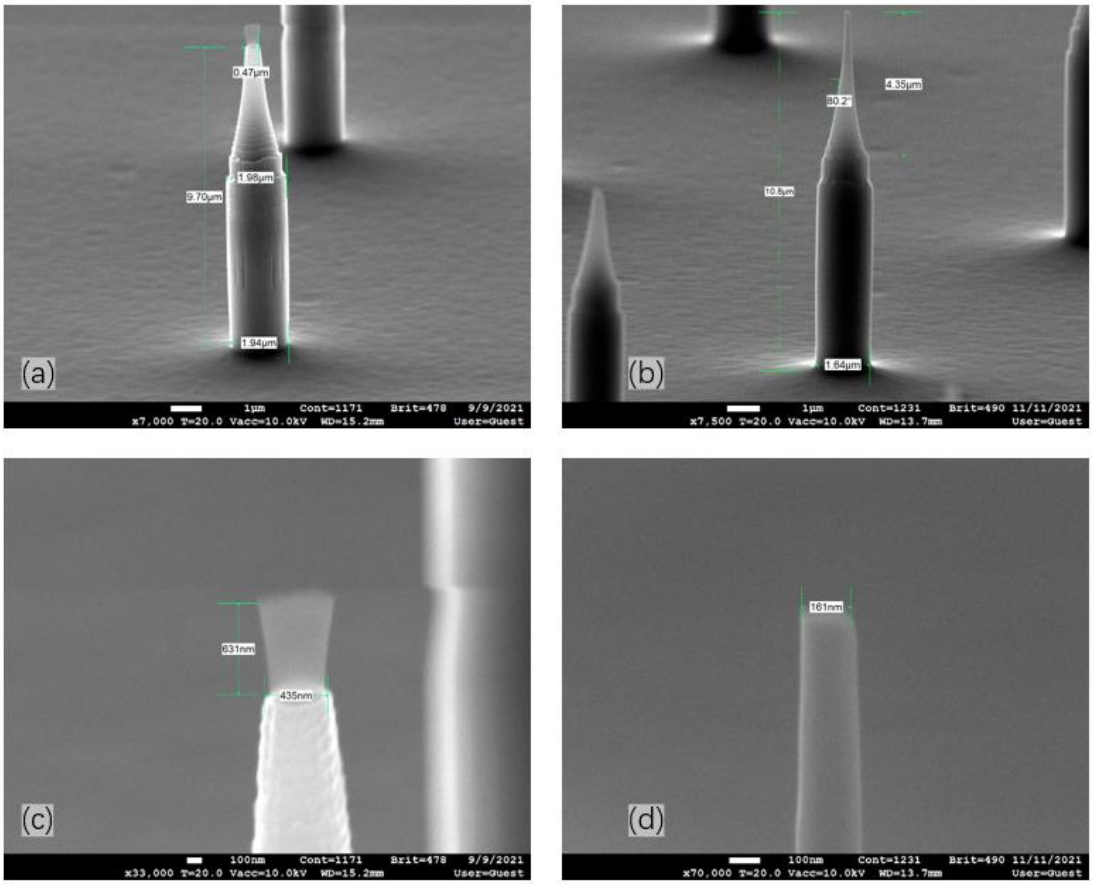

Fig. 4.7 SEM images before (a-b), and after (c-d) thermal oxidation sharpening. Here c-d is the zoom-in image of a-b.

4.4. Summary and conclusions

In this chapter, a detailed fabrication process for microscale cone shapes by using photoresist as mask is elaborated. This method provides a cost-effective way to fabricate AFM tips. For the recipe we create, the selectivity between Si and photoresist is close to 1:6 which makes the microscale cone shape fabrication by using photoresist as mask possible. The etching rate for this recipe is close to 400nm/min. The introduction of the periodical oxygen shrinking step is an important part in this recipe. Low RF power(5W) can result in much lateral etch for photoresist mask. By controlling the total etching time, the height of the structure can be determined. The diameter of the top part is decided by total oxygen shrinking time. By combining Bosch recipe and this recipe, a 10μm height cone array can be obtained. The taper angle of the top part is about 10°. However, similar to the switching Bosch process, sidewall scalloping effect happens. Thermal oxidation sharpening method can be used not only to smoothen the sidewall but also to achieve a more tapered profile with smaller top diameter. In addition, the etching using C_4F_8, SF_6 and oxygen mixture is recently studied [43] [44], and it may be possible to achieve a tapered profile by using C_4F_8, SF_6 and oxygen mixture gas. This may be one possible direction for future etching process optimization.

Chapter5. Room temperature silicon etching using SF_6/O_2 gas

5.1. Motivation

Since non-switching pseudo-Bosch process requires the gas C_4F_8 to form the passivation layer [45], the polymer accumulation during the etching process [46]will cause a critical chamber contamination issue. For cryogenic etching, the main gas is SF_6 and oxygen. The formation of SiO_xF_y passivation layer can protect the sidewall and the remaining SiO_xF_y can be vaporized at room temperature [18]. However, the cryogenic etching need very low temperature that complicate the tool design. The etching with SF_6 gas is completely isotropic [47]. Yet, at room temperature, the addition of oxygen can help form the SiO_x passivation layer, and thus controlling the profile [48]. This chapter mainly focuses on the trenches structure fabrication [49] [50], yet it should also be possible to fabricate both cone array and pillar array using similar recipe. Compared to cryogenic etching, the main drawback for room temperature etching using the same gas mixture is poorer process/profile control and lower etching selectivity to resist and oxide mask.

5.2. Experimental

In this experiment, since the pattern is micro scale, MLA is employed to fabricate the PR structures. There are three different types of masks, which are Cr (metal mask), SiO_2 (oxide mask) and nLof2035 (photoresist mask). The fabrication process is similar to that shown in Fig 2.1, Fig 3.1 and Fig 4.1. The samples are etched by a mixture of

SF_6 and oxygen plasma. A detailed base recipe is shown in Table 5.1. The parameters can be changed based on the desired profiles.

Table 5-1 Base recipe of SF_6/O_2 etching at near room temperature.

	Temperature (°C)	Pressure(mTorr)	RF(W)	ICP(W)	SF_6(sccm)	O_2(sccm)
Recipe	15	25	30	1000	80	40

5.3. Results and discussion

5.3.1. Effects of different gas flow of SF_6

Fig 5.1 shows the result after 1 minute etching. The etching rate for this recipe is very high compared to the pseudo-Bosch recipe. However, some of the mask fell off due to severe lateral etch. Here the oxygen flow is relatively low compared with SF_6, so the SiOx passivation layer during the etching process is not enough to protect the sidewall. In addition, Cr mask leads to a severe undercut. To solve this problem, it is required to reduce SF_6 gas flow.

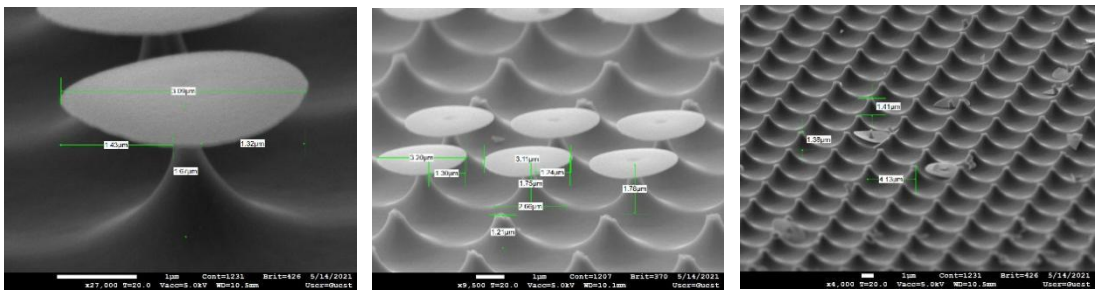

Fig. 5.1 SEM images at three different magnifications after 1 min base recipe etching.

The SF_6 is then reduced from 80 sccm to 40sccm. In addition, the temperature is decreased to 0°C in order to achieve a more vertical profile. As Fig 5.2 shows, the

etching rate doesn't change much. Even some masks still fell off, most of them remained on top. Meanwhile, this recipe gives a smaller undercut which is 1.15μm, as compared to the previous one of 1.3 μm. However, the sidewall and the surface of the sample is rough. Rough surface may be due to inadequate passivation layer formed in this etching process. When etching occurs at the Si surface, heat is produced, further boosting the etching rate at that spot. Such positive feedback makes surface rough.

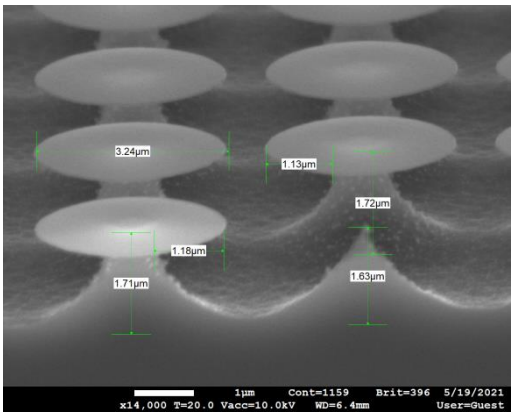

Fig. 5.2 SEM images after 1 min modified recipe etching.

It is possible to further change the gas ratio between SF_6 and oxygen to achieve a vertical profile. Several groups of etching experiment were designed with various flow rates of SF_6 while other parameters remain the same.

Table 5-2 Different etching conditions for different samples.

Sample	RF (W)	ICP (W)	SF_6 (sccm)	O_2 (sccm)	Etching time (min)
Sample 1	50	1000	30	40	8
Sample 2	50	1000	25	40	8
Sample 3	50	1000	20	40	6

For the etching temperature and pressure, they are fixed at 0℃ and 25mTorr.

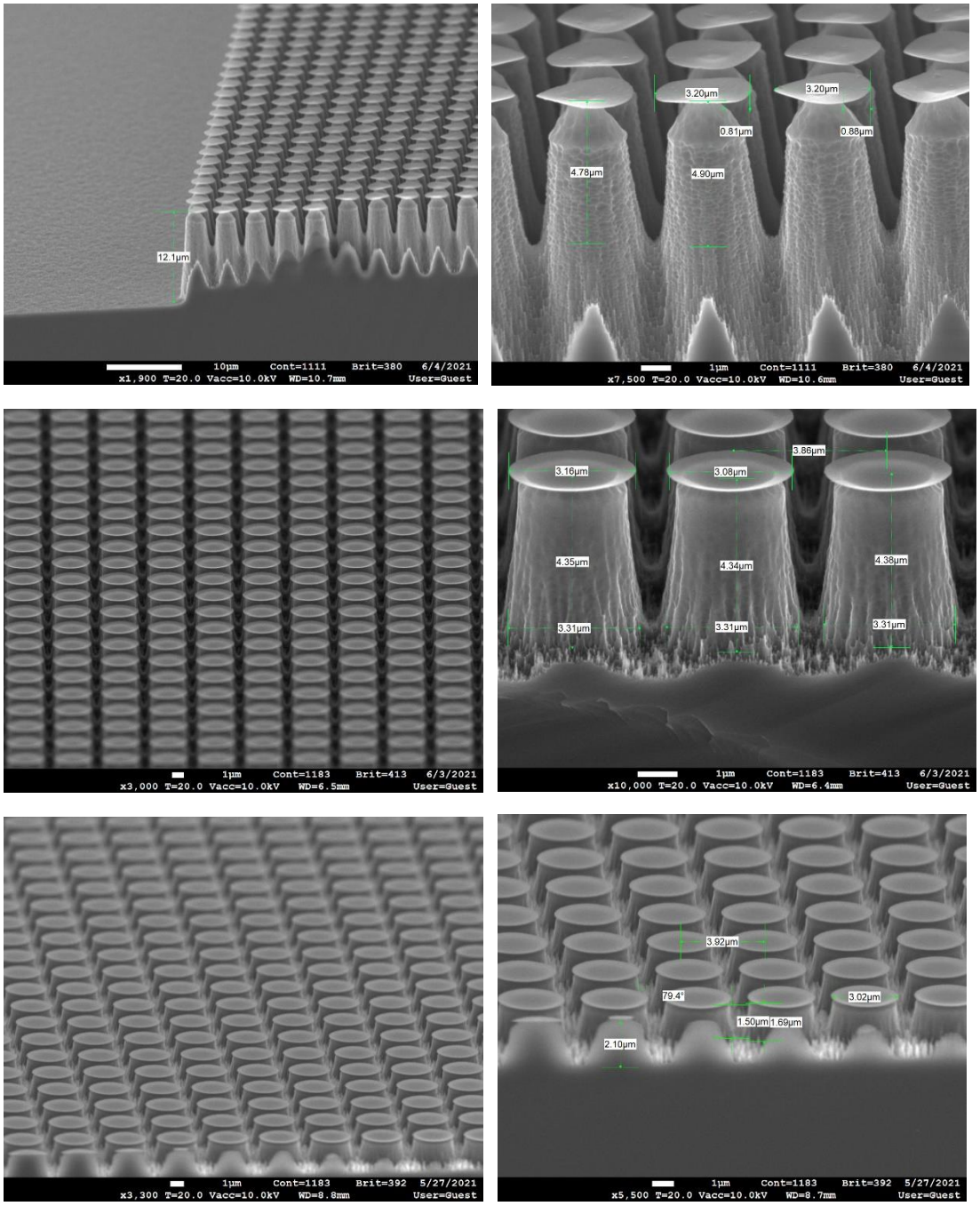

Fig. 5.3 SEM images of Si features after etching. From top to bottom: Sample 1, 2 and 3.

The results shown in Fig.5.3 indicate that the undercut increased while flow rate of SF_6 increased. For sample 1, the etching in lateral direction under the mask is more significant, and even a cone shape is formed at the top. The huge lateral under-mask etching can be explained by the combination of large amount of SF_6 flow and catalysis effect of Cr mask. By decreasing the flow rate of SF_6, a more vertical profile is obtained. However, black silicon (i.e., micro-grass due to micro-masking effect) happened in these experiments. A possible interpretation is that the amount of oxygen in the etching process is excessive thus over-passivation by SiO_x. To remove these black silicon, one solution is to increase RF power and another solution is to reduce the amount of oxygen flow [51]. The increase of RF power will result in a more vertical profile. In addition, during the etching experiment, it is noted that the pressure and temperature did not affect the profile strongly. To keep the machine working more efficiently, it is preferable to set temperature at 15℃, and pressure at 10 mTorr. A perfect vertical profile may be obtained by optimizing the RF power and oxygen flow rate.

5.3.2. Effects of different mask materials and pattern density

As silicon etching process using Cr as mask has a severe undercut, in this experiment, two different types of masks are used: SiO_2 and nLof2035 photoresist. The purpose of this experiment is to investigate the effects of pattern density. In this experiment, 5μm line arrays are used with different pitches which are 7 μm, 9 μm, 13 μm, 15 μm, 20 μm, 25 μm, 35 μm and 50 μm.

Table 5-3 Recipes for line arrays etching

	Temp (℃)	Pressure(mTorr)	RF(W)	ICP(W)	SF_6(sccm)	O_2(sccm)
Recipe	15	10	30	1000	30	30

Table 5.3 shows the details of the recipe. For this recipe, the selectivity between SiO_2 and Si is close to 1:30 while the selectivity between nLof 2035 photoresist and Si is close to 1:7. Compared to previous recipes, RF power is reduced from 50 W to 30 W, and the oxygen flow is decreased from 40 sccm to 30 sccm. It might be favorable to get a more vertical sidewall at lower RF power [52]. The reduction of oxygen flow can solve the problem of black silicon formation [53].

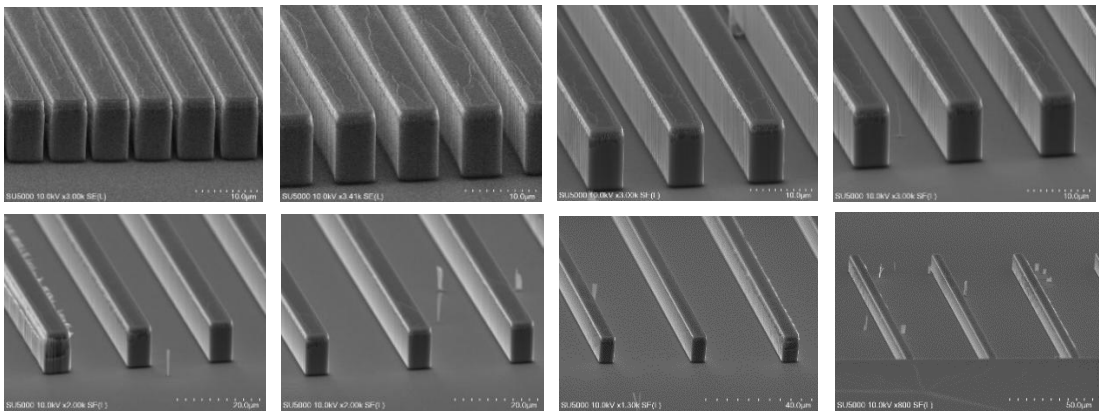

Fig. 5.4 SEM images of line array after 7 min etching using SiO_2 as mask. From left top to right bottom, the pitches are 7 μm, 9 μm, 13 μm, 15 μm, 20 μm, 25 μm, 35 μm and 50 μm.

Fig 5.4 shows the profile after 7 min etching with the mask of SiO_2. As shown in this figure, there is not any black silicon. It is thus proved that the reduction of oxygen can eliminate black silicon. In addition, the profile does not have obvious undercut

compared to Cr mask. It can also be concluded that this recipe can be used not only to etch isolate high pillars, but also to fabricate deep trenches with a straight sidewall.

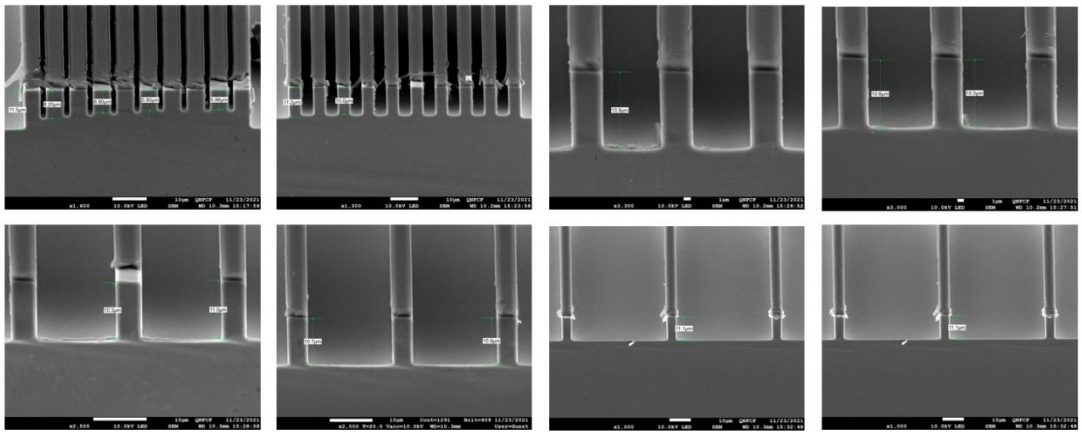

Fig. 5.5 SEM images of line array after 8 minutes etching using nLof2035 as mask. From left top to right bottom, the pitches are 7 μm, 9 μm, 13 μm, 15 μm, 20 μm, 25 μm, 35 μm and 50 μm.

Fig 5.5 shows the profile of Si walls after 8 minutes etching using the mask of nLof2035 photoresist. The cross-section images show that a vertical profile can be obtained for all different pitches. However, it should be noted that for 7 μm pitch patterns, the trenches do not get etched uniformly. The difference between pattern edge and inner part can be explained by ARDE (aspect ratio dependent etching) effect as discussed in Chapter 2. For other pitch patterns, they show similar profile to SiO_2 mask. A comparison of etching profile using these two different masks etching profile does not show a significant difference for trench or isolated line array etching. Present results indicate that a vertical pillar array with least undercut can be achieved by using SiO_2 or photoresist as mask.

5.4. Summary and conclusions

In this chapter, a detailed analysis of fabrication of cone and pillar array is demonstrated. It is possible to use SF_6/O_2 mixture to obtain microstructures at room temperature. Based on current results, the black silicon formation can be avoided by reducing the ratio of $O_2/(O_2+SF_6)$ to 1. However, it should be noted that this ratio is highly dependent on other etching parameters. In addition, the selection of mask affects the degree of undercut. Since this is a non-switching process, the sidewall is smooth without scalloping. The etching selectivity between Si and SiO_2 or photoresist is reasonably high (around 10), though not as high as that of cryogenic etching (several tens of). The etching rate for this recipe is about 1.2 μm/min, which is very high compared with pseudo-Bosch recipe. The surface is always smooth. This etching process provides an alternative way of pseudo-Bosch process to fabricate vertical structures without any concern of contamination by fluorocarbon polymer.

Chapter6. Conclusion and future work

In this thesis, several cone etching methods have been conducted. For nanoscales cone array, the combination of tapered Si etching and maskless etching is feasible to achieve a controllable dimension of patterns as described in Chapter 2. The tapered Si etching is achieved by a non-switching pseudo-Bosch recipe. The increasement of C_4F_8/SF_6 ratio can achieve a larger taper angle while the etching rate is low, and the chamber will be contaminated by F-C polymer deposition. The addition of oxygen plasma cleaning step can effectively alleviate this problem. Also, the increase of RF power can result in a larger taper angle, but the selectivity between mask and Si may be affected. For microscales cone shape etching, it is more favorable to use high RF power or small C_4F_8/SF_6 ratio. As discussed in Chapter 3, the SiO_2 mask will shrink dramatically when it is nearly fully etched and can result in a cone shape. However, this type of shrinkage is not controllable. An alternative mask, nLof2035 photoresist, is introduced in Chapter 4. Photoresist can be shrunk by oxygen plasma. The combination of vertical profile Si etching recipe with periodical oxygen plasma shrinking is introduced in Chapter 4. This method has been proved possible to obtain a cone shape. Since it is a switching process, there are many steps on sidewall, but it can be solved by thermal oxidation sharpening. Due to contamination concern from carbon fluoride polymer, we also investigate SF_6/O_2 etching at room temperature in Chapter 5. It has been shown that it is possible to achieve not only cone shape but also pillar shape by SF_6/O_2 etching. This recipe also holds a satisfied etching selectivity between Si and

other mask material. It can be an alternative way for Bosch and non-switching pseudo-Bosch recipe.

The controllable size of cone shape etching by combining modified pseudo-Bosch and maskless etching is favorable for nanoscale cone shape etching. The process is relative complex, but the structure is more controllable. Such nano scale cone array is always applied in solar cells or photodetectors due to their excellent performance in capturing light. In addition, such small size cone array can also be applied in biology field such as tracking of DNA by coating AuNPs or investigating the mechanical properties of cell membranes. For the cone fabrication by using photoresist mask, the height is always tens of micrometer. Such microscale cones can be used in the fabrication of AFM tip part since it is more cost-effective. The investigation of near room temperature SF_6/O_2 etching makes it possible to be an alternative way of pseudo-Bosch process. This recipe holds the abilities of high etch rate, good selectivity, smooth sidewall, and fine profile control. It can be used for microneedle fabrication. Such device can be used for nanomedicine delivery purpose.

For future research, the combination of near room temperature SF_6/O_2 etching and oxygen plasma shrinking may be another possible way to achieve a micro scale cone array.

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