TiO_2 and Biomaterials based Memristor Devices and its In-Memory Computing Applications

by

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Author's declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

As information technology is moving toward a big data era, the conventional Von Neumann architecture has shown limitation in performance. This is constrained by the large volume of data being continuously fetched and stored through input-output (IO) device, which not only adds performance penalty but power penalty as well. Therefore, it is necessary to bring processing unit as close as possible to memory for minimizing data transmission. Memristors provide dual functionalities of data storage and computing at the same location without data transmission, therefore is one of the most promising candidates for energy efficient in-memory computing. However, being stochastic in nature, variations in memristor device is one of the major challenges in its use towards in-memory computing. In this thesis, we demonstrate novel memristor devices with unique characteristics, which could facilitate reprogrammable application and high-density storage. Further, we demonstrate the applications of the fabricated memristor devices for in-memory computing, with a motive for less sensitive circuits towards variations in devices.

In the first device, TiO_2 and maple leaves (ML) are combined to form a functional layer (TiO_2-ML) inside memristive devices, which demonstrate both the capacitive effect and the non-volatile storage capability. When the voltage increases from zero, the device firstly enters a capacitive-coupled memristive state at low voltage before switch to normal memristive state at a higher voltage. The existence of capacitive coupled and memristive behavior, modulated by programming voltage, forms a unique reprogrammable device. In the second device, formed by Al/TiO_2-Graphene-DNA/Pt layers, high performance and stable intermediate multistate resistive switching behaviors have been achieved. Further, for in-memory computing, a high-density memory and multibit parallel logic computations are realized based on the multistate resistive switching behaviors. This improves data storage capacity and performance up to $2\times$ with respect to conventional single bit memristor devices when they are used to store binary data, without any compromise in accuracy. Further, we use Al/TiO_2/Al memristor device, to demonstrate a variation tolerant analog-digital-hybrid matrix multiplication circuit, for high precision and efficient in-memory computing. It was observed that, in comparison to conventional analog based matrix multiplication scheme using memristor, the proposed scheme improves the average accuracy up to 16.35%, with sacrificing power, performance and area up to 18.5%, 8.2% and 3.2% respectively. This work provides a new horizon on the memristor devices and will improve the understanding of engineering device and circuits for efficient and variation tolerant in-memory computing.

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Chapter 1
Introduction

1.1 In-Memory Computing

1.1.1 Need for New Computing Paradigm

Artificial intelligence and machine learning have proven to provide means for several advanced applications. Recently, various improvements and achievements have been accomplished through deep leaning to implement a wide range of applications such as object detection, face detection, self-driving cars, predictive technology, chat bots, self-learning robots, game playing computers, etc. [1-9]. Although machine learning theories have been developed since 1980s, it was not until the last decade when the field started to boom with an explosive scale of real-world applications. [10-12].

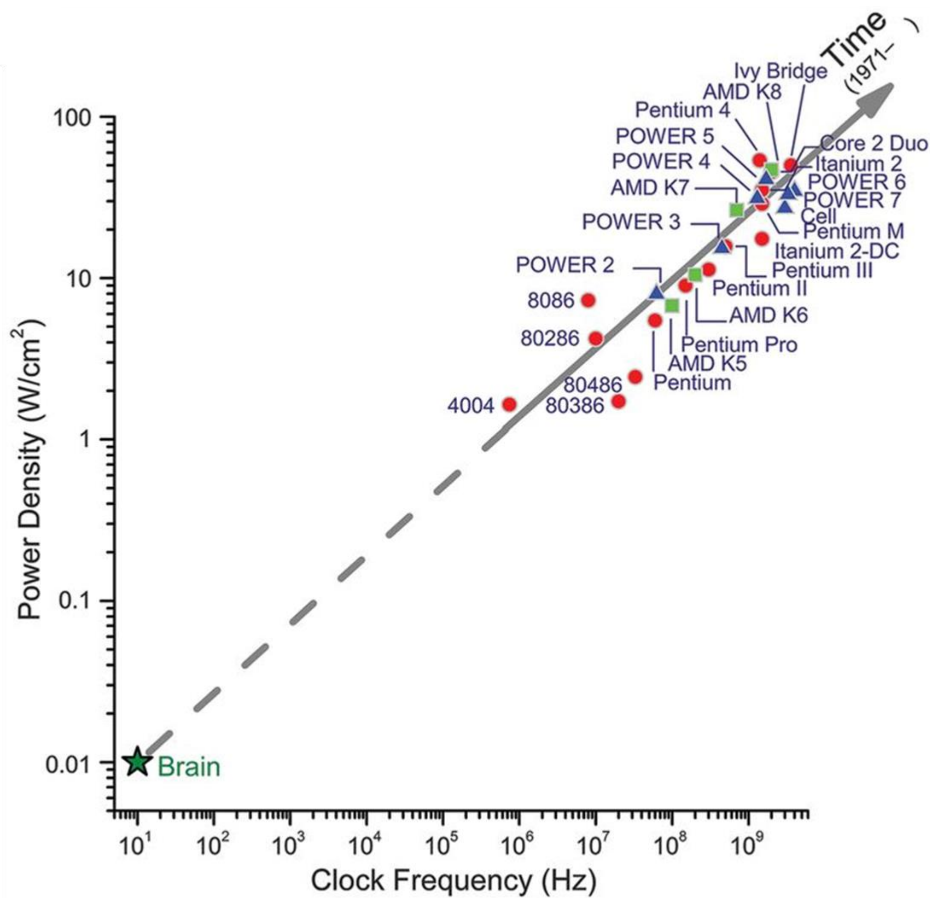


Figure 1.1. The trend of increasing power densities and clock frequencies of processors [13].

One of the key challenges in the early days was inability of hardware machines to support these applications to process large database, often with hundred or more parameters associated with it. Fortunately, continuous CMOS scaling has eventually reached the level to enable the hardware for implementation of deep learning applications.

The CMOS scaling, i.e., the decreasing size of transistor, has been directly associated with the increase in frequency of the processor which in turn can speed up the computation. However, as the frequency of the processor is increased, its power density increases as well. As historical data shown in Figure 1.1 [13], the frequency and power of modern processors have been increasing in a highly correlated manner since 1971. Such trend, however, has started to saturate when Moore's Law eventually comes to an end. Under the current scaling scenarios, with further increase in frequency, the power density would become too large and it is impossible for the chip to cool down by evacuating heat. Therefore, anymore increase in frequency could result in damaging the chip. This is the known as heat wall and is the first limitation in the existing computing paradigm.

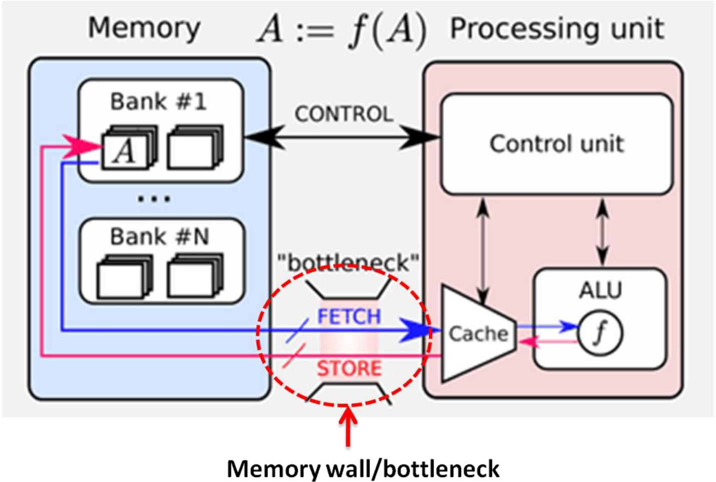


Figure 1.2. Memory wall issue in conventional Von Neumann Architecture [14].

The second limitation of the scaling is shown in Figure 1.2, which is known as memory wall [13,14]. The conventional computers are based on Von-Neumann architecture, where the CPU or the basic processing unit and memory unit are separate. However, in case of data intensive computation such as deep learning, a high volume of data movement between processing unit and the memory is involved, which causes high

latency and power consumption. In addition, as the technology is scaled, the gap between performance of processing unit and memory is widening, as shown in Figure 1.3 [15]. Thus, increasing frequency further adds only little to performance in case of data intensive operation, as processing units needs to sit idle for the time the data is being fetched from the memory.

Hence, the traditional Von-Neumann architecture is no longer efficient moving forward. Novel computing architectures are explored for more advanced applications and faster processing.

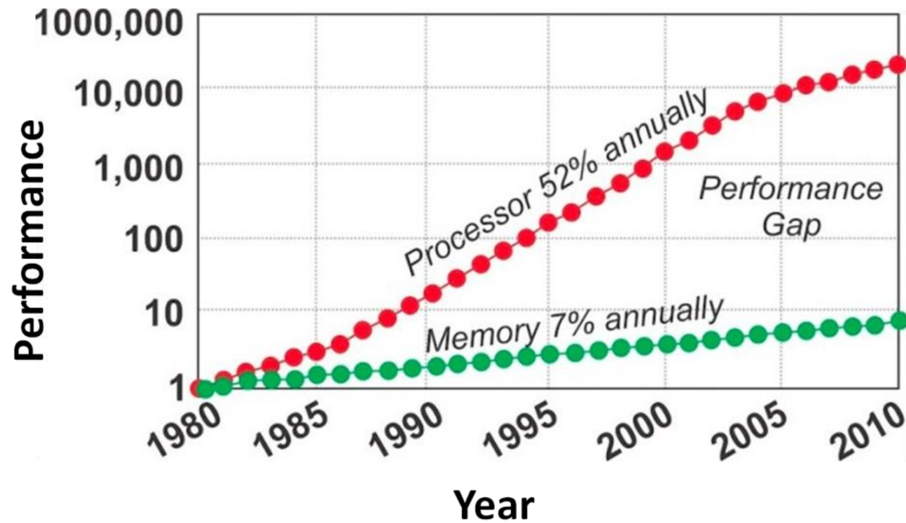


Figure 1.3. Processor Memory performance gap widening trend [15].

1.1.2 In-Memory Computing

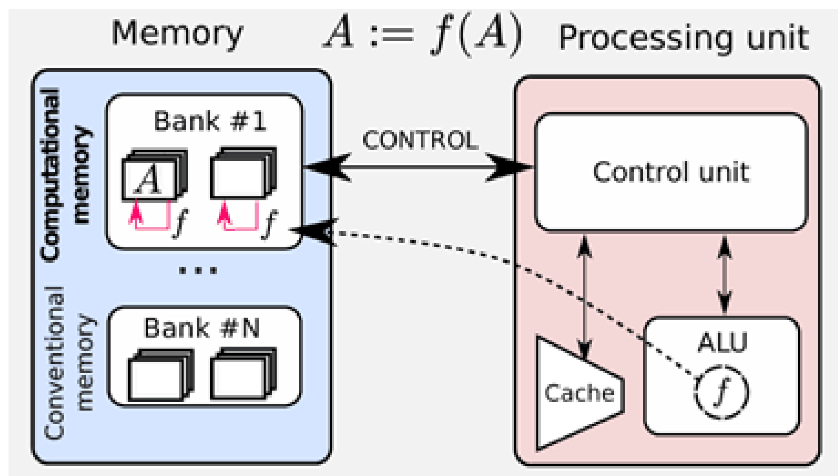


Figure 1.4. In-memory computing paradigm [14].

As illustrated in the Figure 1.1, human brain has much less power density as well as lower frequency of operation comparing with processors based on Von-Neumann architecture, yet it is able to solve very complex problems. One of the key reasons for such efficient operation is that the operation of the brain involves computation and storage of the data in the same region. Therefore, for performing more complex operation more efficiently, it is necessary to shift hardware designs more closer to paradigm of brain. This has inspired researchers to explore in-memory computing architecture, in which computation and memory storage takes within the same unit, as shown in Figure 1.4. These architectures are termed as in-memory computing architectures.

1.2 Memristor

Several emerging nanoscale memory technologies such as memristor, phase change memory, magnetic memory, and ferromagnetic memory have been explored for in-memory computing [16].

The memristor was proposed by L. Chua in 1971 based on missing element in the symmetry of fundamental circuit theory [17]. The classical circuit theory is based on four fundamental quantities (i) current, (ii) voltage, (iii) charge, and (iv) flux-linkage. The resistor, capacitor and inductor relate voltage-current, voltage-charge and current-flux linkage respectively. Therefore, based on symmetry, L. Chua proposed fourth element relating charge and flux, and named it as memristor. Although it was proposed in 1971, the memristor remain unobserved for several decades. It was identified recently in 2008 in HP labs [18]. Memristor devices have many attractive properties such as nanoscale dimensions, low power consumption and non-volatile memory [19-22]. This makes them suitable for many applications such as computer memories, programmable circuits and in-memory computing circuits [16].

Memristor (also known as resistive random-access memory, RRAM or ReRAM), is a combination of two words, memory and resistor. As its name indicates, memristor behaves similar to a non-linear resistor in a sense that it opposes the flow of charge in the same as resistor does. The difference is that the memristor has nonvolatile memory of its states [19]. So, its resistance value changes permanently depending on how much charge has flown through the device. As long as the input signal across the memristor is applied, the device keeps changing its resistance. Once the input signal is removed the memristor will in theory maintain its resistance indefinitely or until input signal is applied again. To change the resistance of the device, appropriate input voltages need to be applied for the appropriate duration of time.

The structure of a memristor device is a simple two-terminal structure where a dielectric layer is sandwiched between two electrodes. The resistance of the sandwiched dielectric layer is controlled by the potential difference applied across it, thus forming a memristor.

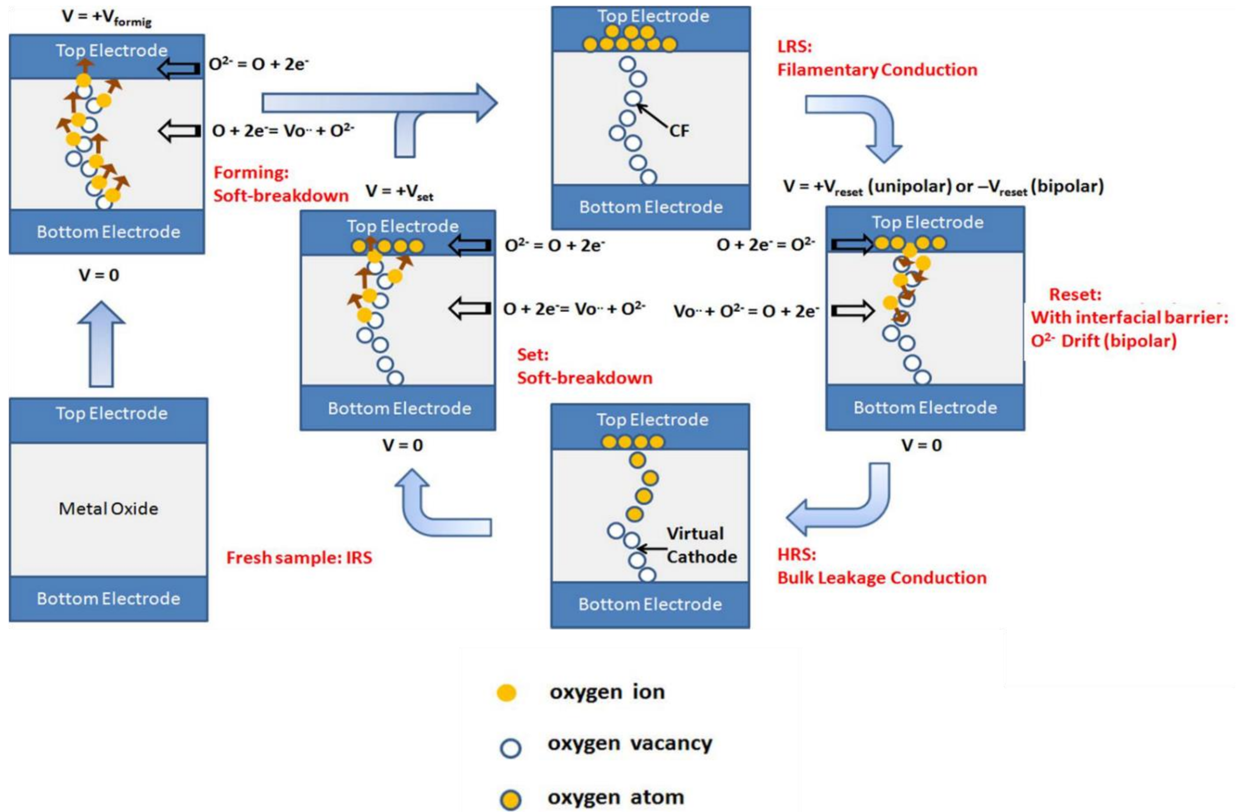


Figure 1.5. Schematic illustration of switching mechanism of memristor [23].

The operation of device can be explained by conductive filament growth and rupture in oxide region with application of potential difference at both the electrodes, as shown in Figure 1.5 [23]. During the one-time electroforming process after the device fabrication, a high voltage, known as forming voltage, is applied to generate mobile oxygen ions through dielectric breakdown. As a result, a conductive filament is formed due to oxygen vacancies in the dielectric layer. During normal write operations, a programming voltage, lesser than forming voltage, is applied between top electrode and bottom electrode to control this conductive filament and thus device resistance. When a negative programming voltage V_{reset} is applied at top electrode with bottom electrode grounded, the oxygen ions migrate back to the oxide layer. Therefore, the conductive filament ruptures and the device behaves as a high resistance device, which is known as high resistance state (HRS) of the device. Similarly, when a positive programming voltage V_{set} is applied at top electrode

with bottom electrode grounded, the conductive filament grows back again and the device behaves as a low resistance device, which is known as low resistance state (LRS) of the device. To read the resistance state of the device, a read voltage V_{read}, ($V_{\text{read}} < V_{set}/2$; $V_{\text{read}} < V_{reset}/2$) is applied across the device to sense the read current.

An ideal memristor should have large I_{LRS}/I_{HRS} ratio ($>10^2$) i.e.., the ratio of read current when the device is in LRS (low resistance state) to that when the device is in HRS (high resistance state) [16,23-25]. Additionally, an ideal memristor should have high endurance (i.e., device characteristics should not change with several set and reset cycles) and retention (i.e., the device should be able to retain resistance state for a long period of time) ability. It has been shown that very high level of endurance (120 billion cycles) and retention (> 10 years) have recently been achieved in memristor device [16].

1.3 Scope of Research

One of the major hurdles for the use of memristor is its stochastic nature including cycle to cycle variations and device to device variations. This has limited the use of memristor yet to be commercialized even though posing enormous benefits. Moreover, there still remains a lot from a materials point of view to be explored in order to achieve better performance and more stable device, especially using biomaterials, which provides a cleaner source of fabrication for the memristor device.

In this thesis, we will try to address these issues in in-memory computing using memristor devices. The thesis will cover development of memristor device using maple leaves as biomaterials. Further, we will explore the use of DNA along with graphene, for the fabrication of memristor device and its application towards development of high-density memory and parallel logic circuits. Lastly, we will discuss novel circuits for performing matrix multiplication using memristor, with the proposed design being more tolerant towards stochastic nature of the memristor device.

1.4 Organization

The thesis is divided in four main chapters. The Chapter 2 covers brief review about the related work about memristor devices and its applications in in-memory computing. In Chapter 3, memristor device development using maple leaves as a part of functional layer and the behavior of the device under different voltage range will be discussed. In Chapter 4, high density memory and parallel in-memory logic operations using memristor based on DNA as biomaterial functional layer along with graphene and TiO_2 will be presented. In Chapter 5, novel analog-digital-hybrid matrix multiplication scheme to counter stochastic

nature of the device will be discussed based on memristor with TiO_2 as functional layer. The Chapter 6 summarizes the research work and proposes the future work.

Chapter 2
Related work

2.1 Introduction

Since the discovery of memristor device in 2008 by HP, a wide range of materials have been explored to improve the device stability, behavior, endurance, and fabrication methods. Recently, a lot of work has also been particularly devoted towards fabrication of memristor using biomaterials for its easy availability, cheaper fabrication method and environment friendly source. From the circuit and system levels, memristor devices have been widely explored for its applications in in-memory computing. In this chapter, we will discuss briefly about previously explored materials for the memristor in section 2.2, followed by various applications of the memristor in in-memory computing in section 2.3.

2.2 Development of Memristor Device

The structure of a memristor device is a simple two-terminal layered structure, where an oxide layer is sandwiched between two metal electrodes, as shown in Figure 2.1. However, the selection of materials and the fabrication method plays an important role in the device characteristics.

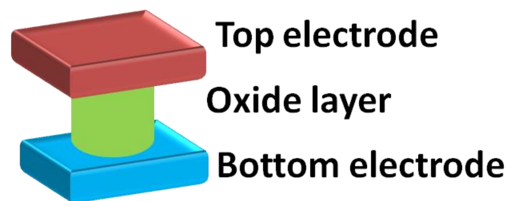


Figure 2.1. Structure of memristor device.

The materials for the oxide layer can be a single uniform oxide layer or a combination of multiple oxide layer. Broadly, the oxide layer can be categorized as inorganic layer, and organic layer, which are discussed in following section 2.1.1 and 2.1.2 respectively.

2.2.1 Memristor based on Inorganic Materials

A number of inorganic metal oxides have been observed to show memristive behavior, with majority of them are transition metal oxides, and few are lanthanide series metal oxides [23]. It has been observed that among different oxides, Cu_2O and WO_3, shows most compatibility with the conventional CMOS devices

because a single additional oxidation stage of the Cu or W via/plug is required respectively [23]. The deposition methods of these inorganic metal oxides usually include the ALD (atomic layer deposition), PLD (pulse laser deposition), reactive sputtering, and oxidation of a corresponding metal.

TiO_2 is one of the initial materials to be explored for the memristor application. Yang et al. fabricated 50nm x 50nm Pt/TiO_2/Pt memristor devices, which exhibited stable switching behavior [26]. Strukov et al. explained that the switching mechanism of the Pt/TiO_2/Pt device is based on the movement of the positive charged oxygen vacancies [18]. HfO_2 is also an excellent memristor material and its explored widely for its application in memristor technology. In the primary stage of HfO_2 based memristor investigation, the TiN/HfO_2/Pt structure is typically used to achieve the memristive characteristics [27].

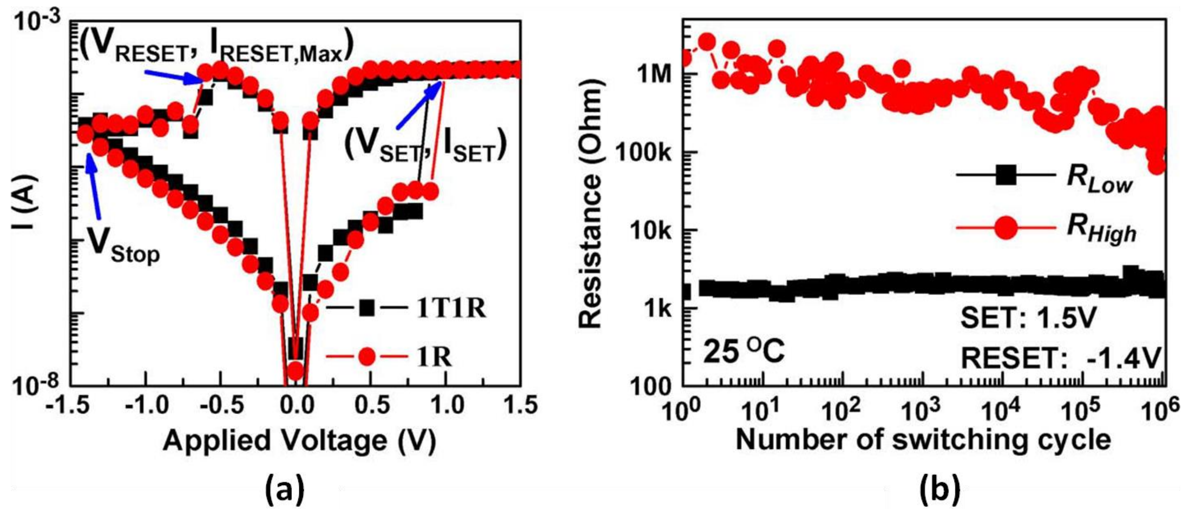


Figure 2.2. TiN/TiO_2/HfO_2/TiN memristor behavior (a) I-V characteristics. (b) switching endurance [28].

H. Lee et al. used combination of TiO_2 and HfO_2 as oxide layer for the fabrication of memristor. The typical I–V curve and the variation in resistance with switching cycle for the fabricated memristor, is shown in Figure 2.2 [28]. The resultant TiN/TiO_2/HfO_2/TiN memristor with high-speed operation showed large I_{LRS}/I_{HRS} ratio (> 100), reliable switching endurance (> 10^6 cycles), long high-temperature lifetime, and high device yield (~100%).

Among other materials, Al_2O_3 based memristor behaves very similar to that of HfO_2 based memristor in many characteristics. Additionally, Al_2O_3 based memristor also showed unique characteristics

of the low reset current [23]. Using Al/AlO_2/Pt memristor device, Wu et al. first demonstrated low reset current down to ~1 uA [29]. Further, Kim et al. doped the AlO_2 with nitrogen and achieved even lower reset current (< 100 nA). The low energy/power consumption of AlO_2 based memristor is a striking feature [30].

2.2.2 Memristor based on Organic Materials

In comparison to memristor with inorganic oxide layer, the oxide layer based on biomaterials are relatively less stable, have lower endurance and lower I_{LRS}/I_{HRS} ratio. However, the major advantage of using biomaterials for the fabrication of memristor is its easy availability, cheaper cost of fabrication and environmentally friendly source [16,31].

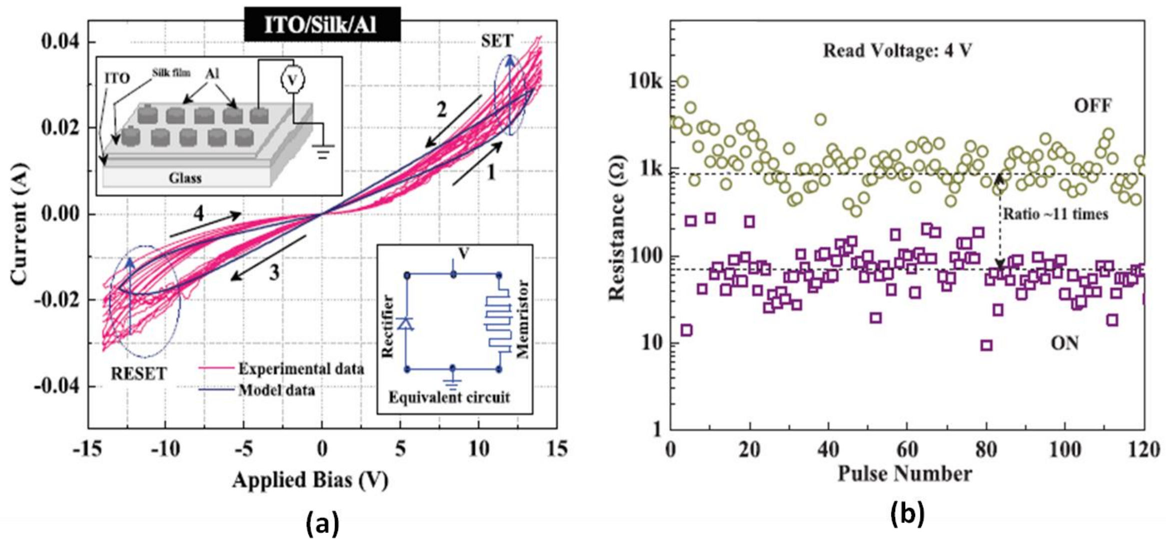


Figure 2.3. Silk based memristor behavior (a) I-V characteristics. (b) Endurance test [32].

Hota et al., demonstrated fabrication of memristor based on biomaterials using natural silk cocoon fibroin protein of silkworm, Bombyx mori [32]. Additionally, the film developed was transparent across most of the visible spectrum. ITO and Al were used as top and bottom electrode. The I-V characteristics of the device is shown in Figure 2.3a. The endurance test of the device is shown in Figure 2.3b. It can be clearly observed that in comparison to device based on complete inorganic oxide layer (shown in Figure 2.2), device based on biomaterials shows lesser endurance with cycle, and has lower I_{LRS}/I_{HRS} ratio.

B. Sun et al., demonstrated fabrication of memristor with natural biomaterials made from spider silk (fibroin) developing Ag/Fibroin/Au structure, where the device showed I_{LRS}/I_{HRS} of 60 [33]. Chen et al., fabricated memristor with egg albumen film Al/egg white/ITO structure, where the device showed I_{LRS}/I_{HRS} > 10^3 [34].

Mao et al., demonstrated environmentally friendly and sustainable bio-memristor device with Ag/walnut skin (WS)/ITO structure. Interestingly, the fabricated device exhibited an overwhelming capacitance effects in the bio-memristor device [35]. Xingli He et al., demonstrated use of Egg albumen as the dielectric, and dissolvable Mg and W, as the top and bottom electrodes, respectively in order to produce water soluble memristors [36]. The device showed I_{LRS}/I_{HRS} ratio in the range of 10^2~10^4. It was further demonstrated that the Mg and W electrodes, and albumen film all can be dissolved in water within 72 hours.

Ham et al., demonstrated tunable memristor using light illumination [37]. The fabricated device consisted of organolead halide perovskite (OHP) as dielectric layer, in which the resistance state is modified by both electrical pulses and light illumination. Owing to the accelerated migration of the iodine vacancy inherently existing in the coated OHP film under light illumination, the OHP based device exhibited light-tunable resistivity functionalities with very low programming inputs (≈0.1 V).

Ku et al., reported the use of organic-inorganic hybrid perovskite materials for the fabrication of Ag/$MAPbI_3$/FTO memristor [38]. Further they demonstrated the use of fabricated device for neuromorphic computing. The results showed that the with energy consumption of the $MAPbI_3$-based memristor to be estimated as low as 47 fJ/um^2, which as close as human brain.

The conduction mechanisms observed for the memristor based on organic materials remains same as memristor based on inorganic materials (formation and rupture of conductive filaments), which was confirmed by SEM imaging [16,23,31]. Generally, for the deposition of biofilm, spin coating method was used in above cases, which makes the fabrication step very easy [32-35]. However, the inability to control film thickness and maintaining film uniformity using spin coating deposition, is one of its major drawbacks. Therefore, the device shows lesser endurance and retention ability in comparison to inorganic oxide films. However, other than cheaper fabrication and maintaining cleaner environment, the organic materials based memristor also adds extraordinary features to the device, which makes it noteworthy to be investigated further.

2.3 Applications of Memristor for In-Memory Computing

As discussed in chapter 1, in-memory computing is to perform computation within the memory blocks. As shown in Figure 2.4, there are several aspects related to computations within the memory [16]. In this section, we will briefly examine the different digital and analog computing schemes that have been proposed. The most important element of in-memory computing is development of high-density memory architecture. We will discuss various recent advancements in 2D, and 3D memory architectures based on memristor devices in section 2.3.1. For in-memory digital computing, in-memory logics are also being explored for implementation of general logic computation within the memory. Memristor provides various alternative to carry out digital Boolean operations, which will be briefly reviewed in section 2.3.2. One of the other important innovations in in-memory computing is the development of hardware based neural networks and deep learning within the memory, which deals in TBs of data. The hardware implementation of such in-memory computing based machine learning applications, has shown promising results in terms of performance improvement and power reduction in comparison to Von-Neumann architecture [16], which will be discussed in section 2.3.3. In section 2.3.4, brain inspired computing or neuromorphic processors within the memory will be discussed, which relies on fundamental principal of working of brain, and is one the major focus of recent study on in-memory computing.

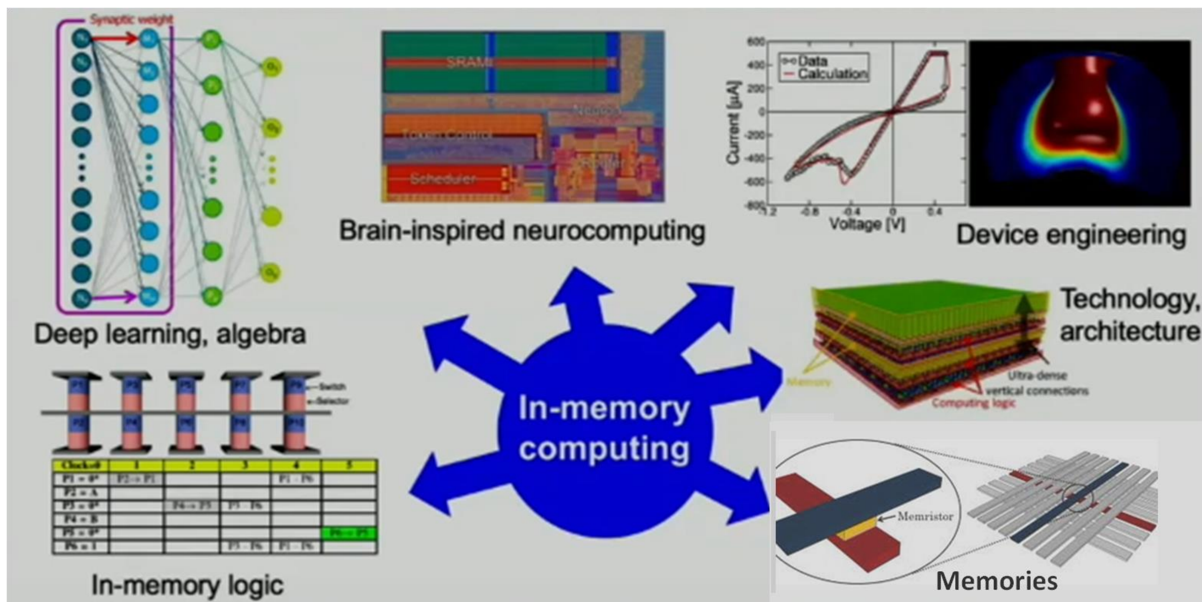


Figure 2.4. Aspects of in-memory computing [16].

2.3.1 Development of High-Density Memory

The memristor device is widely explored as non-volatile memory in various computing architectures, largely due to its smaller area, high packing density, low power, high switching speed and its compatibility with conventional CMOS device. The data is stored in form of resistance state of the device. Broadly, the use of memristor as non-volatile memory can be categorized as analog memory and digital memory.

Generally, a crossbar structure is utilized for memory using memristor, where top electrode forms the word line and bottom electrode forms the bit line, and the memristor device is formed at junction of each wordline and bitline. For digitally storing data in memristor, 0s and 1s are stored in form of HRS and LRS respectively [39-42]. For writing data, a V_{set} or V_{reset} potential difference is applied across the device through word line and bit line. For reading the data, a V_{read} pulse (generally lower than $V_{set}/2$ and $V_{reset}/2$) is applied at the word line and current flowing through bit line is sensed to determine the stored resistance state of the device [44].

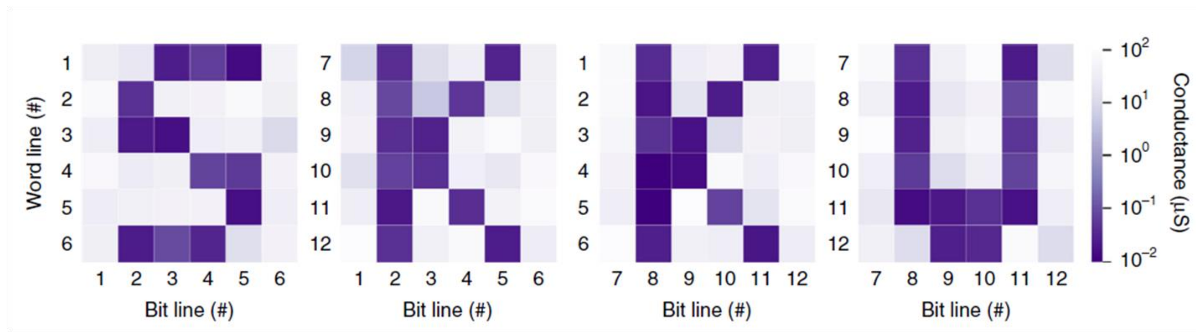


Figure 2.5. The colour map of the readout conductance with a reading voltage of 3 V using memristor based on hexagonal boron nitride and graphene [44].

However, it has been demonstrated that memristor could be used in more efficient manner in an analog way, where more information can be stored in a single memristor. In this, intermediate resistance states are being explored to store data. The use of memristor in analog way helps in reducing the area of the memory significantly [44, 45].

L. Sun et al., demonstrated use of memristor as memory in an analog way as shown in Figure 2.5, where a 12x12 crossbar structure was used to store data in form for conductance. The device used for the demonstration based on hexagonal boron nitride and graphene, with I_{LRS}/I_{HRS} ratio larger than 10^3 [44]. However, the use of memristor as memory in analog way also creates issue of precision during memory write operations due to stochastic nature of memristor device [46-48].

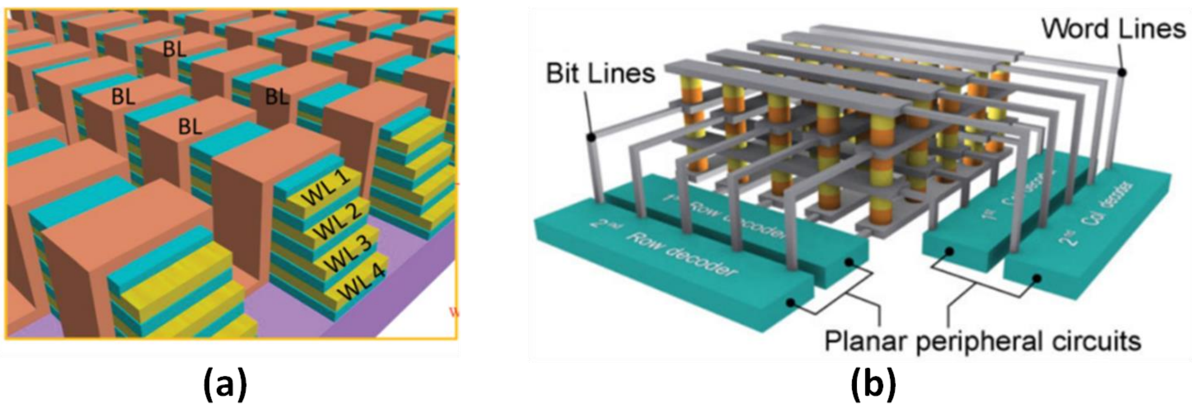


Figure 2.6. (a) The schematic of 3D vertical memristor array [49]. (b) The schematic of stacked memristor based memories with peripheral circuit [50].

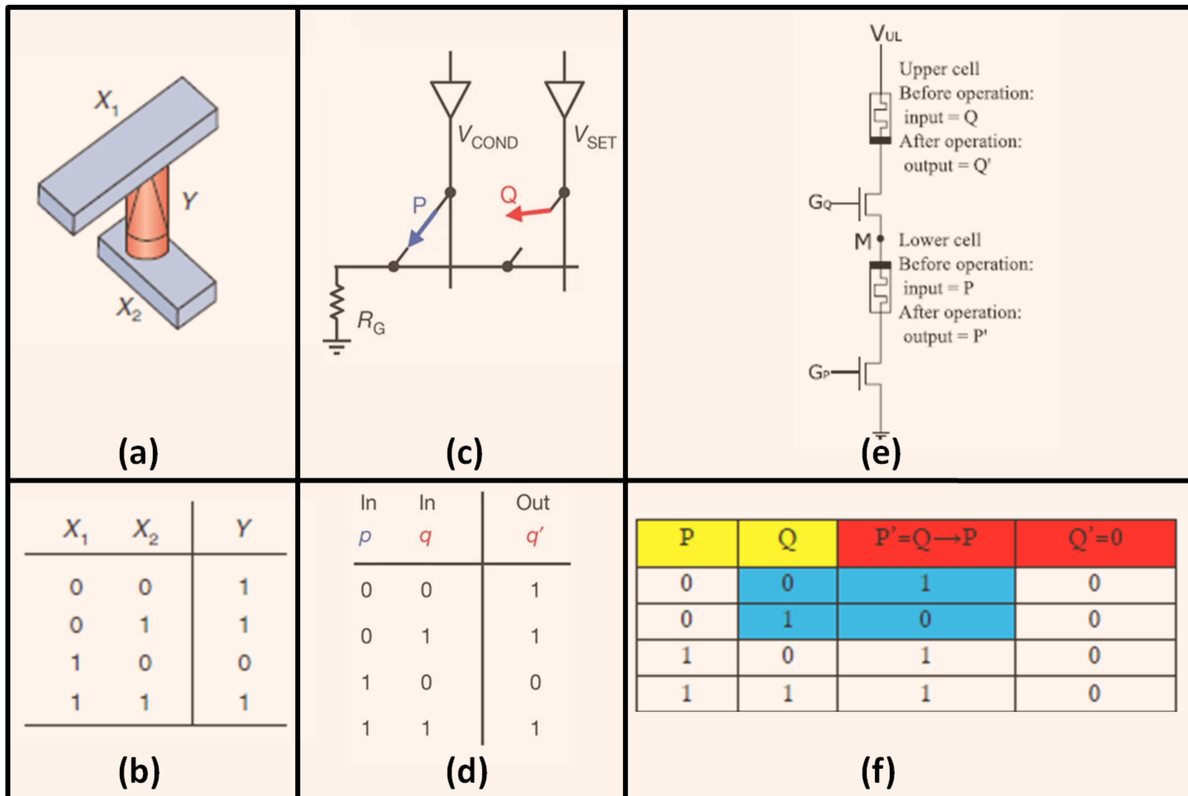
Other than planer crossbar structure, a lot of research has also been focused on developing architecture in 3D manner to increase the memory density, as shown in Figure 2.6 [49,50]. The Figure 2.6a shows stacking of memristor positioned vertically over one another [49]. The Figure 2.6b shows stacking of memristor layer over the other [50]. The integration of memristor in 3D architecture manner increases the memory density; however, it makes the fabrication process significantly more complex and potentially more expensive.

2.3.2 In-Memory Logic

In the past two decades, in-memory digital computing has focused on identifying novel logic gate concepts with lower energy and area consumption [16]. Resistive switching devices, such as memristor, provides a number of advantages in digital computing, including direct access by interconnect lines, the capability to electrically reconfigure the device, and nanoscale miniaturization. Figure 2.7 shows various methods to perform digital Boolean operations using memristor, differing by the input type, the output type, and the physical operation to describe the logic function [51-53].

In the logic gate of Figure 2.7a, the two input states X1 and X2 are represented by the voltage values applied to the top and bottom electrodes, respectively, while the output of the logic operation is stored as the resistance of the memristor device [51]. The output of the computation is the resistive state, namely a logic value 0 for the HRS, and 1 for the LRS, where the memristor device is initialized to state 1. One of the major drawbacks of this method is the requirement of sense amplifier to detect the state of the device, and the conversion of resistive state to voltage state for the operations. Figure 2.7b shows the inputs

and outputs for implementation of IMP logic. The IMP or "imply logic" is a fundamental but powerful Boolean logic operation on two operands (p and q) such that "p IMP q" is equivalent to "(~ p) OR q".



X_1	X_2	Y
0	0	1
0	1	1
1	0	0
1	1	1

In p	In q	Out q'
0	0	1
0	1	1
1	0	0
1	1	1

P	Q	P'=Q→P	Q'=0
0	0	1	0
0	1	0	0
1	0	1	0
1	1	1	0

Figure 2.7. (a) V–R logic gate based on memristor, and (b) corresponding truth table for material implication (IMP) operation [16]; (c) The basic gate/latch circuit based on memristor, and (d) The truth table for the q←pIMPq [52]; (e) 2T2R logic structure with back-to-back RRAM pair, and (f) corresponding truth table for P/Q and P'/Q' when (V_U, V_L, G_P, G_Q) = (1, 0, 1, 1): P'=Q→P (IMP), Q'=0 (bit set). P'=Q→0 (NOT) operation is highlighted in blue [53].

The logic gate in Figure 2.7c, is fully resistance based logics, where the inputs are stored initially in memristor p and q. Bit '0' is stored in form of HRS, while bit '1' is stored in form of LRS [52]. To execute IMP function a pulse of V_{cond} and V_{set} is applied to p and q respectively, and the final result is stored in form of resistance state of q. Figure 2.7d shows the truth table for the operation of IMP function using logic gate shown in Figure 2.7c.

The Figure 2.7e shows another example fully resistance logic, based on memory ratioed logic [53]. In this, two memristor are connected back to back and are initialized to inputs P and Q. After application of

appropriate voltage pulse, memristor P stores the final resistance state as P`=Q→P and Q`=0 as shown in truth table 2.7f. The basic principal behind is the voltage drop across the memristors based on its initial input resistance values.

2.3.3 Machine Learning Accelerators

One of the important uses of memristors for in-memory computing is in machine learning accelerators for faster and efficient matrix multiplication using crossbar array. A crossbar array consists of multiple intersections between orthogonal row and column electrodes, each intersection containing a memristor element [16]. The crossbar memories are extremely attractive to reduce the bit cell size, as the individual device area is just $4F^2$, where F is the lithographic feature size in the process technology. From the viewpoint of in-memory computing, the crossbar array naturally provides a hardware accelerator for analog matrix–vector multiplication (MVM). Figure 2.8 illustrates the concept of MVM in a crossbar array, where a voltage V_j is applied to the jth column, with j = 1, 2, …, N, where N is the number of rows and columns. The voltage-induced currents of each resistive element are collected at the grounded rows, yielding a total current.

$$I_i = \sum_j G_{ij} V_j \quad (2.1)$$

at the ith row, where G_{ij} is the conductance of the resistive memory at row i and column j. Equation (2.1) is the analog product of the conductance matrix G_{ij} and the voltage vector V_j, which implements a hardware-based MVM via Ohm's law and Kirchhoff 's law [54].

Crossbar MVM can be adopted for a broad range of problems, including image compression, sparse coding, and implementation of artificial neural networks (ANNs), where G_{ij} has the meaning of a synaptic weight, V_j is a pre-synaptic spike amplitude, and I_i is the input signal to the ith neuron.

The time consumed in computation of complex algorithms in machine learning and deep learning is dominated by repeated matrix vector multiplication on huge data set. A separate hardware for matrix multiplication inside memory provides huge boost in performance of machine learning algorithms. The analog MVM in the crossbar can be carried out in just one step, as opposed to the digital CMOS based MAC operation, which is a time and energy-consuming step in classical computers. Note that a significant amount of energy for crossbar-based MVM is spent in operating analogue-to-digital converters that transform the digital input vector into analog voltages V_j in cases where the input of the calculations does not come directly from analog sensors, or where further digital processing of the output is needed [16,55].

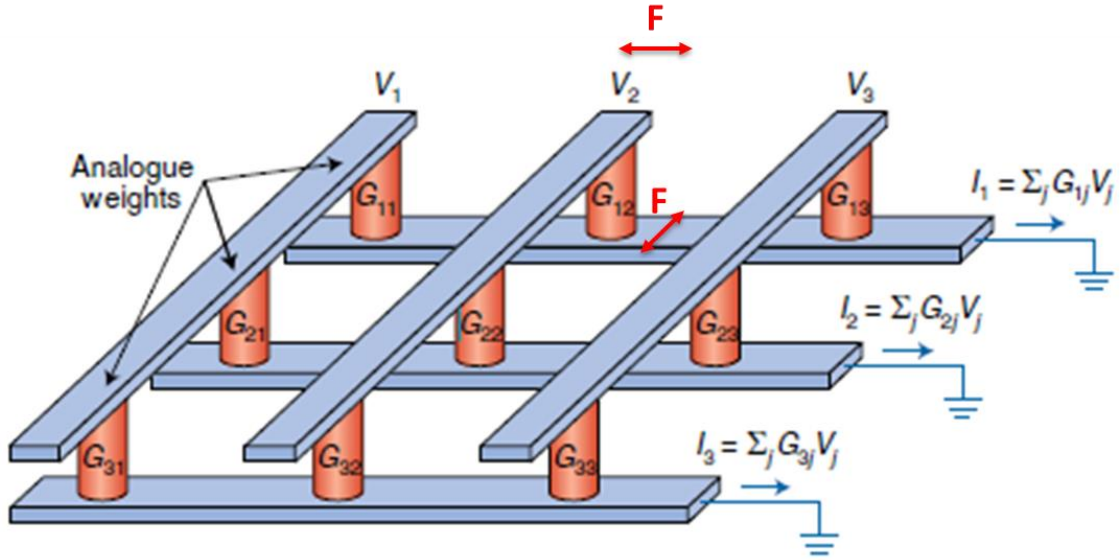


Figure 2.8. Matrix vector multiplication using analog crossbar array memristors [16].

Crossbar MVM has one of the major disadvantages in terms of precision as it relies on memristor devices, which are stochastic in nature [48,55]. The precision is least of intermediate resistance, when performing analog matrix vector matrix multiplication. Another method, proposed by Leibin Ni et al which performs MVM on memristor crossbar array in digital way, where memristor is programmed only to HRS and LRS, thus avoiding the precision issue. As shown in Figure 2.9, the method is based on four major steps [55,56].

The first step is called parallel digitizing, which requires N × N memristor crossbars. The idea is to split the matrix vector multiplication to multiple inner-product operations of two vectors. Each inner product is produced by one memristor crossbar. All columns are configured with same elements that correspond to one column, therefore the voltages on bit-lines (BLs) are all identical. The key to obtain the inner product is to set ladder type sensing threshold voltages for each column.

The inner-product output of parallel digitizing step is determined by the position where the result of first step changes from 0 to 1. In the second step, XOR operation is performed for every two adjacent bits on the output of the first step, which gives the result index. The third step takes the output of XOR step and produces in binary format as an encoder. The last step is comprised of addition of all inner products.

In contrast to analog MVM using memristor crossbar array, this method provides better precision and consumes lesser area, with penalty in power by 3.12x [55].

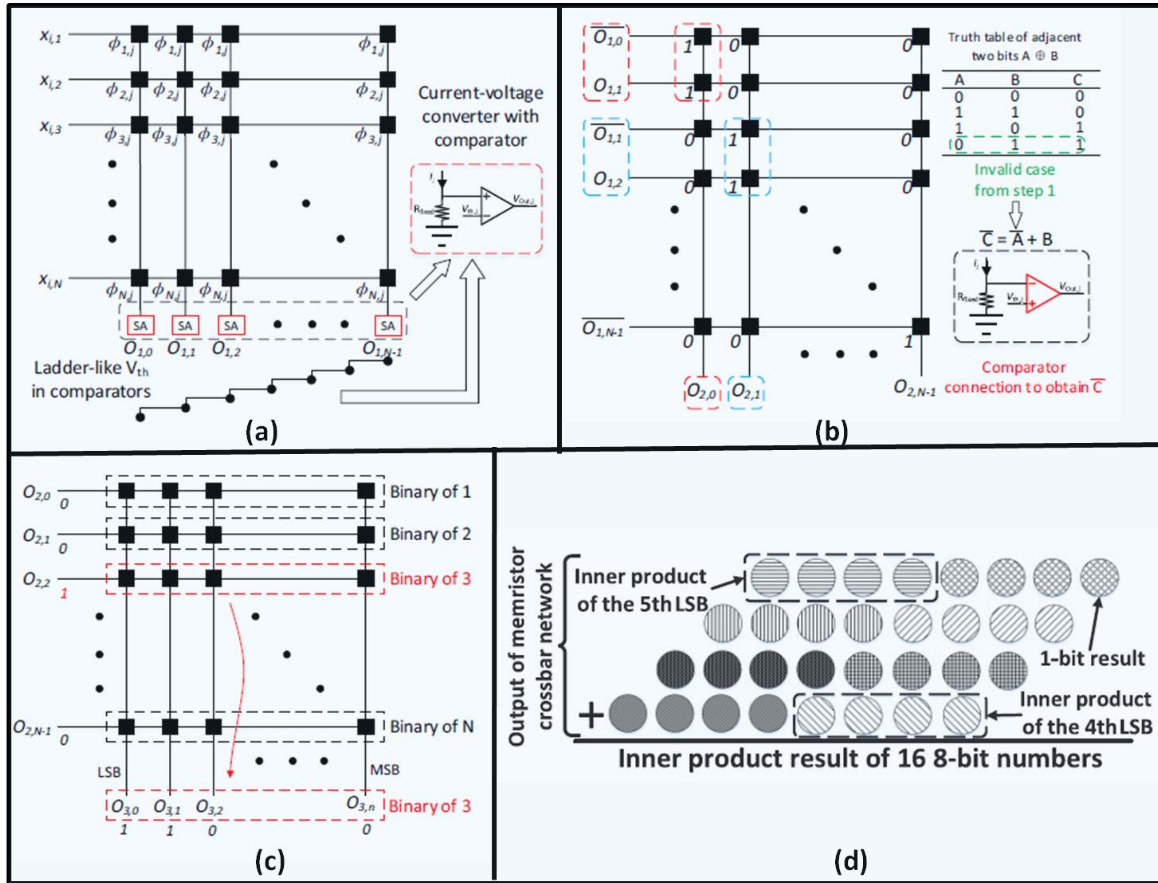


Figure 2.9. Digital Matrix Vector Multiplication using memristor crossbar array (a) Parallel digitizing step of RRAM crossbar in matrix multiplication. (b) XOR step of RRAM crossbar in matrix multiplication. (c) Encoding step of RRAM crossbar in matrix multiplication (d) RRAM-based inner-product operation [55,56].

2.3.4 Neuromorphic Computing

Similar to functioning of brain, in addition to performing all the computation within the memory, the neuromorphic computing is based on mimicking the brain synapse on hardware. Various models such as leaky integrate and fire, Hodgkin-Huxlex, integrate and fire models, etc have been proposed to imitate functioning of brain to implement neuromorphic computing. In various research papers, memristor is used as implementation of synapse [57-64]. Inside the human brain, to neurons are connected through synapse. In neuromorphic computing, weight between two neurons (or the connection between two neurons) is stored

in form of memristor's resistance state. The weight of this device is updated depending upon neuron spike. STTP is one example of weight update rule [60].

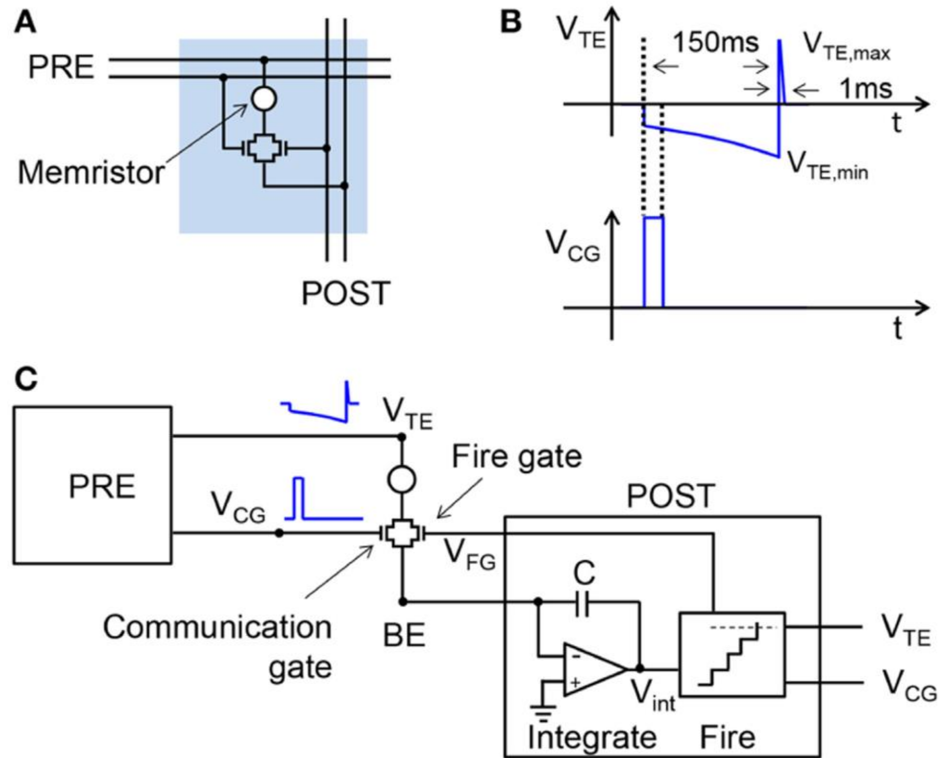


Figure 2.10. (a) memristor-CMOS synapse with 2T1R configuration. (b) voltage waveforms for V_{CG} and V_{TE} applied by the pre-synaptic neuron in the spike event (c) and overall circuit including the synapse and the pre- and post-synaptic neurons. The overlap between V_{CG} and V_{TE} pulses causes a negative current proportional to the synaptic weight, which is integrated by the post-synaptic neuron and eventually contributes to fire [60].

Figure 2.10 shows implantation of leaky integrate and fire model using memristor [60]. Figure 2.10b shows the voltage V_{CG} applied to the gate of the communication gate and V_{TE} to the top electrode, which are both applied by the pre-synaptic neuron in the spike event. The applied voltage spikes in the figure induce a spiking synaptic current, which is proportional to the conductance of the memristor, thus serving as a storage element of the synaptic weight. The synaptic current flows through the synaptic circuit and is fed into the input terminal of the post-synaptic neuron, where integration and fire take place as shown in the schematic circuit of Figure 2.10c. As the integrated current exceeds a certain threshold, the post-synaptic neuron fires, sending a spike to the following neurons in the network, as well as applying a feedback spike to the fire gate.

Several neurons are connected together, forming virtual brain on hardware, which forms basis of neuromorphic computing, which is a promising candidate for the next generation of computing technologies. [57-60].

2.4 Summary

The memristor provides an efficient hardware technology to perform in-memory computing in terms of power, area, speed and functionality. However, the roads are not straight forward, rather it is full of challenges such as stochastic nature of the device, fabrication of 3D architecture, etc. In this thesis we will discuss the fabrication of memristor using maple leaves along with TiO_2 layer, where the device shows reversible capacitive coupled and pure memristive behavior, modulated by external voltage. Further, we will discuss the fabricated device using graphene as interlayer, where the device shows great potential for multi bit memory, rendering the need for 3D memory architecture moot. Lastly, we will discuss novel design for machine learning accelerator using memristor, with better precision and more tolerance to variation, at the moderate expense of power, performance and area.

Chapter 3
Capacitive-Coupled Memristive Behavior based on Organic-Inorganic Heterojunction

3.1 Overview

The reprogrammable device is one of the important needs for circuit design. In this Chapter, TiO_2 and maple leaves (ML) are combined to form a functional layer (TiO_2-ML) inside memristive devices, which demonstrate both the capacitive effect and the non-volatile storage capability. When the voltage increases from zero, the device firstly enters a capacitive-coupled memristive state at low voltage before switch to normal memristive state at a higher voltage. The existence of the capacitive behavior results in a non-zero-crossing I-V characteristic different from the zero-crossing curve observed in normal memristive device.

3.2 Introduction

Both memristor and capacitor share a similar two-terminal structure with a dielectric layer sandwiched between two metal electrodes. While ideal capacitor has a dielectric layer with infinite resistance, resistive paths form and rupture inside the dielectric layers of memristors. Thus, the memristor could demonstrate capacitance characteristic during a unique/extreme phase of operation [65, 66]. That is to say that the capacitive effect and the memristive effect can evolve with each other [67].

In previous reports, the capacitive effect was usually submerged by the high current density caused by the formation of conductive filaments [68]. That is, after the conductive filament was formed between the top electrode and the bottom electrode, it will short-circuit the capacitive effect, thereby exhibiting a pure memristive effect. I. Valov and J. L. M. Rupp's groups emphasized that the redox reaction caused by moisture at the interface/surface plays a leading role for the generation of capacitive state in a memristive device [69-71]. However, moisture does not provide a reliable way to precisely control the electronic behavior. In addition, moisture should generally be avoided in the operation of electronic device because moisture often causes the failure of electronic performance. Besides, the previously observed such behaviors provide very small difference between memristive states of the device to be used in applications.

In this Chapter, we proposed a new device structure which uses voltage to control the device evolving between capacitive behavior and pure memristive behavior. The organic-inorganic heterojunction provides better stability and a greater difference between the resistance states of memristor device. Based on theoretical analysis, a physical model is proposed to understand the evolution process.

In the following section 3.3, we will discuss device fabrication steps and its characterization. In section 3.4, we will discuss the results, followed by conclusion in section 3.5.

3.3 Device Fabrication and its Characterization

The preparation process of the organic-inorganic heterojunction device with Ag/TiO_2-ML/Al structure is shown in Figure 3.1.

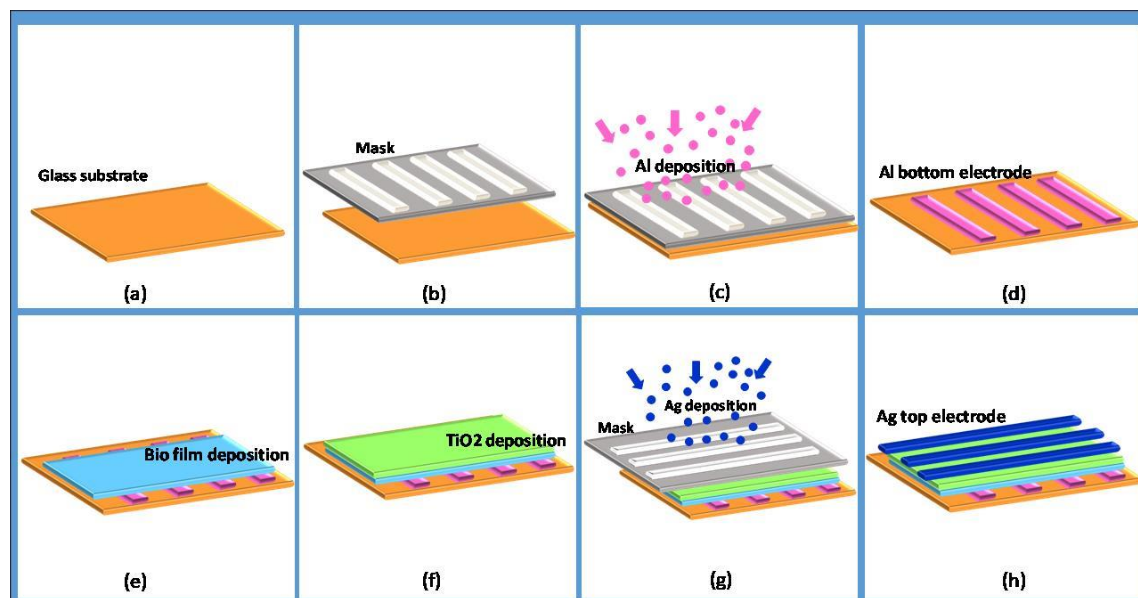


Figure 3.1. The preparation process of organic-inorganic heterojunction device with Ag/TiO_2-ML/Al structure. (a) masking for bottom electrode deposition (c) Al sputtering for bottom electrode (d) formation of bottom electrode (e) deposition of bio film using spin coating method (f) TiO_2 film layer formation over bottom electrode (g) Al sputtering for top electrode (h) device formation.

Firstly, glass substrates were cleaned subsequently in acetone, ethanol and isopropyl alcohol, and dried under nitrogen gas flow. We use the shadow mask process to deposit bottom electrodes. The mask is placed on the clean glass substrate, and the Al bottom electrode with a thickness of ~200 nm was deposited using sputtering. Next, the mask was removed, and biofilm made of maple leaves was deposited using a spin-coating technique. To prepare bio-film layer, we extracted the ultrafine ML powder from maple leaves by multiple grinding and suction filtration methods, as shown in Figure 3.2. Then we prepared a ML solution for the deposition of ML film by spin coating on a glass substrate with the Al bottom electrode. The sample was then allowed to dry in the oven for ~24 hours in order to remove any moisture, followed by the deposition of second oxide layer TiO_2 with the thickness of ~20 nm using sputtering. Finally, the top

electrode Ag with a thickness of ~300 nm was deposited using sputtering with the mask rotated by 90° compared to the bottom electrode. An organic-inorganic heterojunction memristive device with Ag/TiO_2-ML/Al structure was obtained following these steps. An optical photograph of the as-prepared device is shown in Figure 3.3.

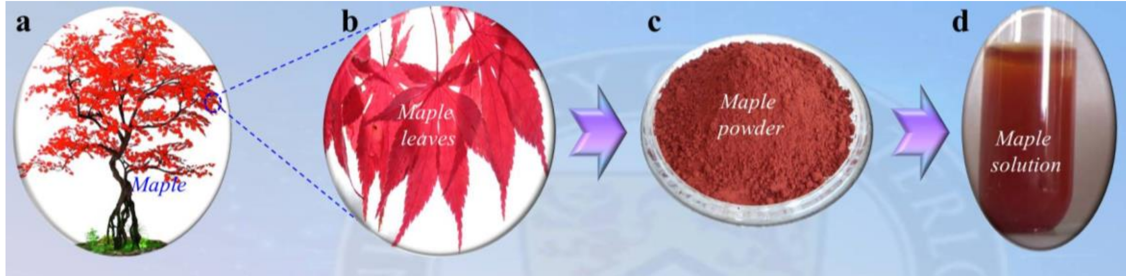


Figure 3.2. The preparation process of maple leaf solution for memristor. (a) Maple. (b) Maple leaves. (c) Maple leaf powder. (d) Maple leaf powder solution.

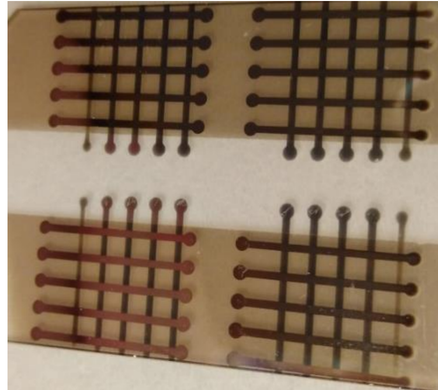


Figure 3.3. The optical photograph of the as-prepared device.

To study the memristive device behavior, we connect the bottom electrode to the ground and then apply voltage sweep at the top electrode in the order of 0 V → 1.0 V → 0 V → -1.0 V → 0 V varying linearly at a constant rate of 0.1 V/s. The experiment is repeated by increasing the voltage ranges from ±1.0 V to ±3.0 V, ±5.0 V, and ±7.0 V, respectively. Finally, the experiment is repeated by changing the voltage sweeping rate.

3.4 Result and Discussions

The I-V curves with V_{max} = 1.0 V, 3.0 V, 5.0 V and 7.0 V are presented in Figure 3.4a, c, e, g (linear scale) and Figure 3.4b, d, f, h (logarithmic scale), respectively. These I-V curves with 30~100 cycles are shown

in Figure 3.5. At V_{max} = 1.0 V, Figure 3.4a shows that the I-V curve is non-zero crossing and does not have point of intersection. It is known that this non-zero-crossing I-V curve indicates that a capacitive effect is present in the memristor [72-74].

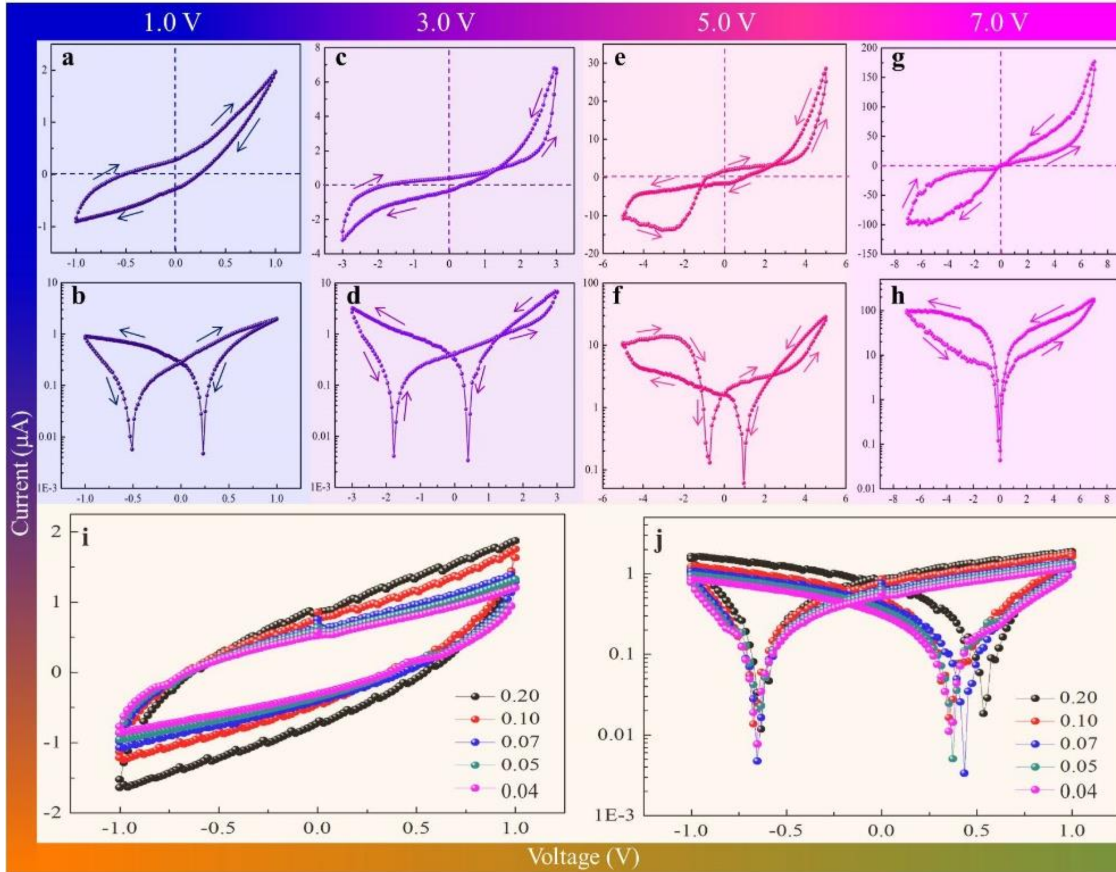


Figure 3.4. (a, c, e, g) The I-V curves under different voltage windows. (b, d, f, h) The corresponding logarithmic I-V curves. (i) The I-V curve at 1.0 V under different voltage change rate. (j) The corresponding logarithmic I-V curves.

When V_{max} is increased to 3.0 V, it can be observed that there is a crossover behavior in the I-V curve, and the intersection is in the first quadrant (Figure 3.4c). However, this I-V curve is still non-zero-crossing. When continuing to increase the test voltage to V_{max} = 5.0 V, the I-V curve shows two cross-over actions, as observed from Figure 3.4e, and the two intersections are in the first and third quadrants, respectively. This is when the device transits from capacitive behavior into capacitive-coupled memristive behavior. In order to further observe the change of the I-V curve at a higher voltage, the V_{max} was further increased to 7.0 V (Figure 3.4g). The standard memristive behavior is observed with a zero-crossing I-V

hysteresis curve. These I-V characteristics are repeatable, which can be controlled by the selection of V_{max}. By increasing V_{max}, the proposed device evolves from a capacitive behavior to capacitive-coupled memristive behavior and eventually to a pure memristive behavior.

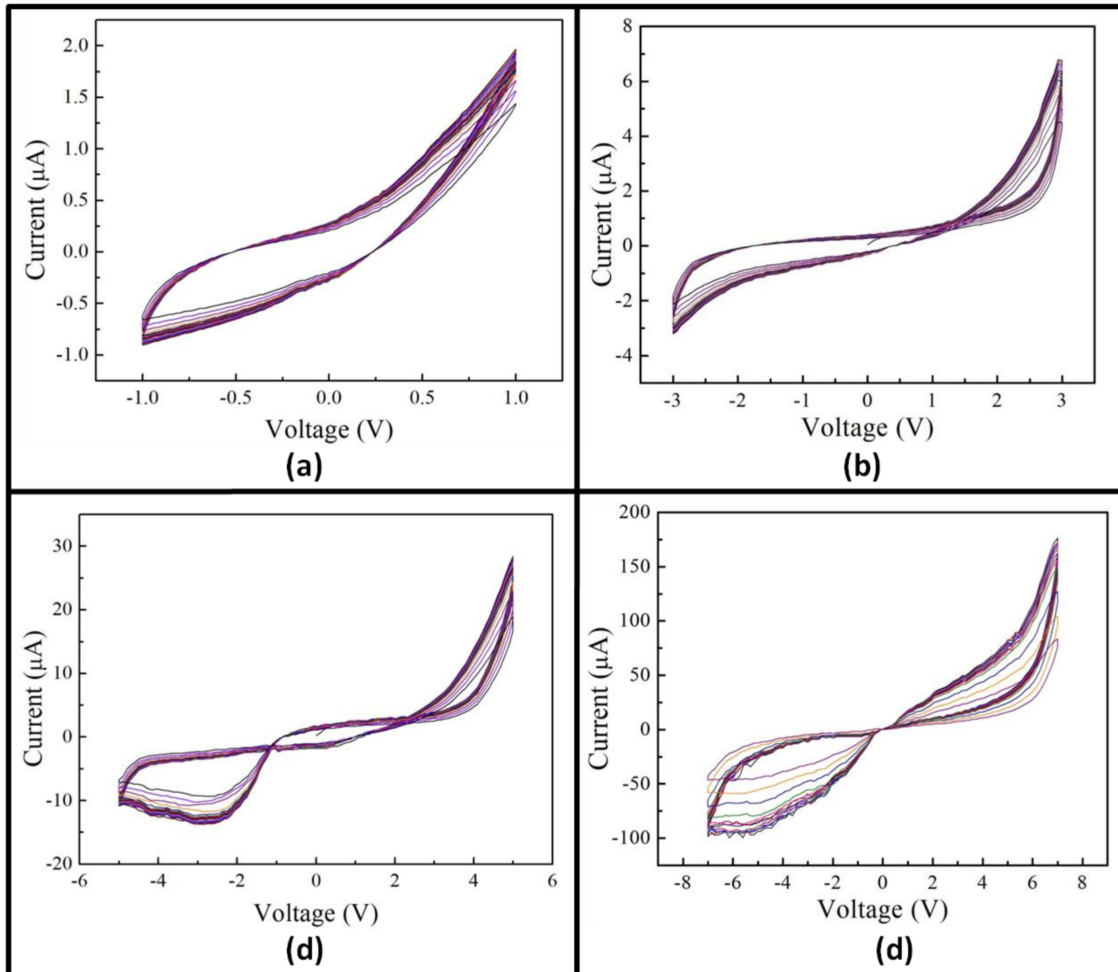


Figure 3.5. The I-V curves for multiple cycles (a) 100 cycles under voltage window of 1.0 V. (b) 80 cycles under voltage window of 3.0 V (c) 50 cycles under voltage window of 5.0 V (d) 30 cycles under voltage window of 7.0 V.

Besides, to understand the capacitive effect in the capacitive-coupled memristive device, different voltage sweep rates (dV/dt) of 0.20, 0.10, 0.07, 0.05 and 0.04 V/s are applied with $V_{max} = 1.0$ V. These results are shown in Figure 3.4i (linear scale) and Figure 3.4j (logarithmic scale). The bottom electrode is grounded, and voltage sweep is applied at the top electrode from 0 V → 1.0 V → 0 V → -1.0 V. In a

capacitor, I ∝ dV/dt, it is consistent with these results shown in Figure 3.4i. This further proves the occurrence of capacitive effect in the device at low voltage.

The endurance test and the retention test of the device was performed for standard memristor behavior, when the voltage sweeping window is varied as 0 V → 7.0 V → 0 V → -7.0 V. The endurance test of the device measured at reading voltage of 0.25V is shown in Figure 3.6a. The test shows that cycle to cycle the device shows small variations in resistance states. The retention test of the device measured for 1000sec for HRS and LRS state of the device is shown in Figure 3.6b. The test shows the device is able to retain the resistance state without much degradation.

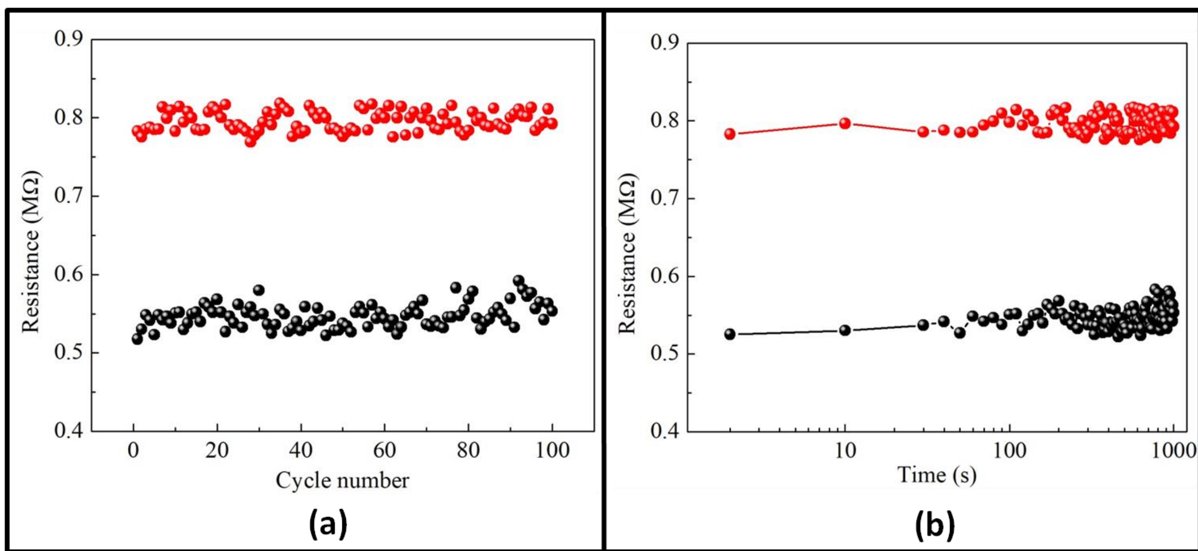


Figure 3.6. (a)The endurance test of the device at Vread of 0.25 V. (b) Retention test of the device.

To understand the conduction mechanism in Ag/TiO_2-ML/Al device, we re-plotted the I-V curves in a log–log scale (with |V| for negative voltages), as shown in Figure 3.7, and perform linear extrapolation to each section of the curves. Based on the fitting results, it is very obvious that there are sections in the log-log I-V curves with negative slopes (e.g. -0.15, -4.15 and -2.05) when the device is tested at V_{max} = 1.0 V, 3.0 V, and 5.0 V. However, no negative slope is observed when the device is tested at 7.0 V. The appearance of these negative slopes is most likely due to the I-V behavior of a capacitive device [72-75]. When the test voltage is low, no conductive filament exists in the dielectric layer. Thus, the capacitive effect dominates in the proposed device. However, when the external voltage is increased to 7.0 V, a conductive filament was formed in the functional layer of the device, which shorts the top and bottom electrodes of the device.

In this case, the current is dominated by conduction current, causing the capacitance effect to disappear, thereby exhibiting a pure memristive effect with positive slopes in log-log I-V curves.

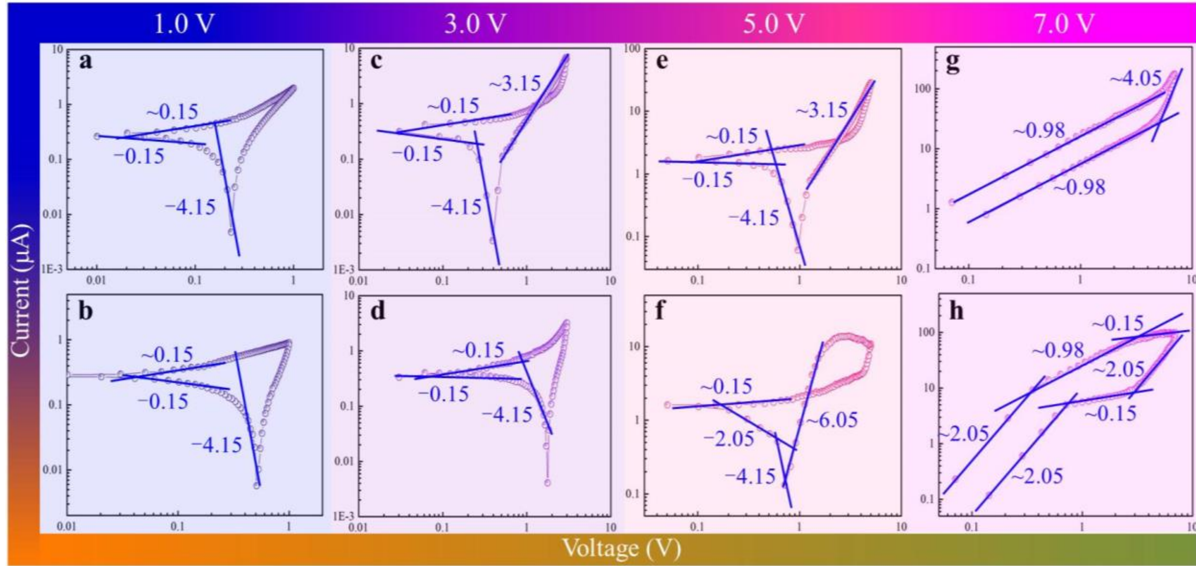


Figure 3.7. (a, c, e, g) Experimental data and fitted lines of I-V curves of memory device in positive voltage region. (b, d, f, h) Experimental data and fitted lines of I-V curves of memory device in negative voltage region.

In addition, we further analyze the case of a positive slope. We can see that the Ohmic conduction behavior (slope of ~1.0) occurs in the positive voltage region when a low voltage is applied to the device (Figure 3.7g). However, the device obeys the space-charge-limited conduction (SCLC) behavior (slope ~ 2.0) in the negative voltage region when a low voltage is applied to the device (Figure 3.7h), indicating that electrons are conducted from the un-filled SCLC of the trap change to the trap filled SCLC[76-79]. It obeys the following equation:

$$J_{trap-filled} = \frac{9}{8} n\varepsilon\mu[\frac{V^2}{d^3}] \qquad (3.1)$$

where J is the current density, n is the permittivity of free space, ε is the relative dielectric constant, μ is the mobility of charge carriers, V is the applied voltage, and d is the thickness of the functional layer. At the same time, we can observe larger slopes (~3.15 and ~4.05) in the high voltage range. This larger slope reflects the current density and energy distribution of the trap. That is to say, a conductive filament was formed in the functional layer at a high voltage, at this point, the capacitive effect completely disappears. Based on the above analysis, it is thus expected that the main conduction mechanism in our device would

be the trap-controlled SCLC by the defects and formation of conductive filaments induced by oxygen vacancies and Ag ions inside the TiO_2-ML bilayer film, as shown in Figure 3.8.

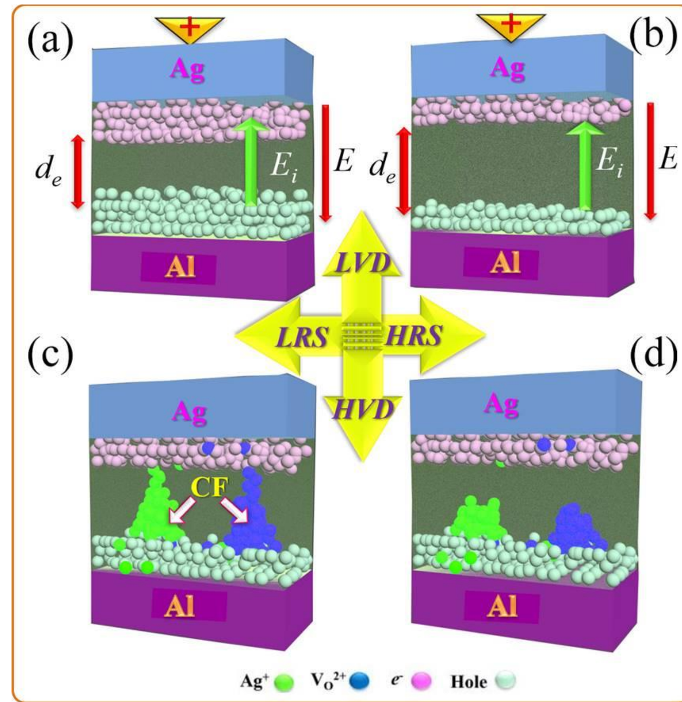


Figure 3.8. Schematics showing the electrons and oxygen vacancy diffusion processes. The conductive channel is multilevel formed under high voltage district (HVD).

Figure 3.8 illustrates the carrier transport mechanism in the TiO_2-ML bilayer film, which display the conversion of the device between high resistance state (HRS) and the low resistance state (LRS) in the low voltage district (LVD) and the high voltage district (HVD), respectively. It can be seen that when a positive voltage is applied to the top electrode of the device, a positive charge, including oxygen vacancies (V_0^{2+}) and holes, will move toward the bottom electrode along the direction of the electric field and a negative charge region will be shielded at the bottom interface. At the same time, the anode dissolution reaction equation of Ag atoms in the top electrode occurs according to the reaction [80,81].

$$Ag \rightarrow Ag^+ + e— \qquad (3.2)$$

The positive and negative ions moving in the electric field carry displacement current, which leads to the capacitive effect at the low voltage in the functional layer (Figure 3.8a, b). The displacement current exhibits a non-zero-crossing I-V curve. Moreover, as the voltage increases, the ion concentration correspondingly increases, which further changes the memristive behavior (the circular direction of the I-

V curve) because of the internal electromotive force [82], thus exhibiting a different mode of capacitive-coupled memristive effect in our device.

At high voltages, the device generates Joule heat locally due to high currents, which enhances the mobility of Ag ions and oxygen vacancies, and the high electric field can effectively accelerate the migration of electrons and ions [83-85]. After it reaches a certain threshold, it will eventually form Ag conductive filaments and oxygen vacant conductive filaments inside TiO_2-ML functional layer (Figure 3.8c). Once the conductive filaments were formed, it provides a path for the conductive current to travel between the two electrodes, overwhelming any displacement current. At this time, the capacitive effect completely is largely suppressed, showing a pure memristive effect. After the voltage polarity is inverted, the Ag^+ ions and oxygen vacancy will be pushed back to the top electrode due to the Coulomb repulsion effect, resulting in the conductive filament to be partially dissolved to form a large gap in the functional layer [86-88]. The carriers of the conduction current are expected to tunnel through this gap. Hence, the device returns to the HRS after such a reset process (Figure 3.8d). This process at high voltage is similar to those reported in the standard memristive device.

3.5 Summary

In summary, through the organic-inorganic heterojunction devices fabricated using TiO_2 and natural maple leaves as a functional layer, we proposed a novel memristive device which shows capacitive behavior at low voltages and normal memristive behavior at high voltages. Further, a theoretical analysis is provided to explain the operation and behavior of the device. The existence of capacitive coupled and memristive behavior, modulated by programming voltage, could provide way for new reprogrammable devices for in-memory computing.

Chapter 4

High Density Memory and Multibit In-Memory Logic based on Graphene as Interlayer in Multi-State Memristor

4.1 Overview

As information technology moves toward a big data era, the conventional Von Neumann architecture has shown limitation in performance. This is constrained by the continuous large volume of data being fetched and stored through input-output (IO) device [89, 90]. Therefore, it is necessary to bring processing unit as close as possible to memory for minimizing data transmission. Memristors provides dual functionalities of data storage and computing at the same position without data transmission, therefore is one of the most promising candidates for energy efficient in-memory computing. In this chapter, we demonstrate a memristor device, formed by Al/TiO_2-Graphene-DNA/Pt layers, with high performance and stable intermediate multistate resistive switching behaviors. It was observed that the asynchronous conduction by either oxygen vacancies migration or injected electron transfer is responsible for the multistate resistive switching behaviors. Further, for in-memory computing, a high-density memory and multibit parallel logic computations are realized based on the multistate resistive switching behaviors. This improves data storage capacity and performance up to 2× with respect to conventional memristor devices when they are used to store binary data. This work provides a new horizon on the multistate resistive switching and the complete logic hardware.

4.2 Introduction

Recent research has been devoted to design advanced biomaterial-based resistive switching devices in order to achieve sustainable, environmental-friendly and biodegradable electronics [32-36,77,91-94]. Unfortunately, the performance of pure biomaterial-based resistive switching device is usually inferior compared to inorganic materials-based counterparts. This is because biomaterials are prone to degrade under the electric field or via chemical reactions with water molecules in the air, which ultimately leads to the failure of device [94, 95]. Therefore, inorganic-organic multilayer structures, as functional materials in resistive switching device, have recently attracted great attention. These hybrid structures can achieve better performance in terms of HRS/LRS resistance ratio, retention and cycle stability [96-98].

Since resistive switching behavior firstly reported in TiO_2 a few decades ago, it has been observed in other semiconductor materials systems [18,99,100]. Meanwhile, DNA, an organic compound of deoxyribonucleic acid, is a natural, renewable, and biodegradable biomaterial which shows potential in light emitting diodes and field effect transistors [101, 102]. Recently, DNA has been reported as a functional layer in resistive switching devices which exhibit good memory behaviors [103, 104].

Moreover, graphene has different electron conductivity along horizontal and vertical directions of the basal plane, which can be used in advanced electronic devices [105, 106]. Here, we design a new inorganic-organic TiO_2-Graphene-DNA hybrid multilayer, as a functional layer to study its memory behaviors in resistive switching devices.

In this chapter, we explore, for the first time, the behavior of inorganic-organic TiO_2-Graphene-DNA hybrid materials in non-volatile resistive switching devices. It was fabricated with a simple capacitor configuration consisting of Al/TiO_2-Graphene-DNA/Pt. We demonstrate that this memristor has advantages in in-memory computing by achieving parallel computing, higher storage capacity, and improved area savings. In the previous works, memristors were used as planer digital memory (storing binary data in form of either HRS or LRS) [39-42]. However, the memory density in case of using memristor as planer digital memory remains poor as only single bit can be stored in memristor. Furthermore, it was also demonstrated that memristors could be used in multilevel way, where device is used in analog mode by utilizing intermediate resistance state of the device [44,45]. However, the accuracy and precision of writing data in form of intermate resistance state of the device is very poor [46-48]. In order to achieve higher memory density and higher accuracy, 3D architectures were proposed, which makes the fabrication steps complicated [49,50]. In this chapter, we demonstrate high density memory can be achieved by storing 2-bits using fabricated device Al/TiO_2-Graphene-DNA/Pt, without any compromise in accuracy and maintaining easier fabrication method. Further, we demonstrate the cell can be used perform two simultaneous operations at a time. Compared with other in-memory computing techniques, this memory system has great advantages in parallel processing, power reduction and area savings. The described resistive switching device has stable multi-resistance states, which can process up to two parallel operations in a single memristor.

4.3 Device Fabrication and its Characterization

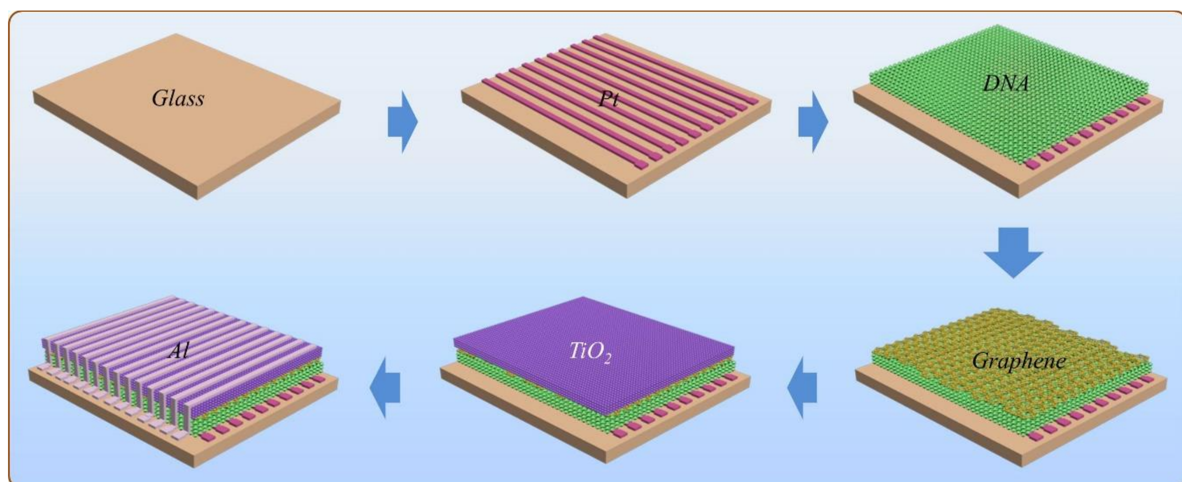


Figure 4.1. The preparation process of memristive device with Al/TiO2-Graphene-DNA/Pt structure.

For the device fabrication, firstly, glass substrates were cleaned and dried by nitrogen gas flow. Subsequently, a layer of Pt was deposited on the glass substrate by magnetron sputtering, as shown in Figure 4.1. Then an organic DNA layer was spin-coated onto a bottom electrode Pt. When the spin-coated DNA was completely dried, a layer of graphene was deposited on the DNA by solution method. Then, we deposited a layer of titanium dioxide (TiO_2) film on graphene by magnetron sputtering. Finally, a mask was used to deposit a top electrode Al with 300 nm thickness and 500 µm in width. As a result, we got a resistive switching device with Al/TiO_2-Graphene-DNA/Pt structure. The current-voltage (I-V) properties were measured using an electrochemical workstation, where a pulse is applied at the top electrode of the fabricated device, with its bottom electrode grounded. Similarly, devices with structure Al/TiO_2 /Pt, Al/ DNA/Pt, and Al/TiO_2-DNA/Pt were fabricated and their I-V properties were measured.

4.4 Device Characteristics and Study of its Mechanism

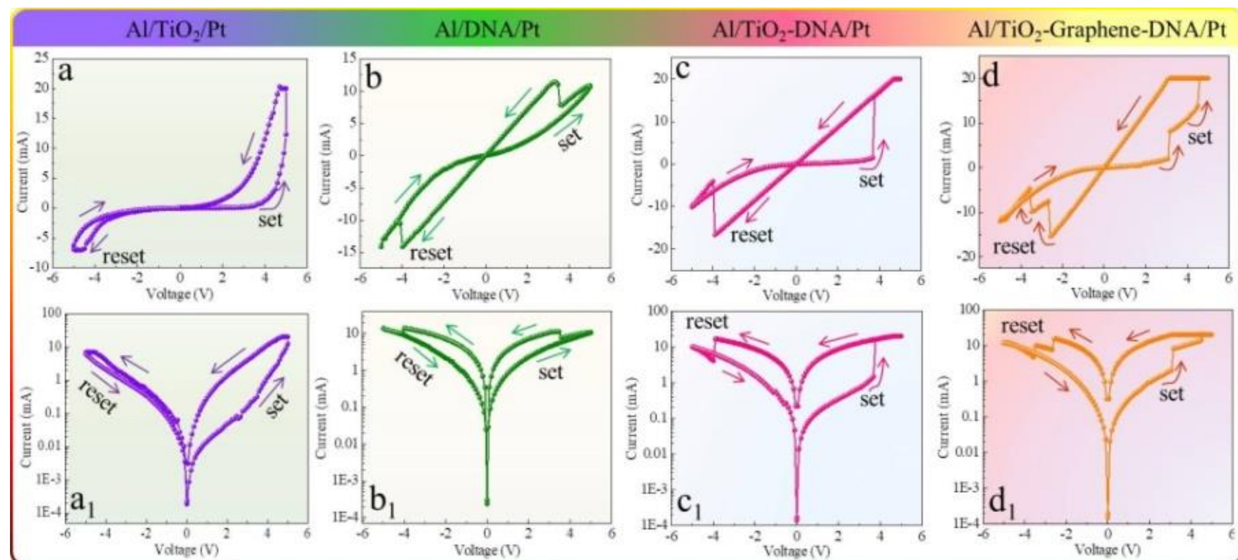


Figure 4.2. (a-d) I-V curves for the first cycle. (a1-d1) corresponding logarithmic I-V curves.

The Figure 4.2 presents typical first cycle I-V characteristics of four fabricated devices (Al/TiO_2/Pt, Al/DNA/Pt, Al/TiO_2-DNA/Pt and Al/TiO_2-Graphene-DNA/Pt) under the voltage sweep of 0 V → 5.0 V → 0 V → −5.0 V → 0 V. The I-V curve with more than 100 cycles is shown in Figure 4.3. We can observe that the I-V curve given after many cycles (>100 cycles) is nearly identical to the curve obtained in the initial characterization, indicating excellent endurance of the resistive switching device. The corresponding I-V curves of Figure 4.2a-d in logarithmic form are displayed in Figure 4.2a1-d1.

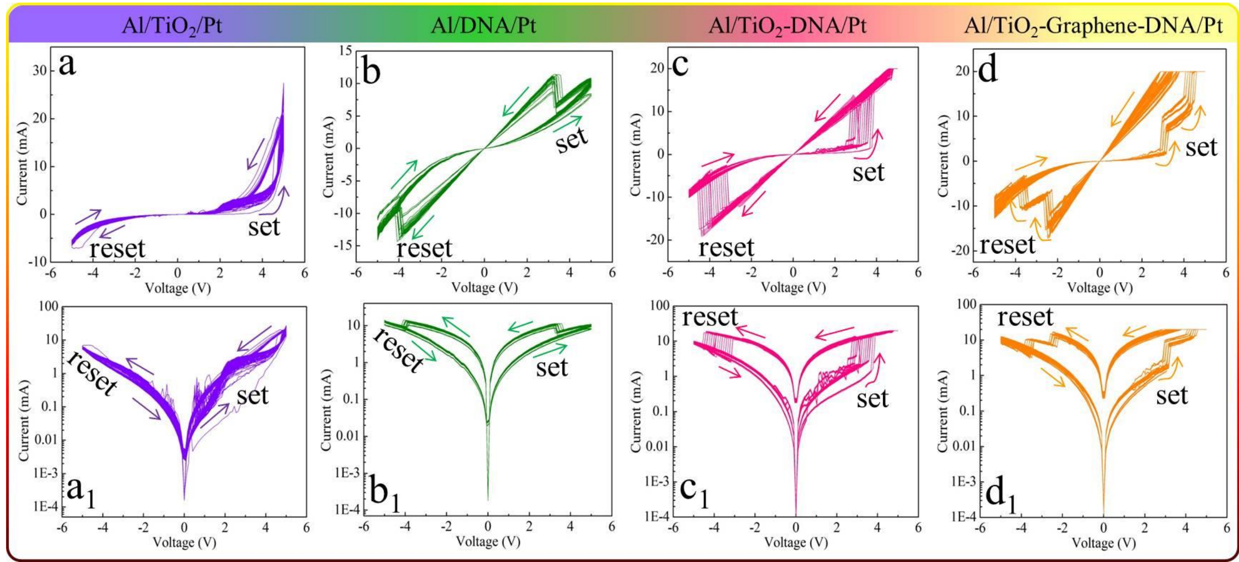


Figure 4.3. (a-d) The I-V curves with 100 consecutive cycles. (a1-d1) The corresponding logarithmic I-V curves.

The I-V response curves of these devices show obvious changes with different device structures in Figure 4.2. As the number of active layer increases, the loop of the I-V curve becomes larger. In particular, for Al/TiO_2-Graphene-DNA/Pt device (Figure 4.2d), when an external voltage is scanned from 0 to 5.0 V, the device switches from HRS to LRS after two set processes around voltage of 3.05 V and 4.25 V. After this transition, the LRS would not change until a sufficiently large opposite voltage is applied. The resistance state returns to the HRS after it goes through two reset processes happening around voltages of -2.45 V and -3.75 V. The two set and two reset processes appear in the opposite voltage regions, indicating that the as-prepared device displays bipolar multistate resistive switching memory performance [107].

The uniformity of DNA film is critical for the device prepared by spin-coating method. This may affect the stability and reliability of the switching operation. To evaluate the stability of as-prepared devices, we randomly characterize the resistance switching characteristics at different locations of the devices. Fitting to Gaussian distributions, Figure 4.4 shows the medians of the set voltages in each type of devices are 4.85 V (Al/TiO_2/Pt), 3.40 V (Al/DNA/Pt) and 3.30 V (Al/TiO_2-DNA/Pt). By nonlinear fitting, the medians of the reset voltages in each type of device are -4.5 V (Al/TiO_2/Pt), -3.85 V (Al/DNA/Pt) and -3.80 V (Al/TiO_2-DNA/Pt), respectively.

However, for Al/TiO_2-Graphene-DNA/Pt device, there are two distinguished peaks, with median set voltages (3.05 V and 4.25 V) and two peaks of reset voltages (median value at -3.75 V and -2.45 V). Since the set and reset voltages correspond to the write and erase operation in the resistive switching device [108], these multilevel set and reset processes provide a basis for the preparation and application of multistate memory in memristor devices [109].

The Al/TiO_2-Graphene-DNA/Pt devices exhibit multilevel conduction states, as shown in Figure 4.5. At different negative bias of 3.75 V and 2.45 V, it can be observed a current of 0.135 mA (defined as state-0) and 4.75~6.65 mA (defined as state-1) at reset voltages of -2.45 V and -3.7 V, respectively. Subsequently, the device shows a current of 7.25~11.45 mA (defined as state-2) and 17.85~19.85 mA (defined as state-3) at the set voltage of 3.05 and 4.25 V, respectively. The multilevel conduction states are likely due to the formation of different conductive

filaments in the TiO_2-Graphene-DNA layer at different biases. When the set voltage exceeds 4.25 V, the conductive filaments are completely formed between the top electrode and the bottom electrode, resulting in the maximum current of 20 mA. The device shows the four resistance states are almost the same over 100 test cycles, as shown in Figure 4.5. No obvious deterioration was observed, which indicates a good operational stability of the memory device.

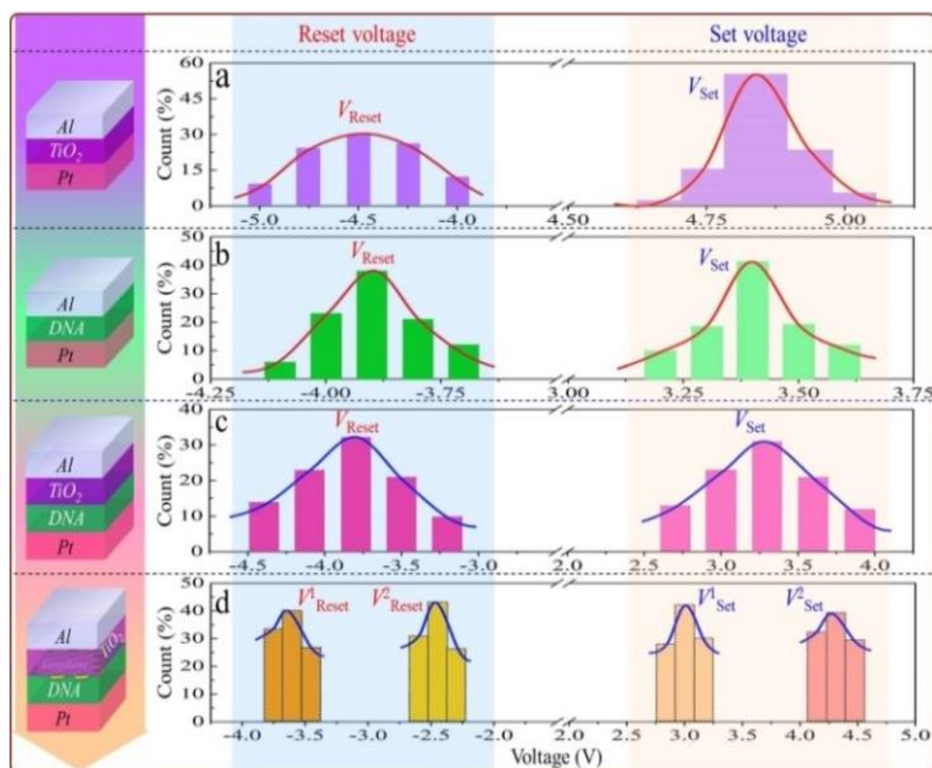


Figure 4.4. The range of V_{set} and V_{reset} voltages, and the fitting curve is satisfied the Gaussian distribution. a Al/TiO_2/Pt device. b Al/DNA/Pt device. c Al/TiO_2-DNA/Pt device. d Al/TiO_2-Graphene-DNA/Pt device.

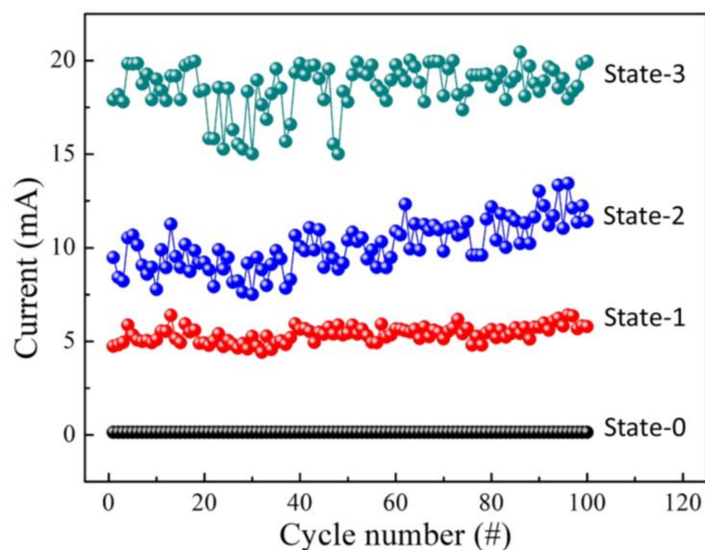


Figure 4.5. The endurance characteristics of Al/TiO_2-graphene-DNA/Pt device at different conduction states under different bias.

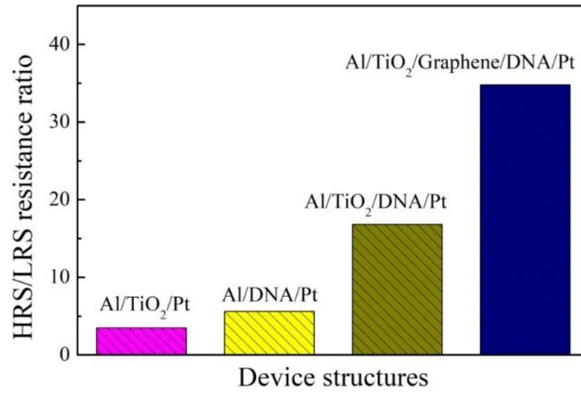


Figure 4.6. The relation between HRS/LRS resistance ratio and device structures.

The relationship between HRS/LRS resistance ratio and device structures is shown in Figure 4.6. It is worth noting that the Al/TiO_2-Graphene-DNA/Pt device represents the largest resistance ratio (~34.8) among the four types of devices. With the increases of the number of the active material layers, the HRS/LRS resistance ratio of devices is enlarged gradually. More importantly, graphene as an insertion layer can significantly improve the HRS/LRS resistance ratio of the device. This may be because graphene hinders the rapid migration of electron and oxygen vacancies along the vertical direction of basal plane, so that conductive filaments cannot be formed at low voltages across the top and bottom electrodes.

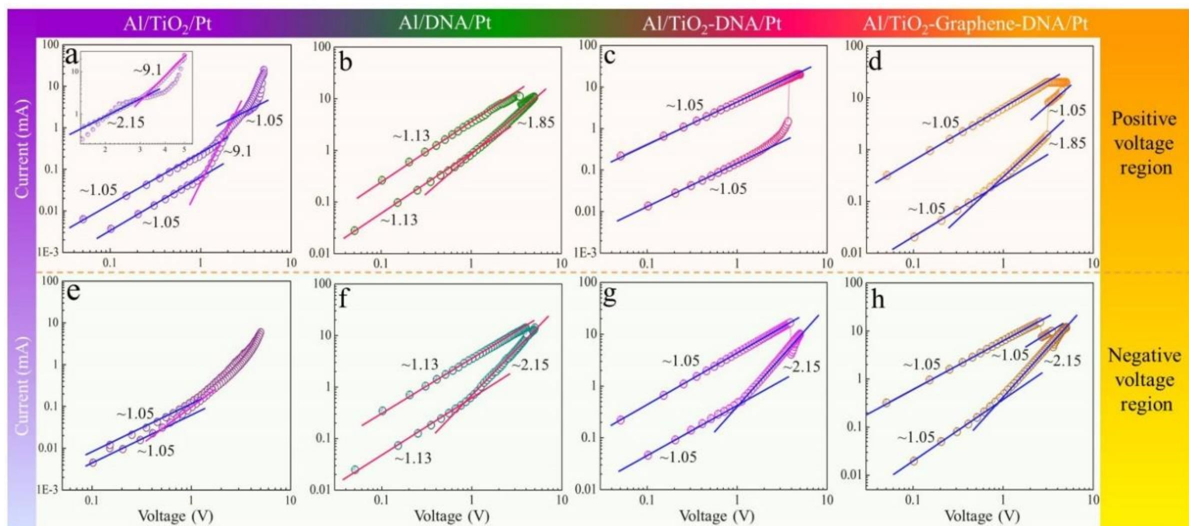


Figure 4.7. Experimental data and linear fitting of I-V curves of memory device in positive and negative voltage regions, respectively. (a) Al/TiO_2/Pt device. (b) Al/DNA/Pt device. (c) Al/TiO_2-DNA/Pt device. (d) Al/TiO_2-Graphene-DNA/Pt device.

It is necessary to explore the resistive switching mechanism in this new hybrid inorganic-organic multilayer structure. In previous reports, researchers have proposed physical models to explain the resistance switching phenomenon in different types of resistance switching devices [110-113]. Defect states, such as lattice defects and oxygen vacancies, can be readily formed in the DNA film

during the solution-based thin film-deposition processes, which may act as trapping sites of charge carrier [114-116]. To further understand the mechanism based on conduction theory, the I-V curves were plotted in a semi-logarithmic scale as shown in Figure 4.7, the I-V curve with slope of ~1.0 can be attributed to Ohmic conduction in the lower-voltage region, and its *J-V* resigned equation is as follows [117]:

$$\boldsymbol{J = qn\varepsilon\mu\,\frac{V}{d}} \tag{4.1}$$

The above equation reflects the relationship between the current (J), electronic charge (q), the concentration of the free charge carriers (n), dielectric constant (ε), electron mobility (μ), applied voltage (V) and thickness of the functional layer (d). In the region with slope of ~1.13 for Al/DNA/Pt device, the current conduction is dominated by Poole–Frenkel (PF) conduction in the DNA layer, as shown in Figure 4.7b, f. It can be described by the equation [118]:

$$\boldsymbol{J_{\mathrm{PF}} = qn\varepsilon\mu \cdot \exp\left(\frac{-q(\Phi_{\mathrm{B}}-\sqrt{(qE/\pi\varepsilon\varepsilon_0\,)}}{k_{\mathrm{B}}T}\right.} \tag{4.2}$$

where Φ_B is the barrier height, k_B is the Boltzmann constant, T is the absolute temperature, and ε_0 is the permittivity of free space. In addition, the I-V curve obeys space-charge-limited conduction (SCLC) with slope of ~2.0 at the higher bias voltage region [119]. As the number of injected carriers into the functional layer increases under higher electric field, the traps in the interface charge limited region are continuously filled up with injected carriers. It is usually called trap-filled SCLC, which can be described as follows [119]:

$$\boldsymbol{J_{\mathrm{trap-filled}} = \frac{9}{8}n\varepsilon\mu\left[\frac{V^2}{d^3}\right]} \tag{4.3}$$

After that, the injected carriers move freely into the TiO_2-Graphene-DNA functional material, leading to the current rapidly jumping up to LRS. In the LRS, the current is fully controlled by the oxygen vacancy conduction. In this situation, the I-V curve follows Child's conductive law, that is $J \propto V^2$ [120]. Therefore, the I-V curve corresponds to Ohmic and SCLC conduction mechanism in three other devices in Figure 4.7, while Al/DNA/Pt device is followed by PF conduction.

Based on the conductive analysis in Figure 4.7, the conduction mechanism of Al/TiO_2-Graphene-DNA/Pt device would be the trap controlled SCLC by the defects and the formation of conductive filaments, which are induced by oxygen vacancies inside the TiO_2-Graphene-DNA multilayer film, shown in Figure 4.8. A large amount of oxygen vacancies is contained in the TiO_2 film prepared by sputtering [121-123]. Initially, the oxygen vacancies in the TiO_2 layer move toward the TiO_2/graphene interface along the direction of the applied electric field, and the electrons in the DNA layer move toward the graphene/DNA interface, shown in Figure 4.8b. Due to the blocking of graphene, most of oxygen vacancies are unable to pass through the graphene into the DNA layer at low voltage, while electrons are also limited at the graphene/DNA interface at low voltage, shown in Figure 4.8b.

With the oxygen vacancies accumulate in the TiO_2 layer, a conductive filament composed of oxygen vacancies is gradually formed [81, 124].

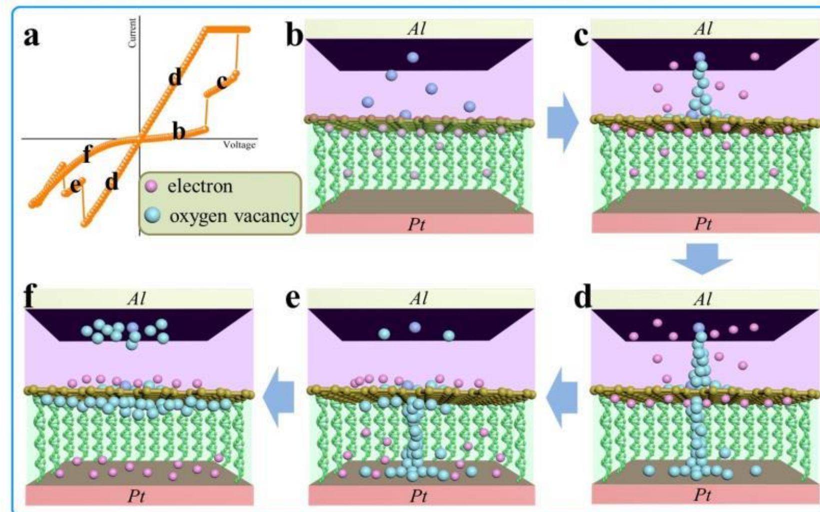


Figure 4.8. (a) Typical I-V curve labelled different states with the models showing in (b-f); (b-f) the schematic diagram of physical dynamic processes for these states for Al/TiO2-Graphene-DNA/Pt device.

When this filament shorts the top electrode Al and graphene, there is a sudden increase in current, shown in Figure 4.8c. As the external voltage is further increased, oxygen vacancies overcome the energy barrier and enter the DNA layer in Figure 4.8d. Oxygen vacancies are also accumulated to form conductive filaments along DNA. Since DNA is a complex macromolecule containing nucleotides, carbohydrates, and phosphate groups, which provides a good channel for the formation of conductive filaments. When the oxygen vacancies conductive filament shorts the top electrode A1 and the bottom electrode Pt, we observe the sudden increase of current again, shown in Figure 4.8d. With the voltage sweep enters the negative voltage region, the conductive filaments, composed of oxygen vacancies, are successively disconnected in the TiO_2 layer (Figure 4.8e) and the DNA layer (Figure 4.8f) due to the electrochemical reaction processes. Thus, the current has two mutational reductions correspondingly. Therefore, the multilevel conduction and disconnection of the conductive filaments lead to two sets and two resets processes, respectively, in the resistance switching devices. The novelty of our method is that the use of a graphene interlayer allows the conductive filaments to be multilevel states. This enables achieving an implementation of a multilevel memory. This is important for non-volatile memory and logic operation [125].

4.5 High-Density Memory using Al/TiO_2-graphene-DNA/Pt as Memristor

As discussed in Chapter 2, memristor could be used as memory in two ways i.e., in digital mode or in analog mode. In digital mode, HRS and LRS state of the device is used to store binary data ‘0’ and ‘1’. However, in this mode, the memory density is relatively lower, as only single bit can be stored in the device. In the analog mode, intermediate resistance state of the device is utilized in order to store

more information in single memristor device, or in other words, memory density is higher in analog mode. However, memristor being stochastic in nature, results in inaccuracy during memory write operation, especially when writing to an intermediate resistance state of the device.

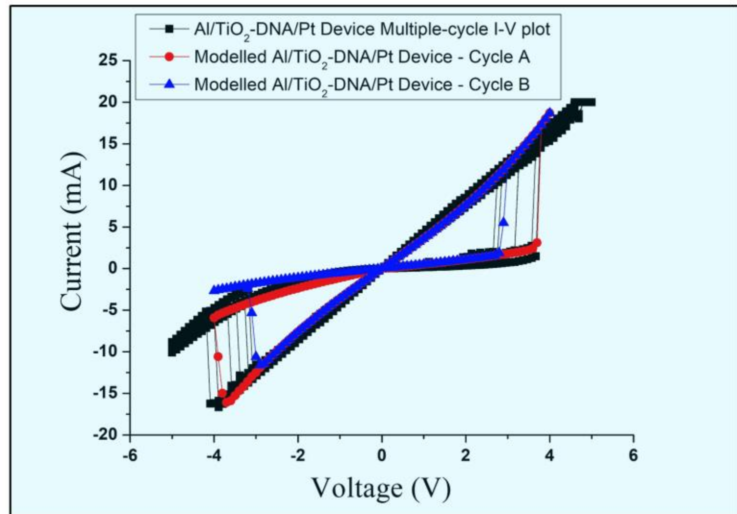


Figure 4.9. Al/TiO_2-DNA/Pt device modelling with variation. Cycle A represents device characteristics with maximum V_{set} and V_{reset}. Cycle B represents device characteristics with minimum V_{set} and V_{reset}.

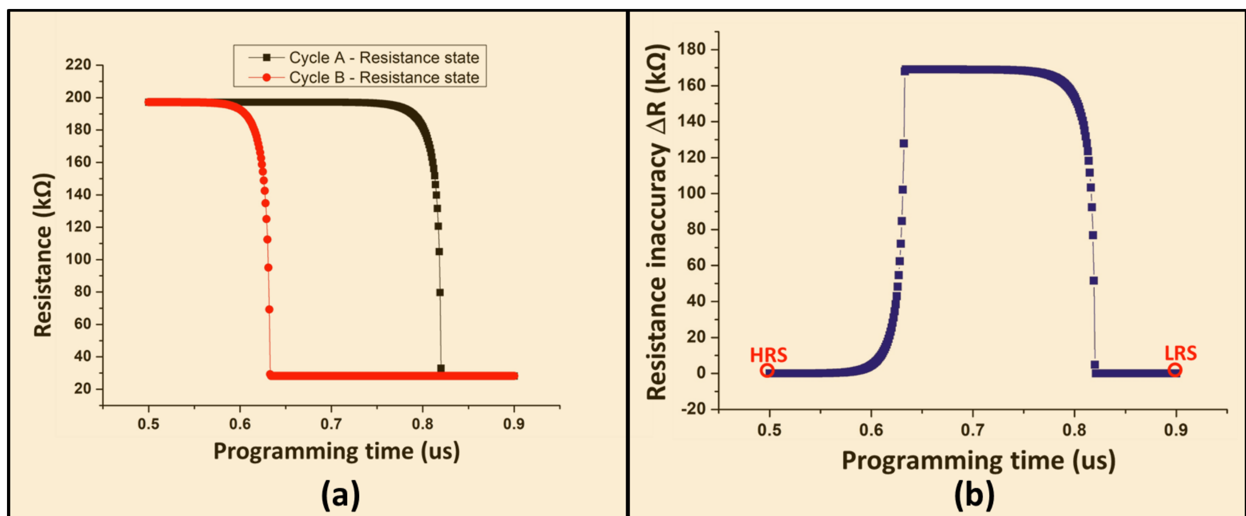


Figure 4.10. (a) Write operation in Al/TiO_2-DNA/Pt device in Cycle A (with maximum V_{set} and V_{reset}) and Cycle B (with minimum V_{set} and V_{reset}). (b) Variation in resistance state between Cycle A and Cycle B in Al/TiO_2-DNA/Pt Device.

To understand the effect of variation, we use the ASU ReRAM model [126] tuned to the fabricated Al/TiO_2-DNA/Pt device, having typical memristor characteristics. The comparison between modelled device and the fabricated device is shown in Figure 4.9a. The device variation is also measured and

modelled by adjusting the parameters between Cycle-A and Cycle-B to cover the maximum and minimum change in V_{set} and V_{reset}. Due to this variation, the programming of data in the system generates inaccuracy as shown in Figure 4.10. Therefore, it can be inferred that the usage of unstable intermediate states in memristors can lead to imprecision. As shown in Figure 4.10b, it can be observed that, writing inaccuracy is maximum for intermediate state, while minimum for LRS and HRS. The maximum and minimum possible length of the conductive filament in oxide layer restricts the variation of HRS and LRS states.

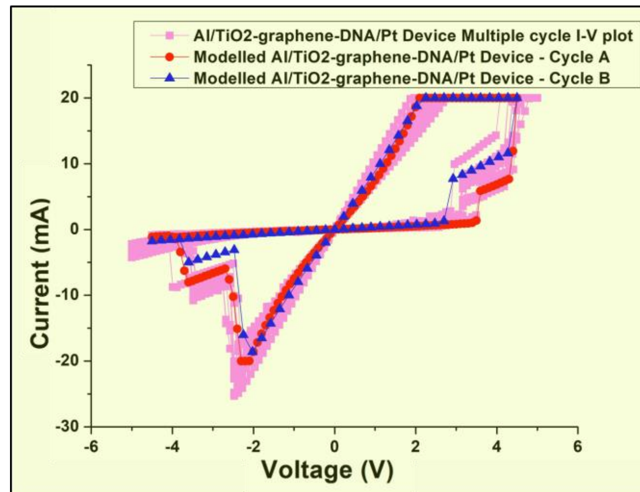


Figure 4.11. Al/TiO_2-graphene-DNA/Pt device modelling with variation. Cycle A represents device characteristics with maximum V_{set1} V_{set2} V_{reset1} and V_{reset2}. Cycle B represents device characteristics with minimum V_{set1} V_{set2} V_{reset1} and V_{reset2}.

To overcome this challenge of overall accuracy within small area, the proposed Al/TiO_2-Graphene-DNA/Pt device can provide a promising solution for high density memory [16,127,128]. The flexibility of four stable memory states in the device can play an important role in designing a memristor chip because a single device can store and process 2-bits at the same time. As a result, the memory array based on Al/TiO_2-Graphene-DNA/Pt resistive switching cells can be used to perform multibit operation with improved speed and accuracy in a small area and easier fabrication technique.

As shown in Figure 4.11, the ASU ReRAM model [126] is tuned to the fabricated Al/TiO_2-DNA/Pt device. The device variation is also measured and modelled by adjusting the parameters between Cycle-A and Cycle-B to cover the change in V_{set1}, V_{set2}, V_{reset1} and V_{reset2}. In Figure 4.12, the as-fabricated Al/TiO_2-Graphene-DNA/Pt device shows 4 stable states with two stable intermediate states, which can store 2-bits data at same time. In order to write bits '11','10', a set voltage of 4.25V and 3.05V are applied at the top electrode respectively, with bottom electrode grounded. Similarly, in order to write bits '01', '00', a reset voltage of 3.75V and 2.45V are applied respectively, with top electrode at 0V. In-order to read the resistance state of the device, a read voltage of 1V is applied across the device to measure the current. A current of 8.71mA,1.91mA, 1.12mA and 0.27mA currents were observed

flowing through the device during the reading operation of '10','11','01' and '00', respectively. This proves the use of device for the storage of 2-bits in a single memristor.

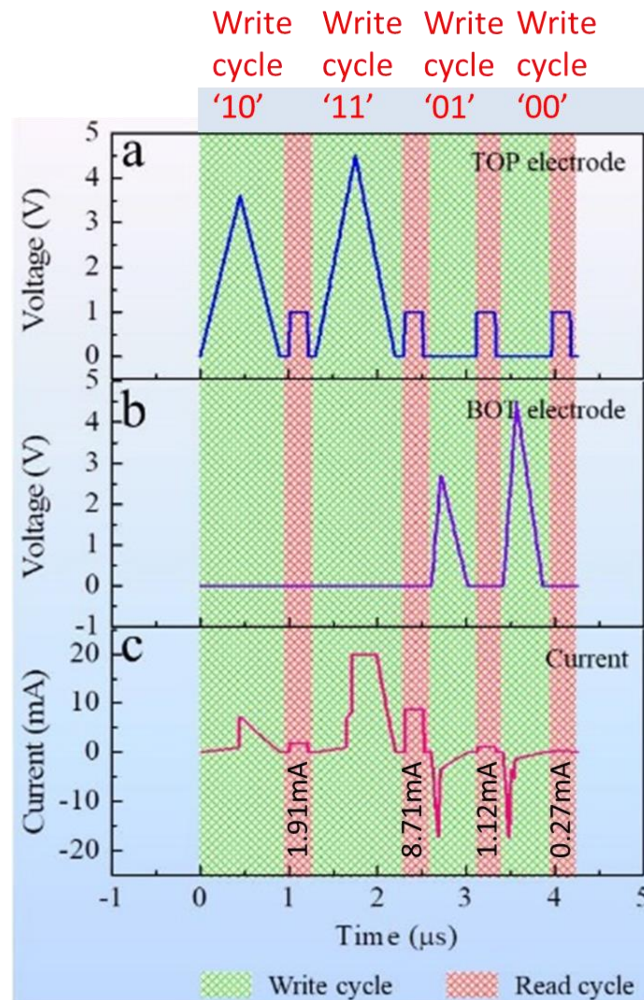


Figure 4.12. 2-bit memory operation using Al/TiO_2-graphene-DNA/Pt modelled device (a) Word line or the top electrode voltage (b) bit line or the bottom electrode voltage (c) device current. Cycle-1 represents writing and reading data '10', followed by writing and reading data '11','01' and '00' in cycle-2, cycle-3 and cycle-4 respectively. 1.91mA, 8.71mA, 1.12mA and 0.27mA currents were observed flowing through the device during the reading operation of '10','11','01' and '00', respectively.

Moreover, as shown in Figure 4.13a, the proposed device shows can be programmed to 4 stable states despite variations in device. The Figure 4.13b, the change in programing resistance state due to variation in device. It can be overserved that, similar to Al/TiO_2-DNA/Pt device with conventional memristor characteristics, though the intermediate resistance state is affected due to variations, resistance state-3, state-2, state-1, and state-0 can be programmed with more precision, attributed to limits in growth and rupture of conductive filament growth. The storing of data digitally significantly increases the accuracy w.r.t variations in device, and the fabricated Al/TiO_2-Graphene-DNA/Pt device reduces the number of required memristor to store the data digitally by half. The proposed Al/TiO_2-

Graphene-DNA/Pt device shows a great potential for the use in non-volatile memories in the existing technologies with the potential of storing twice the data size for the same number of memristors, without any loss of accuracy and maintaining simpler fabrication method.

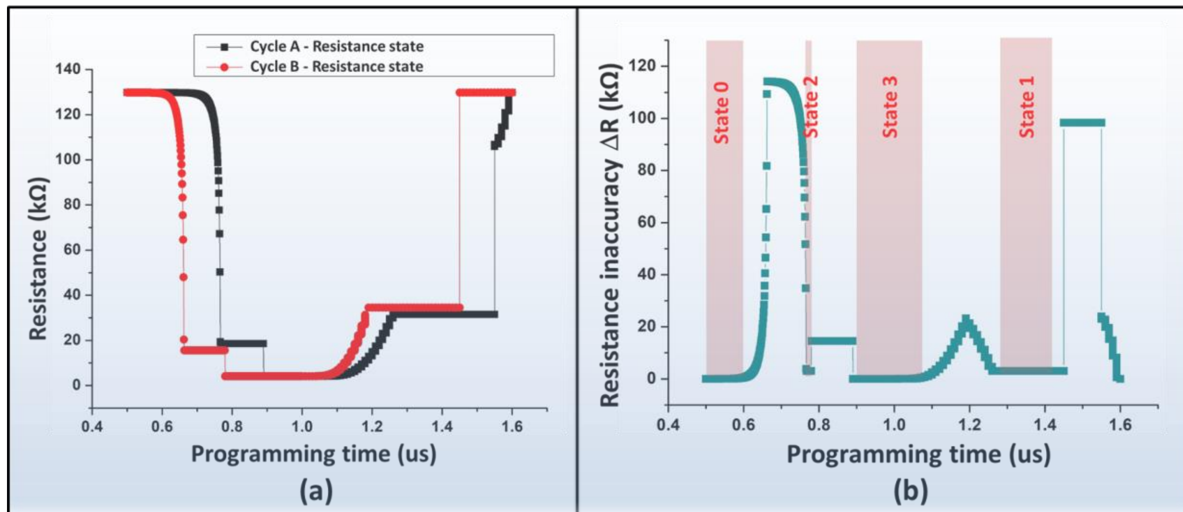


Figure 4.13. (a) Write operation in Al/TiO2-grphene-DNA/Pt device in Cycle A (with maximum V_{set1} V_{set2} $V_{reset1}$and V_{reset2}) and Cycle B (with minimum V_{set1} V_{set2} $V_{reset1}$and V_{reset2}). (b) Variation in resistance state between Cycle A and Cycle B in Al/TiO2-graphene-DNA/Pt Device.

4.6 In-Memory Logic

In this section, we demonstrate a system, which can perform two operations in parallel with maximum six inputs operands using the as-prepared cell. One operation calculates the output A_ as a function of input A, C, D, E, and F, while the other operation calculates the output B_ as a function of inputs A, B, C, D, E, and F, where A and B are the initial resistance states, C and D are word line amplitude, E and F are bit line amplitude, and A_ and B_ are final resistance states of the device. The parallel operations are performed on resistance states.

The inputs A and B are mapped with one of the four resistance states of a single memory cell prior the operation. The state (A, B) = (11) is applied by initializing the resistive switching device with an experimentally obtained set voltage of 4.25 V. This will result in the resistance state of read current ~8.71 mA at read voltage of 1.0 V. Similarly, the logical states (AB) = (10), (01), (00) correspond to the resistance states after applying a set voltage of 3.05 V or a reset voltage of -2.45 V or a reset voltage of -3.75 V, respectively. The read current for these logical states (10), (01), and (00) are 1.91 mA, 1.12 mA and 0.2739 mA, respectively in the corresponding reading cycle, when read voltage of 1.0 V was applied. Thus, it can store and process 2-bits A and B at same time. The inputs C and D are mapped as input word line voltage on the top electrode of resistive switching device. If the input of (C, D) is (11), the word line voltage level during the operation is 4.25 V. Similarly, if the inputs are (C, D) = (10), (01) and (00), the word line voltages during operation are 1.3 V, -1.7 V and -4.7 V, respectively. The system

is designed to accommodate all transitions in resistance states ranging from state 3 to state 0 and then from state 0 to state 3, depending upon word line and bit line voltage. The device could be used for different voltage ranges, depending upon which the operations will differ. The bit line voltage on the bottom electrode maps the 2-bits E and F in same manner as C and D on word line voltage on the top electrode. The output of the computation is stored as the final resistance state of memristor A_ and B_ after the word line and bit line voltage pulse. The truth table for A_ and B_ is shown in Figure 4.14a and 4.14b respectively. To identify the dependencies of final resistance state (A_, B_) on word line (C, D), bit line (E, F) and initial state of the device (A, B), we solve Karnaugh map [129] derived from the truth tables, shown in Figure 4.15 and Figure 4.16. As shown in Figure 4.15, in order to derive equation of A_, a six variable Karnaugh map is drawn and output A_ corresponding to the input combination of A, B, C, D, E and F are mapped. Similarly, as shown in Figure 4.16, in order to derive the equation of B_, a six variable Karnaugh map is drawn and output B_ corresponding to the input combination of A, B, C, D, E and F are mapped. The Karnaugh map is solved based on maximum grouping of all outputs of A_ and B_. All the groups formed are shown in Figure 4.15 and Figure 4,16, each forming a component in sum of product (SOP) form equation of A_ and B_ respectively.

The output resistance state of the operation after solving Karnaugh maps can be written as following complex equation (4.4) and (4.5):

$$A_{_} = C.\sim E + A.\sim E.\sim F + D.\sim E.\sim F + A.D.\sim E + A.C.\sim F + C.D.\sim F + A.C.D \qquad (4.4)$$

$$B_{_} = C.\sim E.\sim F + C.D.\sim E + A.B.\sim E + A.B.C + B.\sim C.\sim D.\sim E + B.\sim C.\sim E.F + B.C.\sim D.\sim F + B.C.E.F + B.\sim C.D.E.\sim F + A.\sim C.\sim D.\sim E.F + A.\sim C.D.E.\sim F + A.C.\sim D.E.F \qquad (4.5)$$

The two computations are performed in parallel, thus saving processing cost up to two times.

Figure 4.17 shows a group of all 2-operand parallel operations that can be performed. The parallel AND operation is demonstrated in Figure 4.18. When we fix D, E and F as “1”, equations (4.4) and (4.5) will be simplified to AND operations of A_ = A AND C, B_ = B AND C, as the first group in Figure 4.17, as shown in below in equations (6) and (7), respectively.

$$A_{_} = C.(0) + A.(0).(0) + (1).(0).(0) + A.(1).(0) + A.C.(0) + C.(1).(0) + A.C.(1)$$

$$A_{_} = A.C \qquad (4.6)$$

$$B_{_} = C.(0).(0) + C.(1).(0) + A.B.(0) + A.B.C + B.\sim C.(0).(0) + B.\sim C.(0).(1) + B.C.(0).(0) + B.C.(1).(1) + B.\sim C.(1).(1).(0) + A.\sim C.(0).(0).(1) + A.\sim C.(1).(1).(0) + A.C.(0).(1).(1)$$

$$B_{_} = A.B.C + B.C = B.C \qquad (4.7)$$

To physically implement these AND operations, we first program (initialize) the cell to one of the four resistance states correspond to the input (A, B). In this case, the input A and B are “bit 1” and “bit

0", respectively. Thus, the cell is initialized to (10) state, the resistance state 2. During the operation 1 in Figure 4.17, a pulse of fixed 4.25 V is applied on BL (the bottom electrode) as shown in Figure 4.18. (As E and F are constant "bit 1" for operation 1, thus (E, F) = (1 1), therefore BL voltage is 4.25 V). On WL (the top electrode), if input C is "bit 1", a pulse of 4.25 V is applied during operation 1 in Figure 4.17. At this case (C, D) = (1 1), thus, WL voltage is 4.25 V. If input C is "bit 0", a pulse of -1.7 V is applied during the operation 1. At this case (C, D) = (0 1), therefore WL voltage is -1.7 V, as explained in paragraph above. The final resistance gives the output (A_B_). In this example, input C is "bit 1", thus WL pulse of 4.25 V is applied, as shown in Figure 4.18. The read operation of (1 0), the resistance state 2, shows successful parallel AND operation A_= A AND C (input A = 1, C = 1) and B_ = B AND C (input B = 0, C = 1). This implies the resultant resistance states A_ and B_ are "bit 1" and "bit 0" respectively. Figure 4.19 shows all other possible combination of inputs A, B and C to perform parallel operations A_= A AND C and B_= B AND C. Figure 4.17 shows a list of 2-operand parallel operations that can be performed. The system is able to compute all operations in a single step and inputs are in their true states. No complementary versions of inputs were required. In a similar manner, 3-operand and 4-operand parallel operations can be derived from equations (4.4) and (4.5).

A	B	C	D	E	F	A_
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	0	0	1	1	0
0	0	0	1	0	0	1
0	0	0	1	0	1	0
0	0	0	1	1	0	0
0	0	0	1	1	1	0
0	0	1	0	0	0	1
0	0	1	0	0	1	1
0	0	1	0	1	0	0
0	0	1	0	1	1	0
0	0	1	1	0	0	1
0	0	1	1	0	1	1
0	0	1	1	1	0	1
0	0	1	1	1	1	0
0	1	0	0	0	0	0
0	1	0	0	0	1	0
0	1	0	0	1	0	0
0	1	0	0	1	1	0
0	1	0	1	0	0	1
0	1	0	1	0	1	0
0	1	0	1	1	0	0
0	1	0	1	1	1	0
0	1	1	0	0	0	1
0	1	1	0	0	1	1
0	1	1	0	1	0	0
0	1	1	0	1	1	0
0	1	1	1	0	0	1
0	1	1	1	0	1	1
0	1	1	1	1	0	1
0	1	1	1	1	1	0
1	0	0	0	0	0	1
1	0	0	0	0	1	0
1	0	0	0	1	0	0
1	0	0	0	1	1	0
1	0	0	1	0	0	1
1	0	0	1	0	1	1
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1	0	0	1	1	1	0
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1	1	0	0	1	1	0
1	1	0	1	0	0	1
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1	1	0	1	1	0	0
1	1	0	1	1	1	0
1	1	1	0	0	0	1
1	1	1	0	0	1	1
1	1	1	0	1	0	1
1	1	1	0	1	1	0
1	1	1	1	0	0	1
1	1	1	1	0	1	1
1	1	1	1	1	0	1
1	1	1	1	1	1	1

(a)

A	B	C	D	E	F	B_
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	0	0	1	1	0
0	0	0	1	0	0	0
0	0	0	1	0	1	0
0	0	0	1	1	0	0
0	0	0	1	1	1	0
0	0	1	0	0	0	1
0	0	1	0	0	1	0
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0	1	0	0	1	1	0
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0	1	1	0	1	1	1
0	1	1	1	0	0	1
0	1	1	1	0	1	1
0	1	1	1	1	0	0
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	0	0	0	1	1
1	0	0	0	1	0	0
1	0	0	0	1	1	0
1	0	0	1	0	0	0
1	0	0	1	0	1	0
1	0	0	1	1	0	1
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1	0	1	0	0	0	1
1	0	1	0	0	1	0
1	0	1	0	1	0	0
1	0	1	0	1	1	1
1	0	1	1	0	0	1
1	0	1	1	0	1	1
1	0	1	1	1	0	0
1	0	1	1	1	1	0
1	1	0	0	0	0	1
1	1	0	0	0	1	1
1	1	0	0	1	0	0
1	1	0	0	1	1	0
1	1	0	1	0	0	0
1	1	0	1	0	1	1
1	1	0	1	1	0	1
1	1	0	1	1	1	0
1	1	1	0	0	0	1
1	1	1	0	0	1	1
1	1	1	0	1	0	1
1	1	1	0	1	1	1
1	1	1	1	0	0	1
1	1	1	1	0	1	1
1	1	1	1	1	0	1
1	1	1	1	1	1	1

(b)

Figure 4.14. (a) Truth table for A_. (b) Truth table for B_.

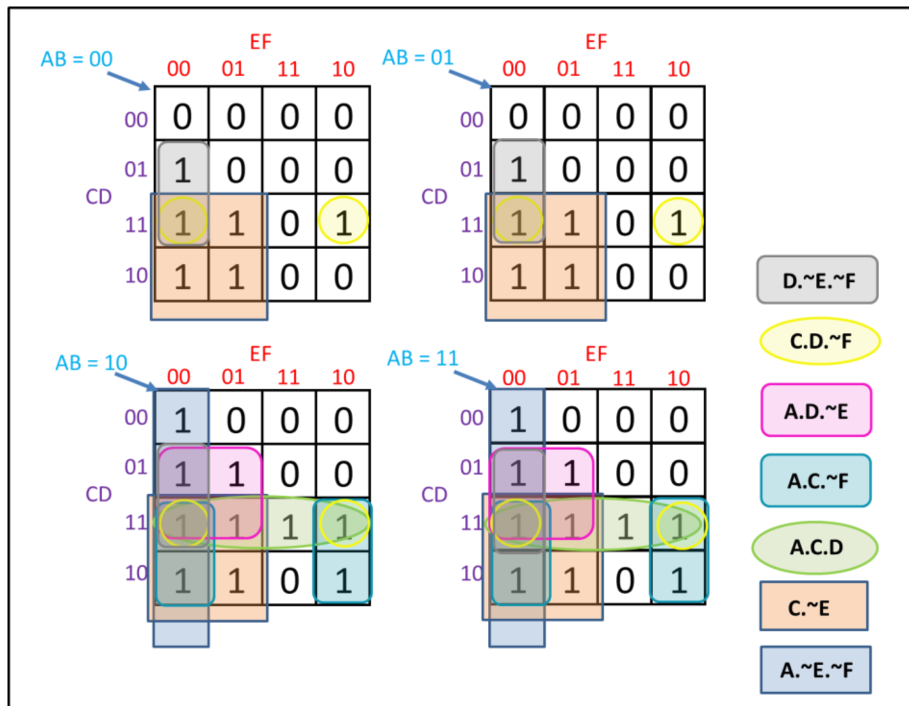


Figure 4.15. Derivation of A_ in SOP form using Karnaugh map.

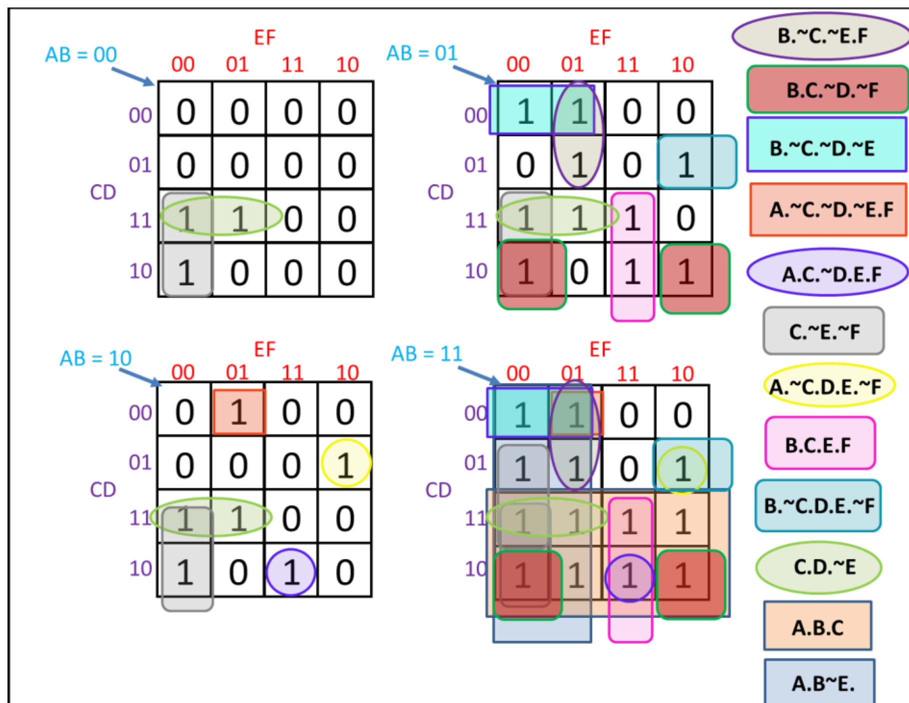


Figure 4.16. Derivation of B_ in SOP form using Karnaugh map.

	Operations	Inputs		Output	Conditions
OPERATION 1	AND	A	C	A_ = A.C	D = E = F =1
		B	C	B_ = B.C	
OPERATION 2	NOT	E	-	A_ = ~E	A=0; B=0; C=1; D=0
	NAND	E	F	B_ = ~(E.F)	
OPERATION 3	NOT	E	-	A_ = ~E	A=1; B=1; C=0; D=1
	NAND	E	F	B_ = ~(E.F)	
OPERATION 4	NOR	E	F	A_ = ~E.~F	A=0; B=1; C=0; D=1
	EXOR	E	F	B_ = E.~F + ~E.F	
OPERATION 5	NAND	E	F	A_ = ~(E.F)	A=1; B=0; C=1; D=0
	EXNOR	E	F	B_ = E.F + ~E.~F	
OPERATION 6	RIMP	C	E	A_ = C + ~E	A=1; B=0; D=0; F=0
	IMP	C	E	B_ = C.~E	
OPERATION 7	IMP	C	E	A_ = C.~E	A=B=D=F=0
	IMP	C	E	B_ = C.~E	
OPERATION 8	OR	A	C	A_ = A+C	B=D=E=F=0
	BIT TRANSFER	C	-	B_ = C	

Figure 4.17. Parallel operations allowed by the proposed Al/TiO2-Graphene-DNA/Pt device.

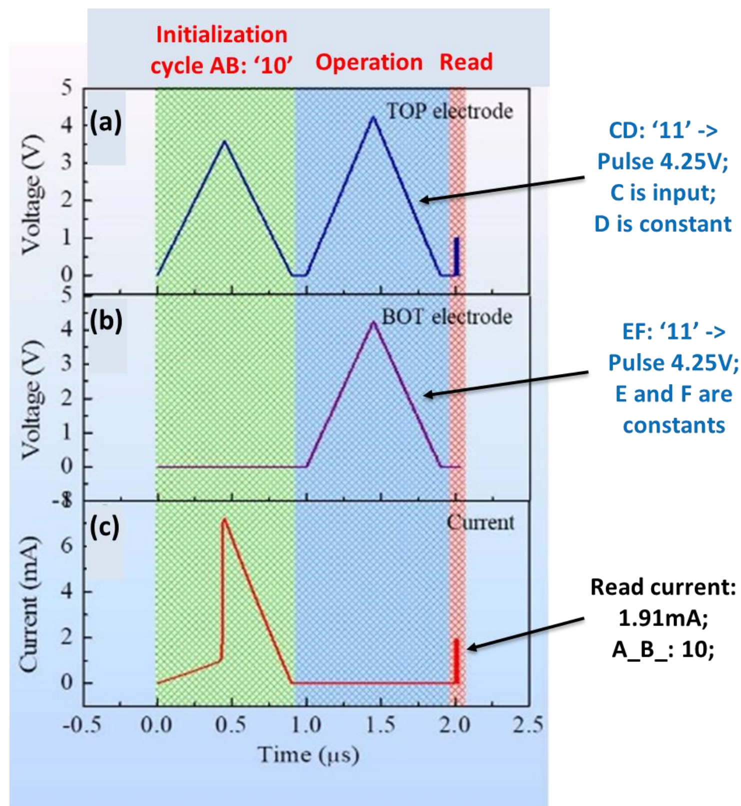


Figure 4.18. Parallel AND operations A_ = A AND C and B_ = B AND C for inputs A, B and C as 1, 0, and 1, respectively. (a) Word line or the top electrode voltage (b) bit line or the bottom electrode voltage (c) device current.

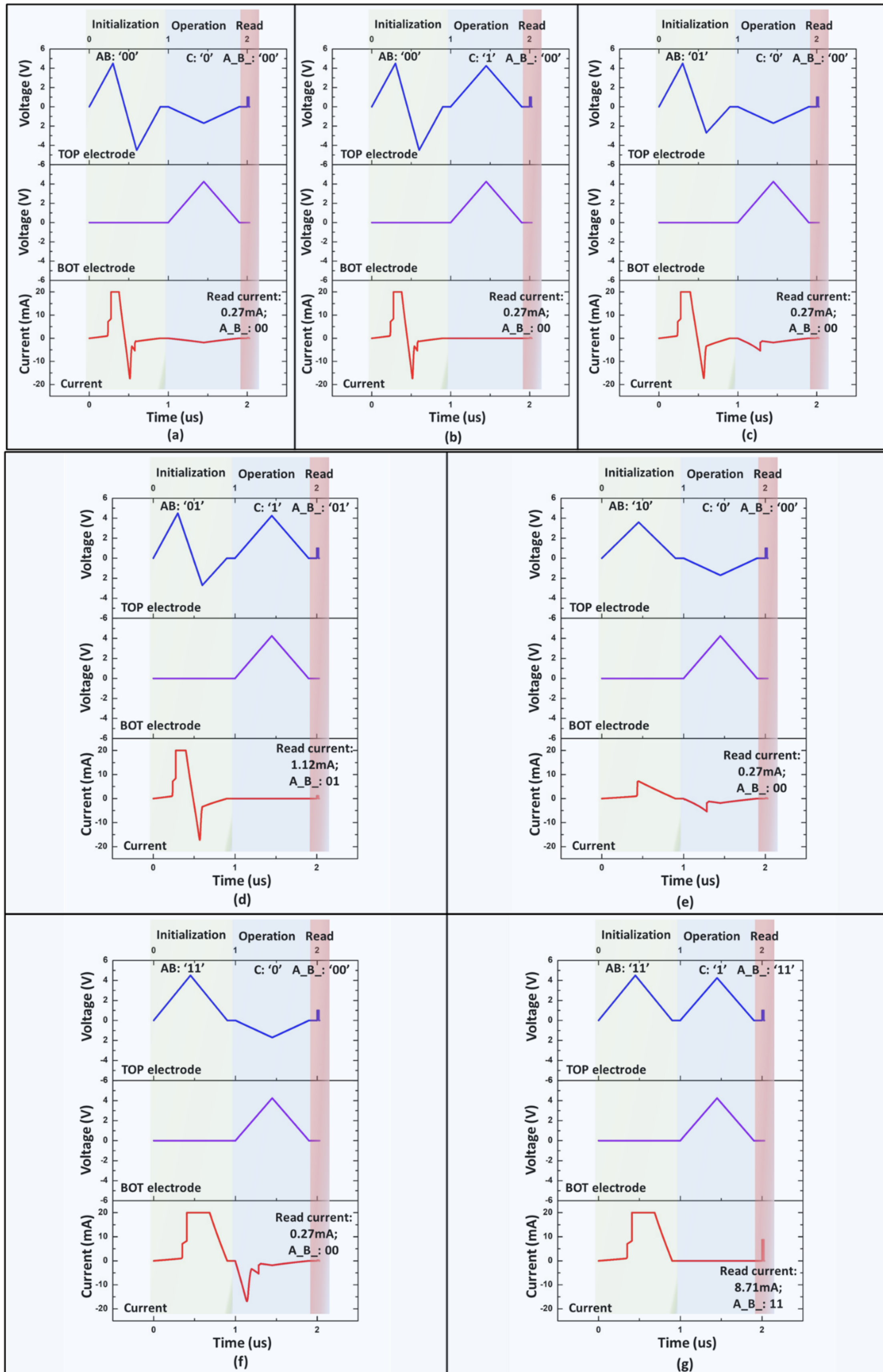


Figure 4.19. Parallel AND operations A_ = A AND C and B_ = B AND C for inputs A, B and C as (a) 000; (b) 001; (c) 010; (d) 011; (e) 100; (f) 110; (g) 111, respectively.

4.7 Summary

In summary, a novel resistive switching device has been demonstrated with the structure of Al/TiO_2-Graphene-DNA/Pt. The device shows an excellent resistive switching memory behavior with stable multi-level resistance states, which enables 2-bit storage capacity in a single device. Using such device, parallel logic operations for in-memory computing can be performed, which could provide a way for more faster and energy efficient solution for in-memory logic. Our study provides a guide for the design of new functional materials for the multistate logic operation in advanced resistive switching devices, which could move toward environmentally friendly as well as energy efficient in-memory computing.

Chapter 5
Varition Tolerant Matrix Multiplication Method using Memristor for In-Memory Computing

5.1 Overview

Recently, the emphasis has been shifted toward hardware architectures for the implementation of machine learning applications to meet the demand for faster and more efficient operations on the massive amount of data. Because of their advantages of non-volatility, nanometer size, and easily integrated crossbar structure, memristor devices are widely explored for such hardware implementations. In these applications, matrix multiplication is one of the most frequently executed operations. Most of the current matrix multiplication schemes using memristors are highly variation sensitive and suffer from programming inaccuracy. In this work, we propose an analog-digital-hybrid based matrix multiplication approach to address the issue, providing an efficient way to implement matrix multiplication using memristor devices. For an input matrix size of 8 with 10-bit elements, the proposed technique improves the average accuracy up to 16.35% with penalties in power, performance, and area up to 18.5%, 8.2%, and 3.2% respectively compared with conventional matrix multiplication design using memristors in the analog/multi-level manner.

5.2 Introduction

With the recent technology advancements, the society has entered a new era of big data. A drastic amount of information is generated and processed all the time. Such huge volume of data enables a rapid growth in the domains of machine learning, which in turn post challenges in hardware technology. It is expected that innovations in hardware technology would lead to better data-heavy machine learning applications at higher speed, better energy efficiency, etc. One of the major requirements in implementing machine learning algorithms, particularly neural network and deep networks, is to perform matrix multiplication repeatedly on large volumes of data [56,130,131]. On average, 80-90% of the runtime in machine learning algorithms is consumed by matrix multiplication [132]. While there are many ways to conduct matrix multiplication on hardware, memristor provides one of the most efficient methods in terms of area, speed and power consumption [55,133,134]. However, there are several challenges associated with the matrix multiplication using memristor. In this chapter, we propose an analog-digital-hybrid approach to counter the problems with moderate penalty in power, performance and area (PPA). In the following section 5.3, the fabrication and the operation of memristor devices will be discussed. In section 5.4, the existing matrix multiplication techniques using memristors will be briefly reviewed. In section 5.5, design technique is proposed to counter the

problems associated with the existing design technique. Section 5.6 and 5.7 include experimental setup and the results to compare the designs. Section 5.8 summarizes the chapter.

5.3 Fabrication and Operation of memristor devices

5.3.1 Device Fabrication

As discussed in previous chapters, memristor (or RRAM) device is a two-terminal device comprising an oxide dielectric layer sandwiched between the top and bottom electrode as shown in Figure 5.1a. In this work, we fabricated the device with structure Al/TiO_2/Al. The detailed fabrication step is shown in Figure 5.1b-h. Firstly, glass substrates were cleaned subsequently in acetone, ethanol and isopropyl alcohol, and dried under nitrogen gas flow. We use the shadow mask process to deposit bottom electrodes. The mask is placed mounted on the clean glass substrate, and the Al bottom electrode with a thickness of ~200 nm was deposited using sputtering, as shown in Figure 5.1b-d. This is followed by the deposition of oxide layer TiO_2 with the thickness of ~30 nm using sputtering, as shown in Figure 5.1e-f. Finally, the top electrode Al with a thickness of ~300 nm was deposited using sputtering with the mask rotated by 90° relative to the bottom electrode, as shown in Figure 5.1g. Following these steps, a metal-oxide-metal device with Al/TiO_2/Al structure was obtained at each junction of top and bottom electrodes, as shown in Figure 5.1h.

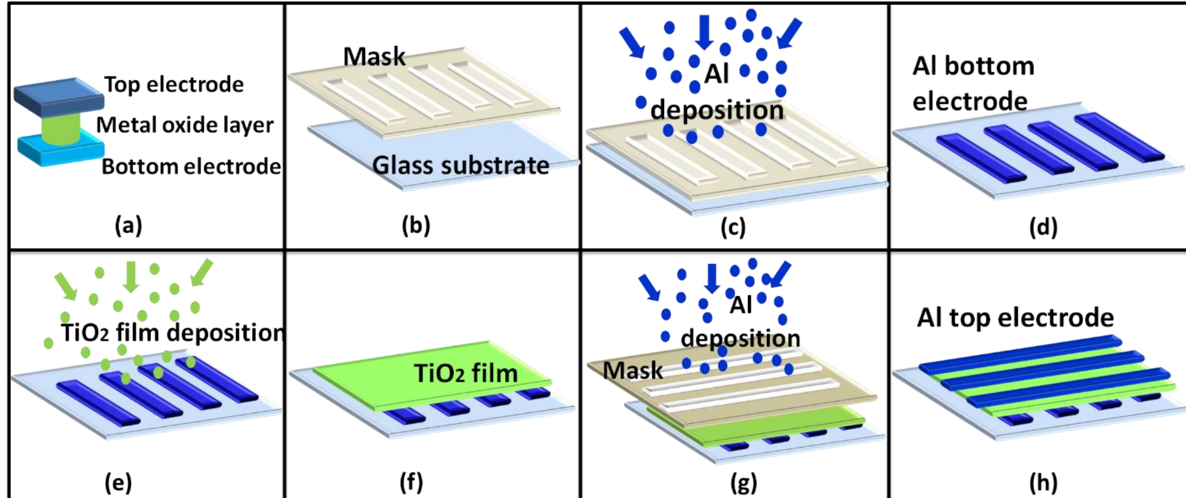


Figure 5.1. Schematics showing the deposition process of layers for memristor device. (a) schematic for memristor structure (b) masking for bottom electrode deposition (c) Al sputtering for bottom electrode (d) formation of bottom electrode (e) deposition of TiO_2 film (f) TiO_2 film layer formation over bottom electrode (g) Al sputtering for top electrode (h) device formation

5.3.2 Device Operation

The I-V curve of the fabricated memristor device to be used in this chapter is shown in Figure 5.2a. The operation of device can be explained by conductive filament growth and rupture in oxide region with

application of potential difference at both the electrodes. During the one-time electroforming process after the device fabrication, a high voltage, known as forming voltage, is applied to generate mobile oxygen ions through dielectric breakdown. As a result, a conductive filament is formed due to oxygen vacancies in the dielectric layer.

During normal write operations, a programming voltage, lesser than forming voltage, is applied between top electrode and bottom electrode to control this conductive filament and thus device resistance. When a negative programming voltage V_{reset} around -2.3V is applied at top electrode with bottom electrode grounded, the oxygen ions migrate back to the oxide layer. Therefore, the conductive filament ruptures and the device behaves as a high resistance device, which is known as high resistance state (HRS) of the device. Similarly, when a positive programming voltage V_{set} around +2.5V applied at top electrode with bottom electrode grounded, the conductive filament grows back again and the device behaves as a low resistance device, which is known as low resistance state (LRS) of the device. To read the resistance state of the device, a read voltage V_{read} of 0.1V is applied across the device to sense the read current. The ratio of read current in LRS and HRS (i.e., I_{LRS}/I_{HRS}) for the fabricated device is observed to be ~8.

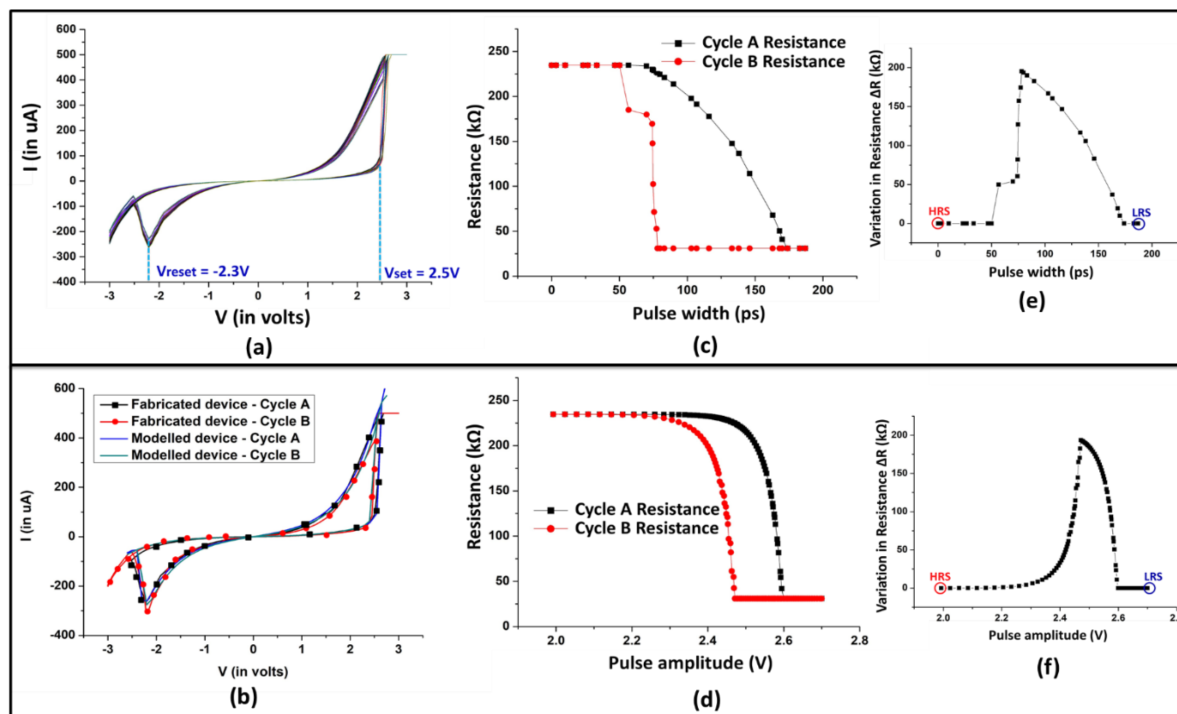


Figure 5.2. (a) Multiple cycle I-V curve of fabricated device. (b) Variation in I-V curve for fabricated and modelled device for maximum V_{set} (Cycle A) and minimum V_{set} (Cycle B). (c) Programming by changing pulse width at 2.6V pulse amplitude (d) Programming by changing pulse amplitude at 20ps pulse width (e) Variation in resistance between cycle A and cycle B when programmed by changing pulse width at pulse amplitude of 2.6V (f) Variation in resistance between cycle A and cycle B when programmed by changing pulse amplitude at pulse width of 20ps.

To use memristor in digital circuit, the binary data is stored in form of HRS and LRS of the device. For applications in analog circuits, the memristor is programmed to intermediate resistance values by

partially forming conductive filament. The intermediate resistance state is achieved either by controlling voltage [47,135] between V_{set} and V_{reset} or by varying pulse width to control of conductive filament length.

The current I can be expressed in terms of the length of this conductive filament and applied voltage V, as shown in Equation (5.1) [126], where g is the gap between conductive filaments.

$$I = I_o \exp(-\frac{g}{go}) \sinh(\frac{V}{Vo}) \quad (5.1)$$

The I_o, g_o and V_o are the fitting parameters, adjusted according to the fabricated device.

The growth and rupture of conductive filament can be expressed in terms of gap g between conductive filaments as expressed below:

$$\frac{dg}{dt} = - v_0 [\exp(-\frac{qEag}{kT}) \exp(\frac{\gamma a0}{L}\frac{qVp}{kT}) - \exp(-\frac{qEar}{kT}) \exp(-\frac{\gamma a0}{L}\frac{qVp}{kT})] \quad (5.2)$$

The device is modelled with the ASU RRAM model [126] calibrated to experimental data, as shown in Figure 5.2b. The modelled device I-V characteristics matches with that of the experimental data. Due to stochastic nature of the conductive filament formation, even small atomic fluctuations result in difference in resistance state of device. Thus, the device tends to have lot of variations, which is evident from multiple cycle of the I-V curve in Figure 5.2a. The device variation is also measured and modelled by adjusting the parameter of γ in the equation (5.2) between 17.59 (Cycle-A) and 18.04 (Cycle-B) to cover the maximum and minimum change in V_{set} and V_{reset}. γ is monotonically related with how much g responses to the programming voltage.

The variation in device leads to programming inaccuracy, which is most vulnerable for intermediate states. The Figure 5.2c and Figure 5.2d shows the programming inaccuracy for device with maximum and minimum V_{set}. The device programming is performed by changing pulse amplitude and pulse width, as shown in Figure 5.2c and 5.2d respectively. It can be clearly observed that even due to small variations in device the programming inaccuracy is significant. The programming inaccuracy due to variation for the intermediate resistance state is maximum, while for the device's HRS and LRS states it is minimum as shown in Figure 5.2e and 5.2f. The higher precision for HRS and LRS can be explained because of lower and upper limits to conductive filament formation. Thus, by increasing the time-period or amplitude of the pulse, it is possible to ensure better accuracy in programming the device to HRS and LRS states.

5.4 Existing Matrix Multiplication Technique using Memristor

In many reported matrix multipliers, memristor crossbar is used in an analog way [48,136,137]. In this, as shown in Figure 5.3, each memristor conductance is programmed to different levels according to the first input matrix. The second input matrix is programmed to word line voltage amplitude through a DAC (Digital-to-Analog Converter). When the voltage pulse is applied, there will be a current

associated with each cross point of memristor crossbar array. The sum of current through each cross point in bitline corresponds to the element of output matrix. The output current through bit line is amplified and passed through ADC (Analog-to-Digital Converter) to compute and store the resultant matrix in digital form. However, this approach is highly sensitive to memristor variation [46,48,138-142]. Moreover, programming each memristor device to an intermediate state is itself a challenge. Though techniques have been proposed to improve programming accuracy [143-146], it does not eliminate the problem completely and increases the programming time. Thus, it counters the advantage of using memristor crossbar to speed up the matrix multiplication in the first place.

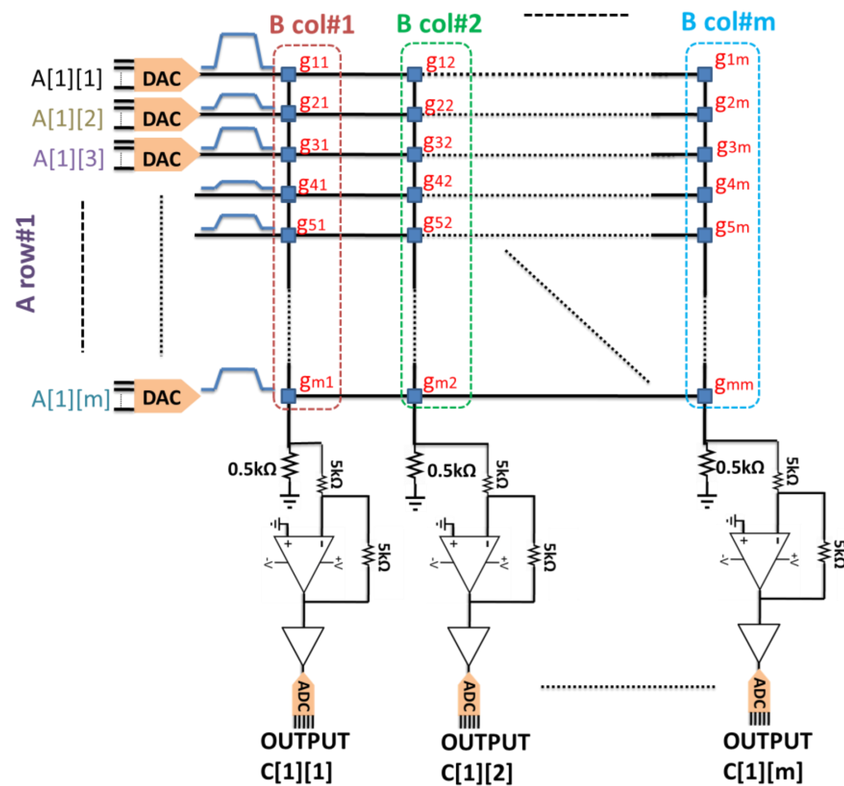


Figure 5.3. Analog matrix multiplication using memristor. The conductance of each memristor cell (e.g. g11, etc.) are sensitive to the device variation and noise.

One other approach proposed in the literature [55,56] is using a digitalized matrix multiplication technique. The digitalized way of matrix multiplication only uses binary state of memristor and is more tolerant of variation. It also saves area since there is no requirement of ADC and DAC, at the expense of speed and power. However, it can be used only for binary matrix multiplication. To perform decimal matrix multiplication, it requires circuit for multiple threshold calculations, and circuit for shift and add operation after each binary multiplication, which leads to significant penalty in delay. Compared to analog counterpart, digitalized approach [56] suffers 3.12x power consumption. In this work, we propose an analog-digital-hybrid matrix multiplication technique, to counter the variation in the memristor device moderate trade-off of power, speed or area as compared to analog matrix multiplication.

5.5 Design for Matrix multiplication

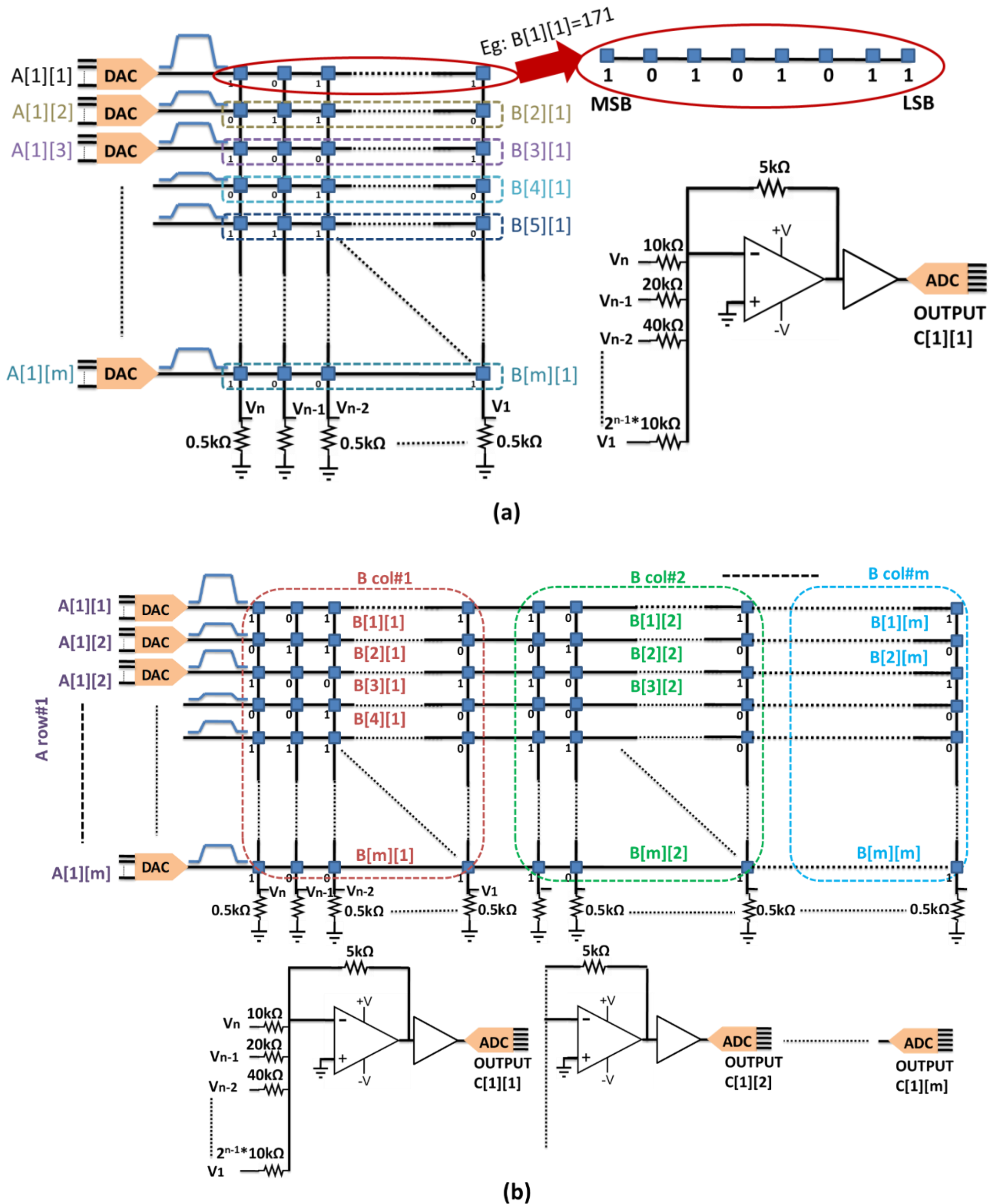


Figure 5.4. (a) Schematic for computation of single output element (C[1][1] = A[1,1..m] x B[1..m, 1]) using the proposed analog digital hybrid matrix multiplication. Each element in B is a n-bit binary number. (b) Full schematic for analog digital hybrid matrix multiplication (not necessarily m copies of Figure 5.4a).

In the proposed matrix multiplication circuit, to calculate output matrix C = A x B, we use an analog-digital-hybrid approach to address the issue of variation in memristor devices. A and B are input matrices with m # of columns and rows respectively. If digitized, each element of A corresponds to a

p-bit binary number and each element of B corresponds to a n-bit binary number, where n and p depends upon the range of values in the input matrices. Each element of A used in multiplication is mapped to programming voltage levels using p-bit DACs during the computation. Each element of Input B in active computation is mapped to the resistance values of n # of memristor cells in a binary approach (i.e., 1 mapped to LRS and 0 mapped to HRS) to improve programming accuracy and decrease the sensitivity to variations. Figure 5.4a explains the circuit to implement multiplication of A row#1 (1st row of matrix A) and B col#1 (1st column of matrix B), consisting of a crossbar array with size m x n single-bit memristor cells and an amplifying circuit.

Using p-bit DACs, the elements A row#1 (i.e., A[1][1], A[1][2], A[1][3],……, A[1][m]) are converted to different levels of voltages (i.e., V(A[1][1]), V(A[1][2]), V(A[1][3]),……, V(A[1][m])) to be fed into the wordlines of the RRAM array, respectively. The top and bottom electrodes of the memristor are connected to the wordlines (whose voltages are controlled by Matrix A) and bitlines (which are then each connected to a resistor r respectively. The ith element (i=1,2,3,….m) of B col#1 (i.e., B[i][1]) is stored in the ith row of the memristor matrix, with conductance of the n # of memristor devices in that row to be g_1(B[i][1]), g_2(B[i][1]), to g_n(B[i][1]). These conductances are the reciprocal of either LRS or HRS values.

The current flowing through j^{th} bit line can be computed as:

$$I_j = \sum_{i=1}^{i=m} V(A[1][i]) * g_j(B[i][1]) \quad (5.3)$$

A small resistance r is used to sense current through each bit line. The value of r (= 0.5kΩ in this example, ~0.02xLRS) should be much smaller than the value of LRS, in order to avoid any alteration in current flowing through each bit line. The voltage across r in each jth bit line can be given as:

$$V_j = I_i * r = \sum_{i=1}^{i=m} r * V(A[1][i]) * g_j(B[i][1]) \quad (5.4)$$

Now, weighted sum of each sampled voltage is added using an inverting sense amplifier. This can be expressed as:

$$V_{sa} = - \sum_{j=1}^{j=n} R_1*[V_j / (2^{n-b}R_2)] \quad (5.5)$$

The value of R_1 and R_2 used in this case is 5kΩ and 10kΩ respectively. The output matrix element C[1][1] is finally computed by amplifying V_{sa} using another inverting buffer followed by an (n+p+$\log_2(m)$)-bit ADC, and is stored in digitized form, where m is input matrix size.

The Figure 5.4a shows computation of single element (C[1][1]) of output matrix. The Figure 5.4b shows the computation of first row of output matrix, where all m # of columns of Matrix B are stored in digital form in memristor crossbar array of size m x (mn). Once the output is computed, in the next step, a set of pulse corresponding to next row of Matrix A is applied to word line to compute next row elements of output Matrix. This process is repeated for all rows of matrix A to perform matrix multiplication.

Similar to the conventional analog multiplication method, I_i (and thus V_i) reflects the levels of the DAC outputs from input A. However, unlike the conventional analog method, memristor cells are only

used as binary devices. This avoids the impact from variations which are problematic for multi-level memristor cells. Moreover, though this proposed hybrid approach requires more memristor cells, the total memristor array area is still only marginal compared with the peripheral circuit. In contrast to digital matrix multiplication technique, which involves multiplication in memristor crossbar array, repetitive threshold calculation, comparator circuit, XNOR circuit, decoding logic followed by a shift and add circuit, all resulting in more performance delay and power loss, the proposed technique is simple to implement with less power consumption and less delay in performance.

5.6 Using proposed matrix multiplication circuit for neural network application

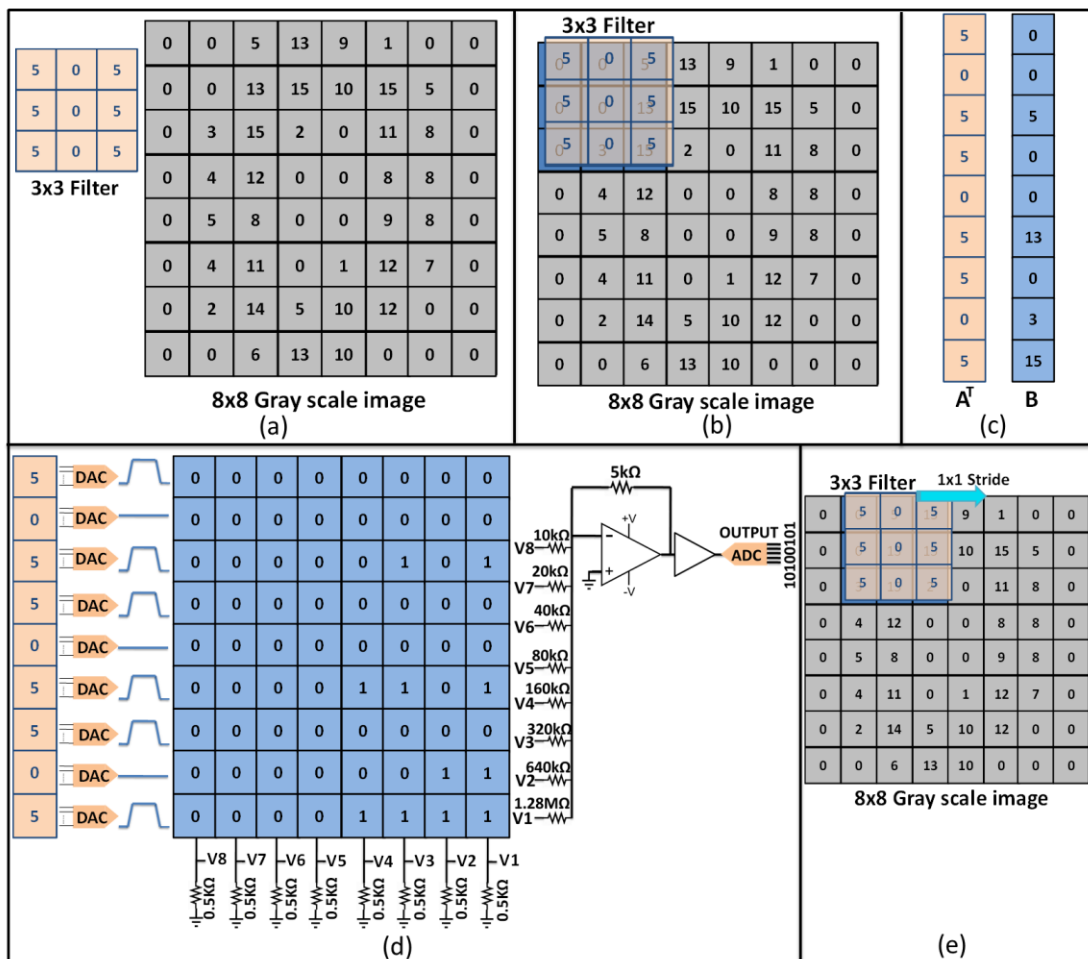


Figure 5.5. Edge detection by convolution of matrix. (a) Filter and Input image. (b) Computation of first element of convolution matrix. (c) Conversion of filter and image patch to 1D. (b) Matrix multiplication using analog-digital hybrid matrix multiplication circuit. (e) Computation of second element of convolution matrix.

We perform image classification by implementing a convolution neural network (CNN) to compare the design's performance and accuracy. A CNN consists of multiple matrix convolution layers, pooling layers, and weighted summation layer followed by an activation function. The matrix convolution layer is the key component of CNN and is the most computationally heavy block. In this, convolution of input image takes place through mathematical filters by repeated matrix multiplication, to detect the presence

of a set of features in the image. In this paper, we discuss only the matrix multiplication component in matrix convolution layer of the image classification using CNN.

A set of 250 hand-written digit images from the UCI data set [147] were used as inputs to matrix convolution layer in CNN, for matrix multiplication. The original 8x8 pixel grayscale images were passed through a 3x3-dimensional filter, as shown in Figure 5.5b. The convolution is performed by fattening out image and filter first in one-dimension matrix, as shown in Figure 5.5c, and performing matrix multiplication to compute the output element, as shown in Figure 5.5d. The image pixel data is mapped to memristor crossbar, and filter is passed as word line voltage. The image pixel is mapped to memristor crossbar by applying a programming voltage of 2.6V and pulse width of 20ps and varying them w.r.t inputs. The output is computed using summation of weighted current flowing through each bit line, as discussed in section 5.5. The filter is shifted by 1 pixel and the experiment is repeated to compute the next element of convolution matrix, as shown in Figure 5.5e. The results of the matrix multiplication using the memristor crossbar array, and the effect of variations, with both the analog matrix multiplication method and the proposed analog-digital-hybrid matrix multiplication method were analyzed and compared, which are discussed in following section 5.7.

5.7 Result and Discussions

5.7.1 PPA Analysis

It is observed that the total power of the proposed approach increases modestly compared to that of the analog matrix multiplication technique, as shown in Figure 5.6a. The reason behind the trend is that a major portion of power during matrix multiplication is consumed by peripheral devices comprised of the sense amplifier, ADC and DAC, as shown in Figure 5.6b. However, during the initial programing stage, where a larger memristor array is required to be initialized as per the input matrix, it causes additional power dissipation.

In the matrix multiplication computation in section 5.6, it is observed that the average speed for analog-digital-hybrid matrix multiplication technique degrades by ~4 to 8.2% overall, as in analog-digital-hybrid matrix multiplication, higher resistance values are required for the summation stage i.e., $2^{n-1}R_2$ (e.g., ~250 times higher resistance, if range of values is 256), thus adding propagation delay to the signal. In addition, the sense amplifier inputs need to be stabilized before computing the output, which adds to the delay.

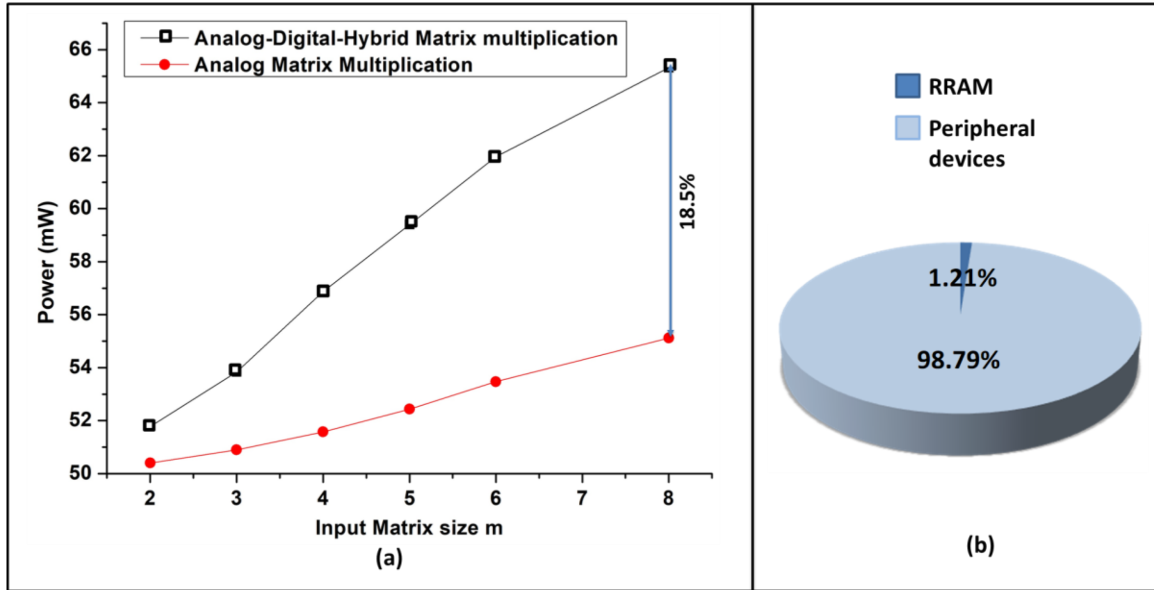
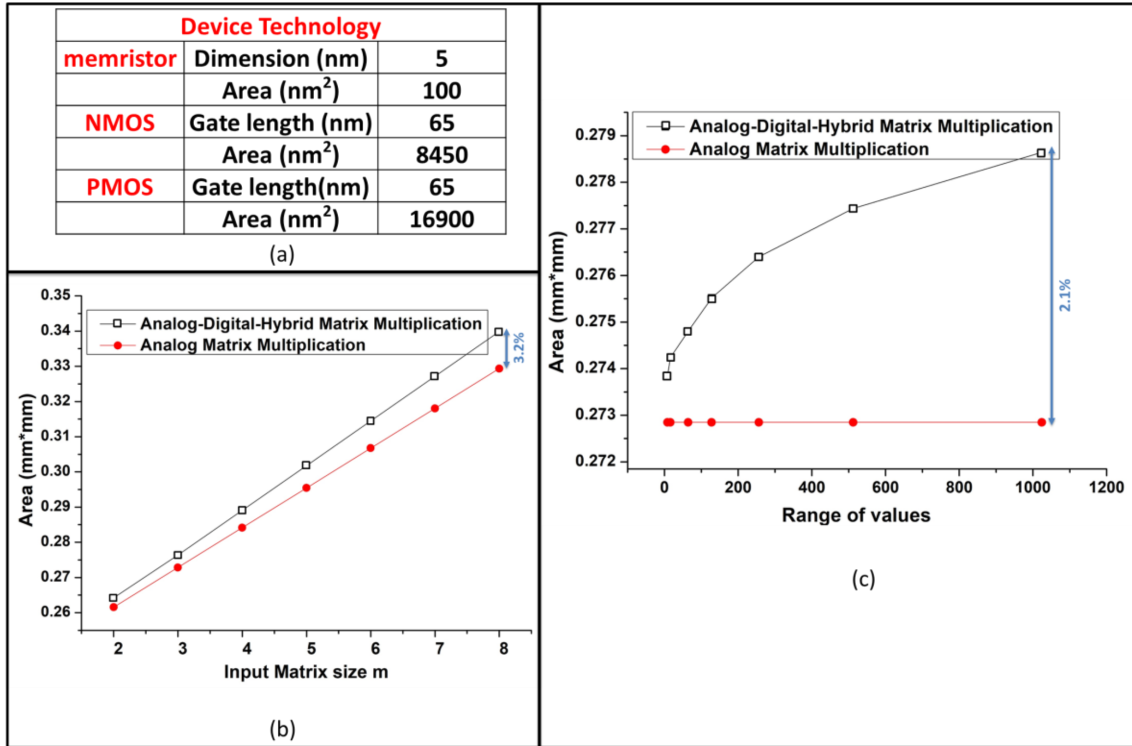


Figure 5.6. (a) Total Power (memristor programming + Matrix multiplication) for analog design technique and analog-digital-hybrid design technique. (b) Power distribution (for Matrix multiplication only) for analog-digital-hybrid matrix multiplication technique.

The area of the design is evaluated based on number of memristors and transistors and widths of transistors used in the schematic. (Figure 5.7a). Figure 5.7b shows the estimated area penalty with respect to analog matrix multiplication varying with matrix size when the range of element values (p and n) is kept constant. When matrix size is varied from 2 to 8, keeping range of element values as 256 (i.e. $p = n = 8$ for Matrix A and B), the area increase varies from 1.1% to 3.2% for the proposed design technique compared to analog matrix multiplication technique. Figure 5.7c shows the estimated area penalty varying with range of element values, keeping matrix size the same. When range of element values is varied from 16 to 1024 (i.e. $p = n = 4$ to 10), keeping matrix size of 3, the area increase varies from 0.9% to 2.1% for the proposed design technique compared to analog matrix multiplication technique. The increase in area is due to the need for circuit to sum up the weighted currents and a larger memristor array for binary processing of matrix.

In comparison to digital matrix multiplication method (without including externally required shift and add circuit in digital matrix multiplication method) [55], the estimated power consumption is reduced to 37% and the speed is enhanced by 277%, however, the gain is at the expense of area penalty of approximately 11.65 times, for a matrix size of 8. The reason behind the increase in area consumption is the use of DAC and ADC circuits in analog-digital-hybrid matrix multiplication, which are not required in digital matrix multiplication circuit.



Device Technology		
memristor	Dimension (nm)	5
	Area (nm^2)	100
NMOS	Gate length (nm)	65
	Area (nm^2)	8450
PMOS	Gate length(nm)	65
	Area (nm^2)	16900

Figure 5.7. (a) Device dimensions used for design evaluation. (b) Circuit Area vs Matrix size for analog matrix multiplication technique and analog-digital-hybrid design technique for range of element values as 256 and input matrix size varying from 2 to 8. (c) Circuit Area vs Matrix size for analog matrix multiplication technique and analog-digital-hybrid design technique for input matrix size 3 and range of element values varying from 16 to 1024 (i.e. *n* from 4 to 10 and assuming *n* = *p*).

5.7.2 Impact of variations in memristor

The resistance of the memristor device is a function of the gap between the formation of the conductive filament. The stochastic nature of memristor leads to variations in conductive filament growth and thus the resistance (or conductance) of the device, as discussed in section 5.3. We use cycle A as the reference memristor behavior. The device behavior, as shown in Figure 5.2b, would vary between the black and red curves, corresponding to Cycle A and Cycle B, respectively. The average variation in conductive filament growth between Cycle A with maximum V_{set} and another cycle is defined as Δg. Δg for cycle B with minimum V_{set} in the measured fabricated memristor, is observed to be ~ 0.21nm. To study the effect of variation, we induce this variation (or change) in the conductive filament gap. This is done by varying model from Cycle A (i.e., model parameter γ=17.59) with maximum V_{set} to Cycle B (i.e., γ=18.04) with minimum V_{set}, discussed in section 5.3, with intermediate γ values and observe the effect on output computation for matrix multiplication in convolution layer of CNN, discussed in section 5.6. These γ values correspond to Δg from 0 to 0.21nm. We define the output error as change in output value w.r.t Cycle A (model parameter γ=17.59), indicating how far the output is from that of the reference. As shown in Figure 5.8a, the variation in output of the analog matrix multiplication technique is much more dominant as compared to the analog-digital-hybrid matrix

multiplication method. Moreover, as the range of element values is increased, the effect of variation becomes more severe in analog matrix multiplication, as shown in Figure 5.8b.

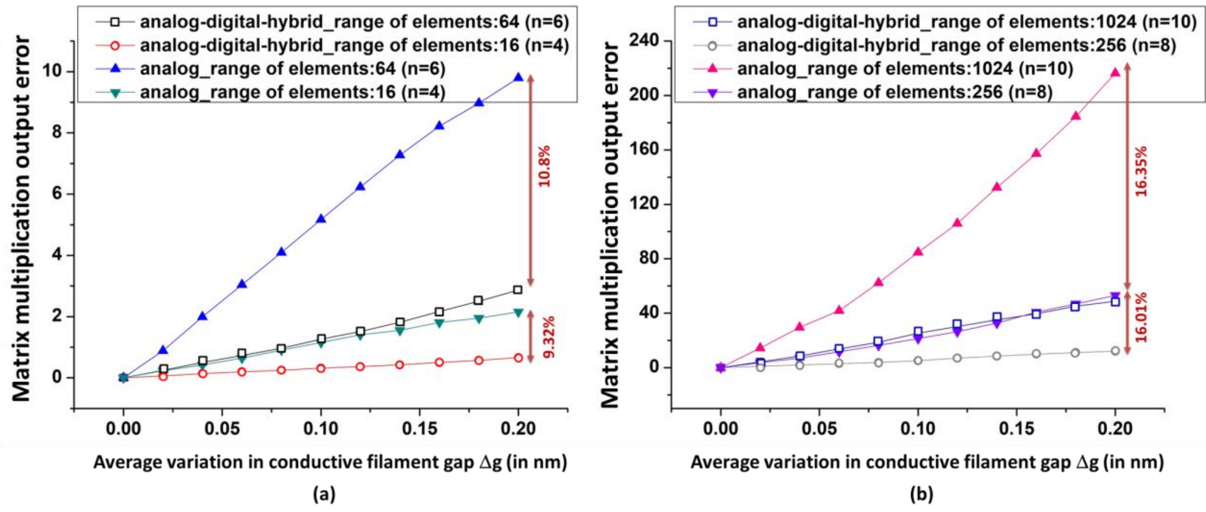


Figure 5.8. Matrix multiplication computation output error (w.r.t computation in cycle-A i.e., γ=17.59) between analog design technique and analog-digital-hybrid design technique with respect to variations in memristor devices. (a) Matrix multiplication output error for range of element values as 64 ($n = p = 6$) and 16 ($n = p = 4$). (b) Matrix multiplication output error for range of element values as 1024 ($n = p = 10$) and 256 ($n = p = 8$).

Due to such impact, matrix multiplication using memristor crossbar array in analog way becomes less practical for matrix with large range of element values (i.e., large p and n), even with significant advantages in power and performance with respect to CMOS based matrix multiplication circuits [148,149]. While in the proposed analog-digital-hybrid matrix multiplication technique the vulnerability due to variation is less and does not deteriorates with increasing range of elements values (i.e., large p and n).

This high level of variation tolerance is expected in the proposed circuit because by digitally storing matrix in memristor crossbar, no intermediate resistance levels in the memristor devices are used. In case of storing data in analog way in memristor, the effective difference between resistance states is comparatively smaller. Binary memristor cells are also more robust in terms of retention and endurance. These benefits are particularly helpful with scaling of the circuit when variation, retention and endurance could hurt more at the circuit level.

5.8 Summary

The analog-digital hybrid approach of memristor based matrix multiplication design is proposed. The performance and accuracy of the proposed design is examined using an example of matrix multiplication in convolution neural network (CNN). Comparing with the widely used analog approach, the proposed method demonstrates significant improvement against the impact of variation with small

penalty of area, power and performance. The robustness against variation in the proposed approach would be more beneficial with increasing matrix size and range of element values. Thus, the proposed design could play an important role in moving forward towards faster machine learning accelerators with better accuracy.

Chapter 6
Conclusions and Future Work

6.1 Conclusions

The research focused on TiO_2 based memristive devices, along with biomaterials for the applications in in-memory computing. Three types of TiO_2 based memristive devices were explored and their switching mechanisms were discussed, along with various applications in in-memory computing.

The first device, based on TiO_2 with maple leaves as oxide layers, exhibited a unique property of capacitive coupled behavior at low voltage, while memristive behavior at high voltage. The existence of capacitive coupled and memristive behavior, modulated by programming voltage, could provide way for new reprogrammable devices for in-memory computing.

The second memristor, based on TiO_2, graphene and DNA as oxide layers, shows resistive switching memory behavior with stable multi-level resistance states, which enables 2-bit storage capacity in a single device. The device provides an alternative for high density memory using memristor, with easier fabrication technique and without any loss of accuracy. Using the device, parallel logic operations for in-memory computing was performed, which could provide a way for more faster and energy efficient solution for in-memory logic.

Further, the third memristor device, based on TiO_2 as a single oxide layer, was utilized to study and design variation tolerant matrix multiplication system for in-memory computing. It was demonstrated that with respect to conventional analog matrix multiplication using memristor, the proposed analog-digital-hybrid matrix multiplication could improve the accuracy up to 16.35%, with the power, performance and area loss up to 18.5%, 8.2% and 3.2% respectively.

The proposed memristors with their novel applications could provide a new prospect for engineering devices and circuits for in-memory computing applications.

6.2 Future Work

For future work, the devices and circuits could be modified and explored further to improve the area density and power. The detailed research for the future work is listed as follows:

1. Development of selector based memristor devices in order to avoid sneak path current, is one of the major tasks for future work. In order to avoid sneak path current without sacrificing circuit packing density due to added transistors, addition of selector materials integrated within memristor devices could prove helpful.
2. The deposition process used for biomaterials in the research was spin coating. In spic coating method, it is difficult to achieve uniformity in devices and control the thickness of the layers.

Therefore, in order to reduce variations among devices and increasing reproducibility of devices with same oxide thickness, more sophisticated deposition method such as MLD (Molecular layer deposition) process can be used.

3. The fabrication technique used in the research is shadow mask process, where masks with dimensions of um scale were used. This process enables fast and cheap prototyping. However, it not only adds area to the device, but also increases cycle to cycle variations, as the probability of multiple conductive filaments formation increases. Consequently, as the number of conductive filaments formed between top and bottom electrode increases and varies with each cycle, the cycle to cycle variation also increases in the device. Therefore, in order to reduce the cycle to cycle variations in the fabricated device, the mask dimensions and thus device area should be reduced.
4. The fabricated devices, especially those using biomaterials present high current. Though the device shows unique features, high currents increases the power dissipation. In order to reduce the current, as disused above, MLD process can be explored to control film thickness and area of the device can be reduced to avoid multiple conductive filament formation. In addition to that, materials such as Al_2O_3 (which has shown low power memristive effect) can be used along with the existing oxide layer.
5. The proposed device based on TiO2-graphene-DNA as functional layer has shown four stable resistance state, which was utilized to demonstrate 2-bit memory storage and parallel operations. The device could be engineered to support a greater number of stable resistance state, by increase the number of active layer materials in addition to graphene layer.

Bibliography

[1] M. Shah and R. Kapdi, “Object detection using deep neural networks,” *Proc. 2017 Int. Conf. Intell. Comput. Control Syst. ICICCS 2017*, vol. 2018-Janua, pp. 787–790, 2017, doi: 10.1109/ICCONS.2017.8250570.

[2] S. S. Farfade, M. Saberian, and L. J. Li, “Multi-view face detection using Deep convolutional neural networks,” *ICMR 2015 - Proc. 2015 ACM Int. Conf. Multimed. Retr.*, pp. 643–650, 2015, doi: 10.1145/2671188.2749408.

[3] X. Sun, P. Wu, and S. C. H. Hoi, “Face detection using deep learning: An improved faster RCNN approach,” *Neurocomputing*, vol. 299, pp. 42–50, 2018, doi: 10.1016/j.neucom.2018.03.030.

[4] X. Chen, H. Ma, J. Wan, B. Li, and T. Xia, “Multi-view 3D object detection network for autonomous driving,” *Proc. - 30th IEEE Conf. Comput. Vis. Pattern Recognition, CVPR 2017*, vol. 2017-Janua, pp. 6526–6534, 2017, doi: 10.1109/CVPR.2017.691.

[5] X. Wang, W. Zhang, X. Wu, L. Xiao, Y. Qian, and Z. Fang, “Real-time vehicle type classification with deep convolutional neural networks,” *J. Real-Time Image Process.*, vol. 16, no. 1, pp. 5–14, 2019, doi: 10.1007/s11554-017-0712-5.

[6] M. Bojarski *et al.*, “End to End Learning for Self-Driving Cars,” pp. 1–9, 2016, [Online]. Available: http://arxiv.org/abs/1604.07316.

[7] R. Yan, “‘Chitty-chitty-chat bot’: Deep learning for conversational AI,” *IJCAI Int. Jt. Conf. Artif. Intell.*, vol. 2018-July, pp. 5520–5526, 2018.

[8] P. C. Yang, K. Sasaki, K. Suzuki, K. Kase, S. Sugano, and T. Ogata, “Repeatable Folding Task by Humanoid Robot Worker Using Deep Learning,” *IEEE Robot. Autom. Lett.*, vol. 2, no. 2, pp. 397–403, 2017, doi: 10.1109/LRA.2016.2633383.

[9] V. Mnih *et al.*, “Playing Atari with Deep Reinforcement Learning,” pp. 1–9, 2013, [Online]. Available: http://arxiv.org/abs/1312.5602.

[10] T. M. Mitchell, “The Need for Biases in Learning Generalizations,” *Readings Mach. Learn.*, no. CBM-TR-117, pp. 184–191, 1980, [Online]. Available: http://citeseerx.ist.psu.edu/viewdoc/summary?doi=10.1.1.19.5466.

[11] M. Education, “Readable introduction to Unix has plenty of examples,” pp. 510–511.

[12] M. M. T. Carbonel, G. jaime, Michalski, S.Ryszard, “an-Overview-of-Machine.Pdf.” p. 23, 1983.

[13] P. A. Merolla *et al.*, “A million spiking-neuron integrated circuit with a scalable communication network and interface,” *Science (80-.).*, vol. 345, no. 6197, pp. 668–673, 2014, doi: 10.1126/science.1254642.

[14] A. Sebastian *et al.*, “Temporal correlation detection using computational phase-change memory,” *Nat. Commun.*, vol. 8, no. 1, 2017, doi: 10.1038/s41467-017-01481-9.

[15] P. Jacob *et al.*, “Mitigating memory wall effects in high-clock-rate and multicore CMOS 3-D processor memory stacks,” *Proc. IEEE*, vol. 97, no. 1, pp. 108–122, 2009, doi: 10.1109/JPROC.2008.2007472.

[16] D. Ielmini and H. S. P. Wong, “In-memory computing with resistive switching devices,” *Nat. Electron.*, vol. 1, no. 6, pp. 333–343, 2018, doi: 10.1038/s41928-018-0092-2.

[17] L. O. Chua, “Memristor—The Missing Circuit Element,” *IEEE Trans. Circuit Theory*, vol. 18, no. 5, pp. 507–519, 1971, doi: 10.1109/TCT.1971.1083337.

[18] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, “The missing memristor found,” *Nature*, vol. 453, no. 7191, pp. 80–83, 2008, doi: 10.1038/nature06932.

[19] R. Waser, R. Dittmann, C. Staikov, and K. Szot, “Redox-based resistive switching memories nanoionic mechanisms, prospects, and challenges,” *Adv. Mater.*, vol. 21, no. 25–26, pp. 2632–2663, 2009, doi: 10.1002/adma.200900375.

[20] C. Schindler, M. Weides, M. N. Kozicki, and R. Waser, “Low current resistive switching in Cu-SiO2 cells,” *Appl. Phys. Lett.*, vol. 92, no. 12, pp. 1–4, 2008, doi: 10.1063/1.2903707.

[21] A. C. Torrezan, J. P. Strachan, G. Medeiros-Ribeiro, and R. S. Williams, “Sub-nanosecond switching of a tantalum oxide memristor,” *Nanotechnology*, vol. 22, no. 48, 2011, doi: 10.1088/0957-4484/22/48/485203.

[22] S. H. Jo, K.-H. Kim, and W. Lu, “High-Density Crossbar Arrays Based on a Si Memristive System,” *Nano Lett.*, vol. 9, no. 2, pp. 870–874, 2009, doi: 10.1021/nl8037689.

[23] H. S. P. Wong *et al.*, “Metal-oxide RRAM,” *Proc. IEEE*, vol. 100, no. 6, pp. 1951–1970, 2012, doi: 10.1109/JPROC.2012.2190369.

[24] M. Lanza *et al.*, “Recommended Methods to Study Resistive Switching Devices,” *Adv. Electron. Mater.*, vol. 5, no. 1, pp. 1–28, 2019, doi: 10.1002/aelm.201800143.

[25] Z. Tang, Y. Wang, Y. Chi, and L. Fang, “Comprehensive sensing current analysis and its guideline for the worst-case scenario of rram read operation,” *Electron.*, vol. 7, no. 10, pp. 14–16, 2018, doi: 10.3390/electronics7100224.

[26] J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, and R. S. Williams, “Memristive switching mechanism for metal/oxide/metal nanodevices,” *Nat. Nanotechnol.*, vol. 3, no. 7, pp. 429–433, 2008, doi: 10.1038/nnano.2008.160.

[27] L. Goux *et al.*, “Evidences of oxygen-mediated resistive-switching mechanism in TiN\ HfO 2 \Pt cells,” *Appl. Phys. Lett.*, vol. 97, no. 24, pp. 2010–2013, 2010, doi: 10.1063/1.3527086.

[28] H. Y. Lee *et al.*, “Low power and high speed bipolar switching with a thin reactive ti buffer layer in robust HfO2 based RRAM,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 3–6, 2008, doi: 10.1109/IEDM.2008.4796677.

[29] Y. Wu, B. Lee, and H. S. P. Wong, “Al2O3-based RRAM using atomic layer deposition (ALD) with 1-

μa RESET current,” *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1449–1451, 2010, doi: 10.1109/LED.2010.2074177.

[30] W. Kim et al., "Forming-free nitrogen-doped AlOX RRAM with sub-μA programming current," 2011 Symposium on VLSI Technology - Digest of Technical Papers, Honolulu, HI, 2011, pp. 22-23.

[31] T. Fu *et al.*, “Bioinspired bio-voltage memristors,” *Nat. Commun.*, vol. 11, no. 1, pp. 1–10, 2020, doi: 10.1038/s41467-020-15759-y.

[32] M. K. Hota, M. K. Bera, B. Kundu, S. C. Kundu, and C. K. Maiti, “A natural silk fibroin protein-based transparent bio-memristor,” *Adv. Funct. Mater.*, vol. 22, no. 21, pp. 4493–4499, 2012, doi: 10.1002/adfm.201200073.

[33] B. Sun, D. Liang, X. Li, and P. Chen, “Nonvolatile bio-memristor fabricated with natural bio-materials from spider silk,” *J. Mater. Sci. Mater. Electron.*, vol. 27, no. 4, pp. 3957–3962, 2016, doi: 10.1007/s10854-015-4248-9.

[34] Y. C. Chen, H. C. Yu, C. Y. Huang, W. L. Chung, S. L. Wu, and Y. K. Su, “Nonvolatile bio-memristor fabricated with egg albumen film,” *Sci. Rep.*, vol. 5, pp. 1–12, 2015, doi: 10.1038/srep10022.

[35] S. Mao *et al.*, “A Bio-memristor with Overwhelming Capacitance Effect,” *Electron. Mater. Lett.*, vol. 15, no. 5, pp. 547–554, 2019, doi: 10.1007/s13391-019-00150-x.

[36] X. He *et al.*, “Transient Resistive Switching Devices Made from Egg Albumen Dielectrics and Dissolvable Electrodes,” *ACS Appl. Mater. Interfaces*, vol. 8, no. 17, pp. 10954–10960, 2016, doi: 10.1021/acsami.5b10414.

[37] S. Ham, S. Choi, H. Cho, S. I. Na, and G. Wang, “Photonic Organolead Halide Perovskite Artificial Synapse Capable of Accelerated Learning at Low Power Inspired by Dopamine-Facilitated Synaptic Activity,” *Adv. Funct. Mater.*, vol. 29, no. 5, pp. 1–8, 2019, doi: 10.1002/adfm.201806646.

[38] B. Ku, B. Koo, A. S. Sokolov, M. J. Ko, and C. Choi, “Two-terminal artificial synapse with hybrid organic–inorganic perovskite (CH3NH3)PbI3 and low operating power energy (∼47 fJ/μm2),” *J. Alloys Compd.*, vol. 833, 2020, doi: 10.1016/j.jallcom.2020.155064.

[39] Y. Y. Chen *et al.*, “Endurance/Retention Trade-off on <formula formulatype="inline"><tex Notation="TeX">$\hbox{HfO}_{2}/\hbox{Metal}$</tex> </formula> Cap 1T1R Bipolar RRAM,” *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 1114–1121, 2013, doi: 10.1109/TED.2013.2241064.

[40] Y. Chen and C. Petti, “ReRAM technology evolution for storage class memory application,” *Eur. Solid-State Device Res. Conf.*, vol. 2016-October, pp. 432–435, 2016, doi: 10.1109/ESSDERC.2016.7599678.

[41] Y. Ji *et al.*, “Integrated all-organic 8 × 8 one transistor-one resistor (1T-1R) crossbar resistive switching memory array,” *Org. Electron.*, vol. 29, pp. 66–71, 2016, doi: 10.1016/j.orgel.2015.11.020.

[42] C. Xu *et al.*, “Overcoming the challenges of crossbar resistive memory architectures,” *2015 IEEE*

21st Int. Symp. High Perform. Comput. Archit. HPCA 2015, pp. 476–488, 2015, doi: 10.1109/HPCA.2015.7056056.

[43] P. Schrögmeier *et al.*, “Time discrete voltage sensing and iterative programming control for a 4F2 multilevel CBRAM,” *IEEE Symp. VLSI Circuits, Dig. Tech. Pap.*, pp. 186–187, 2007, doi: 10.1109/VLSIC.2007.4342708.

[44] L. Sun *et al.*, “Self-selective van der Waals heterostructures for large scale memory array,” *Nat. Commun.*, vol. 10, no. 1, pp. 1–7, 2019, doi: 10.1038/s41467-019-11187-9.

[45] H. Kim, M. P. Sah, C. Yang, and L. O. Chua, “Memristor-based multilevel memory,” *2010 12th Int. Work. Cell. Nanoscale Networks their Appl. CNNA 2010*, vol. 1, no. 5, pp. 1–6, 2010, doi: 10.1109/cnna.2010.5430320.

[46] F. Alibart, L. Gao, B. D. Hoskins, and D. B. Strukov, “High precision tuning of state for memristive devices by adaptable variation-tolerant algorithm,” *Nanotechnology*, vol. 23, no. 7, pp. 3–10, 2012, doi: 10.1088/0957-4484/23/7/075201.

[47] R. Berdan, T. Prodromakis, and C. Toumazou, “High precision analogue memristor state tuning,” *Electron. Lett.*, vol. 48, no. 18, pp. 1105–1107, 2012, doi: 10.1049/el.2012.2295.

[48] B. Li, P. Gu, Y. Wang, and H. Yang, “Exploring the Precision Limitation for RRAM-Based Analog Approximate Computing,” *IEEE Des. Test*, vol. 33, no. 1, pp. 51–58, 2016, doi: 10.1109/MDAT.2015.2487218.

[49] Q. Luo *et al.*, “Super non-linear RRAM with ultra-low power for 3D vertical nano-crossbar arrays,” *Nanoscale*, vol. 8, no. 34, pp. 15629–15636, 2016, doi: 10.1039/c6nr02029a.

[50] M. J. Lee *et al.*, “Low-temperature-grown transition metal oxide based storage materials and oxide transistors for high- density non-volatile memory,” *Adv. Funct. Mater.*, vol. 19, no. 10, pp. 1587–1593, 2009, doi: 10.1002/adfm.200801032.

[51] E. Linn, R. Rosezin, S. Tappertzhofen, U. Böttger, and R. Waser, “Beyond von Neumann - Logic operations in passive crossbar arrays alongside memory operations,” *Nanotechnology*, vol. 23, no. 30, 2012, doi: 10.1088/0957-4484/23/30/305205.

[52] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, “Memristive switches enable stateful logic operations via material implication,” *Nature*, vol. 464, no. 7290, pp. 873–876, 2010, doi: 10.1038/nature08940.

[53] Z. Yang, Y. Ma, and L. Wei, “Functionally complete boolean logic and adder design based on 2T2R RRAMs for post-CMOS in-memory computing,” *Proc. ACM Gt. Lakes Symp. VLSI, GLSVLSI*, pp. 147–152, 2019, doi: 10.1145/3299874.3317993.

[54] S. N. Truong and K. S. Min, “New memristor-based crossbar array architecture with 50-% area reduction and 48-% power saving for matrix-vector multiplication of analog neuromorphic computing,” *J. Semicond. Technol. Sci.*, vol. 14, no. 3, pp. 356–363, 2014, doi: 10.5573/JSTS.2014.14.3.356.

[55] L. Ni, Y. Wang, H. Yu, W. Yang, C. Weng, and J. Zhao, "An energy-efficient matrix multiplication accelerator by distributed in-memory computing on binary RRAM crossbar," *Proc. Asia South Pacific Des. Autom. Conf. ASP-DAC*, vol. 25-28-Janu, pp. 280–285, 2016, doi: 10.1109/ASPDAC.2016.7428024.

[56] H. Yu, L. Ni, and H. Huang, "Distributed in-memory computing on binary memristor-crossbar for machine learning," *Stud. Comput. Intell.*, vol. 701, no. 3, pp. 275–304, 2017, doi: 10.1007/978-3-319-51724-7_12.

[57] W. Ma, M. A. Zidan, and W. D. Lu, "Neuromorphic computing with memristive devices," *Sci. China Inf. Sci.*, vol. 61, no. 6, pp. 1–9, 2018, doi: 10.1007/s11432-017-9424-y.

[58] I. Boybat *et al.*, "Neuromorphic computing with multi-memristive synapses," *Nat. Commun.*, vol. 9, no. 1, pp. 1–12, 2018, doi: 10.1038/s41467-018-04933-y.

[59] P. Sheridan and W. Lu, "Memristor Networks," *Memristor Networks*, 2014, doi: 10.1007/978-3-319-02630-5.

[60] D. Ielmini, "Brain-inspired computing with resistive switching memory (RRAM): Devices, synapses and neural networks," *Microelectron. Eng.*, vol. 190, pp. 44–53, 2018, doi: 10.1016/j.mee.2018.01.009.

[61] L. Chua, V. Sbitnev, and H. Kim, "Hodgkin-Huxley axon is made of memristors," *Int. J. Bifurc. Chaos*, vol. 22, no. 3, pp. 1–48, 2012, doi: 10.1142/S021812741230011X.

[62] L. Chua, "Memristor Networks," *Memristor Networks*, 2014, doi: 10.1007/978-3-319-02630-5.

[63] M. Teimoori, A. Ahmadi, S. Alirezaee, S. V. A. D. Makki, and M. Ahmadi, "A novel memristor based integrate-and-fire neuron implementation using material implication logic," *Can. Conf. Electr. Comput. Eng.*, vol. 2015-June, no. June, pp. 1176–1179, 2015, doi: 10.1109/CCECE.2015.7129442.

[64] J. Q. Yang *et al.*, "Leaky integrate-and-fire neurons based on perovskite memristor for spiking neural networks," *Nano Energy*, vol. 74, p. 104828, 2020, doi: 10.1016/j.nanoen.2020.104828.

[65] R. and M. A. Stefan Tappertzhofen, Ilia Valov, Tohru Tsuruoka, Tsuyoshi Hasegawa, "Generic Relevance of Counter Charges," ACS Nano, vol. 7, no. 7, pp. 6396–6402, 2013.

[66] S. Tappertzhofen, S. Menzel, I. Valov, and R. Waser, "Redox processes in silicon dioxide thin films using copper microelectrodes," Appl. Phys. Lett., vol. 99, no. 20, pp. 2011–2014, 2011, doi: 10.1063/1.3662013.

[67] B. Sun et al., "A Unified Capacitive-Coupled Memristive Model for the Nonpinched Current-Voltage Hysteresis Loop," Nano Lett., vol. 19, no. 9, pp. 6461–6465, 2019, doi: 10.1021/acs.nanolett.9b02683.

[68] G. Zhou, X. Yang, L. Xiao, B. Sun, and A. Zhou, "Investigation of a submerging redox behavior in Fe2O3 solid electrolyte for resistive switching memory," Appl. Phys. Lett., vol. 114, no. 16, 2019, doi: 10.1063/1.5089147.

[69] S. et al. Archibald, “Ac ce pte d M us pt,” Geophys. Res. Lett., vol. in press, pp. 0–31, 2017.

[70] D. Y. Cho, M. Luebben, S. Wiefels, K. S. Lee, and I. Valov, “Interfacial Metal-Oxide Interactions in Resistive Switching Memories,” ACS Appl. Mater. Interfaces, vol. 9, no. 22, pp. 19287–19295, 2017, doi: 10.1021/acsami.7b02921.

[71] F. Messerschmitt, M. Jansen, and J. L. M. Rupp, “When Memristance Crosses the Path with Humidity Sensing—About the Importance of Protons and Its Opportunities in Valence Change Memristors,” Adv. Electron. Mater., vol. 4, no. 12, pp. 1–10, 2018, doi: 10.1002/aelm.201800282.

[72] S. Zhu et al., “An excellent pH-controlled resistive switching memory device based on self-colored (C7H7O4N): N extracted from a lichen plant,” J. Mater. Chem. C, vol. 7, no. 25, pp. 7593–7600, 2019, doi: 10.1039/c8tc06207b.

[73] S. Mao et al., “PH-Modulated memristive behavior based on an edible garlic-constructed bio-electronic device,” New J. Chem., vol. 43, no. 24, pp. 9634–9640, 2019, doi: 10.1039/c9nj02433f.

[74] L. Zheng et al., “Metal ions redox induced repeatable nonvolatile resistive switching memory behavior in biomaterials,” ACS Appl. Bio Mater., vol. 1, no. 2, pp. 496–501, 2018, doi: 10.1021/acsabm.8b00226.

[75] I. Salaoru, A. Khiat, Q. Li, R. Berdan, and T. Prodromakis, “Pulse-induced resistive and capacitive switching in TiO2 thin film devices,” Appl. Phys. Lett., vol. 103, no. 23, 2013, doi: 10.1063/1.4840316.

[76] H. Wang et al., “Configurable Resistive Switching between Memory and Threshold Characteristics for Protein-Based Devices,” Adv. Funct. Mater., vol. 25, no. 25, pp. 3825–3831, 2015, doi: 10.1002/adfm.201501389.

[77] N. R. Hosseini and J. S. Lee, “Biocompatible and Flexible Chitosan-Based Resistive Switching Memory with Magnesium Electrodes,” Adv. Funct. Mater., vol. 25, no. 35, pp. 5586–5592, 2015, doi: 10.1002/adfm.201502592.

[78] H. Wang et al., “Sericin for resistance switching device with multilevel nonvolatile memory,” Adv. Mater., vol. 25, no. 38, pp. 5498–5503, 2013, doi: 10.1002/adma.201301983.

[79] N. Raeis Hosseini and J. S. Lee, “Resistive switching memory based on bioinspired natural solid polymer electrolytes,” ACS Nano, vol. 9, no. 1, pp. 419–426, 2015, doi: 10.1021/nn5055909.

[80] G. Zhou et al., “Investigation of the behaviour of electronic resistive switching memory based on MoSe2-doped ultralong Se microwires,” Appl. Phys. Lett., vol. 109, no. 14, 2016, doi: 10.1063/1.4962655.

[81] G. Zhou et al., “Coexistence of Negative Differential Resistance and Resistive Switching Memory at Room Temperature in TiOx Modulated by Moisture,” Adv. Electron. Mater., vol. 4, no. 4, pp. 1–12, 2018, doi: 10.1002/aelm.201700567.

[82] I. Valov et al., “Nanobatteries in redox-based resistive switches require extension of memristor

theory," Nat. Commun., vol. 4, pp. 1771–1779, 2013, doi: 10.1038/ncomms2784.

[83] M. S. Kadhim et al., " Existence of Resistive Switching Memory and Negative Differential Resistance State in Self-Colored MoS 2 /ZnO Heterojunction Devices ," ACS Appl. Electron. Mater., vol. 1, no. 3, pp. 318–324, 2019, doi: 10.1021/acsaelm.8b00070.

[84] X. Yan et al., "Self-Assembled Networked PbS Distribution Quantum Dots for Resistive Switching and Artificial Synapse Performance Boost of Memristors," Adv. Mater., vol. 31, no. 7, pp. 1–9, 2019, doi: 10.1002/adma.201805284.

[85] C. Zhang et al., "Bioinspired Artificial Sensory Nerve Based on Nafion Memristor," Adv. Funct. Mater., vol. 29, no. 20, pp. 1–10, 2019, doi: 10.1002/adfm.201808783.

[86] S. Seo et al., "Recent Progress in Artificial Synapses Based on Two-Dimensional van der Waals Materials for Brain-Inspired Computing," ACS Appl. Electron. Mater., vol. 2, no. 2, pp. 371–388, 2020, doi: 10.1021/acsaelm.9b00694.

[87] L. Shao et al., "Optoelectronic Properties of Printed Photogating Carbon Nanotube Thin Film Transistors and Their Application for Light-Stimulated Neuromorphic Devices," ACS Appl. Mater. Interfaces, vol. 11, no. 12, pp. 12161–12169, 2019, doi: 10.1021/acsami.9b02086.

[88] Y. Wang et al., "Self-Doping Memristors with Equivalently Synaptic Ion Dynamics for Neuromorphic Computing," ACS Appl. Mater. Interfaces, vol. 11, no. 27, pp. 24230–24240, 2019, doi: 10.1021/acsami.9b04901.

[89] M. M. Shulaker *et al.*, "Carbon nanotube computer," *Nature*, vol. 501, no. 7468, pp. 526–530, 2013, doi: 10.1038/nature12502.

[90] T. Hasegawa, K. Terabe, T. Tsuruoka, and M. Aono, "Atomic switch: Atom/ion movement controlled devices for beyond von-Neumann computers," *Adv. Mater.*, vol. 24, no. 2, pp. 252–267, 2012, doi: 10.1002/adma.201102597.

[91] S. P. Park, Y. J. Tak, H. J. Kim, J. H. Lee, H. Yoo, and H. J. Kim, "Analysis of the Bipolar Resistive Switching Behavior of a Biocompatible Glucose Film for Resistive Random Access Memory," *Adv. Mater.*, vol. 30, no. 26, pp. 1–8, 2018, doi: 10.1002/adma.201800722.

[92] B. Sun *et al.*, "An organic nonvolatile resistive switching memory device fabricated with natural pectin from fruit peel," *Org. Electron.*, vol. 42, pp. 181–186, 2017, doi: 10.1016/j.orgel.2016.12.037.

[93] Z. Lv, Y. Zhou, S. T. Han, and V. A. L. Roy, "From biomaterial-based data storage to bio-inspired artificial synapse," *Mater. Today*, vol. 21, no. 5, pp. 537–552, 2018, doi: 10.1016/j.mattod.2017.12.001.

[94] K. Nagashima *et al.*, "Cellulose nanofiber paper as an ultra flexible nonvolatile memory," *Sci. Rep.*, vol. 4, pp. 1–7, 2014, doi: 10.1038/srep05532.

[95] W. Wu *et al.*, "Biodegradable skin-inspired nonvolatile resistive switching memory based on gold nanoparticles embedded alkali lignin," *Org. Electron.*, vol. 59, pp. 382–388, 2018, doi:

10.1016/j.orgel.2018.05.051.

[96] E. Ercan *et al.*, "A Redox-Based Resistive Switching Memory Device Consisting of Organic–Inorganic Hybrid Perovskite/Polymer Composite Thin Film," *Adv. Electron. Mater.*, vol. 3, no. 12, pp. 1–8, 2017, doi: 10.1002/aelm.201700344.

[97] J. Choi, J. S. Han, K. Hong, S. Y. Kim, and H. W. Jang, "Organic–Inorganic Hybrid Halide Perovskites for Memories, Transistors, and Artificial Synapses," *Adv. Mater.*, vol. 30, no. 42, pp. 1–21, 2018, doi: 10.1002/adma.201704002.

[98] K. Mohanta, J. Rivas, and R. K. Pai, "Reverse switching phenomena in hybrid organic-inorganic thin film composite material," *J. Phys. Chem. C*, vol. 117, no. 1, pp. 124–130, 2013, doi: 10.1021/jp309750p.

[99] D. H. Kwon *et al.*, "Atomic structure of conducting nanofilaments in TiO2 resistive switching memory," *Nat. Nanotechnol.*, vol. 5, no. 2, pp. 148–153, 2010, doi: 10.1038/nnano.2009.456.

[100] B. J. Choi *et al.*, "Resistive switching mechanism of TiO_2 thin films grown by atomic-layer deposition," *J. Appl. Phys.*, vol. 98, no. 3, 2005, doi: 10.1063/1.2001146.

[101] P. Zalar *et al.*, "DNA electron injection interlayers for polymer light-emitting diodes," *J. Am. Chem. Soc.*, vol. 133, no. 29, pp. 11010–11013, 2011, doi: 10.1021/ja201868d.

[102] C. Yumusak, T. B. Singh, N. S. Sariciftci, and J. G. Grote, "Bio-organic field effect transistors based on crosslinked deoxyribonucleic acid (DNA) gate dielectric," *Appl. Phys. Lett.*, vol. 95, no. 26, pp. 0–3, 2009, doi: 10.1063/1.3278592.

[103] S. Qin, R. Dong, X. Yan, and Q. Du, "A reproducible write-(read)n-erase and multilevel bio-memristor based on DNA molecule," *Org. Electron.*, vol. 22, pp. 147–153, 2015, doi: 10.1016/j.orgel.2015.03.045.

[104] B. Sun, L. Wei, H. Li, X. Jia, J. Wu, and P. Chen, "The DNA strand assisted conductive filament mechanism for improved resistive switching memory," *J. Mater. Chem. C*, vol. 3, no. 46, pp. 12149–12155, 2015, doi: 10.1039/c5tc02732b.

[105] A. A. Balandin *et al.*, "Superior thermal conductivity of single-layer graphene," *Nano Lett.*, vol. 8, no. 3, pp. 902–907, 2008, doi: 10.1021/nl0731872.

[106] D. C. Marcano *et al.*, "Improved synthesis of graphene oxide," *ACS Nano*, vol. 4, no. 8, pp. 4806–4814, 2010, doi: 10.1021/nn1006368.

[107] Q. Liu *et al.*, "Formation of multiple conductive filaments in the Cu/ ZrO2:Cu/Pt device," *Appl. Phys. Lett.*, vol. 95, no. 2, pp. 3–6, 2009, doi: 10.1063/1.3176977.

[108] J. Park, S. Lee, J. Lee, and K. Yong, "A light incident angle switchable ZnO nanorod memristor: Reversible switching behavior between two non-volatile memory devices," *Adv. Mater.*, vol. 25, no. 44, pp. 6423–6429, 2013, doi: 10.1002/adma.201303017.

[109] L. Liu *et al.*, "Multilevel resistive switching in Ag/SiO2/Pt resistive switching memory device," *Jpn. J. Appl. Phys.*, vol. 54, no. 2, pp. 3–6, 2015, doi: 10.7567/JJAP.54.021802.

[110] F. C. Chiu, T. M. Pan, T. K. Kundu, and C. H. Shih, "Thin film applications in advanced electron devices," *Adv. Mater. Sci. Eng.*, vol. 2014, pp. 2–4, 2014, doi: 10.1155/2014/927358.

[111] J. Szmytkowski, "The influence of the thickness, recombination and space charge on the loss of photocurrent in organic semiconductors: An analytical model," *J. Phys. D. Appl. Phys.*, vol. 40, no. 11, pp. 3352–3357, 2007, doi: 10.1088/0022-3727/40/11/015.

[112] D. S. Jeong *et al.*, "Emerging memories: Resistive switching mechanisms and current status," *Reports Prog. Phys.*, vol. 75, no. 7, 2012, doi: 10.1088/0034-4885/75/7/076502.

[113] A. V. Shaposhnikov, T. V. Perevalov, V. A. Gritsenko, C. H. Cheng, and A. Chin, "Mechanism of GeO 2 resistive switching based on the multi-phonon assisted tunneling between traps," *Appl. Phys. Lett.*, vol. 100, no. 24, 2012, doi: 10.1063/1.4729589.

[114] J. Kim, S. H. Lee, J. H. Lee, and K. H. Hong, "The role of intrinsic defects in methylammonium lead iodide perovskite," *J. Phys. Chem. Lett.*, vol. 5, no. 8, pp. 1312–1317, 2014, doi: 10.1021/jz500370k.

[115] M. A. Green, A. Ho-Baillie, and H. J. Snaith, "The emergence of perovskite solar cells," *Nat. Photonics*, vol. 8, no. 7, pp. 506–514, 2014, doi: 10.1038/nphoton.2014.134.

[116] H. Shi and M. H. Du, "Shallow halogen vacancies in halide optoelectronic materials," *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 90, no. 17, pp. 1–6, 2014, doi: 10.1103/PhysRevB.90.174103.

[117] F. C. Chiu, H. W. Chou, and J. Y. M. Lee, "Electrical conduction mechanisms of metal La2 O3 Si structure," *J. Appl. Phys.*, vol. 97, no. 10, 2005, doi: 10.1063/1.1896435.

[118] S. Wu *et al.*, "Bipolar resistance switching in transparent ITO/LaAlO3/ SrTiO3 memristors," *ACS Appl. Mater. Interfaces*, vol. 6, no. 11, pp. 8575–8579, 2014, doi: 10.1021/am501387w.

[119] H. W. Shin, J. H. Park, H. Y. Chung, K. H. Kim, H. D. Kim, and T. G. Kim, "Highly uniform resistive switching in SiN nanorod devices fabricated by nanosphere lithography," *Appl. Phys. Express*, vol. 7, no. 2, 2014, doi: 10.7567/APEX.7.024202.

[120] Y. Sharma, P. Misra, and R. S. Katiyar, "Unipolar resistive switching behavior of amorphous YCrO3 films for nonvolatile memory applications," *J. Appl. Phys.*, vol. 116, no. 8, pp. 1–6, 2014, doi: 10.1063/1.4893661.

[121] J. Zhang *et al.*, "Increasing the oxygen vacancy density on the TiO2 surface by La-doping for dye-sensitized solar cells," *J. Phys. Chem. C*, vol. 114, no. 43, pp. 18396–18400, 2010, doi: 10.1021/jp106648c.

[122] R. Schaub *et al.*, "Oxygen vacancies as active sites for water dissociation on rutile TiO2(110)," *Phys. Rev. Lett.*, vol. 87, no. 26, pp. 266104-1-266104–4, 2001, doi: 10.1103/PhysRevLett.87.266104.

[123] E. Carter, A. F. Carley, and D. M. Murphy, "Evidence for O2- radical stabilization at surface oxygen vacancies on polycrystalline TiO2," *J. Phys. Chem. C*, vol. 111, no. 28, pp. 10630–10638, 2007, doi: 10.1021/jp0729516.

[124] U. Celano *et al.*, "Three-dimensional observation of the conductive filament in nanoscaled resistive

memory devices," *Nano Lett.*, vol. 14, no. 5, pp. 2401–2406, 2014, doi: 10.1021/nl500049g.

[125] Z. Lv *et al.*, "Mimicking Neuroplasticity in a Hybrid Biopolymer Transistor by Dual Modes Modulation," *Adv. Funct. Mater.*, vol. 29, no. 31, pp. 1–11, 2019, doi: 10.1002/adfm.201902374.

[126] P. Y. Chen and S. Yu, "Compact Modeling of RRAM Devices and Its Applications in 1T1R and 1S1R Array Design," *IEEE Trans. Electron Devices*, vol. 62, no. 12, pp. 4022–4028, 2015, doi: 10.1109/TED.2015.2492421.

[127] Y. Wang *et al.*, "Photonic Synapses Based on Inorganic Perovskite Quantum Dots for Neuromorphic Computing," *Adv. Mater.*, vol. 30, no. 38, pp. 1–9, 2018, doi: 10.1002/adma.201802883.

[128] M. D. Pickett, G. Medeiros-Ribeiro, and R. S. Williams, "A scalable neuristor built with Mott memristors," *Nat. Mater.*, vol. 12, no. 2, pp. 114–117, 2013, doi: 10.1038/nmat3510.

[129] J. H. Tucker and M. A. Tapia, "Using Karnaugh maps to solve Boolean equations by successive elimination," *Conf. Proc. - IEEE SOUTHEASTCON*, vol. 2, no. 7, pp. 589–592, 1992, doi: 10.1109/secon.1992.202260.

[130] L. Ni, H. Huang, and H. Yu, "On-line machine learning accelerator on digital RRAM-crossbar," Proc. - IEEE Int. Symp. Circuits Syst., vol. 2016-July, no. 3, pp. 113–116, 2016, doi: 10.1109/ISCAS.2016.7527183.

[131] M. C. Lee, W. L. Chiang, and C. J. Lin, "Fast matrix-vector multiplications for large-scale logistic regression on shared-memory systems," Proc. - IEEE Int. Conf. Data Mining, ICDM, vol. 2016-Janua, pp. 835–840, 2016, doi: 10.1109/ICDM.2015.75.

[132] V. Sze, Y. H. Chen, J. Einer, A. Suleiman, and Z. Zhang, "Hardware for machine learning: Challenges and opportunities," Proc. Cust. Integr. Circuits Conf., vol. 2017-April, 2017, doi: 10.1109/CICC.2017.7993626.

[133] M. Hu et al., "Dot-product engine for neuromorphic computing," pp. 1–6, 2016, doi: 10.1145/2897937.2898010.

[134] H. Huang et al., "A 3D multi-layer CMOS-RRAM accelerator for neural network," 2016 IEEE International 3D Systems Integration Conference (3DIC), San Francisco, CA, 2016, pp. 1-5, doi: 10.1109/3DIC.2016.7970014.

[135] J. Gomez, I. Vourkas, A. Abusleme, G. C. Sirakoulis, and A. Rubio, "Voltage Divider for Self-Limited Analog State Programing of Memristors," IEEE Trans. Circuits Syst. II Express Briefs, vol. 67, no. 4, pp. 620–624, 2020, doi: 10.1109/TCSII.2019.2923716.

[136] L. Xia et al., "Technological Exploration of RRAM Crossbar Array for Matrix-Vector Multiplication," J. Comput. Sci. Technol., vol. 31, no. 1, pp. 3–19, 2016, doi: 10.1007/s11390-016-1608-8.

[137] M. Hu, H. Li, Y. Chen, Q. Wu, G. S. Rose, and R. W. Linderman, "Memristor crossbar-based neuromorphic computing system: A case study," IEEE Trans. Neural Networks Learn. Syst., vol. 25, no. 10, pp. 1864–1878, 2014, doi: 10.1109/TNNLS.2013.2296777.

[138] M. Zhao, B. Gao, Y. Xi, F. Xu, H. Wu, and H. Qian, "Endurance and Retention Degradation of

Intermediate Levels in Filamentary Analog RRAM," IEEE J. Electron Devices Soc., vol. 7, pp. 1239–1247, 2019, doi: 10.1109/JEDS.2019.2943017.

[139] Y. Liao et al., "A Compact Model of Analog RRAM with Device and Array Nonideal Effects for Neuromorphic Systems," IEEE Trans. Electron Devices, vol. 67, no. 4, pp. 1593–1599, 2020, doi: 10.1109/TED.2020.2975314.

[140] Y. Xiang et al., "Impacts of State Instability and Retention Failure of Filamentary Analog RRAM on the Performance of Deep Neural Network," IEEE Trans. Electron Devices, vol. 66, no. 11, pp. 4517–4522, 2019, doi: 10.1109/TED.2019.2931135.

[141] E. A. Cartier et al., "Reliability Challenges with Materials for Analog Computing," IEEE Int. Reliab. Phys. Symp. Proc., vol. 2019-March, pp. 1–10, 2019, doi: 10.1109/IRPS.2019.8720599.

[142] H. Wu et al., "Reliability Perspective on Neuromorphic Computing Based on Analog RRAM," IEEE Int. Reliab. Phys. Symp. Proc., vol. 2019-March, pp. 1–4, 2019, doi: 10.1109/IRPS.2019.8720609.

[143] Y. Liu, B. Gao, M. Zhao, H. Wu, and H. Qian, "The impact of endurance degradation in analog RRAM for in-situ training," Proc. Int. Symp. Phys. Fail. Anal. Integr. Circuits, IPFA, 2019, doi: 10.1109/IPFA47161.2019.8984759.

[144] W. Huangfu et al., "Computation-oriented fault-tolerance schemes for RRAM computing systems," Proc. Asia South Pacific Des. Autom. Conf. ASP-DAC, pp. 794–799, 2017, doi: 10.1109/ASPDAC.2017.7858421.

[145] A. Hayakawa et al., "Resolving endurance and program time trade-off of 40nm TaOx-based ReRAM by Co-optimizing verify cycles, reset voltage and ECC strength," 2017 IEEE 9th Int. Mem. Work. IMW 2017, vol. 4, pp. 2–5, 2017, doi: 10.1109/IMW.2017.7939101.

[146] Z. Song et al., "ITT-RNA: Imperfection Tolerable Training for RRAM-Crossbar based Deep Neural-network Accelerator," IEEE Trans. Comput. Des. Integr. Circuits Syst., vol. XXX, no. XXX, pp. 1–14, 2020, doi: 10.1109/TCAD.2020.2989373.

[147] E. Alpaydin and Fevzi. Alimoglu. (1998, July). Pen-Based Recognition of Handwritten Digits Data Set. . [Online]. Available: http://archive.ics.uci.edu/ml/datasets/Pen-Based+Recognition+of+Handwritten+Digits

[148] Z. Sun, G. Pedretti, E. Ambrosi, A. Bricalli, W. Wang, and D. Ielmini, "Solving matrix equations in one step with cross-point resistive arrays," Proc. Natl. Acad. Sci. U. S. A., vol. 116, no. 10, pp. 4123–4128, 2019, doi: 10.1073/pnas.1815682116.

[149] Z. Sun, G. Pedretti, and D. Ielmini, "Fast solution of linear systems with analog resistive switching memory (RRAM)," Proc. 4th IEEE Int. Conf. Rebooting Comput. ICRC 2019, no. 648635, pp. 1–5, 2019, doi: 10.1109/ICRC.2019.8914709.