Design of 28 GHz 4x4 RF Beamforming Array for 5G Radio Front-Ends

by

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Abstract

Current state of wireless infrastructure sees mass migration to higher frequencies as much of the already used spectrum is insufficient in supporting the influx of numerous users and various data intensive mobile applications. Data rates are projected to increase by an order of magnitude and harnessing the necessary bandwidth below 6 GHz is not feasible. A move to higher frequencies sees not only increased fractional bandwidth, but also significantly enhanced antenna apertures as a result of beamforming capabilities. Due to device level complications with frequencies nearing the unit gain frequency of transistor technology, high output power is seldom found, and in conjunction with severe path loss, communication links cannot be established without the usage of antenna arrays.

Phased array systems offer significant upside to the traditional array implementation as it permits reconfigurable directive communication. However, Ka-Band phased arrays still struggle to arrive at a reasonable tradeoff between design complexity, cost and performance. With a divide between both organic and printed circuit board (PCB) based approaches to the development of an antenna-in-package (AiP), this thesis sides with the latter. An antenna-on-PCB variant of the AiP is developed, which implements both commercially available RF laminates and RFIC front end modules to produce a 28 GHz 4x4 RF beamforming phased array that is found to exhibit extremely low loss (-0.66 dB), adequate scan volume ($\theta_o = +/-45^\circ$, in E and H planes) and large bandwidth (3 GHz) for a single layer, non-isolated patch antenna design. Unit cell, infinite array analysis is emphasized and lattice resizing is leveraged to obtain desired scan performance, while significantly reducing design complexity via the absence of intricate isolation enhancement techniques.

In an effort to aid in application based design, the AiP is extended to application of linearization where it is found that the inclusion of dummy elements along the perimeter of the package not only serve as element pattern enhancement, but also provide reliable means of output signal capture. Negating the traditional transmitter observation receiver (TOR) architecture, the AiP design as a TOR for millimeter-wave communication proves optimistic in the quest for maximum system efficiency.

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Dedication

This is dedicated to my Nonno, Renzo Baggio, for inspiring me as a child, always pushing me to my limits, regardless of age, and instilling in me the need to do more.

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Chapter 1

Introduction

Current wireless infrastructure and user equipment are mainly operating below 6 GHz. Going forward, to meet the demands for ultra-broadband mobile access and the requirements enforced by the internet of everything, wireless networks will have to extend to the untapped millimeter-wave (mmWave) frequency bands [12]. Yet, this will impose significant challenges to development of the underlying infrastructure given the very high path loss at mmWave. First, wireless communication will need to migrate from a broadcasting based transmission to a directive one. Second, the wireless networks will need to be ultra-dense with very small cells and consequently interferences will need to be well handled. To tackle these challenges, large scale multiple antenna technology and the associated beamforming and multi-user massive Multiple Input Multiple Output (MIMO) features will be paramount [12]. In fact, the successful deployment of the future wireless infrastructure, commonly called 5G, is predicated to the development of high performance mmWave large scale multi-antenna systems.

1.1 Motivation

Over the years, wireless infrastructure has evolved and society has seen first through fourth generation networks. Within the past five years, many services previously bound by wire transmission have made way to being available over wireless and as of 2014, global mobile traffic saw an increase of roughly 70%. Smartphones contributed to a significant portion of this growth, responsible for near 88% of the total traffic [13, 14]. Services like video streaming, with the desire for ultra high definition and reduced latency, constitute up to a 51 percent of this mobile traffic volume [15]. Technology giants like Cisco Systems

projected in 2016, a network involving greater than 50% of its devices being smart devices by 2019. Recent publications by Cisco suggest this to be true at 44% for smartphones alone [16]. Factoring in that the average user is expected to download near 1 terabyte of data annually by 2020 [13], the existing wireless network infrastructure is in question.

Companies are exercising their imagination and developing new use cases for wireless, with applications in augmented reality, online gaming, video conferencing, financial technologies and electronic health care. Furthering this, developments in internet of vehicles (IoV), in addition to internet of things (IoT), device to device (D2D) and machine to machine (M2M) communications, yield extreme stress for the network. With 4G LTE technology, the theoretical limitations on the downlink speed place data rates near 150 Mbps, supporting a maximum of 600 users per cell. Knowing that IoT and M2M look to push cell capacity to tens of thousands of users per individual cell, solutions are under development to tackle mass congestion [13, 17, 18].

Capacity, or the maximum data rate that can be achieved by a communication channel, depends highly on available bandwidth, spectral efficiency and in fact, cell size [13, 19]. In an effort to alleviate the problems foreseen with existing technologies, portions of the frequency spectrum above the traditional "sweet spot" or "beachfront", 0 - 3 GHz, has been opened for commercial use. Given that a minute fraction of the frequency spectrum at mmWave (30 - 300 GHz) results in predominantly large available bandwidths, the data rate possibilities extend by a massive one to two orders of magnitude from the current standing [13, 20].

1.1.1 Broadcasting versus Line of Sight

Extending network concepts to mmWave creates both advantages and disadvantages for the development of commercial technologies. Considering that an increase, as mentioned previous, in the number of connected devices is expected, cells can become over cluttered increasing user interference and effectively limiting the potential for efficient usage of the allotted spectrum. Combine the former with poor signal propagation characteristics in the mmWave band [12, 13], which immediately promote smaller cell sizes and shorter communication link distances, and the problem can be perceived as unsolvable.

In Electromagnetic Theory, there exists a relationship of inverse proportionality between the physical size of electronic structures and the representative wavelength corresponding to its operating frequency. Simply put, as operating frequency increases, electronics get smaller. Exploiting this fundamental concept allows one to overcome immediate challenges moving to mmWave, taking advantage of antenna design concepts previously

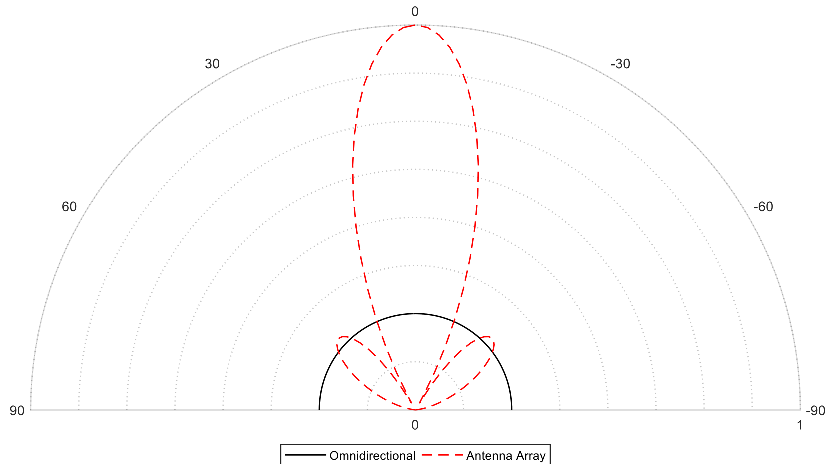


Figure 1.1: Radiation patterns of an omnidirectional and antenna array

deemed impractical, and ultimately driving the decision to migrate from broadcasting to line of sight communication.

Broadcasting, implemented in previous generation networks, utilizes omnidirectional antennas which transmit signal in all directions. To ensure the communication link can always be closed between the base station and the user in question, the power transmitted must be large enough such that the receiver can distinguish usable signal from noise. Transitioning to mmWave and broadcasting the same output power, the communication link would not work. Atmospheric absorption, rain and material penetration, all together account for much of the signal power reduction, significantly limiting the users ability to recover the information sent. Compensating for this, transmit power can be increased, but this not only decreases the efficiency of the link, but also presents extreme challenges in simply generating such high power at these frequencies. Therefore, broadcasting at mmWave is not very practical.

Line of sight communication employs the concept of antenna arrays, which utilizes multiple antennas in a given grid arrangement, at the expense of physical electronic structure size, to yield the ability to focus transmitted power in a specific direction. Focused energy introduces the potential for significant improvements; it can reduce the necessary transmitted power for a given link distance, or can evidently extend coverage range for the same output power. Further, knowing the aforementioned inverse relationship between size and frequency, mmWave operation can overcome large antenna array footprints, having arrays exhibit similar size to that of single sub 6 GHz omnidirectional antennas. In addition, focused energy introduces spatial diversity. Off axis communication experiences little to no

transmitted power, enabling users in densely populated areas to simultaneously occupy the same communication channel while not interfering with one another, effectively improving spectral efficiency by frequency reuse. Encompassed within all mentioned, is that of the communication link reconfigurability. By manipulation of the signal phase injected into each antenna within the array, power can be refocused in different directions, leaving no user at a disadvantage. This is the fundamental principle behind phased arrays.

1.1.2 Operating Frequency & Integration Complexity

In transitioning to the mmWave bands, practical limitations restrict the potential upside phased arrays have to offer. For instance, considering traditional base station architecture, the antenna is isolated from the RF front end, via an isolator, permitting more appropriate conditions for the amplifying hardware. Scaling in frequency brings reduced component size and inhibits the usage of such dependable components. Further, parasitic effects from component packaging and placement pads weigh in considerably on simulation complexity, introducing new boundaries in the design stage.

In terms of system packaging, component integration presents significant challenges for the mmWave designer. Involved in the operation of phased array transceivers are RF front end modules (RFFEMs), low frequency and microwave signal distribution networks, power distribution and heat management devices. With module package sizes on the order of millimeters and interconnects involving wire bonds and flip chip based ball grid arrays, system packages need to be critically assessed to ensure optimal overall system performance. This deviates from the conventional design philosophy, which emphasizes the performance of individual components and lacks view of top level function.

1.1.3 Commercial Availability & Scalability

Phased arrays for mmWave are scarce in the current commercial landscape. Due to specification requirements of developing 5G systems, optimal antenna design requires exotic material selection, directly impacting cost and limiting the potential for small parties to develop phased array systems. Given the importance of mutual coupling and the negative effect beam scanning can have on the circuit level components driving the array, much of the design time is spent achieving a trade-off between usable bandwidth and scan range. Encompassed within all this is the manufacturability of the overall package. Designs are constrained within precision of the fabrication house in addition to that of the thermo-mechanical overhead imposed by the active circuitry [21].

Additionally, something that is not trivial is the scalability of the system. Much of the desirable attributes associated with phased arrays come from the array factor; enhanced gain, narrow beam width and beam reconfigurability, all stem from the inclusion of many antenna elements. Unfortunately, due to the nature of mutual coupling, system performance at one array size does not accurately predict the performance at another, if not handled. Edge elements exhibit vastly different characteristics and as a result, the designer must utilize a methodology that captures a balance between design time, performance and feasibility.

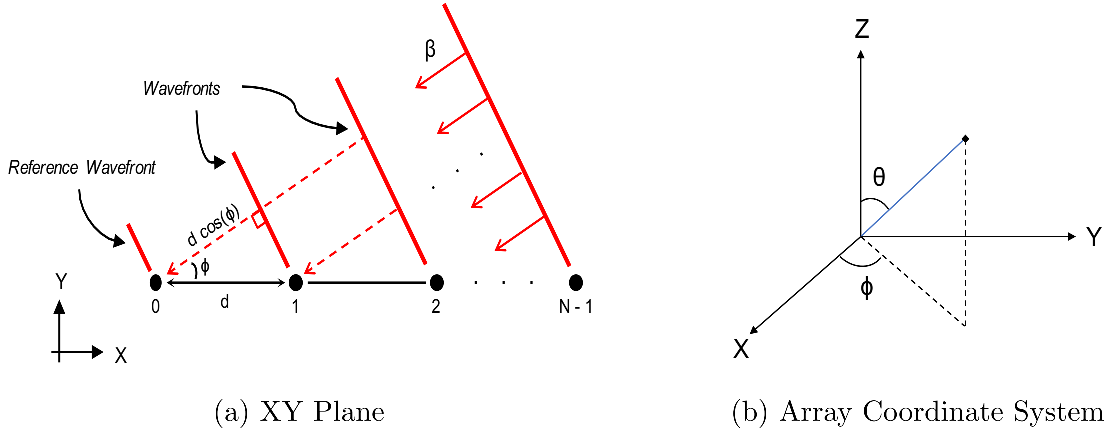
Chapter 2

Background and Literature Review

In recent years, the development of mmWave 5G transceivers has drawn a lot of attention from academia and industry, and significant improvement efforts have been made in semiconductor device technologies, mmWave circuits and transmitter and receiver architectures. Given the importance of directing transmitted signals in a specific direction and the ability to electronically steer according to a users position, much of the development extends itself to innovative architectural implementations and system optimization. At the forefront of the directional transceiver is the antenna array, an integral component that if handled improperly, can act as a bottleneck to the system. Much of the capabilities attainable by antenna arrays originate from thorough understanding of theoretical concepts and knowledge of circuit realizability. Possessing such enables the designer to place emphasis on integration of the antenna array with driving circuitry and peripheral components, increasing the potential for optimal system functionality.

2.1 Arrays: Linear & Planar

The antenna array model consists of two parts; the antenna element pattern and the array pattern, where all elements are replaced with isotropic point sources of equivalent amplitude and phase [22]. Due to the pattern multiplication principle, this model can be reinterpreted as a system consisting of a single antenna, referenced to a specific point in space, where its radiated fields are amplified by some multiple, deemed the array factor (AF) [10]. Because the total fields radiated by the array depend significantly on the array factor, an examination of the array factor formulation is paramount in the initial design of a phased array.



(a) XY Plane

(b) Array Coordinate System

Figure 2.1: An N isotropic element linear array operating in RX mode

2.1.1 Array Factor

Given an ideal phased array composed of N isotropic radiating elements, a relationship can be drawn between the angle of arrival (departure) of the incoming (outgoing) plane wave and the respective signal delay each antenna exhibits (introduces) within the array. The array factor devises the relationship between these two quantities and results in an antenna independent model parameter. Figure 2.1 illustrates a one dimensional N element linear array spaced distance d apart in the XY plane, where the spatial delay relationship of the nth element, $n\gamma$, with reference to the edge element ($n = 0$), is the product of the wave vector magnitude, β, and the perpendicular distance between wave fronts, $d\,cos(\phi)\,sin(\theta)$.

$$\gamma(\phi, \theta) = \beta d\,cos(\phi)\,sin(\theta) \tag{2.1}$$

Knowing a plane wave yields equal amplitude across a given wavefront, labelled here as unity for simplicity, and isotropic sources are spatially independent, each antenna generates signals of equal amplitude with phase delay corresponding to spatial delay, γ. The array factor therefore, can be written as the summation of these signals, weighted individually by each respective RF chain in amplitude, A_n, and linear phase, α,

$$AF(\phi, \theta, \alpha) = I_0(\alpha) + I_1(\alpha)\,e^{j\gamma(\phi,\theta)} + \cdots + I_{N-1}(\alpha)\,e^{j(N-1)\gamma(\phi,\theta)} = \sum_{n=0}^{N-1} I_n(\alpha)\,e^{jn\gamma(\phi,\theta)} \tag{2.2}$$

where $I_n(\alpha) = A_n\,e^{jn\alpha}$ and is the weighting factor of the nth RF path.

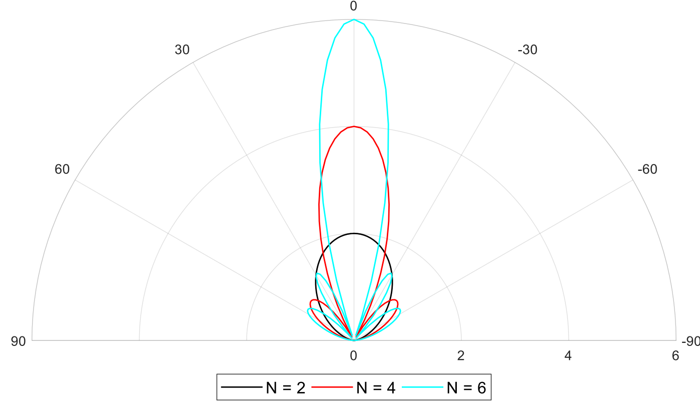


Figure 2.2: Array factor for a uniformly excited N element linear array, $(\phi_o = 0)$

Assuming uniform excitation (UE) such that $A_0 = A_1 = A_2 = \cdots = A$ and defining $\psi = \alpha + \gamma(\phi, \theta)$, the array factor can be rewritten in an easy to interpret form that illustrates the significance of the array principle.

$$AF(\psi) = A \sum_{n=0}^{N-1} e^{jn\psi} \tag{2.3}$$

By simple examination, one can notice the function evaluates to a maximum of AN for $\psi = 0$. This dictates that the array factor maximum scales linearly with the number of elements, N, seen in Figure 2.2. Additionally, a closer examination of the factor ψ suggests that this maxima can be obtained for different angles of arrival, or departure, implying the phased array can refocus its maximum radiation direction by adjusting the phase weighting parameter, α.

$$\begin{aligned} \alpha &= -\gamma(\phi_0, \theta_0) \\ &= -\beta d\, cos(\phi_0)\, sin(\theta_0) \end{aligned} \tag{2.4}$$

$$\big(\phi_0, \theta_0\big) = \text{ main beam pointing direction}$$

Forcing $\psi = 0$, the linear phase relationship given by equation (2.4) is obtained. Utilizing this and compensating for the spatial delay in the RF chain is one of the phased arrays most substantial functions, yielding an extremely versatile device that can maximally combine

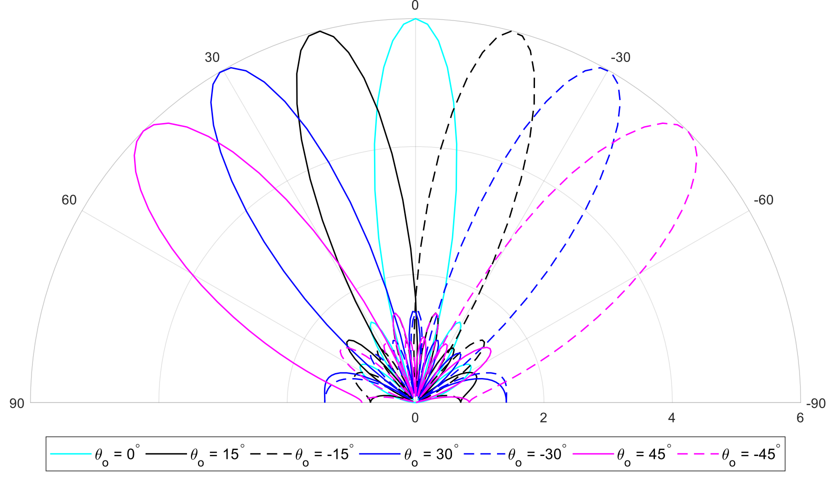


Figure 2.3: AF(ϕ, θ) for various scan angles of a six element UE linear array, $(\phi_o = 0)$

at any angle of arrival (ϕ_0, θ_0). This is illustrated in Figure 2.3. Given antennas usually conform to the principle of reciprocity, this is also true when the array is transmitting.

Previously mentioned, one of the advantages to antenna arrays was the ability to focus energy such that users could enforce frequency reuse in a given high density cell. Practically, this can be achieved by extremely precise radiation patterns. When the array factor is rewritten in the normalized form of $|f(\psi)|$, the significance of the number of elements is further enforced.

$$|\,f(\psi)\,| = \left| \frac{sin\left(\frac{N\psi}{2}\right)}{N\,sin\left(\frac{\psi}{2}\right)} \right| \tag{2.5}$$

$$\psi = \frac{2m\pi}{N} \quad \text{for existence of a null} \tag{2.6}$$

By simple examination of the first array factor null, $|f(\psi)| = 0$, $m = 1$, due to the inverse proportionality in relation (2.6), an increase in the number of elements enforces the first null at a reduced value of ψ. This implies a reduction in the main beam width for an increase in the number of elements, as illustrated in Figure 2.4. Moreover, it can easily be seen that for an increased N the side lobe peaks decrease. This further aids in the concept of frequency reuse in dense coverage areas.

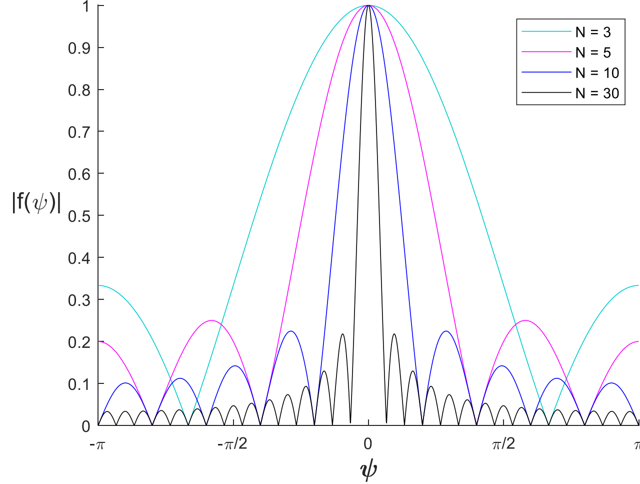


Figure 2.4: Normalized array factor for an N element UE linear array

Exploiting the concepts discussed with respect to linear arrays presents limitations in practice. Versatility is at a minimum when scan functionality is of priority. Linear arrays are subject to severe scan restrictions where beam steering is confined to a single plane. In the ever evolving landscape, many applications call for the ability to scan in both principal planes, ($\phi = 0°, 90°$), alleviating many of the potential mechanical dependencies in design. Additionally, employing linear arrays that look to harness the advantages of antenna array gain via many antenna elements is considerably problematic. Given the array scales in one dimension, it is most suitable to achieve such characteristics in a smaller form factor. Utilizing a multidimensional array permits the user to attain such functionality in a smaller form factor, albeit without the introduction of new considerable affects.

For planar phased arrays where the z-axis is normal to the plane of the array, the array factor can be written as the product of two linear array factors, assuming the current distribution in all rows is similar, where the same is true for all columns [22, 10]. Under uniform excitation, it can be described using equation (2.7), where α_x, α_y are independent variables.

$$AF(\psi_x, \psi_y) = A^2 \sum_{n=0}^{N-1} e^{jn\psi_x} \sum_{m=0}^{M-1} e^{jm\psi_y} \tag{2.7}$$

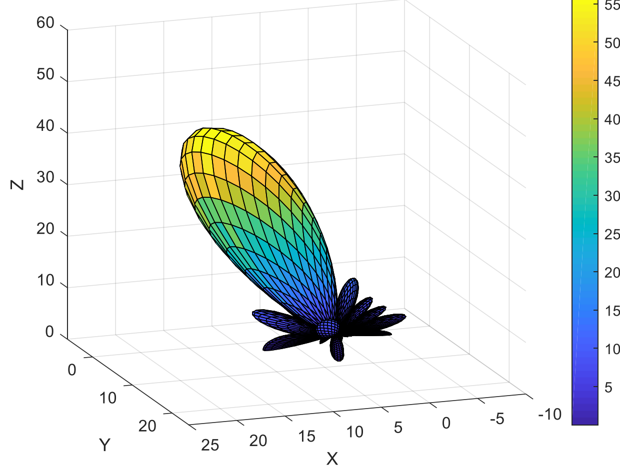


Figure 2.5: AF(ϕ, θ) of an 8 x 8 UE planar array, main beam direction $(\phi_o = 45°, \theta_o = 30°)$

where,

$$\psi_x = \beta d_x \, cos(\phi) \, sin(\theta) + \alpha_x$$

$$\psi_y = \beta d_y \, sin(\phi) \, sin(\theta) + \alpha_y$$

To produce a single main beam directed toward angle (ϕ_o, θ_o), relations (2.8) and (2.9) should be used, resulting in an array factor resembling that of Figure 2.5.

$$\alpha_x = -\beta d_x \, cos(\phi_o) \, sin(\theta_o) \tag{2.8}$$

$$\alpha_y = -\beta d_y \, sin(\phi_o) \, sin(\theta_o) \tag{2.9}$$

2.1.2 Mutual Coupling Effects

In section 1.1.2, the array factor was presented where by pattern multiplication, the total field could be computed through multiplication with the pattern of a single antenna element. This assumes that each antenna acts independently within the array and element currents are not affected by surrounding array radiators. This in practice is not the case. Termed mutual coupling, antennas in close proximity exhibit characteristics that are a

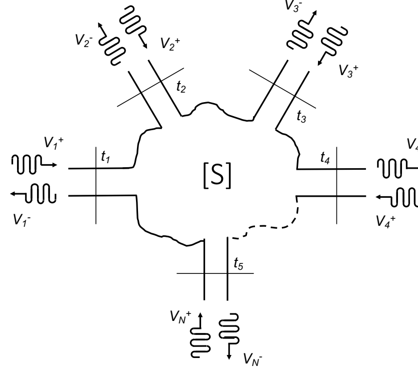


Figure 2.6: An arbitrary N-Port microwave network [3]

function of one another, where current in one element can be affected by direct radiation from another element, secondary reflections from surrounding media, or signal feed line leakage. General trends for mutual coupling consist of the following; with distance d, mutual coupling decreases by rate of $1/d^2$, element pattern characteristics are proportional to the level of coupling with narrow patterns yielding lower coupling than broad, element polarization perpendicular to element alignment yields increased coupling and most importantly, larger elements are known to exhibit less coupling [22].

The coupling phenomena manifests itself in alterations to the element pattern, changing the radiation characteristics of the array. From a microwave engineering perspective, this behaviour is characterized through off diagonal terms in the network scattering parameters, S_{ij}. Network scattering parameters relate voltage waves, both incident, V^+, and reflected, V^-, at each of the N ports within the microwave network (Figure 2.6), through the following relationship,

$$\begin{bmatrix} V_1^- \\ V_2^- \\ \vdots \\ V_N^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \cdots & S_{1N} \\ S_{21} & & & \vdots \\ \vdots & & & \vdots \\ S_{N1} & \cdots & \cdots & S_{NN} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ \vdots \\ V_N^+ \end{bmatrix} \quad \text{or} \quad \left[V^-\right] = \left[S\right]\left[V^+\right] \tag{2.10}$$

where an entry in the scattering matrix is defined as,

$$S_{ij} = \left.\frac{V_i^-}{V_j^+}\right|_{V_k^+=0 \ for \ k \neq j}. \tag{2.11}$$

Seen from the perspective of one element, any reflected signal is a linear combination of the incident waves at all other ports, weighted by the off diagonal parameters. The result, an active reflection coefficient (ARC), Γ_i, given by (2.12), which governs the ith antennas bandwidth. Due to its phasor dependence, the reflection coefficient retains the ability to change in both magnitude and phase with array scanning, presenting itself as a potential variable load to driving circuitry. Because of this, the active reflection coefficient extends itself as a key array performance metric and must be minimized for all elements, at a wide range of scan angles.

$$\Gamma_i = \frac{V_i^-}{V_i^+} = \sum_{j=1}^{N} \frac{S_{ij} \, V_j^+}{V_i^+} \tag{2.12}$$

2.2 Beamforming Architectures

Incorporating the antenna array into a system that yields both versatility and peak performance is a daunting task. At the forefront of the phased array system is the beamforming architecture, a block level implementation scheme that can severely enhance or hinder system capability dependant on the underlying use case. Many of the applications looking to exploit the massive MIMO concept at mmWave for improved spectral efficiency and path loss compensation present the designer with significant system level tradeoffs between total capacity, user flexibility, design complexity and power consumption. Three architectures are commonly implemented; digital, analog and hybrid.

2.2.1 Digital Beamforming

Digital beamforming (D-BF), the most resourceful of the three beamforming architectures, is widely implemented in classical low frequency systems, enabling the potential for MIMO functionality [23]. Each antenna is met with its own RF chain ($N_A = N_{RF}$), consisting of mixed signal (analog to digital (ADC) & digital to analog (DAC) converters), frequency translating and RF front end circuitry. Total number of users equals the total number of antennas, permitting the system to operate at highest spectral efficiency via digital precoding, and in a case where spatial multiplexing is not desired, the array can be reconfigured to serve a single user exploiting the array factor to enhance transceiver gain. Due to the large number RF chains however, power consumption exceeds all other beamforming architectures for same data converter resolution, with the move to mmWave exhibiting a

near linear relation between power and system bandwidth [23]. Further, increased system complexity introduces denser circuitry, new signal processing overhead and resulting latency [24]. Because of this, digital beamforming, without the help of lower resolution data converters and reduced system bandwidth [23], is said to be not feasible for mmWave massive MIMO operation [23, 24, 4].

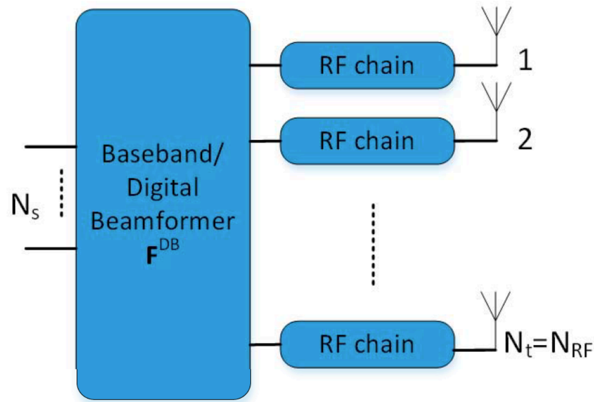


Figure 2.7: Digital beamforming [4]

2.2.2 Analog (RF) Beamforming

Analog RF beamforming (RF-BF) combats power consumption at the expense of multi-user support. Largely adopted, RF beamforming depends on line of sight links, where it assigns the necessary magnitude and phase weighting for each antenna in the analog domain via variable attenuators and phase shifters. This results in lack of precoding flexibility and in turn places larger strain on the RF front end, limited by gain behaviour and bit resolution of the phase shifter [24]. The entire antenna array is driven with one RF chain ($N_{RF} = 1, N_{RF} \neq N_A$), reducing system complexity, routing density and signal processing overhead, in addition to introducing considerable power savings. As a result, array size has less impact on power budget, where consumption depends solely on RF FEM efficiency, allowing for significantly larger array size, increased signal-to-noise ratio (SNR) and reduced susceptibility to co-channel interference [24].

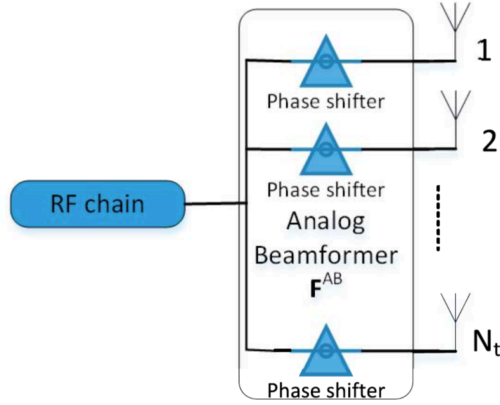


Figure 2.8: Analog beamforming [4]

2.2.3 Hybrid Beamforming

Hybrid beamforming (H-BF) looks to combine the benefits of both fundamental architectures; increased spectral efficiency and minimal power consumption. By limiting the number of data streams, using digital precoding for multistream transmission combined with analog beamforming for antenna gain, hybrid beamforming yields massive MIMO functionality with reduced complexity and power overhead. The architecture has two basic forms; sub-array and full array. The sub-array setup consists of multiple analog beamforming sub-arrays ($N_{RF} \neq N_A$), where each sub-array can radiate its own independent beam. For non-line of sight channels, additional precoding can be performed digitally to utilize the entire array for the set of users. Enhancing usable gain at the expense of additional RF paths, the full array setup yields the same number of RF chains, however each chain now connects to all antennas [24, 4]. Determining the optimal number of RF chains, antenna elements and architectural arrangement depends on proper channel estimation and usability case, presenting a unique optimization problem to the designer.

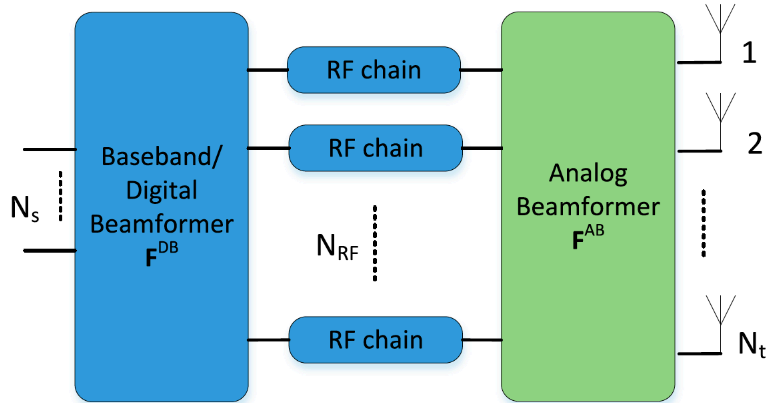


Figure 2.9: Hybrid beamforming [4]

2.3 Review of mmWave RF-BF Phased Arrays

A comparison of the known beamforming architectures leads to the obvious conclusion that hybrid beamforming is the solution to mmWave phased array implementation. However, considering the integration complexity previously mentioned, efficiency of circuit level components at mmWave and availability of commercial front end modules that can yield even the most basic analog beamforming functionality, one can quickly conclude that RF beamforming is the necessary first step in the development of 5G phased array systems. RF beamforming has the core capabilities to showcase the potential of initial 5G network implementations and presents the necessary architectural simplicity to develop an appropriate methodology for phased array scaling. Due to this, section 2.3 focuses its review on mmWave RF beamforming phased array systems, with later sections outlining the design and implementation contributions.

Near the beginning of the 21st century, Parker and Zimmerman outlined state of the art phased array implementations and suggested future trends based off the foreseen benefits such systems could bring to radar and communication applications [25]. As of 2002, phased array implementation was passive, predominantly used for radar, where hardware design catered to the type of radar; ground, surface based, airborne or space based. Due to the lack of maturity and high cost associated with active devices, arrays were conveniently designed using corporate or series fed networks where loss minimization was of most importance. With the introduction of gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) technology and automated module assembly techniques, cost associated with

active array development experienced an order of magnitude decrease. This meant that active arrays were sufficient for a subset of radar applications, but further cost and weight reductions were necessary to extend to space based radar [25].

Implementing an array involved architectural considerations, appropriate radiator selection and isolation investigations to determine the optimal active array formulation. At the time, many high tech array systems were based off the “brick architecture”, where linear multi-module sub-arrays were stacked on top one another to yield one large array. Transmit and receive modules were kept separate, to achieve maximum isolation while lowering manufacturing cost and improving system yield. Front end circuitry and radiating elements were housed in separate modules than that of the beam steering control unit. Radiator selection criteria was based on achievable impedance bandwidth, scan angle, cost and installation environment, and applications requiring low profile designs used patch antennas. Parker and Zimmermann depicted a prime example of this; the L-Band array developed by NASA. This array utilized a multilayer planar structure, integrating both signal and power distribution networks in the system package, mounting MMIC’s via flip-chip interconnect, foreshadowing the future of array implementation [25].

Beamforming architecture was under question, as analog beamformers were said to be complex and expensive and digital implementations were focused on available data converter technology, concerned that signal processing cores could not handle the potential system throughput. Nonetheless, Parker and Zimmerman claimed that the ultimate goal in 2002 was an active implementation that utilized a fully digital beamformer, projecting the eventual replacement of many analog implementations [25]. Bosch Satcom, Marconi Communications and the European Space Agency took an alternative approach, where Butz et al. investigated the potential for a hybrid, multi beam modular array implementation for Ka-Band satellite communication. The designed array utilized an analog beamformer MMIC control module and a solid state GaAs MMIC power amplifier (PA), housed on a low temperature co-fired ceramic (LTCC) substrate, and a radiating module consisting of 24 radiating patches. Adopting a sub-array architecture enabled testing feasibility, considering operating the entire array of 520 patches produced an astonishing 60 dBm effective isotropic radiated power (EIRP), with an even more astounding power consumption of 430 watts. This was the first reported multi-beam Ka-Band phased array, built from highly integrated modules, where 500 MHz impedance bandwidth and a scan range of 41.5 degrees off bore sight was attainable [26]. Butz et al. array implementation was state of the art and outlined one of the key problems future integrated array implementations would face; mass heat dissipation from amplifier circuits in a compact volume.

With continued development in process technologies, the scope of phased array integration soon extended its reach beyond GaAs to silicon (Si) based beamforming front ends.

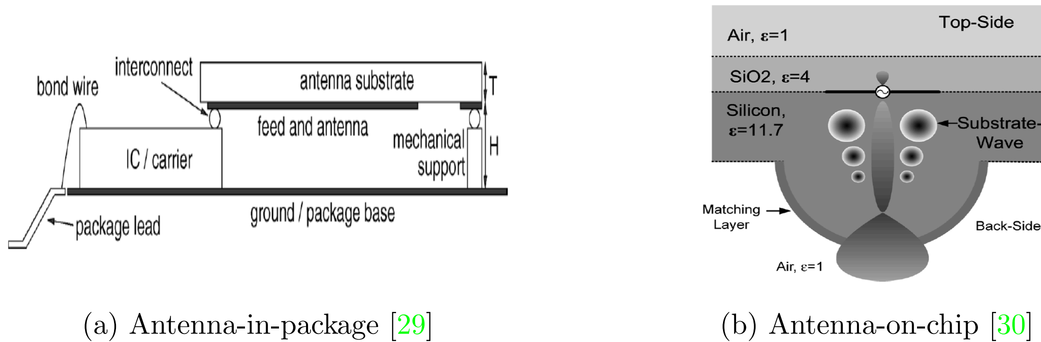
Transistor cut-off frequencies approached 100 GHz, making silicon a prime candidate for mmWave systems. Nonetheless, key weak points in the silicon process, being low breakdown voltage, integrated passive losses, low power budget, cost and area constraints, made architectural decisions challenging [27]. Supporting such a transition however, was the known impact array systems had on communication links. An increase in signal to noise ratio (SNR) from antenna beamforming allowed the system to achieve data rates similar to single path systems, while operating on less total power, making silicon even more of a possibility.

In 2004, Hashemi et al. introduced an 8-Path fully integrated 24 GHz phased array receiver in silicon and outlined key circuit level and architectural trade offs in building silicon based integrated array systems [27, 28]. Hajimiri et al. summarized the advantages and disadvantages in different beamforming architectures, taking into consideration power consumption and array functionality. Within the context of band limited signals, true time delay was emphasized for proper array operation, as approximating a time delay with a phase shift introduced increasing distortion in the constellation for larger bandwidth to carrier ratio. Phase shifting at RF was not implemented due to large phase shifter loss at 24 GHz, and given the need for amplitude and phase decoupling in the beamformer, the phase shift was implemented in the local oscillator (LO) path. The outcome of this work, an 8 element analog beamforming phased array with gain of 61 dB, supported the transition to silicon based phased arrays.

In 2006, low cost packaging solutions for commercial use began to be investigated for the untapped mmWave V-Band (40 - 75 GHz) frequencies, in addition to W-Band (75 - 110 GHz). To develop packaging that was compatible with mmWave integrated circuits allowing for large impedance bandwidth and high system efficiency, researchers Thomas Zwick, Duixian Liu and Brian P. Gaucher proposed the usage of antennas integrated into the package, a possibility given the small wavelengths at 60 GHz. Zwick et al. developed a planar radiating structure printed on low cost substrate using printed circuit board technology (PCB) (Figure 2.10a). Interconnect loss to transceiver front end was minimized via solder ball mount (flip-chip interconnect), resulting in efficiency's of better than 80% [29].

In contrast to antenna in package, Babakhani et al. proposed the integration of radiating structures directly on the silicon chip at 77 GHz, a concept that could potentially improve system reliability and repeatably by ridding the complex arrangement of costly interconnects. Due to the challenges faced with power generation at mmWave, such an implementation was advantageous, however due to silicon exhibiting high dielectric constant and low substrate resistivity, antenna implementation was not quite trivial. Babakhani et al. showed that a simple top side radiating structure is not sufficient due to much of

the radiated power being absorbed into the silicon substrate. In addition, efforts at implementing a ground shield to redirect radiation resulted in reactive effects for low antenna to ground distance, and high power surface waves for large distances. Such a scenario attributed to increased heat dissipation, or edge radiation from surface wave exit. The solution proposed utilized a hemispherical silicon lens, with matching layer, which converted the trapped surface wave energy to radiation (Figure 2.10b). An increase in gain of 10dB was realized, with total antenna gain being 2dBi, a value still quite low [30].



(a) Antenna-in-package [29] (b) Antenna-on-chip [30]

Figure 2.10: Initial proposed integration schemes

As a result of such efforts, Duixian Liu and Brian Gaucher of T. J. Watson Research Center, IBM, outlined design considerations for mmWave antennas within a chip package in their 2007 IEEE conference proceeding. In their article, Liu and Gaucher identified key factors involved in packaged mmWave antenna design that is not traditionally of concern for sub 10 GHz. Characteristics like high bandwidth, efficiency and small form factor all originate from the underlying material selection, feed line connection architecture, manufacturing precision and potential surrounding electromagnetic interference (EMI) [31].

Material selection inherits two separate categories; antenna substrate and packaging material. Antenna substrates tend to have low dielectric constant and exhibit an ideal zero loss. However, at mmWave, many material specifications are measured at very low frequencies with many RF materials around 10 GHz. This introduces significant issues in the accuracy of the model representing the antenna structure. In addition, packaging materials are quite lossy, which can ultimately degrade system efficiency, and should be accounted for in the antenna design stage [31].

Feed line connections present multiple issues that can inherently impact signal quality and reduce assembly flexibility. At mmWave, wire-bonds tend to introduce inductive effects, degrading antenna impedance characteristics. Flip-chip mounting is generally preferred, however to enable such a low loss interconnect, the connecting transmission line

must yield the appropriate metal arrangement (ground-signal-ground) to be compatible with that of the flip-chip. Additional limitations on feed lines stem from the manufacturing precision as not all characteristic impedance's are achievable under a limited line width. This has the potential to lead to significant mismatch issues introducing the need for complex, lossy matching networks [31].

The ultimate challenge Liu and Gaucher stated for printed planar antennas was bandwidth gain product maximization given all the constraints. Of most importance was mentioned the suppression of surface waves, something that is usually strong in planar antennas and significantly deteriorates efficiency, while increasing the antennas dependence on the surrounding environment. Further, with the inclusion of active circuitry, surface waves can introduce new means on EMI. However, as a means to inhibit surface wave excitation, Liu and Gaucher identified a robust mechanism that involved the usage of metal rings surrounding the antenna structure, a common technique employed in designs of today [31].

2.3.1 Initial Developments at V-Band (40 - 75 GHz)

Given the necessary requirement of 24 - 64 antennas for 60 GHz phased array systems to overcome high path loss and PA technology limitations, enabling high speed applications, much attention at first was given to the reduction of chip size. In 2009, as an attempt to rid the system of independent transmit and receive circuitry, Cohen et al. introduced the first bi-directional Tx/Rx four element phased array chipset for 60 GHz applications. This chipset took advantage of common elements like the phase shifter, combining network and frequency translating circuitry to enable a compact form factor comparable to that of a single Tx or Rx chip. Reported with the lowest power consumption and size at the time, and compatible with the time division duplex (TDD) communication standard, this enabled the possibility of significantly reduced antenna package size which would translate to board level scalability [32, 33].

Integrating active circuitry and antenna arrays via a low cost, high performing package was not a trivial task. In 2008 Antti E. I. Lamminen, Jussi Sily, and Antti R. Vimpari began investigating low-temperature cofired ceramic (LTCC) substrates for passive antenna array packaging [34], due to its superior electrical properties; low-loss dielectrics and conductors, good thermal conductivity, high degree of integration capability, low water absorption and good mechanical properties. Extending this to active arrays, Hong et al. developed a 24 element array integrated in an LTCC based package, driven by a single beamforming IC via flip-chip interconnect. Deemed Antenna-in-Package (AiP), the array design focused on differences that can arise between development for proto-type and mass market [5].

Hong et al. outlined that prototype development introduced nonstandard and non-guaranteed techniques that cannot allow realization of a truly low cost and high reliability package. Their attempt at developing an antenna in package for mass market, therefore lead to an eleven layer stackup consisting of 100μm thick layers, with permittivity 5.8 and loss tangent 0.004 (Figure 2.11). Utilizing a circular stacked patch radiator with buried ground vias, suppressing surface waves and emulating a cavity, along with ground shielding to create a quasicoaxial feed, the 4x6 layout was capable of 9 GHz BW and 14.5 dBi gain. Full wave analysis allowed for accurate model representation, however due to incorporating a single densely populated beamformer chip, feed lines were uniquely designed and optimized to ensure matched phase response. This tedious task amounted to 0.7 dB amplitude and 8 degree phase deviation across lines, introducing potential impairments in the system. Gain oscillation were found to be present in measurement and later attributed to fabrication process deviations, as well as radiation from edge diffraction and surface waves [5].

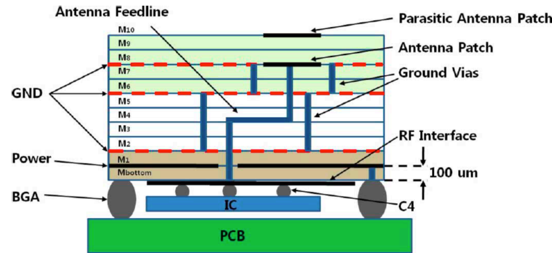


Figure 2.11: 60 GHz LTCC antenna-in-package [5]

In an effort to allow the 60 GHz market to continue to flourish, Dong Gun Kam and fellow researchers developed an LTCC independent packaging solution that saw improved cost savings. Using standard organic PCB processes to combine newly developed alternative mmWave packaging material, liquid crystal polymer (LCP), with that of RF based glass reinforced PCB laminates, a package structure was developed that was compatible with mainstream manufacturing and assembly, conformed to the structure of the IC and yielded good RF performance and mechanical reliability. The stackup consisted of 5 stacked layers (6 metal); one LCP core, and two top and bottom Rogers 4000 (RO 4000) laminates. Jade adhesives were used to bind the RO laminates, meanwhile a combination of Jade and LCP bondyply was used for the core. An open air cavity at the bottom of the package allowed the beamformer IC to flip chip mount directly onto the inner LCP core layer, avoiding significant high loss via transitions (Figure 2.12). Material properties needed to be extracted before hand for EM simulation integration, due to lack of manufacturer knowledge at 60 GHz. A planar radiator utilizing an aperture coupled feed, with under patch air cavity

was used to improve bandwidth and radiation efficiency, while simultaneously isolating the radiator from the active circuitry. Utilizing quadrant symmetry, the feed line design was simplified with faster simulation times considering the usage of a single chip [6].

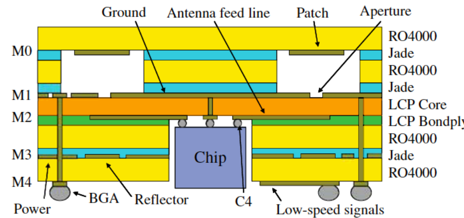


Figure 2.12: 60 GHz Organic antenna-in-package [6]

The array of 16 elements assembled in a ring shape, yielded higher side lobe levels than that of a 16 element linear array. Performance was adequate, with single element gain of 5.5 dBi, however significant variation of gain (2-8 dBi) was seen across different elements in the array. This was attributed to finite array behaviour, encompassing coupling to surrounding elements, and a truncated ground plane leading to parallel plate mode and surface wave radiation. The active return loss was assessed, incorporating the effect of coupling (simulations showed -17 dB), and the array exhibited 10 GHz bandwidth. Overall, measurement and simulations exhibited good correlation. A 5.6 Gbps link using a single carrier, 16 quadrature amplitude modulation (QAM) signal was achieved at a link distance of 4 meters. The author made note however, of the fact that assembling such a structure with new materials like LCP was challenging. LCP integrated into the PCB process caused adhesives to introduce voids, which later with gas trapped at high temperature triggered delamination [6].

In 2012, knowing that high loss, low gain and low radiation efficiency on chip antennas were not the feasible mass market solution for commercial applications, Hong et al. continued their development in low cost packaging and introduced a third potential variant for the Antenna-in-Package design scheme. Also known as antenna on PCB, the designed package leveraged the existing FR4 PCB production line capabilities to yield an ultra low cost stackup constructed solely from FR4 materials; one 150μm core ($D_k = 3.54$) and four 50μm prepregs ($D_k = 3.59$), bonded via 5μm FR4 adhesives. The package combated potential signal loss from high loss laminates, $tan(\delta) = 0.012$, via vertical schematic layout and intelligent feed line design (Figure 2.13). Due to the limited via travel in the FR4 process, the vertical schematic assigned the antenna and feed line to the upper and middle layers respectively, leaving low frequency and power distribution on the bottom of the stack. A circular stacked patch radiator was implemented which utilized a surrounding

ground plane for the probe fed radiator in conjunction with alternating ground vias to minimize parallel plate and surface wave modes. The feed line made use of a coplanar waveguide (CPW) structure, with transitions ground shielded and treated as quasicoaxial. Resulting unit loss exhibited characteristics similar to that of LTCC, however impedance match could not be improved due to FR4 PCB process line width limitations [7].

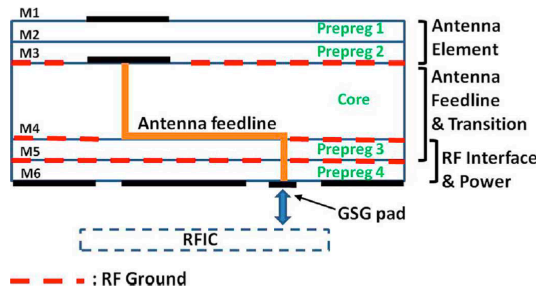


Figure 2.13: 60 GHz PCB based antenna-in-package [7]

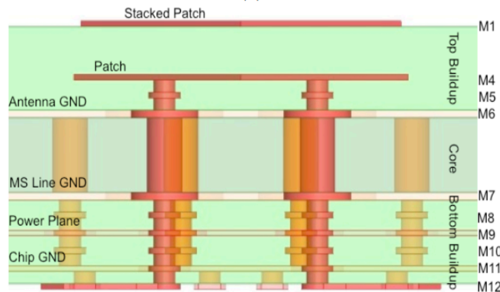
The antenna array was composed of a 4x2 arrangement of radiators, exhibiting a simulated -19 dB mutual coupling. Wafer probe measurements were conducted as IC implementation was to be investigated at a later date, however feed lines were designed with Y-axis symmetry assuming single chip integration. The antenna exhibited 4.1 dBi gain and 76% radiation efficiency and a bandwidth of 9 GHz (57 - 66 GHz). Measurement discrepancies again saw off axis radiation deviation from simulation, attributed to potential scattering and multipath effects along with finite ground edge radiation. Despite the high loss tangent and minor measurement setbacks, the efforts Hong et al. put forth introduced a viable alternative for mmWave phased array package design [7].

2.3.2 Successive Developments at W-Band (75 - 110 GHz)

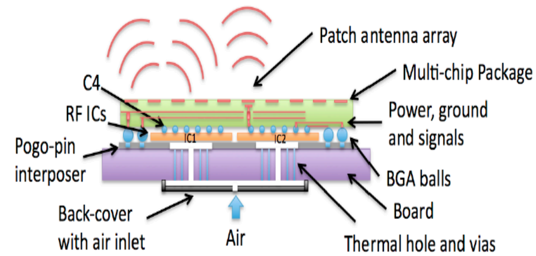
Applications like imaging and radar make use of large available bandwidth and improved atmospheric absorption characteristics at W Band, however systems are still subjected to extreme pathloss given the inverse relationship between frequency and wavelength. W Band communication systems traditionally utilized waveguide interfaces with expensive modules and narrow beam high gain antennas to support high data rate links [35]. Taking advantage of phased array development at 60 GHz and harnessing spectrally efficient techniques, researches extended the capabilities of phased array systems upwards of 75 GHz.

In 2013, great efforts by researchers at IBMs T.J. Watson Research Center were put into the development of a fully integrated dual polarization transceiver. Their 2013 conference proceeding titled "A Fully-Integrated Dual-Polarization 16-Element W-band Phased-Array Transceiver in SiGe BiCMOS" introduced a suitable, compact, low weight and low volume RFIC for W Band, which housed two independent chains per polarization. With the highest level of monolithic integration achieved in silicon at the time, the beamformer IC contained IF and LO distribution on chip, set up for operation in 16Rx-16Rx or 16Tx-16Rx simultaneously. The IC employed compact form factor to conform to half wavelength lattice spacing, enabling phased array solutions to potentially scale at the board level [36].

Implementing dual polarization antennas with fine pitch at W Band reserved itself as a challenge to many package manufacturers. In 2014, Liu et al. introduced a planar stacked patch antenna for organic antenna-in-package implementation. The dual polarized probe fed stacked patch harnessed a 12 metal layer stackup with 2 metal core and 5 metal top and bottom build ups exhibiting the same permittivity (Figure 2.14). The feed line consisted of a direct via with vertical ground shielding resembling that of coaxial line, that travelled from the fed patch layer (M4) down to the bottom layer (M12). The antenna exhibited 3 dBi peak gain and 8 GHz bandwidth, centered at 94 GHz with slight deviations from simulation due to metal fill requirements in the organic buildup process [37].



(a) Organic package stackup [37]

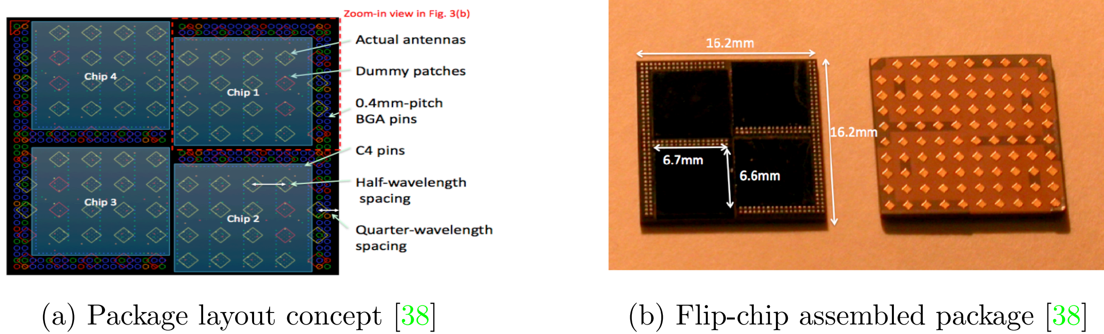


(b) Modular concept [38]

Figure 2.14: IBM Research W-Band phased array stackup and module integration scheme

Integrating both the beamforming IC and antenna element, Gu et al. developed a 100 element array with 64 active elements and 36 dummy elements. By sheer integration complexity, a larger package allowed the implementation of 4 beamforming ICs at the expense of antenna fill factor (Figure 2.15). Fill factor for this array of 64% required random placing of dummy elements to minimize the impact on side lobes. Simulation times for the 128 port array took place in ANSYS High Frequency Structure Simulator (HFSS) full wave electromagnetic simulator, which took an elapsed time of 9 hours and

146 GB peak memory for a single frequency. The array was later simulated in 16 element quadrants, enhancing simulation time, where all other elements were assumed to exhibit same behaviour. The bottom buildup in the organic stack contained low frequency signal routing and extensive circuit-package-antenna co-design was performed to yield optimal placement of ICs to enable board level scaling [38].

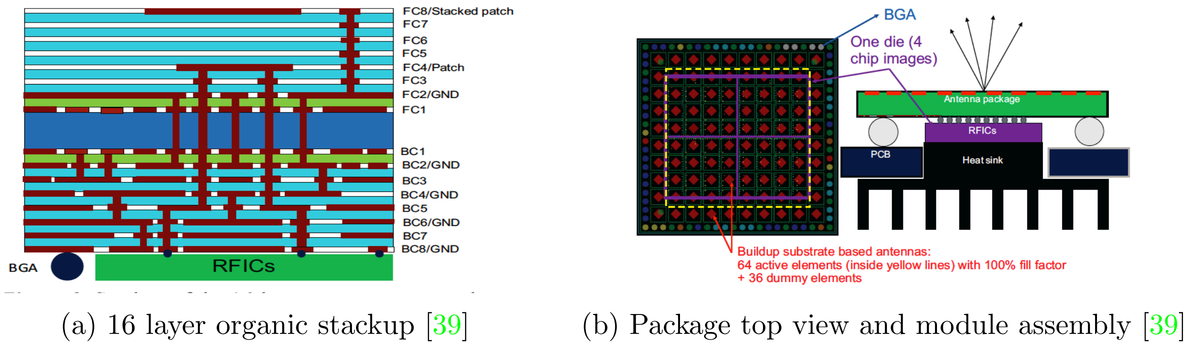


(a) Package layout concept [38] (b) Flip-chip assembled package [38]

Figure 2.15: IBM Research W-Band phased array implementation

The array assembly process incorporated underfill after IC attachment to enhance structural reliability and distribute thermal mistmatch stress. An evaluation board with high speed pogo pins test socket was used to monitor synthesizer locking and voltage and current consumption of power supplies, prior to package assembly on PCB. This module level testing further supported the scalable architecture. Final measurements illustrated cross polarization isolation of -25 dB for the full array with single elements exhibiting -15 dB. Similar gain variation to V-Band arrays was seen with -5 to +2 dBi measured. Maximum EIRP was measured at 28 dBm for 64 transmit antennas which indicated the feasibility of board level scalable phased arrays [38]

Further efforts at enhancing said design architecture came in 2018, where the organic stackup was extended to 16 metal layers, utilizing a super die composed of 4 SiGe RFICs. This introduced reduced assembly steps and improved overall assembly yield. Additionally, the array architecture was redefined, where 100 elements (64 active, 36 dummy) were still utilized, however fill factor was improved to 100%. By placing the dummys on the perimeter of the array, element pattern uniformity was enhanced without impacting active array performance. This employed an additional level of symmetry in feed line routing, where all lines were identical and phase matched. The array exhibited slightly higher bandwidth, simulated scan range of +/- 30 degrees, peak realized element gain of 2 dBi, -12 dB cross polarization isolation and -20 dB side lobes [39].

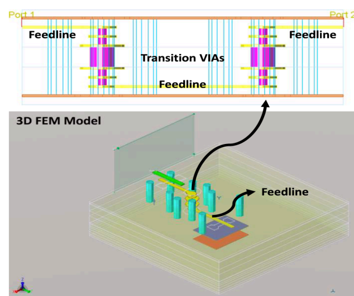


(a) 16 layer organic stackup [39] (b) Package top view and module assembly [39]

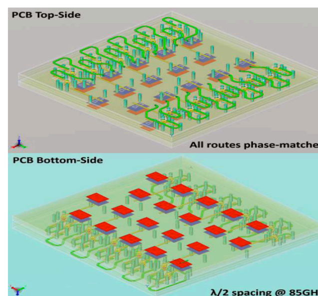
Figure 2.16: IBM Research Enhanced W-Band phased array implementation

In contrast to the efforts by IBM research, antenna-on-PCB implementations at W Band have also been developed by Bell Laboratories, first in 2015, with a second generation implementation in 2018. Shahramian et al. introduced a 20 element transceiver chipset, where 16 elements were Tx (Rx) and 4 elements were Rx (Tx) [40]. Two chipsets were flip-chip mounted and drove two separate 20 element arrays, housed on the same PCB. One array was designed to operate in vertical polarization, while the other horizontal. This demonstrated dual polarization support for increased throughput. Utilizing an aperture coupled stacked patch radiator to isolate the radiator from the feed along with several coupling apertures to allow for the use of only a single via transition, the antenna design exhibited an astonishing 1 dB feed line loss measured at 100 GHz (Figure 2.17). Several 3D FEM based electromagnetic simulations were performed on the entire stackup with IC and PCB co-design via the inclusion of the flip-chip bump parasitic model, yielding optimal matching conditions. Package stackup was not disclosed.

Array implementation involved half wavelength lattice spacing, arranged in a triangular grid of 4x5 elements. Assembly incorporated underfill after RFIC placement to distribute added stress from thermal expansion mismatch between the RFIC and PCB at the attachment joints. First generation array prototypes exhibited 34 dBm EIRP across a wide bandwidth (80 - 90 GHz), with 14 dBi array gain, -15 dB side lobe level and - 25 dB cross polarization. A 20 meter link was measured achieving 4.8 Gbps under QPSK modulation scheme in each polarization [40]. Second generation designs exceeded the previous, achieving 8 Gbps at 20 meters, with a 1 meter link extending rates all the way to 30 Gbps using 64 QAM. Utilizing both arrays, 60 Gbps is achievable. Scan range included out to +/- 30 degrees, and individual antenna radiation efficiency achieved an even more remarkable 92% at 90 GHz [35].



(a) Antenna feed line [35]



(b) Phased array antenna structure [35]

Figure 2.17: W-Band antenna-on-PCB phased array implementation

2.3.3 Current Developments at Ka-Band (27 - 40 GHz)

Developments at Ka Band have been most rapid due to the anticipation of upcoming 5G networks, with several variations of packaged phased arrays developed within the last two years. Knowledge acquired from extensive research conducted at V and W Band, allowed many of the designed 5G phased arrays to share similar buildup and package methodology. The package variants introduced almost 10 years prior have stood the test of time and with cost driving mainstream phased array implementation, materials like LTCC are seldom found in Ka Band antenna-in-package realization. As mentioned in the published article on W Band scalable phased arrays, fabrication of organic based packages exhibit lower tolerances than that of PCB fabricators [41]. However, due to the inverse relationship between frequency and wavelength, tolerance becomes effectively more tolerable at Ka Band, where wavelengths range from 7.49mm to 11.10mm as opposed to 2.73mm to 4.00mm at W Band.

Carrying over experience gained from W Band implementations, IBM research's first attempt at an organic antenna-in-package solution for 30.5 GHz took place in 2017 with the anticipation of their upcoming 32 element phased array transceiver IC with concurrent dual polarized beams [42]. Introduced in their publication titled "Antenna-in-Package Design Considerations for Ka-Band 5G Communication Applications" and abiding by fabrication constraints and limited material selection, a 14 metal layer stackup was implemented which consisted of a thicker core (4 metal layers), with thinner top and bottom buildups (5 metal layers each), all exhibiting relatively high loss tangent of 0.01. Governed by significant fabrication constraints, antenna design was constricted to limited via density, where three ground vias were used to shield the vertical quasicoaxial transition leading to 0.5 dB loss, with thicker core layer requiring larger via diameter and increased spacing, ultimately

placing limitations on line characteristic impedance. A dual polarized, probe fed stacked patch was utilized where patch corners were cut to modify resonance behaviour. Utilizing grounded metal rings (mentioned previous) to reduce surface wave excitation, the antenna was able to achieve 0.8 GHz bandwidth, 3 dBi gain and less that -20 dB mutual coupling. Impedance bandwidth outlined itself as the main bottleneck and was attributed to limited material selection with appropriate permittivities, low layer count resulting in lack of antenna volume, necessary requirement of half wavelength spacing for beamforming and dual polarization functionality restricting the number of usable bandwidth extension techniques [21].

In an attempt to alleviate the impedance bandwidth limitations, IBM research introduced a second generation complex multi tier organic stackup which consisted of a 14 metal layer base, similar to previous, with the introduction of a 2 layer lid substrate and 2 layer frame for the formation of a uniform air cavity (Figure 2.18). Utilizing a dual polarized aperture coupled stacked patch with each polarization fed on separate layers, and harnessing the uniform air cavity for increased bandwidth, gain and reduced surface wave excitation, the antenna element was capable of 3.3 - 3.7 GHz bandwidth for each polarization. A prototype test vehicle was fabricated prior to array implementation which allowed researchers to investigate interconnect performance, package warpage and chip and board level reliability prior to full array implementation [43, 44].

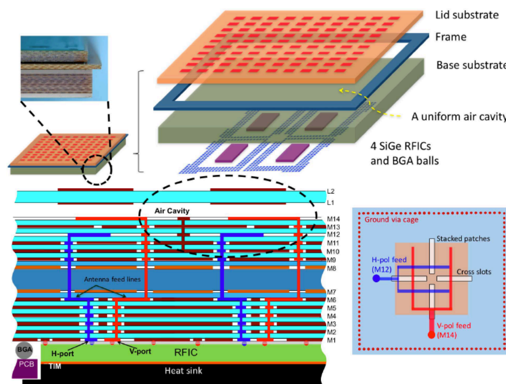


Figure 2.18: 28 GHz Organic AiP [8]

Similar to the implementation at W Band, a 100 element array was implemented with 64 active elements and 36 dummy elements around the edge to improve element pattern uniformity, leading to 100% fill factor. Four 32 element RFICs with internal frequency translation are flip chip mounted with underfill, and the package is further mounted via

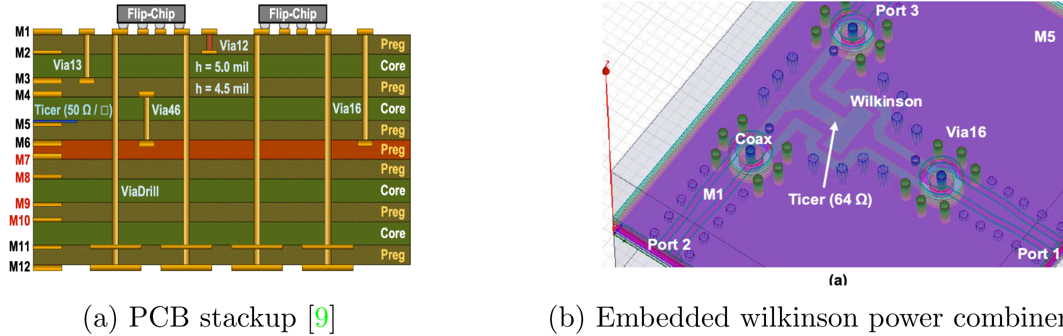
BGA to a breakout PCB housing IF, LO, control signals and bias. The array exhibited 54 dBm EIRP at broadside, with +/- 40 degree scan range in both principle E and H planes, for both polarizations. Using no calibration, the array was able to achieve -12 dB side lobe level and 20 dB deep pattern notches. Link measurements using two arrays, each with two single 64 element beams (one per polarization) and a carrier aggregated 8x100 MHz 256 QAM signal, resulted in an astounding 21 Gbps data rate. Extending the range to 50 meter and 19 meter through glass links, 6.7 Gbps raw data rate with 4-5% error vector magnitude (EVM) was achieved [43, 44]. IBM's research efforts resulted in state of the art performance at the expense of complex packaging and assembly.

In contrast to organic implementations, in 2017, leveraging the lack of publications in packaged antenna array and transceiver implementations for 28 GHz, researchers Kim et al. of LG Electronics developed a 28 GHz CMOS direct conversion transceiver integrated with a 2x4 element antenna array in an PCB based antenna-in-package design. Design objectives included high EIRP, good beamforming capability and low in band signal distortion (EVM). Kim et al. proposed a stackup consisting of 8 metal layers, one 400μm core ($D_k = 4.4$, $tan(\delta) = 0.006$), 3 30μm prepreg layers on top and bottom ($D_k = 3.7$, $tan(\delta) = 0.007$), followed by top and bottom 15μm solder resist ($D_k = 3.5$, $tan(\delta) = 0.015$). Utilizing a single probe fed patch with ground via fence to improve isolation from adjacent antennas, the antenna exhibited 1.5 GHz bandwidth and worst case -18 dB mutual coupling [45].

Array implementation involved half wavelength spacing to avoid potential grating lobes in the scan range, combined with high routing complexity due to single RFIC driving the array. The resulting feed line loss neared 1 dB with final array measurements indicated 13 dBi realized gain. Achievable scan range was limited to +/- 30 degrees, with broadside EIRP of 23 dBm for 8 elements active. Link measurements indicated that at 25 meters, 2.2 - 7.6% EVM was attainable dependant on array drive, where signal bandwidth was limited to 20 MHz, limiting system throughput [46].

In an effort to demonstrate the sheer capability of a 5G link, researchers at UCSD leveraged the low cost nature of PCB fabrication in conjunction with symmetrical design to develop a scalable phased array capable of double digit gigabit speeds. Presented in their 2018 IMS conference proceeding [47] and later extended in their MTT transaction [9], Kibaroglu et al. introduced an antenna on PCB design that utilized a 12 metal layer symmetric stackup composed of megtron-6 core and prepreg layers ($D_k = 3.3$, $tan(\delta) = 0.005$ @ 29 GHz), where design emphasis was placed on a 2x2 unit cell, which could be scaled to any effective size (Figure 2.19a). Master slave boundaries in HFSS were used to analyze single element behaviour in a periodic arrangement and resulting behaviour was combined with circuit simulator to design the antenna matching network and integrate their in house flip-chip bump parasitic model. A probe fed stacked patch was fed with

highly isolated feed lines to not introduce random amplitude and phase errors across lines and the resultant bandwidth was 4 GHz, with feed line loss ranging from 0.8 - 1.3 dB.



(a) PCB stackup [9]

(b) Embedded wilkinson power combiner [9]

Figure 2.19: 28 GHz antenna-on-PCB phased array implementation

A 100 element array was developed with 36 dummy elements used around the edges to improve element pattern uniformity (Figure 2.20). An asymmetric lattice was used, consisting of 0.5λ x 0.63λ spacing, limiting the effective scan range. Since the usage of small beamformer RFICs was employed, feed line design was simplified and performed in a symmetric manner. This however makes RF routing much more complicated, and in this case an embedded wilkinson with resistive Ticer layer was utilized to perform on PCB power splitting / combining (Figure 2.19b). Due to the efforts involved in maximizing symmetry, array performance is superior without calibration. Scan range exhibits +/- 50 degrees in the H plane, with +/- 25 degrees in the E plane (limitation on lattice dimension), without significant deterioration in side lobe level, or beam pointing direction. A saturated EIRP of 52 dBm was achievable with a demonstrated 300 meter link composed of a transmit and receive array achieving 8-12 Gbps for 16/64 QAM waveforms, with 1.5 - 3 GHz modulation bandwidth, and resulting in 5 - 10% EVM [9]. The aforementioned design outlines the ramifications of symmetric design, reducing cost not only in the structure, but that of cost associated with calibration efforts in production environment, albeit given the complex package implementation, RFIC antenna in house co-design capabilities, and limited scan range.

A final most notable implementation which enabled a larger scanning range at the expense of increased loss came in the form of the 5G phased array system developed by Risto Valkonen of Nokia Bell Labs, in 2018. Taking advantage of affordable RF laminates (Rogers RO 4350B (D_k = 3.66, $tan(\delta)$ = 0.0037) and RO 4450F bondply (D_k = 3.52, $tan(\delta)$ = 0.0037)), a 10 metal layer antenna on PCB package was constructed. Valkonen applied the sub array scaling principle and designed a 2x2 unit cell, which was later fed

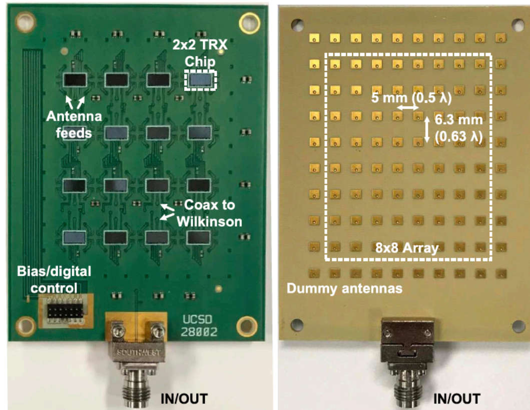
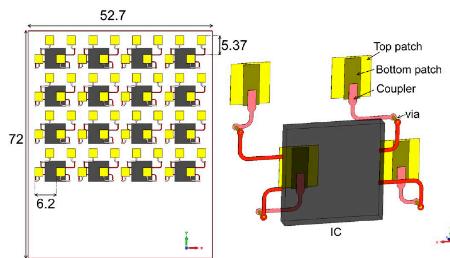
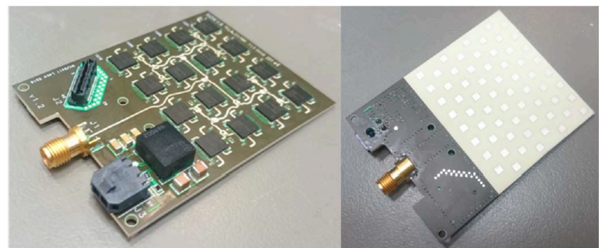


Figure 2.20: 28 GHz Fabricated Antenna-on-PCB [9]

with Anokiwave 0108 commercial QFN packaged beamformer chip. Using an equilateral triangular grid, elements could be placed further apart without impeding the scan range, while simultaneously improving isolation. A stacked, capacitively coupled patch radiator was used, however due to the array arrangement, multiple layers were required to be used to achieve matched phase condition across feed lines. This effectively introduced significant losses in the system, where feed lines were yielding 2-2.5 dB loss. Despite this, the array achieved 3 GHz impedance bandwidth with scan range of +/- 45 degrees in both E and H planes. Without calibration, the array exhibited 48 dBm EIRP with side lobe levels -13.1 dB, matching simulation within +/- 1.1 dB [48].



(a) 2x2 sub-array [48]



(b) Fabricated array [48]

Figure 2.21: 28 GHz antenna-on-PCB phased array implementation with a triangular grid

2.3.4 Implementation Summary

As established in the aforementioned review, LTCC substrates are rarely found in Ka-Band phased array implementation. Organic packages yielded the potential for similar performance, with improved cost benefit. However, organic packages exhibit higher cost than that of PCB, and this is a result of reduced fabrication tolerance with increased potential for design realization. Yet, such upside cannot compensate for the complex stackup definition and radiator design shown necessary by IBM Research to achieve desired performance for fifth generation networks.

Similar performance to organic implementations were found in several antenna-on-PCB packages within the last two years, all exhibiting significantly reduced stackup complexity. Nonetheless, said implementations still presented significant bottlenecks in overall design. LG Electronics attempt saw poor bandwidth and complex feed line routing due to single IC implementation. UCSD achieved remarkable data rates with no calibration, however the stackup implemented required non-traditional Ticer resistve layer implementation, not found in all fabrication houses. Half wavelength spacing was not met in both principle planes, and a limited scan range resulted. Further, the benefit the design received from in-house IC design does not extend to parties wishing to design a system without such resources. Nokia's attempt at PCB AiP implementation outlined one of the simplest approaches taken, achieving significant scan volume with both commercial RF laminates and beamformer RFICs. Nevertheless, this was met with significant feed line loss, reducing radiator efficiency and ultimately demanding more from the QFN packaged beamformer.

Considering all this, no such package implementation exists that compensates for the above-mentioned disadvantages, yet meets 5G phased array requirements; large scan volume and >10% bandwidth. Going foreword therefore, this work looks to achieve a significantly reduced complexity design that can meet fifth generation specifications, improve system efficiency and leverage commercial technologies to drive mass market realization.

Chapter 3

Antenna-in-Package Design for RF Beamforming 28 GHz Applications

Extensive past research efforts have outlined the superiority of the antenna-in-package concept for phased array implementation across multiple frequency bands. Given the ever evolving requirements for Ka Band phased array systems and rapid ongoing development efforts, an implementation which encompasses the capabilities of past implementations, while simultaneously mitigating the collective limitations is crucial to harnessing the sheer potential of the 5G network infrastructure.

Mass market solutions favor scalability, low cost of production and high reliability, while communication needs desire large impedance bandwidth, efficient circuit operation and beam steering versatility. Utilizing an antenna-on-PCB implementation of the AiP concept, an RF beamforming phased array can be designed to leverage both existing, mature PCB fabrication processes along with commercially available, leading edge RF components, to simplify the design process, meeting communication standards and alleviate existing system limitations.

3.1 Project Scope

Developing a phased array system for 28 GHz operation requires preliminary project scoping to minimize the need for redesign due unrealizable circuit layout and fabricator incompatibility, increase the likelihood of successful of assembly and ensure optimal system level performance due to maximal model to hardware correlation.

3.1.1 Components

Required for phased array operation are both the RF front end module and the antenna array. Integrating the two with minimal impact on performance is the PCB package. Therefore, priority is placed on beamformer selection in order to predfine the package potential. To utilize the RF beamforming architecture in conjunction with maximizing potential beamforming capability, the quad core beamformer RFIC developed by Anokiwave is chosen. The Anokiwave AWMF 0158 silicon based Tx/Rx four channel RFIC is a half duplex beamformer that exhibits a Tx (Rx) gain of 25 dB (30 dB), with 15.5 dBm Tx OP1dB and 4.8 dB Rx NF per channel. Frequency translation is performed off chip for IF flexibility at the expense of RF package routing complexity. The device is packaged in a 3.6 mm x 3.6 mm wafer level chip scale package (WLCSP) for easy flip-chip installation [site anokiwave]. Small form factor and quad core design decrease layout density and improve system reliability, with any IC failure yielding significantly less impact on array fill factor.

3.1.2 Constraints

Constraints on the design landscape effectively dictate the manufacturing feasibility of the AiP. A system of such complexity is subjected to constraints imposed by the PCB fabricator, in addition to the ones set in place by the chip manufacturer regarding system assembly. Following guidelines in place by such entities is detrimental to package realization as it allows processes to be utilized, which come with a high guarantee of success, further supporting mass market implementation.

For optimal performance, Anokiwave's beamformer IC requires specific landing pad features, in addition to sufficient grounding across the entirety of the chip. Flip-chip enabled packages like the AWMF 0158 utilize a fine pitch ball grid array to minimize package footprint. To mount to the PCB, the AWMF 0158, with pitch 0.4 mm, requires circular landing pads of 10.5 mil diameter. Meeting this constraint implies pad edge to edge spacing of roughly 5.25 mil. Further, enforcing proper grounding of the chip for areas such as ground-signal-ground (GSG) RF launch points requires the usage of μ-Vias; fine diameter laser drilled vias with the potential for precise placement. Utilizing such a via effectively limits the available number of commercial substrates as implementation requires substrate thickness no greater than 4 mil. Additional substrate limitations arise from the fact that such a chipset does not contain RF power combining / splitting on chip, therefore requiring the PCB to contain low loss, RF compatible laminates that permit reasonable impedance values for PCB line limitations.

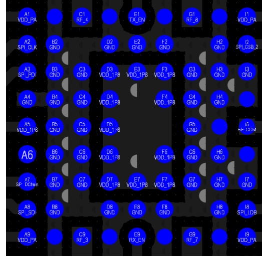


Figure 3.1: AWMF 0158 Landing Pad

PCB fabrication constraints vary dependant on IPC classification. In PCB manufacturing, quality control is of great concern and as a result the IPC standards organization outlined three PCB classes within the IPC-6011 class set [49]. Class 1 is the most broad and outlines constraints for general electronic products. Class 2 focuses its attention on PCBs for dedicated service electronics such as communication equipment. Class 3 extends itself to high reliability electronics, one step short of military and aerospace grade. For this design, Class 2 constraints are used and the ones pertinent to an RF designer are outlined in Table 3.1. Important to note are the line width and edge to edge spacing constraints as they are directly impacted by starting copper thickness and stackup via definitions. Etching procedures perform optimally when metal thickness is low and in multi-layer designs requiring internal interconnects, vias are drilled and plated prior to lamination of additional substrates. Plating is non-ideal and results in copper deposition not only in the hole, but on the PCB surface. Generally, for 1 mil deposited in the drilled hole, one can expect 1.4 mil excess deposited copper on the PCB surface (ratio of 1:1.4) [50]. Therefore much attention is given to the stackup definition as excess plating cycles may potentially inhibit fabrication of the AWMF landing pad.

3.1.3 Specifications

System specifications are predominantly derived from the Anokiwave AWMF 0158 beamformer IC. Outlining necessities in the package, the AWMF 0158 chipset requires low frequency digital control signals (serial peripheral interface - SPI) in conjunction with two individual power supplies. To ensure optimal RF performance, the stack therefore must provide package real estate to maintain bias purity. In addition, given the average current drawn by a single beamformer IC nears 0.5 Ampere, power planes are required for adequate distribution without excessive resistive loss. All together, this imposes a multi-layer spec on the PCB package that extends beyond traditional three layer antenna implementation.

Table 3.1: IPC Class 2 PCB Fabrication Constraints

Constraint	Value
Line Width	4 mil Inner 5 mil Outer
Edge to Edge Spacing	4 mil Inner 5 mil Outer
Through Hole (TH) **Via Diameter**	8 - 12 mil < 100 mil Board Thickness
Blind (BL) **Via Diameter**	Equal to Drill Depth + 2 - 5 mil Over Penetration
μ**-Via Diameter**	<6 mil
Via Pad Diameter	Via Diameter (TH / BL) + 8 - 10 mil
Via Anti Pad Diameter	Via Diameter (TH / BL) + 20 mil

The beamformer IC operates within the 26.5 GHz - 29.5 GHz band, effectively enforcing the antenna impedance bandwidth specification, where matched condition exists for 50 Ohm antenna input impedance when S11 $<$ -10 dB, as recommended by IC manufacturer. Moreover, to leverage the full output power capabilities of the RFIC, antenna efficiency should be maximized, including feed line losses. Consequently, defining the aforementioned specifications indirectly defines a subset of the necessary array specifications when in context of the AiP. However, as identified in section 2.1.2 on mutual coupling effects, input impedance of an antenna within an array is a function of the coupling characteristics (S_{ij}) of the surrounding radiators. As a result, defining a bandwidth spec suggests the imposition of tolerable coupling magnitude.

Although this is true, coupling quantities are complex, consisting of magnitude and phase, and as research outlined in both [51] and [52] suggests, fluctuations in element impedance with scan angle can be reduced by decrease of the array unit cell size. This effectively harnesses the phase properties of the coupling characteristics to work in favor of the array. Therefore, specifications regarding array bandwidth are not trivial to define, yet a reasonable starting point is to assume a sensible level of isolation is achievable. With

Table 3.2: AiP System Requirements and Specifications

Item	Value
Layer Count	>3
Bandwidth	26.5 GHz - 29.5 GHz
Antenna Efficiency	Maximized
Element to Element Isolation (If Achievable)	<-22.5 dB
Power Combiner Output Port Isolation	<-20 dB
Power Combiner to Antenna Array Isolation	Maximized

the assumption of a rectangular array where adjacent elements yield equal magnitude and highest coupling, coupling along the diagonal is negligible and element match is excellent (S11 $<$ -35 dB), a quick calculation advocates coupling magnitude not exceed -22.5 dB for ARC of -10 dB. With mutual coupling handled, scan range can be maximized and effectively becomes a sole function of the array layout and element pattern. To avoid the introduction of grating lobes, element pitch must not exceed free space half wavelength at the highest frequency (29.5 GHz).

Moreover, due to the RFICs requirement of power combining off chip, preliminary combining specifications can be defined to guide the design process. The power combiner must adhere to the bandwidth spec stated previous, with the assumption of 50 Ohm source and load terminations. Isolation is of great importance and at the output of the power combiner, port to port isolation no greater than -20 dB (S23 $<$ -20 dB) is adequate for efficient operation, as cascaded combiner isolation can significantly degrade otherwise. In addition, isolation of the combiner from the antenna array should be maximized due to high gain characteristics of the RFIC. This will ensure the common input of the power combiner yields good match for all scan angles, while simultaneously preventing the introduction of any instability via minimizing feedback to input of the AWMF 0158 beamformer. A summary of all requirements and specifications can be found in Table 3.2.

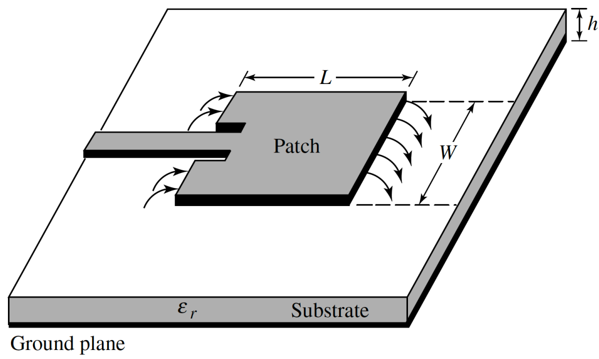
3.2 Radiator Selection and Stackup Definition

Antenna-in-Package implementations can vary significantly based off choice of radiator. When integrating the antenna on a PCB package as in the antenna-on-PCB concept, planar antennas are favored as they are low cost and easy to implement via PCB processes. Given the radiation is directed broadside and not into the PCB, the patch antenna become the most appropriate candidate. However stackup definitions can be detrimental to performance, and given the target bandwidth specification exceeds 10% fractional bandwidth, a radiator that compliments the PCB buildup increases the likelihood of success.

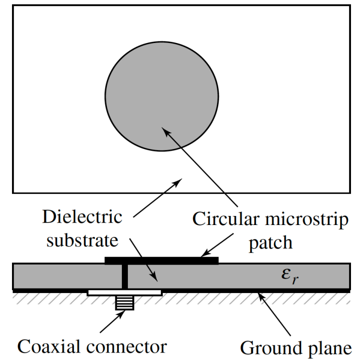
3.2.1 Radiator

Given the AiP is a multilayer structure and active circuitry (bottom side) is to be isolated from the antenna array (top side), vertical transitions are necessary to connect the two. However, interconnects are sources of loss and potential radiation resulting in reduced efficiency and beam pattern non-idealities. Limiting the number of interconnects is paramount in developing a system which exhibits low loss. Leveraging the small form factor of the AWMF 0158, much of the feed line can be implemented on the bottom layer leaving the need for only one vertical transition, with overall feed line length minimized.

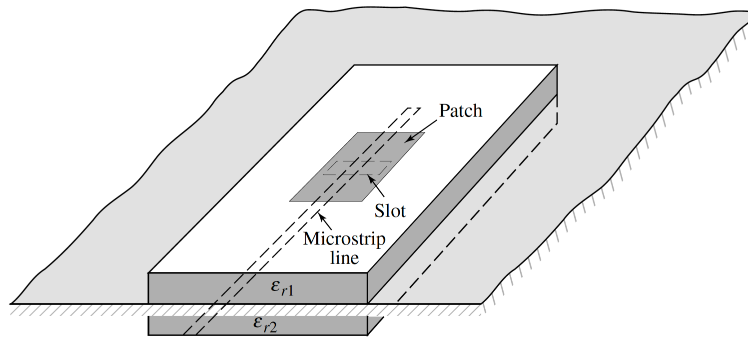
Employing a single via transition and planar patch radiator effectively defines the number of available antenna feeding structures. Typically a patch antenna can be fed via microstrip line, probe, aperture-coupling or proximity coupling (Figure 3.2). Microstrip line feeding requires excess space on the patch layer, and due to its transmission line characteristics and top layer exposure, becomes a potential source of spurious radiation. Probe feeding reduces spurious radiation, however it is known to yield limited impedance bandwidth. As a result, additional parasitic patches are used to broaden available bandwidth albeit the introduction of additional substrate layers. Aperture coupling yields moderate spurious radiation, isolates the feed entirely from the radiator and can leverage slot resonance to obtain large impedance bandwidth. However, aperture coupling is most difficult to fabricate and requires embedded transmission line structures (stripline, co-planar waveguide) to realize the feed below the ground layer. Known for the largest bandwidth of the four, proximity coupling exhibits near 13% bandwidth while simultaneously possessing low spurious radiation. The feed presents moderate fabrication complexity and due to its superior bandwidth characteristics, antenna volume can intentionally be restricted by use of thinner substrates, reducing the number of surface wave modes that can exist at the interface, without significantly impacting the overall bandwidth [10]. Consequently, the proximity coupled patch antenna is the chosen radiator for this design.



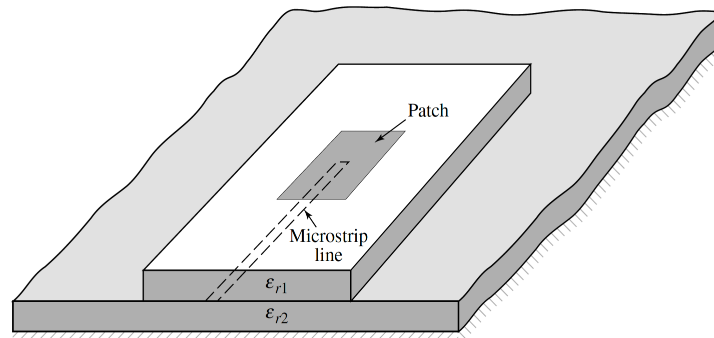
(a) Microstrip line feed



(b) Probe feed



(c) Aperture coupled feed



(d) Proximity coupled feed

Figure 3.2: Feed structures for patch antennas [10]

Table 3.3: Stackup Material Properties [1, 2]

Property	RO 4350B	RO 4450F
Dielectric Constant, ϵ_r	3.66 @ 10 GHz	3.52 +/- 0.05 @ 10 GHz
Dissipation Factor, $tan(\delta)$	0.0037 @ 10 GHz	0.004 @ 10 GHz
Thermal Conductivity (W/m/K)	0.69	0.67
Coefficient of Thermal Expansion (ppm/°C)	10 - X 12 - Y 32 - Z	19 - X 17 - Y 50 - Z

3.2.2 RF PCB Stackup

Multi-layer PCB stackups can be built from a variety of substrates of varying thickness. To ensure maximum fabrication yield, it is often advised to utilize a homogenous structure, where multiples of the same laminate or complimenting laminates are used to construct the stack. For RF PCB applications, low loss materials are preferred, and one common commercial RF laminate used is Rogers RO 4350B with complimenting bondply RO 4450F. Both materials exhibit similar dielectric constant, thermal conductivity and dissipation factor, $tan(\delta)$. Material properties can be found in Table 3.3.

Increased number of layers built into a multi-layer stackup decreases registration accuracy and can affect via placement and overall production yield. Due to the characteristics of the proximity coupled patch allowing for thinner substrates and not requiring parasitic layers, the PCB stackup can utilize less substrate layers for the antenna portion resulting in a thinner overall package and relinquishing potential registration issues.

In determining the number of layers required for the stackup, it is best to implement a vertical schematic outlining layer assignments. Top and bottom layers are reserved for the antenna array patches and RFIC landing pad / power combiner respectively. Two additional layers are required for the implementation of the proximity coupled feed and the patch antenna ground. Mid stack implements IC control signals, with SPI on the top most layer nearest the antenna ground. A ground layer is used to isolate the SPI signals from the two power supply planes delivering +1.8 and + 2.5 volts respectively. A second low frequency layer is implemented for IC chip select and further isolated by an additional ground plane. Finally, an extra ground plane is inserted for μ-via implementation and

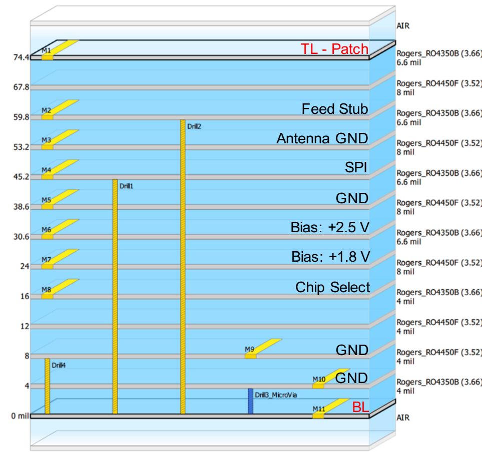


Figure 3.3: RF PCB stackup, vertical schematic and via definitions

serves as the ground reference for the RF power combiner.

Rogers 4000 series laminates, like RO 4350B, are available in various sizes; 4 mil, 6.6 mil, 10 mil, 13.3 mil, 16.6 mil and 20 mil. Bondply materials like RO 4450F however, are manufactured in single 4 mil thick plys. Since a thinner stackup is preferred as it allows for better registration and permits smaller via diameter, substrate thicknesses are kept at 6.6 mil for RO 4350B and two 4 mil RO 4450F bondplys, with two exceptions being the bottom layer, which requires 4 mil RO 4350B for μ-via implementation, and the inserted layer, which uses a combination of 4 mil substrate and bondply to aid in fabrication. In general, 4 mil laminates and sole bondplys were not used due to the fact that the antenna element required 6.6 mil substrate and two 4 mil bondplys to yield optimal performance, further outlined in section 3.3, and the design intended to maximize stackup homogeneity.

Via definitions, as mentioned previous, can impact minimum feature size, especially in areas like the bottom of the package where routing density is high. As a result, definitions must factor in successive drilling and plating steps and their potential implications. As such, to limit the number of drill variations, a single through hole via definition (drill 1 - 8.3 mil diameter) is used for power supply delivery and digital signal interconnects. A separate TH definition (drill 2 - 12/8.3 mil (Signal/GND) diameter) is used to connect the antenna feed layer with the bottom layer of the package and also serve as the feed quasi coaxial ground shield. Further, a μ-via definition (drill 3 - 4 mil diameter) is made to connect the chip landing pad and its respective ground plane, with an additional TH via definition (drill 4 - 9.8 mil diameter) to provide appropriate grounding for edge mount RF connectors. This totals to four separate via definitions, which require plating. A final drill

through the entire stackup is utilized for board mounts, however this is non-plated. The via definitions are illustrated in Figure 3.3, which also outlines the vertical schematic and corresponding stackup definition.

3.3 Antenna Element Analysis and Design

Element design and analysis generally utilizes basic antenna theory for approximation in conjunction with an electromagnetic simulator to optimize for desired radiation characteristics. ANSYS High Frequency Structure Simulator is employed in 3D Layout mode to make use of the predefined stackup such that all design in performed in 2D. This simplifies model management and makes array level layout easier.

3.3.1 Single Element

The proximity coupled patch requires appropriate design of the patch itself, proximity feed, vertical transition and matching network, including the AWMF 0158 landing pad. The design can be decomposed into a series of steps with the first being the determination of patch size for the appropriate resonant frequency. Using the rectangular patch transmission line model, length and width estimates can be obtained for a relative permittivity equal to that of the RO 4350B substrate ($\epsilon_r = 3.66$) and resonance of 28 GHz ($f_r = 28$ GHz).

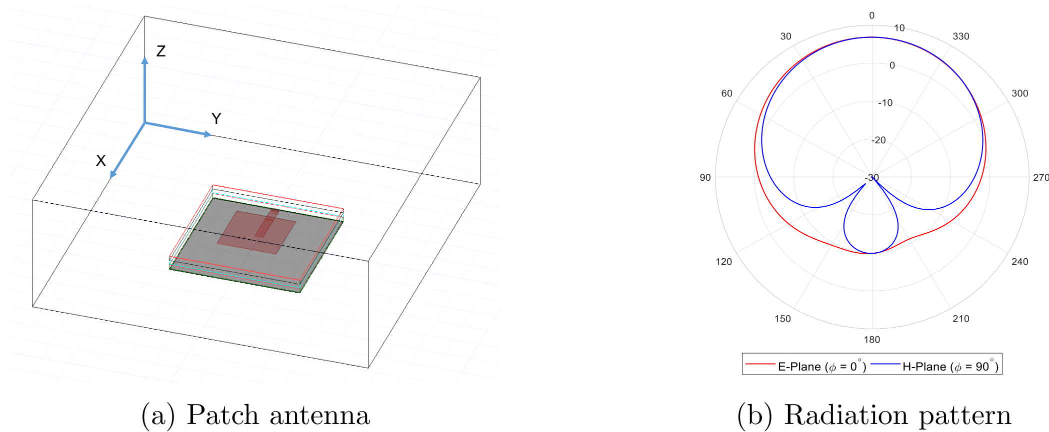
$$W = \frac{\nu_o}{2f_r}\sqrt{\frac{2}{\epsilon_r + 1}} \tag{3.1}$$

$$\epsilon_{reff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left[1 + 12\frac{h}{w}\right]^{-1/2} \quad \text{for} \quad \frac{w}{h} > 1 \tag{3.2}$$

$$\Delta L = 0.412\,h\,\frac{(\epsilon_{reff} + 0.3)}{(\epsilon_{reff} - 0.258)}\,\frac{(\frac{w}{h} + 0.264)}{(\frac{w}{h} + 0.8)} \tag{3.3}$$

$$L = \frac{\nu_o}{2f_r\sqrt{\epsilon_{reff}}} - 2\Delta L \tag{3.4}$$

where ν_o is the free-space velocity of light [10].



(a) Patch antenna

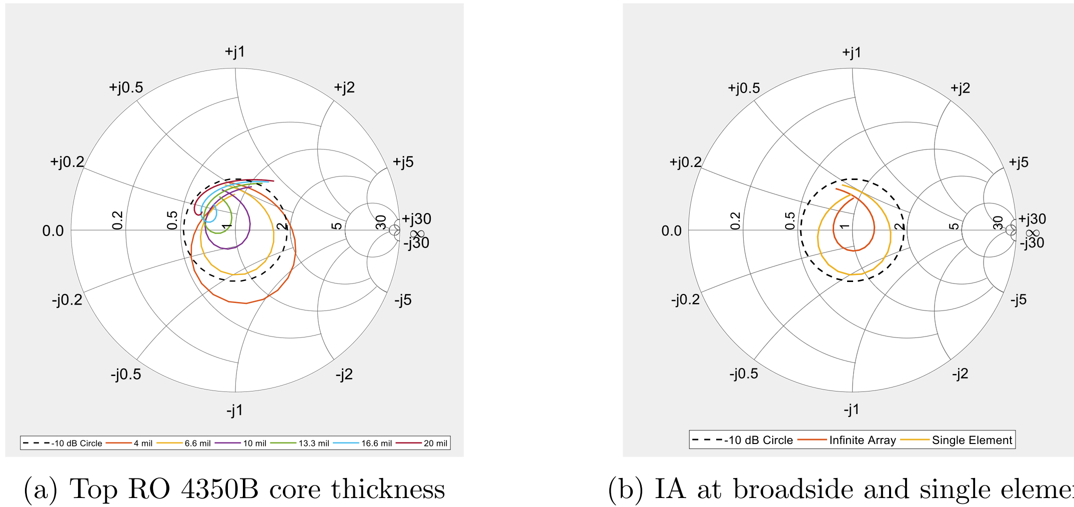
(b) Radiation pattern

Figure 3.4: HFSS 3D Layout model of 28 GHz proximity coupled patch antenna

Between the patch and ground layer, which includes two RO 4350B laminates (referred to as cores going forward) and two 4 mil RO 4450F bondplys (to improve fabrication reliability), substrate thickness can total 16 mil to 48 mil, dependant on core thicknesses implemented. A 50 ohm microstrip feed line implemented between bottom core and top bondply-core superstrate combination is obtained with 12 mil trace width, well above PCB fabrication constraints, utilizing 6.6 mil base core thickness. Such trace width is also important to note, as it must adhere to PCB edge to edge constraints when ground vias are in place for the vertical transition. Variations in superstrate thickness yielded little effect on feed line characteristic impedance. Thus, employing a bottom 6.6 mil core limits total substrate thickness to a range of 18.6 mil to 34.6 mil, which results in patch lengths for of 2.581mm to 2.319 mm, respectively, with corresponding width 3.507 mm. It was found that a symmetric patch of 2.3 mm x 2.3 mm yielded good radiation characteristics at 28 GHz and this can be attributed to proximity coupling being highly dependent on feed stub length and width-to-line ratio of the patch, as well as the inclusion of core permittivity frequency response, extracted from Rogers Microwave Impedance Calculator.

Given the final implementation will include a vertical via transition, design solely of the feed stub and patch focused on the shape of the impedance contour within the smith chart. Feed stub length modifies the amount of electric coupling to the patch, and was therefore optimized to produce a contour that fit within the -10 dB smith chart circle, after renormalization. Absolute impedance values were monitored, keeping mindful of impedance transformation ratios, but not of primary concern as a matching network on the bottom layer of the package would accommodate.

A sweep of the top core thicknesses determines the appropriate substrate height for the



(a) Top RO 4350B core thickness

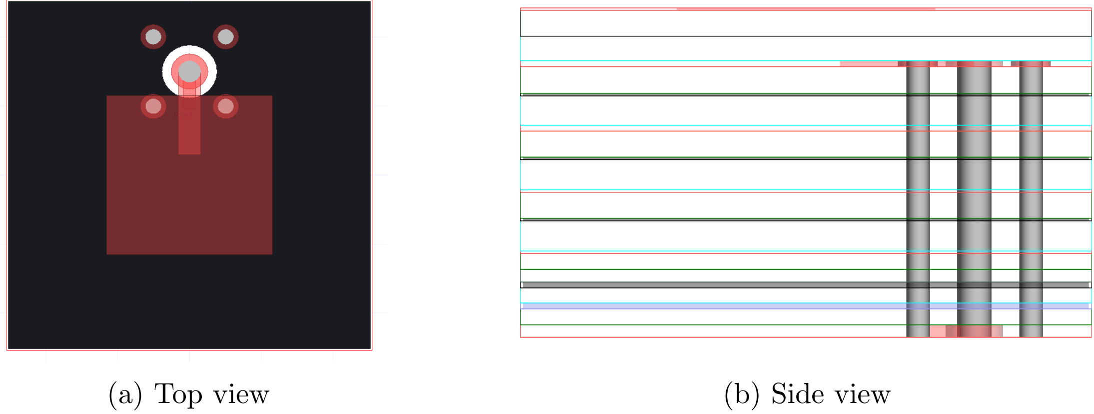
(b) IA at broadside and single element

Figure 3.5: Impedance contour variation for designed antenna, from 25 GHz - 31 GHz

patch antenna. Figure 3.5a illustrates impedance behaviour for core thicknesses 4 mil, 6.6 mil, 10 mil, 13.3 mil, 16.6 mil and 20 mil, with the -10 dB circle outlined in black. The minimum core thickness that achieves the desired bandwidth can easily be identified as 6.6 mil. Minimizing overall thickness as mentioned previous not only aids in fabrication accuracy, but limits the number of surface wave modes that can exist at the metal-substrate interface, aiding in array scan.

To perform preliminary assessment of the antenna functionality within an array setting, infinite array (IA) analysis is conducted. Any major coupling discrepancies can be easily identified prior to array layout and excessive simulation time. ANSYS HFSS utilizes master and corresponding slave boundary conditions to define the array lattice arrangement, where model periodicity is enforced, effectively simplifying array analysis and increasing simulation speed. Electric fields on boundary pairs are assumed to be equal, but with a corresponding phase shift based off input scan angle. Results capture the impact of surrounding elements and relay them in the form of the infinite array element pattern and active reflection coefficient.

Assuming a square array arrangement, with half wavelength spacing for the highest design frequency (29.5 GHz) in both E and H planes, a simulation is conducted to assess the active reflection coefficient. Figure 3.5b outlines the corresponding antenna response, where its resulting impedance contour exhibits improvement. Such an improvement is a results of reduced isolation, however as mentioned previous, coupling characteristics are complex and phase relationships can aid in impedance match. Neglecting structures



(a) Top view

(b) Side view

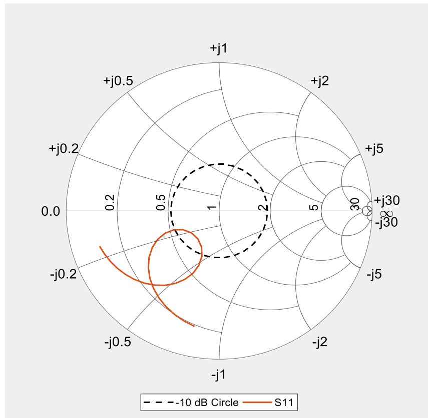
Figure 3.6: Full stack antenna model with vertical transition

that enhance isolation reduces design complexity and as the preliminary results illustrate, such structures may not be entirely necessary especially when used for RF beamforming applications.

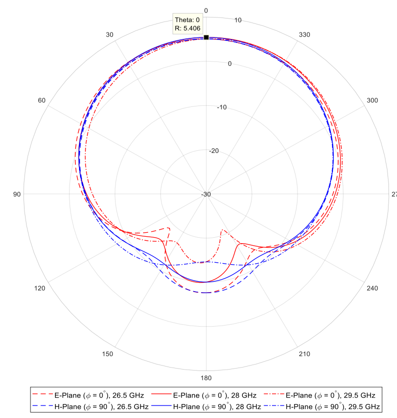
3.3.2 Feed Line

Integration of the vertical feed prior to array layout ensures highest simulation accuracy. Utilizing the 12 mil wide feed stub in conjunction with a 12 mil diameter signal via and 20/30 mil via pad/antipad pairs, a quasicoaxial transition is designed. As outlined in the publication on design considerations for Ka-Band 5G communication applications [21], reviewed in section 2.3, for practical applications three to four ground vias proves sufficient in shielding the transition. Given the fact via to via spacing and interconnecting pad diameters must adhere to PCB fabrication constraints, this design implements four 8 mil diameter ground vias with corresponding 14 mil diameter pads, illustrated in Figure 3.6.

The vertical transition is required to connect the antenna to the RFIC landing pad. A matching network (MN), later discussed, is housed in between to yield 50 Ohm antenna input impedance. However, prior to the MN a 7 mil trace with corresponding 50 Ohm characteristic impedance is used to breakout of the bottom via pad and connect with the MN. A 7 mil trace is utilized as its narrow footprint relaxes PCB edge to edge considerations on the bottom layer and aids in decreased routing density. Figure 3.7 shows the smith chart impedance contour and corresponding antenna radiation pattern, with peak broadside gain 5.41 dB at 28 GHz and efficiency 89%, not accounting for mismatch loss. This implies a



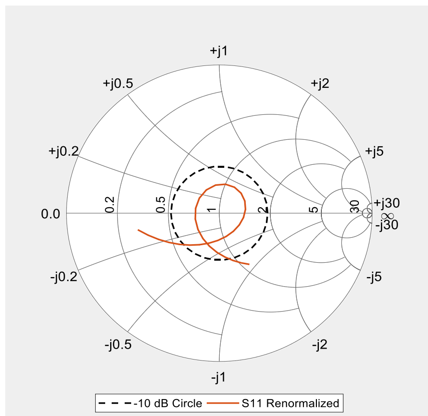
(a) Input impedance prior to MN



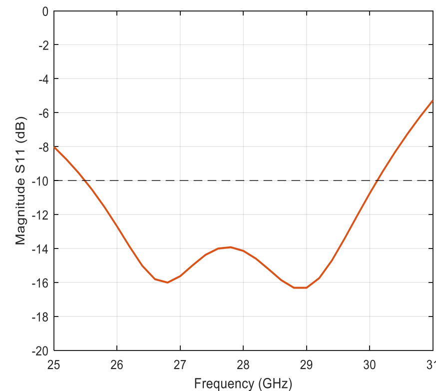
(b) Radiation pattern for 26.5 GHz - 29.5 GHz

Figure 3.7: Antenna input impedance for 25 GHz - 31 GHz and radiation pattern

total loss of 0.5 dB. Pattern stability is excellent in the band of interest, with near 0.35 dB gain variation. Figure 3.8 illustrates the renormalized impedance contour, relative to the center of the loop, and corresponding magnitude plot. A bandwidth of 4.5 GHz prior to any impedance matching is demonstrated.

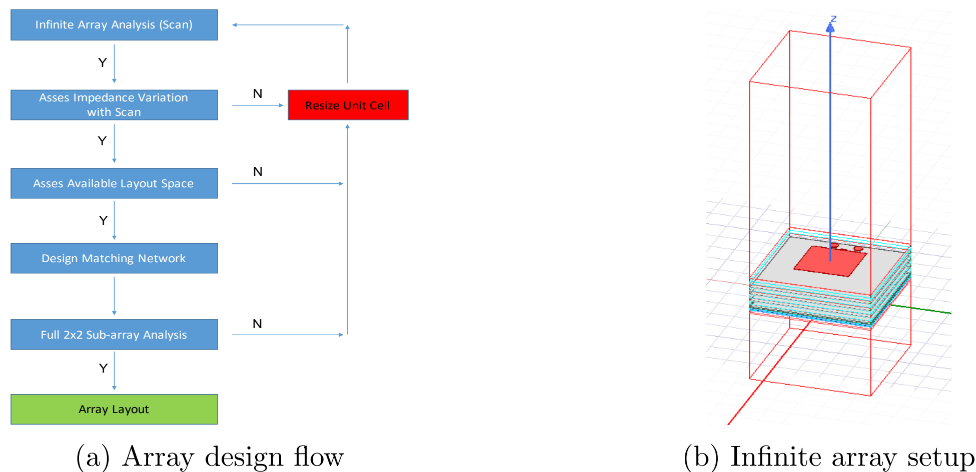


(a) Renormalized input impedance prior to MN



(b) Return loss

Figure 3.8: Renormalized antenna input impedance for 25 GHz - 31 GHz



(a) Array design flow

(b) Infinite array setup

Figure 3.9: Design flow and simulation setup

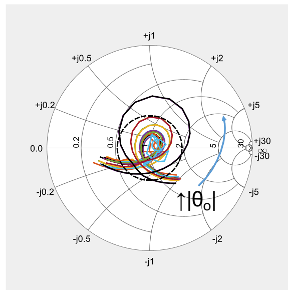
3.4 Planar Array Analysis and Design

To implement the designed antenna element from section 3.3 in a planar array layout that abides by the desired performance specifications, a sequence of analysis steps can be followed which minimize total design time and the potential for numerous revisions. Figure 3.9a outlines the proposed design flow for the planar array design, which leverages the power of infinite array analysis to inspect array performance under scan, prior to layout. Impedance variation with scan angle can be assessed under given active reflection coefficient criteria, in this case -10 dB, and the array unit cell can be resized for conditions not met. If performance is adequate, a quick evaluation of available layout space, considering the inclusion of a MN, low frequency signal routing and RF power combining dictates whether the size of the unit cell is feasible. Upon confirmation, a two port matching network can be designed to transform the center of the antenna input impedance loop to 50 Ohm, seen at the GSG launch point on the AWMF 0158 landing pad. The center of the antenna input impedance loop is chosen to yield approximately equal match across frequency. Finally, full wave analysis can be performed on a 4 element sub-array with inclusion of chip landing pad to confirm layout feasibility and impedance behaviour. If any abnormalities in coupling behaviour exist or radiation performance is not adequate, the design flow can be repeated.

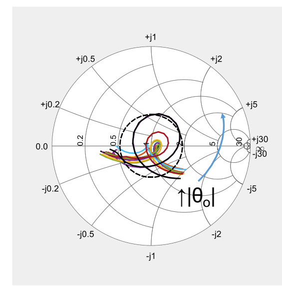
3.4.1 Infinite Array and The Unit Cell

As indicated in section 3.1.3, phased array research outlined in [51, 52] suggests the reduction in array unit cell size for reduced impedance variation with array scan. Thus, beginning with the designed, half wavelength sized full stack model of the proximity coupled patch antenna, master / slave boundary pairs are applied and active reflection coefficient is assessed for various scan angles. Unit cell size is reduced to a minimum of $0.42\lambda_o$ x $0.42\lambda_o$, with vertical feed placement limiting further reduction, and a comparison is made for 25 GHz - 31 GHz (Figure 3.10) which supports both authors findings. Impedance variation with array scan of $\theta_o = +/-45°$ in both E ($\phi_o = 0°$), H ($\phi_o = 90°$) and diagonal (D) planes ($\phi_o = 45°$) exhibits expansion in the smith chart, with the smaller unit cell displaying less variation and confining to the -10 dB ARC circle.

Although simulations indicate a unit cell size of $0.42\lambda_o$ x $0.42\lambda_o$ is sufficient for array implementation, layout feasibility says otherwise. Due to such compactness of the unit cell, the 2x2 sub-array decreases in overall area, however the size of the chip landing pad remains constant, effectively increasing overall bottom layer routing density and introducing potential for PCB constraint violation. Under further inspection, fan-out from the chip landing pad permits low frequency routing along the E plane, subjecting PCB line width and edge to edge constraints primarily along the H plane. As a result, most of the limitation in package real estate exists along the H plane, and an array unit cell size of $0.5\lambda_o$ was the deemed the lower bound. However, to still retain the benefit of reduced lattice size and aid in E Plane scanning, a non-symmetrical unit cell can be utilized. Implemented in this design therefore is a unit cell size $0.42\lambda_o$ x $0.5\lambda_o$ @ 29.5 GHz, with Figure 3.11 showing corresponding dimensions and impedance behaviour, where impedance contours outside the -10 dB circle correspond to $\theta_o = +/-45°$ in the H Plane and reach no larger than -6.3 dB in magnitude.

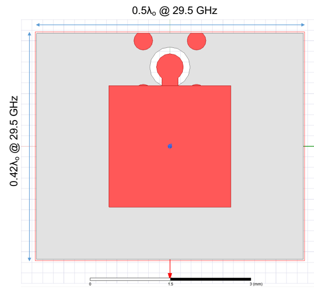


(a) $0.5\lambda_o$ x $0.5\lambda_o$ @ 29.5 GHz

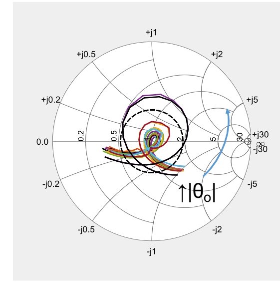


(b) $0.42\lambda_o$ x $0.42\lambda_o$ @ 29.5 GHz

Figure 3.10: Infinite array analysis for $\theta_o = +/-45°$ in E,H and D planes



(a) Model dimensions @ 29.5 GHz

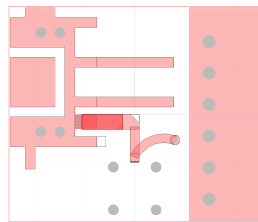


(b) IA analysis with scan for 25 GHz - 31 GHz

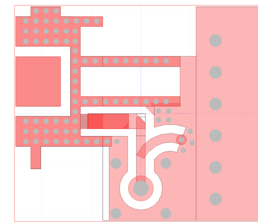
Figure 3.11: Designed $0.42\lambda_o$ x $0.5\lambda_o$ unit cell

3.4.2 Matching Network

A two port, single stub matching network was designed to transform the impedance value at the center of loop located on the smith chart, to 50 Ohm seen at the GSG launch point on the AWMF 0158 landing pad. A short circuit stub is implemented as it requires less length to achieve the desired susceptance for matched condition and further supports bottom layer ground fill for enhanced isolation between microwave components. A simplified model is shown in Figure 3.12a, which outlines both lumped port definitions, noting the usage of a horizontal lumped port to represent chip excitation. The complete model including full stack antenna and associated ground fill, which conforms to PCB edge to edge constraint is presented in Figure 3.12b. Edge to edge distances are kept to 7 mil so as to not disturb the feed line microstrip mode. Final results are outlined in Figure 3.13, displaying a single antenna bandwidth of 3.5 GHz with peak broadside gain of 5.27 dB at 28 GHz, including mismatch loss. Gain variation of near 0.5 dB is exhibited with 4.99 dB and 4.71 dB gain at 26.5 GHz and 29.5 GHz respectively. The design exhibits 85.78% efficiency at the center frequency, corresponding to an overall package loss -0.66 dB.

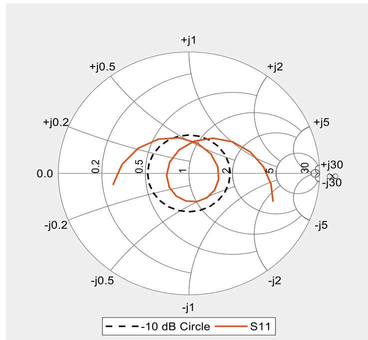


(a) Simplified MN model

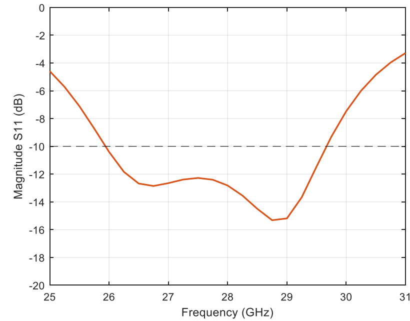


(b) Full model including full stack antenna

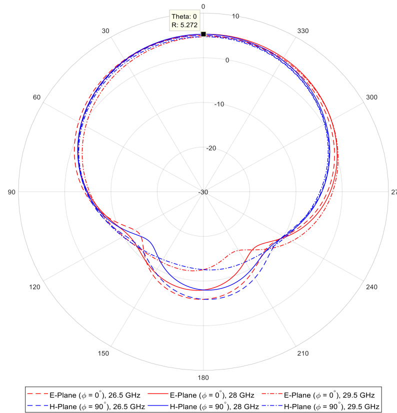
Figure 3.12: Designed bottom layer MN and full stack antenna



(a) Return loss for 25 GHz - 31 GHz



(b) Return Loss

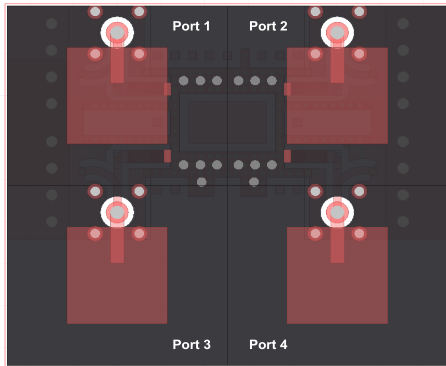


(c) Radiation pattern for 26.5 - 29.5 GHz

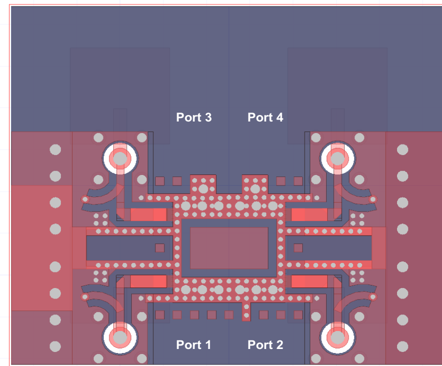
Figure 3.13: Designed full stack proximity coupled patch antenna with MN

3.4.3 2x2 Antenna Sub-Array

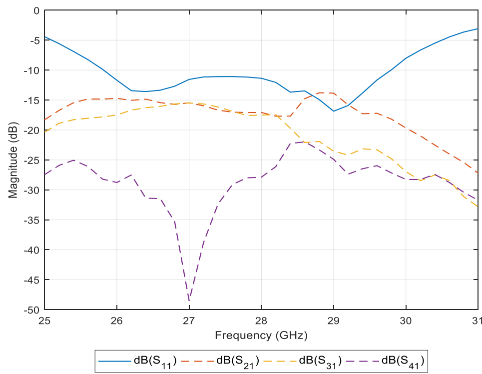
In order to verify the validity of the unit cell analysis and matching network design, HFSS full wave analysis is performed on the 2x2 sub-array, with inclusion of the IC landing pad (Figure 3.14), and corresponding S-parameters and radiation pattern are assessed. With use of Keysight's Advanced Design System (ADS) circuit level simulator, an equal amplitude excitation is be applied to the S-parameter model of the 2x2 sub-array and the resultant active reflection coefficients are determined for each of the four ports. In addition, beam patterns are examined for any significant discrepancies and scan volume is assessed. Broadside gain of 9.46 dB at 28 GHz and 4 GHz bandwidth (not shown) is achieved with Figure 3.15 illustrating the rest of the findings. Due to mutual coupling effects, the antenna element pattern within the 2x2 sub-array exhibits gain of 3.63 dB (Figure 3.14d), resulting



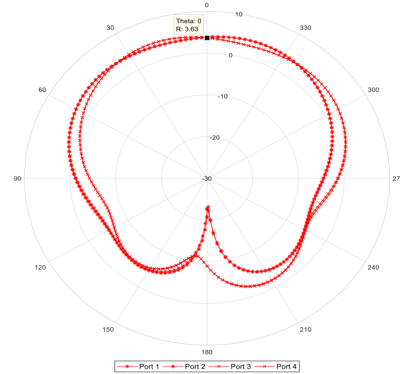
(a) Top view



(b) Bottom view



(c) S-parameters for 2x2 sub-array

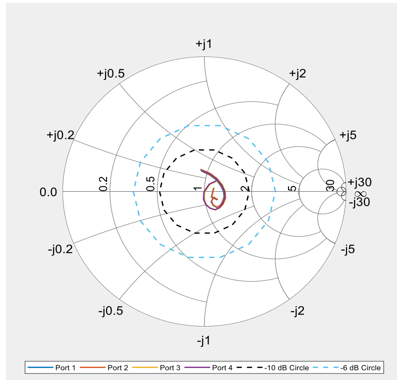


(d) 28 GHz antenna element patterns, E-Plane

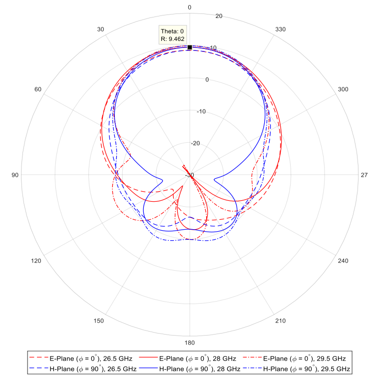
Figure 3.14: 2x2 sub-array full stack HFSS 3D layout model and results

in a lower overall sub-array gain. Variation in the gain is near 1.5 dB with lower edge of the band near 8.50 dB, and upper 9.93 dB. Such variation is a manifestation of the isolation magnitude. Active reflection coefficients are plotted for the bandwidth of interest (26.5 GHz - 29.5 GHz) to easily identify impedance violation of the -10 dB criteria.

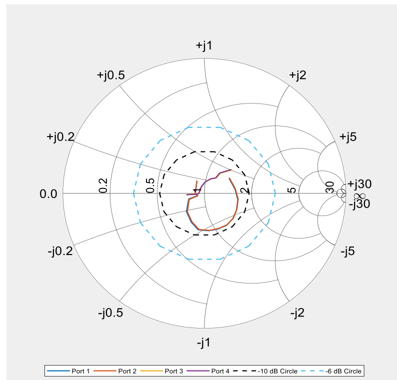
It is evident that the sub-array is limited in scan volume, specifically in the H Plane, as the realized gain slightly decreases. This however can be attributed to the low number of elements and lack of coupling to compensate such impedance variation. An array designed in an infinite setting cannot be expected to scan sufficiently far given no isolation enhancement. As identified in Figure 3.14c, coupling levels range from -17.5 dB at 28 GHz, with slightly greater behaviour at band edge.



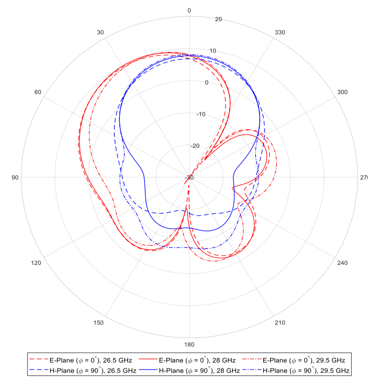
(a) ARC - Broadside



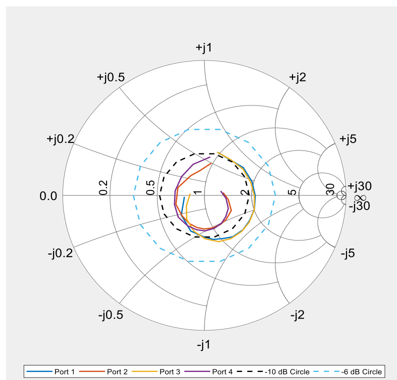
(b) Radiation pattern - Broadside



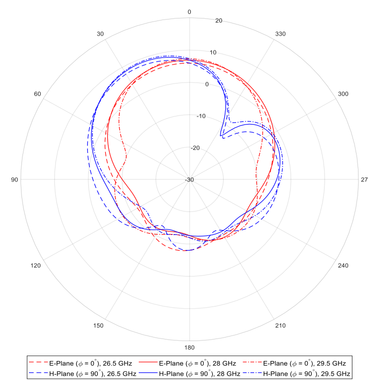
(c) ARC - E Plane ($\theta_0 = 30°$)



(d) Radiation pattern - E Plane ($\theta_0 = 30°$)

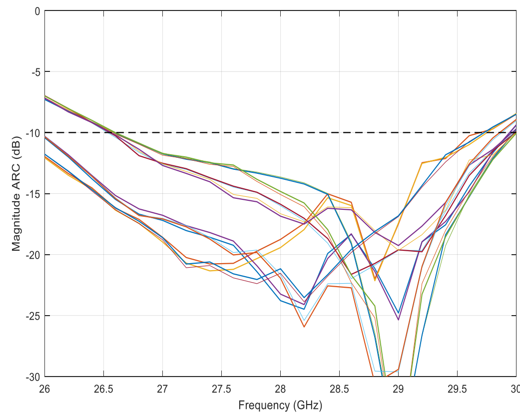


(e) ARC - H Plane ($\theta_0 = 30°$)

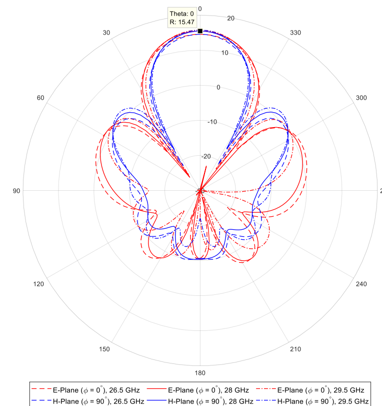


(f) Radiation pattern - H Plane ($\theta_0 = 30°$)

Figure 3.15: 2x2 sub-array HFSS full wave analysis for 26.5 GHz - 29.5 GHz



(a) ARC magnitude for ports 1-16



(b) Broadside Radiation pattern

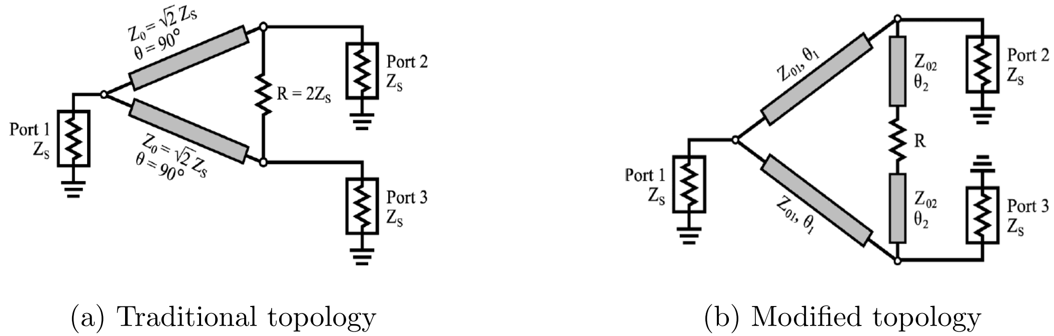
Figure 3.16: 4x4 antenna array HFSS full wave simulation results

3.4.4 4x4 Antenna Array

A similar procedure is followed for the final 4x4 array implementation, as a verification step prior to layout. For brevity, only active reflection coefficient and beam pattern are displayed in Figure 3.16 for broadside main beam, with additional scan performance evaluated later in section 3.6, with inclusion of RF power combiner. The 4x4 array yields a realized gain of 15.47 dB at the center frequency, with corresponding bandwidth 3 GHz. Gain variation across the band is near 1.3 dB with lower and upper frequencies exhibiting 14.56 dB and 15.76 dB respectively. This is approximately 6 dB above the 2x2 sub-array gain, confirming the expected behaviour from increasing array size by factor of 4.

3.5 RF Power Combiner / Splitter

Due to the requirement of off-chip power combining, an RF power combiner must be implemented on the bottom layer of the PCB package. Traditionally, two passive combining options are available; reactive and lossy. To ensure appropriate match in both transmit and receive modes of operation, in addition to exhibiting output port isolation, a lossy combiner is used. A common three port lossy combiner, better known as the wilkinson power combiner (Figure 3.17a), is a passive circuit that utilizes a resistor across its two output transmission line connecting arms to dissipate any reflected power as a consequence of output port mismatch.



(a) Traditional topology

(b) Modified topology

Figure 3.17: Wilkinson power combiner [11]

Wilkinson power combiners are not trivial to design at mmWave frequencies due to the introduction of significant package parasitics associated with placement of the lumped element resistor. Smaller wavelengths introduce potential distributive effects associated with the resistor modelling, in addition to shorter overall transmission line length to achieve wilkinson matched and isolated conditions. Designing for 50 ohm impedance therefore, can cause line length to width ratios to approach unity, reducing routing feasibility, as bends cannot be formed to aid in resistor surface mount device (SMD) placement.

3.5.1 SMD Packaging, Placement and Wilkinson Topology

A variation of the wilkinson power combiner more suited for mmWave implementation was introduced in [11] (Figure 3.17b). It utilizes a high frequency integrated resistor, with resistance value proportional to the area of associated material, which can be modelled via a lumped resistor and a set of transmission lines connected at the output ports. Relationships (3.5), (3.6), (3.7) and (3.8) outline the criteria to enforce both matched and isolated conditions, where r is normalized to the system impedance. Such an implementation introduces resistor value flexibility as the combiner is not restricted to the traditional 2R implementation. This is extremely beneficial to the RF designer as resistors with same package, but different value, may not all yield real valued impedance at mmWave frequencies.

$$z_{01} = z_{02} \tag{3.5}$$

$$r = z_{02}^2 \tag{3.6}$$

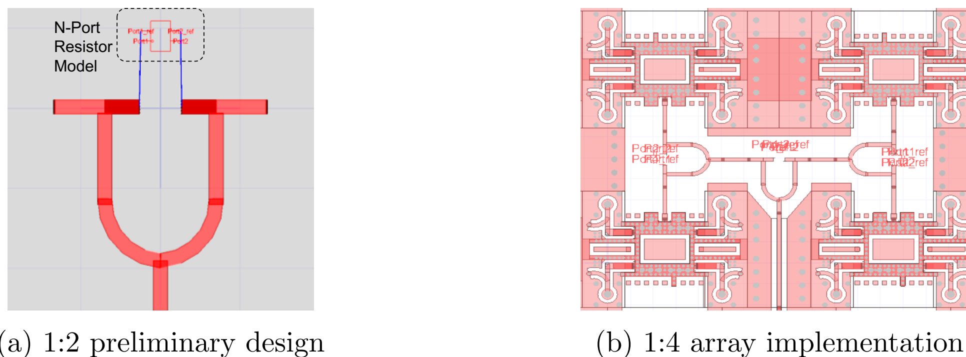
$$\theta_2 = tan^{-1}\left(\sqrt{1-\frac{r}{2}}\right) \tag{3.7}$$

$$\theta_1 = \frac{\pi}{2} + \theta_2 \tag{3.8}$$

3.5.2 Design, Layout Verification and Analysis

Extending this to utilize SMD based resistors, the implementation presented here uses a 50 Ohm Vishay high frequency thin film chip resistor ($r = z_{01} = z_{02} = 1$), in 02016 package, in conjunction with thin 7 mil trace width to yield simultaneous 50 ohm match across all ports, with near -30 dB output port isolation (Figure 3.18a). The form factor is compact and supports array layout as illustrated in Figure 3.18b. For accurate model representation and full wave simulation, HFSS 3D layout incorporates the two port model, provided by Vishay, directly into the simulated structure, reducing the number of port definitions. Simulated response for both the 1:2 preliminary design and 1:4 array implementation with chip landing pad are outlined in Figures 3.19a and 3.19b respectively. Output port isolation meets preliminary specification of $<$ -20 dB, in conjunction with greater than 3 GHz bandwidth and power division -8 dB +/- 0.1 dB across the band of interest.

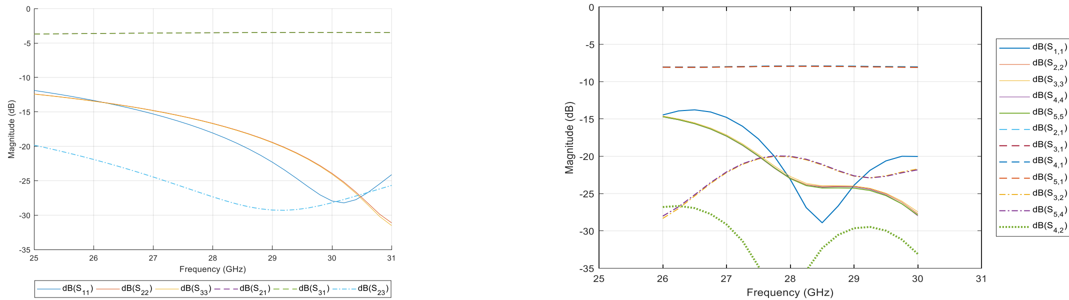
Preliminary specifications emphasized the maximization of isolation between the antenna array and power combiner. This ensures both adequate input match to the combiner,



(a) 1:2 preliminary design

(b) 1:4 array implementation

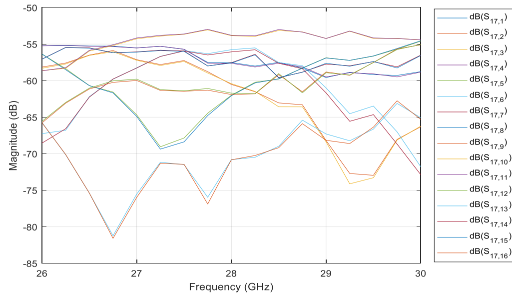
Figure 3.18: Designed wilkinson power combiner and array implementation



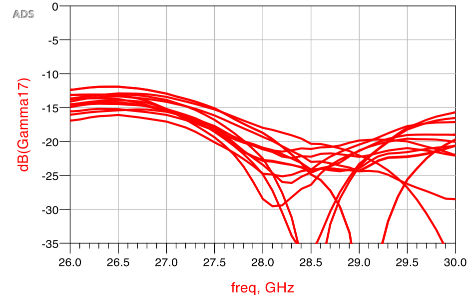
(a) S-parameters for an individual combiner (b) S-parameters for 1:4 array implementation

Figure 3.19: Simulated response of designed wilkinson power combiner

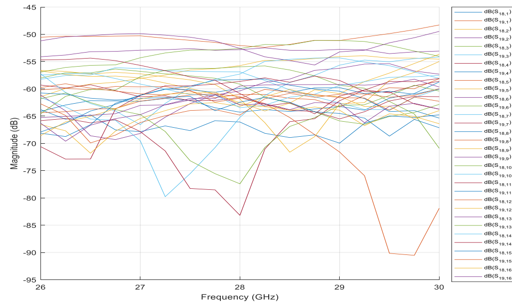
in addition to minimal feedback at the RFIC common input. Utilizing ADS circuit simulator and an extracted 21 port S-parameter model from HFSS, including both the antenna array and 1:4 wilkinson power combiner, input match and power available to each beamformer IC are assessed under various scan conditions. The active reflection coefficient is computed at the input to the array (port 17) and the available power is normalized to the ideal input power, resembling something that of S21 for each RF path. Due to the absence of an S-parameter model for the commercial IC, a simulation test bench is built that compensates for Wilkinson insertion loss of -8 dB and applies appropriate port voltages to represent the 25 dB gain exhibited by the AWMF beamformer IC. The input power to each antenna is set as the OP1dB of the beamformer IC (+15.5 dBm), and all other values are computed using the gain. Figure 3.20 illustrates the findings for main beam direction $\theta_o = +/-45°$ in both E and H planes. Isolation between antennas (ports 1-16) and the wilkinson input (port 17), as well as wilkinson outputs (ports 18-21) are also plotted. It is evident that the level of isolation is sufficient, as it permits minor variation in input match, with slightly larger variation in delivered power (+/- 1.5 dB).



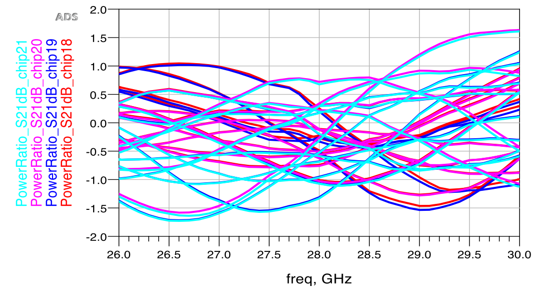
(a) Antenna to Wilkinson Input



(b) Wilkinson input ARC



(c) Antenna to Wilkinson Output



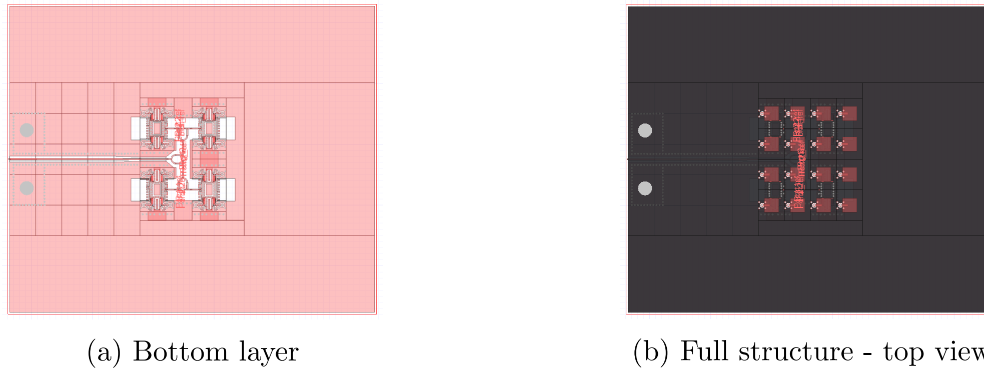
(d) Wilkinson output "S21"

Figure 3.20: Isolation, input ARC and synonymous "S21" for scan $\theta_o = +/-45°$ in E, H

3.6 Phased Array PCB Layout

Package completeness requires the implementation of the entire vertical schematic outlined in the aforementioned text. However, it also requires board level interfacing via connector mounts. As such, the final implementation utilizes a larger footprint to accommodate connector placement (Figure 3.21). Due to significantly large connector footprints, the package is expanded in both X,Y directions with the final implementation being almost square. The overall package dimensions are 59.94 mm x 50.42 mm x 2.03 mm, and the active reflection coefficients with -10/-6 dB circles and corresponding radiation patterns for main beam directions $\theta_o = 0°, 30°, 45°$ in E and H planes are displayed in Figures 3.22, 3.23 and 3.24.

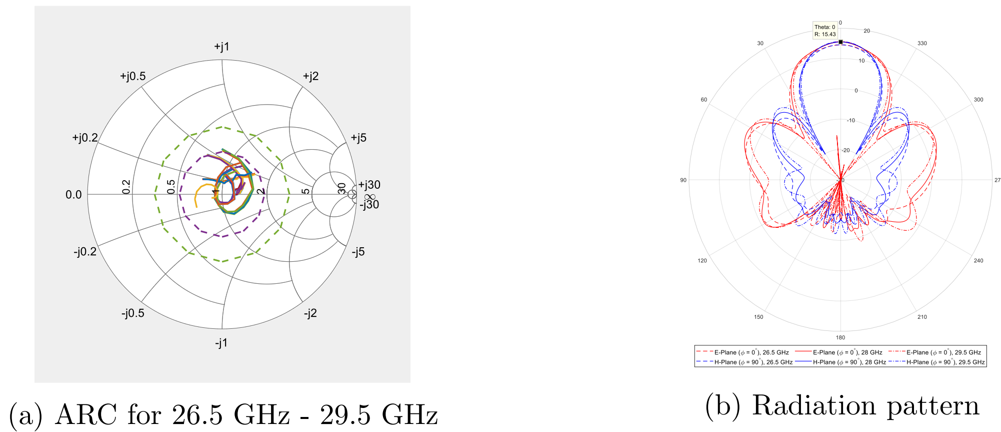
The array exhibits peak broadside gain of 15.43 dB at the center frequency, with 1.1 dB in band variation. Near all elements are confined within the -10 dB ARC circle, in the bandwidth of interest. Scan performance in Figures 3.23 and 3.24 depict the limitations of the small array, with the H plane again experiencing much of the deterioration in the



(a) Bottom layer

(b) Full structure - top view

Figure 3.21: HFSS full package layout



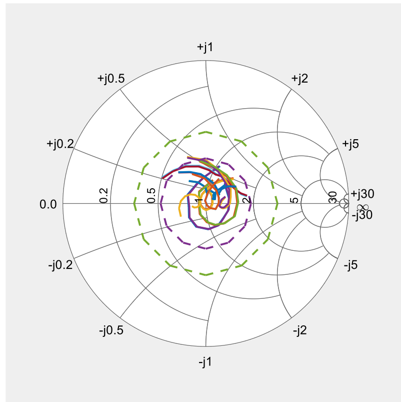
(a) ARC for 26.5 GHz - 29.5 GHz

(b) Radiation pattern

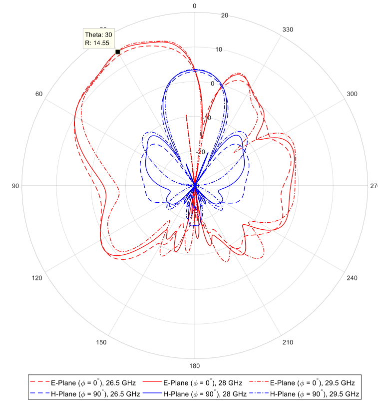
Figure 3.22: Full package layout: Broadside Performance

smith chart. Both 30° E and H plane beams exhibit 14.00 dB to 14.55 dB gain across the bandwidth of interest. Moreover, as the array is scanned further to $\theta_o = 45°$, the E plane beams shows its superiority maintaining higher realized gain, with effects also seen in the smith chart. Almost all elements abide by the -10 dB circle in the E plane, however the H plane nears -6 dB ARC for all elements in the array.

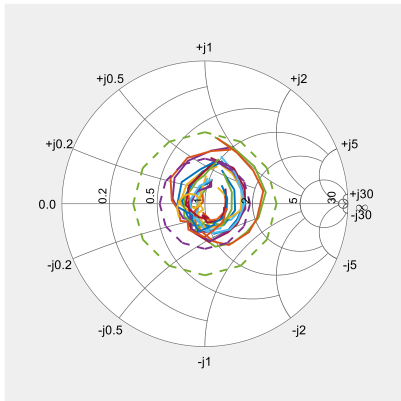
No visible grating lobes are seen in the aforementioned patterns due to the compact lattice structure of the array. However, beam deformation is visible when compared to the 4x4 array verification results (Figure 3.16b, with the E plane exhibiting most of the discrepancy. Such a result is attributed to the expansion of the array footprint for layout requirements. A larger ground plane, especially in the E plane which exhibits the smallest unit cell dimension, contributes to beam widening and results in dips in the pattern at



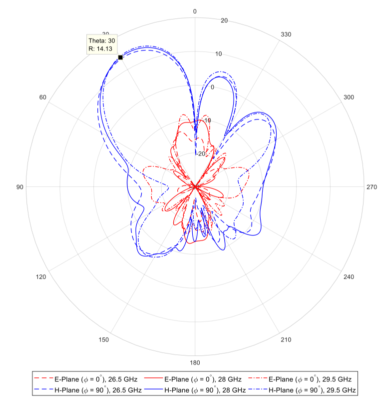
(a) ARC for 26.5 GHz - 29.5 GHz



(b) Radiation pattern



(c) ARC for 26.5 GHz - 29.5 GHz



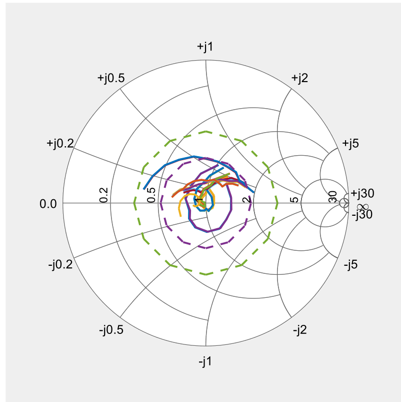
(d) Radiation pattern

Figure 3.23: Full package layout: $\theta_o = +30°$, E and H Performance

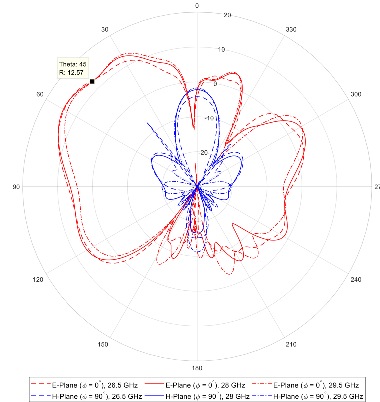
extreme scan angles. Figure 3.25 shows the same E plane scan to +45°, for both the sole 4x4 array and full package layout, where discrepancies are clearly identified.

3.6.1 Board Level I/O

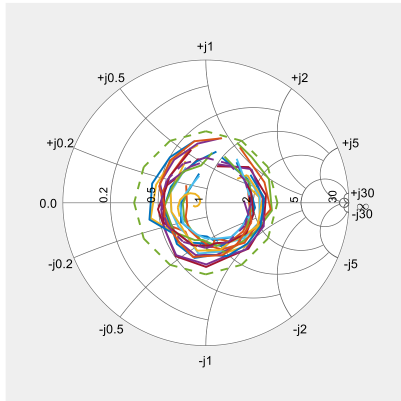
To aid in low frequency routing and SMD placement, Altium designer is used in conjunction with HFSS 3D layout to combine both traditional PCB and RF layout functionality. Illustrated in Figure 3.26a is the PCB layout with patch, feed stub, bottom layer and overlay visible. In order to interface with the AiP, I/O connections were defined on the



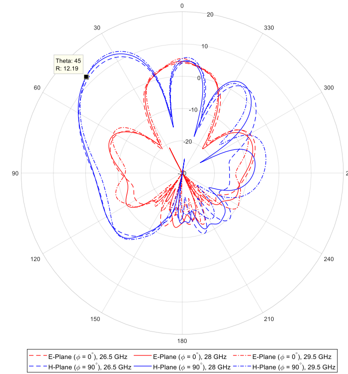
(a) ARC for 26.5 GHz - 29.5 GHz



(b) Radiation pattern



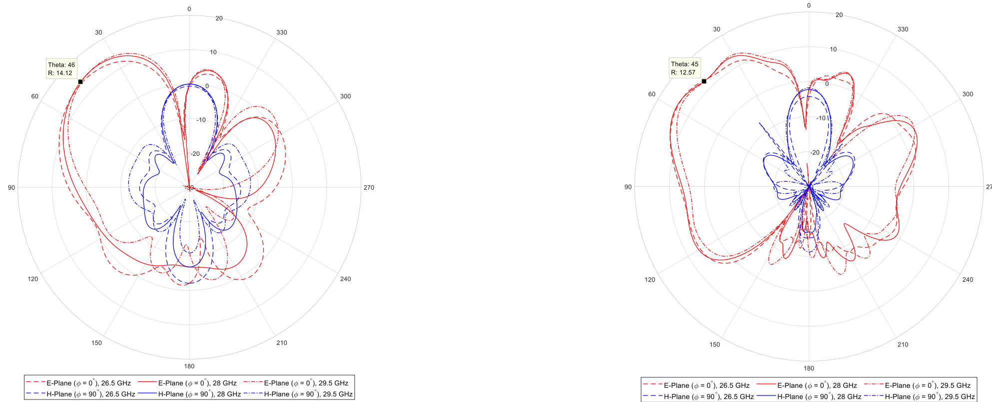
(c) ARC for 26.5 GHz - 29.5 GHz



(d) Radiation pattern

Figure 3.24: Full package layout: $\theta_o = +45°$, E and H Performance

perimeter of the array backside, maintaining adequate distance from all beamformer ICs 3.26b. Two low frequency connectors; one Harwin 8 pin 2.54 mm pitch header and one Samtec 24 pin FLE female socket are located on the short side, adjacent to one another and opposite to the RF input. The header supplies both +1.8 and +2.5 volts, via 2 pins each, with 4 ground pins, to minimize resistive loss and maximize design reliability. The female socket is responsible for relaying all low frequency control signals to an off-package National Instruments (NI) controller. Supplying the modulated RF signal to the array power combining network is a Southwest Microwave 1092-04A-5, 2.92 mm 40 GHz edge mount connector. A corresponding grounded co-planar waveguide (G-CPW) was designed in HFSS 3D layout and is utilized in the connector transition to the package.



(a) Array footprint - E Plane, $\theta_o = +45°$ (b) Full package footprint - E Plane, $\theta_o = +45°$

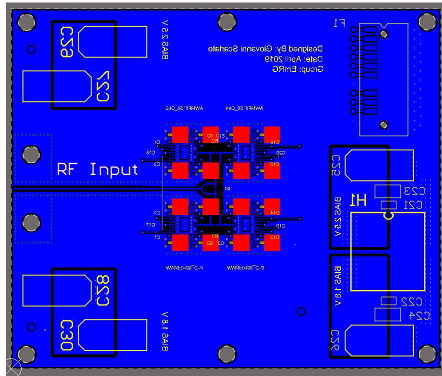
Figure 3.25: Radiation pattern deformation: Array vs full package

3.6.2 SMD Component Placement

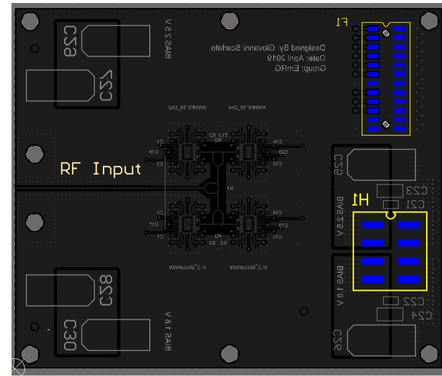
Given the large degree of SMDs included on the bottom layer of the AiP, of most importance are the power amplifier bias decoupling capacitors nearest the beamformer ICs. To minimize the potential for circuit non-idealities, which may result in significant calibration efforts, the capacitors are symmetrically placed to ensure all power amplifiers are subjected to similar bias behaviour at the package level. Line lengths are kept short as bias lines can operate as transmission lines at higher frequencies, introducing potential in band coupling mechanisms, which are to be avoided. Figure 3.27 illustrates decoupling capacitor placement and corresponding fan-out for a single AWMF 0158 RFIC.

3.6.3 Solder Mask Definition

Due to the AWMF 0158 utilizing a wafer level chip scale package, flip chip mounting requires specific solder mask definitions to ensure reliable assembly. Shown in figure 3.28 is the solder mask layer (negative) for a single AWMF 0158 beamformer. Openings of 10.5 mil diameter ensure proper attachment due to surrounding solder dams confinement of flow, effectively minimizing potential for displacement or pin-to-pin shorting. For increased assembly yield, PCB manufacturing requires precise solder mask registration in order not to impede chip solderability. Additional solder mask considerations are given to all RF structures, where all solder mask is removed in an effort to maximize performance and overall correlation with simulation.



(a) PCB layout view



(b) Package I/O connections

Figure 3.26: Designed 28 GHz RF beamforming 4x4 AiP

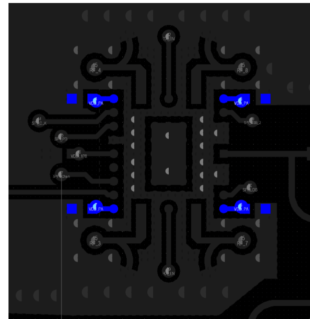


Figure 3.27: Power amplifier decoupling capacitor placement

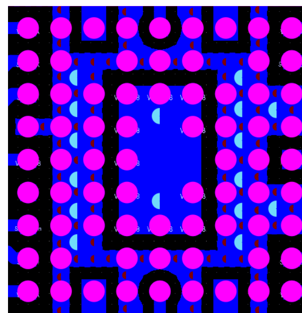


Figure 3.28: AWMF 0158 bottom solder mask definition

Chapter 4

Antenna-in-Package Design as a Transmitter Observation Receiver

Motivation to move to higher frequencies ensures increased data rate via improved spectral efficiency due to beamforming capabilties. However, as outlined in Section 2.3, device technology limitations permits extreme conditions for power amplifier operation. Due to relatively low unity gain frequency in current technologies, operation in the mmWave bands sees reduced amplifier gain and as a result, leverages the power of over the air combining. This is an excellent means of compensation, but nevertheless, not adequate in terms of overall system efficiency. Systems require high efficiency front end modules that ultimately do not compromise overall linearity.

In order to maximize efficiency, power amplifiers generally operate near their respective saturation region, or maximum output power. Yet near maximum output power, characteristics of the amplifier become extremely non-linear, introducing spectral regrowth when under modulated signal stimulus (Figure 4.1). Such behaviour is intolerable in today's communication standards and can be detrimental for users in adjacent channels. Fortunately, a technique known as Digital Predistorition (DPD) has been developed in decades previous to alleviate this phenomena. With the use of a transmission observation receiver (TOR) for output capture, a sample of the power amplifiers output signal, $y(t)$, is utilized to build a non-linear model. Its inverse is applied prior to the corresponding PA input, which therefore compensates the non-linear behaviour (f) an input signal $x(t)$ would exhibit, permitting amplification at traditionally non-linear regimes, ultimately aiding in the preservation of system efficiency.

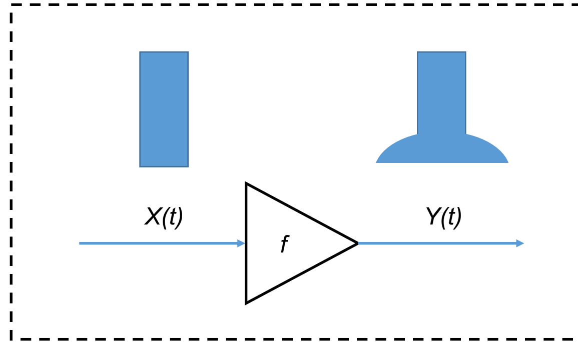


Figure 4.1: Spectral regrowth due to power amplifier non-linearity

4.1 Traditional TOR Architectural Limitations

Conventional DPD schemes make use of circuit level techniques to capture the samples required for appropriate PA modelling. Traditional TOR implementations therefore utilizes passive coupling techniques (directional, hybrid) to sample a fraction of the PA output, without interrupting output match characteristics. For single path systems, the output of one power amplifier is monitored and samples can be easily captured for DPD coefficient computation. The same is said for sub-6 GHz MIMO systems, employing a single coupler per transmit chain. However, this becomes increasingly impractical for the shift to mmWave frequencies, as systems that harness the capabilities of massive MIMO are projected to utilize a minimum number of 64 RF front ends.

In addition, system compactness and package integration of both the RFICs and antenna array eliminates any possibility of coupler implementation. As outlined in the previous section on antenna element design (Section 3.3), feed line length must be minimized to ensure maximum efficiency, where the ideal implementation was found to utilize a direct vertical via transition to the antenna layer. Remaining space permits implementation of the associate matching network, however traditional passive microwave devices like the directional coupler require significantly greater package real estate. This motivates the need for package level innovation to further the capabilities of mmWave phased array systems.

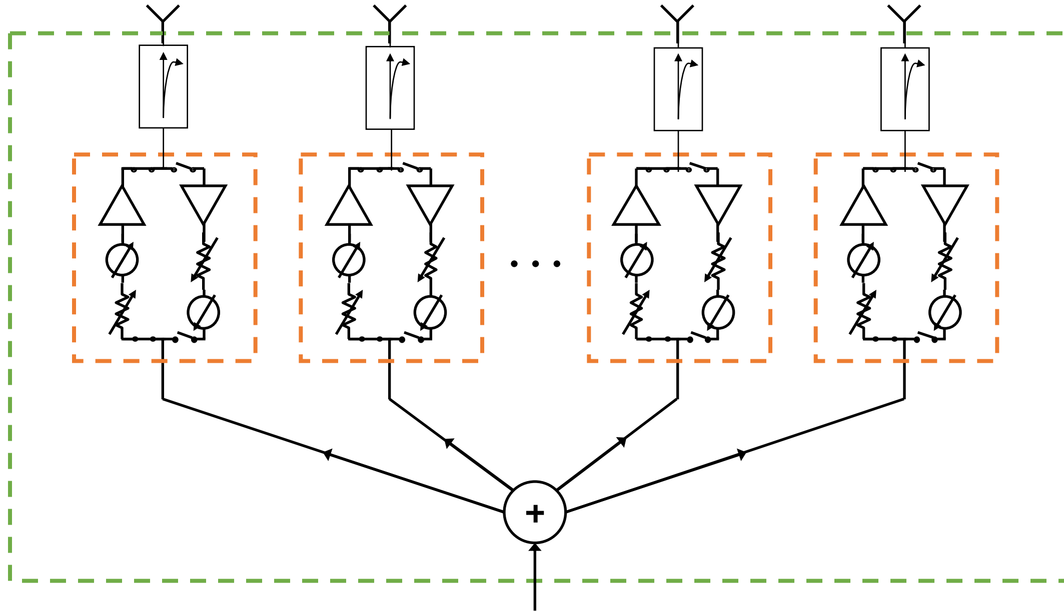


Figure 4.2: Impractical TOR implementation for mmWave massive MIMO systems

4.2 Proposed Architecture

Developing a TOR architecture which leverages the compactness of the package, as opposed to furthering package density, is the preferred route at mmWave and presents itself as a significant challenge. The implementation must still capture a portion of the output signal from all PAs, however it does not have to restrict observations to each individual PA. Coupled signals must capture general array behaviour, especially in RF beamforming applications where each PA amplifies an amplitude and phase weighted version of the same signal. This must all be accomplished without imposing an detrimental effects on radiation performance of the array as this would not be representative of in-field performance.

Such implementation considerations therefore lead to the usage of the package perimeter as an efficient and effective means of TOR implementation. As identified in many past mmWave package publications reviewed in section 2.3, dummy elements are commonly utilized to improve element pattern uniformity which aids in overall scan performance, without introducing new side lobe impairments from decreased array fill factor. As a result, dummy element introduction can be seen as entirely positive with regards to radiation performance, with the exception being board level scalability. Given the array is of sufficient size and scalability is not of concern, dummy element implementation can be har-

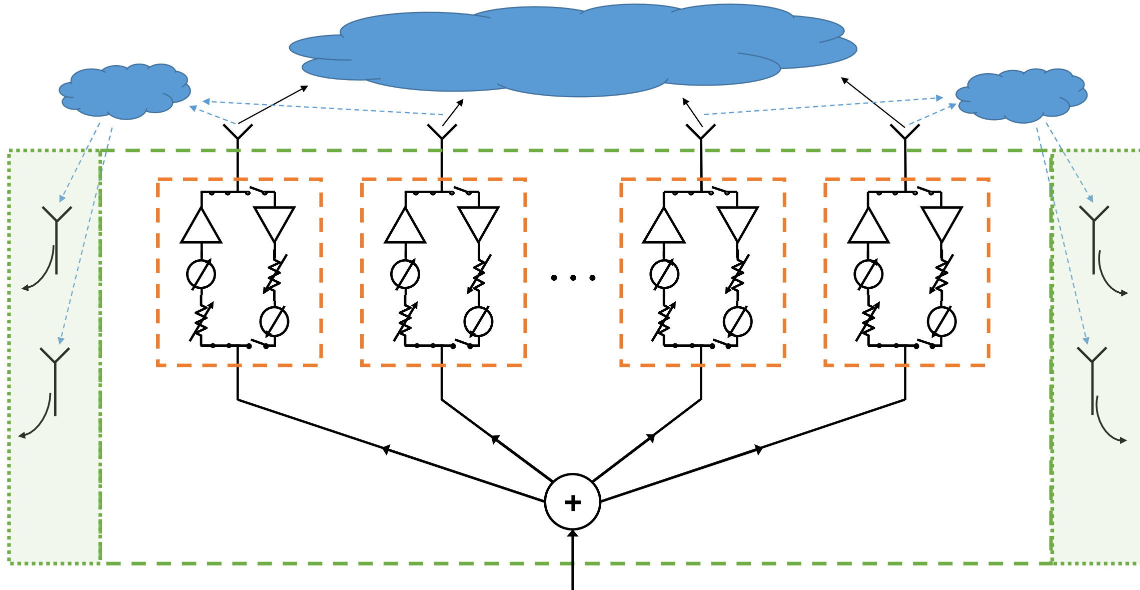


Figure 4.3: Proposed TOR implementation for mmWave massive MIMO systems

nessed to leverage finite element-to-element isolation to constructively capture overall PA behaviour along several points on the array perimeter. Figure 4.3 illustrates the proposed block level architecture.

4.3 TOR Integrated Antenna-in-Package

Utilizing the designed antenna-in-package from the previous section, an arrangement of elements were placed along the perimeter of the 4x4 array (Figure 4.4), where board level interfacing and SMD placement limited the total probe fill factor (PFF). In a 4x4 array arrangement, a total of 20 elements can be used to surround the array. Implemented in this design are eight elements, with two placed at each side center, resulting in a probe fill factor of PFF = 8/20 = 0.4, or 40%. Figure 4.5 shows the probe placement, with connector footprint outlined in yellow. Amphenol high frequency SMPM connectors are used to interface with the probing antennas and exhibit relatively good response at mmWave frequencies, limiting potential mismatch and re-radiation.

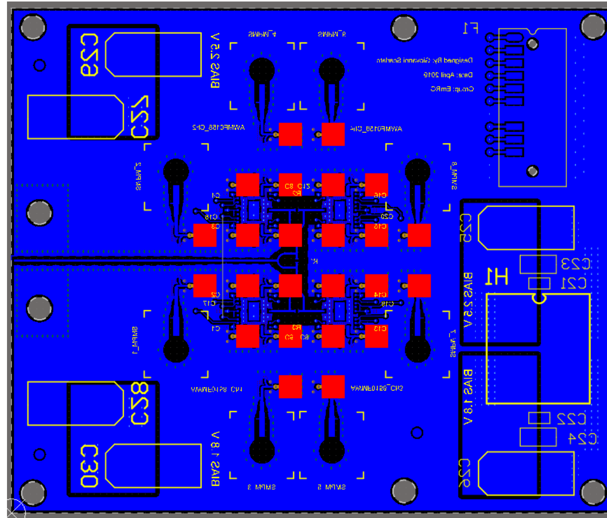


Figure 4.4: PCB layout view

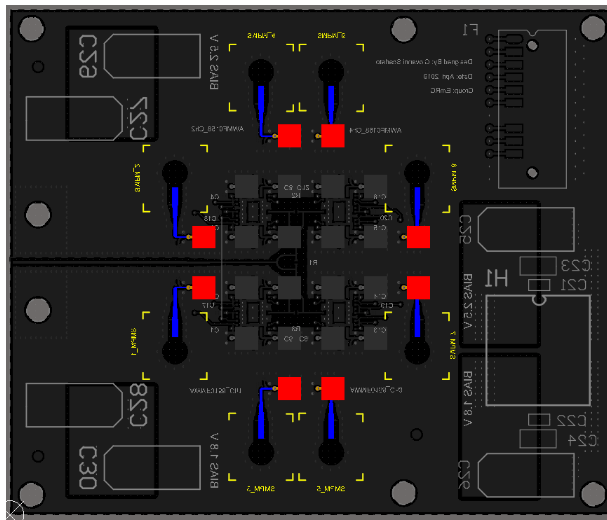


Figure 4.5: TOR probing antenna arrangement

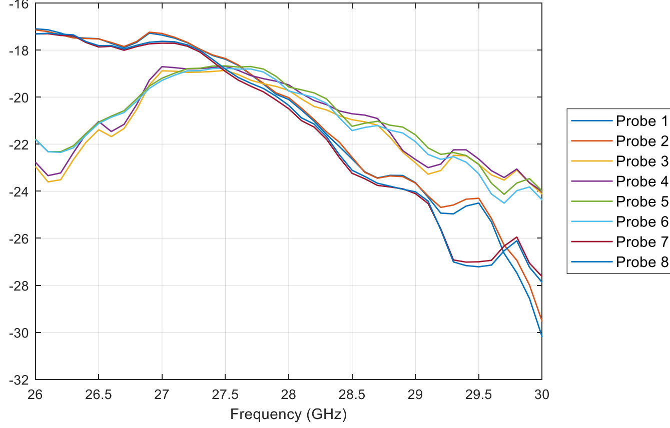
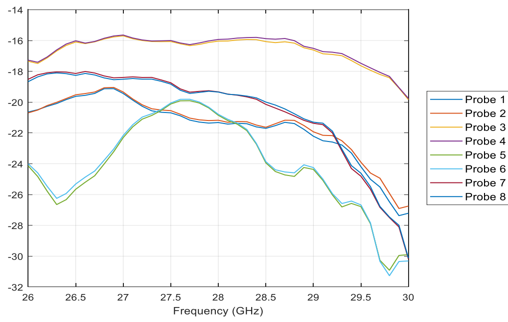


Figure 4.6: Normalized probe frequency response with array main beam pointed broadside

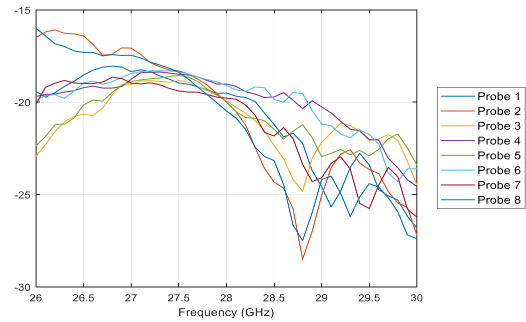
4.3.1 Coupling Characteristics

At the core of the TOR functionality is the antenna-to-probe coupling behaviour. With an extracted S-parameter model from HFSS 3D Layout full wave simulation, the normalized overall frequency response (H_i) of the ith probe can be evaluated using relation (4.1), where ϕ_j is the phase weighting of the jth antenna to yield main beam direction (ϕ_o, θ_o) and N is the total number of radiating elements in the array. Due to the phasor relationship exhibited, channel response varies with main beam direction. To yield optimal coupling behaviour, channel response should be flat, with minimal variation in the bandwidth of interest. As depicted in Figures 4.6 and 4.7, not all probing antennas exhibit maximally flat characteristics. However, given a main beam direction, E and H planes exhibit elements of symmetry, and as a result select probe antennas share similar characteristics with flat frequency response across 26.5 GHz - 29.5 GHz. Given a main beam direction therefore, DPD can exploit different probing elements within the TOR to ensure accurate output signal capture.

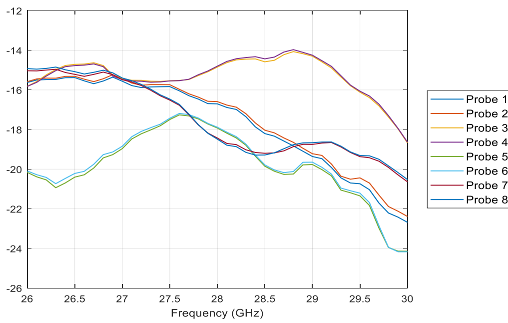
$$H_i = \sum_{j=1}^{N} S_{ij} e^{j\phi_j} \tag{4.1}$$



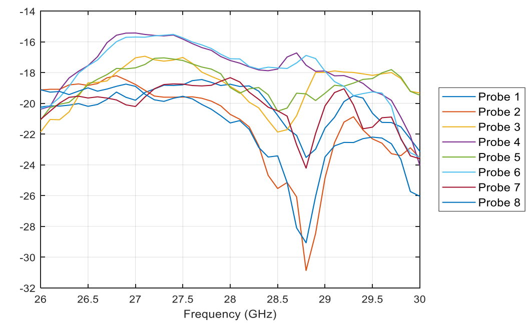
(a) E Plane - $\theta_o = 15°$



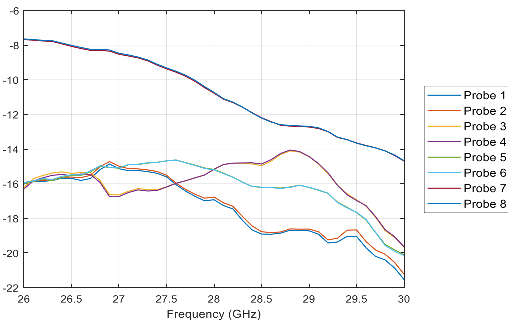
(b) H Plane - $\theta_o = 15°$



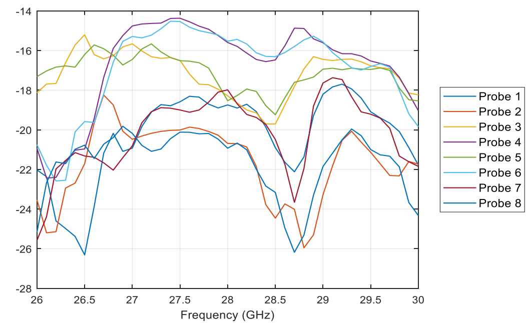
(c) E Plane - $\theta_o = 30°$



(d) H Plane - $\theta_o = 30°$



(e) E Plane - $\theta_o = 45°$



(f) H Plane - $\theta_o = 45°$

Figure 4.7: Normalized probe frequency response for $\theta_o = 15°, 30°, 45°$ in E and H planes

Chapter 5

Test Fixture Measurements and Simulation Validation

In order to gauge the suitability for assembly of both the AiP and TOR variant, several test fixtures were designed and included on the fabricated panel. The test fixtures included both the radiating element in various configurations along with the RF power combiner. SMPM 40 GHz connectors were used to interface with the antenna test structures, while the Southwest Microwave 1092-04A-5, 2.92 mm 40 GHz edge mount connector was used for the wilkinson.

Due to the additional SMPM to 2.92 mm conversion cable, the measurement plane could not be placed at the input of the SMPM connector. As a result, a through, reflect line (TRL) calibration kit was designed to de-embed the effect of the SMPM connect and conversion cable, moving the measurement plane after the connector and onto the device under test. The TRL calibration through, reflect and line standards are illustrated in figure 5.1. The reference plane sits at the center of the through standard, effectively de-embedding all that precedes. The line standard utilizes an extra quarter wavelength line at 28 GHz, with corresponding phase delay of roughly 10 ps. All standards are implemented on a Keysight PNA-X microwave network analyzer, which computes the necessary error terms allowing for TRL calibration directly on bench. Two and four port calibrations are performed, with the three port power combiner using Keysight's E-cal apparatus, not TRL calibration.

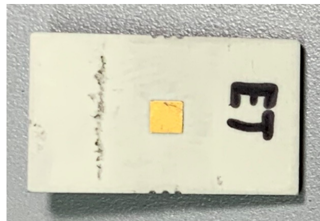
Because the test fixtures are assembled by hand via solder stencil and hot plate, the calibration standards do not exhibit precise similarities. For instance, connector placement from standard to standard varies, and this can introduce shifts in the reference plane.

Figure 5.1: Designed TRL calibration kit

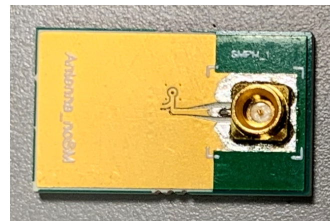
In addition, the amount of solder utilized changes the corresponding pin diameter and resultant performance. This effectively can result in unequal return loss for the standards, yielding slight differences in performance between ports.

5.1 Single Antenna Element

A single antenna element was fabricated using the 12-Layer stackup, with overall footprint much larger than the designed unit cell size described in chapters previous (Figure 5.2). This is due to connector requirement, where the connector exhibits similar size to that of the antenna. The antenna element shares the same parameters as that of the antenna element implemented within the array, with the exception of overall size.



(a) Top view



(b) Bottom view

Figure 5.2: Test fixture: single antenna element

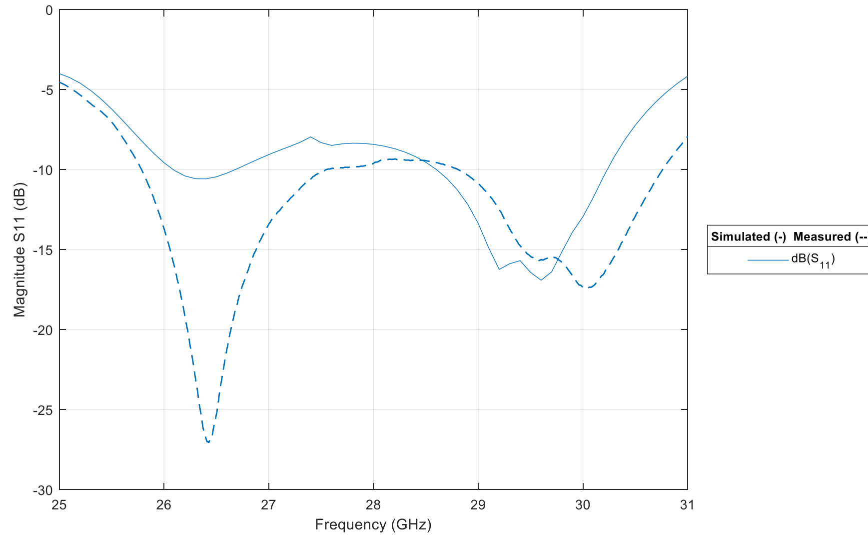
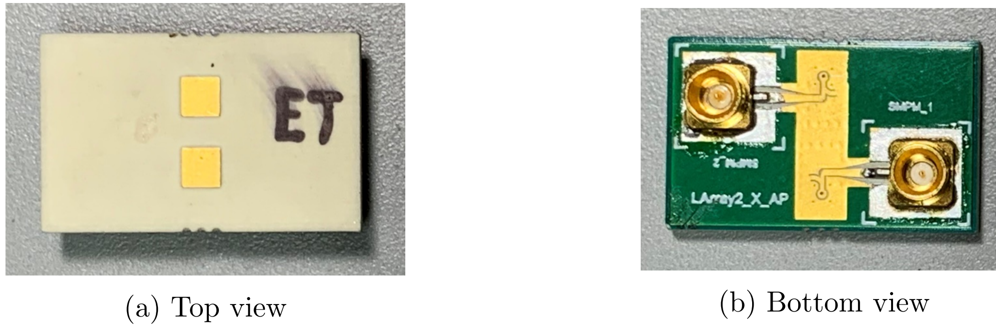


Figure 5.3: Antenna element simulation comparison to measurement after TRL calibration

The measured response is outlined in Figure 5.3 and is compared to the simulated performance. Both measurement and simulation are compared at the same reference plane. The antenna test fixture exhibits excellent correlation to measurement, with observed resonance near 26.5 GHz and 29.5 GHz. A slight frequency shift is present, however as outlined earlier, this can be attributed to numerous items. Connector placement of the device under test can differ from that of the TRL standards, introducing shifts in the reference plane. In addition, the soldered connection may be different than that of the standards, introducing additional error not captured in the performed calibration. When considering potential variations in the test fixture itself, surface roughness can translate to alterations in the effective permittivity. Finally, manufacturing tolerance is equally probable.

5.2 Two Element Array

A two element array was designed, using the aforementioned antenna element, with arrangement along the E Plane. Elements were placed in an anti-phase configuration to aid in connector placement. Figure 5.4 depicts the designed test fixture. Solder mask is kept off areas with transmission line to minimize potential discrepancy between simulation and measurement.



(a) Top view

(b) Bottom view

Figure 5.4: Test fixture: two element array

Simulated and measured results are displayed in Figure 5.5, with corresponding reference plane at the middle of the through standard. Results are displayed for a single element in the array due to the structural symmetry. Excellent correlation between simulation and measurement is observed with resonance in the return loss corresponding to that of simulation. Isolation shows significant similarities with pronounced resonance near 29.7 GHz. The slight shift in the isolation response suggests potential fabrication non-idealities, however the correlation in return loss, and variation from that of the single element results suggests minor discrepancies between the connector transition on the device under test and that of the calibration standards.

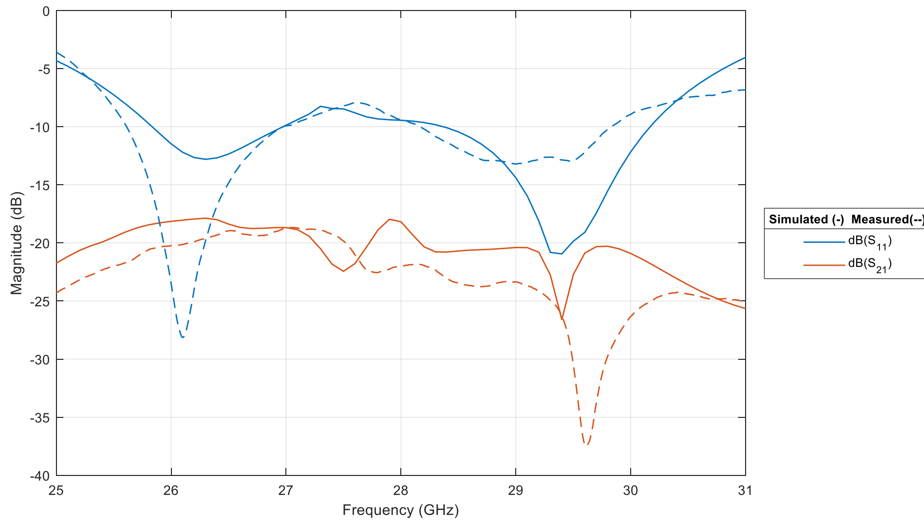
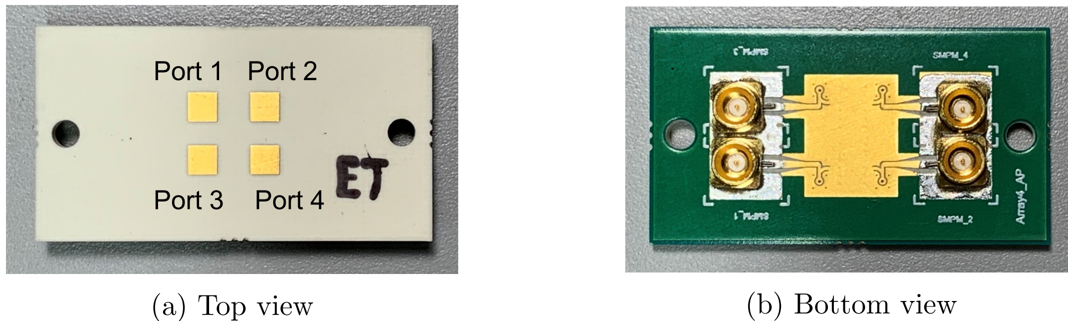


Figure 5.5: Two element simulation comparison to measurement after TRL calibration



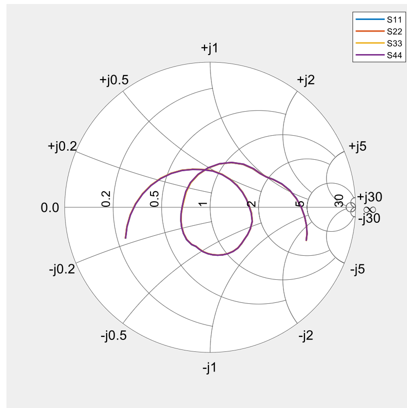
(a) Top view (b) Bottom view

Figure 5.6: Test fixture: four element array

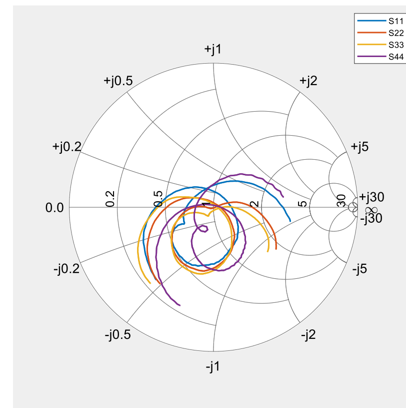
5.3 Four Element Array

A four element array was also designed using the aforementioned antenna element, with a 2x2 arrangement. Elements again were placed in an anti-phase configuration to aid in connector placement and structure symmetry. Figure 5.6 depicts the designed 2x2 antenna array test fixture.

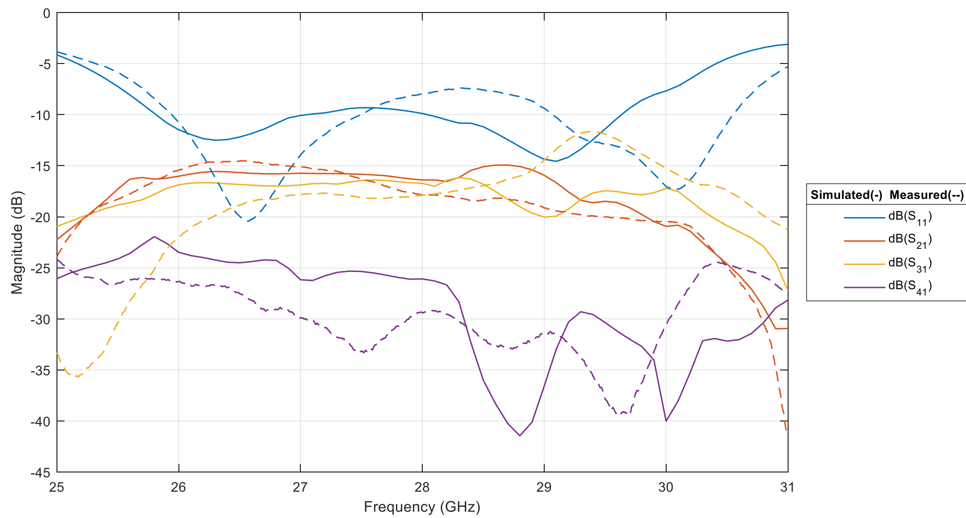
Simulated and measured results in smith chart format are displayed in Figures 5.7a and 5.7b, with a magnitude plot only shown for a single element due to structural symmetry (Figure 5.7c). The corresponding reference plane is again set at the middle of the through standard for both simulation and measurement. Return loss impedance contours in the smith chart share the same loop behaviour, albeit with a slight shift south west. As outlined earlier, port to port behaviour varies as many mechanisms of error are introduced via test fixture hand assembly. Outlined in the magnitude plot, a 500 MHz frequency shift is observed with upward shift in resonance, while notable increased coupling behaviour is exhibited in the E Plane near 29.4 GHz for antennas 1 and 3, as well as 2 and 4 (not shown). Such an abnormality can be attributed to the potential discrepancy in connector placement, specifically with this device under test. Due to the solder mask opening being sufficiently large, in addition to connector placement considerably close to one another, during the assembly stage the hot plate resulted in connectors fusing together for ports 1,3 and 2,4. This could have the potential to influence ground currents ultimately exposing an alternative coupling path. Altogether, despite the slight non-idealities, measurements exhibit direct correlation with simulation, providing validity in the simulation methodology. Further radiation pattern measurements are necessary to fully validate the PCB test fixture design however, a broadband mmWave antenna standard was not available at the time of measurement to facilitate such tests.



(a) Simulated Return Loss

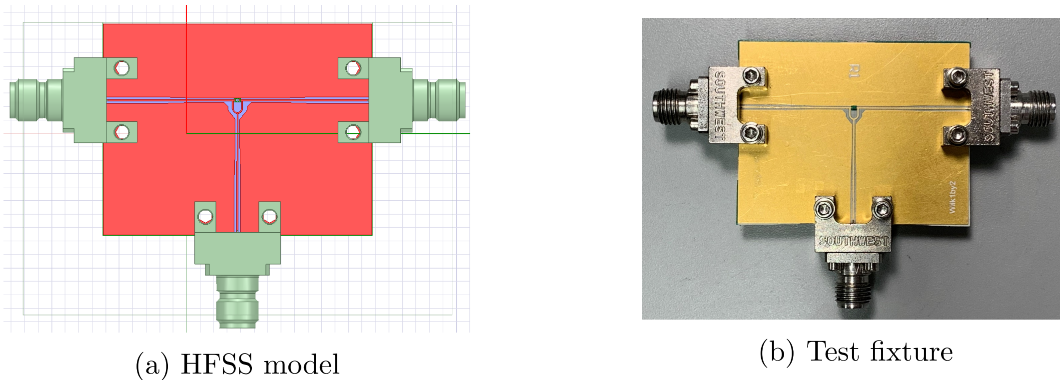


(b) Measured Return Loss after TRL calibration



(c) Measured S-parameters after TRL calibration

Figure 5.7: 2x2 array simulation vs measurement after TRL calibration, for 25 - 31 GHz



(a) HFSS model

(b) Test fixture

Figure 5.8: Test fixture: 1:2 wilkinson power combiner

5.4 RF 1:2 Power Combiner

With the ability to incorporate the Southwest Microwave 1092-04A-5, 2.92 mm connector in simulation, the reference plane could be placed at the boundary of the RF power combiner (Figure 5.8). By utilizing the E-cal standard apparatus provided by Keysight, calibration errors were mitigated as a result of not having to use user defined calibration kits. Accurate calibration could therefore be performed in order to eliminate the effect of connecting 2.92 mm cables.

The measured results in Figure 5.9 suggest some notable discrepancies with simulation. Insertion loss nears -6 dB and correlates well with simulation. Isolation retains the same shape in magnitude, however the measured isolation is worse by a factor of 7 dB at the center frequency. When inspecting the return loss, the input port exhibits significant differences with resonance near 26 GHz and 30 GHz, while the output ports exhibit resonance shift. Such behaviour suggests a variety of things. Proving detrimental to the isolation could be incorrect installation of the surface mount thin film resistor. Error introduced via hand assembly of 5 mm packaged resistor is extremely likely and basic DC tests cannot be conducted due to the power combiner presenting a short circuit at 0 Hz. In addition, discrepancies could arise from different resistor package parasitics, as the substrate the Vishay resistor was measured on to extract its associated N-port model is likely to be different than that of the Rogers RO 4350B 4 mil core implemented in this design. Finally, Southwest connector edge mounting proves problematic as metal pull back and air gap at the edge significantly degrade impedance match. The test fixture edge was shaved down and a basic through transmission line test suggested 5 mil gap in simulation best represented the test fixture.

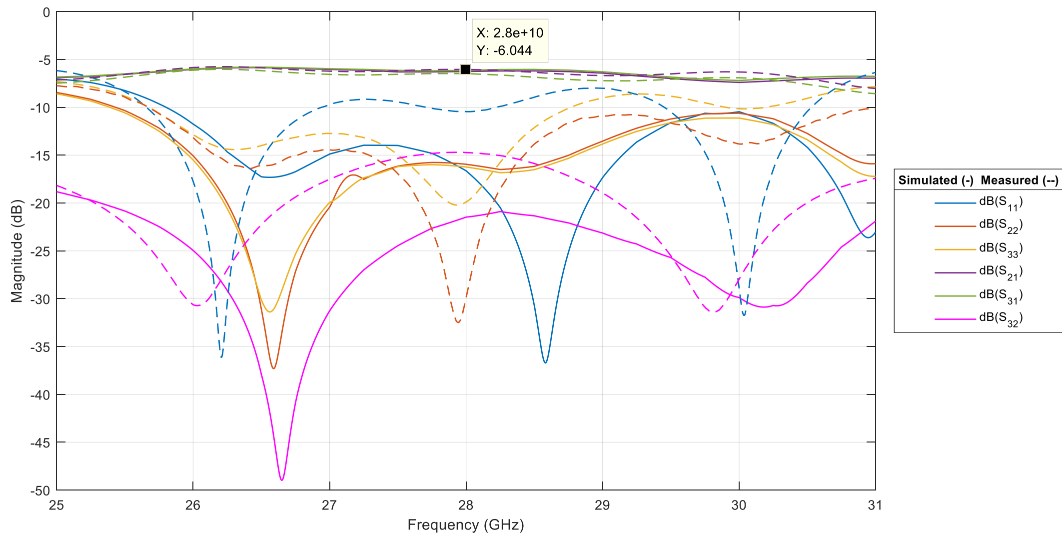


Figure 5.9: Wilkinson simulation comparison to measurement

Chapter 6

Conclusion

The motivation behind the need for mmWave phased array systems was brought forth by the benefits obtained from line of sight links. Due to the crowded beach front spectrum and demand for fast data rates, communications are utilizing mmWave bands to contribute to larger available bandwidth with further improvements in spectral efficiency via incorporation of massive MIMO technologies. At the core, phased array systems offer channel capacity enhancement via larger array gain and complimenting beamforming techniques. Extensive work over the past decade has been conducted in technological implementations for V, W and Ka-Bands. Competing package methodologies outlined the benefits and disadvantages of various implementation schemes and their respective applicability to a certain frequency range. Much of the Ka-Band implementations carry over innovative techniques first established at V-Band, for 60 GHz commercial in door communications and are currently being refined to yield the most versatile solution.

Deemed most important were factors such as cost, design complexity, material availability and system performance such as scan range and bandwidth, when determining the traits most collectively neglected. This work therefore presented an attempt at resolving the aforementioned issues, bringing together a balanced system that can perform even under the stringent constraints imposed by commercial vendors such as PCB fabricators and component manufacturers. The proposed antenna-on-PCB variation of an antenna-in-package is designed for RF beamforming applications to enable architectural flexibility and ease of board level scalability. The design prioritizes loss minimization to yield maximum system efficiency. in addition to reduced design complexity to aid in design realization. Commericial RF laminates and RFIC modules are incorporated to exemplify the capability of a phased array system that can be designed without the added advantage of custom substrates and in-house circuit models. An overall package conforming to fabrication IPC

Class 2 standards was fabricated with preliminary simulation results highlighting its potential.

Antenna element design incorporated preliminary vertical schematic layout and stackup definition to assign layer priority and ensure fabrication compatibility. A proximity coupled patch was employed to yield maximum achievable bandwidth under the smallest number of laminates, improving design registration. Substrates were kept thin to aid in surface wave suppression, without the need for intricate isolation enhancement such as patch backed cavities or via fencing. A direct via feed connecting both the antenna and the bottom layer was implemented to reduce overall feed line length and minimize total number of layer to layer interconnects. Infinite array analysis was performed to minimize design time, in addition to providing preliminary checks for element design in array environment. The phase attributes of the coupling characteristics to adjacent elements was then utilized to improve antenna bandwidth in the array environment, with unit cell resizing to reduce impedance variation with scan. A final element design size of $0.42\lambda_o$ x $0.5\lambda_o$ at 29.5 GHz ensured adequate preliminary scan performance, with the absence of grating lobes in the visible range. Full stack HFSS 3D Layout simulations exhibited 85.78% total efficiency, with an overall package loss of -0.66 dB, something not previously achievable in PCB implementation. A gain of 5.27 dB, including mismatch loss, at 28 GHz with a bandwidth of 3.5 GHz was achieved, meeting all design specifications. A 2x2 sub-array was simulated via full wave analysis to verify the findings and results confirmed aforementioned behaviour. Preliminary element-to-element isolation specification was not met, however this was deemed acceptable due to mechanisms used to achieve desired scan range.

A 4x4 antenna array was implemented by creating a 2x2 version of the 2x2 sub-array and performance was assessed via full wave simulation. A peak broadside gain of 15.47 dB was achieved at 28 GHz, accounting for mismatch loss. Active reflection coefficients were also evaluated and exhibited 3 GHz bandwidth, centered around 28 GHz. Before final implementation, a variation of the traditional wilkinson power combiner was designed that utilized a 50 Ohm thin film, high frequency resistor that exhibited greater than 3 GHz bandwidth, with the 1:2 variant possessing near -30 dB isolation, with 1:4 splitter meeting preliminary specifications and maintaining a value below -20 dB for the entire frequency range. Final layout required package expansion, which introduced deformation in the beam pattern, most notably in the E plane. This was a result of necessary board I/O connector placement and could not be avoided for such an array size. A realized gain of 15.43 dB was achieved with near 1 dB in band variation. Power combiner to antenna array isolation was assessed via active reflection coefficient computation for combiner input and synonymous "S21" for combiner output / RFIC input. Preliminary specifications set out to maximize isolation, and values ranging from -50 dB to -55 dB were obtained, which

resulted in minimal ARC variation and +/- 1.5 dB variation at chip input for scan range of $\theta_0 = +/-45^\circ$ in both principle planes.

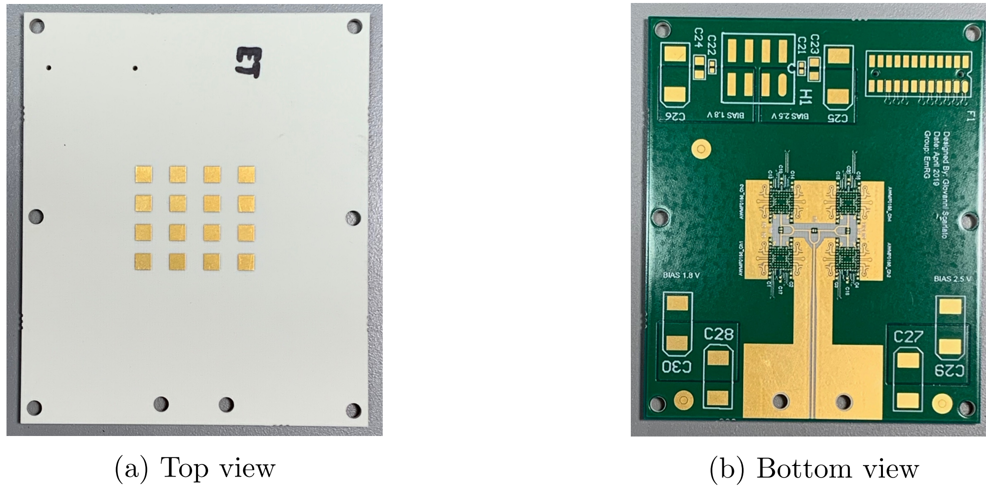
The AiP design was then extended to operate as a transmitter observation receiver for mmWave linearization schemes. The proposed TOR highlighted impractical attributes of traditional implementations and their applicability at mmWave. Utilizing a common technique for array pattern improvement with scan angle, dummy elements were Incorporated with probing fill factor limited to 40% due to space constraints, and element-to-element coupling served as the mechanism for output signal capture. The coupling frequency response was shown to be a function of main beam direction, (ϕ_o, θ_o), and for maximal flatness, symmetry could be leveraged to utilize a given set of probes for linearization at a given scan angle.

A series of test fixtures were used to validate simulation methodology and aid in determining the suitability for assembly. Microwave network analysis was performed with Keysight's PNA-X for one, two and four element arrays, in addition to a wilkinson power combiner. A TRL calibration kit was designed to de-embed the effects of the SMPM high frequency connector and aid in simulation comparison. Antenna performance exhibited excellent correlation with simulation, with response variation much attributed to error involved in hand assembly and its relation to the calibration standards. The RF power combiner utilized an edge mount connector in simulation and measurement to eliminate the need for user defined calibration standards and results showed discrepancy with simulation. Most notably, the input return loss and its relation to connector placement and edge gap, in addition to isolation degradation which has significant dependency on resistor hand assembly.

6.1 Future Works

Given the adequate results obtained from test fixture measurements, the designed AiP and TOR variant are to be assembled and characterized in future works. Figures 6.1 and 6.2 depict the fabricated AiP and TOR variant. Professional assembly will be used, and is often required for fine pitch flip-chip packaged RFICs to ensure optimal performance. Moreover, professional assembly yields an added benefit for the overall package as all other SMDs will exhibit reduced variability in placement.

Future implementations of the designed AiP look to expand the array size to a minimum of 64 elements, to maximize the array performance via approaching an infinite array footprint. A 64 element implementation is most applicable for mmWave deployment and



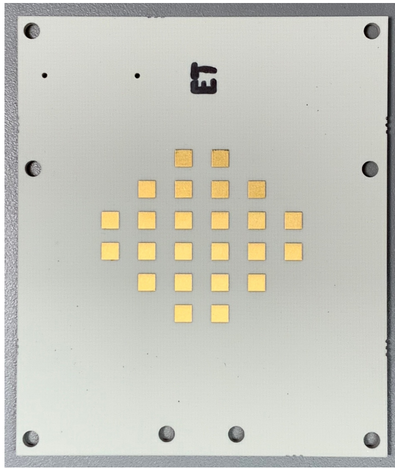
(a) Top view (b) Bottom view

Figure 6.1: Fabricated AiP

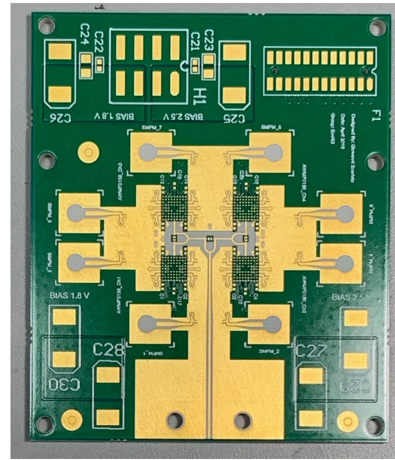
serves as the phased array reference for many applications. With the designed array, 64 elements is expected to abide by the bandwidth specification for larger scan angles, with improved beam pattern due to the reduced sensitivity to package expansion, given a larger array footprint.

Board level scalability is next in priority, and a reduced package footprint is ultimately necessary to achieve this. Such compact form factor permits the hybrid beamforming architecture, as IF is handled entirely off package. Currently a hybrid implementation of 4x64 element arrays is under development, and expected to be appended to the next fabrication run.

Finally, the proposed TOR architecture requires further investigation into integration within the array active area, without the introduction of pattern non-idealities. Given the current arrangement is restricted to array perimeter, it may be advantageous to investigate electromagnetic structures which can be integrated without significant increases in package density. Additional, probe placement optimization is also of great interest, as there may exist an arrangement of radiators that can aid in linearization for most of the scan range.



(a) Top view



(b) Bottom view

Figure 6.2: Farbricated AiP TOR variant

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