Extensible Architecture for Superconducting Quantum Computing

by

Thomas G. McConkey

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Examining Committee Membership

The following served on the Examining Committee for this thesis. The decision of the Examining Committee is by majority vote.

External Examiner	Name:	Dr. David Pappas
	Title:	Project Leader - NIST, Lecturer - University of Colorado
Supervisor	Name:	Dr. Matteo Mariantoni
	Title:	Assistant Professor
Supervisor	Name:	Dr. Hamed Majedi
	Title:	Professor
Internal Member	Name:	Dr. Zbig Wasilewski
	Title:	Professor
Internal Member	Name:	Dr. Chris Backhouse
	Title:	Professor
Internal/External Member	Name:	Dr. Jonathan Baugh
	Title:	Associate Professor

Author's Declaration

This thesis consists of material all of which I authored or co-authored: see Statement of Contributions included in the thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Statement of Contributions

Chapter 4 is based on the work in Ref. [1] which was a massively collaborative effort. Material from the published work which the author of this thesis was not involved in to some degree has been omitted. Components with which the author had little involvement with but is required for the presentation of later material has been heavily summarized or cited from the paper. The contributions for this chapter are listed below.

- T.G. McConkey - initial concept/design, microwave package design, spring characterization, microwave measurements, resonator fitting, fabrication, circuit design, simulations (both circuitry and package), editing.
- J.H. Bejanin - package holder design, microwave measurements, resonator fitting, magnetic measurements, editing.
- J.R. Rinehart - TDR measurements (not included), editing.
- C.T. Earnest - fabrication.
- C.R.H. McRae - fabrication, resonator fitting, circuit design.
- D. Shiri - microwave package design, spring characterization, resonator fitting.
- J.D. Bateman - simulations, spring characterization.
- Y. Rohanizadegan - laboratory setup.
- B. Penava, P. Breul, S. Royak and M. Zapatka - INGUN employees. Machined the three-dimensional wires, isolated wire measurements.
- A.G. Fowler - theory work.
- M. Mariantoni - supervision, project development and management, data measurements and analysis, editing.

This work was only made possible through the partnership with INGUN. The collaborative effort began using one of their standard coaxial pogo pins from which modifications were iteratively made based on our test results. All manufacturing of the coaxial pogo pin was done at INGUN's facility in Germany. All testing, besides the isolated wire measurement, was done in the Digital Quantum Matter Laboratory at the Institute for Quantum Computing. The isolated wire measurement was handled by INGUN due to having a well established testing procedure in place for all of their products.

Chapter 5 is based on the work in Ref. [2]. The only contributions made for this work as presented were from the thesis author and M. Mariantoni.

All circuit designs in this work are from the author or the author's parametrized circuit models under the author's supervision. All lithographic fabrication the author took part in followed SOPs that were developed by C.T. Earnest and C.R.H. McRae. C.T. Earnest is the sole DQM operated of the JEOL and as such fabricated all Josephson junctions, following the author's design.

Measurement and control software was written jointly by the author, J.H. Bejanin and J.R. Rinehart. Analysis software was written jointly by the author, J.H. Bejanin and C.R.H. McRae.

Abstract

Quantum computing architectures with ten or more quantum bits (qubits) have been implemented using trapped ions and superconducting devices. The next milestone in the quest for a quantum computer is the realization of quantum error correction codes. Such codes will require a large number of qubits that must be controlled and measured by means of classical electronics. This scaling up leads to a number of problems and sources of error that must be accounted for in order to have an operational system.

One architectural aspect requiring immediate attention is the realization of a suitable interconnect between the quantum and classical hardware. Our proposed solution to this wiring problem is the quantum socket, a three-dimensional wiring method for qubits with superior performance as compared to two-dimensional methods based on wire bonding. The quantum socket also provides a means to counteract another scaling problem, the coupling of qubits to unwanted cavity modes resulting in coherent leakage error. By following our proposed wiring methodologies, half-wave fencing or antinode pinning, we show how the error due to leakage can be mitigated to orders of magnitude below current state-of-the-art error probabilities.

Acknowledgments

I would first like to thank my supervisors, Dr. Matteo Mariantoni and Dr. Hamed Majedi, for the supervision and support through my PhD candidacy. Working as a member of Dr. Mariantoni's Digital Quantum Matter Laboratory was a privilege and I believe resulted in a number of great works.

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With respect to the work in Chapter 4, I acknowledge the support by the Alfred P. Sloan Foundation as well as the Natural Sciences and Engineering Research Council of Canada (NSERC), the Ministry of Research and Innovation (MRI) of Ontario, and the Canadian Microelectronics Corporation (CMC) Microsystems. Helpful discussions with John M. Martinis and the Martinis Group, Eric Bogatin, and William D. Oliver, and assistance from Adrian Lupascu as well as Patrick Smutek of Plassys-Bestek SAS for Al deposition. Further, thanks to Dario Mariantoni and Alexandra V. Bardysheva for their help with a few images and figures. For the work of Chapter 5, I acknowledge the support by the Canada First Research Excellence Fund (CFREF), the Discovery Grant Program of NSERC, and CMC.

The Quantum NanoFab team of IQC, lead by Vito Logiudice, has my gratitude for their assistance as does the machine shop of Science Technical Services, lead by Harmen Vander Heide. I am also grateful to Jean-Luc Orgiazzi for helpful discussion on experimental setups, and Andrew Dunsworth for help on resonator fitting analysis. Douglas Harder has my thanks for his advice and support with my teaching endeavors while at the University of Waterloo. I also appreciate the number of outreach programs I was able to be involved in thanks to Dr. Martin Laforest, Tobi Day-Hamilton and Angela Olano.

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Preface

Quantum computing has in recent years been gathering greater focus from researchers in both academia and industry. The nature of this research is very cross disciplinary, as the construction of a quantum computer needs expertise from many fields. It would not be at all surprising to see a new discipline of engineering develop, in much the same way as nanotechnology engineering has in recent years, focused around quantum computing and the related research. Although there are currently many proposed approaches for developing a quantum computer, the current choice seeming popular in is based on superconducting circuits. Such circuits have been available for multiple decades.

The first appearance of superconductivity was experimentation involving mercury, from the work by Heike Kamerlingh Onnes in 1911 [3]. This was soon followed by the Leiden laboratory discovering new superconducting materials [4] and Meissner and Ochsenfeld [5] determining the magnetic properties of superconductors, giving what is now known as the Meissner effect and the thermodynamic treatment of superconductivity.

At a similar time the London brothers published their semi-phenomenological theory of superconductivity in 1935 and explained the Meissner effect [6]. They also also derived the superconducting parameter, the London penetration depth λ_{L}. This parameter plays an important part in superconducting circuit design, as a magnetic field $\vec{\mathbf{B}}$ penetration of the superconductor is found from

$$|\vec{\mathbf{B}}\,(x)\,| = B_0 \mathrm{exp}\left[-\frac{x}{\lambda_{\mathrm{L}}}\right], \tag{1}$$

where B_0 is the magnitude of the parallel magnetic field at the superconductors surface and x is the depth into the superconductor. The brothers' work also showed the connection between the critical temperature (T_c) and critical current (I_c). This work was further expanded on by Vitaly Lazarevich Ginzburg and Lev Landau in 1950 [7], providing a full phenomenological explanation of the macroscopic properties of superconductors where the superconductor can be represented

by the macroscopic quantum wave function

$$\Psi = |\Psi| \exp[j\phi] \tag{2}$$

where $|\Psi|^2$ corresponds to the density of the superconducting state (or Cooper pairs which are next introduced), and ϕ to the phase of the superconducting wave function. All explanations of superconductivity had been phenomenological until Bardeen, Cooper and Schrieffer [8] introduced their theoretical explanation based on quantum first principles, which also introduced the concept of Cooper pairs. It was from this and other previous work that Brian David Josephson accurately predicted the tunneling of Cooper pairs through an insulating barrier in 1962 [9] (experimental results had shown this tunneling prior, incorrect explanations for the results had been provided) and derived the now well known Josephson effect equations [10] using the Ginzburg-Landau representation of the superconductors.

$$\begin{aligned} I(t) &= I_0 \sin(\phi_d(t)) \\ V(t) &= \frac{\hbar}{2e}\frac{\delta\phi_d}{\delta t} \\ \phi_d &= \phi_L - \phi_R \end{aligned} \tag{3}$$

where I/V refers to the current/voltage of the junction, I_0 is the critical current of the junction, $\hbar$ is the reduced Plank constant, e the electron charge. ϕ_d is the difference in phase between the left (ϕ_L) and right (ϕ_R) superconductors composing the junction. Although numerous research groups at this time were investigating aspects of superconductivity, it is still somewhat surprising that Ford Motor Co. Scientific Research Laboratory is responsible for the invention of the DC SQUID. Lambe accidentally stumbled across the effect while investigating nuclear double resonance, which Jaklevic used to create the first DC SQUID [11]. Although SQUIDs are the equivalent to a qubit as a MOSFET is to a bit, it would be another 30 years before the first superconducting qubit entered the scene.

The early stages of quantum computing took form in 1981 through Richard Feynman's presentation of a basic model of a quantum computer capable of simulating the evolution of a quantum system during a talk at MIT (as well as in his lecture "Theres plenty of room at the bottom"), which was later published [12]. Building off of Feynman's ideas, David Deutsch described a quantum universal Turing machine [13], a quantum computer which could simulate any other quantum computer as well as perform certain probabilistic tasks faster than a classical system. Shortly after at Bell Labs, both Peter Shor [14] and Lov Grover [15] showed such possible speed up with their respective quantum algorithms for factoring and database searching. The Shor algorithm is heavily responsible for the increased interest in quantum computing from all fields, as it not only showed the potential of computational speed up, but also increased interest outside of academia

given the numerous applications of factoring for government and industry (such as cracking RSA encryption). At the same time Seth Lloyd showed Feynman's conjecture to be correct, that a quantum computer can be programmed to simulate any local quantum system [16].

Although these proposals were all sound, they were still theoretical. In 1996 David Divincenzo proposed five requirements for the physical implementation of this theory of a quantum computer [17]:

1. "The degrees of freedom required to hold data and perform computation should be available as the dimension of the Hilbert space of a quantum system" in addition to being precisely identifiable. In essence the qubits must be well defined.
2. The quantum system can be placed in an arbitrary initial state reliably.
3. The quantum system must be isolated from coupling to its environment, or in other words the qubits must suffer low decoherence.
4. "It must be possible to subject the quantum system to a controlled sequence of unitary transformations", meaning a collection of accurate and reliable gate operations are required.
5. It must be possible to subject the system to a strong quantum measurement. In other words one must be able to be confident the measured result accurately represents the state of the system.

Cirac and Zoller provided one of the first results showing the feasibility of a quantum computer by showing the means to couple qubits together in a controlled manner so as to enable two qubit gates [18]. Without the clear ability to enable some form of a multiple qubit gate, there would be no means to run any form of quantum algorithms. Even today one of the most difficult components for a quantum computer is a fast and reliable two qubit gate.

In the same paper in which he proposed such requirements, DiVincenzo discussed a number of then current concepts in quantum error correction, a somewhat "unofficial" sixth requirement for the above list. Although error correction of classical bits was well established, many of the approaches could not be employed due to the no-cloning theorem (in simple terms that quantum bits can not be copied). Peter Shor and Andrew Steane each proposed a coding scheme that could function with qubits and correct for both bit flip errors and sign errors [19, 20]. The Shor code will correct for any arbitrary single-qubit error by taking a qubit state $|\psi\rangle$ and transforming it into the product of 9 qubits. If an error occurs to one of these qubits, it is able to be corrected so that the original state $|\psi\rangle$ can be recovered.

An alternative quantum error correcting code is a topological one such as the toric code introduced by Alexei Kitaev [21] and expanded on by Daniel Gottesman in 1997 [22] with his

in-depth analysis of stabilizer codes. This array of qubits with repeating offset stabilizers, seen in Fig. 1, was sound in theory but was still far from an actual physical design on which to process quantum computations. Further work from Kitaev as well as work from Sergay Bravyi [23, 24] and Robert Raussendorf [25] have lead us to the state of the surface code we have today, as best summed up by Austin Fowler et. al. [26].

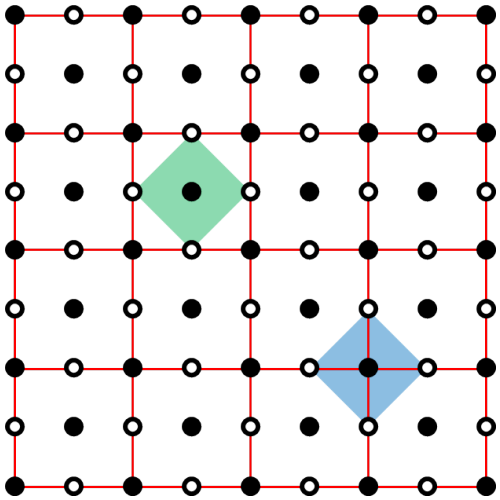

Figure 1: Lattice showing the planar code with Z-type stabilizers (living on plaquettes in green) and X-type stabilizers (living on vertices in blue) with data qubits on the edges of the lattice.

Parallel to the work on the surface code was the foundation of the superconducting qubit. The first use of a Josephson junction to acquire quantum coherence with a single Cooper pair was achieved by Vincent Bouchiat in 1998 [27]. The first superconducting qubit, the Cooper pair box (CPB), was created just a year later by Yasunobu Nakamura [28], making use of the DC SQUID to enable tuning of the Josephson energy by an external magnetic field.

Other superconducting qubits were soon developed, being the phase and flux qubit, but the next step of interest was the work from Schoelkopf's group in 2004 where a CPB was embedded in the middle of a coplanar waveguide (CPW) resonator to create the circuit equivalent of cavity quantum electrodynamics [29]. This approach provided a path to a scalable system that could easily follow the proposed surface code structure, yet it suffered from significant charge noise leading to poor T_2 times. A few years later Jens Koch, from the same research group, designed the now well known transmon which operates at a much higher ratio of Josephson energy (E_J) to charging energy (E_C) than the CPB [30], and giving far higher T_2 times. This design still suffered some issues regarding the ease of coupling multiple qubits, particularly if the goal was to create a physical implementation of the surface code.

In 2013 the Xmon was introduced by the Martinis Group at UCSB [31]. The Xmon had the same benefits of the transmon, but enabled the qubit to be connected to multiple circuits far more easily. It is this qubit, or variations of it, which has been the focus of research for

numerous groups and corporate initiatives into quantum computing research, such as Google, IBM or Rigetti.

Chapter 1

Introduction

At present, one of the main objectives in the quantum computing community is to build and prototype practical hardware technology for scalable architectures that may lead to the realization of a universal quantum computer [13]. Such a computer will make it possible to run certain algorithms much more efficiently than any classical computer [32]. Many implementations of the quantum computer and its primary component, the quantum bit or qubit, are currently under consideration [33], such as trapped ions [34], spins in molecules [35] and quantum dots [36, 37, 38, 39, 40], spins in silicon [39, 41], and superconducting quantum circuits [42, 43, 44].

In recent years, superconducting qubits [42, 45] have become the frontrunner due to the potential for scalability [46, 47] and robustness to dissipative phenomena [31, 48, 49]. In fact, superconducting qubits can be fabricated on a chip using standard lithography techniques and can be operated with available microwave electronics. This ease of use explains how superconducting qubits not only matched the decade long record held by nuclear magnetic resonance of 12 operational qubits [50, 46, 51, 52], but have quickly surpassed it, with the recent ≈ 50 qubit chips announced by IBM Q and Google's *Bristlecone* [1].

It has been shown that the error probabilities associated with the operation of these qubits can be as low as $\bar{p} \sim 10^{-3}$ [53, 54]. While such error probabilities are remarkable for a quantum-mechanical system, they are far from the error rates on the order of 10^{-15} necessary to run advanced quantum algorithms [26]. Achieving such error rates is only possible by means of quantum error correction (QEC) algorithms [32, 55, 56], for example, the surface code algorithm [25, 26]. Current reported error probabilities are below the surface code threshold, $\approx 1\%$, but are still large enough to require a very large array of physical qubits for the logical qubit to have the desired operational error rate. As reported in Ref [26], physical error rates that are one-tenth of the threshold leads to the logical qubit requiring an array of $\approx 100 \times 100$ physical qubits.

[1] Published results of these chips have not yet been made available to the public.

Superconducting qubit systems on such a scale are an entirely new endeavor, leading to new problems that have not been considered before. One of which is the wiring problem. The conventional wiring method of wire bonding suffers from fundamental scaling limitations as well as mechanical and electrical restrictions. Wire bonding relies on bonding pads that are located at the edges of the chip. Considering a two-dimensional lattice of $N \times N$ physical qubits on a square chip, the number of wire bonds that can be placed scales approximately as $4N$ (N bonds for each chip side). Wire bonding will fail to keep up to the required N^2 rate which physical qubits scale on a two-dimensional lattice. Furthermore, for large N, wire bonding is unable to reach physical qubits near the center of the chip. First, long wirebonds introduce significant series inductance which will interfere with microwave signal transmission, as well as lead to stray capacitances and inductances [57]. Second, wirebonds of standard thickness can not mechanically support itself over the distances which would be required on a large array of qubits.

Possible experimental solutions based on wafer bonding techniques [58, 59, 60, 61, 62] or coaxial through-chip vias [63] as well as theoretical proposals [47, 64] have recently addressed the wiring issue, highlighting it as a priority for quantum computing. The key concern for these and any approach is to ensure qubit decoherence and gate fidelities are not significantly impacted, such that the switch from wire bonds introduce a negative impact of no greater than 10% and remain above the surface code threshold [2]. Although ideally an improvement in both metrics would be observed, the slight loss in performance is outweighed by the ability to easily scale.

Another scaling issue that arises is the increased size of the microwave packages which house the qubit chips. The internal cavities of these packages begin to have cavity modes which will be in the frequency range of qubit operation. As discussed in Chapter 5, we found that unwanted cavity-qubit coupling rates can be comparable to those typically used for qubit gate and readout operations [53, 54] and much larger than the state-of-the-art qubit decoherence rates [31, 48, 49], leading to it being a likely source of errors. These can occur as correlated [66] and leakage errors [67, 68, 69]. This interaction can even be strong enough to lead to coherent leakage error probabilities well above $\bar{p}$. Any effective solution would need to ensure the leakage error probability was an order of magnitude less than $\bar{p}$.

1.1 Objective of This Thesis

The purpose of this thesis is to present solutions to some of the current scaling issues the superconducting qubit community are combating, or will be having to deal with in the near future. These solutions will not necessarily enable the construction of a quantum computer on the scale proposed in Ref. [26], where it is proposed that millions of qubits are necessary to factor a 6000

[2] These values vary greatly depending on which qubit implementation is being pursued. Single qubit gate fidelities of 99.9% and decoherence times of 100 µs have been reported [46, 65].

bit number, but will certainly enable systems of hundreds of qubits, which the field estimates is necessary for quantum supremacy and a functional logical qubit, and potentially thousands of qubits, from which a logical qubit with error rates comparable to classical systems could be generated.

Our proposed solution to the wiring problem is the *quantum socket*, a microwave packaging system which uses coaxial pogo pins that can reach any area on a given chip by making contact orthogonally from above, taking advantage of the third dimension. For this reason we refer to these wires as *three-dimensional wires*. The wires inner and outer conductor have diameters of 380 µm and 1290 µm, respectively, at the smallest point and with a maximum outer diameter of 2.5 mm. The movable section of the wire is characterized by a maximum stroke of approximately 2.5 mm, allowing for a wide range of on-chip mechanical compression.

All wire components are non magnetic, so as to minimize any risk of interference with the qubits. The three-dimensional wires work at both room and cryogenic temperatures. The wires have proven to have excellent reliability, with marginal variability over hundreds of measurements. Their electrical performance is good from DC to at least 8 GHz, with a contact resistance smaller than 150 mΩ. Notably, the coaxial design of the wires strongly reduces unwanted crosstalk, which we measured to be at most −45 dB for a realistic quantum computing application.

To mitigate the issue of coherent leakage error, we focus on increasing the detuning between the qubit and unwanted cavity mode. A larger detuning will lead to weaker interaction and in turn a lower error probability. To do so, we investigate two *frequency shifting methods* based on appropriately designed arrays of zero-potential boundary conditions: *Half-wave fencing* and *antinode pinning*. As the frequency shifting methods require the introduction of new boundary conditions, it is readily apparent why the quantum socket is a good match. The three-dimensional wires (or as some groups prefer to refer to as coaxial pogo pins) naturally provide new boundary conditions due to the ground conductor. They can also be placed almost arbitrarily, allowing whatever design is best suited for the frequency shifting method and the on chip circuitry. Alternative wiring methods, such as bump bonds [70, 61, 71, 72] or through-chip vias [63, 70, 73], can also be compatible with such frequency shifting methods. By means of numerical simulations we demonstrate that for a cavity-qubit frequency detuning larger than ∼20 % of the qubit frequency, the coherent leakage error probability is far below $\bar{p}$.

1.2 Outline of This Thesis

Before delving into the research work that was pursued to solve these scaling problems, some theoretical overview is required. This is so as to support the arguments that not only are these problems, or will be in the near future, but our proposed methods are ideal ways by which to solve them.

Chapter 2 will cover classical microwave circuitry and design. We review how to design a coplanar waveguide transmission line for a desired impedance, and how to find the resulting shunt capacitance. Resonators, in the form of lumped, planar and cavity, are presented as well as how to determine the quality factor for resonators with internal quality factors on the order of 10^6. Finally a brief review on signal loss, as well as two level system loss.

The quantum aspects of this work are covered in Chapter 3. The theoretical qubit and gates is briefly covered followed by a quick introduction to the surface code. We look at the quantized resonator, in lumped, planar and cavity form, finding the zero point voltage. The Xmon transmon is introduced along with the Jaynes-Cummings model. From this, the design process for the current Xmon transmon circuit design being used by the DQM Lab is discussed.

Our solution to the wiring problem, the quantum socket, is introduced in Chapter 4. The design process is reviewed in depth, for both the three-dimensional wires and the microwave package. The many aspects of its implementation are covered before presenting characterization measurements. The chapter is concluded with the results from cryogenic characterization, looking at very high quality superconducting resonators at single photon powers.

The scaling problem of coherent leakage due to cavity modes is introduced in Chapter 5. The coherent leakage probability, the metric we use to determine the error rate cause by this leakage, is presented along with the dispersive Purcell rate. Our two frequency shifting methods are introduced and the manner in which we analyze them using electromagnetic-field simulations is explained. We present the impact on cavity modes from our frequency shifting methods and how the coherent leakage and Purcell rate are changed. What these results lead to and how they can be best applied to real world experiments is discussed.

The thesis is then concluded in Chapter 6 with a summary of our results. A unit cell of a potential Xmon transmon circuit design which incorporates both of our proposed solutions is proposed, so as to solve both of the scaling issues presented in this work regardless of the microwave package size being used.

Chapter 2

Superconducting Microwave Circuits

Superconducting microwave circuits play a fundamental role in a number of quantum devices, usually in the form of superconducting resonators or Josephson junctions. From single photon detection [74, 75] to quantum computation and quantum buses [76, 77, 78], all of these applications are heavily dependent on the quality and performance of the circuits in question, such as the energy decay time.

Before addressing these more complex circuits one must first review a general superconducting transmission line (TL). Not only does a TL constitute the majority of a circuit design, but also as a planar resonator is simply a section of a waveguide TL with specific boundary conditions. The microwave TLs for the majority of these applications, and more importantly the case with this research, take the form of a coplanar waveguide (CPW). The CPW structure is fairly simple, a central conductive line with two neighbouring ground planes on top of a dielectric substrate, as seen in Fig. 2.1.

The reason for using CPW instead of microstrip or other planar alternatives is twofold:

- The fabrication process is simpler since all deposition and etching takes place on only one side of the dielectric wafer.
- A larger portion of the guided electromagnetic field is in the air/vacuum above the wafer, such that dielectric loss due to the substrate has less of an impact.

CPWs also have negative aspects to them, such as floating grounds and parasitic modes, but methods are available to combat those issues as discussed in Appendix B.2.

The designing of a CPW TL for specific impedance and capacitance is presented in Sec. 2.1. From this, a planar CPW resonator can be easily generated as shown in Sec. 2.2. This section

also covers the lumped LC resonator, a microwave cavity and the determination of the quality factor for such resonators. Finally, some sources of signal loss in our systems is covered in Sec. 2.3, including a brief discussion on two level system (TLS) loss, which is used as a 'measuring stick' for determining when a resonator is in the single photon power regime.

2.1 Coplanar Waveguide Design

As is the case with all transmission lines, the CPW can be represented in its circuit equivalent form. This makes it easier to design for the desired characteristic impedance, usually being 50Ω. Impedance mismatch generates undesirable reflection planes and transmission loss, though intentional mismatch can be used for filter design or power dividers. How one determines these circuit values based on the geometric dimensions of the CPW for regular materials is well established [79, 80, 81] as is the process for the necessary modifications when using superconducting materials [82, 83]. A full discussion on the CPW design and circuit values is available in Appendix A. For the purposes of this work, a quick review on determining the impedance and the TL capacitance is necessary.

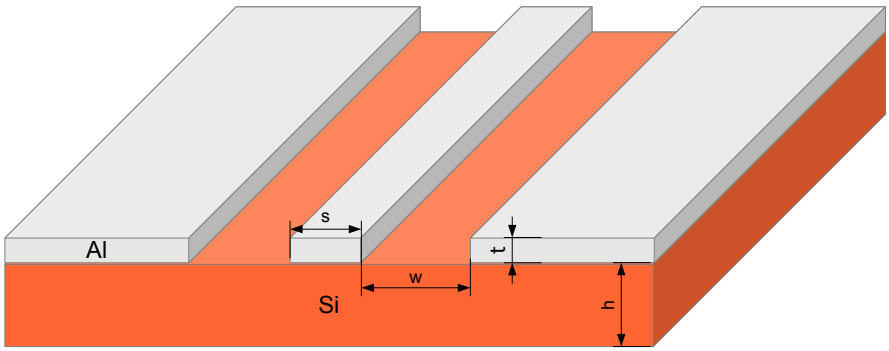

Figure 2.1: Coplanar waveguide structure with important dimensions labeled. t - film thickness, h - substrate thickness, s - width of center conductive line, w - gap between center conductive line and ground planes

The shunt capacitance per unit length, in the case of a CPW TL being between the signal line and the surrounding ground plane, is found from [82][1]

$$C_{dx} = 2\varepsilon_0(\varepsilon_r - 1)\frac{K(k_1)}{K(k_1')} + 4\varepsilon_0\frac{K(k_0)}{K(k_0')}, \tag{2.1}$$

[1]Unless otherwise noted, all equations for this section is from [82].

where $K(x)$ is the complete elliptical integral of the first kind, ε_0 is the free space permittivity, ε_r is the substrate dielectric constant and k_0, $k_0{}'$, k_1, and $k_1{}'$ are found from

$$k_0 = \frac{s}{s+2w} \tag{2.2}$$

$$k_0{}' = \sqrt{1-k_0^2} \tag{2.3}$$

$$k_1 = \frac{\sinh\left(\frac{\pi s}{4h}\right)}{\sinh\left(\frac{\pi(s+2w)}{4h}\right)} \tag{2.4}$$

$$k_1{}' = \sqrt{1-k_1^2} \tag{2.5}$$

where s, h and w are the geometric dimensions of the CPW, as seen in Fig. 2.1. It should be noted this approach is for a 'conventional' CPW, meaning the metallic thin film is treated as having zero thickness $t = 0$. This simplification is relatively accurate provided that $t \ll s + 2w$. If film thickness increases such that $t \approx s+2w$, the 'parallel plate' capacitance between the signal and ground planes must be considered [84, 85, 86], as shown below. The total capacitance of the TL is found from $C = C_{dx} \times l$ where l is the length of the transmission line.

The characteristic impedance of the transmission line can be derived in a similar fashion, although this ignores the potential impact of the kinetic inductance of the superconducting material, so should only be used provided the kinetic inductance is much lower than the external inductance [2]. To find the characteristic impedance, the frequency dependent effective dielectric constant, $\varepsilon_{\mathrm{ref,t}}(f)$, is required. First the effective dielectric constant for a zero thickness conductor at zero frequency is necessary [82],

$$\varepsilon_\mathrm{ref}(0) = 1 + q(\varepsilon_\mathrm{r} - 1), \tag{2.6}$$

where q, the filling factor, is found from,

$$q = \frac{1}{2}\frac{K(k_1)K(k_0{}')}{K(k_1{}')K(k_0)}. \tag{2.7}$$

[2] If the geometries of the circuit are all larger than the coherence length and penetration depth, the kinetic inductance can be practically ignored. For simple superconductors such as aluminum, this is the case when the film thickness is greater than the coherence length.

The filling factor indicates the amount of the electric field which penetrates the substrate, also referred to as the 'participation ratio' in some areas of research. The finite thickness of the film must also be taken into account by

$$\varepsilon_{\mathrm{ref,t}}(0) = \varepsilon_{\mathrm{ref}}(0) - \frac{0.7\left[\varepsilon_{\mathrm{ref}}(0) - 1\right]\frac{t}{w}}{\frac{K(k_0)}{K(k_0')} + 0.7\frac{t}{w}} \tag{2.8}$$

From this, the frequency dependent effective dielectric constant can be found from the closed-form expression

$$\sqrt{\varepsilon_{\mathrm{ref,t}}(f)} = \sqrt{\varepsilon_{\mathrm{ref,t}}(0)} + \frac{\sqrt{\varepsilon_{\mathrm{r}}} - \sqrt{\varepsilon_{\mathrm{ref,t}}(0)}}{1 + g\left(\frac{f}{f_{\mathrm{TE}}}\right)^{-1.8}} \tag{2.9}$$

$$g = \exp\left[u\ln\left(\frac{s}{w}\right)\right] + v \tag{2.10}$$

$$f_{\mathrm{TE}} = \frac{c_0}{4h\sqrt{\varepsilon_{\mathrm{r}} - 1}} \tag{2.11}$$

$$u = 0.54 - 0.64p + 0.015p^2 \tag{2.12}$$

$$v = 0.43 - 0.86p + 0.54p^2 \tag{2.13}$$

$$p = \ln\left(\frac{s}{h}\right) \tag{2.14}$$

where c_0 is the speed of light in a vacuum. The characteristic impedance is then found to be [80]

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{\mathrm{ref,t}}(f)}}\frac{K(k_0')}{K(k_0)} \tag{2.15}$$

It is advisable that resulting designs be simulated in an appropriate software package, e.g. Sonnet (from Sonnet) or HFSS (from ANSYS). This will give a more accurate finalized value, as the analytical approach discussed above fails to consider any components outside the transmission line, such as the capacitive coupling to the microwave package the device under test is housed in.

2.2 Resonators

Superconducting resonators are used in a number of quantum based devices. All of these applications are heavily dependent on the performance of the resonator, specifically the energy decay time. The implications of this can easily be seen in an implementation such as the surface code, since the number of physical qubits needed to create a logical qubit are dependent on what the error rate of the physical qubits are relative to the threshold [26]. Although rather simplified, the below equations provide an argument as to why the resonator quality factor (Q, the ratio of energy stored versus lost) equates to gate fidelity (F) [87]

$$F \approx \mathrm{e}^{-\frac{T_{\mathrm{Gate}}}{T_1}} \tag{2.16}$$

$$T_1 = \frac{Q}{2\pi f} \tag{2.17}$$

where T_1 is the life time of the resonator's Fock state, T_{Gate} is the time for a given qubit gate, and f is the frequency. As the quality factor is inversely proportional to loss, it becomes apparent (broadly speaking) that lower signal loss translates to improved error rates for a quantum computer. Although there are a number of sources for loss in resonators, such as radiative or resistive, as discussed in Sec. 2.3, a well engineered superconducting sample is able to minimize these sources of loss to insignificant levels. However, at the low power and low temperatures necessary for superconducting qubit operations, an additional source of loss can arise, dielectric loss due to TLS [88, 89, 90].

2.2.1 LC Lumped Circuit

The simplest representation of an electrical resonator is the LC circuit, seen in Fig. 2.2. The resonance of this circuit is found from

$$2\pi f_{\mathrm{r}} = \omega_{\mathrm{r}} = \frac{1}{\sqrt{LC}}. \tag{2.18}$$

The classical Hamiltonian, being the total energy of the system, can be found from

$$H_{LC} = \frac{Q^2}{2C} + \frac{\Phi^2}{2L} \tag{2.19}$$

where Q is the charge present in the capacitor and Φ is the flux present in the inductor. It can also be represented in the easier to directly measure values of current and voltage by substituting

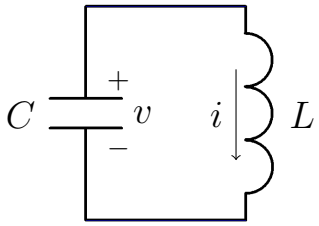

Figure 2.2: Simple LC resonator with natural angular frequency of $1/\sqrt{LC}$.

in the relations $Q = Cv$ and $\Phi = Li$ where v is the voltage drop across the capacitor and i is the current through the inductor, resulting in

$$H_{LC} = \frac{1}{2}Cv^2 + \frac{1}{2}Li^2 \tag{2.20}$$

Further, by using that $\omega = 1/\sqrt{LC}$, the resonance frequency of the resonator, Eq. 2.19 can be modified to be similar in form to the more well known harmonic oscillator

$$H_{LC} = \frac{Q^2}{2C} + \frac{1}{2}\omega_{\mathrm{r}}^2 C\Phi^2 \tag{2.21}$$

where $Q \sim p$, $C \sim m$ and $\Phi \sim x$ [3].

2.2.2 Planar CPW Resonator

Although lumped element resonators can be designed with CPWs, a distributed element resonator is easier to implement and generally of higher quality. These take the form of a length of transmission line which is terminated at both ends by open/capacitive loads (making it a $\lambda/2$ resonator) or shorted at one end (making it a $\lambda/4$ resonator), as seen in Fig. 2.3. In many experiments, resonators are multiplexed and shunted off a transmission line, allowing multiple resonators to be measured at a time. The first resonance frequency (f_{r}) of an ideal resonator can be found from

$$f_{\mathrm{r}} = \frac{\omega_r}{2\pi} = \frac{1}{\eta l\sqrt{(L_{dx,\mathrm{ext}} + L_{dx,\mathrm{k}})C_{dx}(\varepsilon)}} = \frac{c_o}{\eta l\sqrt{\varepsilon_{\mathrm{ref,t}}(f)}} \tag{2.22}$$

where l is the length of the resonator, and the circuit values are as discussed in Sec. 2.1. η is 2 for a half wavelength resonator, 4 for a quarter wavelength resonator [89]. Contrary to the lumped

[3] Where in the harmonic oscillator, p is the momentum, x is the position, and m is the mass of the object.

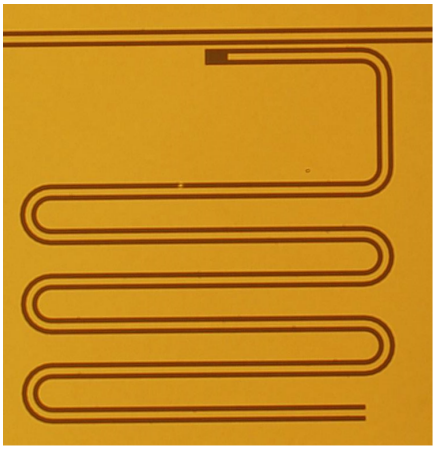

Figure 2.3: A $\lambda/4$ resonator capacitively shunted off of a TL (top).

element resonator, higher frequency modes can also be supported. It should be apparent that any aspect that changes the shunt capacitance, such as a thick metal film or trenching, will also change the resonance frequency of the resonator.

In any practical design the resonator will be coupled to one or many other circuits. For CPW resonators this is generally as a capacitive coupling which causes an increase in the electrical length of the resonator, causing the resonance frequency to decrease. Mazin determined the difference between the ideal resonance frequency ($\omega_{1/4}$) and the capacitively coupled resonance frequency (ω_c) using Eq. 2.23 for a shunted $\lambda/4$ resonator [91]

$$\omega_{\mathrm{c}} - \omega_{1/4} = \frac{-2Z_0\omega_{\mathrm{c}}\omega_{1/4}C_{\mathrm{c}}}{\pi}, \tag{2.23}$$

where C_{c} is the coupling capacitance between the resonator and a transmission line. Alternatively Goppl directly calculated the shifted resonance by generating the Norton equivalent circuit model of the $\lambda/2$ series resonator resulting in (for the first mode) [92]

$$\omega_c = \frac{1}{\sqrt{L_n(C + 2C^*)}}, \tag{2.24}$$

$$C = \frac{C_{dx}l}{2}, \tag{2.25}$$

$$L_n = \frac{2L_{dx}l}{\pi^2}, \tag{2.26}$$

$$C^* = \frac{C_{\mathrm{c}}}{1 + 2\pi f_0 C_{\mathrm{c}}^2 Z_0^2}. \tag{2.27}$$

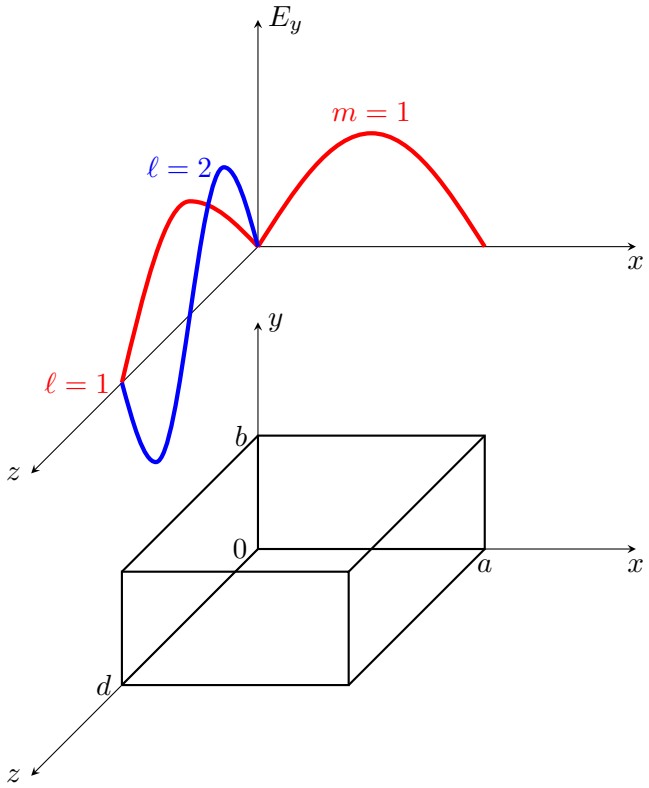

Figure 2.4: A rectangular cavity with dimensions for Eq. 2.28 indicated. The E_y magnitude for TE101 and TE102 for this structure is shown above.

In both cases the value of the coupling capacitance is necessary, though it can be rather difficult to determine analytically from the geometry of the circuit. A simple gap capacitance has been fairly well analyzed [80, 93] by representing it as a capacitive pi network model, though for geometries significantly larger than those employed for superconducting qubits. This model can also be used for interdigitated capacitors.

The best way to determine the necessary circuit design for the desired C_c is through numerical simulations of the electromagnetic fields with the use of a software package such as Q3D from ANSYS. A popular alternative is 'FasterCap', though it is a rather complicated piece of software and quite unfriendly for new users. It is suggested it only be employed when optimizing a final design. The uncoupled resonance frequency of the design can also be simulated using HFSS from ANSYS with the eigenmode solution type, and the transmission of the coupled system with the modal solution type.

2.2.3 Microwave Cavity

Another type of microwave resonator to consider is the microwave cavity. Although any shape of cavity could support resonant modes, we will focus on a box made of conductive material filled

with a dielectric. It is similar in concept to the planar CPW resonator being a 'diced' section of transmission line, but in this case being a microwave waveguide with additional boundary conditions. The CPW planar resonator (practically) supports modes in just the one dimension of its length, whereas the microwave cavity supports modes in all three dimensions, being transverse electric (TE) or transverse magnetic (TM) modes. The frequencies of these modes for a rectangular cavity are found from

$$f_{nm\ell} = \frac{c}{2\pi\sqrt{\mu_{\rm r}\varepsilon_{\rm r}}} k_{nm\ell} = \frac{c}{2\pi\sqrt{\mu_{\rm r}\varepsilon_{\rm r}}} \sqrt{\left(\frac{n\pi}{b}\right)^2 + \left(\frac{m\pi}{a}\right)^2 + \left(\frac{\ell\pi}{d}\right)^2}, \tag{2.28}$$

where $\mu_{\rm r}$ is the relative permeability of the dielectric (being 1 for most scenarios), m, n and ℓ are the modes of the resonance and a, b and d are the dimensions of the cavity, as seen in Fig. 2.4.

The equivalent capacitance and inductance for a given mode can be found from [94]

$$L_{nm\ell} = \mu k_{nm\ell}^2 v_0, \tag{2.29}$$

$$C_{nm\ell} = \frac{\varepsilon_{\rm r}\varepsilon_0}{k_{nm\ell}^4 v_0}, \tag{2.30}$$

where v_0 is the cavity volume.

If the material inside the cavity is not homogenous, as is the case with most experiments, the resonant frequencies must be determined through perturbation methods. The perturbed frequency can be found, as described by Pozar [79], from the relative change of permittivity or permeability, provided they are relatively small, in a given area of the cavity from

$$\frac{f_{\rm p} - f_{\rm r}}{f_{\rm p}} \simeq \frac{-\int_{v_0} \left(\Delta\varepsilon \left|\overline{E}\right|^2 + \Delta\mu \left|\overline{H}\right|^2\right) dv}{-\int_{v_0} \left(\varepsilon \left|\overline{E}\right|^2 + \mu \left|\overline{H}\right|^2\right) dv} \tag{2.31}$$

where f_p is the frequency of the perturbed cavity, $\varepsilon = \varepsilon_0\varepsilon_{\rm r}$ and $\mu = \mu_0\mu_{\rm r}$ is the permittivity and permeability of the non-perturbed cavity and $\Delta\varepsilon$ and $\Delta\mu$ is the change to the permittivity and permeability by the perturbation, ε_0 and μ_0 are the vacuum permittivity and permeability respectively. For a simple perturbation, as is seen in Fig. 2.5, of standard dielectric material, such that $\Delta\mu = 0$ and $\Delta\epsilon = (\epsilon_{\rm r} - 1)\epsilon_0$ for $(0 \leq y \leq t)$ and 0 elsewhere, Eq. 2.31 can be easily solved. The numerator becomes

$$(\varepsilon_{\rm r} - 1)\,\varepsilon_0 \int_{x=0}^{a} \int_{y=0}^{t} \int_{z=0}^{d} |E_y|^2 \, dz \; dy \; dx = \frac{(\varepsilon_{\rm r} - 1)\,\varepsilon_0 \; a \; t \; d}{4} A^2, \tag{2.32}$$

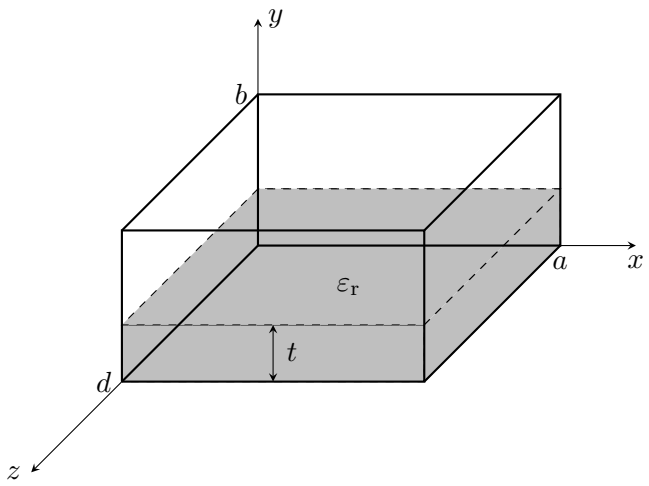

Figure 2.5: A rectangular cavity which has a perturbation from a mismatched dielectric of thickness t.

where A is the amplitude of the field. The denominator is proportional to the total energy in the unperturbed cavity, giving

$$\frac{a\ b\ d\ \varepsilon_0}{2} A^2 \tag{2.33}$$

The resulting frequency of this perturbation is then found to be

$$f_p = f_r - \frac{f_r\,(\varepsilon_r - 1)\,t}{2b} \tag{2.34}$$

2.2.4 Quality Factor

As mentioned previously, the quality factor of a resonator is a key concern for many applications, including superconducting quantum computing. The most common way to determine the quality factor of on chip planar resonators is with the scattering parameters (S-parameters) of the circuit of interest. These are acquired by measurements with a vector network analyzer (VNA). For nearly all experiments discussed in this work, the devices are two port. As such S_{21} can be seen as the power transmitted through the device and S_{11} the power reflected. Generally, if there are no active components in the circuit, it can be presumed it is symmetric ($S_{ab} = S_{ba}$). This symmetry does not hold, for example, when taking measurements of samples in our dilution fridge, due to the amplifiers and circulators that are present.

A simple method to find the quality factor is to measure the S_{21} of the circuit around the resonance frequency, and use Eq. 2.35 with reference to Fig. 2.6 to determine the total or measured

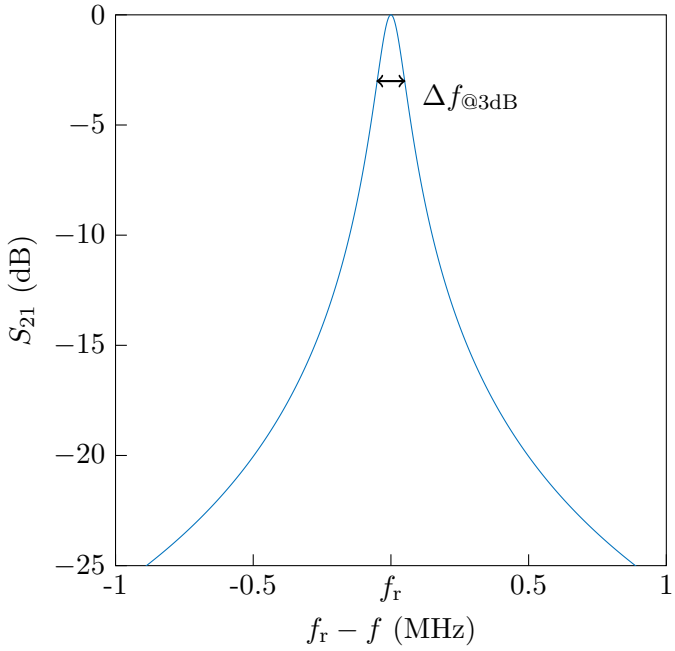

Figure 2.6: The S_{21} measurement about resonance of a series $\lambda/2$ resonator. The 3 dB point for use in Eq. 2.35 is shown.

quality factor

$$Q_T = \frac{\Delta f_{@3dB}}{f_r}. \tag{2.35}$$

This method is over simplified and will not give very accurate results when considering the measurement environment of this work. Formula for accurate fitting of measurement data is somewhat dependent on the surrounding circuitry and type of resonator coupling, although there is even some variance among different research groups using similar setups. As was mentioned previously, the quality factor is a ratio of the energy stored versus the energy lost. As such it should be clear that when an isolated resonator is coupled to another system, such as through a capacitor, the measured quality factor would drop as a new path for energy dissipation has been introduced. The measured, or total, quality factor Q_T is the parallel summation

$$\frac{1}{Q_T} = \frac{1}{Q_c} + \frac{1}{Q_i} \tag{2.36}$$

where Q_c is the coupling (capacitor) quality factor and Q_i is the internal quality factor of the resonator. It is necessary to determine both of these values as Q_i provides information with respect to the quality of fabrication and material loss mechanisms, where Q_c provides confirmation on

if the design of coupling strengths was accurate. For this work, we relied on the procedure as presented in Ref. [95] when analyzing $\lambda/4$ shunted resonators. The transmission is found to be

$$S_{21} = \frac{2V_2}{V_1} = \frac{2Z_0}{Z_1 + Z_2} \frac{1}{1 + Z/2Z_\mathrm{r}}, \tag{2.37}$$

where Z_0 is taken to be 50Ω, $Z_1 = Z_0 + \Delta Z_1$, $Z_2 = Z_0 + \Delta Z_2$ and $1/Z = 1/2Z_1 + 1/2Z_2$. ΔZ_1 and ΔZ_2 are to account for small impedance mismatches of the transmission line on either side of the resonator, but these can be calibrated out by using off resonance measurements. Z_r is found from

$$Z_\mathrm{r} = \frac{Z_0 Q_\mathrm{c}}{2Q_\mathrm{i}}(1 + j2Q_\mathrm{i}\Delta f), \tag{2.38}$$

for frequencies near f_r, where $\Delta f = (f - f_\mathrm{r})/f_\mathrm{r}$. A normalized inverse transmission, $\tilde{S}_{21}$, is then found to be

$$\tilde{S}_{21}^{-1} = 1 + \frac{Z}{2Z_r} = 1 + \frac{Q_\mathrm{i}}{Q_\mathrm{c}^*} e^{j\phi} \frac{1}{1 + j2Q_\mathrm{i}\Delta f}, \tag{2.39}$$

where $Q_\mathrm{c}^* = (Z_0/|Z|)Q_\mathrm{c}$. It is relatively straightforward to fit the normalized inverse transmission measurement to this equation, as it is simply a circle in the complex plane, as seen in Fig. 2.7. At the resonant frequency, $\tilde{S}_{21}^{-1} = 1 + De^{j\phi}$, giving said circle a diameter of $D = Q_\mathrm{i}/Q_\mathrm{c}^*$. This level of analysis, in comparison to Eq. 2.35, is necessary when considering superconducting resonators with Q_i on the order of millions.

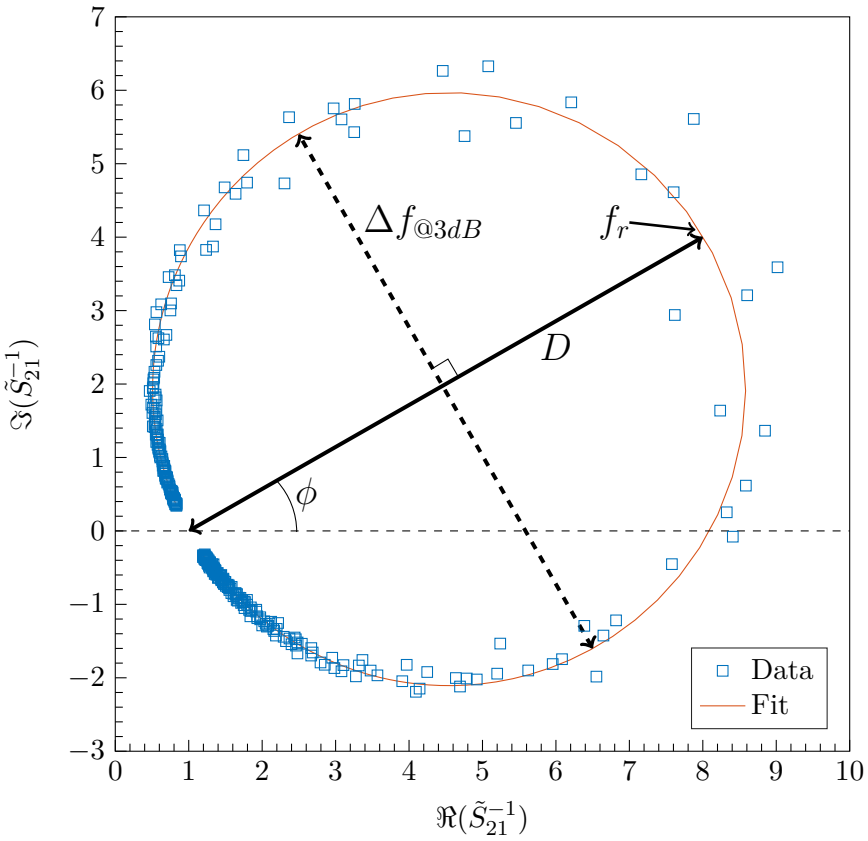

Figure 2.7: Polar plot of the normalized inverse transmission coefficient $\tilde{S}_{21}^{-1}$ for $\lambda/4$ superconducting resonator. Data shown with blue squares, the fit as a solid red line generated with Eq. 2.39. D, $\Delta f_{@3dB}$, f_r and ϕ of Eq. 2.39 are indicated in black.

2.3 Signal Loss

Signal loss can be a significant issue in standard microwave transmission, causing errors or poor signal quality. For quantum computing, it can be completely detrimental. Given how low signal power is for, as an example, qubit readout, attenuation is not simply a drop in power, but can be considered the probabilistic loss of the information entirely.

The sources of loss to consider are:

- **Radiative loss** - any loss of the signal due to some of the electromagnetic wave propagating away from the circuit into freespace or any coupling to an external environment that is not a part of the circuit. For a TL with no shielding, the loss is proportional to the gap and width values of the CPW, with the loss factor being roughly on the order of a percent or lower for the dimensions used in this work [80]. Discontinuities can also increase the amount of radiative loss, though generally the circuit must be simulated in a 3D EM software to accurately determine this. Proper EM shielding around the circuit can prevent this loss,

as discussed in Chapter 4. How radiative loss can impact quantum signals is discussed in Chapter 3 and how to combat such issues in Chapter 5.

- **Conductor loss** - resistance in the conductive material being used will attenuate the signal. The series resistance, as seen in the TL circuit model of Fig. A.1, can be the largest source of signal loss for microwave circuits. The skin effect leads to an increased resistance as frequency increases, such that $R \sim \sqrt{f}$. The "easiest" method to prevent this loss is by using a superconductor at near zero kelvin temperature. At very high frequency (around 10^{11} Hz) the surface resistance of the superconductor begins to become significant, and will completely lose the superconducting benefit if higher than the gap frequency of the superconductor [96].

- **Dielectric loss** - this is calculated by the loss tangent of the dielectric being used. The loss tangent can be expanded to

$$\tan(\delta) = \frac{\epsilon''}{\epsilon'} + \frac{\sigma_n}{2\pi f \epsilon'} \tag{2.40}$$

where the first term represents the loss due to dipole motion in the dielectric and the second term are the 'regular' resistive losses as it represents the conductive channel of free electrons through the dielectric. Generally for a dielectric the conductive channel is non-existent and so can be ignored, but is present in the case of semi-conductors. Some loss due to the dielectric is unavoidable as a physical substrate is necessary to mechanically support the CPW and the technology to fabricate a perfect dielectric does not yet exist. There are however a number of methods to minimize this loss ranging from lowering the filling factor through 'trenching', to advanced deposition techniques. It is also worth noting these methods lower the loss due to TLS as well.

Although this work does not focus on the loss caused by two level systems, such loss is used as an informal 'measuring stick' for determining if the resonator measurements are in the low power regime. The quality factor of the resonator will display a clear 'S-curve' when swept against VNA output power, as seen from[4] [97]

$$\frac{1}{Q_{\mathrm{i}}\left(\langle n_{\mathrm{ph}}\rangle, T\right)} = q\ \delta_{\mathrm{TLS}}\left(\langle n_{\mathrm{ph}}\rangle\right) + \frac{1}{Q^*}, \tag{2.41}$$

where q is the filling factor from Eq. 2.7, $\langle n_{\mathrm{ph}}\rangle$ is the mean photon number in the resonator, Q^* accounts for all of the 'standard' loss mechanisms, and $q\ \delta_{\mathrm{TLS}}\left(\langle n_{\mathrm{ph}}\rangle\right)$ is found from (considering

[4]Working from the assumption that losses are low enough such that $\tan(\delta) \simeq \delta$

only temperatures, T, far below the frequency of the photons being considered)

$$q\ \delta_{\mathrm{TLS}}\left(\langle n_{\mathrm{ph}}\rangle\right) \simeq \frac{q\ \delta^{0}_{\mathrm{TLS}}}{\sqrt{1+\left(\frac{\langle n_{\mathrm{ph}}\rangle}{\langle n_{\mathrm{ph}}\rangle^{c}}\right)}}. \tag{2.42}$$

where $\langle n_{\mathrm{ph}}\rangle^{c}$ is the critical mean photon number (where the TLS's begin to become saturated) and $\delta^{0}_{\mathrm{TLS}}$ is the loss tangent due to TLS's at zero temperature. The TLS saturation is the effect that, although the TLS can be thought of as a lossy coupled resonator, it is only capable of containing a single photon, where other loss mechanisms are relatively independent from photon count. As such, at higher powers, the TLS loss contribution becomes a much smaller portion of the total losses, to the point where they can simply be ignored.

An extensive discussion on TLS loss and the work related to this area the Digital Quantum Matter Laboratory is pursuing can be found from Ref. [97].

2.4 Conclusion

The necessary classical microwave engineering material for this work, and for much of the work in superconducting qubit systems, was presented. All CPW circuit design was based on Ref. [82], from which Matlab code was written so as to generate appropriate CPW geometries for a given desired characteristic impedance. The designs would then be confirmed in simulation software such as HFSS of Ansys Electronic Desktop.

Three important forms of electrical resonators were reviewed: the lumped LC circuit, which is a useful basis for analyzing other resonant systems and quantization as seen in Sec. 3.3; planar CPW resonators, used through out this work; and microwave cavities, where the LC equivalent circuit, used later for the deriving the zero point voltage of a cavity, and the effect of dielectric perturbation of the cavity was shown. Matlab code was also written for generating geometries of planar CPW resonators, with parametrized models in HFSS to confirm desired resonances were reached.

Finally, sources of signal loss were briefly reviewed along with introducing TLS loss which is prominent at low powers and the 'S-Curve'. This is used so as to determine when input measurement power is low enough to be only introducing a small number of photons to the resonator under test. This photon count is relevant as it is the condition a resonator would be experiencing during qubit operation and measurement.

From this classical basis we can transition to the quantum realm through the quantization of our measurable values in the next chapter.

Chapter 3

Circuit Quantum Electrodynamics

To recognize why quantum computing systems must scale to larger qubit counts and why doing so will lead to unwanted errors, a review of quantum information theory and circuit quantum electrodynamics is required. Basic qubit operations and the surface code are briefly covered in Sec. 3.1 and 3.2. The quantization of a superconducting resonator is discussed in Sec. 3.3 followed by the Xmon transmon in Sec. 3.4. Finally the Jaynes-Cummings Model is developed for a cavity qubit system in the one excitation sector in Sec 3.5, which is required for the analysis of coherent leakage errors in later chapters.

3.1 The Qubit

For the uninitiated, the qubit can simply be thought of as the quantum equivalent of the classical bit. Just as the classical bit has states 0 ('off', low voltage, etc.) and 1 ('on', high voltage, etc.), the qubit has states $|0\rangle$ and $|1\rangle$ (or $|g\rangle$ and $|e\rangle$), but also can be in a superposition of the two,

$$|0\rangle = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \qquad |1\rangle = \begin{bmatrix} 0 \\ 1 \end{bmatrix}$$
$$\alpha\,|0\rangle + \beta\,|1\rangle = \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \tag{3.1}$$

where $\alpha, \beta \,\epsilon\, \mathbb{C}$ and $\alpha^2 + \beta^2 = 1$. The values, α^2 and β^2, indicate the probability of measuring that value, presuming measurement is in the same basis. Qubits can also be entangled, in that

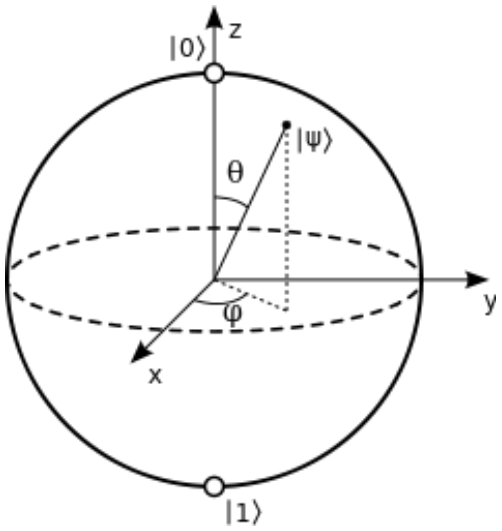

Figure 3.1: Bloch sphere with state of the qubit $|\hat{\psi}\rangle = \cos(\frac{\theta}{2})\,|0\rangle + e^{j\phi}\sin(\frac{\theta}{2})\,|1\rangle$. [98]

the resulting state can not be factored as a product of the individual qubits

$$\begin{aligned} |00\rangle &= \begin{bmatrix}1\\0\\0\\0\end{bmatrix} \qquad\qquad |11\rangle = \begin{bmatrix}0\\0\\0\\1\end{bmatrix} \\ \alpha\,|00\rangle + \beta\,|11\rangle &= \begin{bmatrix}\alpha\\0\\0\\\beta\end{bmatrix} \quad \neq (\alpha_0\,|0\rangle + \alpha_1\,|1\rangle) \bigotimes (\beta_0\,|0\rangle + \beta_1\,|1\rangle) \end{aligned} \tag{3.2}$$

The individual states of the qubit (if in a pure state) can be thought of as a point on the Bloch Sphere, as seen in Fig. 3.1. Single qubit gates X, Y and Z can then be seen as rotations about their respective axis. As an example, an X_π-gate causes a π rotation about the x-axis. For a qubit in the $|g\rangle$ state, this excites it to the $|e\rangle$ state ($X\,|g\rangle = |e\rangle$). The Hadamard, H, gate is often used for entanglement purposes or changing measurement basis, which is the equivalent of a π rotation about the x-axis, and a $\pi/2$ rotation about the y-axis. For useful computations a two qubit gate is also required, such as the C-NOT, which operates in the same manner as the classical C-NOT.

$$\begin{aligned} X = \hat{\sigma}_x &= \begin{bmatrix}0 & 1\\1 & 0\end{bmatrix} \quad Y = \hat{\sigma}_y = \begin{bmatrix}0 & -j\\j & 0\end{bmatrix} \\ Z = \hat{\sigma}_z &= \begin{bmatrix}1 & 0\\0 & -1\end{bmatrix} \quad H = \tfrac{1}{\sqrt{2}}\begin{bmatrix}1 & 1\\1 & -1\end{bmatrix} \end{aligned} \tag{3.3}$$

$$\hat{\sigma}^{\pm} = \hat{\sigma}_x \pm j\hat{\sigma}_y \tag{3.4}$$

$$CNOT = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix} \tag{3.5}$$

3.2 The Surface Code

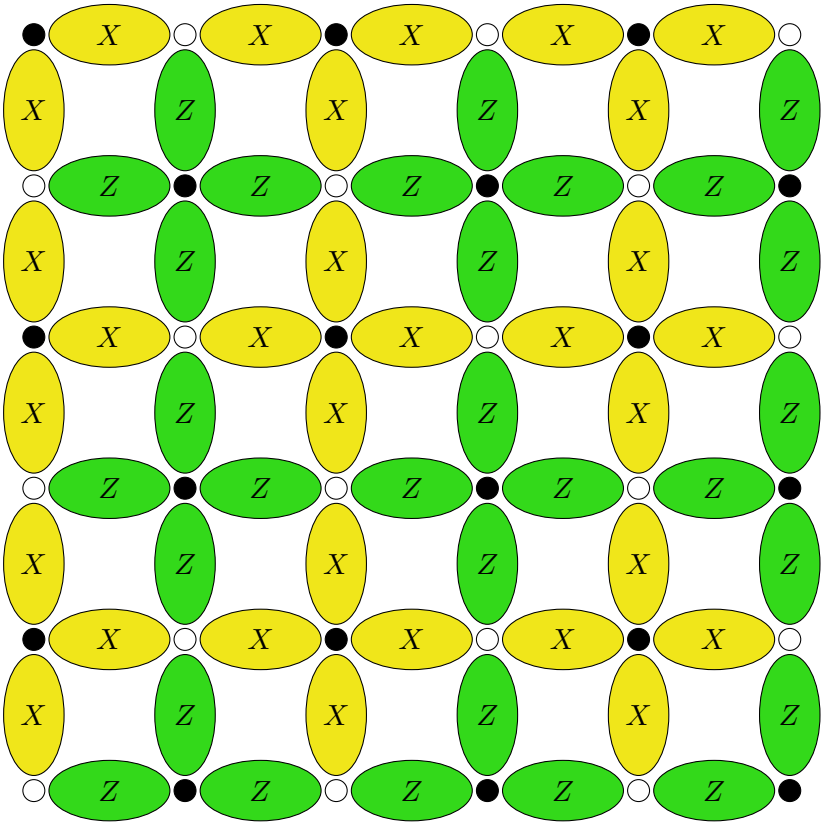

Figure 3.2: Surface code architecture. Black circles represent measurement qubits (yellow for X-measure and green for Z-measure), empty circles represent data qubits.

Given a perfect qubit is practically impossible and errors will always be an issue, the creation of a quantum computer will inevitably involve some form of error correction. The surface code has so far been shown to be the best implementation for error correction of quantum bits as it has both a reasonably low threshold, allowing per operation error rates as high as 1% [99], and lends itself very well to scaling on a 2D planar surface. It operates by spreading the information of an individual logical qubit over numerous physical qubits, as seen in Fig. 3.2. The physical

data qubits (empty circles) are entangled and constantly measured with measurement qubits (the black circles) using a complete set of commuting stabilizers. These do not damage the state of the system but allows detection of an error through a change of the measurement outcome [26]. An example of this process is provided in Appendix C, as was presented by Fowler et. al..

The surface code clearly provides a means of error protection of quantum bits, but the cost of this protection must be considered. The logical qubits will require error rates somewhat equivalent to that of current classical computers ($\sim 10^{-14}$). The code length, or array size, of the logical qubit to reach such error rates is determined on the gate fidelity or error rate of the physical qubits. If a physical error rate of 0.1% is presumed, roughly 3600 physical qubits are required for each logical qubit to have a logical error rate low enough for an algorithm to properly run [26, 25]. This cost in space can become rather significant depending on the qubit implementation being employed. Following an implementation that is currently being pursued by Google, the chip would need to be 2.5 cm $\times$ 2.5 cm, and that is just from considering the Xmon transmon dimensions.

3.3 Quantized Superconducting Resonator

There are various methods to quantize the resonator, such as working from the Lagrangian of the circuit charge and current [100] or the flux [101], but being a report for electrical engineering, it seems appropriate to work from the classical Hamiltonian of the LC form seen in Eq. 2.21 [102]. Taking this form of the classical Hamiltonian, we can replace the classical quantities Q and Φ by the observables in a Hilbert space, $\hat{Q}$ and $\hat{\Phi}$, resulting in the Hamiltonian for the quantum LC resonator

$$\hat{H}_{LC} = \frac{\hat{Q}^2}{2C} + \frac{1}{2}\omega_{\mathrm{r}}^2 C\hat{\Phi}^2, \tag{3.6}$$

where $\omega_{\mathrm{r}} = 2\pi f_{\mathrm{r}}$ and the observables $\hat{Q}$ and $\hat{\Phi}$ are canonically conjugated (as $\hat{p}$ and $\hat{x}$ are) giving the commutation relation

$$\left[\hat{Q}, \hat{\Phi}\right] = j\hbar, \tag{3.7}$$

where $\hbar$ is the reduced Plank constant, in addition to the creation/annihilation operators ($\hat{a}^\dagger$ / $\hat{a}$) which are found to be

$$\hat{a}^\dagger = \frac{1}{\sqrt{2C\hbar\omega_{\mathrm{r}}}}(\hat{Q} - jC\omega_{\mathrm{r}}\hat{\Phi}), \tag{3.8}$$

$$\hat{a} = \frac{1}{\sqrt{2C\hbar\omega_{\mathrm{r}}}}(\hat{Q} + jC\omega_{\mathrm{r}}\hat{\Phi}), \tag{3.9}$$

and that $\hat{Q}$ and $\hat{\Phi}$ can be rewritten as the Hermitian operators ,

$$\hat{Q} = \sqrt{\frac{C\hbar\omega_{\mathrm{r}}}{2}}\left(\hat{a}^{\dagger} + \hat{a}\right), \tag{3.10}$$

$$\hat{\Phi} = \sqrt{\frac{C\hbar\omega_{\mathrm{r}}}{2}}j\left(\hat{a}^{\dagger} - \hat{a}\right), \tag{3.11}$$

which allows the Hamiltonian of the quantized LC resonator to be written as

$$\hat{H}_{LC} = \hbar\omega_{\mathrm{r}}\left(\hat{a}^{\dagger}\hat{a} + \frac{1}{2}\right), \tag{3.12}$$

which leads to the energy levels being

$$E_n = \left(n + \frac{1}{2}\right)\hbar\omega_{\mathrm{r}}, \tag{3.13}$$

for n = 0:∞, with each energy level being equally spaced by $\hbar\omega_{\mathrm{r}}$. This is important to note since on its own such a resonator could not function as a qubit since it lacks easily distinguishable energy levels. This can also be seen in Fig. 3.3 where the probability densities for each energy level is plotted against the potential energy of the LC resonator.

The Hamiltonian in Eq. 2.20 can also be represented in the quantized form as $\hat{Q} = C\hat{V}$ and $\hat{\Phi} = L\hat{I}$,

$$\hat{H}_{LC} = \frac{1}{2}C\hat{V}^2 + \frac{1}{2}L\hat{I}^2 \tag{3.14}$$

From Eq. 3.13 it can be seen that the zero-point energy for this system is $\hbar w/2$, the lowest energy state that can be achieved. From Eq. 3.14 it should also be apparent that this zero-point energy results in a voltage and current being present in the system dependent on the values of the capacitance and inductance. This is clearly seen by finding the zero-point voltage (V_0) of the capacitor and zero-point current of the inductor (I_0). For the case of the capacitor, the quantum

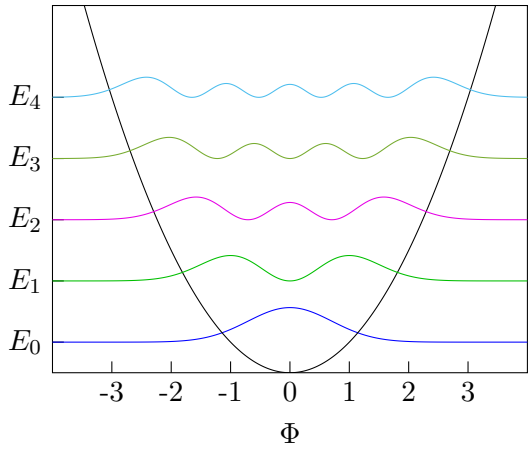

Figure 3.3: Probability densities of the first five eigenstates for the quantized LC resonator. Values have been normalized. Eigenenergies for the respective probability density are listed on the y-axis. Black parabola is overlay of the circuits potential energy.

mechanical expectation value for the capacitor component of Eq. 3.6 can be calculated (using Eq. 3.10) and equated to the capacitor energy at the ground state such that

$$E_{C0} = \frac{1}{2}CV_0^2 = \left\langle 0 \left| \hat{H}_C \right| 0 \right\rangle = \frac{\hbar\omega}{4} \left\langle 0 \left| \hat{a}^{\dagger 2} + \hat{a}^\dagger \hat{a} + \hat{a}\hat{a}^\dagger + \hat{a}^2 \right| 0 \right\rangle = \frac{\hbar\omega}{4} \tag{3.15}$$

in which one can isolate for V_0 to find

$$V_0 = \sqrt{\frac{\hbar\omega}{2C}} \tag{3.16}$$

With the zero-point current being found in the same manner ($I_0 = \sqrt{\hbar\omega/2L}$). This dependence of the zero-point voltage / current on the capacitance / inductance is worth noting considering the impedance of a transmission line is dependent on the ratio between the two ($Z_0 = \sqrt{L/C}$). Depending on the experiment being designed, it could be beneficial to modify the impedance of a resonator to increase the zero-point voltage or current. Note: The zero-point voltage/current for a distributed (TL) resonator is $\sqrt{2}$ greater than that of a lumped circuit resonator [102].

Now all of this analysis is for a discrete lumped LC resonator, yet the circuits for this (and most other) work are finite length transmission lines. Although it is more accurate to solve these systems again from scratch through the Lagrangian as either a chain of LC resonators [101, 103], a position dependent flux variable [100], or from the Heisenberg picture of the voltage and current [102], one can simply recognize that such a resonator consists of multiple modes. For a $\lambda/2$ resonator, the resonant frequencies are $\omega_n = nf_0\pi/l$ where $f_0 = 1/\sqrt{L_{dx}C_{dx}}$ and l is the physical

length of the resonator. With this in mind one can modify Eq. 3.12 to account for the additional modes resulting in

$$\hat{H}_{LC} = \hbar \sum_{n} \omega_n \left(\hat{a}_n^\dagger \hat{a}_n + \frac{1}{2} \right) \tag{3.17}$$

though as we tend to only be interested in the fundamental frequency ($n = 1$), in the ideal lossless case, this can be further simplified to once again be identical to Eq. 3.12.

3.3.1 Quantized Cavity

The Hamiltonian of a vacuum cavity can be derived by considering the electric and magnetic fields for a given frequency, as is derived in [104], though given the Hamiltonian for an LC circuit has already previously been derived, it is relatively straightforward to simply use Eq. 2.29 and 2.30 to generate the equivalent circuit for each mode which leads to the resulting Hamiltonian being

$$\hat{H}_{LC_{nm\ell}} = \frac{1}{2} \frac{\varepsilon}{k_{nm\ell}^4 v_0} \hat{V}^2 + \frac{1}{2} \mu k_{nm\ell}^2 v_0 \hat{I}^2. \tag{3.18}$$

From this, the zero point voltage of the cavity can be derived with Eq. 3.16

$$V_0 = \sqrt{\frac{\hbar 2\pi f k_{nm\ell}^4 v_0}{2\varepsilon}}. \tag{3.19}$$

The zero point electric field, E_0, of said cavity can then be found from

$$\frac{1}{2} C V_0^2 = \frac{1}{2\varepsilon} E_0^2 v_0 \Rightarrow E_0 = \sqrt{\frac{\hbar 2\pi f \varepsilon}{2 v_0}}. \tag{3.20}$$

This equation seems to only be valid up to the sub-IR range.

3.4 Superconducting Xmon Transmon

There are, in essence, three primary types of superconducting qubits, charge [28], phase [105] and flux [106]. From these a number of hybrid superconducting qubits have been developed, such as the transmon which is what is used in this work (more specifically the Xmon transmon). The transmon, as developed by Koch in the Schoelkopf group [30], is based off the charge qubit

[cooper pair box (CPB)] but with a much higher Josephson energy, E_{J}, to charging energy, E_{c}, ratio, $E_{\mathrm{J}}/E_{\mathrm{c}}$, in order to lower sensitivity to charge noise. The values of these are found from

$$E_{\mathrm{J}} = \frac{\Phi_0}{2\pi} I_0 = \frac{2\pi\hbar\Delta_0}{8e^2 R_{\mathrm{n}}} \tag{3.21}$$

$$E_{\mathrm{C}} = \frac{e^2}{2C_{\Sigma}} \tag{3.22}$$

where C_{Σ} is the total capacitance of the qubit (the 'X' island for the case of the Xmon transmon seen in Fig. 3.4), $\Phi_0 = \hbar\pi/e$ is the magnetic flux quantum, I_0/R_{n} is the critical current/normal state resistance of the Josephson junction and Δ_0 is the cooper pair band gap of the superconducting material. With $E_{\mathrm{J}}/E_{\mathrm{c}} < 1$, the qubit is operating in the CPB regime with Hamiltonian

$$\hat{H}_{\mathrm{CPB}} = 4E_{\mathrm{C}} \left(\hat{n} - n_{\mathrm{gate}}\right)^2 - E_{\mathrm{J}} \cos\left(\hat{\phi}_d(t)\right) \tag{3.23}$$

where $\hat{n}$ is the number of cooper pairs gained/lost by the island, n_{gate} is the reduced gate charge and $\hat{\phi}_d(t)$ is the gauge-invariant phase difference between the superconductors (Eq. 3). Analyzing the CPB Hamiltonian is useful as many derivations for it hold with the transmon. Such as how E_{J} can be modified when using a DC SQUID and introducing external flux (Φ) into the SQUID loop. The Hamiltonian for the Josephson component in this scenario becomes [107]

$$\hat{H}_{\mathrm{J}} = E_{\mathrm{J1}} \cos\left(\hat{\phi}_d(t)\right) - E_{\mathrm{J2}} \cos\left(\hat{\phi}_d(t) - 2\pi\Phi/\Phi_0\right) \tag{3.24}$$

since from flux quantization the phase difference can be written in terms of the flux passing through the SQUID [108], $E_{\mathrm{J1}}, E_{\mathrm{J2}}$ are the Josephson energies of each individual junction. Using some trigonometric substitutions this can be rewritten into the form

$$\hat{H}_{\mathrm{J}} = \left(E_{\mathrm{J1}} + E_{\mathrm{J2}}\right) \left|\cos\left(\pi\frac{\Phi}{\Phi_0}\right)\right| \sqrt{1 + d^2 \tan^2\left(\pi\frac{\Phi}{\Phi_0}\right)} \cos\left(\hat{\phi}_d(t) - \phi_0\right) \tag{3.25}$$

$$d = \frac{E_{\mathrm{J1}} - E_{\mathrm{J2}}}{E_{\mathrm{J1}} + E_{\mathrm{J2}}} \tag{3.26}$$

$$\tan\left(\phi_0\right) = d \tan\left(\pi\frac{\Phi}{\Phi_0}\right) \tag{3.27}$$

where d represents the difference in the two junctions. This difference can be intentional so as to have a tuning 'limit', or accidental due to fabrication errors. The constant magnetic flux ϕ_0, due to bias offset or external fields, can be eliminated by a shift of variables [30]. For very small d this simplifies to

$$E_{\mathrm{J}}(\Phi) = (E_{\mathrm{J1}} + E_{\mathrm{J2}}) \left|\cos\left(\pi \frac{\Phi}{\Phi_0}\right)\right| \tag{3.28}$$

Increasing the $E_{\mathrm{J}}/E_{\mathrm{C}}$ ratio takes us to the transmon regime, causing an exponential decrease of the charge dispersion such that no n_{gate} is necessary, as the transition frequency remains constant across all values of the gate voltage, as shown in Ref. [30]. The gain in charge-noise insensitivity is countered by a loss of anharmonicity, but is just an algebraic decrease. This allows an optimal point of operation where the transmon is charge noise insensitive yet still able to operate with fairly fast gates without risk of leakage.

Although we considered the transmon a variation of the CPB, it is no longer quite accurate to say the transmon state m is equivalent to the number of excess Cooper pairs present, since the transmon has slightly shifted from the charge regime into the phase regime. As shown in Ref. [30], a variable number of cooper pairs will be present on the charge island for a given state dependent on the $E_{\mathrm{J}}/E_{\mathrm{C}}$ ratio, the eigenstates of the transmon are no longer pure charge states.

The transmon Hamiltonian becomes rather more complex than the CPB because of this, and it is inappropriate to treat it as simply a two level system. Analytical solutions of the energy levels can be achieved in the phase basis using special Mathieu's functions, though for simple design purposes it is accurate enough to use a perturbative approach treating the transmon as an anharmonic oscillator. Taking an expansion of the $\cos(\hat{\phi}_d(t)$ term for small angles the Hamiltonian can be put in the form of a Duffing oscillator [30]

$$\hat{H}_{\mathrm{pt}} = \sqrt{8E_{\mathrm{C}}E_{\mathrm{J}}}\left(\hat{b}^\dagger\hat{b} + 1/2\right) - E_{\mathrm{J}} - \frac{E_{\mathrm{C}}}{12}\left(\hat{b} + \hat{b}^\dagger\right)^4 \tag{3.29}$$

from which the energy for state m is found to be

$$E_m \simeq \sqrt{8E_{\mathrm{C}}E_{\mathrm{J}}}\,(m + 1/2) - E_{\mathrm{J}} - \frac{E_{\mathrm{C}}}{12}\left(6m^2 + 6m + 3\right) \tag{3.30}$$

which results in the first few energy levels being

$$\begin{aligned} E_0 &\simeq \sqrt{8E_{\mathrm{C}}E_{\mathrm{J}}}\,(1/2) - E_{\mathrm{J}} - \tfrac{E_{\mathrm{C}}}{4} & E_{01} &\simeq \sqrt{8E_{\mathrm{C}}E_{\mathrm{J}}} - E_{\mathrm{C}} \\ E_1 &\simeq \sqrt{8E_{\mathrm{C}}E_{\mathrm{J}}}\,(3/2) - E_{\mathrm{J}} - \tfrac{15E_{\mathrm{C}}}{12} & E_{12} &\simeq \sqrt{8E_{\mathrm{C}}E_{\mathrm{J}}} - 2E_{\mathrm{C}} \\ E_2 &\simeq \sqrt{8E_{\mathrm{C}}E_{\mathrm{J}}}\,(5/2) - E_{\mathrm{J}} - \tfrac{39E_{\mathrm{C}}}{12} & & \end{aligned} \tag{3.31}$$

Where we can see that the frequency for this "oscillator" is $\sqrt{8E_{\mathrm{C}}E_{\mathrm{J}}}$ with an anharmonicity of E_{C}. The transmon can then be designed with a target frequency, $f_{01} = E_{01}/(2\pi\hbar)$, and anharmonicity, $\Delta f = E_{\mathrm{C}}$, through the correct choosing of the qubit capacitance and the critical current or normal state resistance of the junction. The capacitance for the Xmon (which is the form of the transmon used in this work, as seen in Fig. 3.4) is very straight forward to calculate as it is simply a cross formed by two intersecting CPW TLs. As the shunt capacitance of this island is multiple orders of magnitude greater than any of the capacitive coupling or the junction capacitance, it can be the sole value taken to determine E_{C}, where $C_{\Sigma} = 4C_{dx}l$, l being the length of an "arm" of the Xmon and C_{dx} is the transmission line capacitance as determined in Sec. 2.1.

3.5 Jaynes-Cummings Model

The interaction between qubits and resonant systems, be they wanted or unwanted, is commonplace in implementations of superconducting quantum computing. The simple case, one qubit and one resonant mode, has the known Jaynes-Cummings Hamiltonian of [29]

$$\hat{H}_{\mathrm{JC}} = \hat{H}_{\mathrm{r}} + \hat{H}_{\mathrm{q}} + \hat{H}_{\mathrm{int}} \tag{3.32}$$

where H_{int} is the Hamiltonian representing the interaction between the two. It can be more straightforward to analyze the Hamiltonian in the interaction picture

$$\hat{\tilde{H}}_{\mathrm{JC}} = 2\pi\hbar\frac{g}{2}\left(\hat{a}^{\dagger}\hat{\sigma}^{-}\mathrm{e}^{j2\pi\Delta t} + \hat{a}\hat{\sigma}^{+}\mathrm{e}^{-j2\pi\Delta t}\right), \tag{3.33}$$

where g is the coupling rate between the qubit and the resonant mode, $\hat{a}^{\dagger}$ / $\hat{a}$ are the electromagnetic field creation / annihilation operators of the resonant mode (such as Eq. 3.8 / 3.9) and $\hat{\sigma}^{-}$ and $\hat{\sigma}^{+}$ are the lowering and raising operators acting on the energy ground state $|\mathrm{g}\rangle$ and excited state $|\mathrm{e}\rangle$ of the qubit as discussed previously. $\Delta = f_{\mathrm{r}} - f_{\mathrm{q}}$ is the detuning between the resonator and the qubit. The fast rotating terms, $\pm(f_{\mathrm{r}} + f_{\mathrm{q}})$, are discarded due to the rotating wave approximation.

What determines the coupling rate g is dependent on the system and manner in which the two are coupled. For example, if the resonant mode is that of a cavity, and the interaction Hamiltonian is that of an electric-dipole, the coupling rate is $g = E_0 p_q/h$ assuming the qubit is at the modes antinode and has effective electric dipole moment p_{q}, where E_0 is found from Eq. 3.20.

When the cavity-qubit system is prepared in the one excitation sector, the first two energy eigenstates or *dressed states* of the system are obtained from the exact diagonalization of $\hat{H}_{\mathrm{JC}}$ [29],

$$|0,-\rangle = \cos\left(\frac{\theta_0}{2}\right)|1,\mathrm{g}\rangle - \sin\left(\frac{\theta_0}{2}\right)|0,\mathrm{e}\rangle\ , \tag{3.34}$$

$$|0,+\rangle = \sin\left(\frac{\theta_0}{2}\right)|1,\mathrm{g}\rangle + \cos\left(\frac{\theta_0}{2}\right)|0,\mathrm{e}\rangle\ . \tag{3.35}$$

where $\theta_0 = \arctan(g/\Delta)$. The states $|1,\mathrm{g}\rangle$ and $|0,\mathrm{e}\rangle$ are called *bright states* of the Jaynes-Cummings model, whereas state $|0,\mathrm{g}\rangle$ is a *dark state*.

The energy eigenvalues associated with Eq. 3.34 and 3.35 are given by

$$E_{0,\pm} = 2\pi\hbar f_\mathrm{r} \pm 2\pi\hbar\alpha_0\,, \tag{3.36}$$

where $\alpha_0 = \sqrt{g^2+\Delta^2}/2$. The energy eigenvalue for $|0,\mathrm{g}\rangle$, being the vacuum state, is $E_{0,\mathrm{g}} = 2\pi\hbar\Delta/2$.

Considering this system in the Schrödinger picture, the time evolution of a general cavity-qubit state can be written as

$$|\psi(t)\rangle = \mathrm{e}^{-j\pi f_\mathrm{c} t} \quad \Big[\cos\left(\tfrac{\theta_0}{2}\right)|0,+\rangle\,\mathrm{e}^{-j\alpha_0 t} - \sin\left(\tfrac{\theta_0}{2}\right)|0,-\rangle\,\mathrm{e}^{+j\alpha_0 t}\Big]\,. \tag{3.37}$$

3.5.1 Computational and Leakage Subspace

In a quantum computer, the Hilbert space of all qubits and any other internal auxiliary system required to operate them is defined as the *computational subspace*. The space associated with any external system interacting with the qubits is called the *leakage subspace* [69]. In general, the time evolution of a qubit interacting with internal and external systems is described by the combination of a purely unitary generator $\mathcal{H}$ and a purely dissipative generator $\mathcal{D}$ [69, 109].

The generator $\mathcal{H}$ accounts for the qubit Hamiltonian as well as the Hamiltonian of any wanted or unwanted internal or external system, or both. External systems always lead to unwanted dynamics, which causes qubit errors, whereas only unwanted internal systems generate qubit errors. The purely unitary nature of $\mathcal{H}$ results in coherent dynamics, implying that all the errors associated with it are *coherent errors*. In particular, errors due to external systems are called *coherent leakage errors*. The generator $\mathcal{D}$, instead, describes external environments acting as stochastic phenomena (e.g., Markovian noise). Therefore, the qubit errors associated with $\mathcal{D}$ are defined as *incoherent leakage errors*; these errors are typically due to qubit decoherence, i.e., relaxation and dephasing [42, 45]. Note that two- or multi-qubit *correlated errors* can also exist [66]. In this case, when an error occurs on one qubit it affects one or more different qubits in the quantum computer. Correlated errors can stem from either coherent or incoherent dynamics.

In superconducting qubit implementations, a typical example of a wanted internal system is a resonator acting as a quantum bus between pairs of qubits [77]. The states of the bus are populated during computations, although at the end of any computation only qubits' states should remain populated. A special class of wanted internal systems is represented by the driving of classical electromagnetic fields to control and measure the qubit's state. These systems result in unwanted dynamics when leading to stray fields that act on undesired qubits [110]. An example of an external system, instead, is a cavity mode due to the box used to house a superconducting qubit device. This mode can also generate correlated errors between a pair of qubits that interact with it independently.

Considering the interaction between one unwanted cavity mode and one qubit, the unitary generator can be written as $\mathcal{H}_{\mathrm{JC}} = -j[\hat{H}_{\mathrm{JC}}, \hat{\rho}]$, where $\hat{H}_{\mathrm{JC}}$ is the Jaynes-Cummings Hamiltonian [29], $\hat{\rho}$ is the cavity-qubit density matrix, and $j^2 = -1$; the generator $\mathcal{D}$ accounts for cavity and qubit decoherence. The time evolution of $(\mathcal{H}_{\mathrm{JC}} + \mathcal{D})$ can lead to leakage errors. In this case, the interplay between the coherent and incoherent error regimes is dictated by: The cavity-qubit coupling rate g; the detuning between the qubit with transition frequency f_{q} and the cavity mode with resonance frequency f_{c}, $\Delta = (f_{\mathrm{c}} - f_{\mathrm{q}})$; the cavity damping rate κ and the qubit relaxation and dephasing rates γ_{r} and γ_{d}, respectively.

3.6 The Xmon Transmon Circuit Design

From this analysis, we are then able to design qubits and relevant circuits to meet the requirements for a variety of experiments. For the purpose of characterizing the viability of using our three-dimensional wires for qubit measurements, we wanted to minimize the number of unknown variables outside of wire performance. We decided to attempt to mimic the qubit designs implemented by the Google/UCSB group, as presented in Ref. [31] and [65]. Not all of the qubit design parameters were available and there would of course be some inherent variances due to differences in fabrication processes. Even so, avoiding any novelty with the qubit design allows for recognizing if changes in relevant metrics are due to our wiring and packaging methodology. Although there were a number of iterations on the designs of the qubit chips, only the most recent and successful are reported below.

The design process for qubit circuits must consider the overall circuit layout in order to accurately reach desired operating parameters. Individual circuits can be considered in isolation in order to determine initial values, but will require modifying once implemented in the overall circuit design. As seen in Fig. 3.4, the qubit chip reported on in this section comprises two qubits (isolated from each other). Each having an XY-line, Z-line and a $\lambda/4$ readout resonator. Each readout resonator is shunted off of a readout transmission line. There are additional test resonators shunted off of the measurement line in order to test the quality factors of the resonators

without any Josephson junctions being present. Each line is connected to a contact pad at the chip edge following the designs presented in Sec. 4.1. The edges of the chip include numerous test pads for measuring the R_n of DC-SQUIDS which matched the design of the DC-SQUIDS used for our Xmon transmons.

The qubits were designed to have an unbiased frequency of $f_{01} = 6\,\text{GHz}$ and an anharmonicity of $\Delta f = 200\,\text{MHz}$. Although initial designs included a variety of qubit parameters on each chip, it was decided to have both be set to the same values for simplicity of fabrication and analysis of junction fabrication consistency. These target values translate to specific E_J and E_C, derived from Eq. 3.31. In turn, these values translate to the necessary R_n and C_Σ required, respectively, derived from Eq. 3.21 and 3.22.

The design for a particular R_n is more so a fabrication problem, and will be covered in greater depth in future work from Carolyn Earnest. The required C_Σ however, can be easily reached through a careful design and simulation process. The total capacitance the qubit experiences is dominated by the shunt capacitance to ground of the Xmon island, and can be analytically determined as explained at the end of Subsec. 3.4. As stated, it is a simplified approach, and simulations of the resulting circuit are required to have the precise capacitance that is desired. This simulation should include all other circuits that will be near or intentionally coupled to the Xmon, such as the readout resonator or Z-line[1].

As such, the designs for these components must be determined. For these chips, we targeted a mutual inductive coupling between the Z-line and the DC-SQUID of $M = 3\,\text{pH}$, resulting in a bias current of $\approx 350\,\mu\text{A}$ for a half flux quantum. The geometry necessary to achieve such a mutual inductance was determined through simulations in FastHenry, specifically the version modified by Whiteley Research Incorporated to allow for analysis of superconducting materials. It should be noted this circuit design is more of a "galvanic" coupling which gives an effective mutual inductance, as the DC-SQUID loop is partially composed of ground plane which is directly shared by the Z-line. The resulting DC-SQUID shape and Z-line can be seen in Fig. 3.4(b). The coupling between the XY-line and Xmon transmon was set to $\approx 100\,\text{aF}$, based on parameters from [65].

The left and right readout resonators were designed for f_r of 5.3 GHz and 5.8 GHz respectively, with coupling to the Xmon transmon of $g = 50\,\text{MHz}$. These were chosen to attempt to optimize qubit spectroscopy measurements, so as to easily measure anti-crossings. The required resonator length, $l_{1/4}$ is found from Eq. 2.22, which then allows the total isolated shunt capacitance, $C_r = C_{dx} * l_{1/4}$, for the resonator to be calculated from Eq. 2.1. The resonators zero-point voltage, V_0, can then be determined from Eq. 3.16. Using this and the previously determined values, the

[1]The capacitance due to the Josephson junctions themselves were not simulated, but taken into consideration when simulating the C_Σ due to the classical circuitry. The final geometries of the junctions were unknown, so an estimate based on reported designs was used.

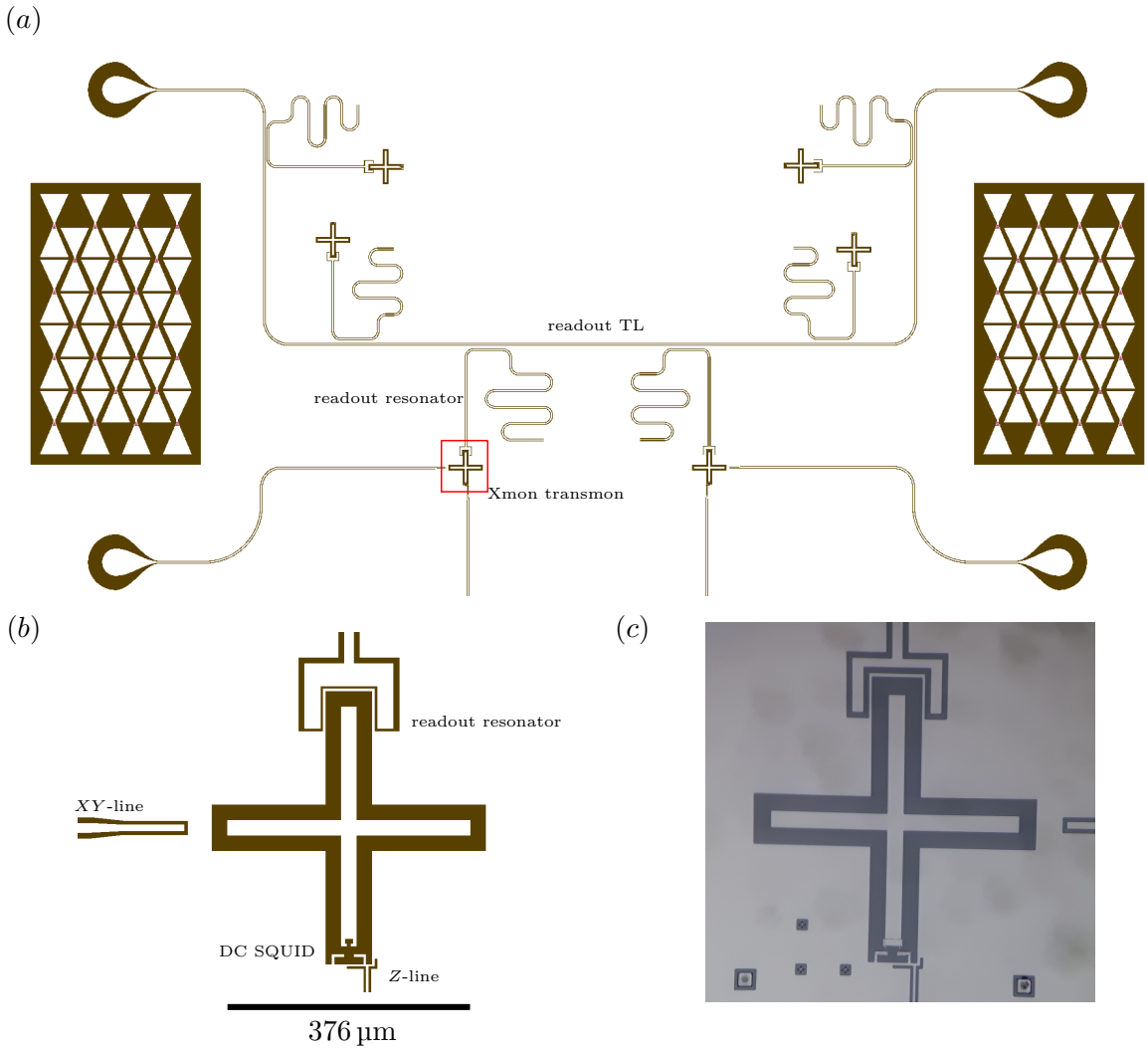

Figure 3.4: Current design for a 2 Xmon transmon qubit chip. Images are negatives, black being the exposed dielectric, white the conductive thin film. North refers to the top of the page. (a) Four contact pads are seen at the chip edges (two remaining are cutoff from the image to the south). The northern two connect the readout TL on which 6 $\lambda/4$ resonators are capacitively shunted. The two southern most resonators are capacitively coupled to two isolated Xmon transmon qubits. The remaining four are capacitively coupled to isolated sections of ground without any Josephson junctions present. The two contact pads at the equator connect to seperate TLs for X/Y signals. (b) The Xmon transmon, highlighted in red in (a), with capacitive coupling to the readout resonator (top), XY-line (left) and mutual inductive coupling to the Z-line (bottom). (c) A previous design which had been fabricated, thin film Al on Si. A noticeably smaller coupling strength to the readout resonator can be seen at the top. Inconsistencies with junction fabrication lead to the slight changes seen at the southern section of the Xmon island in (b).

Parameter	Analytical (Simulated)
E_{J}	1.591E-23 J
E_{C}	1.325E-25 J
R_{n}	11.03 kΩ
C_{Σ}	96.85 fF
X-island Arm Length, Width, Gap	180(188) µm, 24 µm, 24 µm
Resonator Frequency	5.3 GHz
Resonator Length, Width, Gap	5593(5415) µm, 15 µm, 9 µm
C_{g}	3.57 fF
C_{XY}	≈ 100 aF
C_{κ}	≈ 16(12) fF

Table 3.1: List of parameters for the Xmon transmon qubit coupled to the 5.3 GHz readout resonator. Parameter values found from simulations are indicated in parentheses.

capacitive coupling necessary for the desired g between the resonator and Xmon transmon was found from [30]

$$C_{\mathrm{g}} = \frac{C_{\Sigma}\ g\ 2\pi\hbar}{\sqrt{2}\ V_0\ e}\left(\frac{E_{\mathrm{J}}}{8E_{\mathrm{C}}}\right)^{\frac{1}{4}}. \tag{3.38}$$

The necessary coupling rate between the readout resonator and the readout transmission line was determined using Ref. [54]. Although our design currently does not have a Purcell filter, it was considered a reasonable starting point for settling on the resonator leakage rate. An approximate value of $\kappa_r = 25$ MHz was chosen, with the necessary capacitance being determined from Ref. [102] and confirmed against previous resonator measurements. The resonator's capacitive coupling to the TL not being at the resonator's voltage antinode will impact the coupling strength. This was accounted for by increasing the capacitive coupling to account for the slight drop in voltage at the coupling location.

These capacitive couplings of course result in an increase to the electrical length of the resonator. As such, the length of the resonators must be shortened to retain the desired resonance frequency, which in turn will change the resonator's zero point voltage and therefore impact the capacitance necessary for the desired coupling. To reach the desired values self consistent formula are required, but practically overkill given the relatively low coupling strengths being employed for this work and that the designs will need further simulations and modifications. Still, two iterations were run numerically to determine the design parameters before simulation.

The design values, as shown in Table 3.1, were used to generate models for simulation in HFSS and Q3D of ANSYS Electronics Desktop. These were fully parametrized models so as to allow

for quick and easy modification to meet any required design parameters. The various capacitive couplings and C_Σ were finalized in Q3D using the full circuit model, so as to attempt to account for all stray capacitances. Once the geometries for desired capacitances were finalized, the model was then simulated in HFSS using the eigenmode solution type to set the correct length of the readout resonators while coupled. This would lead to a further change in resonator length, in turn causing a change to the resonators zero-point voltage and necessary capacitance for the desired coupling rate to the qubit and transmission line. As such, a couple iterations of this process were ran in order to reach the desired operating parameters. These models were then exported into L-Edit for use in the mask design.

3.7 Conclusion

A very brief review of the theoretical qubit and basic qubit gates was presented so that the reader understood some necessary jargon. The surface code was also briefly presented so that the reader could understand why scaling of a qubit system is a growing concern, and how near term future functional qubit systems would be designed.

Such a system makes use of superconducting resonators as couplers or busses. For this, the LC resonator was quantized and the zero point voltage was derived, as this value is necessary for determining the coupling strength between a qubit and resonator. The microwave cavity was also quantized so as to determine the coupling strength between a cavity and qubit, as shown through the analysis of the Jaynes-Cummings model in the single excitation regime. This provides a means to determine leakage error rates as discussed here and later calculated in Chapter 5.

A guide on the design of an Xmon transmon qubit system, as seen in Fig. 3.4, is presented with focus on numerical real world values following the most recent successful design. These values were generated once again through Matlab code and then modeled in simulation software where possible to confirm the desired values were reached.

This and the previous chapter has covered the necessary theory by which to analyze the scaling solutions provided in the following two chapters. Chapter 4, the solution to the wiring problem, relies primarily on classical microwave design and analysis, using low power resonator measurements as a rough 'measuring stick' by which to determine the potential qubit performance. Chapter 5, the solution to coherent leakage error, relies more so on the material of this chapter, numerically simulating qubit-resonator coupling in order to derive the relevant error rate.

Chapter 4

The Quantum Socket

This chapter is based on the work presented in Ref. [1][1], of which the contributions of the authors is stated in the Statement of Contributions at the start of this thesis. Any components of Ref. [1] which the author of this thesis was not involved in has been excluded from this work. Some new material has been added where relevant.

The wiring problem is one which numerous research groups are currently trying to solve, be it with wafer bonding techniques [58, 59, 60, 61, 62] or coaxial through-chip vias [63, 70, 73]. Our proposal, as discussed in this chapter, is the quantum socket, a microwave packaging system which makes use of three-dimensional wires.

In Sec. 4.1 we present the design of three-dimensional wires, the microwave package and simulations of these designs to predict their microwave behaviour. The implementation of these designs is covered in Sec. 4.2, analyzing the magnetic, thermal and mechanical properties. The quantum socket is then characterized in both DC and microwave frequencies in Sec. 4.3, covering the standard operational ranges of the Xmon transmon qubit. Finally, superconducting resonators are measured at low photon power in Sec. 4.4 , to determine the efficacy of using the quantum socket in a cryogenic environment for qubit operations.

4.1 Design

The development of the quantum socket required extensive micro-mechanical and microwave design and simulations. It was determined that a spring-loaded interconnect, the three-dimensional wire, was the optimal method to electrically connect circuitry on a lithographically fabricated

[1] ©American Physics Society 2016

chip [2] and operated in a cryogenic environment. Basing the interconnect on an already available product also allowed us to take advantage of the knowledge in the existing field of microwave circuit testing [111]. An on-chip contact pad geometrically and electrically matched to the bottom interface of the wire can be placed easily at any desired location on the chip as part of the fabrication process. The coaxial design of the wire provides a wide operating frequency bandwidth, while the springs allow for mechanical stress relief during the cooling process.

4.1.1 Three-dimensional wires

Figure 4.1 shows the design of the quantum socket components. Figure 4.1 (a) displays a model of a three-dimensional wire. The coaxial design of the wire is visible, having a length of 30.5 mm when uncompressed. The inner cylindrical pin has a diameter of 380 µm and an outer cylindrical body (the electrical ground) diameter of 1290 µm at its narrowest region which is referred to as the *contact head* (see the inset of Fig. 4.1 (a), as well as the dashed box on the left of Fig. 4.2 (a)). The contact head terminates at the wire *bottom interface*; to which on chip contact pads are designed to mate to (see Fig. 4.2 (b) and (c)). The outer body includes a rectangular aperture, the *tunnel*, to prevent shorting the inner conductor of an on-chip CPW TL. Two different tunnel dimensions were designed, for trying to optimize between impedance matching and potential alignment errors. The tunnel height was 300 µm in both cases, with a width of 500 µm or 650 µm. The internal spring mechanisms of the wire allows the contact head to be compressed with a maximum stroke of 2.5 mm, although limited to a working stroke of 2.0 mm.

The outer body of the three-dimensional wire is an M2.5 male thread used to fix the wire to the lid of the microwave package (see Fig. 4.1 (b) and (d)). The thread is split into two segments of length 3.75 mm and 11.75 mm that are separated by a constriction with outer diameter 1.90 mm. The constriction is necessary to assemble and maintain in place the inner components of the three-dimensional wire. A laser-printed marker is engraved into the top of the outer body which is aligned with the center of the tunnel. This allows mating the wire bottom interface with a pad on the underlying chip with a high degree of angular precision while the chip is enclosed inside the package.

Figure 4.2 (a) shows a lateral two-dimensional cut view of the three-dimensional wire. Two of the main wire components are the inner and outer barrel, which compose part of the inner and outer conductor. The inner conductor barrel is a hollow cylinder with outer and inner diameters of 380 µm and 290 µm (indicated as part iv in Fig. 4.2 (a)), respectively. This barrel encapsulates the inner conductor spring. The outer conductor barrel is a hollow cylinder as well, in this case with an inner diameter of 870 µm (parts ii and vii). Three polytetrafluoroethylene (PTFE) disks serve as spacers between the inner and outer conductor. The disks contribute minimally to the

[2] A typical chip comprises a dielectric substrate (e.g., silicon or sapphire) and a metallic surface.

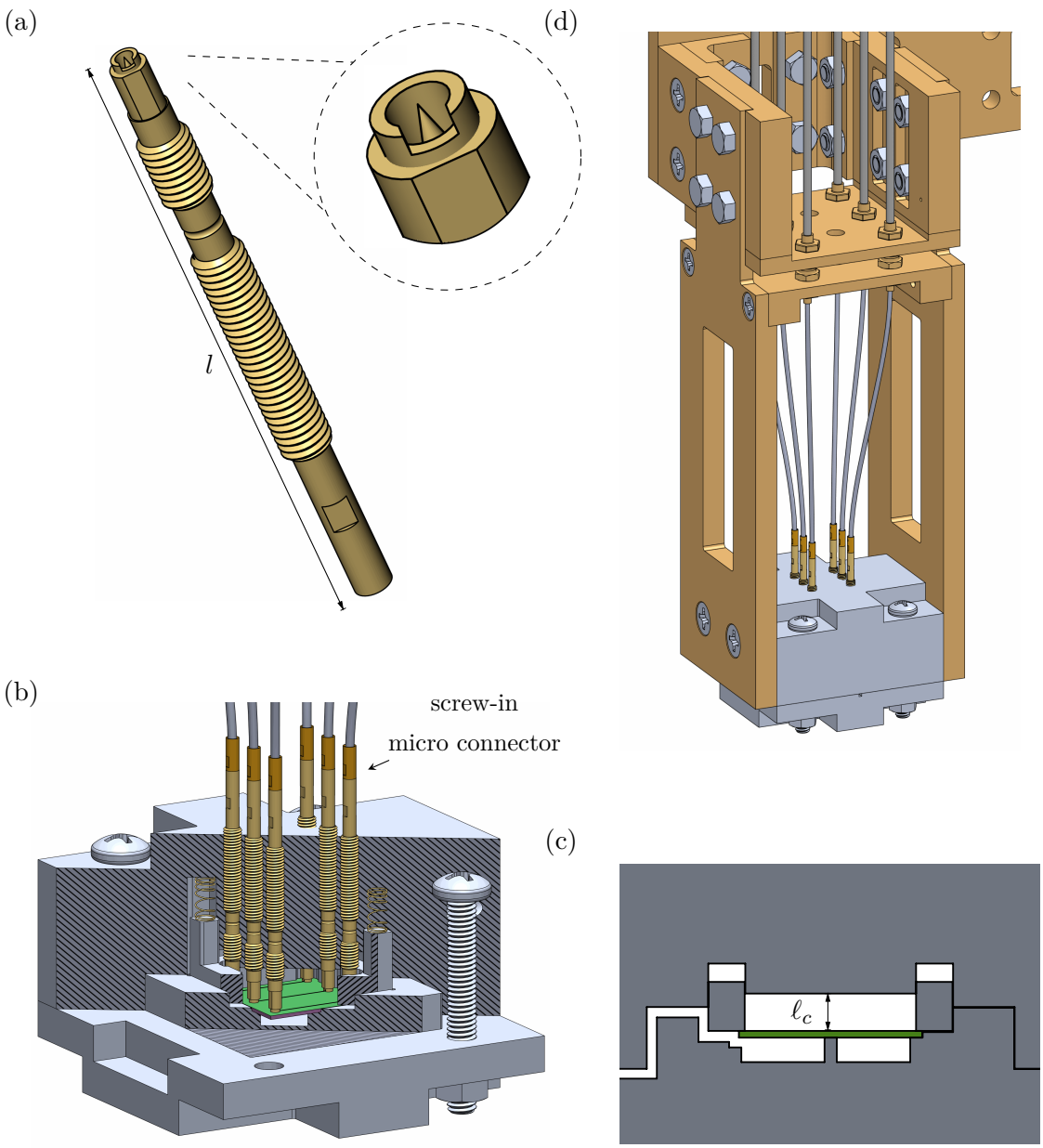

Figure 4.1: Computer-aided designs of the three-dimensional wire, microwave package, and package holder. (a) A wire of length $l = 30.5\,\text{mm}$ along with a detail of the contact head (inset). (b) Assembled microwave package including six three-dimensional wires, washer, washer springs, and chip (shown in green). The arrow indicates the screw-in micro connector on the back end of the wire. Forward hatching indicates the washer cutaway, whereas backward hatching indicates both lid and sample holder cutaways. (c) Cross section of the microwave package showing the height of the upper cavity, which coincides with the minimum compression distance of the three-dimensional wires. A channel with a cross-sectional area of $800\,\mu\text{m} \times 800\,\mu\text{m}$ connects the inner cavities of the package to the outside, thus making it possible to evacuate the inner compartments of the package. This channel meanders to prevent external electromagnetic radiation from interfering with the sample. (d) Microwave package mounted to the package holder, connected, in turn, to the mixing chamber plate of the dilution refrigerator with SMP connectors.

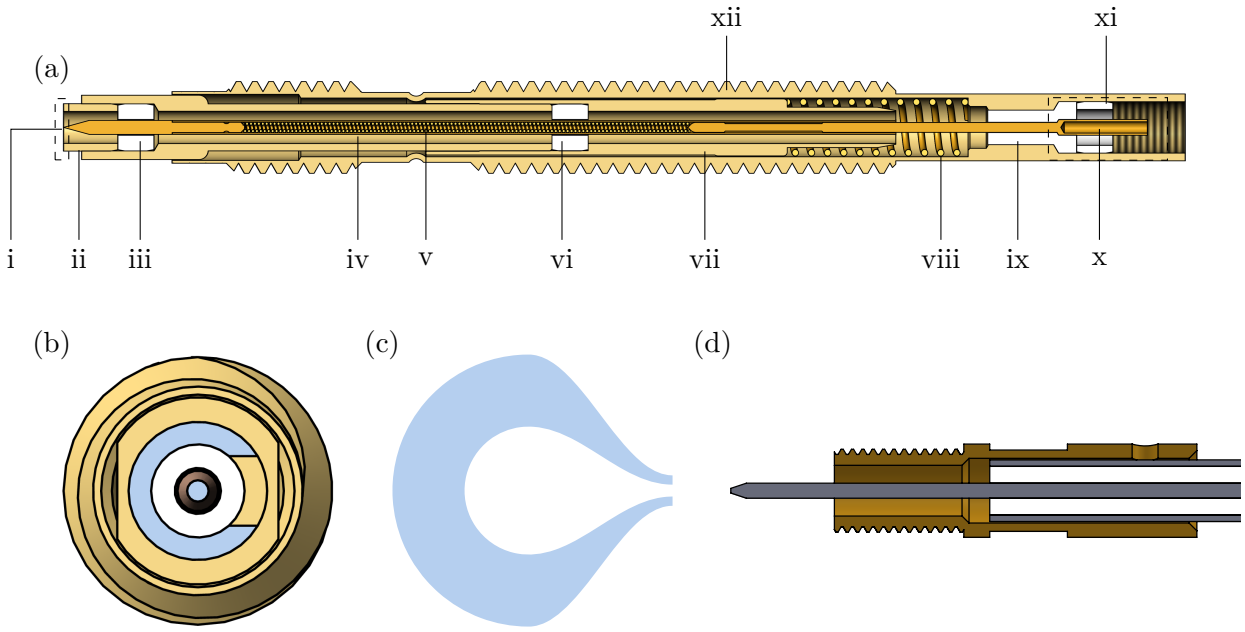

Figure 4.2: Two-dimensional cut view of the three-dimensional wire, contact pad, and screw-in micro connector. (a) Side view of the wire cross section. The wire components are: i, spring-loaded center conductor of the contact head; ii, spring-loaded outer conductor of the contact head; iii, vi, and ix, dielectric spacers; iv, center conductor barrel; v, center conductor spring; vii, outer conductor barrel; viii, outer conductor spring; x, center conductor tail; xi, outer conductor tail; xii, threaded outer body. The dashed box on the left indicates the contact head; that on the right indicates the female threads included for use with the screw-in micro connector. (b) Front view of the wire. The blue surface indicates the wire bottom interface of the contact head. (c) On-chip contact pad. Here the blue indicates exposed dielectric, with white being the conductive thin film. (d) Screw-in micro connector. The left end of the micro connector mates with the back end of the three-dimensional wire; the right end is soldered to a coaxial cable, the inner conductor of which serves as the inner conductor of the micro connector (slotting into x).

wire dielectric volume, the majority of which is air or vacuum. The outer spring is housed within the outer barrel towards its back end, just before the last PTFE disk on the right-hand side of the wire. The *back end* of the wire is a region comprising a female thread on the outer conductor and an inner conductor barrel (see dashed box on the right-hand side of Fig. 4.2 (a)).

The inner conductor tip is a cone with an opening angle of 30°. Such a sharp design was chosen to ensure that the tip would pierce through any possible oxide layer forming on the contact pad metallic surface, thus allowing for good electrical contact.

Figure 4.2 (c) shows the design of a typical on-chip pad used to make contact with the bottom interface of a three-dimensional wire. The pad comprises an inner and outer conductor, with the outer conductor being grounded. The pad in the figure was designed for a silver (Ag) film of thickness 3 µm. A variety of similar pads were designed for gold (Au) and aluminum (Al) films with thickness ranging between approximately 100 nm and 200 nm. The pad inner conductor (for

the Ag film) is a circle with diameter 320 µm that narrows to a CPW TL by means of a raised-cosine taper. The raised cosine makes it possible to maximize the pad area, while minimizing impedance mismatch. As designed, the wire and pad allow for lateral and rotational misalignment of ∓ 140 µm and $\mp 28°$, respectively. The substrate underneath the pad is assumed to be silicon (Si) with a relative permittivity $\epsilon_r \simeq 11$. The dielectric gap between the inner and outer conductor is 180 µm in the circular region of the pad; the outer edge of the dielectric gap then follows a similar raised-cosine taper as the inner conductor. The pad characteristic impedance is designed to be $Z_0 = 50\,\Omega$.

4.1.2 Microwave package

The microwave package comprises three main parts: The lid, the sample holder, and the grounding washer. The package is a parallelepiped with a height of 30 mm and with a square base of side length 50 mm. All these components, with the chip being housed in the sample holder, mate as shown in Fig. 4.1 (b) and (c).

In order to connect a three-dimensional wire to a device on a chip, the wire is screwed into an M2.5 female thread that is tapped into the lid of the microwave package, as depicted in Fig. 4.1 (b). The contact force between the wire and the thin film on chip is set by the depth of the wire in the package, in essence the pressure the wires springs are exerting to the chip. This depth depends on the number of rotations used to screw the wire into the M2.5-threaded hole of the lid. Since the wire's tunnel has to be aligned with the corresponding on-chip pad, a discrete number of wire pressure settings are allowed. The optimal installation depth of the wire was determined from a variety of tests, discussed in Sec. 4.2.3. In the present implementation of the quantum socket, the lid is designed to hold a set of six three-dimensional wires, which are arranged in two parallel rows. In each row, the wires are spaced 5.75 mm center to center, with the two rows being separated by a distance of 11.5 mm.

A square chip of lateral dimensions 15 mm × 15 mm is mounted in the sample holder in a similar fashion as in Ref. [112]. The outer edges of the chip rest on four protruding lips, which are 1 mm wide. Hereafter, those lips will be referred to as the *chip recess*. The chip recess is designed so that the top of the chip protrudes by approximately 100 µm with respect to the adjacent surface of the chip holder to insure the grounding washer makes contact with the chip surface. Assuming a chip thickness of 550 µm, the depth of the recess is set to 450 µm (see Fig. 4.1 (c)).

The grounding washer was designed to substitute the large number of lateral bonding wires that would otherwise be required to provide a good ground to the chip (as shown, for example, in Fig. 6 of Ref. [112]). The washer springs are visible in Fig. 4.1 (b), which also shows a cut view of the washer. The washer itself is electrically grounded by means of the springs as well as through galvanic connection to the surface of the lid. The length of the four feet of the washer, which

can be seen in the cut view of Fig. 4.1 (b), can be modified to vary the contact force between the washer and the thin film.

After assembling the package, there exist two electrical cavities (see Fig. 4.1 (c)): One above the chip, formed by the lid, washer, and metallic surface of the chip (*upper cavity*), and one below the chip, formed by the sample holder and metallic surface of the chip (*lower cavity*), each having multiple cavity resonant modes. The hollow cavity above the chip surface has dimensions 14 mm × 14 mm × 3.05 mm. The dimensions of the cavity below the chip surface are 13 mm × 13 mm × 2 mm [3]. The lower cavity of air or vacuum helps to mitigate any parasitic capacitance between the chip and the package holder. Additionally, it serves to lower the effective permittivity in the region below the chip surface, increasing the frequency of the substrate modes (see Subsec. 4.1.3 and 2.2.3).

A pillar of square cross section with side length of 1 mm is present in the center of the lower cavity, with height of 2 mm, providing mechanical support to the chip [4]. The impact of such a pillar on the microwave performance of the package is discussed in Subsec. 4.1.3.

4.1.3 Microwave simulations

The three-dimensional wires, the 90° transition between the wire and the on-chip pad as well as the inner cavities of a fully-assembled microwave package were extensively simulated numerically at microwave frequencies [5]. The results for the electromagnetic field distribution at a frequency of approximately 6 GHz, which is a typical operation frequency for superconducting qubits, are shown in Fig. 4.3. Figure 4.3 (a) shows the field behavior for a bare three-dimensional wire. The field distribution resembles that of a coaxial transmission line except for noticeable perturbations at the dielectric PTFE spacers. The perturbations were minimal so did not suggest they would be significant reflection planes. Figure 4.3 (b) shows the 90° transition region. This is a critical region for signal integrity since abrupt changes in physical geometry are likely to cause electrical reflections [80, 111]. The impedance matched contact pad and tapering is designed to help minimize the impact of this abrupt change, however, this leads to a large electromagnetic volume in proximity of the pad, as seen in Fig. 4.3 (b). This could possibly result in parasitic capacitance and undesirable crosstalk.

In addition to considering the wire and the transition region, the electrical behavior of the inner cavities of the package were studied analytically and simulated numerically. As described in Subsec. 4.1.2, the metallic surface of the chip effectively divides the cavity of the sample holder

[3] The small parallelepiped of the chips substrate also makes up a portion of the lower cavity.

[4] The pillar was included in the design as there was concern over potential damage to the large 15 mm × 15 mm substrates (particularly the Si ones) from mechanical strain due to the three-dimensional wires pushing on the top of the chip.

[5] The simulation software used was the High Frequency Structure Simulator (HFSS) by Ansys, Inc., which is now incorporated as part of Ansys Electronics Desktop

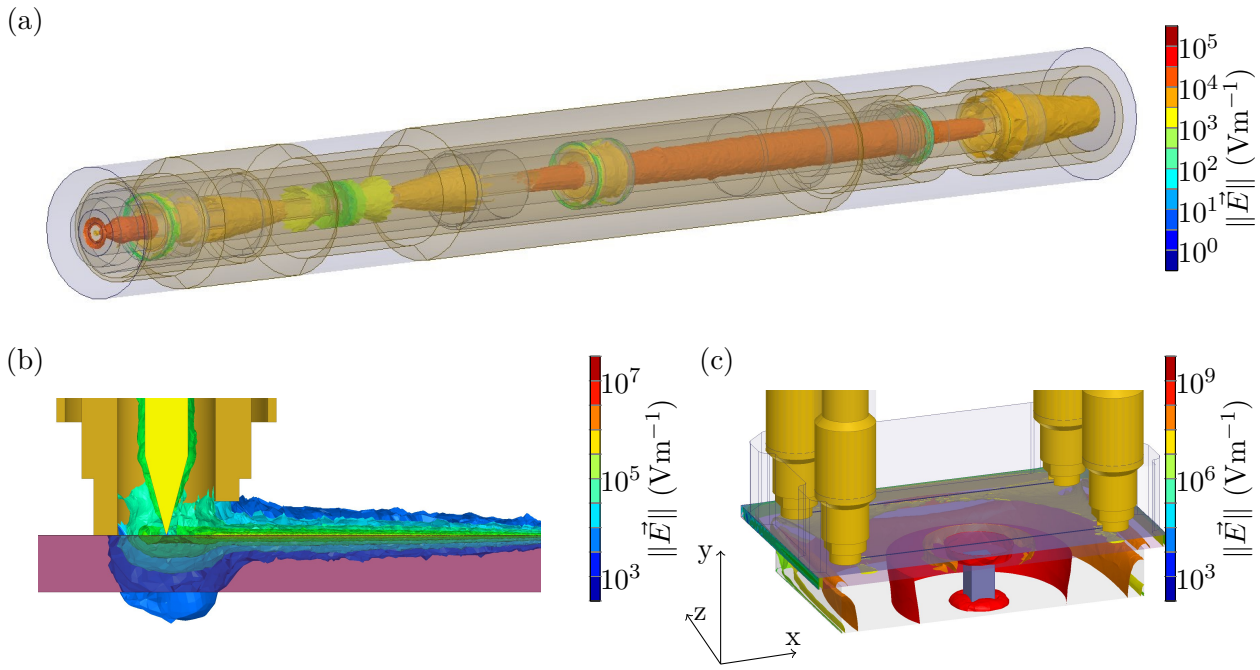

Figure 4.3: Numerical simulations of the electric field distribution. Color bar scales are indicated in their respective panels. (a) $||\vec{E}||$-field for a three-dimensional wire at 6 GHz. (b) Cross section of the $||\vec{E}||$-field of a transmitted signal at the 90° transition region between the three-dimensional wire and CPW TL (where the TL is parallel to the page continuing to the right), also at 6 GHz (c) $||\vec{E}||$-field for the first box mode at 6.3 GHz. Color bar scales are indicated in their respective panels. The x, y, and z directions of a Cartesian coordinate system are also indicated. An offset cross section of the first box mode is shown. The field confinement due to the pillar is clearly visible. There is also a slight field confinement in the region surrounding the chip recess.

into two regions: A vacuum cavity above the metal surface and a cavity partially filled with dielectric below the metal surface. The latter is of greatest concern as the dielectric acts as a perturbation to the cavity vacuum [6], thus lowering the box modes, as discussed in Subsec. 2.2.3. From Eq. 2.34, we estimated this box mode to be 12.8 GHz. However, considering the presence of the pillar, the three-dimensional wires and non-ideal cavity shape, we had to use numerical simulations to obtain a more accurate estimate of the lowest box modes. The results for the first three modes are reported in Table 4.1. Discounting the pillar, the analytical and simulated values are in good agreement with each other. The addition of the support pillar significantly lowers the frequency of the modes. In fact, it increases the relative filling factor of the cavity by confining more of the electromagnetic field to the dielectric than to vacuum for the first mode (and any other modes with antinodes at the pillar location). Given the dimensions of this design, the pillar leads to a first mode which could interfere with typical qubit frequencies. In spite of this, the pillar was included in the design in order provide a degree of mechanical support. Note that the pillar can alternatively be realized as a dielectric material and has been in future versions, e.g.,

[6] Provided the vacuum still constitutes the majority of the volume of the cavity.

Table 4.1: Simulation results for the first three box modes of the lower cavity inside the assembled microwave package shown in Fig. 4.1 (b). The dielectric used for these simulations was Si at room temperature with relative permittivity $\epsilon_r = 11.68$. "Vacuum" indicates that no Si is present in the simulation. "with pillar" indicates that the $1.0\,\text{mm} \times 1.0\,\text{mm} \times 2.0\,\text{mm}$ conductive support pillar is present. Note that the frequency of the first mode of the upper cavity is $\sim 17.2\,\text{GHz}$.

	TE_{110} (GHz)	TE_{120} (GHz)	TE_{210} (GHz)
Vacuum	15.7	24.2	24.2
Vacuum with pillar	13.1	23.6	23.6
Si	13.5	16.8	16.8
Si with pillar	6.3	16.2	16.9

PTFE; a dielectric pillar would no longer cause field confinement between the top surface of the pillar and the metallic surface of the chip and have fairly limited pertubative impact on the the given modes effective permittivity.

4.2 Implementation

The physical implementation of the main components of the quantum socket is displayed in Fig. 4.4. Figure 4.4 (a) shows a macro photograph of a three-dimensional wire. The inset shows a scanning electron microscope (SEM) image of the wire contact head, featuring the 500 µm version of the tunnel. This wire was cycled approximately ten times which resulted in the center conductor conical tip becoming flattened at the top. A slight buildup of on chip film material is also visible. The metallic components of the wire were made from bronze and brass (see Subsec. 4.2.1), and all springs from hardened beryllium copper (BeCu). Except for the springs, all components were gold plated without any nickel (Ni) adhesion underlayer. The wires were tested for reliability, finding a mean number of cycles before failure $> 100,000$.

Figure 4.4 (b) displays the entire microwave package in the process of locking the package lid and sample holder together, with a chip and grounding washer already installed. As shown in the figure, two rows of three-dimensional wires, for a total number of six wires, are screwed into the lid; each wire is associated with one on-chip CPW pad. The four springs that mate with the grounding washer feet are embedded in corresponding recesses in the lid. The springs for the washer are glued in these recesses by way of a medium-strength thread locker that was tested at low temperatures. Figure 4.4 (c) shows a picture of the assembled microwave package attached to the package holder; the entire structure can then be attached to the MC stage of our DR.

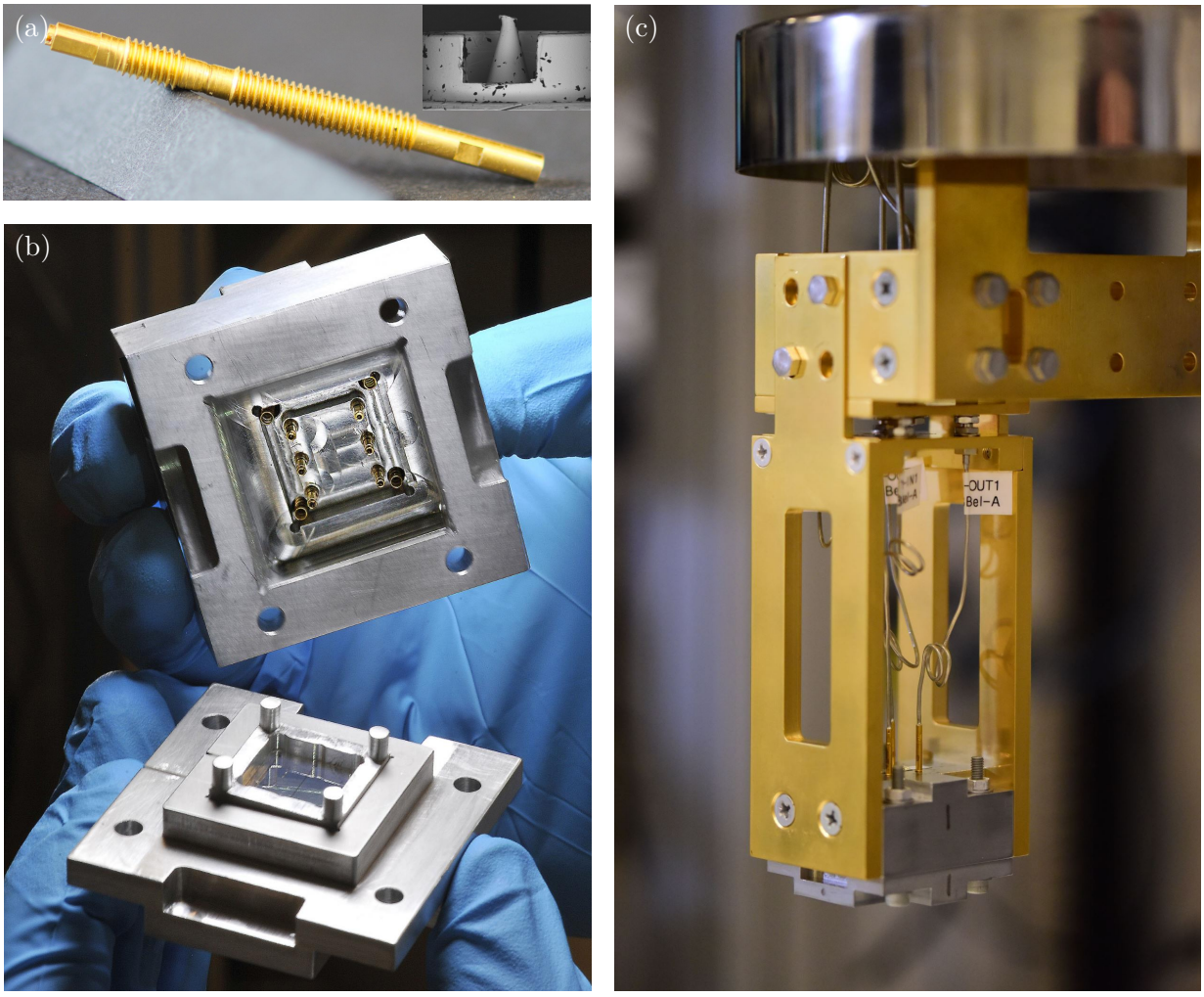

Figure 4.4: Images of the quantum socket as implemented. (a) Macro photograph of a three-dimensional wire; inset: SEM image of the contact head. The tip of the inner conductor shows some wear from multiple cycles and buildup of the on chip thin film. (b) Microwave package lid with six three-dimensional wires and four washer springs, washer, and sample holder with a chip installed. (c) Package holder with attached microwave package mounted to the MC stage of a DR. The top of the panel shows the lid of the custom made magnetic shield.

4.2.1 Magnetic properties

An important stage in the physical implementation of the quantum socket was the choice of materials to be used for the three-dimensional wires. In fact, it has been shown that non-magnetic components in proximity of superconducting qubits are critical to preserve long qubit coherence times [95, 113, 114, 115]. The three-dimensional wires are, in addition to the package, the closest devices to the qubits. For this reason, all their components should be made using non-magnetic materials. However due to machining constraints, alloys containing some ferromagnetic impurities (iron (Fe), cobalt (Co), and Ni) had to be used. For the outer conductor components brass was

used, as it is easy to thread [7]. For the inner conductor components, brass CW724R was unable to meet the stricter machining requirements. Consequently, we decided to use phosphor bronze [8].

The dielectric spacers were made from PTFE and the rest of the components from hardened BeCu as both materials are non-magnetic. The weight percentage of ferromagnetic materials is non-negligible for both CW453K and CW724R. Thus a series of tests were performed using a zero Gauss chamber (ZGC) in order to ensure both materials were sufficiently non-magnetic. The measurements suggested the wires would introduce unwanted flux into a near by qubit on the order of $0.1\%\Phi_0$ [1]. Although undesirable, it is small enough to not have significant impact for initial superconductive microwave and qubit measurements.

The grounding washer was made from high-purity Al alloy 5N5 (99.9995 % purity). The very low level of impurities in this alloy assures minimal stray magnetic fields generated by the washer itself, being measured at less than 10% the strength of the other materials.

4.2.2 Thermal properties

The thermal conductance of the three-dimensional wires is a significant characteristic for operations at cryogenic temperatures. Low thermal conductivity would result in poor cooling of the devices, which may lead to an incoherent thermal mixture of the qubit ground state $|\mathrm{g}\rangle$ and excited state $|\mathrm{e}\rangle$ [116]. Even a slightly mixed state would significantly deteriorate the fidelity of the operations required for QEC [66]. It has been estimated that some of the qubits in the experiment of Ref. [46], which relies solely on Al wire bonds as a means of thermalization, were in an excited state $P_\mathrm{e} \simeq 0.04$. Among other possible factors, it was thought that this was due to the poor thermal conductance of the Al wire bonds. As these bonds become superconductive at the desired qubit operation temperature of $\sim 10\,\mathrm{mK}$, their thermal conductivity becomes negligible, preventing the qubits from being initialized to $|\mathrm{g}\rangle$ with high fidelity.

In order to compare the thermal performance of an Al wire bond with that of a three-dimensional wire, we estimated the heat transfer rate per kelvin, Π_t, by using a simplified coaxial geometry. At a temperature of 25 mK, we calculated $\Pi_\mathrm{t} \simeq 6 \times 10^{-7}\,\mathrm{W\,K^{-1}}$. At the same temperature, the heat transfer rate per kelvin of a typical Al wire bound was estimated to be $\Pi_\mathrm{b} \simeq 4 \times 10^{-12}\,\mathrm{W\,K^{-1}}$. This numerous order of magnitudes difference between the two wiring methods suggests the three-dimensional wires can readily thermalize the qubit chip.

4.2.3 Spring characterization

Another critical step in the physical implementation of the quantum socket was to select springs for the wires and washer that provide reliable spring force at cryogenic temperatures. This

[7] The chosen type was CW724R, alloy 430, grade ISO CuZn21Si3P, UNS C69300.
[8] The chosen type was CW453K, grade DIN 2.1030 - CuSn8, UNS C52100.

force, in turn, determines the wire-chip contact resistance, which impacts the socket's DC and microwave performance. It was quickly determined that springs made from BeCu were required, as alternatives had risk of magnetic impurities, manufacturing issues, or poor cryogenic performance.

To characterize the springs, their compression was assessed at room temperature, in liquid nitrogen (i.e., at a temperature $T \simeq 77\,\mathrm{K}$), and in liquid helium ($T \simeq 4.2\,\mathrm{K}$). The spring performance at 4.2 K is expected to perform similarly at a temperature of 10 mK.

The three types of tested springs are called FE-113 225, FE-112 157, and FE-50 15 and their geometric characteristics are reported in Table 4.2. We ran temperature cycle tests by dunking the springs repeatedly in liquid nitrogen and then in liquid helium without any load. At the end of each cycle, we attempted to compress them at room temperature. We found no noticeable changes in mechanical performance after many cooling cycles. Subsequently, the springs were tested mechanically by compressing them while submerged in liquid nitrogen or helium. In these tests, we only studied compression forces because in the actual experiments the three-dimensional wires are compressed and not elongated.

The compression force was assessed by means of loading the springs with a mass. The weight of the mass that fully compressed the spring determined the spring compression force F_c. The compression force of each spring is reported in Table 4.2. We observed through these tests that the compression force is nearly independent of the spring temperature, increasing only slightly when submerged in liquid helium. Assuming an operating compression $\Delta L = 2.0\,\mathrm{mm}$, we expect a force between 0.5 N and 2.0 N for the inner conductor and between 2.0 N and 4.0 N for the outer conductor of a three-dimensional wire at a temperature of 10 mK. From these values, and further direct on chip measurements, we determined the optimal wire protrusion from the ceiling of the lid to be 4.45 mm. Spring model FE-113 225 was chosen for use with the grounding washer.

Table 4.2: Thermo-mechanical tests on hardened BeCu springs. In the table are reported: The outer diameter D of the coil forming the helix structure of the spring; the diameter d of the circular cross section of the spring (note that the smallest wire diameter is 150 µm); the spring free length L_f, i.e., the spring length at its relaxed position; the number of coils N_c; the spring force F_c (estimated from room temperature measurements).

Spring type	D (mm)	d (mm)	L_f (mm)	N_c (-)	F_c (N)
FE-113 225	2.30	0.26	11.55	11.25	~ 1.0
FE-112 157	1.30	0.22	18.00	42.00	~ 1.0
FE-50 15	0.60	0.15	31.75	150.00	~ 0.5

4.2.4 Alignment

To have reliable and consistent signal transmission, wire to pad alignment had to be insured. This became difficult due to the many stages in which errors harming alignment could occour. These errors are mainly due to: Dicing tolerances; tapping tolerances of the M2.5-threaded holes of the lid; tolerances of the mating parts for the inner cavities of the lid and sample holder and tolerances of the chip recess. These errors can cause both lateral and rotational misalignment and become likely worse when cooling the quantum socket to low temperatures.

The procedure to obtain an ideal and repeatable alignment comprises three main steps: Optimization of the contact pad and tunnel geometry, accurate and precise chip dicing, and accurate and precise package machining. For the quantum socket described in this work, the optimal tunnel width was found to be 650 µm. This maintained reasonable impedance matching, while allowing greater CPW contact pad and tapering dimensions. The contact pad width W_p and taper length T_p were chosen to be $W_\mathrm{p} = 320\,\mu\mathrm{m}$ and $T_\mathrm{p} = 360\,\mu\mathrm{m}$ for the Ag samples, and $W_\mathrm{p} = 330\,\mu\mathrm{m}$ and $T_\mathrm{p} = 520\,\mu\mathrm{m}$ for the Al samples. These are the maximum dimensions allowable that accommodate the geometry of the wire bottom interface for a nominal lateral and rotational misalignment of $\pm$ 140 µm and $\pm$ 28°, respectively.

In our initial design, a perfect match required that the die dimensions should be at most 1 thou smaller than the dimensions of the chip recess, as machined. In the case of the initial sample holder, the chip recess side lengths were 15.028(5) mm, 15.030(5) mm, 15.013(5) mm, and 15.026(5) mm. The initial samples were diced from a Si wafer using a dicing saw from DISCO, model DAD-2H/6, set to obtain a 15 mm × 15 mm die. Due to the saw inaccuracies, the actual die dimensions were 14.96(1) mm × 14.96(1) mm, significantly smaller than the chip recess dimensions. This caused the die to shift randomly between different mating instances, causing significant alignment errors.

This lead us to switching to the dicing saw model DAD3240, also from DISCO Corporation. To obtain the desired die length, both the precision of the saw stage movement and the blade's kerf had to be considered. For the DAD3240 saw, the former is $\sim 4\,\mu\mathrm{m}$, whereas the latter changes with usage and materials. For the highest accuracy cut, we measured the kerf on the same type of wafer just prior to cutting the actual die. Additionally, we used rotational as well as lateral aligning markers; the latter were spaced with increments of 10 µm that allowed us to cut dies with dimensions ranging from 14.97 mm to 15.03 mm, well within the machining tolerances of the sample holder. After machining, the actual inner dimensions of each sample holder were measured by means of a measuring microscope. The wafers were then cut by selecting the lateral dicing markers associated with the die dimensions that fit best the holder being used. Such a meticulous chip dicing procedure is only effective in conjunction with a correspondingly high level of machining accuracy and precision. Machining was performed by the Physics Science and Technical Services machine shop, using standard CNC machining with a tolerance of 1 thou (25.4 µm).

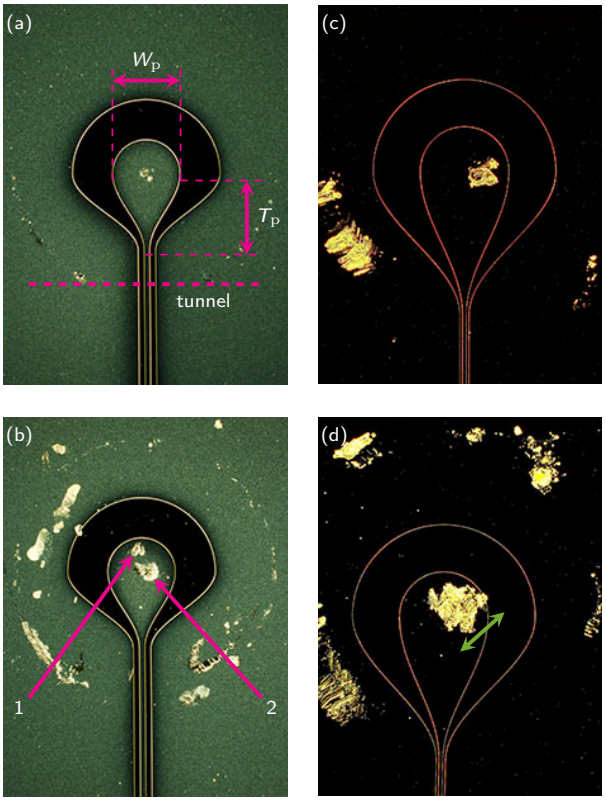

Figure 4.5: Micro images used to evaluate the alignment procedure of the three-dimensional wires. (a),(b) Ag pads. The magenta arrows indicate the first (1) and second (2) mating instance. The lengths W_p and T_p are indicated in (a) by means of magenta bars. (c),(d) Al pad before and after a cooling cycle to $\sim$ 10 mK. Center conductor dragging due to cooling is indicated by a green bar. The magenta dashed line in (a) indicates tunnel (i.e., rotational) alignment for the Ag pad.

Following the aforementioned procedures we were able to achieve the desired wire-pad matching accuracy and precision, which has resulted in only one failure since the implementation of the quantum socket in our lab four years ago. These figures of merit were tested in two steps: First, by micro imaging several pads that were mated to a three-dimensional wire and second, by means of DC resistance tests.

The DC resistance tests provide a quick and easy check for the connectivity of the wires to the contact pads for simple circuit structures at room temperature, before installation into the fridge. For simple TLs, the resistance between the signal line and the ground should measure as an open. A measurement between port 1 and port 2 of the signal line should measure as a short (though some small resistance will be present). Such tests were found to be a reliable indicator of successful microwave transmission at 10 mK.

Micro imaging was performed on a variety of different samples, four of which are exemplified in Fig. 4.5. The figure shows a set of micro images for Ag and Al pads. Figure 4.5 (a) and (b) show two Ag pads that were mated with the three-dimensional wires at room temperature.

Panel (a) shows a mating instance where the wire bottom interface perfectly matched the on chip pad. Panel (b) shows two mating instances that, even though not perfectly matched, remained within the designed tolerances. Notably, simulations of imperfect mating instances revealed that an off-centered wire does not significantly affect the microwave performance of the quantum socket. Finally, panels (c) and (d) display two Al pads which were both mated with a wire one time. While the pad in (c) was operated only at room temperature, the pad in (d) was part of an assembly that was cooled to $\sim$ 10 mK for approximately three months. The image was taken after the assembly was cycled back to room temperature and shows dragging of the wire by a few tens of micrometers. Such a displacement can likely be attributed to the difference in the thermal expansion of Si and Al.

4.3 DC and Microwave Characterization

As the intended use of three-dimensional wires is for control and measurement of superconducting qubits, they must show excellent performance from DC, for the use of current bias to tune qubit transition frequency, to 8 GHz, for both XY control and readout microwave tones [42, 46, 95, 117]. In general, the wires must be capable of transmiting any baseband modulated carrier signal within the specified frequency spectrum at cryogenic temperatures.

4.3.1 Four-point measurements

The wire-pad contact resistance R^{c} is an important property of the quantum socket. In fact, a large R^{c} would result in significant heating when applying DC bias signals and rectangular pulses. This heating would deteriorate qubit performance from the generation of quasiparticles, or worst case, breakdown the thin film superconductivity from hotspot generation.

In order to assess R^{c} for the inner and outer conductor of a three-dimensional wire, we performed four-point measurements using the setup shown in the inset of Fig. 4.6. Using this setup, we were able to measure both the series resistance of the wire R^{w} and the contact resistance R^{c}.

The setup comprises the microwave package with a chip entirely coated with a 120 nm thick Al film; no grounding washer was used. The package featured three three-dimensional wires, of which two were actually measured; the third wire was included to provide mechanical stability. The package was attached to the MC stage of the DR, connected to a set of twisted pairs, and measured at room temperature by means of a precision source-measure unit (SMU).

We measured the resistance between the inner conductor of a wire and ground, R_{ig}. This resistance comprises the inner conductor wire resistance $R_{\mathrm{i}}^{\mathrm{w}}$ in series with the inner conductor

contact resistance $R_{\mathrm{i}}^{\mathrm{c}}$ and any resistance to ground, R_{g}. At the operation temperature of the experiment ($\sim 10\,\mathrm{mK}$), Al is superconducting allowing the metal resistance to be neglected.

Figure 4.6 shows the current-voltage (I-V) characteristic curve for R_{ig}. With increasing bias currents, the contact resistance results in hot-spot generation leading to a local breakdown of superconductivity. For sufficiently high bias currents, superconductivity breaks down completely. At such currents, the observed hysteretic behavior indicates the thermal limitations of our setup [118]. Note, however, that these currents are at least one order of magnitude larger than the largest bias current required in typical superconducting qubit experiments [31].

In order to estimate R_{ig} from the I-V characteristic curve, we selected the bias current region from $-1.5\,\mathrm{mA}$ to $+1.5\,\mathrm{mA}$ and fitted the corresponding slope. We obtained $R_{\mathrm{ig}} \simeq 148\,\mathrm{m\Omega}$. TDR measurements suggest this isn't due to charge accumulation on the tip of the inner conductor. This value, which represents an upper bound for the wire resistance and the wire-pad contact resistance, $(R_{\mathrm{i}}^{\mathrm{w}} + R_{\mathrm{i}}^{\mathrm{c}})$, is significantly larger than that associated with Al wire bonds [119] or indium bump bonds [62]. In future versions of the three-dimensional wires, we will attempt to reduce the wire-pad contact resistance by rounding the tip of the center conductor, stiffening the wire springs, using a thicker metal film for the pads, depositing Au or titanium nitride (TiN) on the pads, and plating the wires with TiN. We note, however, that even a large value of the wire and/or wire-pad contact resistance will not significantly impair the quantum socket microwave performance; for example, the quantum architecture in Ref. [120] would be mostly unaffected by the contact resistance of our three-dimensional wires, as was recently demonstrated in Ref. [121].

This contact resistance in essence creates an upper limit on the number of qubits that can be operated in a given fridge. In that the cooling power at the mixing chamber must be greater than $N \times I_{\mathrm{max\ bias}}^2 \times R_{\mathrm{ig}}$, where N is the number of qubits and $I_{\mathrm{max\ bias}}$ is the max bias current that would be transmitted for qubit control, roughly on the order of $100\,\mu\mathrm{A}$. Although this presents a hard upperbound, of further concern is the potential generation of quasi particles from any thermal load generated at the contact point, which could harm the fidelity of nearby qubits. Practically, if the qubit error rate due to said quasiparticles was less than $\approx 10^{-4}$, it would be negligible compared to other sources of error. What resistance value would lead to said error rate given the expected bias current required would further be dependent on qubit placement with respect to the contact pad. Additionally, quasiparticle traps could be fabricated on chip to help shield the qubit.

4.3.2 Two-port scattering parameters

The two-port scattering parameter (S-parameter) measurements of a bare three-dimensional wire were realized by means of the setup shown in the inset of Fig. 4.7 (a) The device under test (DUT) consists of a cable assembly attached to a three-dimensional wire by means of a screw-in micro

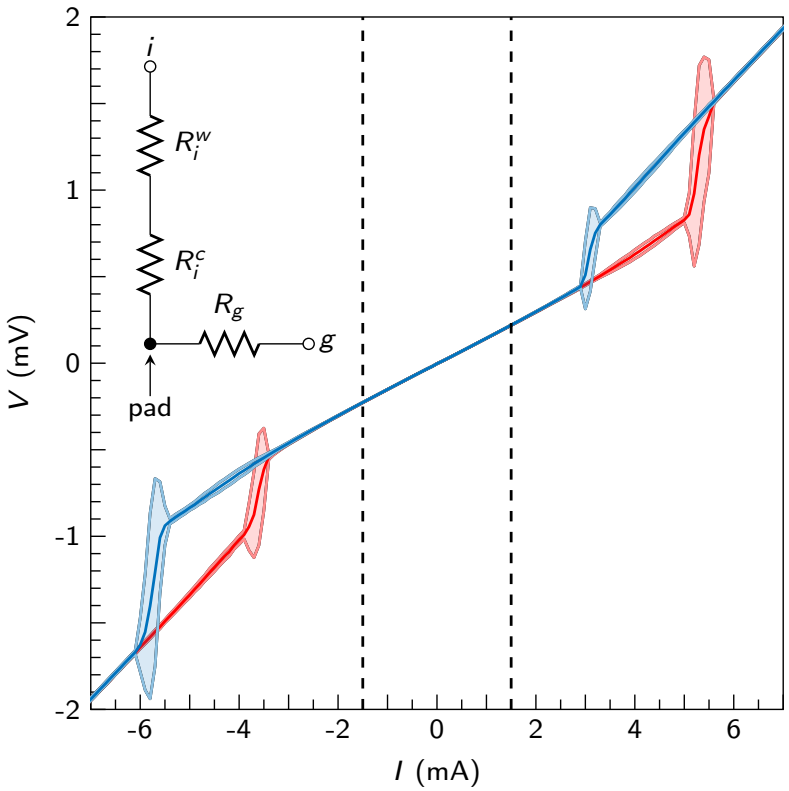

Figure 4.6: I-V characteristic curve for R_{ig}. The sweeps were conducted by both increasing (red) and decreasing (blue) the applied current between $-7\,\mathrm{mA}$ and $+7\,\mathrm{mA}$. The shaded region indicates two standard deviations. The dashed black lines indicate the region ($\mp$ 1.5 mA) for which the resistance value was found using linear regression. The origin of the hystereses is explained in the main text. The inset shows the circuit diagram of the device under test, including all resistors measured by means of the four-point measurement. The position of the pad is indicated by an arrow.©American Physics Society 2016

connector. The bottom interface of the wire is connected to a 2.92 mm end launch connector, which is characterized by a flush coaxial back plane. This plane mates with the wire bottom interface well enough to allow for S-parameter measurements up to 10 GHz. In order to measure the S-parameters of the DUT, we used a vector network analyzer (VNA) and performed a two-tier calibration, which made it possible to set the measurement planes to the ports of the DUT (see supplemental of [1] for details).

The magnitudes of the measured reflection and transmission S-parameters are displayed in Fig. 4.7 (a). We performed microwave simulations of a three-dimensional wire for the same S-parameters (see Subsec. 4.1.3 for the electric field distribution), the results of which are plotted in Fig. 4.7 (b). The S-parameters were measured and simulated between 10 MHz and 10 GHz. The S-parameters $|S_{21}|$ and $|S_{12}|$ show a featureless microwave response, similar to that of a coaxial transmission line. The attenuation at 6 GHz is $|S_{21}| \simeq -0.58\,\mathrm{dB}$ and the magnitude of the reflection coefficients at the same frequency is $|S_{11}| \simeq -13.8\,\mathrm{dB}$ and $|S_{22}| \simeq -14.0\,\mathrm{dB}$. The

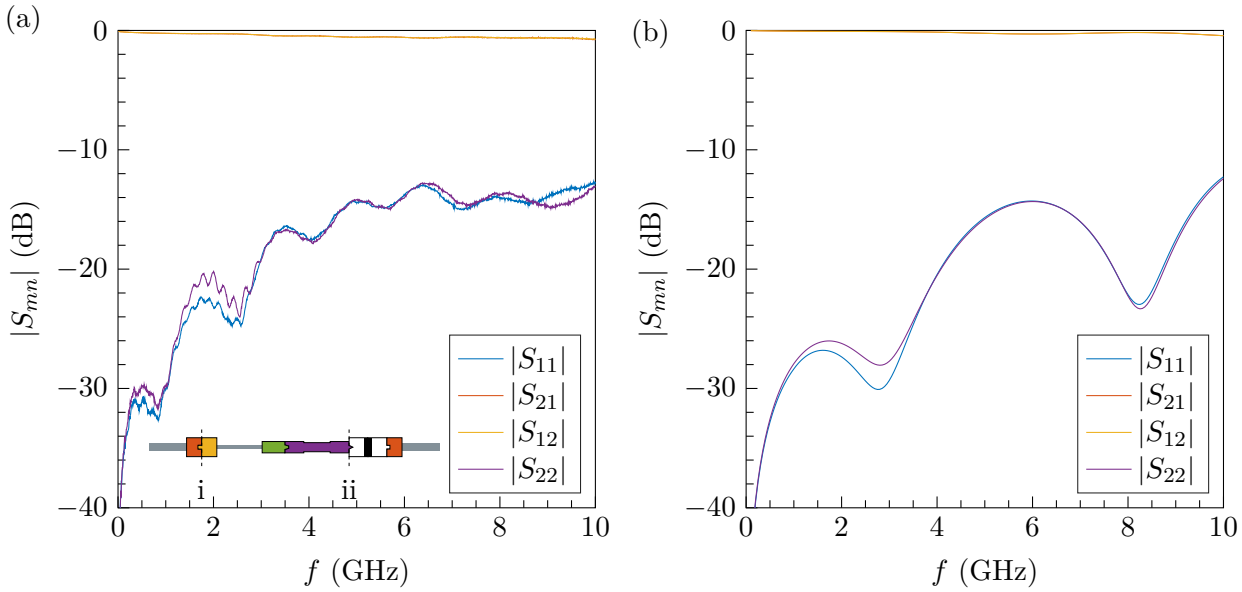

Figure 4.7: S-parameter measurements and simulations of a three-dimensional wire at room temperature. (a) Magnitude of the measured S-parameters $|S_{mn}|$, with $m, n = 1, 2$. Inset: Image of the measurement setup. From left to right: Segment of flexible coaxial cable (grey); Sub-miniature type A (SMA) female connector (red); after plane i, SMA male connector (orange); segment of semi-rigid coaxial cable EZ 47 cable (grey; cf. supplement); screw-in micro connector (green); three-dimensional wire (purple); after plane ii, 2.92 mm end launch connector (white and black); SMA female connector (red); segment of flexible coaxial cable (grey). (b) S-parameter simulations. The ports for simulation were directly at the contact head and back end of the three-dimensional wire. The lower attenuation is believed to be due to idealized material properties and connections.

phase of the various S-parameters (not shown) behaves as expected for a coaxial transmission line. All measurements were performed at room temperature.

The measurement results indicate acceptable operating performance for the three-dimensional wires. However, these measurements alone are insufficient to fully characterize the quantum socket operation. A critical feature that deserves special attention is the 90° transition region between the wire bottom interface and the on-chip CPW pad. It is well known that 90° transitions can cause significant impedance mismatch and, thus, signal reflection [80]. In quantum computing applications, these reflections could degrade both the qubit control and readout fidelity.

Figure 4.8 shows a typical setup for the characterization of a wiring configuration analogous to that used for qubit operations The setup comprises a DUT with ports 1 and 2 connected to a VNA. The DUT in this case is a microwave package with a pair of three-dimensional wires, which connect to a CPW TL on an Ag chip. The microwave package was attached to the package holder, as seen in Figs. 4.1 (d) and 4.4 (c). The TLs were designed to have characteristic impedance of 50Ω at room temperature ($\varepsilon_{\mathrm{r,Si}} = 11.7$). The back end of each three-dimensional wire is connected to one end of an EZ 47 cable by means of the screw-in micro connector; the other end of the

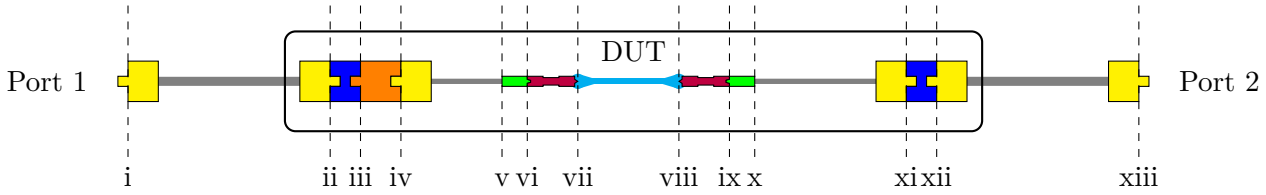

Figure 4.8: Microwave measurement setup. The vertical black dashed lines indicate main reflection planes. The yellow terminations correspond to SMA male connectors at the end of each cable. The input(output) flexible cable corresponds to the region in between planes i and ii(xii and xiii), in gray; the blue blocks correspond to SMA female bulkhead adapters; the plane ii(xii) correspond to the input(output) port of the DUT; the orange block corresponds to an SMA male to SMA female adapter; the EZ 47 input(output) cable corresponds to the region in between planes iv and v(x and xi), in gray of length $\approx$ 100 mm; the plane v(x) corresponds to the solder connection on the three-dimensional wire; the plane vi(ix) is associated with the screw-in micro connector of length 4.5 mm; the plane vii(viii) corresponds to the 90° interface connecting each three-dimensional wire to the input(output) of the CPW transmission line (cyan) of length 11.75 mm. The three-dimensional wires are indicated in red between planes vi and vii(viii and ix) of length 31 mm.©American Physics Society 2016

EZ 47 cable is soldered to an SMA male connector. A calibration using Keysight N4691 ECal was performed for all measurements setting the measurement plane to ii and xii as seen in Fig. 4.8.

We performed a two-port S-parameter measurement of the DUT from 10 MHz to 10 GHz. The measurement results at room temperature are shown in Fig. 4.9 (a).

The measurement results show similarity to that of a transmission line or coaxial connector, all be it with slightly worse attenuation and reflection than is ideal. For example, $|S_{11}|$ is approximately -15 dB; as a reference, for a high-precision SMA connector at the same frequency $|S_{11}| \simeq -30$ dB. It was realized after measurements that the silver had likely interdiffused with the silicon, behaving as a dopant [122], which would also impact the microwave performance. Clearly a buffer material was necessary during fabrication, but for the purposes of room temperature characterization, it was deemed a minor issue.

The presence of the screw-in micro connector can occasionally deteriorate the microwave performance of the quantum socket. In fact, if the micro connector is not firmly tightened, a dip in the microwave transmission is observed. At room temperature, it is straightforward to remove the dip by simply re-tightening the connector when required. However, once installed into the DR and operating at cryogenic temperatures, assuring that the micro connector is properly torqued at all times can be challenging. A recognizable 'dip' appears at approximately 1.8 GHz, with a 3 dB bandwidth of approximately 200 MHz. Analysis of the phase at this frequency didn't show anything to suggest a resonant component [1]. As the dip is far from the typical operation frequencies for superconducting qubits, it was deemed as inconsequential for initial tests and measurements.

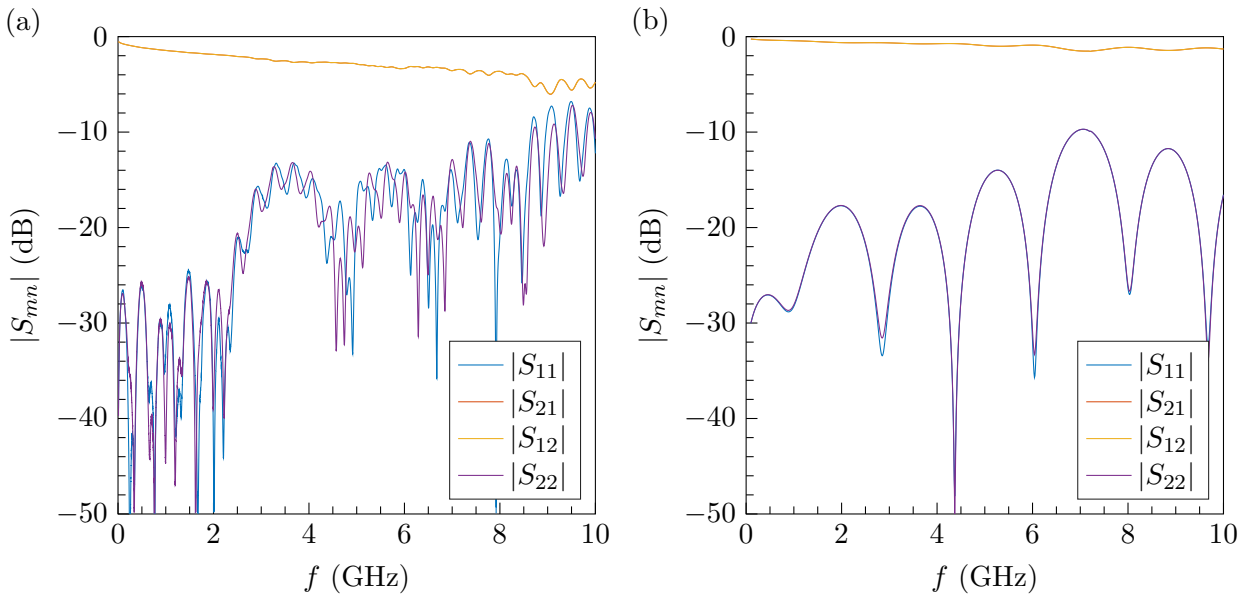

Figure 4.9: S-parameters of the Ag sample. (a) $|S_{mn}|$ measurement at room temperature. (b) $|S_{mn}|$ microwave simulation. The ports for simulation are planes vi and ix as seen in Fig. 4.8. It is believed this is part of the reason for the mismatch between attenuation and reflection, especially above 8 GHz. This is of minimal concern as the control and measurement frequency range of standard Xmon transmons is $\approx$ 4 to 8 GHz©American Physics Society 2016

Figure 4.9 (b) shows a simulation of the S-parameters for the Ag sample, for the same frequency range as the actual measurements. Comparison between the two shows general agreement, though clearly many more reflection planes with the actual measured results. The attenuation is higher with the measured results, believed to be due to a combination of the additional components comprising the DUT, and the on chip thin film not matching that of the ideal (as in not actually 50Ω matched or having the expected resistance).

We also simulated the case where the wire bottom interface is not perfectly aligned with the on-chip pad (results not shown). We considered maximum lateral misalignments of 100 µm and rotational misalignments of $\sim$ 20°, and swept between the ideal and these extremes using parametrized values. Coarser frequency sweeps which focused on key regions of interest were employed. The results showed that the departure between the misaligned and the perfectly aligned simulations was marginal. For example, the transmission S-parameters varied only by approximately $\mp$ 0.5 dB between the best and worst case simulations.

Microwave Parameters

To further analyze the performance of the quantum socket, we calculated other relevant microwave parameters from the measured S-parameters. This allows greater comparison against other wiring methods and insight as to the best ways to improve the design of the three-dimensional wires and

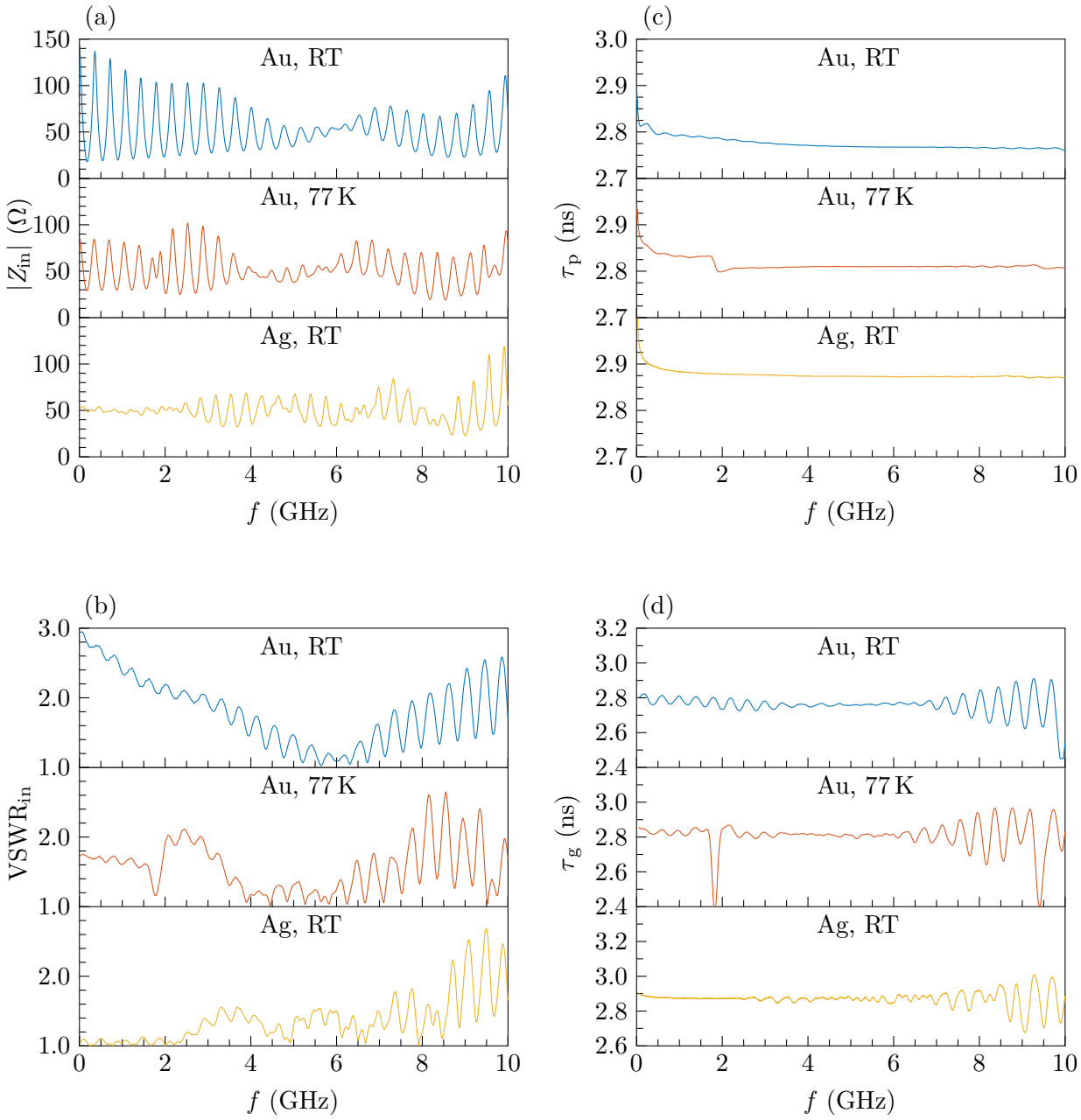

Figure 4.10: Quantum socket microwave parameters. (a) Input impedance magnitude $|Z_{in}|$. (b) Input VSWR, $VSWR_{in}$. (c) Phase delay τ_ϕ. (d) Group delay τ_g. Blue corresponds to the Au sample at room temperature (RT), red to the Au sample at 77 K, and orange to the Ag sample at room temperature (RT). S-parameter results for the Au sample available from [1].©American Physics Society 2016

microwave package. It also informs as to how impactful effects such as dispersion may be, which can be harmful to the pulses used for qubit control and measurement.

The complex input impedance can be obtained from the frequency dependent impedance

matrix $\mathbf{Z} = [Z_{mn}]$as [9]

$$Z_{\text{in}} = Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22} - Z_{\text{L}}} \quad , \tag{4.1}$$

where $Z_{\text{L}} = Z_0 = 50\,\Omega$ is the load impedance. The impedance matrix was obtained using the measured complex S-parameter matrix $\mathbf{S} = [S_{mn}]$ from

$$\mathbf{Z} = \sqrt{\mathrm{Z_c}} \left(\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} + \mathbf{S} \right) \left(\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} - \mathbf{S} \right)^{-1} \sqrt{\mathrm{Z_c}} \quad . \tag{4.2}$$

The magnitude of Z_{in} is shown in Fig. 4.10 (a). The input voltage standing wave ratio (VSWR) was obtained from [79]

$$\text{VSWR}_{\text{in}} = \frac{1 + |S_{11}|}{1 - |S_{11}|} \tag{4.3}$$

and is displayed in Fig. 4.10 (b). The phase delay was calculated as [10]

$$\tau_\phi = -\frac{1}{2\pi} \frac{\angle S_{21}}{f} \tag{4.4}$$

and is displayed Fig. 4.10 (c).

Finally, the group delay was obtained from [79]

$$\tau_{\text{g}} = -\frac{1}{2\pi} \frac{\partial}{\partial f} (\angle S_{21}) \tag{4.5}$$

and is displayed in Fig. 4.10 (d). The derivative in Eq. (4.5) was evaluated numerically by means of central finite differences with 6th order accuracy. The data in Fig. 4.10 (d) were post-processed using 1% smoothing. The output impedance and VSWR were also evaluated and resembled the corresponding input parameters.

The input and output impedances as well as the VSWRs indicate an acceptable impedance matching up to approximately 8 GHz. The phase and group delays, which are directly related to the frequency dispersion associated with the quantum socket suggest minimal dispersion at the frequencies of interest. This matches to what was expected for a combination of coaxial structures (the three-dimensional wires) and a CPW transmission line. Thus, we expect wideband control pulses to be transmitted without significant distortion in applications with superconducting qubits.

[9] See http://www.ece.rutgers.edu/ orfanidi/ewa/.
[10] See http://www.ece.rutgers.edu/ orfanidi/ewa/.

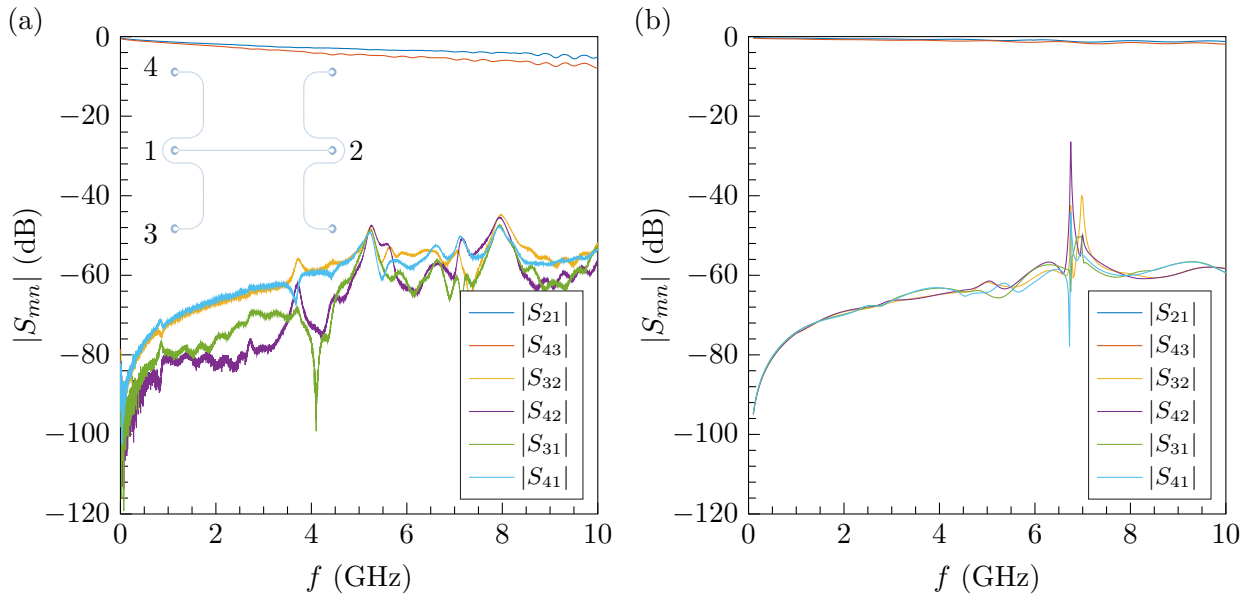

Figure 4.11: Signal crosstalk. (a) Transmission and crosstalk coefficients for the Ag sample shown in the inset. The numbers adjacent to the pads in the inset correspond to the device ports. Reciprocal and reflection S-parameters are not shown. (b) Microwave simulation of the same device. The origin of the peaks at approximately 7 GHz is explained in the main text.©American Physics Society 2016

4.3.3 Signal crosstalk

Crosstalk is the scenario when a signal being transmitted through a channel generates an undesired signal in a different channel. Inter-channel isolation is the figure of merit that quantifies signal crosstalk and is ideally maximized to improve signal integrity. Crosstalk can be particularly large in systems operating at microwave frequencies, where, if not properly designed, physically adjacent channels can be significantly affected by coupling capacitances and/or inductances. In quantum computing implementations based on superconducting quantum circuits, signal crosstalk due to wire bonds has been identified as a significant source of errors, with various methods developed to mitigate it [112, 123, 124]. However, these methods do not fully isolate neighbouring circuits, with isolations still being worse than 20 dB when using wire bonds [11]. As wirebonds are open structures, they will readily radiate noticeable amounts of electromagnetic energy to adjacent circuits. The coaxial design of the three-dimensional wires however, limits crosstalk due to such radiation.

In realistic applications of the quantum socket, the three-dimensional wires must land in close proximity to several on-chip transmission lines. In order to study inter-channel isolation in such scenarios, we designed a special device comprising a pair of CPW transmission lines, as shown in the inset of Fig. 4.11 (a). One transmission line connects two three-dimensional wires (ports 1 and 2), exactly as for the devices studied in Subsecs. 4.3.2; the other line, which also connects

[11] Daniel T. Sank (private communication).

two three-dimensional wires (ports 3 and 4), circumvents the wire at port 1 by means of a CPW semicircle. The distance between the semicircle and the wire outer conductor is designed to be as short as possible, $\sim$ 100 µm.

The chip employed for the crosstalk tests is similar to the Ag sample used for the quantum socket microwave characterization and was part of a DUT analogous to that shown in Fig. 4.8. The DC resistances of the center trace of the $1-2$ and $3-4$ transmission lines were measured and found to be $\sim$ 2.8 Ω and $\sim$ 4.5 Ω, respectively (note that the $3-4$ transmission line is $\sim$ 18.0 mm long, hence, the larger resistance). All DC resistances to ground and between the two transmission lines were found to be on the order of a few kilohms [12], demonstrating the absence of undesired short circuit paths. A four-port calibration and measurement of the DUT were conducted by means of a VNA Among the 16 S-parameters, Fig. 4.11 (a) shows the magnitude of the transmission coefficients S_{21} and S_{43}, along with the magnitude of the crosstalk coefficients S_{31}, S_{41}, S_{32}, and S_{42}.

The results show that the isolation in the typical qubit operation bandwidth, between 4 GHz and 8 GHz, is larger than $\sim$ 45 dB. Note that the crosstalk coefficients shown in Fig. 4.11 (a) include attenuation owing to the series resistance of the Ag transmission lines. The actual isolation, due only to spurious coupling, would thus be smaller by a few decibels.

Figure 4.11 (b) shows the microwave simulations of the crosstalk coefficients, which agree reasonably well with the experimental results. These simulations are based on the models explained in Subsec. 4.1.3. From simulations, we believe the isolation is limited by the crosstalk between the CPW transmission lines, instead of the three-dimensional wires. Note that the peaks at approximately 7 GHz correspond to an enhanced crosstalk due to a box mode in the microwave package, due to the effect of the conductive pillar for mechanical support. The simulations assume the package is a perfect conductor, and this effect may appear in measurements performed below $\sim$ 1 K, when the Al package becomes superconductive. For the room temperature measurements shown in Fig. 4.11 (a), these peaks are smeared out due to the highly lossy Al package.

4.4 Cryogenic Characterization

Thus far, we have shown a detailed characterization of the quantum socket in DC and at microwave frequencies at high power. In order to demonstrate the quantum socket operation in a realistic quantum computing scenario, we used a socket to wire a set of superconducting CPW resonators cooled to approximately 10 mK in a DR. We were able to show an excellent performance in the frequency range from 4 GHz to 8 GHz, which is the bandwidth of our measurement apparatus. We measured multiple times multiple chips using the same quantum socket, demonstrating

[12] The relatively low resistance to ground being likely due to properties discussed in Ref. [122].

the repeatability of our wiring method. We measured five Al on Si samples, as well as one Al on gallium-arsenide (GaAs) sample [125] (data not shown) and one Al on sapphire sample. The Al on sapphire device, in particular, featured a few resonators with quality factor comparable to the state-of-the-art in the literature [95], both at high and low excitation power.

Figure 4.12 shows a macro photograph of a 15 mm × 15 mm chip housed in the sample holder. The chip is thin film Al on Si and comprises a set of three CPW transmission lines, each connecting a pair of three-dimensional wire pads. Multiple shunted CPW resonators are capacitively coupled to each transmission line. In this section, we will focus only on transmission line three and its five resonators. The transmission line has a center conductor width of 15 µm and gap width of 9 µm, resulting in a characteristic impedance of approximately 50 Ω. These dimensions were determined using the permitivity of silicon at cryogenic temperatures, $\varepsilon_{\mathrm{r,Si}} \approx 11.45$ [126]. The resonators are $\lambda/4$-wave resonators, each characterized by a center conductor of width W and a dielectric gap of width G. The open end of the resonators runs parallel to the transmission line for a length ℓ_κ, providing a capacitive coupling; a 5 µm ground section separates the gaps of the transmission line and resonators. The nominal resonance frequency $\tilde{f}_0$ as well as all the other resonator parameters are reported in Table 4.3.

A typical DR experiment employing the quantum socket consists of the following steps. First, the chip is mounted in the microwave package, which has already been attached to the package

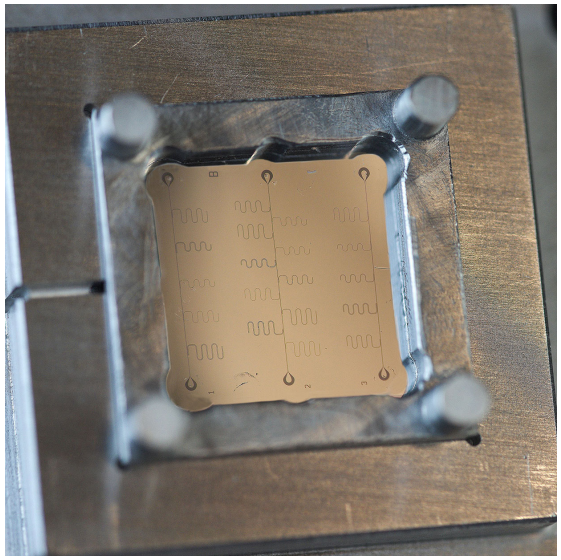

Figure 4.12: Macro photograph of an Al chip on Si substrate mounted in a sample holder with grounding washer. The image shows three CPW transmission lines each coupled to a set of $\lambda/4$-wave resonators. The grounding washer, with its four protruding feet, is placed above the chip covering the chip edges. The marks imprinted by the bottom interface of the three-dimensional wires on the Al pads are noticeable. This chip and similar other chips with analogous microwave structures and geometries, including one Al on GaAs sample as well as one Al on sapphire sample, were used in the measurements at $\sim$ 10 mK in the dilution refrigerator (DR).

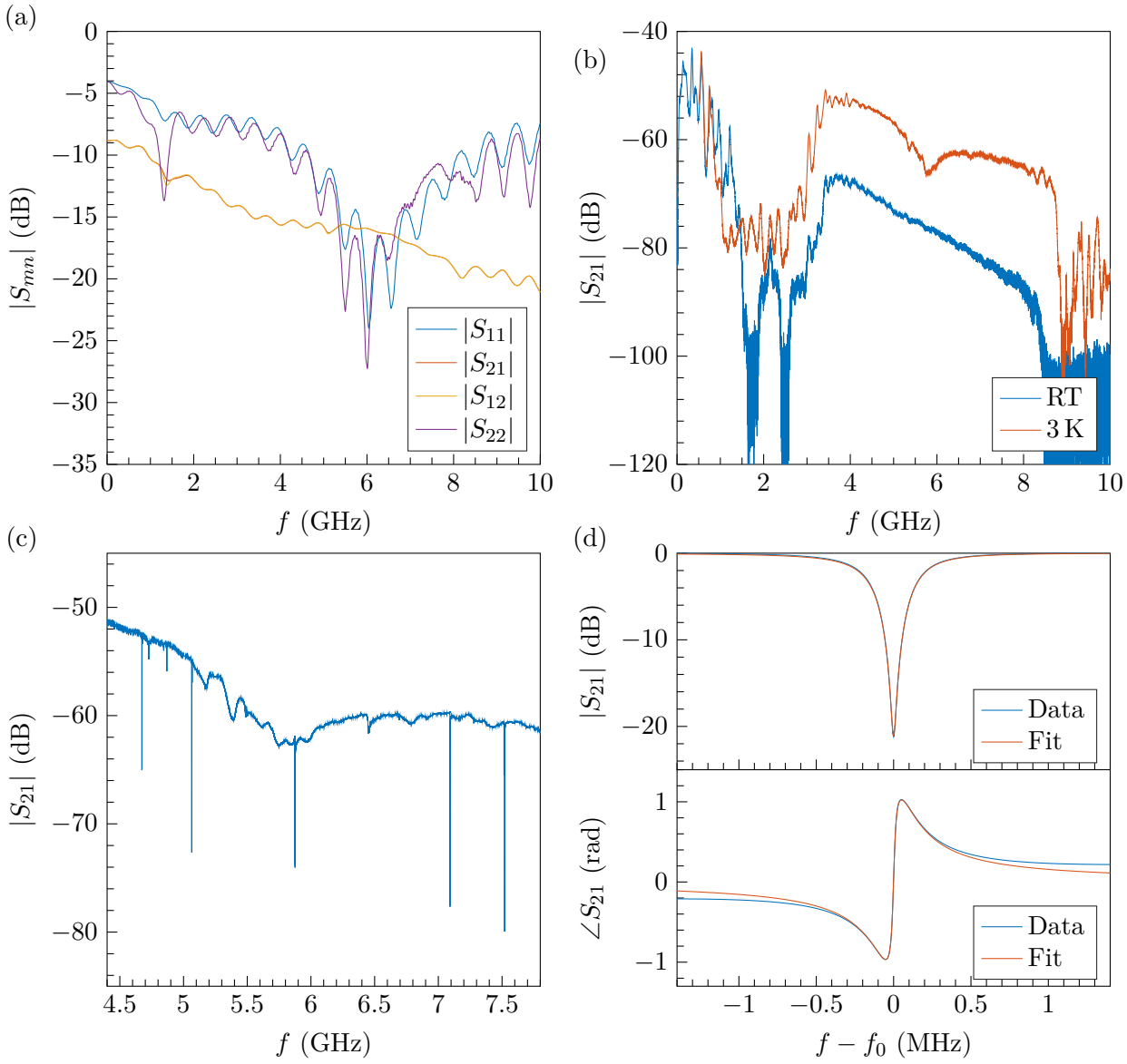

Figure 4.13: Measurements of Al on Si resonators. (a) Benchtop measurement of the S-parameters of the CPW transmission line three conducted at room temperature. (b) $|S_{21}|$ measurement of the same line with the chip mounted on the MC stage of the DR at room temperature (blue) and $\sim$ 3 K (orange). (c) $|S_{21}|$ measurement of the sample at approximately 10 mK. The five dips correspond to $\lambda/4$-wave resonators. (d) Magnitude and phase of S_{21} for resonator 3 of Table 4.3.©American Physics Society 2016

holder (see Sec. 4.2). Second, a series of DC tests are performed at room temperature to confirm good wire contact to the chip. Third, the package holder assembly is characterized at room temperature by measuring its S-parameters. The results of such a measurement are shown in Fig. 4.13 (a). Fourth, the package holder is mounted by means of the SMP connectors to the MC stage of the DR and a S_{21} measurement is performed. The DR setup is described in Appendix D. The results (magnitude only) are shown in Fig. 4.13 (b) in the frequency range between 10 MHz

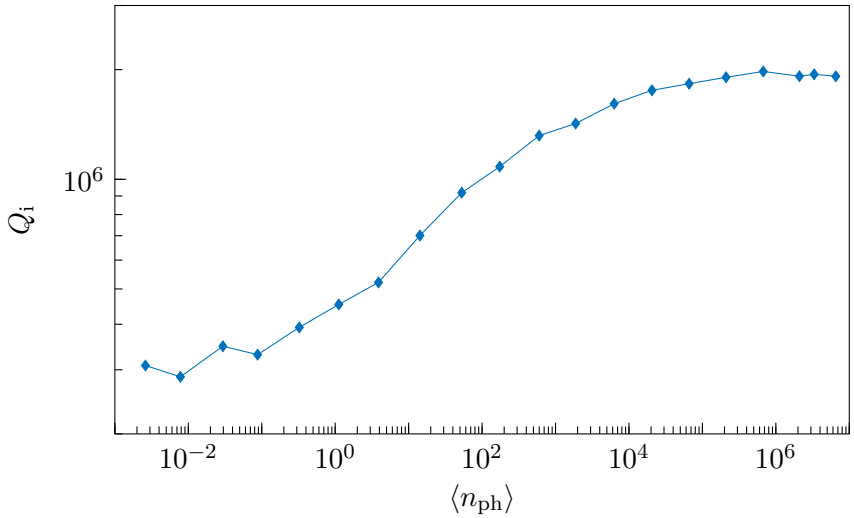

Figure 4.14: Measurement of Q_i as a function of $\langle n_{ph} \rangle$ for one of the Al on sapphire resonators. The confidence intervals were evaluated from the standard errors of the fitting parameters of the normalized inverse transmission coefficient $\tilde{S}_{21}^{-1}$. All measurements were performed at $\sim$ 10 mK. The typical quality factor "S-curve" is observed; the plateaus on the leftmost and rightmost regions of the curve indicate saturation at low and high values of $\langle n_{ph} \rangle$, respectively.©American Physics Society 2016

and 10 GHz. Fifth, the various magnetic and radiation shields of the DR are closed and the DR is cooled down. Sixth, during cooldown the S_{21} measurement is repeated first at $\sim$ 3 K and, then, at the DR base temperature of approximately 10 mK. The results are shown in Fig. 4.13 (b) and (c), respectively. At $\sim$ 3 K we note the appearance of a shallow dip at approximately 5.7 GHz, believed to be due to the screw-in micro connector losening during cooldown. At the base temperature, all five resonators are clearly distinguishable as sharp dips on the relatively flat microwave background of the measurement network. We then select a narrower frequency range around each resonator and make a finer S_{21} measurement. For example, Fig. 4.13 (d) shows the magnitude and phase of the resonance dip associated with resonator number 3.

The normalized inverse transmission coefficient $\tilde{S}_{21}^{-1}$ was fitted as in Ref. [95] and as discussed in 2.2.4. The fit results are shown in Table 4.3. The plot of the fits for the magnitude and phase of S_{21} for resonator 3 are overlaid with the measured data in Fig. 4.13 (d).

The resonator mean photon number $\langle n_{ph} \rangle$ can be estimated from the room temperature power at the input channel P_{in} and the knowledge of the total input channel attenuation α. From basic circuit theory and Ref. [127], we obtain

$$\langle n_{ph} \rangle = \frac{2}{h\pi^2} \frac{Q_{T^2}}{Q_{c^*}} \frac{P'_{in}}{\tilde{f}_0^2} \quad , \tag{4.6}$$

where h is the Planck constant, $1/Q_T = 1/Q_i + 1/Q_c^*$ is the inverse loaded quality factor of the resonator, and $P'_{in} = P_{in}/\alpha$ is the power at the resonator input. For example, $\langle n_{ph} \rangle \simeq 1.54 \times 10^7$ for resonator 3.

Table 4.3: Resonator parameters. The measured resonance frequency is f_0. The rescaled coupling and internal quality factors Q_c^* and Q_i, respectively, are obtained from the fits of the measured transmission coefficients (see SubSec. 2.2.4 for details). These quality factors were measured at a high resonator excitation power, corresponding to $\langle n_{ph} \rangle > 10^5$.

i	$\tilde{f}_0$	f_0	W	G	ℓ_κ	Q_c^*	Q_i
(-)	(MHz)	(MHz)	(µm)	(µm)	(µm)	(-)	(-)
1	4600.0	4673.2	8	5	400	5012	21243
2	5000.0	5064.5	15	9	300	14567	165559
3	5800.0	5872.9	25	15	400	10269	47165
4	7000.0	7091.7	15	9	300	6230	54894
5	7400.0	7520.1	8	5	400	4173	28353
6	4700.0	4717.6	15	9	45	244960	1977551

The fabrication process of the resonators described in Table 4.3 was not optimized for high values of Q_i, which, however, is an important figure of merit for applications to quantum computing. In order to verify the compatibility of the quantum socket with resonators of higher quality, we decided to fabricate a sample featuring an Al thin film deposited by means of a ultra-high vacuum electron beam physical vapor deposition (EBPVD) system; the substrate of choice was, in this case, sapphire. The sample design is similar to that shown in Fig. 4.12 [13] and the sample preparation analogous to that in Ref. [95]. We were able to measure a few resonators with $Q_i > 10^6$ for large values of $\langle n_{ph} \rangle$. For one of these resonators, we measured Q_i as a function of $\langle n_{ph} \rangle$, as shown in Fig. 4.14. As expected from literature measurements [95], Q_i decreased by approximately one order of magnitude when the resonator mean photon number was reduced from $\langle n_{ph} \rangle \simeq 10^8$ to $\simeq 10^{-2}$, due to the appearance of TLSs, as discussed in Subsec.2.3. For the lowest mean photon number, $Q_i \simeq 2.8 \times 10^5$; such a quality factor is a good indication that the quantum socket will likely preserve quantum coherence sufficiently well when utilized for the manipulation of superconducting qubits.

4.5 Conclusion

A full breakdown of the design and simulation of the quantum socket was provided to a level of detail such that the reader could easily replicate the device. All components were generated in Solidworks[14] and incorporated into a model of DQM's dilution fridge to ensure structural compatibility. These models were imported into HFSS for simulating the microwave performance.

[13] CPW TL dimensions were modified due to the change in permittivity.

[14] The coaxial pogo-pin model was modified from a model provided by INGUN.

They were further modified with parametrized values when modifications to improve performance were pursued. Blueprints were generated from these models following the standards and practices of the Science and Technical Services machine shop.

Once manufactured, the individual components were first measured and tested. The spring performance of the wires was tested in-depth to ensure compatibility in a cryogenic environment. Mechanical reliability was tested by multiple cooling cycles in both liquid nitrogen and liquid helium, and mechanical stability through measurement of the spring constant while cooled to cryogenic temperatures, both being found to be excellent. Alignment of the wires to the contact pads was also heavily analyzed and optimized. First through minimizing the margin of error for all components of the quantum socket, such as adding dicing markers to the chips as part of the lithographic fabrication. Second, by maximizing the allowable misalignment by optimizing the contact pad design. This has lead to only 1 misalignment over 30 months of use.

The quantum socket's electrical performance was then determined. Four-point measurements were undertaken in the dilution fridge to determine the wire's contact resistance under operational conditions. Although ideally this resistance would be zero, it was found to be low enough for initial measurements. The microwave performance of the quantum socket was determined first by room temperature measurements and the calculation of relevant microwave parameters, having performance equivalent to the standard wirebond. Potential for crosstalk was also analyzed, with the quantum socket being found to have better channel isolation than comparable packages using wirebonds. Cryogenic measurements in the dilution fridge focused on superconducting resonators. High power quality factors indicated the quantum socket caused no detriment to classical measurements. Low power measurements found reasonable quality factors given the fabrication processes used in this work, supporting that the quantum socket can be compatible with qubit operations.

These results give credence that the quantum socket is a viable solution to the wire scaling problem. It can be readily scaled to larger sizes in order to house chips with numerous physical qubits, such as the $\approx$ 100 necessary for a reasonable performing logical qubit or to achieve quantum supremacy. However, following the package analysis of Subsec.4.1.3, it is clear undesired cavity modes would become more prominent with larger package sizes, leading to information loss as explained in Sec. 3.5. The solution to this scaling problem is presented in the following chapter.

Chapter 5

Mitigating Coherent Leakage in Cavity-Qubit Systems

This chapter is based on the work presented in Ref. [2][1], of which the contributions of the authors is stated in the Statement of Contributions at the start of this thesis. Any components of Ref. [2] which the author of this thesis was not involved in has been excluded from this work.

As microwave packaging systems grow in size to accommodate the ever increasing number of superconducting qubits, unwanted cavity modes will become present in the usual qubit operational frequencies. As explained in Subsec. 3.5.1, interaction between the qubits and these modes will lead to new errors which could be detrimental to the operation of a quantum computer.

To determine the degree of such errors, in Subsec. 5.1.1 we study the interaction between one unwanted mode and a qubit in the one excitation sector and in absence of any damping. This allows us to characterize purely coherent leakage errors by defining an upper bound for the error probability p. We also analyze the case of a damped mode by considering the incoherent errors due to the Purcell rate Γ_c. For both scenarios, we demonstrate that suitably increasing Δ results in error rates due to such effects dropping far below the best currently achievable in the field.

The resonance frequencies of a cavity are determined by the electromagnetic field boundary conditions, which can be modified to shift these frequencies. In the case of a cavity-qubit system this results in a change of Δ. Although there are many possible approaches to achieve this goal, in Subsec. 5.1.2 and 5.1.3 we investigate two frequency shifting methods based on suitably designed arrays of zero-potential boundary conditions: Half-wave fencing and antinode pinning.

In order to test the efficacy of our methods, we first need a manner by which to determine the coupling strength between a realistically designed qubit and unwanted cavity mode, as shown in

[1]

Subsec. 5.1.5. We consider the medium-scale quantum processor introduced in [1], a scaled up version of the package discussed in Chapter 4, for simulations of the frequency shifting methods in Subsec. 5.2.1. It was shown that a 10×10 array of Xmon transmon qubits [31] could be realized on a $72\,\text{mm} \times 72\,\text{mm}$ dielectric substrate in a box of similar lateral dimensions. This box, however, leads to unwanted modes with resonance frequencies in the region of the qubits' transition frequency. Very similar architectures have been envisioned and implemented by other research groups [70, 121]. [2]

How the frequency shifting methods impact both coherent leakage error and the Purcell rate in the medium-scale quantum processor is analyzed in Subsec. 5.2.2. We show that both methods are able to readily drop the error of concern to orders of magnitude below error rates, $\bar{p}$, currently achievable in the field. Finally, in Sec. 5.3, we discuss the optimal manner by which to apply these methods, how higher order modes are impacted, and application of the methods for dealing with dielectric modes.

5.1 Methodology

Half-wave fencing, inspired by the picket fence Faraday cage, provides a straightforward analytical solution that can be used to quickly estimate the resources required for the desired change in Δ. In the case of perfect conductors, antinode pinning provides the optimal method (against resource usage) to modify boundary conditions, transforming cavity mode antinodes into nodes through an iterative procedure. A consistent metric to analyze resulting error from both coherent leakage and the Purcell rate is also presented (see Subsec. 5.1.1).

5.1.1 Coherent leakage error probability and dispersive Purcell rate

Consider a qubit interacting with an unwanted cavity mode with coupling rate g and damping rates $\gamma_\text{r} = \gamma_\text{d} = \kappa = 0$, where γ_r and γ_d are the qubit's relaxation and dephasing rate, and $\kappa = 0$ is the cavity's loss rate. A quantum-mechanical representation of this system is provided by the Jaynes-Cummings Hamiltonian as disussed in Sec. 3.5. Presuming the scenario of a single excitation, which is a fair assumption for quantum computing applications, the time evolution in the Schrödinger picture gives us Eq. 3.37. If we focus on the initial condition of $|\psi(0)\rangle = |0, \text{e}\rangle$,

[2] A common feature to these architectures is the metalization of almost the entire substrate surface, the majority of which serves as a ground plane. The area of dielectric exposed to the box due to the required circuit components is low enough not to significantly perturb the modes of the system, nor do the circuits themselves. This feature allows us to study and propose remedies for box and substrate modes independently, as well as to ignore specific circuit designs.

the practical scenario in the single excitation sector, the time evolution of $|\psi(t)\rangle$ informs us of the coherent leakage that has occoured at a particular t. Assuming perfect measurement,

$$P_{0,\mathrm{e}}(t) = |\,\langle 0,\mathrm{e}|\psi(t)\rangle\,|^2 = P_{\mathrm{e}}(t,\Delta). \tag{5.1}$$

If there is no leakage, we would expect $P_{\mathrm{e}}(t,\Delta)$ to remain constant at 1, and any deviation to be an error. As such we choose

$$p = 1 - \min\left(P_{\mathrm{e}}(t,\Delta)\right), \tag{5.2}$$

where taking the minimum gives the worst case scenario for the error value. Otherwise some arbitrary choice of t would be required which would be dependent on a number of factors, such as gate and measurement times. Taking the minimum allows for a consistent metric which is independent of the implementation being pursued. First solving for $\langle 0,\mathrm{e}|\psi(t)\rangle$ using Eq. 3.37, 3.35 and 3.34 gives us

$$\begin{aligned}\langle 0,\mathrm{e}|\psi(t)\rangle &= \langle 0,\mathrm{e}|\mathbf{e}^{-j\pi f_{\mathrm{c}} t}\left[\cos\left(\tfrac{\theta_0}{2}\right)|0,+\rangle\,\mathbf{e}^{-j\alpha_0 t} - \sin\left(\tfrac{\theta_0}{2}\right)|0,-\rangle\,\mathbf{e}^{+j\alpha_0 t}\right]\rangle \\ &= \mathbf{e}^{-j\pi f_{\mathrm{c}} t}\left[\cos\left(\frac{\theta_0}{2}\right)^2\mathbf{e}^{-j\alpha_0 t} + \sin\left(\frac{\theta_0}{2}\right)^2\mathbf{e}^{+j\alpha_0 t}\right]\end{aligned} \tag{5.3}$$

where $\theta_0 = \arctan\left(g/\Delta\right)$ and $\mathbf{e}$ is Euler's number. We can then plug this into Eq. 5.2 to get

$$p = 1 - \cos^4\left(\frac{\theta_0}{2}\right) - \sin^4\left(\frac{\theta_0}{2}\right) + 2\cos^2\left(\frac{\theta_0}{2}\right)\sin^2\left(\frac{\theta_0}{2}\right). \tag{5.4}$$

This measure purposely neglects incoherent errors due to damped cavity modes, allowing us to determine whether the condition $p \ll \bar{p}$ can be reached by means of our frequency shifting methods, where $\bar{p}$ is the acceptable error ceiling.

It is worth considering three limiting cases of Eq. 5.4. First, when $\Delta = 0$ (which is known as the *resonant regime*), it is easy to show that $p = 1.0$, corresponding to the highest possible coherent leakage error. This occurs, for example, at the point in time when one quantum of information has completely swapped from the qubit to the cavity mode. Second, when $\Delta \gg g$ (which is known as the *dispersive regime*), the error probability Eq. 5.4 can be approximated as $p \sim (g/\Delta)^2$. The purpose of the frequency shifting methods is to reach this regime in order to strongly suppress the amplitude of P_{e}. Third, when $\Delta \to \infty$ and for a constant g, we readily find that $p \to 0$. In this case, an ideal frequency shifting method has entirely removed any coherent leakage error due to the cavity mode.

Suppose that the unwanted cavity mode is characterized by a nonzero damping rate κ, as in $Q_i < \infty$. When $\Delta = 0$, depending on whether the cavity-qubit interaction is in the strong or weak coupling regime, $g \gg \kappa$ or $g \ll \kappa$, the resulting leakage errors are coherent or incoherent errors, respectively [3]. In the weak coupling regime, in particular, the presence of the mode results in the enhancement of the qubit spontaneous emission rate [128]. In this regime, with $\Delta \gg g$ instead, the cavity inhibits spontaneous emission, resulting in the dispersive Purcell rate [29]

$$\Gamma_{\rm r} \sim \left(\frac{g}{\Delta}\right)^2 \kappa = \left(\frac{g}{\Delta}\right)^2 \frac{2\pi f_{\rm r}}{Q_{\rm i}}\,. \tag{5.5}$$

We note that Eq. 5.5 remains a valid approximation as long as $\kappa \ll \Delta$, i.e., for a mode with sufficiently narrow Lorentzian linewidth (high-$Q_{\rm i}$ cavity limit). In the presence of qubit decoherence, the rate Eq. 5.5 should be engineered not to exceed the qubit bare relaxation rate, i.e., $\Gamma_{\rm c} < \gamma_{\rm r}$. Assuming a fixed g, the rate Eq. 5.5 can be reduced using two approaches, increasing Δ or decreasing κ. The frequency shifting methods allow us to implement the first approach, whereas engineering the highest attainable $Q_{\rm i}$ makes it possible to realize the second. In the limit of $\kappa \to 0$, purely coherent leakage errors become the dominating error source. Notably, an unwanted high-$Q_{\rm i}$ cavity mode that is initially resonant with the qubit and then shifted to a large detuning condition helps protect the qubit from spontaneous emission in free space.

5.1.2 Half-wave fencing

The inner space of a microwave package in vacuum can be modeled by a box with square cross-section of side length $\mathcal{L}$ and height h. Modifying Eq. 2.28 with $a = h$ and $b = d = \mathcal{L}$ results in

$$f_{nm\ell} = \frac{c}{2}\left(\frac{\ell^2 + n^2}{\mathcal{L}^2} + \frac{m^2}{h^2}\right)^{1/2}. \tag{5.6}$$

When $\mathcal{L} \gg h$, the mode with the lowest resonance frequency or dominant mode is the $\mathrm{TE}_{nm\ell} = \mathrm{TE}_{101}$ mode. The corresponding resonance frequency is $f_{101} = c/(\sqrt{2}\mathcal{L})$. Under these conditions, the box can be represented by a two-dimensional square membrane with side $\mathcal{L}$, as shown in Fig. 5.1 (a). The $\mathcal{L}^2$ square can be iteratively divided into smaller squares with dimensions $\{(\mathcal{L}/2)^2, (\mathcal{L}/4)^2, \ldots, [\mathcal{L}/(2^d)]^2\}$, where $d \in \mathbb{N}$ is the number of iterations. The total number of squares after d iterations is thus $2^{2d} = n_{\rm c}$.

The physical implementation of this method is realized by dividing the box in a number of smaller boxes or *cells*, which are encapsulated by perfectly conducting grounded walls; each cell behaves as a Faraday cage. The walls can be replaced by a set of three-dimensional wires, resulting

[3] The transition between the coherent and incoherent error regimes takes place for $g \sim \kappa$.

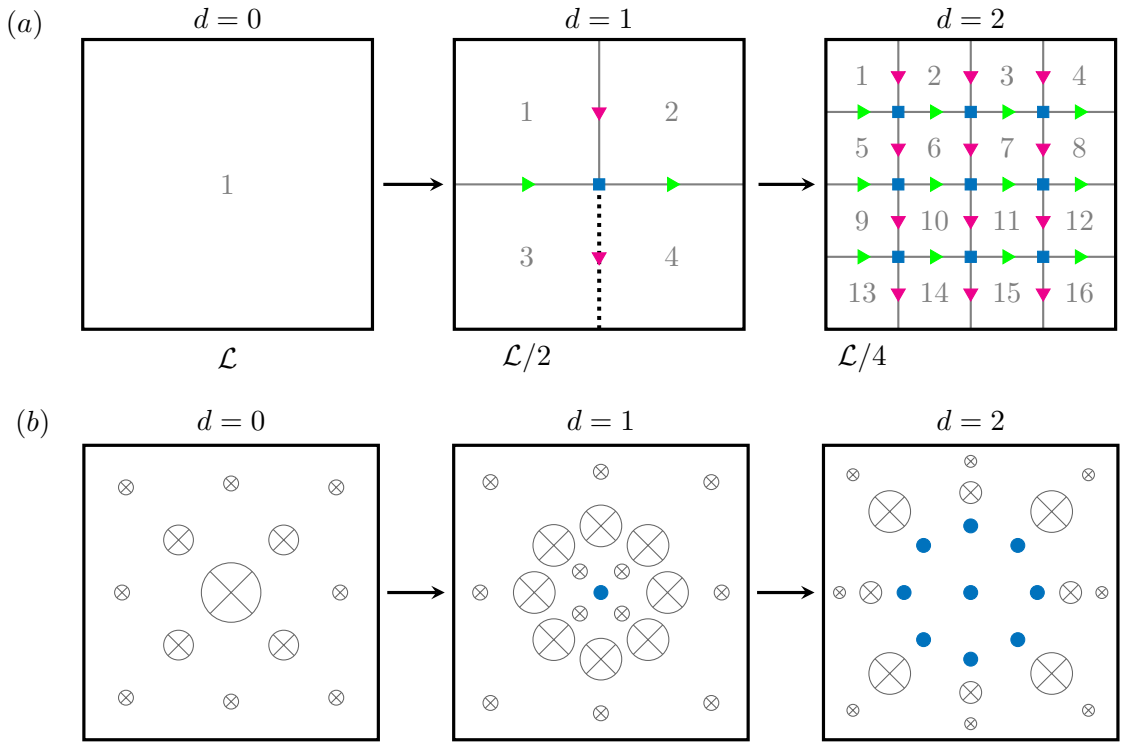

Figure 5.1: First three iterations of the two proposed frequency shifting methods. The rectangular box of side $\mathcal{L}$ is viewed along the y-axis (i.e., top view). (a) Half-wave fencing. Numbers indicate each of the n_c cells for the various iterations. Gray lines represent the geometric boundary of a cell; the thick dashed black line in the subpanel $d = 1$ indicates one inner edge of a cell. Full blue squares show the position of the coaxial Pogo pins on the square grid associated with the first term in Eq. 5.7b; full down magenta and right green triangles correspond to pins on the two orthogonal rectangular grids associated with the second term in Eq. 5.7b. (b) Antinode pinning. Pins are indicated by full blue circles. Crossed circles indicate the electric field distribution, with cross-circle size relating to the field strength (not to scale). For $d = 0$, the TE_{101} mode is shown. For $d = 1$, one pin is placed in correspondence to the antinode of TE_{101}, resulting in a toroidal field distribution. For $d = 2$, eight additional pins partially suppress the circular antinode. Note that, in this case, the field inside the eight-pin "circle" is very weak compared to the rest of the field and, thus, is not shown.

in a Faraday picket fence. Figure 5.1 (a) displays the fences for $d = 0, 1, 2$. The iteration $d = 1$, for example, comprises one vertical and one horizontal fence. In the simplest case, each of these two fences can be approximated by three equally separated pins, one of which is in the center of the $\mathcal{L}^2$ cell (with the center pin being used only once). This method, which we name half-wave fencing, makes it possible to shield pairs of adjacent cells. After d iterations, the ideal frequency of the lowest resonant mode for each of the cells and the total number of pins are given by

$$\begin{cases} f_c = f_{101}\, 2^d & \text{(5.7a)} \\ \\ N = (2^d - 1)^2 + 2{\times}2^d\,(2^d - 1) & \text{(5.7b)} \end{cases},$$

respectively, where $N \in \mathbb{N}$ is obtained from a simple counting argument [see Fig. 5.1 (a) for a schematic pin counting representation]. As expected, f_c increases with d (the smaller the cell, the higher the resonance frequency). By substituting the expression for 2^d obtained from Eq. 5.7a into Eq. 5.7b, we obtain a quadratic equation in the variable f_c/f_{101} with parameter N. By selecting the positive solution of this equation, we find an analytic expression for f_c as a function of N, which reads

$$f_c = \frac{f_{101}}{3}\left(2 + \sqrt{1 + 3N}\right). \tag{5.8}$$

Realistically, this equation is only valid for values of N corresponding to integer values of d given by Eq. 5.7b. Interpolating Eq. 5.8 for arbitrary real values of N helps us to understand qualitatively the frequency shifting trend offered by the method (see examples in Subsec. 5.2.2). Again, these would not be physically meaningful given scenarios not matching to integer values of d would have unpredictable mode frequencies and distributions.

For the picket fence approach to actually match the ideal results given from Eq. 5.8, enough wires to create a full wall would need to be used. This is impractical not only due to the suboptimal resource usage, but the restrictions caused to on chip circuit designs. As such, the fences are built from the minimal number of wires possible while still managing to provide isolation between neighboring cells, being $\lambda_c/4$ apart, where λ_c is the wavelength of the frequency described by Eq. 5.7a. For resulting modes with resonance frequency much higher than f_c, the gaps between the pickets make the fence practically transparent to the field. This, however, is not a major concern if those modes are already well separated in frequency from the qubit transition frequency f_q, $f_c \gg f_q$. In fact, if this is not the case more steps of the method have to be applied to sufficiently shift the frequency of lower modes.

5.1.3 Antinode pinning

An alternative method to increase the resonance frequency of the modes in a cavity can be realized by introducing new zero-potential boundary conditions at the antinodes of the cavity electric field $\vec{E}$, i.e., where $\|\vec{E}\|$ is maximum. Each new boundary condition suppresses the corresponding antinode, thus effectively transforming it into a node. These boundary conditions can again be implemented using the three-dimensional wires, where the outer conductor forces $\|\vec{E}\| = 0$. Figure 5.1 (b) displays the first three iterations of the algorithm used to perform this method, which we name antinode pinning. The spatial distribution of the electric field associated with the TE_{101} mode of a rectangular cavity is characterized by a sinusoidal shape with the field antinode being located at the center of the cavity. When introducing a wire at this location, iteration $d = 1$, the dominant mode (and all other modes) increase in frequency and the field

distribution no longer resembles that of a $\mathrm{TE}_{nm\ell}$ mode. In this case, $\|\vec{E}\|$ has a toroidal structure with a continuous antinode distribution of circular shape.

The pins, however, can only be placed at semi-discrete locations. Thus, when performing iteration $d = 2$, it is only possible to partially suppress the entire antinode distribution by means of a finite number of pins. The performance of the method improves with the number of pins, until reaching the limit where the pins start touching each other. The optimal placement for such continuous antinode distributions can be difficult to determine. A square or octagon placement in the case of circular antinode seems to give the best results while still maintaining resource optimization. The cavity modes depart from simple geometric structures that can be described with analytical functions. Under these conditions, the pin placement and corresponding electromagnetic field distribution must be determined through numerical simulations. These can be simplified by solving the two-dimensional wave equation, i.e., ignoring the y-axis, assuming the pins to be additional boundary conditions. It is possible to perform the antinode pinning method efficiently by executing the algorithm of Fig. 5.1 (b) automatically until a desired frequency or maximum number of pins is reached.

5.1.4 Electromagnetic-field simulations setup and settings

In order to study in detail the effects of the frequency shifting methods on unwanted cavity modes, we resort to numerical simulations of the electromagnetic field using the high-frequency three-dimensional full-wave electromagnetic-field simulation software (also known as HFSS) by Ansys, Inc. [4].

The typical model used in our simulations is an ideal box with dimensions $\mathcal{L} = 72\,\mathrm{mm}$ and $h = 3\,\mathrm{mm}$, which is simulated by means of the HFSS eigenmode solution type. When considering a large number of coaxial Pogo pins inside the box, the electric field distribution is initially unknown. Thus, we do not make use of any mesh operation at the beginning of the simulation, instead allowing the adaptive meshing procedure to determine the optimal meshing layout. A maximum delta frequency pass of $0.01\,\%$ is used, with a minimum converged pass count of 3. High iterations of d fail to converge as the mesh density required exceeds the memory capacity of our computer.

In the case of the antinode pinning method, we solve for the dominant eigenmode of a certain model that is then overlaid with the resulting $\|\vec{E}\|$. To suppress the antinode of this eigenmode, we assume perfectly conducting coaxial pins with given diameter (see Subsec. 5.2.1). We note that the actual outer conductor of the pins used in our packages is made from brass [1]. However, the thickness of this conductor is orders of magnitude larger than the skin depth and, thus, the perfect conductor idealization can be safely used. After pinning the antinode, we solve again for

[4] See http://www.ansys.com/products/electronics/ansys-hfss for details on HFSS.

the dominant eigenmode and repeat the procedure by placing new pins at each antinode of the new eigenmode. The half-wave fencing method is simpler to study than the antinode pinning method because it can be simulated without previous knowledge of the electric field distribution at each iteration.

5.1.5 Estimate of box-qubit coupling rates

To properly determine results for both p and Γ_r, an accurate value for the coupling, g, between the cavity and a Xmon transmon qubit with practical dimensions must be determined. To do so, we emulated the qubit by means of the microwave structure depicted in Fig. 5.2 (a) and simulated its interaction with a box mode. The structure comprises a CPW cross on the xz-plane, with the center bottom attached to a micro-coaxial half-wave resonator of length R that extends outside the box, along the y-axis. The cross acts as an "antenna" that couples to the box modes with resonance frequencies given by Eq. 5.6, which are set by the geometry of the box. By continuously varying R, it is possible to sweep the resonance frequency of the resonator, f_R, resulting in a tunable resonator coupled to a set of fixed box modes. The cross lies on the same plane as the metallic bottom wall of the box, with a dielectric substrate directly below. The center of the cross is positioned at the antinode of the electric field of the dominant mode. The dimensions of the CPW cross are the center conductor width S, the gap width W, and the arm length A; the substrate is characterized by a height h_s and relative permittivity ε_r.

We performed electromagnetic field simulations of the cross-box coupled system using ANSYS HFSS. We sweep f_R through f_c[5] obtaining the first two eigenmodes. An accurate simulation of this system is computationally intensive due to the high aspect ratio between the largest and smallest features of the system ($\sim$10 mm/10 µm). This issue can be overcome by scaling up the dimensions of the cross, while maintaining the same box size. The dimensions of each simulated cross are determined from $S/X = W/X = 100\,\mu\mathrm{m}$ and $A/X = 1000\,\mu\mathrm{m}$, where X is a scaling factor [see Fig. 5.2 (a) for numerical values]. We simulated the coupled system for progressively smaller cross dimensions until exceeding the computing capabilities of our machine. Values of g for even smaller cross sizes can be extrapolated following the trend established by the simulated systems.

The first two eigenmodes of the electric field for $X = 3.0$ are shown in Fig. 5.2 (b). This diagram resembles the energy level anti-crossing of a coupled cavity-qubit system. Thus, it can be used to estimate g by fitting the simulated frequency eigenmodes to the frequencies associated with the first two energy dressed states of the Jaynes-Cummings Hamiltonian $\widehat{H}_\mathrm{JC}$, $|0,-\rangle$ and $|0,+\rangle$, respectively, subtracted by the frequency of the ground state energy (see Sec. 3.5),

[5] f_c is used in this chapter to indicate the frequency of the lowest mode supported by the cavity in question, but is equivalent to f_r when dealing with an ideal cavity.

$$\begin{aligned} \bar{f}_{0,\pm} &= \frac{E_{0,\pm} - E_{0,\mathrm{g}}}{2\pi\hbar} \\ &= \left(f_{\mathrm{r}} \pm \alpha_0 - \frac{\Delta}{2} \right) . \end{aligned} \tag{5.9}$$

The curve fitting results are shown in Fig. 5.2 (b), where the Jaynes-Cummings model overlays

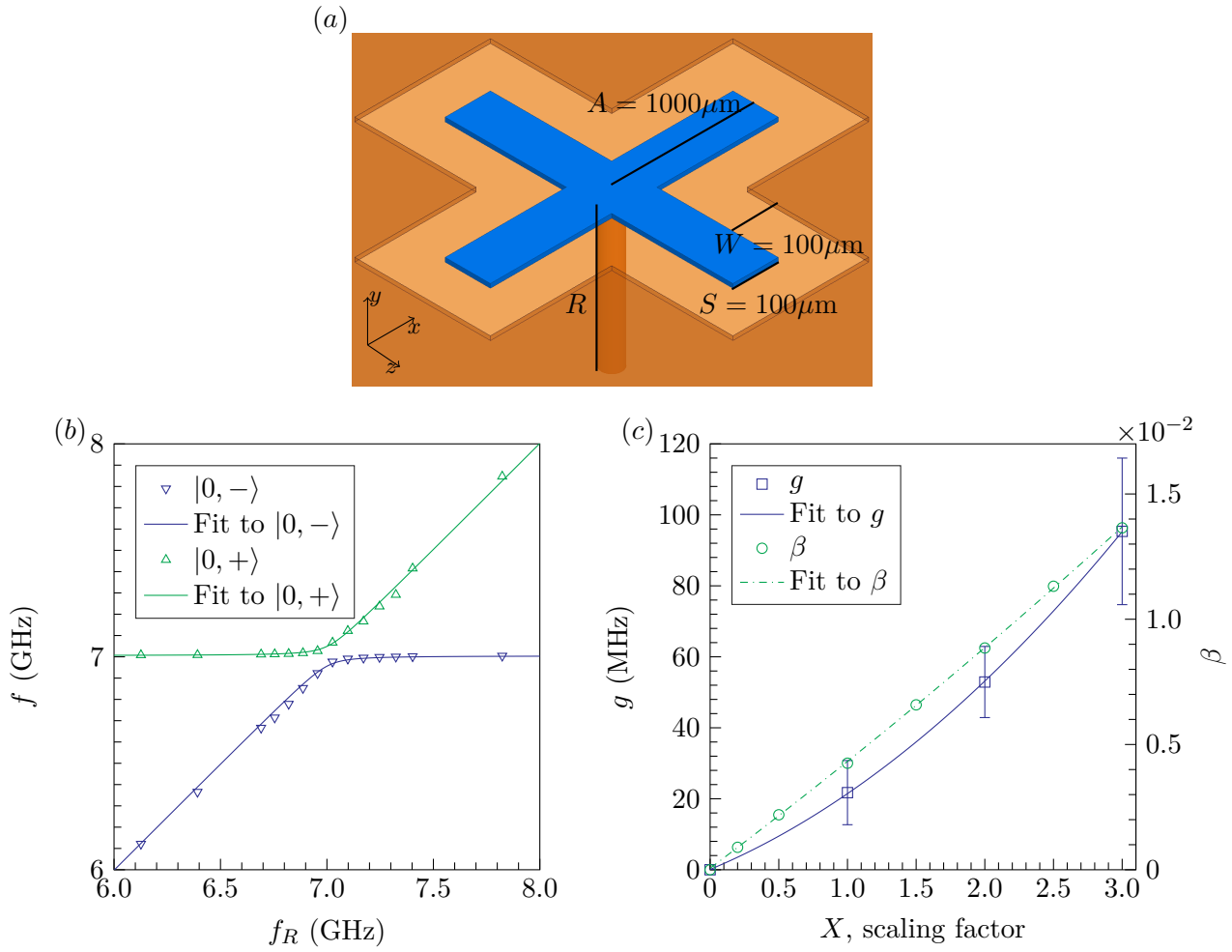

Figure 5.2: Model and simulation results for the coupling between an Xmon transmon qubit and a box mode. (a) CPW cross described in the text for $X = 1.0$, $h_{\mathrm{s}} = 500\,\mu\mathrm{m}$, and $\varepsilon_{\mathrm{r}} = 11.45$ (i.e., silicon at $\approx 4\,\mathrm{K}$). (b) f vs. f_R: Simulation results for the first two eigenmodes of a cross-box system for $X = 3.0$. The box dimensions are $\mathcal{L} = 30.26\,\mathrm{mm}$ and $h = 3\,\mathrm{mm}$, resulting in $f_{\mathrm{c}} \approx 7\,\mathrm{GHz}$. The downward open blue triangles and the upward open green triangles correspond to $|0,-\rangle$ and $|0,+\rangle$, respectively. The solid lines are fitting curves obtained from Eq. 5.9. (c) Left y-axis: g vs. X (open blue squares) obtained from the fitting procedure in (b), with error bars indicating the 95 % confidence intervals of the fitting. The solid blue line is a quadratic fit. Right y-axis: β vs. X (open green circles) with quadratic fit (dashed green line).

the simulated data.

We perform the simulation and curve fitting procedure for three different values of X. The corresponding values of g are displayed in Fig. 5.2 (c) that also shows a quadratic polynomial fit of the data, allowing the estimation of g for other values of X. The electric field sinusoidal distribution is taken into account in the simulations.

For the parameter space chosen in the simulations, our scaling argument and derived coupling values are consistent with those in [129], which follows the black body simulation approach. In that study, it is shown that a change in transmon qubit geometry is equivalent to a change in the capacitance ratio $\beta \approx C_{\mathrm{g}}/(C_{\mathrm{g}} + C_{\mathrm{p}})$ for a constant cavity height. This ratio accounts for the capacitances C_{g} and C_{p} between the CPW cross and the cavity top and bottom walls, respectively, and directly relates to a change in g. The capacitance the josephson junctions would contribute in a real system are ignored as they are orders of magnitude smaller than C_{p}. We calculate β from C_{g} and C_{p} obtained for the values of X used to find g, as well as for additional intermediate values. The capacitances C_{g} and C_{p} are simulated with ANSYS Q3D Extractor [6]. The results are shown in Fig. 5.2 (c). The figure also displays a quadratic polynomial fit of the simulated data, allowing us to compare the relationship between β and g. In spite of a slight mismatch, the results are in near enough agreement to provide an upper bound for the coupling coefficient of a typical Xmon transmon qubit. An upper bound for our purposes would be a worst case scenario, which is sufficient for determining if the frequency shifting methods are effective at lowering leakage error to reasonable levels.

5.2 Simulated and Analytical Results

To determine the effectiveness of the frequency shifting methods in a realistic physical setting, a series of electromagnetic field simulations were run, as shown in Subsec. 5.2.1. The degree to which this change in delta improves both the coherent leakage error and Purcell rate was then determined analytically, as discussed in Subsec. 5.2.2.

5.2.1 Simulations of the frequency shifting methods

Figure 5.3 displays simulations of the ideal box introduced in Subsec. 5.1.4 for wires of two different diameters. The wires with the larger diameter correspond to those currently used in our packages, whereas the smaller wires are a future version planned to enable greater extensibility.

The simulation results show a clear correlation between wire diameter and frequency shifting, where larger wires cause a larger shift for both methods. In the case of half-wave fencing, the

[6] See http://www.ansys.com/Products/Electronics/ANSYS-Q3D-Extractor for details on Q3D.

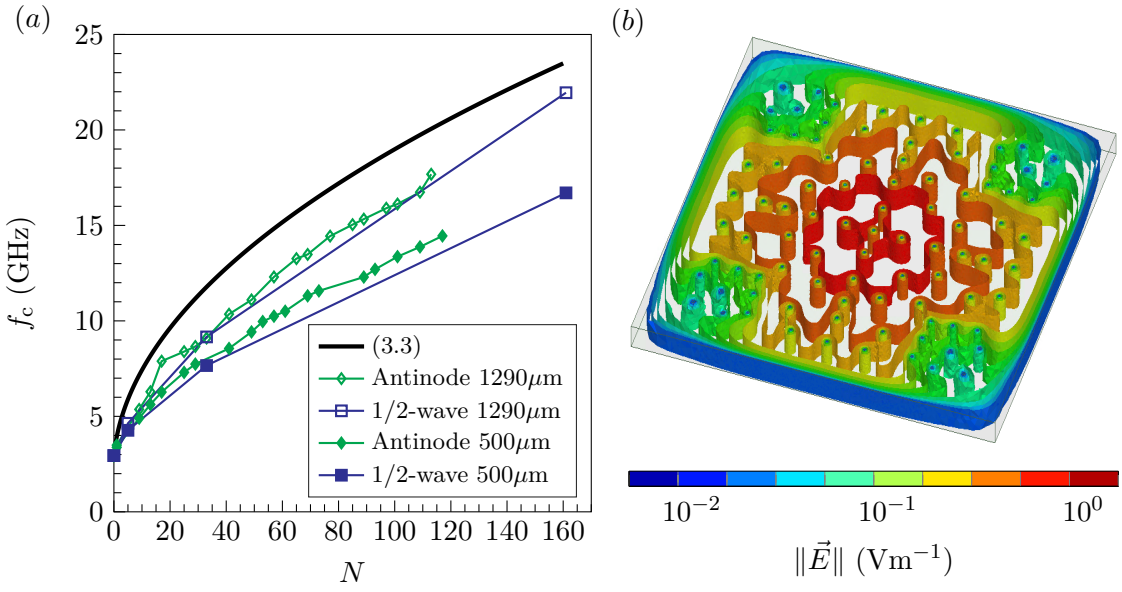

Figure 5.3: Simulation results of the frequency shifting methods. (*a*) f_c vs. N for the box dimensions given in Subsec. 5.1.4, corresponding to $f_{101} \approx 2.9\,\text{GHz}$. "1/2-wave": Half-wave fencing; "Antinode": Antinode pinning; pin dimensions indicated in the legend. The continuous solid black line plots Eq. 5.8, providing a pseudo-upper bound for all frequency shifting methods; the methods, however, are only simulated for values of N corresponding to integer values of d (symbols), both for half-wave fencing and antinode pinning. (*b*) $\|\vec{E}\|$ for the first resonant mode obtained with $N = 89$ and a pin diameter of 500 µm using the antinode pinning method; $f_c \approx 12.3\,\text{GHz}$. Note that the case $N = 89$ is obtained by extending the procedure depicted in Fig. 5.1 (*b*) and corresponds to iteration $d = 15$. This panel shows that certain modes are characterized by distributed antinodes such that the pin placement has to be chosen heuristically.

correlation is due to the fact that larger wires better approximate a solid wall, where each cell is more isolated from its neighbors. In addition, wires with a larger diameter modify the ideal square shape of the cell, perturbing the corresponding electric field and resulting in a higher f_c. This effect becomes more prominent with higher values of d as the wire is proportionally bigger than each new cell size. This effect is also present in the case of antinode pinning, as bigger wires create larger new zero-potential boundary conditions. As a consequence, the relative gap between Eq. 5.8 and simulations reduces with N.

We note that the antinode pinning method provides a slight advantage over the half-wave fencing method. However, the advantage is significant only when using wires with a smaller dimension. In fact, even an infinitesimally small wire would be sufficient to suppress an antinode, provided the perfect conductor assumption remains fulfilled.

The simulation results also support the reasoning behind resource optimization with respect to half-wave fencing. Consider Fig. 5.4(a) for $N = 33$ wires. The frequency $f_c(N = 33)$ obtained with half-wave fencing for 500 µm pins can be found in Fig. 5.3 (*a*), $f_c \approx 7.7\,\text{GHz}$. Consider

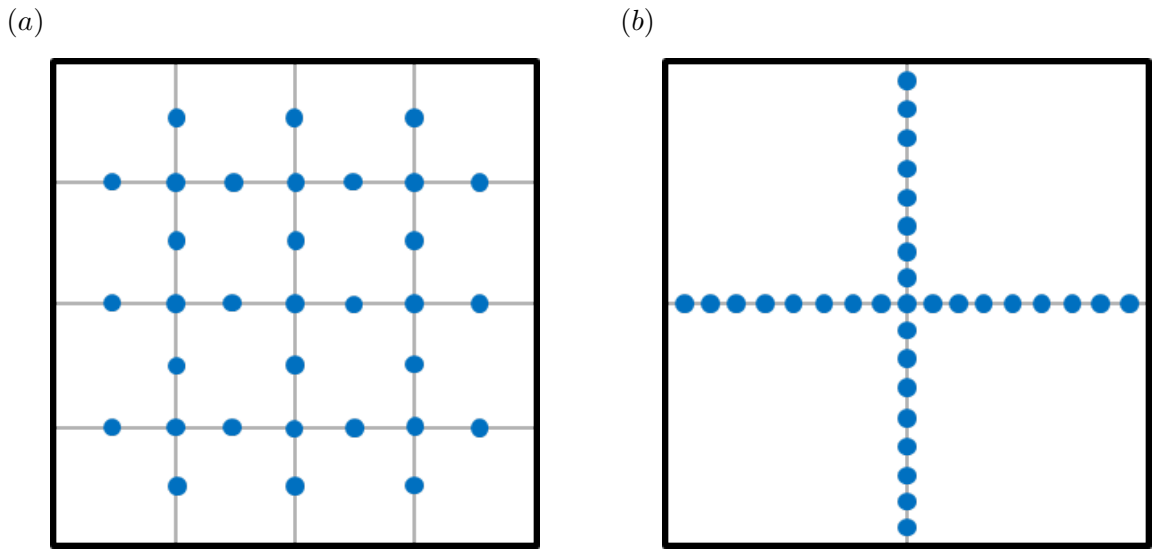

Figure 5.4: Two scenarios for N = 33 wires using half-wave fencing given the cavity simulated in Fig. 5.3. (*a*) $d = 2$ for the half-wave fencing method described in Subec. 5.1.2. Results in a $f_c \approx 7.7\,\text{GHz}$. (*b*) $d = 1$ using the 33 wires to instead generate maximally dense fence. In this case the maximum f_c can reach is 6 GHz.

Table 5.1: Approximate value of f_r for an "isolated box" and for a box perturbed by exposed dielectric or "perturbed system" as seen in Fig.5.5. In both cases, we apply the 1/5-wave fencing method for different iterations d.

d	f_c for isolated box (GHz)	f_c for perturbed system (GHz)
0	2.9	2.8
1	12.0	11.8

alternatively Fig. 5.4(b) using the same wire count, but a denser fence. Even assuming such a dense fense are perfect solid walls, the first mode resonance frequency for each of the four resulting cells would be 6 GHz. As such, it seems a more optimal approach is to implement further steps of the method with minimal fence density than to maximize said density to reach ideal isolation.

Figure 5.3 (*b*) displays an example of $\|\vec{E}\|$ for a box partially filled with coaxial pins, where only the outer conductor (the electrical ground) is accounted for. The electric field distribution clearly shows a situation where the optimal placement of the pins is made difficult by the complicated spatial distribution of the antinode.

Confirmation of Physical Realizations

When considering a package that houses a substrate enclosed in a similarly sized box, treating box and substrate modes separately is a suitable assumption only if the substrate surface is completely metalized. In real applications, typical circuit designs naturally result in regions of exposed dielectric that perturb the box modes. However, the ratio between the area of exposed dielectric and metalized ground plane is small enough not to significantly perturb the mode resonance frequencies. We confirm this argument by simulating a substrate patterned with abnormally large sections of exposed dielectric, as shown in Fig. 5.5. The results are compared to the idealized case, with and without the implementation of the frequency shifting methods.

When no methods are applied, the modes with lowest resonance frequency are those associated with the substrate due to its relative permittivity. In this case, we determine the box mode with lowest resonance frequency by plotting $\|\vec{E}\|$ for a few possible modes and selecting the one with closest resemblance to the TE_{101} box mode.

The following methods are then applied: 1/5-wave fencing for the box and 1/10-wave fencing for the substrate in combination with antinode pinning for $d = 2$ within each fenced cell [7]. In this manner, we ensure that the lowest substrate mode frequency is higher than the lowest box mode frequency. The simulation results are reported in Table 5.1. The impact of the exposed dielectric on f_c is $\approx 120\,\mathrm{MHz}$ for the bare box and $\approx 160\,\mathrm{MHz}$ with or without frequency shifting methods.

In order to understand whether the presence of superconducting circuitry can impact the frequency shifting methods significantly, we consider the quantum-mechanical interaction between the qubits and cavity modes in the dispersive regime. Assume an array of 1000 qubits all strongly, but (for simplicity) independently interacting with an unwanted cavity mode with coupling rate $g \sim 10\,\mathrm{MHz}$. Suppose a frequency shifting method results in $\Delta \sim 1\,\mathrm{GHz}$, the AC Stark shift of the mode resonance frequency due to each qubit is $\Delta f \sim (g^2/\Delta)\hat{\sigma}_z$, where $\hat{\sigma}_z$ is the usual Pauli matrix. Depending on the qubit state $\hat{\sigma}_z$ simply changes the sign of the Stark shift. Under these conditions, the total frequency shift can be estimated by multiplying the shift due to one qubit by 1000, resulting in $\Delta f \sim \pm 100\,\mathrm{MHz}$. This shift is similar to those generated by exposed dielectric reported in Table 5.1. Thus, we conclude that treating the box and substrate modes independently and, to a good extent, ignoring the design details of specific circuit layouts is a reasonable idealization.

To verify that our frequency shifting methods can be used for almost arbitrarily large cavities, we simulate half-wave fencing assuming two different boxes with dimensions $\mathcal{L} = 0.25\,\mathrm{m}$ and

[7] Note that, in this case, we cannot apply antinode pinning for $d = 1$ because the simulated circuit is located at the field antinode. Although this combination of methods is suboptimal in terms of frequency shifting, it is the easiest for the abnormal circuits considered in these simulations.

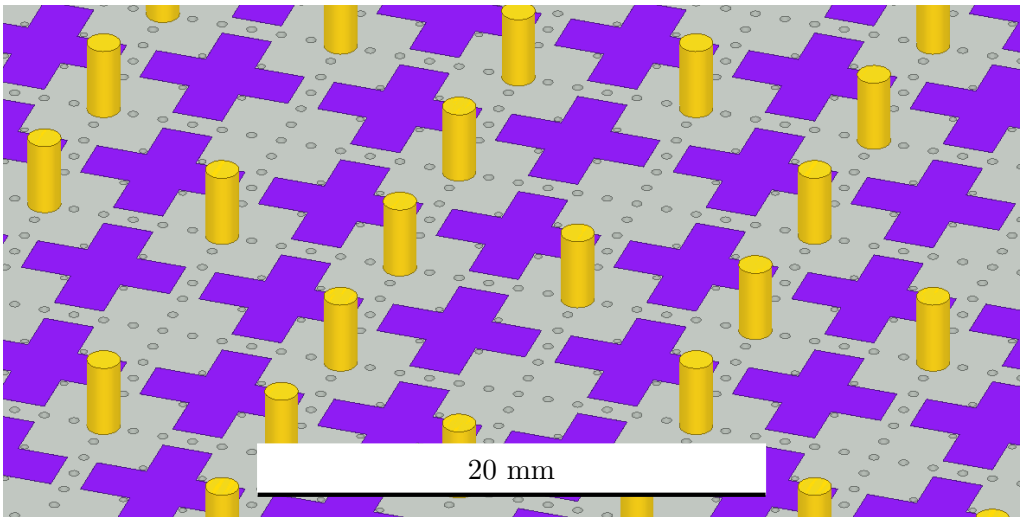

Figure 5.5: Model for the simulation of the impact of exposed dielectric. A square substrate and box both with dimensions given in the text; the substrate thickness is $t_s = 500\,\mu m$, with a relative permittivity $\varepsilon_r = 11.45$ (i.e., silicon at $\approx 4\,K$). The metalized surface (light gray) has a thickness of 100 nm. The exposed dielectric islands [blue (dark gray)] have a cross shape with arm length of 3 mm and width of 2 mm. The vias used to implement the combined frequency shifting methods on the substrate (see text for details) are visible as small open circles; the yellow cylinders represent the coaxial Pogo pins used to shift the box modes.

$\mathcal{L} = 1\,m$, in both cases with $h = 3\,mm$. For iteration $d = 5$, we find $f_c \approx 26.8\,GHz$ and $\approx 4.5\,GHz$ for the small and large box, respectively. We are not able to simulate larger values of d for the large box due to the computational cost of the simulation. Even though, in this case, $d = 5$ is insufficient to increase f_c above the typical qubit frequencies, the simulation trend shown in Table 5.2 is very comforting. In fact, by fitting the values in the table using Eq. 5.8 with a multiplicative reduction factor as a single fitting parameter (that accounts for the difference between theory and realistic simulations), we find that $d = 6$ results in $f_c \approx 8.7\,GHz$. From these results it seems to hold that the frequency shifting methods can be employed successfully for a cavity with arbitrarily large lateral dimensions.

5.2.2 Frequency shifting methods in a realistic quantum computing configuration

We consider a realistic quantum computing configuration, where a typical Xmon transmon qubit interacts with the modes of a box. The size of the box is purposely chosen to be sufficiently large such that $f_{101} < f_q$, thus resulting in the unwanted interaction between higher box modes and the qubit. In order to closely match the experimental scenario simulated in Subsec. 5.2.1, we choose $f_{101} = 3\,GHz$ and a fixed $f_q = 2f_{101} = 6\,GHz$. In this case and in absence of any additional zero-potential boundary conditions, the qubit is resonant with the fourth mode of

Table 5.2: Approximate value of f_c for two large boxes with different lateral dimensions $\mathcal{L}$ applying the half-wave fencing method for different iterations d.

d	f_c for $\mathcal{L} = 0.25\,\mathrm{m}$ (GHz)	f_c for $\mathcal{L} = 1\,\mathrm{m}$ (GHz)
0	0.9	0.2
1	1.2	0.3
2	2.1	0.5
3	4.5	0.9
4	10.6	2.0
5	26.8	4.5

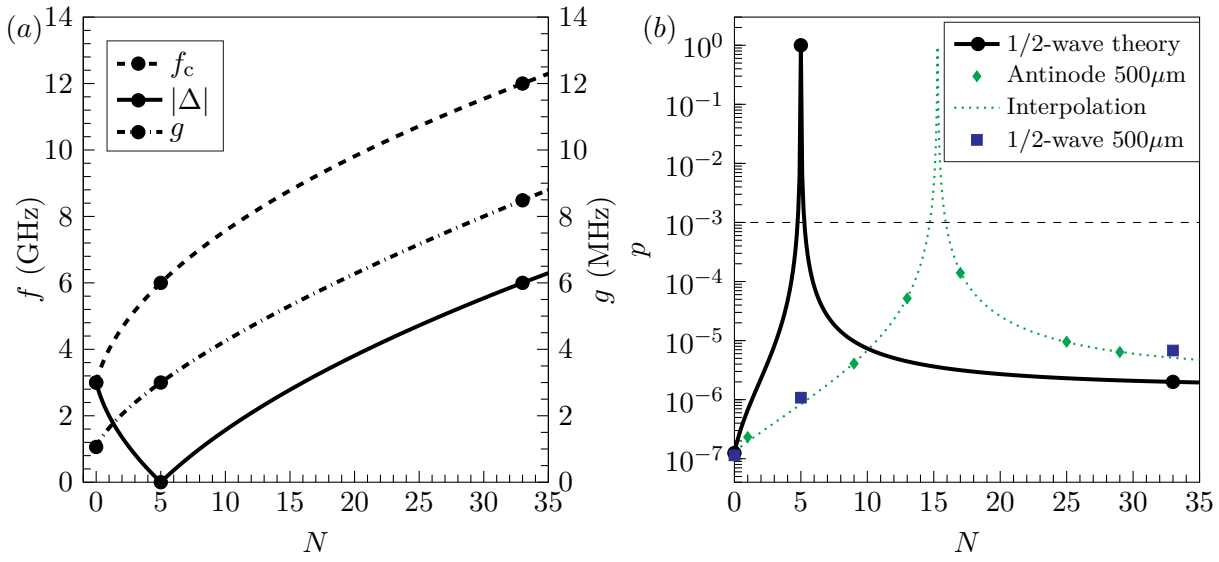

Figure 5.6: Parameters and efficacy of the frequency shifting methods (see Subsec. 5.2.2). For ease of understanding, lines are obtained assuming continuous values of N. Symbols are shown for actual iteration steps, d, of the methods. We choose $f_{101} = 3\,\mathrm{GHz}$, $f_q = 6\,\mathrm{GHz}$, and $g_{202} = g(N = 5) = 3\,\mathrm{MHz}$. The value $g(N = 0) \approx 1.1\,\mathrm{MHz}$ is extrapolated from $g(N = 5)$ using Eq. 3.20. (*a*) Left y-axis: Frequency $f = f_c$ and $f = |\Delta|$ vs. N. Right y-axis: g vs. N. (*b*) Error probability p vs. N for the theoretical values shown in (*a*), "1/2-wave theory", and for the simulated values in Fig. 5.3 (*a*) in the case of 500 µm pins. The dotted green line for the simulated values is obtained from a polynomial interpolation of the data in Fig. 5.3 (*a*), "Interpolation". The position of the maximum error probability $p = 1.0$ (peak) varies between the theoretical and simulated cases, since the zero-detuning condition is reached at different values of N. Due to the discrete nature of the frequency shifting methods, however, this condition is actually never reached. We note that p is the error probability caused by the dominant mode. In fact, leaving the box frequency unchanged, i.e., for $N = 0$, does not protect from all higher modes that can strongly interact with the qubit. Hence, the only relevant values of p to be considered are those to the right of each peak, as in this case all higher modes are further shifted in frequency from f_q. The horizontal dashed black line indicates $\bar{p}$.

the box, $f_q = f_{202}$. An upper bound for the coupling rate between this mode and the qubit is obtained from the simulations shown in Subsec. 5.1.5, $g_{202} = 3\,\text{MHz}$. This rate is comparable or larger than other typical qubit rates, possibly leading to significant coherent leakage errors.

These errors can be mitigated by the changing of Δ using the frequency shifted methods discussed previously. For simplicity, we focused on half-wave fencing as this method can easily be represented in analytical form. Figure 5.3 (a) displays f_c given by Eq. 5.8 and $|\Delta|$ as a function of N, where N is given by Eq. 5.7b. The discrete values of f_r increase with the corresponding values of N and, thus, of the iteration number d.

As shown in Fig. 5.1 (a), iteration $d = 1$ is realized for $N = 5$, resulting in $n_c = 4$. The qubit can be positioned at any point of any the four cells, where each cell is characterized by $f_r = f_q$. This corresponds to the *zero-detuning condition* for any of the four cell-qubit systems, $\Delta = 0$. For higher values of d, Δ increases (similarly to f_r) and a zero-detuning condition can never be reached again. This is due to the fact that we are considering the lowest resonant mode of each cell.

Assuming the qubit to be positioned at the electric field antinode of one of the four cells, we can choose the cell-qubit coupling rate to be $g(N = 5) = g_{202}$. This qubit position results in the strongest cell-qubit resonant interaction, leading to the highest coherent leakage error probabilities. As shown in Fig. 5.6 (a), g increases with N due to the functional dependence of Eq. 3.20 on f_c and, thus, on N. This effect partially counteracts the benefit of the half-wave fencing method, as for larger values of N the ratio $g(N)/\Delta(N)$ decreases at a slower rate than if g were independent from N.

The coherent leakage error probability p given by Eq. 5.4 for the values of Δ and g reported in Fig. 5.6 (a) is shown in Fig. 5.6 (b). This panel also shows an estimate of p for the values of f_c associated with half-wave fencing and antinode pinning for 500 µm pins found from the simulations in Fig. 5.3 (a). These values of f_c correspond to the lowest Δ for a given N among all scenarios simulated in Subsec. 5.2.1, thus resulting in an upper bound of p for the box-qubit configuration studied here. As an example, the simulated Δ obtained with half-wave fencing when $N = 33$ (i.e., $d = 2$) is sufficient to reduce p by more than two orders of magnitude compared to $\bar{p}$. A similar result is found for the simulated Δ due to antinode pinning when $N = 29$.

In the presence of damped cavity modes, our frequency shifting methods help reduce the ratio $\eta = \Gamma_r/\kappa$, where Γ_r is given by Eq. 5.5. The simulated values of g and Δ at $N = 33$ for half-wave fencing in the case of 500 µm pins, $g \approx 8.5\,\text{MHz}$ and $\Delta \approx 1.7\,\text{GHz}$, result in $\eta \approx 2.5 \times 10^{-5}$. It has been experimentally demonstrated that superconducting boxes can reach a quality factor $Q_c > 10^8$ [130], corresponding to $\kappa \sim 1\,\text{kHz} \ll g$. Under these conditions, coherent leakage represents the main error source due the box mode. It is not until a box damping rate $\kappa > 10g$ that qubit decoherence due to the dispersive Purcell effect should be considered. In fact, when $\kappa = 10g$ the resulting Purcell rate for the simulated values considered above is $\Gamma_r \approx 2.1\,\text{kHz}$, which is still

approximately two orders of magnitude lower than the most conservative Xmon transmon qubit energy relaxation rate $\gamma_r = 100\,\mathrm{kHz}$ [8]. In fact, a box with much higher κ (as long as $\kappa \ll \Delta$) would still not impact the qubit decoherence rate significantly.

5.3 Discussion

The choice of the optimal frequency shifting method depends on a variety of factors: The qubits operation frequency; the dominant mode frequency of the package's box; the number of input and output lines required to control and measure the qubits; the size of the coaxial Pogo pins. In addition, any constraints on the qubit circuit layout can impact the pin placement.

Naturally, the half-wave fencing method is well suited to grid-type architectures such as, e.g., that underlying the surface code. As an example, considering a 10×10 qubit array, the number of wires calculated from Eq. 5.7b does not match the required 250 wires for any value of d [9]. However, the half-wave fencing method can be generalized to a method where the box side $\mathcal{L}$ is divided by $n > 1$, the $1/n$-wave fencing method. In this case, the quantity 2^d in Eq. 5.7a and Eq. 5.7b has to be substituted by n^d, and $n_c = n^{2d}$. Notably, the functional dependence of f_c on N is given by Eq. 5.8 for any value of $n \in \mathbb{W}$. Following this approach it is possible to wire up any $n \times n$ qubit array, while simultaneously mitigating coherent leakage errors.

If the available number of wires is the limiting resource, antinode pinning is the ideal method of choice. In fact, it typically results in the greatest return on wire count, particularly when using small pins. Additionally, this is the most appropriate method when the constraints on the circuit layout are very restrictive. Suppose, for example, the user must initially place a set of wires at specific locations, ignoring any frequency shifting method. This scenario can be treated as the $d = 0$ iteration of the antinode pinning method, thus making the method suitable for cavities of arbitrary shape.

It is also worth noting that the two frequency shifting methods are not mutually exclusive. Instead, they can be combined depending on the user requirements. If the $1/n$-wave fencing method only partially meets the wire requirements of an arbitrary two-dimensional array of qubits, the wiring can be completed by means of antinode pinning. This, for example, is a good strategy when N does not correspond to any integer value of d in Eq. 5.7b. In this case, the available wires can be used to form as many fully $1/n$-wave fenced cells as possible, with the residual wires implementing antinode pinning.

We note that the effect of the frequency shifting methods on higher cavity modes must also be taken into account. In fact, the frequency shift relative to higher modes is less pronounced than

[8] This corresponds to a qubit relaxation time $T_1 = 10\,\mu\mathrm{s}$.

[9] Working under the design assumption of 1 XY-line, 1 Z-line and 1 readout line shared among 4 qubits.

for the dominant mode. This can result in a qubit being dispersively coupled to, e.g., m modes close to each other in frequency. In absence of any damping, we can assume these modes to act as multiple independent leakage channels. In this case, assuming a mean coherent leakage error probability $\langle p \rangle$ for each mode (this is a worst-case scenario assumption since p is smaller for higher modes), the total error probability can be estimated to be $\sim m\langle p \rangle$. According to the results in Fig. 5.6 (b), we can easily tolerate up to $m \sim 100$.

In order to clearly show the effect of higher cavity modes on the operation of one qubit, we consider a box with $f_{101} = 3\,\mathrm{GHz}$ and sweep f_q over a wide range from 1 to 20 GHz, which comprises 60 box modes for a bare box (i.e., where no frequency shifting method is applied). Among these 60 modes, 27 are degenerate and thus discarded. When assuming maximum qubit coupling by positioning the qubit at the mode antinode, it is physically impossible to simultaneously couple the qubit to any pair of degenerate modes [10]. Figure 5.7 is generated using Eq. 5.4 for each of the 33 modes. In the dispersive regime regions, the total error probability p_tot is obtained by summing the error probability of all modes assuming the probabilities to be independent from each other; in the semi-resonant regime regions, p_tot is that of the only mode on or close to resonance with the qubit. The plot in Fig. 5.7 (a) further clarifies that the low error probability for $f_\mathrm{c} \ll f_\mathrm{q}$ in the case of a bare box, as shown in Fig. 5.6 (b), is only possible when considering the coupling to the lowest resonant mode. However, the presence of higher modes for the same box size is highly detrimental to the qubit operation. The plot in Fig. 5.7 (b) demonstrates that half-wave fencing for $d = 2$ makes it possible to operate the qubit safely at all frequencies $< 10\,\mathrm{GHz}$, since the resonance frequency of the lowest and of all higher box modes is well above this frequency.

In presence of damped cavity modes, the scenario differs depending on the magnitude of the damping rate of each mode. In case of low damping, i.e., κ is much smaller than the frequency separation between two consecutive modes up to a cutoff mode $\overline{m}$ (for higher modes the detuning is large enough that the dispersive Purcell rate associated with them can be neglected), the total dispersive Purcell rate for these modes is given by $\sim\sum_{j=1}^{\overline{m}} \Gamma_{\mathrm{c}j}$, where $\Gamma_{\mathrm{c}j}$ is the Purcell rate of the j-th mode [131]. For example, assuming a mean dispersive Purcell rate $\langle\Gamma_\mathrm{c}\rangle\sim 1\,\mathrm{kHz}$ for all modes up to $\overline{m}$ (see estimate in Subsec. 5.2.2), we can tolerate up to $\overline{m} \sim 100$ before the Purcell rate starts impacting qubit decoherence. When κ becomes large enough that the modes strongly overlap with each other, then this set of modes should be treated as a continuous mode distribution.

An unwanted cavity mode can also mediate interactions between pairs of (or even multiple) qubits. The corresponding dynamics can lead to correlated errors. The frequency shifting methods introduced here allow the separation of the qubits transition frequency from the cavity resonance frequency such that the qubit-cavity-qubit interaction gives rise only to virtual transitions. This result is similar to the dispersive two-qubit $\sqrt{j\mathrm{SWAP}}$ gate introduced in [29]. Assuming both qubits are coupled with the same coupling coefficient g to the cavity mode, the

[10] Mode mnl is degenerate with lnm.

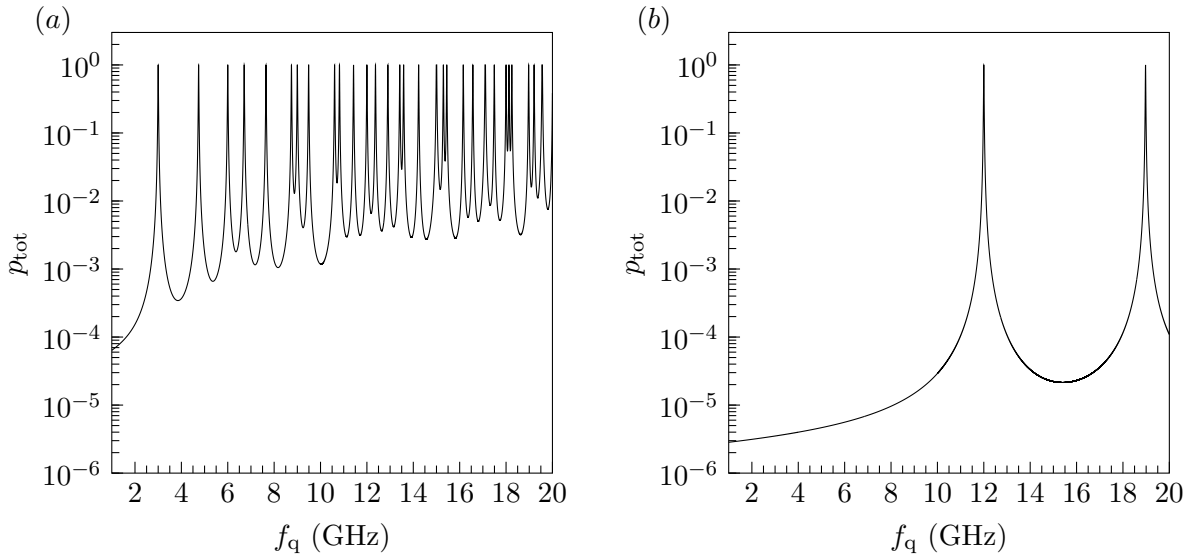

Figure 5.7: Qubit operation in presence of multiple nondegenerate box modes. The plots are obtained by sweeping continuously $f_{\rm q}$ in Eq. 5.4 for the first 33 modes of the bare box [panel (*a*)] and for the first two modes of the modified box [panel (*b*)] (see details in the main text about the probability summation method). The resonance frequencies of the modes are obtained from Eq. 5.6, with $f_{101} = 3\,\text{GHz}$ for the bare box. For simplicity, we choose $g = 10\,\text{MHz}$ for all modes in the case of the bare and modified box. This choice of g approximately captures the fact that higher modes have a larger zero-point electric field [29]. In real applications, the value of g varies for each mode due the qubit being at a different frequency and possibly not being positioned at the antinode of that mode. In fact, it is impossible to position the qubit at the antinode of all modes at the same time (at most the qubit can be positioned close to the antinode of several modes simultaneously). In both panels, we display $p_{\rm tot}$ vs. $f_{\rm q}$. (*a*) Bare box. (*b*) Box modified by means of the half-wave fencing method for $d = 2$. Simulations for both cases ignored thermal excitations.

worst case scenario is when the qubits are in resonance with each other and detuned by Δ from the mode. The effective qubit-qubit coupling strength is then g^2/Δ (dispersive coupling), which is strongly suppressed for values of Δ larger than several times g.

Our frequency shifting methods are directly applicable to the problem of dielectric substrate modes, which has been addressed qualitatively in [123]. In this case, the resonance frequency of the substrate modes is given by Eq. 5.6 replacing c with $c/\sqrt{\varepsilon_{\rm r}}$, where $\varepsilon_{\rm r}$ is the relative permittivity of the substrate. The pins must be replaced by superconducting vias [70, 73], with all other methodological requirements remaining unchanged. The number of vias embedded in the substrate will need to be significantly higher than the number of pins in free space due to the lower frequency of the dominant mode. Though as fabricating a large array of vias is a relatively simple process that can be made compatible with standard qubit fabrication techniques, this greater density isn't overly problematic.

Finally, it is worth commenting on the possibility to reduce leakage errors due to unwanted

cavity modes by decreasing the cavity-qubit coupling rate g. There are three main mechanisms to reduce g: First, place the qubits only in proximity of cavity field nodes; second, increase H thereby decreasing Eq. 3.20; third, modify the qubit geometry to decrease β (see Subsec. 5.1.5). The first approach is impractical as it severely limits the available space on the chip. In order to be useful, the second mechanism can easily lead to new unwanted cavity modes. In the case of transmon qubits, the third mechanism strongly affects the qubit charging energy possibly having detrimental effects on its decoherence properties and anharmonicity. For these reasons it is best to focus on Δ for the purposes of reducing leakage error.

5.4 Conclusion

Expanding upon the theory presented in Sec. 3.5, a system independent metric of an ideal system for measuring error due to coherent leakage was presented. The dispersive Purcell rate was also presented to cover scenarios in which the system is non-ideal. The two frequency shifting methods to mitigate these sources of error, half-wave fencing and antinode pinning, were explained, including a guide on the iterative steps necessary to implement them. For a proper analysis on the efficacy of these methods, a realistic coupling strength is necessary for determining the resulting error metric. This was accomplished through classical simulations of the cavity-qubit system while sweeping the "qubit" frequency through that of the cavity and fitting the resulting anti-crossing to the Jaynes-Cummings dressed states.

Implementations of the frequency shifting methods were then simulated using a realistic system and the three-dimensional wires of the quantum socket (both the current version and potential future designs). The reliability of these results for comparison to real world system were confirmed through simulating non-ideal systems with extreme profiles to maximize potential detriments to the frequency shifting methods. The results showed the methods were very reliable for practically any microwave packaging system used for quantum computing. Using the resulting detuning value from these simulations allowed for predicting the coherent leakage error rate and the dispersive Purcell rate. It was clearly shown that near term microwave packages, for ≈ 100 qubits, can be easily modified so as to prevent any impact on qubit error from these two sources. Such that, merely through the wiring of the qubits, these error sources can be mitigated to far below the current best error rate achievable in the field. Further, that future microwave packages would still be able to negate these error sources through further iterations of the frequency shifting methods, regardless of the wiring implementation pursued.

Chapter 6

Conclusion

In a recent work [43], seven sequential stages necessary to the development of a quantum computer were introduced. Currently, the next stage to be reached is the implementation of a single logical qubit characterized by an error rate that is at least one order of magnitude lower than that of the underlying physical qubits. In order to achieve this task, a two-dimensional lattice of 10×10 physical qubits with an error rate of at most 10^{-3} is required [26]. As has been discussed throughout this work, an array of such a size begins to suffer from the scaling issues of both the wiring problem and leakage errors.

We have shown a promising solution to the wiring problem in the form of the quantum socket [1]; the three-dimensional wires operated well at microwave frequencies in the cryogenic environment necessary for superconducting quantum computing. We showed successful measurements of high quality superconducting resonators at single photon power levels, suggesting the quantum socket is compatible with qubit operations. This is further supported by the recent work from IBM and NIST [121] which used a variation on the quantum socket to successfully control and measure 7 non-tunable Xmon transmon qubits. While undesirable contact resistance of the three-dimensional wires does make them less optimal for use with tunable Xmon transmon, designs for future versions of the wires have been modified in a bid to lower said resistance.

For combating the issue of leakage errors, we proposed two methods, half-wave fencing and antinode pinning, that allow us to reduce the effect of unwanted cavity modes by means of the same wires used for qubit control and measurement [2]. For example, the 250 wires required to operate a 100 qubit processor make it possible to reach coherent leakage error probabilities of $\sim 10^{-5}$, which are significantly lower than the state-of-the-art error probabilities for superconducting qubit operations. Similarly, our methods allow us to reduce the effect of damped modes below the typical decoherence rates of superconducting qubits. Our simulations demonstrate that unwanted modes for boxes as big as $1\,\mathrm{m} \times 1\,\mathrm{m}$ can be mitigated using the frequency shifting methods. It is worth noting that our methods can also be combined with the modular architecture proposed

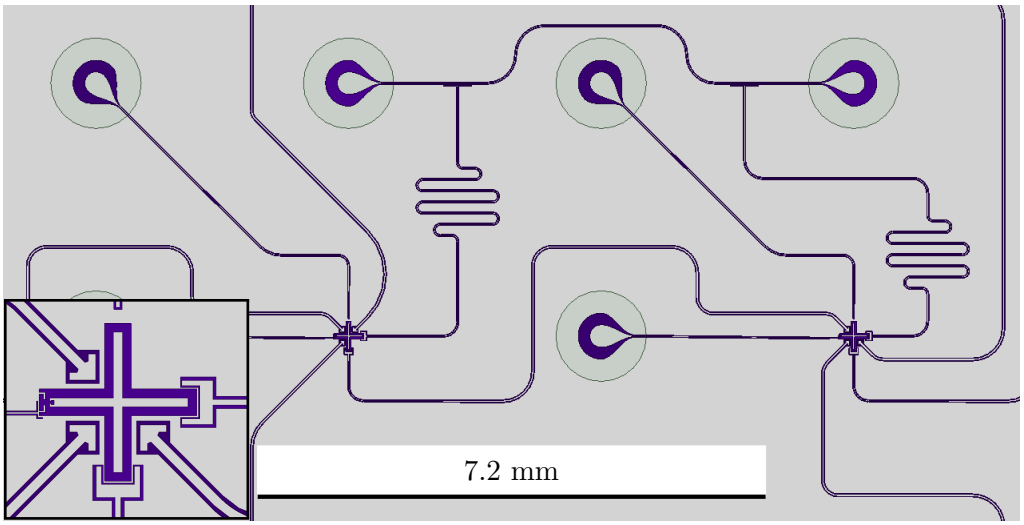

Figure 6.1: One unit cell of an array of Xmon transmon qubits coupled by nearest neighbor interactions and compatible with 1/10-wave fencing (and any arbitrary $1/n$-wave fencing). The circles enclosing the contact pads show the footprint of the coaxial pins. Inset: Detail of the Xmon transmon qubit with capacitive couplings to the XY, measurement, and inter-qubit coupling resonators, as well as inductive-galvanic coupling to the Z line. ©2018 IOP Publishing

in Ref. [64], where boxes containing hundreds of qubits are coupled together to form systems with thousands of qubits. Our frequency shifting methods can also be used to mitigate the effects of substrate modes, another important source of errors in extensible superconducting qubit architectures.

These two solutions can be combined to enable a fully scalable system. Let us consider the $1/n$-wave fencing method using the three-dimensional wires of the quantum socket. This enables the generalization to a repeatable cell structure, as seen in Fig. 6.1 which would be easily compatible with the grid-type architectures necessary for the surface code. In said figure, two Xmon transmon qubits can be seen along with 6 wires. Two of said wires provide connection to the XY-lines, two to the Z-lines, and the remaining two for a shared readout line. Using this cell to generate a 10×10 array of Xmon transmon qubits would give the equivalent to a 1/10-wave fencing for $d = 1$. A simulation of this configuration resulted in $f_c \approx 29.7\,\mathrm{GHz}$, easily mitigating any problems with coherent leakage error. The unit cell can be repeated to form much larger arrays while maintaining $f_c \gg f_q$. This would effectively provide an extensible architecture which solves both the wiring problem and that of leakage error to a scale at which new scaling issues become the bottleneck.

6.1 Future Work

Near term goals for the continuation and expansion of this work would be the measurement of a tunable superconducting qubit using the quantum socket. Managing to show that no significant impact to the qubit's decoherence rate or gate fidelities would be the ideal result of such measurements. This is currently ongoing in the DQM laboratory, with initial qubit measurements having been completed. Full characterization is targeted for midsummer 2018.

Experimental confirmation of the frequency shifting methods is another near term goal. Following the measurement steps provided by Ref. [132], and making use of a cavity-qubit system in which additional pinning locations could be easily introduced, would provide such confirmation. Including a tunable qubit and sweeping it near cavity resonance would provide data which the analytical and simulated data of Subsec. 5.2.2 could be compared against.

Mid term goals would be the combination of both of these systems towards the purpose of generating a functional logical qubit. A system based on the quantum socket which could support a very simple logical qubit was reported on in Ref. [121], though the package used in that work did not account for leakage error. This work could be expanded on by implementing a quantum socket which, incorporated a frequency shifting method, a chip of ≈ 20 qubits, and included frequency shifting methods to mitigate substrate modes. This would confirm that the solutions provided in this thesis are feasible for the generation of a basic logical qubit.

The long term goal would be expanding the mid term system up to the qubit count necessary for a logical qubit with error rates better than the physic qubits which make up said logical qubit. Using the design shown in Fig. 6.1 to the necessary array size, $\approx 100 \times 100$ would allow for not only showing the efficacy of the solutions provided in this thesis, but give the necessary experimental results to show the effectiveness of superconducting quantum computing and the surface code.

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Appendix A

Coplanar Waveguide Expanded

A more in depth review on superconductive coplanar transmission lines, as was presented in the author's comprehensive report, is presented below. It is included for the sake of completeness, so the inquisitive reader can find all potentially necessary information in one document, but is not required for understanding the work presented in this thesis.

The design of a superconducting microwave circuit follows the same steps as with standard conductive material but for a slight modification. This modification is achieved by making use of the two fluid model of superconductivity [133, 96]. It should be noted the two fluid model only holds when operating below the gap frequency of the superconductor and far from the critical temperature. The material parameters of the superconductor can also be derived from the Mattis-Bardeen formula, but require that the coherence length be large compared to the London penetration depth of the superconductor [134].

The two fluid model simply accounts for both the superconducting charge carrier density (being the Cooper pairs, the density of which can be seen as $|\Psi|$ from Eq. 2) and the normal conductive channel, with the ratio of the two being temperature (relative to the critical temperature T_c) and total charge density n_0 dependent, as can be clearly seen from Eq. A.1 and A.2 which are the Gorter-Casimir expressions.

$$n_\mathrm{s}(T) = n_0 \begin{cases} 0 & T \geq T_\mathrm{c} \\ 1 - \left(\frac{T}{T_\mathrm{c}}\right)^\gamma & T \leq T_\mathrm{c} \end{cases} \tag{A.1}$$

$$n_\mathrm{n}(T) = n_0 \begin{cases} 1 & T \geq T_\mathrm{c} \\ \left(\frac{T}{T_\mathrm{c}}\right)^\gamma & T \leq T_\mathrm{c} \end{cases} \tag{A.2}$$

where γ is a phenomenological constant based on the material being used (which for simple s-wave LTS materials, $\gamma = 4$). From this model, the surface resistance ($R^t_{\mathrm{s,sc}}$) and surface reactance ($X^t_{\mathrm{s,sc}}$) of the superconducting film at angular frequency $2\pi f$ can be found from

$$R^t_{\mathrm{s,sc}} = \frac{1}{\delta_{\mathrm{sc}}\sigma_{\mathrm{n}}}\left(\frac{\lambda_{\mathrm{L}}}{\delta_{\mathrm{sc}}}\right)^3 \frac{\sinh\left(\frac{2t}{\lambda_{\mathrm{L}}}\right) + \left(\frac{\delta_{sc}}{\lambda_{\mathrm{L}}}\right)^2 + \sin\left(\frac{2t\lambda_{\mathrm{L}}}{\delta^2_{\mathrm{sc}}}\right)}{\sinh^2\left(\frac{t}{\lambda_{\mathrm{L}}}\right) + \sin^2\left(\frac{t\lambda_{\mathrm{L}}}{\delta^2_{\mathrm{sc}}}\right)} \tag{A.3}$$

$$X^t_{\mathrm{s,sc}} = \frac{1}{2}2\pi f\mu_0\lambda_{\mathrm{L}} \frac{\sinh\left(\frac{2t}{\lambda_{\mathrm{L}}}\right) - \left(\frac{\lambda_{\mathrm{L}}}{\delta_{\mathrm{sc}}}\right)^2 \sin\left(\frac{2t\lambda_{\mathrm{L}}}{\delta^2_{\mathrm{sc}}}\right)}{\sinh^2\left(\frac{t}{\lambda_{\mathrm{L}}}\right) + \sin^2\left(\frac{t\lambda_{\mathrm{L}}}{\delta^2_{\mathrm{sc}}}\right)} \tag{A.4}$$

where $\sigma_{\mathrm{n}}(T)$ is the conductivity of the normal channel of the superconductor, $\lambda_{\mathrm{L}}(T)$ is the temperature dependent london penetration depth, and $\delta_{\mathrm{sc}}(2\pi f, T)$ is the skin depth of the superconductor in the normal channel and are found from

$$\sigma_{\mathrm{n}}(T) = \begin{cases} \sigma_0 & T \geq T_{\mathrm{c}} \\ \sigma_0(\frac{T}{T_c})^\gamma & T \leq T_{\mathrm{c}} \end{cases} \tag{A.5}$$

$$\lambda_{\mathrm{L}}(T) = \begin{cases} \infty & T \geq T_{\mathrm{c}} \\ \frac{\lambda_{\mathrm{L}}(0)}{\sqrt{1-(\frac{T}{T_{\mathrm{c}}})^\gamma}} & T \leq T_{\mathrm{c}} \end{cases} \tag{A.6}$$

$$\delta_{\mathrm{sc}}(2\pi f, T) = \sqrt{\frac{2}{2\pi f\mu_0\sigma_{\mathrm{n}}(T)}} \tag{A.7}$$

where σ_0 is the DC conductivity at T just above T_{c}. The surface resistance and reactance (or real and complex components of the surface impedance) are just properties of the material and independent of CPW structure geometries. They do not directly give any of the values for the circuit model of Fig. A.1. However using these values as a ratio against the circuit resistance and inductance does enable us to determine one of our necessary values for calculating the characteristic impedance of our CPW,

$$\frac{R_{\mathrm{sc}}}{R^t_{\mathrm{s,sc}}} = \frac{2\pi f L_{dx,\mathrm{k}}}{X^t_{\mathrm{s,sc}}}. \tag{A.8}$$

This ratio equivalence makes sense when realizing that the series resistance and series inductance (the kinetic and external, presuming the use of a standard substrate) are only dependent

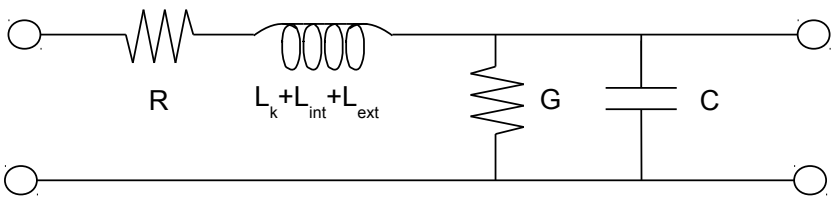

Figure A.1: Equivalent lumped element circuit model for superconducting transmission line.

on the conductive material. The shunt capacitance and admittance however are dependent on the substrate material being used, as is easily recognized by recalling that the basic equation for parallel plate capacitors includes the permittivity of the insulating material. For a CPW of finite substrate thickness the shunt capacitance (C_{dx}) is found from

$$C_{dx} = 2\varepsilon_0(\varepsilon_\mathrm{r} - 1)\frac{K(k_1)}{K(k_1')} + 4\varepsilon_0\frac{K(k_0)}{K(k_0')} \tag{A.9}$$

where $K(x)$ is the complete elliptical integral of the first kind, ϵ_0 is the free space permittivity, ε_r is the substrate dielectric constant and k_0, k_0', k_1, and k_1' are found from

$$k_0 = \frac{s}{s+2w} \tag{A.10}$$

$$k_0' = \sqrt{1-k_0^2} \tag{A.11}$$

$$k_1 = \frac{\sinh\left(\frac{\pi s}{4h}\right)}{\sinh\left(\frac{\pi(s+2w)}{4h}\right)} \tag{A.12}$$

$$k_1' = \sqrt{1-k_1^2} \tag{A.13}$$

where s, h and w are the geometric dimensions of the CPW, as seen in Fig. 2.1. It should be noted this approach is for a 'conventional' CPW, meaning the metallic thin film is treated as having zero thickness. This simplification is relatively accurate provided the actual film thickness is a couple orders of magnitudes less than s+2w. If the film thickness becomes larger than this, the shunt capacitance begins to increase and must be accounted for [84, 85, 86].

The shunt conductance (G_{dx}) in an ideal scenario can be ignored, as a perfect substrate would have no dielectric loss. This is of course never the case, but is often treated as such if the loss mechanisms are dominated by other components besides the dielectric. The shunt conductance is found from

$$G_{dx} = 2\pi f\, C_{dx}\, q \tan(\delta) \tag{A.14}$$

where $\tan(\delta)$ is the loss tangent of the dielectric substrate and q is the filling factor. This filling factor gives the amount of the electric field penetrating the substrate (compared to the amount that is in vacuum)

$$q = \frac{1}{2}\frac{K(k_1)K(k_0{}')}{K(k_1{}')K(k_0)} \tag{A.15}$$

The series inductance (L_{dx}) is found from the sum of both the external inductance ($L_{dx,ext}$) and (in the case of superconductive material) the kinetic inductance ($L_{dx,k}$). The external inductance accounts for the magnetic energy outside the conductive material (the magnetic field present in the substrate/vacuum) and is found from

$$L_{dx,\mathrm{ext}} = \frac{\mu_0}{4}\frac{K\left(k'\right)}{K\left(k\right)} \tag{A.16}$$

where μ_0 is the free space permeability, $4\pi 10^{-7}$ H/m. The kinetic inductance, in the simplest description, is the kinetic energy of the Cooper pairs. The Cooper pairs have inertia, and so it takes some amount of energy and time for their direction of travel to change. This can be related to a series inductor as it has an equivalent reactance and so can be represented in this manner. The kinetic inductance is found from

$$L_{dx,\mathrm{k}} = \frac{\mu_0 \lambda_{\mathrm{L}} C'}{4A'D'K(k_0)} \times \left(\frac{1.7}{\sinh\left(\dfrac{t}{2\lambda_{\mathrm{L,eff}}}\right)} + \frac{0.4}{\sqrt{\left[\left(\dfrac{B'}{A'}\right)^2 - 1\right]\left[1 - \left(\dfrac{B'}{D'}\right)^2\right]}} \right) \tag{A.17}$$

$$A' = -\frac{t}{\pi} + \frac{1}{2}\sqrt{\left(\frac{2t}{\pi}\right)^2 + s^2} \tag{A.18}$$

$$B' = \frac{s^2}{4A'} \tag{A.19}$$

$$C' = B' - \frac{t}{\pi} + \sqrt{\left(\frac{t}{\pi}\right)^2 + w^2} \tag{A.20}$$

$$D' = \frac{2t}{\pi} + C' \tag{A.21}$$

The effective London penetration depth is found from

$$\lambda_{\mathrm{L,eff}}(T,t) = \lambda_{\mathrm{L}}(T)\coth\left(\frac{t}{2\lambda_{\mathrm{L}}(T)}\right) \sim \frac{\lambda_{\mathrm{L}}(T)^2}{t} \tag{A.22}$$

This is a somewhat simplified formulation for the effective London penetration depth, but accurate enough for a CPW transmission line design. Generally, provided all of the conductor dimensions (including film thickness) are larger than $2\lambda_{L,\mathrm{eff}}$, the kinetic inductance will be quite small compared to the external inductance and the circuit analysis is over all straight forward. For the cases where film thickness (or other dimensions) is below this bound is discussed briefly in Appendix B.3.

With all of the circuit model values having been determined, the characteristic impedance can be found from

$$Z_0 = \sqrt{\frac{R_{dx} + j2\pi f\left(L_{dx,\mathrm{k}} + L_{dx,\mathrm{ext}}\right)}{G_{dx} + j2\pi f C_{dx}}} \tag{A.23}$$

The circuit values that are found are for a unit length of transmission line. To determine the value for a length of transmission line, the calculated value is multiplied by that length. When actually designing a CPW thin film circuit, a target characteristic impedance will already be in mind and the film/substrate thickness will be somewhat set based on material and fabrication restrictions. This leads to the ratio between the center line width (s) and the gap width (w) being the parameter by which to design the desired characteristic impedance. The analysis can also be somewhat simplified as both the resistance (R_{dx}) and conductance (G_{dx}) can usually be ignored. The kinetic inductance ($L_{dx,\mathrm{k}}$) will play a very small role in the total inductance provided the geometries are all relatively large compared to the coherence length and penetration depth, so can also be disregarded. It is also important to keep in mind any limitations that are imposed by fabrication methods, as both the resolution and critical dimension of a final product will be dependent on everything from the mask quality to the etching technique employed.

Appendix B

Signal Loss and Interference

A review on transmission line attenuation, parasitic modes and airbridges, and concerns due to superconducting properities, as was presented in the author's comprehensive report, is presented below. It is included for the sake of completeness, so the inquisitive reader can find all potentially necessary information in one document, but is not required for understanding the work presented in this thesis.

B.1 Attenuation

Attenuation of a signal, be it in a planar transmission line or cavity resonator, can be detrimental to system performance. When dealing with signals that are approximately only a single photon in power, it can be disastrous, as the attenuation relates more to the probability of your signal disappearing rather than just a drop in power. For the case of a CPW transmission line, the attenuating component of the circuit can be simplified to a single value, being the real component (α, the attenuation constant) of the transmission lines propagation constant

$$\gamma = \sqrt{\left(R_{dx} + j(2\pi f)(L_{dx,k} + L_{dx,ext})\right)\left(G_{dx} + j(2\pi f)C_{dx}\right)} = \alpha + j\beta \tag{B.1}$$

where γ is from the solution of the Telegrapher's equation

$$\begin{array}{lll} \frac{\partial^2 V(x)}{\partial x^2} = \gamma^2 V(x) & \Rightarrow & V(x) = V^+ e^{-\gamma x} + V^- e^{\gamma x} \\ \frac{\partial^2 I(x)}{\partial x^2} = \gamma^2 I(x) & \Rightarrow & I(x) = \frac{1}{Z_0}\left(V^+ e^{-\gamma x} - V^- e^{\gamma x}\right) \end{array} \tag{B.2}$$

One can then predict the attenuation for the designed transmission line. Other derivations at a more accurate attenuation constant for a superconducting CPW (only looking at the conductive losses) have been attempted, such as Eq. B.3 from Ref. [135],

$$\alpha \approx \frac{R_{sm} b^2}{16 Z_0 \left(K\left(a/b\right)\right)^2 \left(b^2 - a^2\right)} \left\{ \frac{1}{a} \left(\frac{2a\left(b-a\right)}{\Delta(b+a)} \right) + \frac{1}{b} \ln \left(\frac{2b\left(b-a\right)}{\Delta(b+a)} \right) \right\} \tag{B.3}$$

where Δ is the stopping distance based on the local edge geometry and determined numerically [136, 80], R_{sm} is a modified surface impedance and

$$\begin{aligned} 2b &= s + 2w \\ 2a &= s \end{aligned} \tag{B.4}$$

$$R_{sm} = \mu_0 2\pi f t \mathrm{Im} \left(\frac{\cot\left(k_c t\right) + \csc\left(k_c t\right)}{k_c t} \right) \tag{B.5}$$

where k_c is the complex wavenumber

$$k_c^2 = \left(\frac{1}{\lambda} \right)^2 + 2j \left(\frac{1}{\delta_{sc}} \right) \tag{B.6}$$

The caveat to the attenuation determined from these methods is that it is not power dependent. If only operating at (relatively) high power, on the order of 10^6 photons or greater, this is not an issue (presuming not exceeding the capacity of the superconductor of course). At lower power levels, two level system loss begins to play a significant role in signal degradation.

B.2 Parasitic Modes

As was briefly mentioned, one of the issues that can arise when using CPWs is the presence of various parasitic modes and floating grounds. A completely symmetric and ideal CPW transmission line will only have the fundamental ('even mode') quasi-TEM mode present. The frequency dispersion of this mode is quite low (necessary for when needing to send nanosecond Gaussian pulses) and the electromagnetic field distribution is tightly confined around the center conductor.

A second mode can occur in some instances that does not have these benefits, suffering from poor dispersion and a much larger field distribution, as discussed in Ref. [81]. This parasitic slotline mode (or 'odd mode') is a side effect caused by the two ground planes having mismatched voltage or an asymmetric distribution of the electromagnetic field. Coupling between the two

modes is highly undesirable, and steps must be taken to minimize the coupling and likelihood of the slotline mode forming.

Ideally the ground planes are always at zero voltage, but practically this will never be the case, especially with a complex circuit layout. Three likely causes of a slotline mode are:

- *Bend in the transmission line.* If the geometries of the transmission line are on the order of the wavelength of the signal being carried, any deviation from a straight path could generate a slotline mode. If the ratio between the difference in length of the two slot paths and the wavelength of the signal is significant ($\Delta l/\lambda$>0.1) the electric field on either side of the conductive line will be out of phase, leading to a difference in voltage between the two ground planes [137, 138].

- *Discontinuities.* A break or sudden change in the ground plane will generate slotline modes. A gap in the ground plane can actually be considered a slotline mode waveguide, and will result in part of the transmitted signal being sent along this gap as a slotline mode. The change of impedance of the transmission line at this gap will also result in a reflection plane. A completely enclosed ground discontinuity (as in a floating ground that has no conductive contact with the rest of the ground of the circuit) will exacerbate this issue and lead to unwanted coupling between different circuit components, as the floating ground acts as a capacitive island [139, 137].

- *Asymmetry of the ground planes.* The ground plane widths being unequal will lead to an asymmetric distribution of the electromagnetic field. This field will be a summation of both the odd and even mode. As the mismatch between the ground plane widths increases, so too will the amount the slotline mode composes of the total field. The mismatch will have less of an effect if the ground plane widths are significantly larger than the CPW geometries (as in s and w) [140].

Although some of these instances can be avoided through smart design of the circuit layout, it will be impossible to completely do so as circuit complexity increases. However, a number of the various solutions to the wiring problem present viable solutions, including the three-dimensional wires presented in this work. High quality air bridges is one solution, being included as a step in the lithographic fabrication process [81, 137, 141]. The approach of wafer bonding, be it using indium bump bonds or full thermocompressive wafer bonding [59, 97] provides a means by which to provide short electrical length connections between areas of ground that could be at different voltages.

B.3 Superconducting Considerations

The critical current of thin film devices can differ from that of the bulk superconductor material. When the dimensions of the superconducting circuit fall below that of the penetration depth and/or coherence length, many of the bulk critical values are no longer applicable. For thin films, the superconductor may behave as a pseudo 2-dimensional object, with all values being constant in the z-axis [142]. With the film that thin, the effective penetration depth must be considered instead of the regular London penetration depth. If the width of the circuit falls below two times the effective penetration depth (known as the Pearl length), instead of the critical current, it is more useful to consider the critical sheet current at zero temperature ($K_{c,clem}$) [143]

$$K_{c,clem} = \frac{\Phi_0}{\rceil \pi \mu_0 \xi \Lambda} \tag{B.7}$$

where Φ_0 is the magnetic flux quantum, and $\rceil$ is Euler's number. This analysis is reached by considering the Gibbs free energy barrier is preventing the nucleation of vortices. As the current increases, the energy barrier decreases and allows for a vortex to traverse the circuit, generating voltage.

Vortices, a 'hurricane' of electrons circling a flux quanta that is penetrating the superconductor, form in type II superconductors when exposed to a magnetic field greater than B_{c1} but lower than B_{c2}. A type I superconductor, such as the aluminum used in this work, can also have vortices form if using very thin films [144]. As just previously mentioned, vortices can also form from strong currents in superconductors falling under a specific range of geometries. Vortex-antivortex pairs can also become unbound (traveling with opposite velocities) from simple thermal excitations [145].

Pinning sites, holes in the superconductor to allow for 'trapping' of the vortices, can be designed around the circuit to prevent any of these scenarios from arising, though ideally one should simply try to prevent any scenarios where vortex generation is likely to occur. The strength of such pinning sites, which can be artificial or 'naturally' occurring defects in the material, is dependent on the frequency of the signal being transmitted through the device [146, 115]. At lower frequencies the vortex will remain trapped to the pinning site but oscillate as a harmonic resonator, though will 'escape' the pinning at a high enough frequency.

A final matter, although there certainly are others not discussed in this report, to keep in mind when designing superconducting circuits is that of current crowding. When current travels through a bend or change in geometry, the current distribution will not be consistent or uniform [142]. This can lead to localized areas where the current density exceeds the critical current density, generating a hotspot and breakdown of the superconductivity. 'Soft' rouded corners should always be favoured when possible, as a hard corner will more likely lead to such issues.

Appendix C

Surface Code

A simplified example of the surface code, as was presented in the author's comprehensive report, is provided below. It is included for the sake of completeness, so the inquisitive reader can find all potentially necessary information in one document, but is not required for understanding the work presented in this thesis.

Figure C.1 shows the layout for a simplified surface code example for two data qubits (a and b) being stabilized by one X-measure qubit and one Z-measure qubit. This circuit should stabilize the two data qubits into the simultaneous eigenstate of $\hat{X}_a\hat{X}_b$ and $\hat{Z}_a\hat{Z}_b$. We will assume the data qubits are in an arbitrary entangled two-qubit state $|\psi_{ab}\rangle$. Step 1 simply initializes the measure qubits into the ground state such that the state of the system is

$$|\psi_1\rangle = |g\rangle \otimes (A\,|gg\rangle + B\,|ge\rangle + C\,|eg\rangle + D\,|ee\rangle) \otimes |g\rangle = A\,|gggg\rangle + B\,|ggeg\rangle + C\,|gegg\rangle + D\,|geeg\rangle \tag{C.1}$$

where A, B, C and D are arbitrary complex values (and for simplicity normalization is ignored). Step 2 applies a Hadamard gate to the X-measure qubit, so that it switches it from the Z basis to the X basis ($|+\rangle$ and $|-\rangle$) putting the circuit in the form

$$|\psi_2\rangle = A\,(|gggg\rangle + |eggg\rangle) + B\,(|ggeg\rangle + |egeg\rangle) + C\,(|gegg\rangle + |eegg\rangle) + D\,(|geeg\rangle + |eeeg\rangle) \tag{C.2}$$

In step 3 a C-NOT is applied between the X-measure qubit (the control) and the a data qubit (the target) gives the state

$$|\psi_3\rangle = A\,(|gggg\rangle + |eegg\rangle) + B\,(|ggeg\rangle + |eeeg\rangle) + C\,(|gegg\rangle + |eggg\rangle) + D\,(|geeg\rangle + |egeg\rangle) \tag{C.3}$$

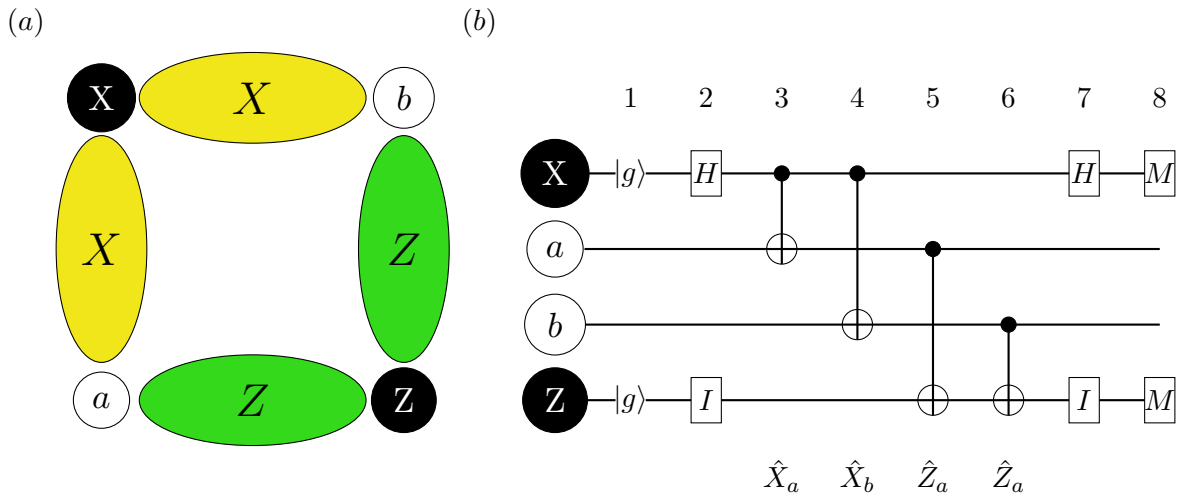

Figure C.1: (a)Four physical qubit surface code example. (b) The quantum circuit shows the process for one cycle of the surface code given the layout seen in (a). The steps indicated on top correspond to that described in the text and the equations in this appendix as listed.

Step 4 applies a C-NOT between the X-Measure qubit and the b data qubit, followed by two C-NOTs (step 5 and 6) which are applied between the a data qubit and the Z-measure qubit and the b data qubit and the Z-measure qubit

$$|\psi_4\rangle = A\left(|gggg\rangle + |eeeg\rangle\right) + B\left(|ggeg\rangle + |eegg\rangle\right) + C\left(|gegg\rangle + |egeg\rangle\right) + D\left(|geeg\rangle + |eggg\rangle\right) \quad \text{(C.4)}$$

$$|\psi_5\rangle = A\left(|gggg\rangle + |eeee\rangle\right) + B\left(|ggeg\rangle + |eege\rangle\right) + C\left(|gege\rangle + |egeg\rangle\right) + D\left(|geee\rangle + |eggg\rangle\right) \quad \text{(C.5)}$$

$$|\psi_6\rangle = A\left(|gggg\rangle + |eeeg\rangle\right) + B\left(|ggee\rangle + |eege\rangle\right) + C\left(|gege\rangle + |egee\rangle\right) + D\left(|geeg\rangle + |eggg\rangle\right) \quad \text{(C.6)}$$

The X-measure qubit undergoes another Hadamard in step 7 giving the final state (before measurement)

$$\begin{aligned}|\psi_7\rangle = {} & A\left(|gggg\rangle + |eggg\rangle + |geeg\rangle - |eeeg\rangle\right) + B\left(|ggee\rangle + |egee\rangle + |gege\rangle - |eege\rangle\right) \\ & + C\left(|gege\rangle + |eege\rangle + |ggee\rangle - |egee\rangle\right) + D\left(|geeg\rangle + |eeeg\rangle + |gggg\rangle - |eggg\rangle\right) \quad \text{(C.7)}\end{aligned}$$

Table C.1: The four measurement results and the resulting Bell state the data qubits have been projected into.

M_X, M_Z	$\|\psi_{ab}\rangle$
+1,+1	$\|gg\rangle + \|ee\rangle$
-1,+1	$\|gg\rangle - \|ee\rangle$
+1,-1	$\|ge\rangle + \|eg\rangle$
-1,-1	$\|ge\rangle - \|eg\rangle$

which if we collect like data qubit states

$$\begin{aligned} |\psi_7\rangle = &(A+D)\,|g\rangle \otimes (|gg\rangle + |ee\rangle) \otimes |g\rangle \\ &+ (A-D)\,|e\rangle \otimes (|gg\rangle - |ee\rangle) \otimes |g\rangle \\ &+ (B+C)\,|g\rangle \otimes (|ge\rangle + |eg\rangle) \otimes |e\rangle \\ &+ (B-C)\,|e\rangle \otimes (|ge\rangle - |eg\rangle) \otimes |e\rangle \end{aligned} \tag{C.8}$$

For step 8 $\hat{Z}$ measurements are performed on the Z-measure and X-measure qubits ($|g\rangle \to +1$ and $|e\rangle \to -1$) where the four possible results from the measurement gives which of the four Bell states the data qubits have been projected into based off of the probabilities determined from Eq. C.8, seen in Table C.1. Further another run of the cycle will give the exact same result, showing this quantum circuit acts as a stabilizer. That the measurement result will be the same after each cycle unless a change to a data qubit occurs is what allows for the error detection ability while not disturbing the state of the data. As an example, given a measurement result of -1,+1, the data qubits are in the state $|gg\rangle - |ee\rangle$ which is the input state $A = 1$, $B = C = 0$ and $D = -1$. From Eq. C.8 we can see from these values of the input state the resulting measurement will again be -1,+1.

It can be rather cumbersome to analyze the surface code using state notation, as can be seen from the expansive formulas for just 4 physical qubits from above, so a more compact form using stabilizer notation is beneficial. The same cycle example as walked through previously is given

Table C.2: The surface code cycle for four physical qubits presented in stabilizer notation.

Step	X Stabilizer	Z Stabilizer
2	$\hat{X}_X\hat{I}_a\hat{I}_b\hat{I}_Z$	$\hat{I}_X\hat{I}_a\hat{I}_b\hat{Z}_Z$
3	$\hat{X}_X\hat{X}_a\hat{I}_b\hat{I}_Z$	$\hat{I}_X\hat{I}_a\hat{I}_b\hat{Z}_Z$
4	$\hat{X}_X\hat{X}_a\hat{X}_b\hat{I}_Z$	$\hat{I}_X\hat{I}_a\hat{I}_b\hat{Z}_Z$
5	$\hat{X}_X\hat{X}_a\hat{X}_b\hat{X}_Z$	$\hat{I}_X\hat{Z}_a\hat{I}_b\hat{Z}_Z$
6	$\hat{X}_X\hat{X}_a\hat{X}_b\hat{I}_Z$	$\hat{I}_X\hat{Z}_a\hat{Z}_b\hat{Z}_Z$
7/8	$\hat{X}_a\hat{X}_b$	$\hat{Z}_a\hat{Z}_b$

in Table C.2 but using the stabilizer notation. This also makes it easier to see why the order of the C-NOTs is significant as otherwise the stabilizers no longer commute with the single qubit measurements $\hat{X}_X$ and $\hat{Z}_Z$ and final measurements would give random results.

The surface code locks the quantum system into a particular state, but degrees of freedom can be achieved by limiting the number of stabilizer measurements. The basic 2-D planar array has two degrees of freedom more than it does constraints from stabilizer measurements, due to the boundaries at the edges of the array. It is possible to apply an operator to these degrees of freedom though a chain of operators being applied to neighbouring physical data qubits provided said chain of operators commutes with the necessary stabilizer.

Appendix D

Dilution Fridge and Measurement Systems

A collection of the various electronics used in the presented and planned experiments of this thesis, as was presented in the author's comprehensive report, is presented below. It is included for the sake of completeness, so the inquisitive reader can find all potentially necessary information in one document, but is not required for understanding the work presented in this thesis.

Numerous pieces of electronics are required for any experiments with superconducting resonators or qubits, ranging from microwave signal generation to simple DC biasing. A collection of the relevant components are compiled below for reference.

- Internal Electronics (inside the Fridge)
  - SMA Feedthroughs: Huber and Suhner Type 34_SMA-50-0-3/111_N (hermetic) and Type 34_SMA-50-0-1/111_N (regular feedthrough). The hermetic seal feedthrough are only used on the top of the fridge, placed in custom machined KF-40 and ISO-63 blinds. Regular feedthroughs are used on every stage inside the fridge and for some transition points outside of the fridge.
  - RF Attenuators: XMA Cryogenic attenuators (eg. 2082-6418-30-CRYO). A selection of different attenuation values from this series of cryogenic attenuators was purchased. Necessary for giving thermal anchoring of the center conductive line of the coaxial cable (as is thermally isolated by the dielectric in the cable) in addition to simply attenuating any input signals from the high power (high SNR) down to the power level required at the device. Being at cryogenic temperatures greatly reduces their noise temperature such that it has very little impact on the SNR of the signal.
  - Circulator: Raditek Cryogenic Circulator (RADC-4-8-Cryo-0.02-4K-S23-1WR-MS-b). These are required to prevent any reflected signal from the amplifier traveling back to the devices undergoing tests. The circulators contain a (relatively) strong magnetic field necessary for

their non-reciprocality and so require magnetic shielding and to not be placed any where near a superconducting qubit.

  - Amplifier: Low Noise Factory LNF-LNC4_8C (4-8 GHz, 39dB gain) and LNF-LNC1_12A (1-12 GHz, 39dB gain). The two amplifiers can be interchanged depending on the experiment being run. The 4-8 GHz being better suited for qubit experiments (having a noise temperature of only 2K) where the 1-12 GHz is better for resonator measurements (having a noise temperature of 4 to 6 K) given the larger bandwidth. The low noise is necessary to avoid washing out the readout signal as it is on the order of -110 dBm or lower.
  - Switch: Radiall 6-way cold SMA switch (R573423605). A switch is used (at the MXC stage) to provide a means to measure multiple devices, yet only have one measurement output line (meaning only one amplifier and chain of circulators). Output choice is controlled by a digital input line which controls inductively powered actuators. A resting period after any change of output selection is required to insure thermal equilibrium is reached.
  - Filters: RLC Electronics (low and bandpass) and Marki (low pass). A selection of various cutoff frequencies and bandwidth filters used at different stages depending on the characteristics of the signal.

- External Electronics (outside the Fridge)
  - Amplifier: Miteq AMF-6F-04000800-15-25P / 4-8 GHz or AMF-4D-02001200-33-20P / 2-12 GHz Amplifier. High gain and low noise amplifiers for qubit readout and low power resonator measurements.
  - Filters: See Internal Electronics.

- Resonator Measurements
  - Vector Network Analyzer (VNA): Keysight N5242A 10 MHz to 26.5 GHz PNA-X. Allows S-parameter measurements, by which the quality factor of the resonators can be determined, as discussed in Sec. 2.2. Can be upgraded to allow for X-parameter measurements (nonlinear/large signal equivalent of S-parameters).

- IV Characterization
  - Source/Measure Unit (SMU): Keysight B2911A SMU. For determining the contact resistance of three-dimensional wires or IV characteristics of fabricated Josephson junctions. Has a minimum source/measurement resolution of 10 fA and 100 nV.

- Qubit Experiments
  - Isolate Voltage Source: Stanford Research Systems SIM 928. For providing a stable low noise constant bias for the Z-line.
  - Arbitrary Waveform Generator (AWG): Tabor WX2184-C 2.3GS/S Four-Channel Arbitrary Waveform Generator with 16M. Used to generator the envelopes of the X/Y gates, and the fast control of the Z-line. It is also used for generating the measurement pulse, though a lower sample rate AWG would suffice as measurement times are greater than 100ns.
  - Local Oscillator: Keysight PSG 10 MHz - 20 GHz E8257D-521 and Phase Matrix 10 GHz FSW-0010. The PSG is used as the local oscillator for qubit gate operations (X/Y line) with the Phase Matrix being used for the qubit dispersive measurement (red line in Fig. D.1).

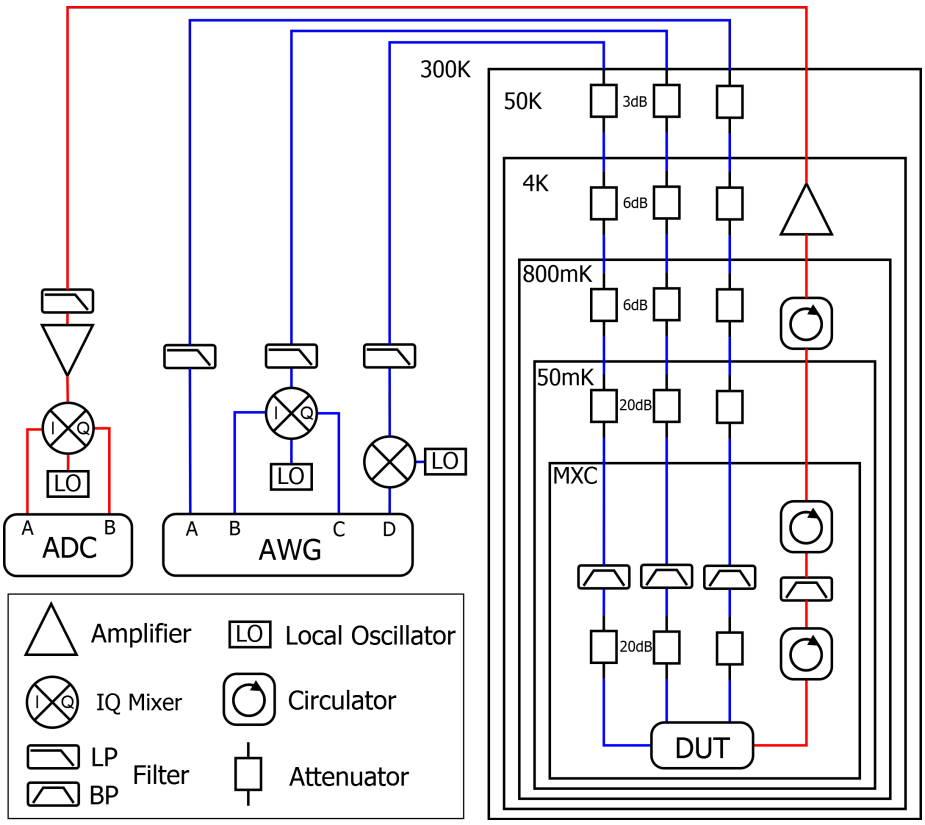

Figure D.1: A simplified electronics setup for a standard qubit experiment. Input lines (blue) are composed of the Z bias line (AWG-A), X/Y gates (AWG-B and C) and the measurement pulse (AWG-D). AWG-A can often also include a DC component for providing a constant bias to the DUT. The output line (red) uses the same LO used for the measurement pulse to down convert the signal to determine the qubit state. Each component is described in this section.

- Spectrum Analyzer: Keysight N9000A CXA 9 kHz - 26.5 GHz. To measure any generated signals (primarily but not exclusively from the AWG) to insure the desired spectrum is present without any desirable sidebands.
- Oscilloscope: Keysight DSO91204A Infiniium Oscilloscope - 12 GHz 40 GSa/s 4 Ch. To measure any generated signals (primarily but not exclusively from the AWG) to insure the desired pulse shaping is present with no unexpected spurs or anomalies. Given the similarity to single qubit gate pulses and digital data signals, eye patterns can also be used to analyze gate pulse performance.
- Digitizer: Ultraview PCI-Express AD12-2000, 2000 MS/sec 12-bit ADC. Digitizes the measurement signal after having been down converted (heterodyne) from the IQ mixer. Digital signal is then analyzed following standard 2^m-PSK techniques (where m is the number of qubits multiplexed off of the readout).

Resonator measurements are relatively straight forward, using the VNA to measure the S-Parameters of the device being tested. The difficulty lies in that calibration is practically impossible to accomplish. Although steps can be taken to somewhat move the measurement plane

near the device undergoing testing, it can not accurately be placed directly at the device's ports. For the low power quality factor measurements the signal must approach single photon power, which requires a heavy amount of attenuation before the device (also due to thermal grounding requirements) and that attenuation must be done at low temperatures to keep the signal to noise ratio (SNR) high. The readout signal must then be amplified, using amplifiers with very low noise temperatures to keep the high SNR, before being sent to the VNA.

This attenuation and amplification also is necessary for the qubit experiments. These experiments involve the generation of X/Y gates, biasing of the qubit (Z-line) and measurement readout, which involves both the generation of a measurement pulse and analyzing the measurement pulse after passing through the device. The generation of X/Y gates is very similar to digital modulation schemes, relatable to quadrature amplitude modulation (QAM) with a 1024 or 2048 constellation. The difference lies in that the amplitude envelope tends to be a different shape for the inphase and quadrature component depending on the desired gate. The dispersive measurement can be somewhat related to 2^m-phase-shift keying (2^m-PSK, where m is the number of qubits being multiplexed off a single measurement line). The state of the qubit causes a phase shift to the measurement signal, such that the resulting constellation points (after calibration) translate into the state(s) of the qubit(s).