# Growth of Silicon Nanowire Mechanical Oscillators for Force-Detected Magnetic Resonance Measurements

by

Xudong Liu

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# Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

# Abstract

This thesis describes two ways to grow silicon nanowires with the catalyst gold (Au) by Chemical Vapor Deposition (CVD) system. One way to prepare catalyst is drop-casting gold nanoparticles solution, the other is making a gold pattern by electron beam lithography (EBL). The diameters of silicon nanowires can be controlled by size of gold nanoparticles in the solution or the size of gold nano-disks which is achieved by EBL. The position-controlled epitaxial growth of Si nanowires is realized by gold nano-disks pattern through EBL. Our Si nanowires are grown on the n-type Si (111) wafer at the same condition. The length is 12-17 μm for Si nanowires 50-150nm in diameter. The taper of Si nanowires is 1 nm/μm in both ways. We found that the growth rates are depend on the size of Si nanowires in drop-casting method, but independent in EBL method. Our purpose of growing Si nanowires is to use it as a cantilever in magnetic resonance force microscopy (MRFM) due to its high aspect ratio and low mechanical dissipation. Therefore, the Si nanowires is required to be vertical and smooth. A high vertical yield, 80%, is achieved by our growth recipe. With HCl added, the surface of Si nanowire is polished. Moreover, the lowest intrinsic dissipation of our nanowire is $6 \times 10^{-15}\ kg/s$ at room temperature, and our Si nanowires can be used as a force sensor for MRFM.

# Acknowledgement

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I thank all my friends. Their friendship makes my life more colorful and meaningful here. Thank you for being there for me when I need you. It doesn't matter where we are in this world or in our lives, I know you will stand with me. Specially thanks Junan Lin for his support in academic research.

Thanks to my family: my parents and grandparents for supporting me spiritually.

Finally, I would like to thank my fiancée, Siqi Han. 幸得识卿桃花面，自此加国多暖春。

# Dedication

This thesis is dedicated to people I love.

# Table of Contents

# List of Tables

# List of Figures

# Chapter 1 Introduction

One dimensional nanostructures are useful in nanoscale applications, and silicon (Si) nanowires are one of the most common.[1] They are widely used in the solar cells[2], electronic and optical devices[3], transistor devices[4] and memory[5,6]. Recently, researchers paid much more attention to vertical aligned silicon nanowires due to their unique application in vertical field-effect transistors and economical process of fabricating nanowire-based devices,[4,7] where it is important to control the position of silicon nanowires growth precisely.[8]

Silicon nanowires have been studied for over fifty years.[9] The first publication about silicon nanowires is Orientation Habits of Metal Whiskers by Treuting and Arnold.[10] In the 1960s, the famous vapor liquid solid (VLS) mechanism was proposed by Wagner and Ellis.[11] VLS is the most common way to fabricate Si nanowires now. Starting in the mid-1990s, the number of papers about nanowires increased rapidly with fundamental aspects of VLS having been studied over 30 years.[12] The chart below shows the number of publications about silicon whisker and nanowire as a function of time.[9]

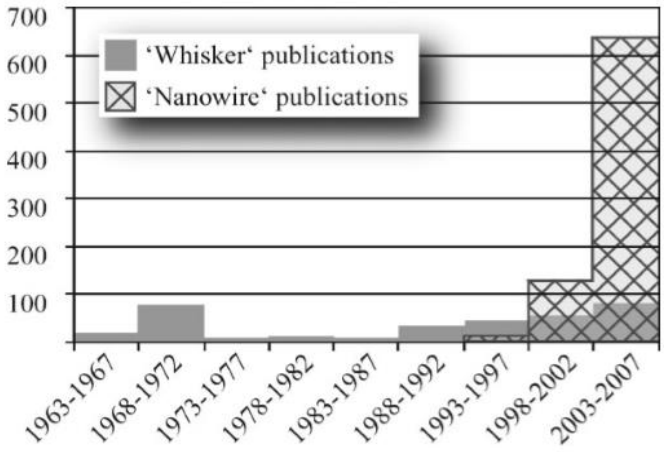


*Figure 1 The number of publication about silicon whisker and Nanowire. Source: ISI Web of Knowledge (SM); search date October 9th 2008*[9]

In our group's project, High-Resolution Nanoscale Solid-State Nuclear Magnetic Resonance Spectroscopy[13], the silicon nanowires are used as a probe which is part of force detection system for

magnetic resonance force microscopy (MRFM).[14] For example, the force on a single proton in a magnetic field of gradient of $10^7$ T/m is in the range of $10^{-19}$ N, which is even smaller than the forces probed in atomic force microscopy (AFM).[15] For such a small force, a sensitive detection system is necessary. Additionally, signal to noise ratio needs to be relative high. The concept of signal to noise ratio, which is the ratio of the magnetic force power on the cantilever and the force noise power of the cantilever, is[16]

$$SNR = \frac{N(\mu_N G)^2}{S_F B} \propto \frac{G^2}{S_F} \tag{1.1}$$

$$S_F = 4k_B T\Gamma \propto 4k_B T\Gamma_0 \tag{1.2}$$

For these parameters, G is the magnetic field gradient at the position of sample, and $S_F$ is the force noise spectral density. G is determined by the magnetic field system, and $S_F$ is proportional to temperature and $\Gamma_0$, which is the intrinsic cantilever dissipation.[16] Other parameters can be found in Appendix. For a cylindrical cantilever with length L and radius R, the intrinsic cantilever dissipation is[17]

$$\Gamma_0 = \frac{k}{\omega_c Q} \propto \frac{R^3}{LQ} \tag{1.3}$$

Where k is spring constant, $\omega_c$ is resonance frequency of the probe, Q is quality factor. To decrease the intrinsic dissipation, the cantilever is needed to be thin and long. The chart below is a summary for the intrinsic dissipation of different material potential probes used in the MRFM, which are published recently.

*Table 1- 1 The mechanical characteristics for potential probes in the MRFM*

| Material | Length | Width | Thickness | Base diameter | Tip diameter | $\omega_c/2\pi$ (kHz) | k (μN/m) | Q ($10^3$) | $\Gamma_0$ ($10^{-15}$ $kg/s$) |
|---|---|---|---|---|---|---|---|---|---|
| GaAs/AlGaAs[18] | 24.5 μm | N/A | N/A | 560 nm | 600 nm | 420 | $10^4$ | 50 | 483 |
| el-SCD[19] | 240 μm | 12 μm | 280 nm | N/A | N/A | 13 | 4800 | 380 | 153 |
| Si[19] | 170 μm | 4 μm | 135 nm | N/A | N/A | 5 | 83 | 12 | 220 |
| Si[14] | 17.7 μm | N/A | N/A | 175 nm | 60 nm | 553 | 667 | 7.5 | 26 |
| Si[14] | 12.9 μm | N/A | N/A | 46 nm | 46 nm | 265 | 66 | 4.0 | 10 |
| Si[14] | 14.4 μm | N/A | N/A | 44 nm | 44 nm | 208 | 28 | 4.0 | 5 |
| CNT*[20] | 4 μm | N/A | N/A | 30 nm | 30 nm | 4200 | 7 | 48 | $5.5 \times 10^{-3}$ |

The el-SCD is electronic-grade single crystal diamond, and CNT is carbon nanotube. All the parameters in the table above are measured at room temperature except CNT which is measured at 1.2K. The width and thickness is for rectangular probes. The base and tip diameters are just for cylindrical probes. Most probes in the table are cylindrical probe. According to Table 1-1, the CNT has the lowest intrinsic dissipation. However, the single CNT now is fabricated in the doubly clamped geometry, which cannot be used as a cantilever in most of MRFM.[21] Based on the Nichol's work, silicon nanowires can be used as a probe in the MRFM.[22] According to Table 1-1 the silicon nanowire has the lowest intrinsic dissipation now. Moreover, lessening the size of silicon nanowire is helpful for decreasing the intrinsic dissipation. The diameter needs to be larger than 50 nm since the limitation of the laser system used to detect nanowires' displacement.[14] As a result, silicon nanowires can be used as a cantilever in MRFM to achieve a great signal to noise ratio. [23]

This thesis describes techniques for Si nanowire growth using chemical vapor deposition (CVD) and electron beam lithography (EBL). Chapter 2 is an overview of the concepts relevant to the theory of Si nanowires growth. We review basic ideas of vapor liquid solid (VLS) mechanism and chemical vapor deposition (CVD) technology. Some brief introduction of experimental details, such as catalyst, precursor ($SiH_4$) and adjuvant gas (HCl), is shown.

Chapter 3 is about the experimental steps in the clean room. Description on details of process steps before growth, which is divided into 2 parts, is shown. One is substrate cleaning and the other is catalyst preparation. We use two ways to fabricate catalysts, drop-casting and electron beam lithography (EBL) patterning.

Chapter 4 describes the recipe for silicon nanowires growth. A detailed presentation of our chemical vapor deposition (CVD) system is in given this chapter.

Chapter 5 surveys and analyses our growth results, which are taken by scanning electron microscope (SEM). The length, diameter and growth rate of silicon nanowires are the parameters we study. We compare Si nanowires grown by different methods. The mechanical properties of Si nanowires are

measured. To integrate Si nanowires into MRFM which requires the nanowires to be vertical, the vertical yield is analyzed.

Chapter 6 is the conclusion and future directions for this project.

# Chapter 2 Preliminaries

In this chapter, we start with a basic introduction of Vapor-Liquid-Solid (VLS) Mechanism, which has played a theoretical role in the growth of silicon nanowires. We also show a summary of different growth methods, highlighting Chemical Vapor Deposition (CVD). A discussion of the catalyst is given. Finally, we discuss the details of growing Si nanowires.

## 2.1 Vapor-Liquid-Solid (VLS) Mechanism

In 1964, Wagner and Ellis announced the VLS mechanism,[11] which is the basic and key mechanism for silicon wires growth. [9]The proposal of VLS mechanism is based on two important concepts.[11] One is that an impurity, actually metallic, is the essential element for silicon growth. Another is that there is a small metallic ball, which stays at the tip of the wire during the growth period. [11]

In Wagner and Ellis' experiment, they used a gold (Au) particle as an impurity on a (111) Si wafer. After heating the sample to 950 ℃, the Au particle formed a droplet of Au-Si. Afterwards, a mixture gas of hydrogen ($H_2$) and silicon tetrachloride ($SiCl_4$) were sent into system. As Wager and Ellis said in their paper, "The liquid alloy acts as a preferred sink for arriving Si atoms or, perhaps more likely, as a catalyst for the chemical process involved."[11] Once this condition is satisfied, the growth happens in the (111) direction. The silicon wires growth stops when the growth environment is changed.[9, 11]

In general, the whole process starts with a silicon base with a metallic liquid drop on it. The chamber is filled with gas that contains silicon element, for instance silane ($SiH_4$). When the gas comes in contact with the substrate at liquid-solid interface, silicon atom is extracted and forms a fresh layer of solid silicon. Essentially, the liquid acts as a catalyst for turning vapour into solid. The silane ($SIH_4$) cracks at the vapor liquid interface. Hydrogen ($H_2$) released, Si alloys with the gold. When the gold and silicon alloyed is saturated, silicon precipitates at the liquid solid interface. The silicon grows epitaxially with Si (111) substrate. (As shown in Figure 2.1[9]) This is the reason why it is called Vapor-Liquid-Solid (VLS) Mechanism.

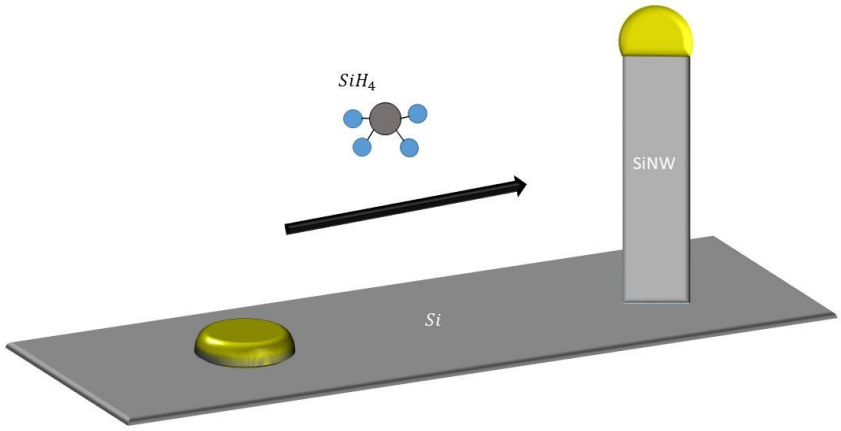


*Figure 2-1 Schematic Diagram of VLS Growth*[9]

## 2.2 Silicon nanowires growth Techniques

Before introducing the details of my project, a brief introduction of the growth methods, Chemical Vapor Deposition (CVD), is given. Actually, there are so many different ways to grow silicon nanowires, including Evaporation of silicon monoxide (SiO)[24], Molecular Beam Epitaxy (MBE)[25,26], top-down Fabrication method[27,28] and so on[9]. Here we only show the details of chemical vapor deposition (CVD) since we only use chemical vapor deposition (CVD) in our project.

### 2.2.1 Chemical Vapor Deposition (CVD) technology

Chemical vapor deposition (CVD) is a widely used chemical technology in many different fields.[29–32] To this materials-processing technology, most of its applications involve in coating a solid film to surface, produce high-quality bulk material and play a key role in some nano-fabrication process. [33] In a couple of sections, I will spend a good amount of time on CVD because I used this tool in the project.

Broadly speaking, chemical vapor deposition (CVD) refers to coating a film or forming a specific structure on a substrate by initiating a chemical reaction, which is induced by a gas precursor.[34] Normally the chemical reactions occur near to substrate's surface, causing the deposition of a particular material.[35] Therefore, it can be distinguished from physical vapor deposition (PVD) where no chemical reactions

occurs during the whole process,[34] for instance, E-beam & resistive heating thermal evaporator, which is also used in this project.

The earliest idea, which is from Wohler, about CVD process was probably in 19 century.[34] However, it did not get deserved concern due to the limitation of technology and relatively poor quality of experimental apparatus. According to the records, the appearing of the first report about deposition of silicon by using CVD is in 1909.[36] The worldwide use of CVD began at the beginning of World War II, because of application of thin silicon films in the electronics industry.[37] In the mid-1970s, with the rapid development of the microelectronics industry, the requirement for Si integrated circuit technology becomes higher and higher.[38] That is the main motivation to develop CVD technology. The modern CVD system came into existence at that time.[33]

Chemical vapor deposition systems are classified by operating pressure into atmospheric pressure CVD (APCVD), low-pressure CVD (LPCVD) and ultrahigh vacuum CVD (UHVCVD).[33] Nowadays, most of active systems use LPCVD or UHVCVD.[34] In terms of reaction mechanism, chemical vapor deposition systems are classified in different ways, but the most common ones are thermal CVD and (Plasma-enhanced CVD) PECVD.[34] As mentioned before, chemical reactions occur during the process. There are some different ways to promote or excite reactions, such as heat (thermal CVD), UV (photo-assisted CVD) or a plasma (Plasma-enhanced CVD).[33]

A series of gas-phase reaction and surface reaction occur in a conventional CVD process.[34] Normally, we use overall reaction to describe the whole entire process, like the chemical equations below.[34]

$$SiH_4(g) \xrightarrow{500-800℃} Si(s) + 2H_2(g) \uparrow$$

$$SiH_4(g) + O_2(g) \xrightarrow{350-475℃} SiO_2(s) + 2H_2(g) \uparrow$$

$$3SiH_4(g) + 4NH_3(g) \xrightarrow{800℃} Si_3H_4(s) + 12H_2(g) \uparrow$$

The first reaction equation is the overall equation of my project, which describes the growth of Silicon nanowires.[39] The second equation is for growth of silicon dioxide ($SiO_2$) thin film.[40] The third one is for silicon nitride ($Si_3N_4$) thin film, which is a common insulating material in the semiconductor industry. [41]

For different CVD systems, the key physicochemical steps are similar:[34]

1. Delivery of precursors into the reactor zone through the gas flow controllable conveyor system.
2. In the reaction zone, the gas phase precursors are transferred to the substrate surface and transform into intermediates and by-products.
3. The target atoms or molecules crowd to growth positions, nucleation and lead to final products, like nanowires or film.
4. Discharge the remaining gas out of the reaction zone.

In CVD system, the growth rate, especially the film growth rate, is mainly determined by the temperature of the substrate, environment pressure in reaction zone and the physical and chemical properties of gaseous reactants and solid reactants.[42]

### 2.2.2 Chemical Vapor Deposition (CVD) Precursors

In chemistry, a precursor is a compound that could produce another substance in a reaction.[43] In the chemical vapor deposition system, the precursor is normally the key reactants in the reaction zone. In this section, a brief introduction of chemical vapor deposition precursors is shown.

#### *2.2.2.1 Precursor Requirements*

Regardless of the type of CVD system, the basic requirements for precursors are generally same. They can be summarised as follows:[34]

- Stable enough during volatilization and transportation
- High enough volatility at the needed evaporation temperature to get the certain growth rate
- Easy to react mildly in the reaction zone
- The decomposition temperature is much higher than room temperature
- No harmful by-product to growth and system
- Long shelf life under standard storage conditions
- High purity and high output ratio

For other CVD systems, such as PECVD or MOCVD, there are some other requirements for precursors. The requirements above are suitable for our thermal LPCVD system where the reaction process could be easily controlled by adjusting ambient temperature and pressure.

#### *2.2.2.2 Precursor Thermal Stability*

Thermal stability of the CVD precursor is a very important factor for a successful CVD process. There are two main terms for thermal stability.[34] Firstly, the precursor should be able to be stored at room temperature for a long time. Moreover, the decomposition of precursor should be well-controlled.[34] For common gas, researchers could just search related paperwork to know how to use it in the CVD system. To make sure the uncommon or new gas is thermal stable enough, users could use Differential Scanning Calorimetry (DSC), which is used to measure the difference in heat flux between the targeted material and a reference material.[44] According to DSC trace, users could draw conclusions about the gas thermal stability.[45] Silane ($SiH_4$) is widely used to grow silicon nanowires and its storage technology is mature now.[9,46]

#### *2.2.2.3 Precursor Purity and purification techniques*

It is universally acknowledged that the purity of the reactants is extremely important in a chemical process.[43] And the same applies to CVD process.[33] The purity of the reactants influences the physical and chemical properties of the final product, such as the thin film and nanowires. Purifying the precursor has played an important role in the semiconductor industry since 1980s.[34] Commonly used purification techniques are sublimation, recrystallization, rectification, preparative chromatography and adduct purification. [34,47] We require the purity of precursor to levels of up to 99.9999%.[48]

## 2.3 Catalyst

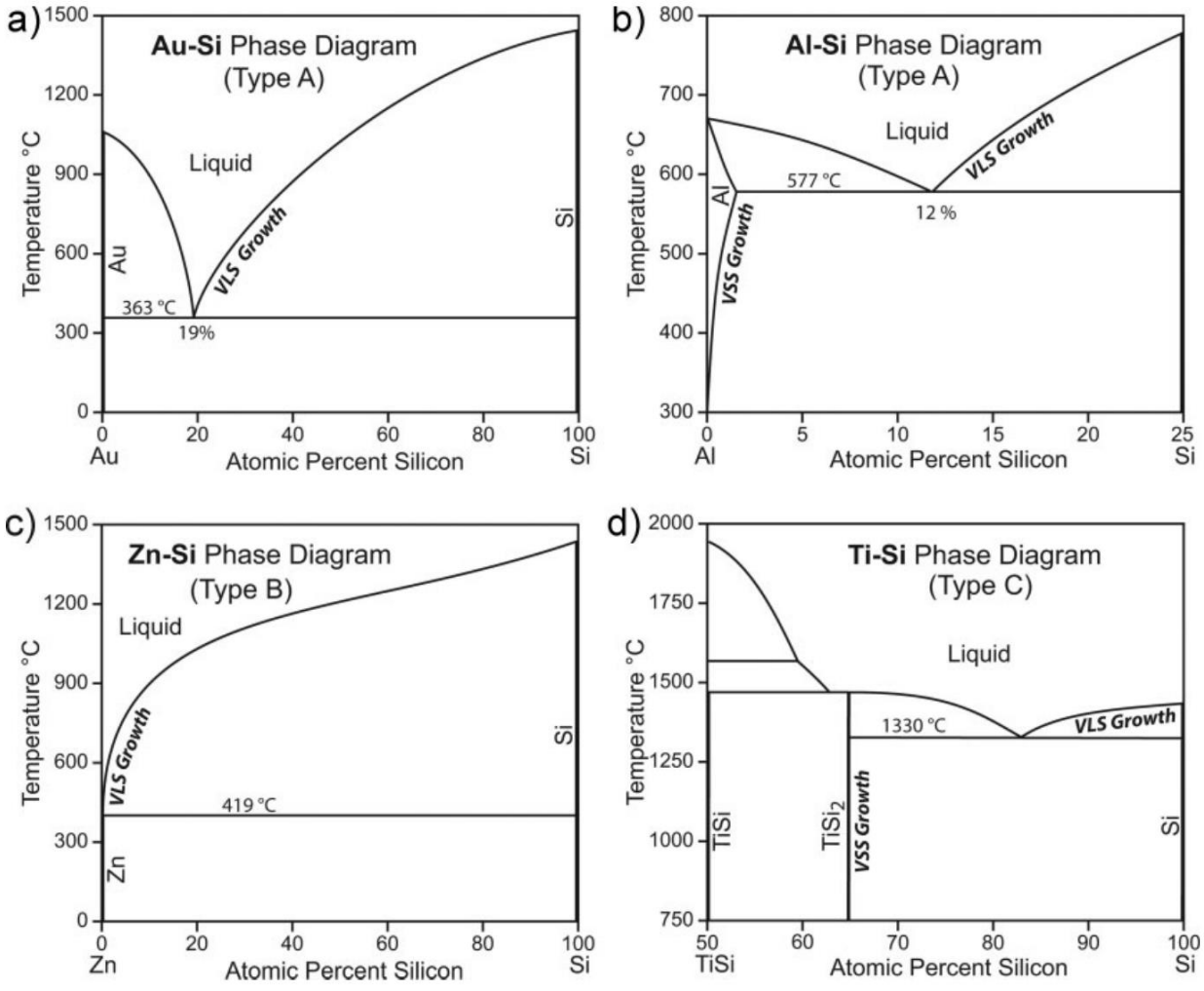


*Figure 2-2 Phase diagrams of various metal-Si : a) Au-Si, b) Al-Si, c) Zn-Si, d) Ti- Si [9]*

There are hundreds of papers which mentioned that gold (Au) could be used as a catalyst in growing Si nanowires. It also could be said that gold is one of the most popular catalyst material in the world.[9] Actually, there are many other different materials which can be catalyst materials, like copper (Cu),[11,49] silver (Ag),[50,51] aluminium (Al), [49,52]iron (Fe),[53] magnesium (Mg)[51] and so on.[9] Based on the characteristics of the corresponding metal-silicon binary phase diagram, people divide these catalyst materials into three types, type A, type B and type C.[54] There is the single eutectic point which is normally greater than 10 at.% in the phase diagram of Type A materials. Gold (Au) is a type A material.

For type B, the eutectic point is smaller than 1 at.%. If there are more than one eutectic points in the phase diagram, we call them type C materials.[9] Actually all the different type materials can be used as catalyst material in the research and industry. For example, with complementary metal–oxide–semiconductor (CMOS) technology, people would use Ti, which is a type C material, as a catalyst to grow Si nanowires.[55,56] To consider the electronic properties of the final silicon products, people sometimes chose type B materials, like Bi, Sn or Tl, to synthesize Si nanowires.[49,57]

### 2.3.1 Gold as Catalyst

To explain the reasons for choosing gold (Au) as a catalyst, I will present some advantages of using gold to grow silicon nanowires firstly. Gold is one of the most available and standard materials in the fabrication center all over the world, especially for evaporation system.[9] Therefore, depositing the gold layer would not involve a new machine or step. Moreover, it is convenient for researchers to use gold (Au) colloid nanoparticle solution, which can be bought from the commercial companies (Ted Pella or BBI solution). The size of nanoparticles is from 5nm to 250 nm, which is expedient for any purpose use. Most importantly, as an inert material, the biggest advantage is its chemical stability.[43] During pre-growth and growth process, the catalyst material might be exposed in oxygen ($O_2$). Meanwhile, the high chemical stability of gold (Au) could reduce the technological requirement of the growth system and process. The use of gold (Au) would not lead to extra safety requirements since the Au is not reactive. For better explanation, the Au-Si binary phase diagram is shown in Figure 2.2 a). As mentioned before, gold (Au) is type A material, which has a eutectic point at about 19 at.% and 363℃. That means the melting point of Au-Si is much lower than the melting point of pure Si (1414℃)[58] or pure Au (1064℃)[59]. Therefore, heating the Si covered by thin Au film at or over the eutectic point, the liquid Au-Si alloy will be formed. The process is along with de-wetting, which means that instead of forming the uniform layer, a small Au-Si droplet is synthesized.

According to the Au-Si binary phase diagram, Figure 2-2 a), the Si is abundant when the formation of Au-Si alloy occurs on the pure Si substrate. When the new Si atoms, like silane ($SiH_4$), are added into the

system constantly, the equilibrium condition of Au and Si in the droplet will be broken, and the system will move into VLS growth part in the Au-Si binary phase diagram. In order to re-establish the equilibrium state of Au-Si, the system needs to go back to liquid section, the redundant Si atoms in the droplet of Au-Si alloy would separate out. It is well known that akin atoms prefer to aggregate. Therefore, the growth occurs at the side of Si substrate, and gold could be a catalyst for Si nanowires growth via this process. [9]

Another advantage of gold is its relatively high silicon concentration at the eutectic point. What is more important is its relatively low requirement of temperature for the eutectic point, 363℃. That means that it costs relatively low energy to dissolve Si in Au-Si alloyed droplet. The energy cost of increasing its concentration to beyond its equilibrium value for Si atoms to should be low. Therefore, we only need a comparably low Si pressure during the growth process. Additionally, gold (Au) has a very low vapor pressure (around $10^{-8}$ mbar below 800℃)[60,61] and high enough surface tension (more details in section 2.4). Despite some possible disadvantages of gold such as its high price and relatively low adhesion to silicon, it is still considered as a good catalyst.

## 2.4 Thermodynamics of VLS Wires growth

To analyse the physics of silicon nanowire growth process, some brief descriptions about surface stress, surface tension and surface free energy are necessary in order to present growth process clearly. These three things often leave people confused since, unlike liquid, they are not necessarily equal for solids. At the beginning of 20 century, Josiah Willard Gibbs firstly made a comment on a concept of line tension $\tau$, just like the concept of surface tension, to depict the force at boundary of different phases.[62] In the normal situation, people do not talk about this tension since its value is in the range of $10^{-11} J\ m^{-1}$to $10^{-9}\ J\ m^{-1}$.[63] Moreover, at the equilibrium conditions, introducing the line tension will lead to an additional term $\tau/r$ where r is the radius of circular boundary line. When the scope of studying is down to a few nanometers or smaller, the term from the line tension could not be safely neglected. Fortunately, the

smallest diameter of Si nanowire in our project is around 40 nm. As a result, the term of the line tension is neglected in the following part. [9]

For surface tension in the solid, it is related to the work of adding atoms to the surface.[64] The surface energy is the one consumed by the destruction of the intermolecular chemical bond when the new surface of the material is created.[65] The surface stress is related to the work of surface elastic deformation.[66] Because the liquid cannot withstand the shear stress, and there is no plastic deformation,[67,68] the surface energy of the liquid is as same in value as the surface tension.[69] But since solids can withstand shear stress from external force effect is increasing in the surface area. Part of the force results plastic deformation, and thus solid surface energy and surface tension are not equal.[69] For silicon surface, the surface stress is represented by a second rank tensor. Fortunately, for an isotropic solid surface, like a silicon (111) substrate, the surface stress tensor becomes a scalar. In the following part, we will just treat it as surface tension.[9]

In our case, there is a droplet of silicon (Si) and gold (Au) on a silicon substrate. In this environment, silane gas ($SiH_4$), as a precursor, provides Si to growing nanowire. During the project, it was found that the base diameter of Si nanowires is large than top. It is necessary to note that this is not another growth of a new Si nanowire, but just the nanowire base diameter being enlarged during the growth. To explain it, we need to start with the contact angle which is defined here the angle in the liquid. Based on Ressel's work in 2003[70], the contact angle of Au-Si alloy droplet on a flat Si surface is $\beta_0 = 43^{\circ}$ at the temperature between 400℃ and 650℃. This data is suitable for us because our growth temperature is 650℃. However, according to the work of Kodambaka in 2006, the contact angle between the Au-Si droplet and the Si nanowire is around 120°.[71] Therefore, the shape of Si-Au droplet suffers from a changing stress during the growth. It is easy to assume that the surface tension of the catalyst droplet is $\sigma_l$, the surface tension of the Si wire is $\sigma_s$ and the surface tension of the liquid-solid interface is $\sigma_{ls}$.[9] When the growth rate of Si nanowire is slow enough, we can model the growth process as quasi-static. That means all tensions are at balance at each moment. At equilibrium, all the tensions follow the Neumann triangle relation.[63,72]

$$\sigma_l \cos(\beta) = \sigma_s \cos(\alpha) - \sigma_{ls} \tag{2.1}$$

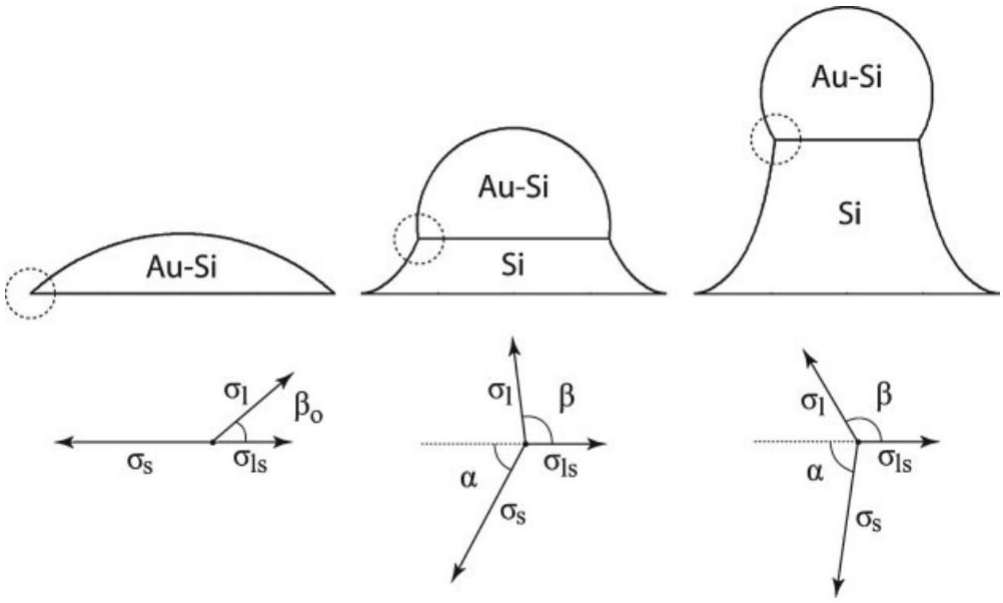


*Figure 2-3 Schematic Development of the Droplet and Wire Shape in the Initial Phase of VLS Wire Growth. The corresponding equilibrium balance of surface force is indicated below. The horizontal force components add up to zero.*[9]

At the beginning of growth process, the contact angle $\alpha$ is zero. In the horizontal plane, the surface force cancels each other and gets zero net force. After starting growth, the $\alpha$ increases as the height of the silicon nanowire increases.

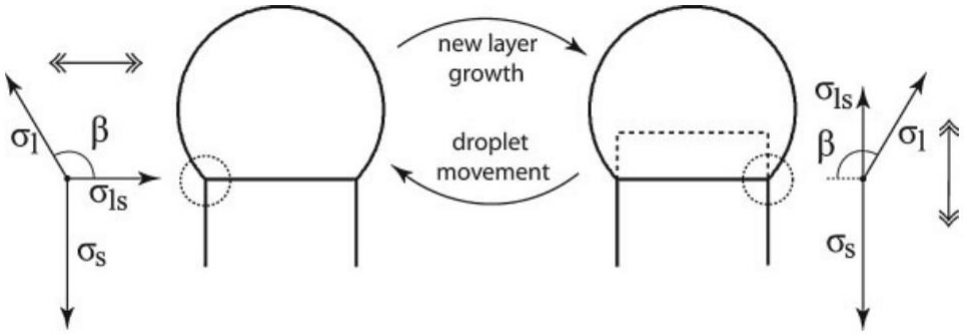


*Figure 2-4 Two Consecutive Growth Steps of Si nanowires. The force balance in horizontal direction has to be taken into account on the left-hand side. The force balance of the vertical force components needs to be considered on the right-hand side.*[9]

For the growth part, we can assume there are two steps like shown in the Figure 2-4. The first one is that a new layer of silicon grows at the interface of Si-Au alloy droplet and the top of Si wire. The second

step is that the droplet moves upward along the edge of new layer of silicon. By repeating these two steps, the Si nanowire grows. For the first step, the appearance of new silicon layer breaks the equilibrium condition. The droplet 'wet' the new Si layer. At that moment, there is only one degree of freedom for Si-Au alloy droplet, namely in the vertical orientation. There must be an upward force to push the droplet to get its initial condition. For the initial growth condition in Figure 2-3, the equilibrium equation is

$$\sigma_l cos\beta = -\sigma_{ls} \tag{2.2}$$

For the first step, the condition equation is

$$\sigma_l sin\beta + \sigma_{ls} > \sigma_s \tag{2.3}$$

Combining these two equations above, we have

$$sin\beta - cos\beta > \frac{\sigma_s}{\sigma_l} \tag{2.4}$$

The maximum of $sin\beta - cos\beta$ is $\sqrt{2}$ when the contact angle $\beta = 135°$. To make sure the condition equation is satisfied during the whole growth process, we have

$$\frac{\sigma_s}{\sigma_l} < \sqrt{2} \rightarrow \sigma_l > \frac{\sigma_s}{\sqrt{2}} \tag{2.5}$$

This is the Nebol'sin stability criterion.[49] For silicon, $\sigma_s = 1.2\ J\ m^{-2}$. Therefore, the threshold for Si nanowire growth is $\sigma_l = 0.85\ J\ m^{-2}$. In the CVD system, the common catalysts are Au and Al. The value of $\sigma_l$ for gold (Au) is about $0.9\ J\ m^{-2}$.[49] For aluminium (Al), the value of $\sigma_l$ is around $0.8\ J\ m^{-2}$.[49,52] Therefore, gold is appropriate as a catalyst in Si nanowires growth, while Al is not.

## 2.5 The effect of HCl in the growth of Si nanowires process

Unlike the use of HCl in the semiconductor industry, which is etching silicon,[73] HCl is mainly used for surface chlorination in growing silicon nanowires.[74,75] HCl does not react with Au, since the Gibbs formation energy of $AuCl_3$ is positive.[75] According to Gentile and Oehler' work, HCl is shown to prevent the gold migration on the silicon surface.[76,77] As a result, HCl could play an important role at the early stage in the growing silicon nanowires. HCl is a suitable associated gas in the nano-fabrication for straight structure. Based on the Gentile's work in 2012, HCl enacts a critical role in the shape control of

doped silicon nanowires.[77] Hydrogen chloride (HCl) decreases the density of metallic impurities on the surface of Si nanowires, which is a major source of defects. A smooth surface can be achieved from a growth recipe with HCl. Figure 2-5 shows a boron-doped Si nanowires grown in two steps.[77] It is grown in a $H_2$ flow of 1 $L\ min^{-1}$, a $SiH_4$ flow of 50 sccm and $P(B_2H_6)/P(SiH_4)$=1 × $10^{-3}$ with $P_{tot} = 3\ Torr$ at 650℃. The first step is growing silicon nanowires with HCl, the second step is growing silicon nanowires without HCl. It can be clearly observed that there are two regions on the silicon nanowire. According to the picture, the surface of silicon nanowire is rougher in the second step's region. Moreover, the diameter slightly increases, and there are gold clusters on the surface in the second region. [77]

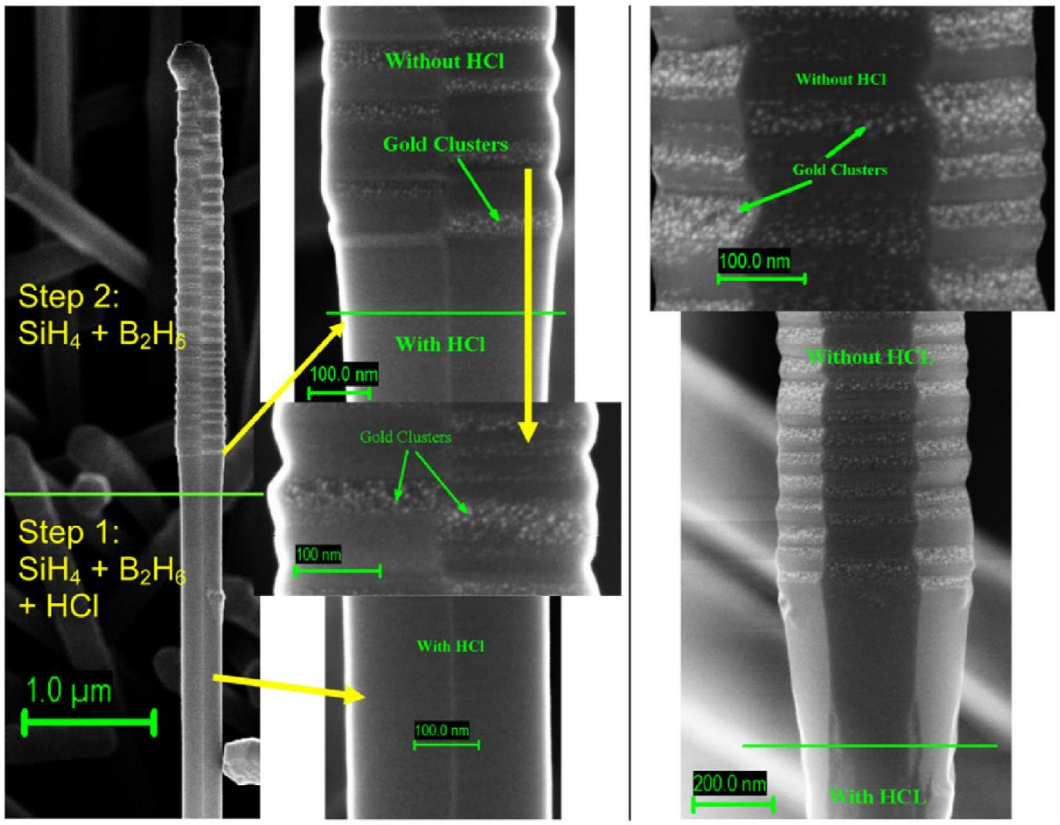


*Figure 2-5 SEM images of boron-doped Silicon nanowires grown in two steps under different condition. Step 1 with HCl and step 2 without HCl. In the zoom of the region grown without HCl, the gold clusters are at the surface with an increase of the diameter and the roughness.*[77]

Oehler found that it was easier to grow thin Si nanowires with HCl.[76] In the presence of HCl, small gold nanoparticles remain roughly in the same position as time passes. As a result, small gold droplets would not aggregate during heating and small silicon nanowires growth. The chart below shows the

diameter distribution of silicon nanowires grown, with or without HCl, at 650℃, 25 sccm $SiH_4$, 100 sccm HCl.[76] The first chart shows the distribution of silicon nanowires larger than 100 nm. The second chart shows the distribution of silicon nanowires smaller than 100 nm, which is obtained from SEM. [76] According to the chart, it is obvious that it is much easier to grow small silicon nanowires with hydrogen chloride (HCl) flow gas, especially for wires smaller than 80 nm. [9,76]

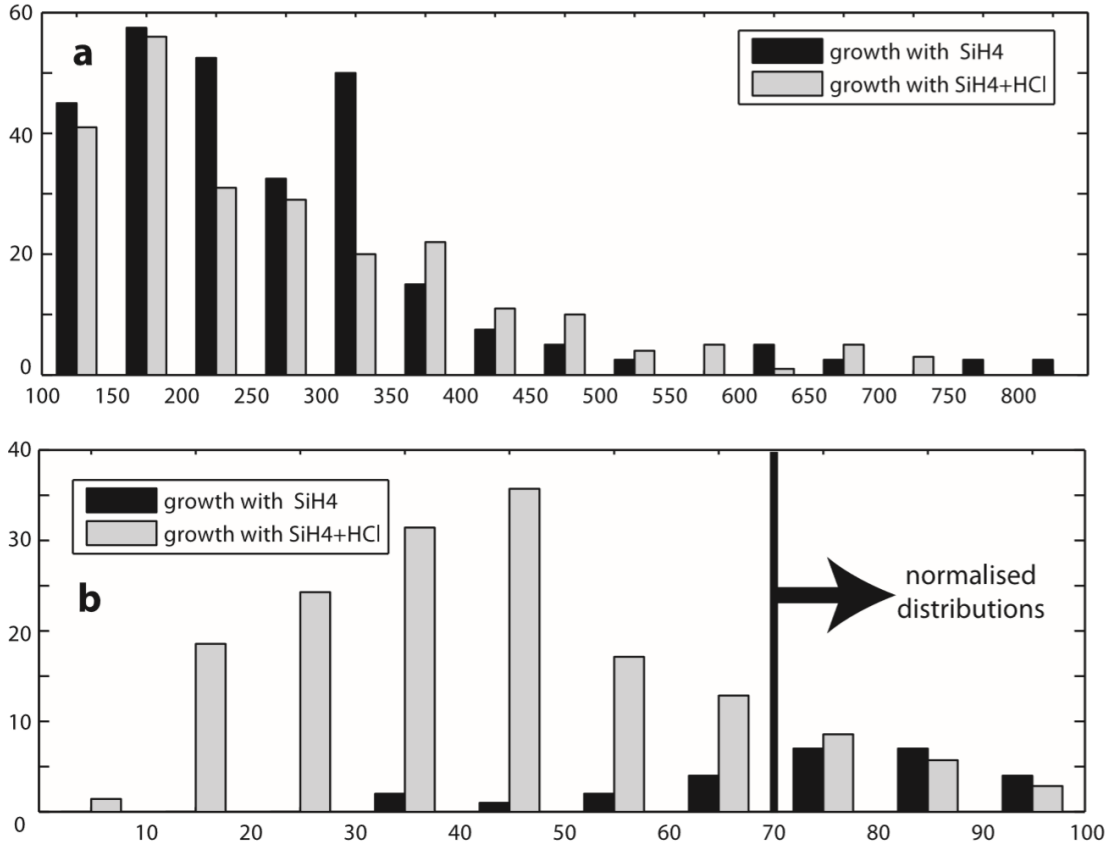


*Figure 2-6 Diameter Distribution of Silicon Nanowires Grown with or Without HCl. (a) the large diameter distribution. (b) shows the small diameter distribution.[76]*

# Chapter 3 Preparation of Substrate and Catalyst in the Cleanroom

## 3.1 Substrate preparation

To grow vertical nanowires on the silicon substrate, the silicon (111) wafers are used most commonly.[78] For silicon (111), Young's modulus, Poisson's ratio, and shear modulus are isotropic, but anisotropic for silicon (100) and (110).[78] Moreover, the bulk shear modulus varies minimally with crystallographic orientation on silicon (111).[78] We generally use 3 inch n-type (111) silicon wafer with native oxide layer, unless stated otherwise.

The 3-inch wafer is cut into smaller pieces for processing using a DISCO DAD3240 dicing saw. Prior to dicing the wafer, it is spin-coated with a protective layer of Shipley S1811 photoresist [see appendix], which is subsequently removed by sonicating the sample in acetone. Since the growth of silicon nanowires will be negatively impacted by substrate contamination, it is necessary to perform a standard RCA clean on the silicon substrate chips before proceeding with the application of the gold catalyst. The RCA clean consists of immersing the chips sequentially into two heated solutions; SC-1 to remove organic residues and SC-2 to remove metal ions [see appendix].

## 3.2 Catalyst Preparation

There are two different ways to prepare the catalyst. One is treating gold (Au) nano-particles solution to catalysts, growing the silicon nanowires in CVD system. Another is making patterns by using EBL and growing silicon nanowires. The second one is to grow vertically location-controlled Si nanowires.
The silicon nanowires are grown on the N-type Si (111) substrate.

### 3.2.1 Drop-cast

The simplest way of applying gold catalyst to the silicon substrate chips is by drop-casting with colloidal dispersions of gold nanoparticles[9]. This results in a random distribution of spherical catalyst particles across the entire substrate surface.

*3.2.1.1 Colloidal solutions of gold nanoparticles*

Gold is a metal that has been used for over a thousand years. As a material it is very stable, generally non-reactive and has good electrical properties. Recently, colloidal suspensions of gold nanoparticles have found numerous applications in electronics, nanotechnology and material science. [79,80]

Colloidal gold is available commercially in a range of diameters. The colloidal gold suspensions used in this project were purchased from Ted Pella and had particle diameters of 50 nm, 100 nm and 150 nm.

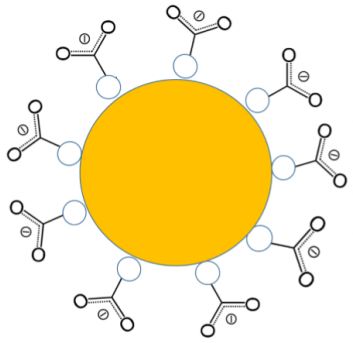

*Figure 3- 1 The Structure of Gold (Au) Nanoparticle in the Solution*[81]

Based on the manual of the gold nanoparticle solution, the Au nanoparticle in the solution is surrounded by some carboxyl ions, −COO−, just as shown in the figure. The negative ions here are to keep particles at arm's length from each other. The 50nm, 100 nm and 150 nm nanoparticle solutions were bought from Ted Pella. In the clean room, 500 µL of 1M HF was added to a plastic beaker which contains 250 $\mu L$ of the Au nanoparticles solution and 11750$\mu L$ deionized water (DI water). All the glass container, vials, pipette tips and Millipore water should be cleaned to eliminate any possible pollution on the Au nanoparticles and Si substrate. The 100 nm Au nanoparticles are separated enough to assemble a larger Au nanoparticle group by $H^+$.

*3.2.1.2 Drop-casting process*

After RCA clean, all preparations for drop-casting are done. To protect laboratory technician, personal protective equipment (PPE) should be worn all the time during whole process, since this step involves HF which is an extremely dangerous acid solution. No stainless steel tools are allowed in this process. A long plastic tweezer is recommended. In order to control precisely the concentration of Au nanoparticles, the micropipettes should be used. On account of the micropipettes and tips being for the public, no green nitrile gloves should be worn when users use micropipettes. The recipes of Au nanoparticle solution are shown in appendix. Before immersing the gold nanoparticles solution, a native silicon oxide ($SiO_2$) layer should be removed. In order to etch silicon oxide layer, the RCA cleaned chips should be left in the 1M HF solution over 10 min. Take the sample out of the 1M HF solution, dripping off any excess HF solution, then fully immerse the substrate into the Au Colloid mixture for 10 seconds. Move the drop-cast sample into the DI water bath in beaker and leave for at least 30 seconds. Afterwards, dry the chip slowly and gently by using the nitrogen gas gun. Because the silicon oxide layer grows very quickly in the air environment, the drop-casted chips should be stored in the vacuum bag as soon as possible. The whole process is shown in the diagram below.

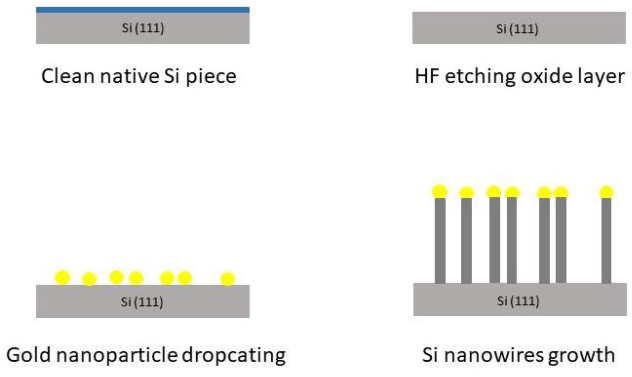


*Figure 3- 2 Illustration of the growth process on Si (111) by drop-casting*

### 3.2.2 Lift-off Process for Patterning of Evaporated Catalyst Array

For experimental applications, it can be advantageous to grow silicon nanowires in ordered arrays. This requires that the gold catalyst is patterned onto the silicon substrate chips, which can be done using an electron beam lithography lift-off process.

#### *3.2.2.1 Lithography*

Since Feynman's presentation "There is plenty of room at the bottom" at California Institute of Technology in 1959, nanotechnology gradually becomes a new field of science.[82] On account of the theoretical limitation of photolithography, which has pushed the production line into the 32nm era, [65] a new non-optical lithographic techniques should be considered. The new technique is also very important for integrated circuits (IC), biosensors, microelectromechanical systems (MEMS) and so on. Nowadays, there are many different ways to do patterning in microfabrication. Photolithography and electron beam lithography (EBL) are the most common tools.[83] Photolithography, also called UV lithography, is developed in the 1960s. However, according to physical reason showed below, it is difficult to reach the resolution in the range of nanometers. Electron beam lithography (EBL) is one method which can surpass the photolithography.[84] Without using a mask, electron beam lithography write a designed pattern on the sample directly. It can reach a resolution of sub 10 nm, higher than any other tools.[85] It is based on an electron beam source which is same with the basis of Scanning Electron Microscopy (SEM).[86] Electron beam lithography is popular due to its high resolution, relative low cost and high reliability for writing complicated structures on a large area. [84,87]

Associated with de Broglie wavelength relationship,

$$\lambda = \frac{h}{p} \tag{3.1}$$

For an electron with 1 eV, the wavelength is

$$\lambda = \frac{h}{p} = \frac{h}{\sqrt{2mK}} = \frac{6.626 \times 10^{-34} Js}{\sqrt{2(9.11 \times 10^{-31} kg)(1.0 eV)(1.60 \times 10^{-31} J\ eV^{-1})}} = 1.23 nm \tag{3.2}$$

Similarly we can get the wavelength of a photon with 1 eV

$$\lambda = \frac{h}{p} = \frac{hc}{pc} = \frac{1239.84eV}{1.0\ eV} = 1240nm \tag{3.3}$$

The photon beam is a thousand times larger than the electron beam. This is the key reason why EBL has a much better resolution than photolithography.

#### *3.2.2.2 Electron Beam Lithography (EBL)*

The core component of the EBL system is the electron-optical control system, which can generate a highly concentrated electron beam.[87] The EBL system is based on SEM, complemented by a variety of hardware and software.[86,87] Figure 3-3 is a schematic view of the Electron Beam Lithography (EBL) system.[88] It follows that a complete electron beam lithography is extremely complicated, and it would require a separate paper to explain the whole system clearly. Therefore, I will just show some details about electron beam source and beam shapes which are related to the final resolution and e-beam resists.[86] We use Raith $150^{Two}$ Direct Write EBL system in the Quantum Nanofab Facility in University of Waterloo in our project. This device uses ZEISS Gemini electron column with variable accelerating voltage up to 30 kV. The available apertures of Raith $150^{Two}$ are 7.5$\mu m$, 10$\mu m$, 20$\mu m$, 30$\mu m$, 60$\mu m$ and 120$\mu m$. Raith $150^{TM}$ can carry samples from 5mm to 7 inch wafers. [89]

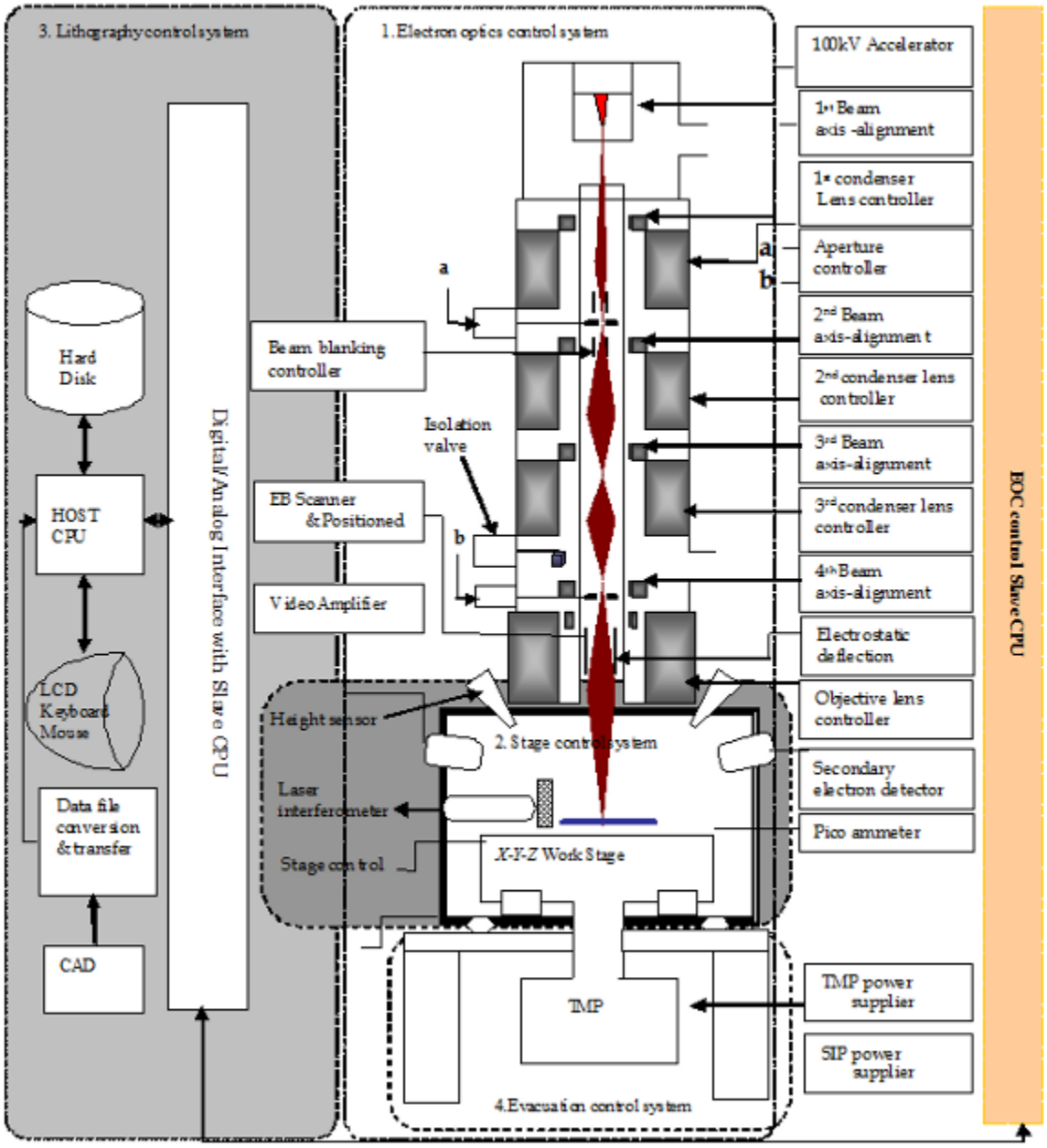


*Figure 3- 3 Diagram of components of electron beam lithography (EBL)*[88]

In principle, an electron gun constitutes a cathode and a lens.[90] The cathode is for emitting electrons, and the lenses, which are called cathode lensed, are used for focusing the electrons from the cathode into a beam. The Figure 3-4 shows the structure of electron beam source. According to the type of emission, we can classify electron gun into three types: thermionic emission,[91] field emission[92] and thermal field emission (TFE), which is also called Schottky field emission.[93] For thermionic emitter, electrons are

extracted by heating. Due to no heating, the field emitter is called cold type gun as well.[94] Electrons escape from gun tip because of high electric field ($10^8\ V/cm$) and high voltage in field emission gun.[95] The last one, thermal field emission cathode, is a bit like the combination of thermionic emission and field emission. In the Schottky field emitter, the electrical field provide additional energy to reduce the energy barrier of source, the thermionic cathode would emit electrons when it is in working condition. Its advantages are that it has high current density and stability, low sensitivity to external influence, relative long cathode life (around 2000 hours) and no requirement for cathode regeneration.[96] The Raith 150 TWO system uses thermal field emitter which is made up of ZrO/W.[89]

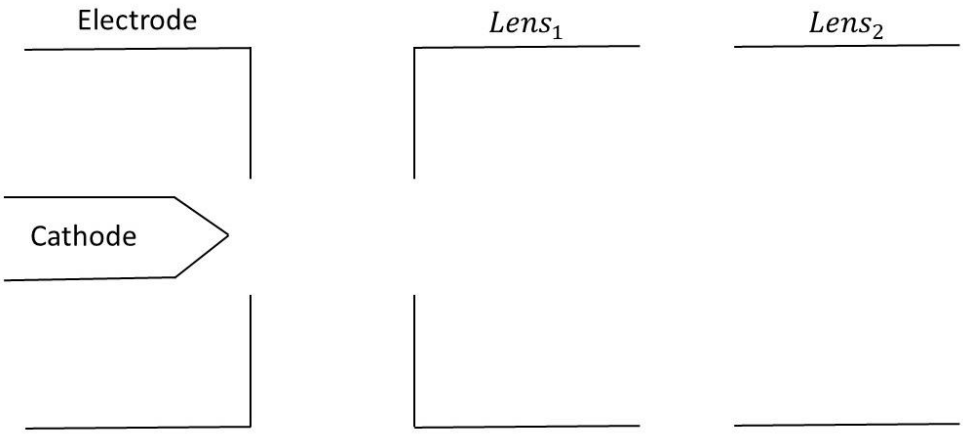


*Figure 3- 4 Schematic diagram of electron beam source*

For different requirement of resolutions, there are two types of beam shapes in the EBL system.[84] Gaussian beam is usually used in process which have a high requirement of resolution, since it converges on a spot as small as possible. However, the working speed of this beam shape is slow because of the small pixel size (around 10 nm). Shaped beam is faster, because there are various apertures in one rectangular electron beam and the pixel area is larger (around 100nm). However, it cannot reach a resolution as high as a Gaussian beam.[97] In our project, we use a Gaussian beam.

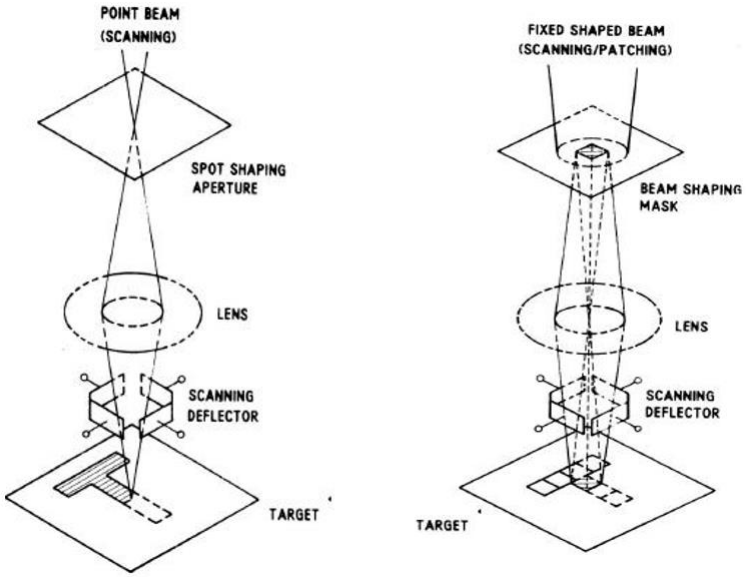


*Figure 3- 5 Schematic diagram of (a) Gaussian beam and (b) shaped beam.*[98]

In order to reach a high enough resolution, many parameters should be considered during the design step and process. Besides the choice of e-beam resists, the electron exposure dose is an important parameter. To each different e-beam resist, different EBL system and different thickness of e-beam lithography layer, the suitable value of dose, with unit $\mu C/cm^2$, is different.[99].

### *3.2.2.3 E-beam Resist*

To get a high resolution in the EBL system, a suitable E-beam is critical. Over past decades, many different E-beam resists have been developed. Based on their chemical composition, people divided them into two groups, organic and inorganic resists. The organic resists are mainly made up of carbohydrates and polymeric materials. The most popular organic resists are Poky methyl methacrylate (PMMA), ZEP, polystyrene (PS) and poly l-butane sulfone (PBS). Inorganic resists have a weak atomic absorption in the EUV region,[100] for example Hydrogen silsesquioxane (HSQ), Lithium fluoride (LiF) and Aluminium fluoride ($AlF_3$) and so on. [101,102]

*Table 3- 1 Common EBL resists with their properties and uses*[102]

| Resist | Type | Developer | Characteristics |
|---|---|---|---|
| PMMA (high molecular weight) | Positive/Organic | MIBK:IPA 1:3 or Cellosolve Methanol 3:7 | High resolution, single layer or top of Hi/Lo bilayer, liftoff |
| PMMA (low molecular weight) | Positive/Organic | MIBK:IPA 1:3 or Cellosolve Methanol 3:7 | High resolution, single layer or bottom of Hi/Lo bilayer, liftoff |
| Copolymer (MMA) | Positive/Organic | Same as above | Large undercut profile for liftoff when used as bottom layer with PMMA on top |
| ZEP 520 | Positive/Organic | Hexyl Acetate, n-Amyl Acetate or Xylenes | High resolution, good etch resistance |
| ZEP 7000 | Positive/Organic | 3-Pentanone Diethyl Malonate | Fast, good for making masks |
| HSQ | Negative/Inorganic | 0.26N TMAH | High resolution, good etch resistance |

In term of the types of the reaction between the electron beam and resists, they can be divided into positive resists and negative resists. After exposing by an electron beam, the exposed positive resists are dissolved in developer, but the negative one remains on the substrate. As shown in the figure below. Based on our design, a positive resist is used in our project.

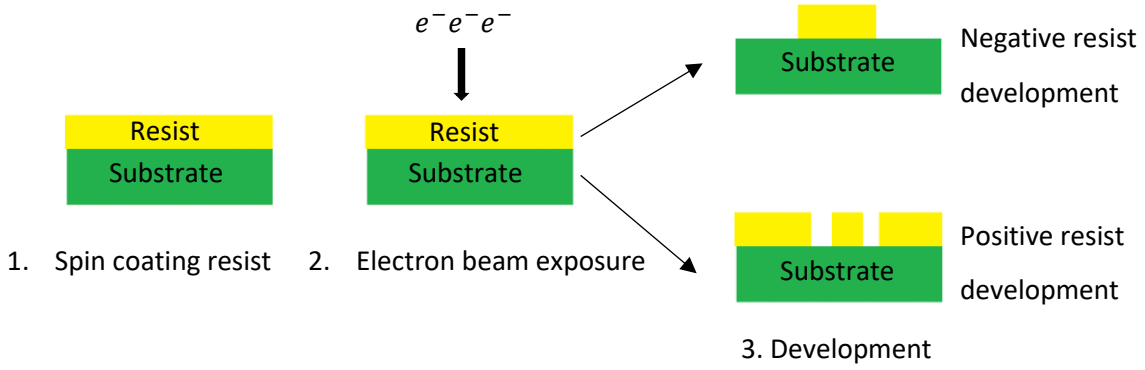


*Figure 3-6 Scheme of Positive Resist Development and Negative Resist Development*

The resists normally have two functions. One is to protect the covered substrate from etching or pollution. The other is to transfer the designed pattern on the target substrate. [103]

PMMA is the first resist for e-beam lithography and one of the most popular e-beam resists now.[104] To estimate the different e-beam, the resist's contrast, γ, is a good reference parameter. This parameter is related to the highest dose, $D_1$, where resist remain and the lowest does, $D_2$, where resist is etched totally. It is defined by [105]

$$\gamma = \frac{1}{\log_{10}(\frac{D_2}{D_1})} \tag{3.4}$$

The higher the contrast is, the clearer the difference can be observed.[101,106] Most resists in the world now have contrast range from 2 to 10.[102] Another important parameter is the sensitivity of resist, which shows the response of resist to e-beam exposure.[107] If the resist was extremely sensitive, a small change in electron beam would cause a huge variation in final product.[108] The thickness of resist is based on the design of final products. Moreover, for a certain thickness of e-beam resist and pattern, the electron exposure dose test needs to be done. PMMA has the contrast range from 6 to 9 and an acceptable sensitivity which make sure a resolution for electron beam lithography.[104] According to Cord's work in 2009, a 10 nm line width can be achieved by using PMMA as an electron beam resist.[85] We use PMMA as our electron beam resist.

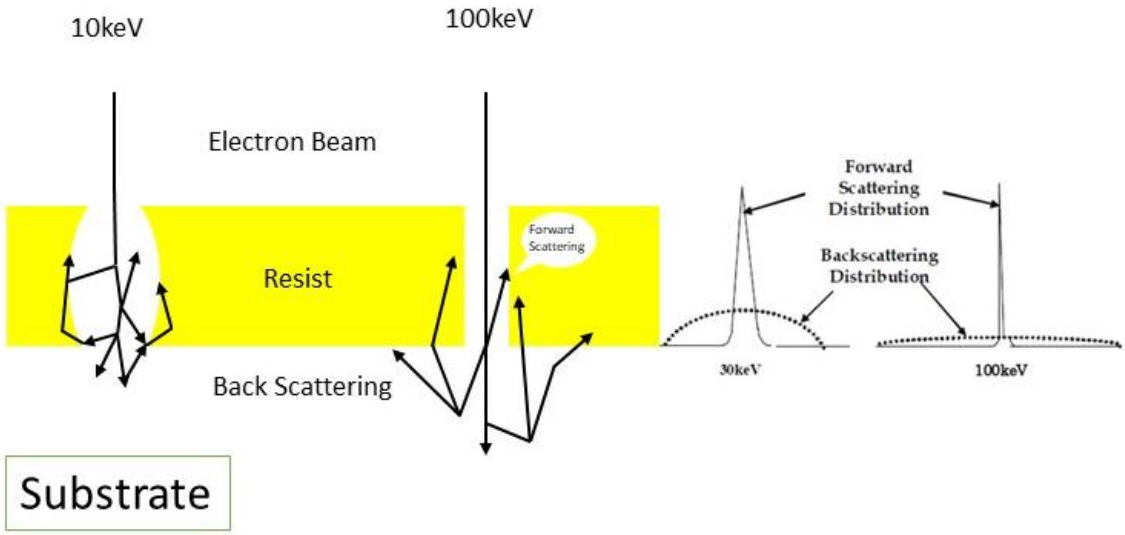


*Figure 3- 7 Diagram of electron beam behavior at 10 kV and 30 kV in resist[88]*

When the prepared sample exposes in the electron beam system, the electron beam enters the resist and interacts with the particles and electrons. These interactions lead into the elastic and inelastic collisions among beam, resist and substrates.[102] Some elastic collisions with a small angle result in the increase of the size of trace in the resist. Other electrons are inelastic scattering which cause backscattering. Most of electron in the beam are absorbed in the substrate. Others, from 10% to 40%, are backscattered. As a result, there is an additional exposure in the resist relative to primary beam exposure, which is named electron beam lithography proximity effect. [85,109]

To reduce the proximity effect, there are two common ways.[109] One is doing the dose correction or improving the design. According to the figure above, minimizing the energy of electron beam is away to make the dose correction. Another way involves specific system like bilayer resist and so on.[88,109]

*3.2.2.4 E-beam lithography lift off*

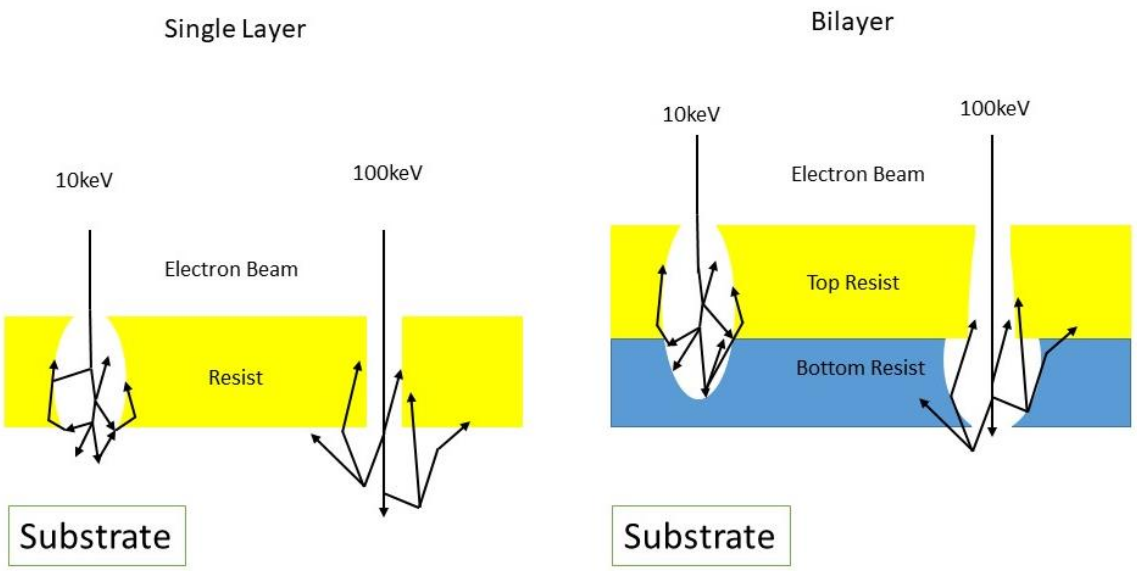


*Figure 3-8 the different electron beam behaviors on single layer and bilayer*

Besides exposure in the EBL and develop step, the lift-off is also a critical step for the final structure. The lift off step consists of removing the sacrificial layer and the corresponding target material. The target

structure is left on the surface of the substrate. The target material here is the gold, which have a weak adhesion with silica and silicon substrates even using adhesion promoting processes. Another way to enhance gold adhesion to deposit the titanium (Ti) and gold (Au) together. However, only the gold here is used to be the catalyst. Therefore, titanium should not be involved in our project. The bilayer resist system is used common for its better lift-off characteristics. Using the MMA as the bottom layer and PMMA as a top layer are the common way. Same as the figure above, the bottom layer is more sensitive to the electron beam. The trace is wider than the one on the top resist (like PMMA). After the deposition of target material (Au), immerse the sample in the lift-off solution. The wider trace is helpful to dissolve the resist faster.[110–112]

### 3.2.3 Electronic Beam Evaporation system

The PVD E-beam and resistive heating thermal evaporator is already a mature commercial fabrication tool. The PVD E-beam thermal evaporator is ion source assisted e-beam and thermal evaporation in ultra-high vacuum. Unlike chemical vapor deposition system mentioned before, the whole process occurring in the system is all physical, no chemical reactions happens. To get target material vapor gas, the target material is heated by using an electron beam. The chamber of e-beam evaporator is filled with target material gas, and the atoms will deposit on the relative 'cool' substrate mounted on stage. The PVD thermal evaporator used in the Quantum Nano-fab Facility in the University of Waterloo is the Intlvac Nanochrome II UHV system (Intlvac, Ontario, Canada). It could reach to $10^{-7}$Torr range after 8 hours pumping down. The available materials in this machine are Silver (Ag), Aluminium (Al), Aluminum oxide ($Al_2O_3$), Gold (Au), Chromium (Cr), Copper (Cu), Nickel (Ni), Palladium (Pd), Platinum (Pt), Titanium (Ti), Silicon monoxide (SiO) and Germanium (Ge). We will use this PVD system to do the gold deposition. The deposition rate is 0.5 $Å/s$, which is the standard deposition rate for gold in this system, and the final thickness of gold layer is 5nm. There is no adhesion layer, like Titanium (Ti), since gold should be on the silicon directly. [113,114]

### 3.2.4 Growing Silicon Nanowires with Electron Beam Lithography (EBL)

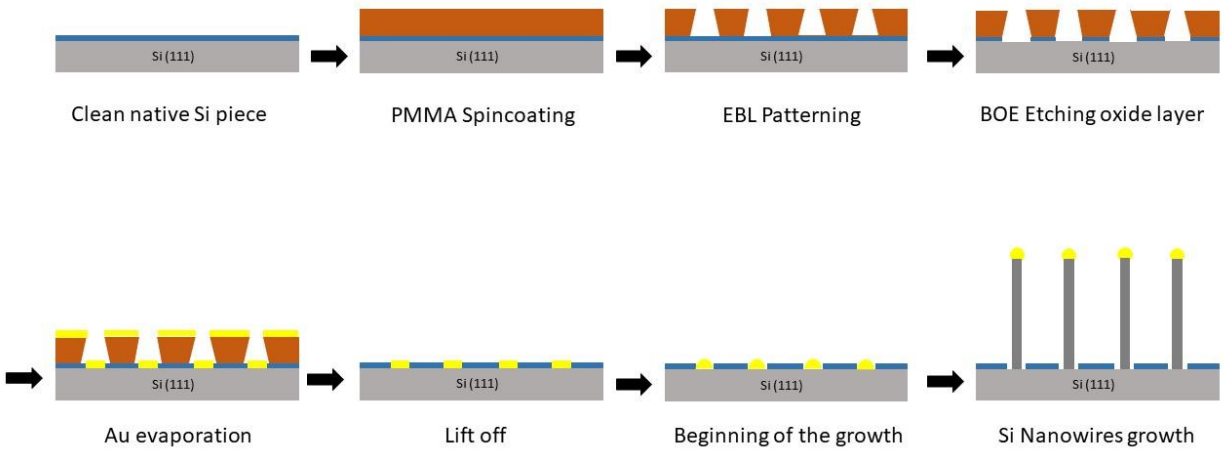


*Figure 3- 9 Illustration of the growth process on Si (111) by EBL*

Preparation part in this method is similar with drop-casting. By using dicing saw, the 3-inch n-type native wafer is cut into 8mm by 8mm chips. Because our target is to get an array of silicon nanowires near the edge, a pre-cut on back side is also necessary here. After the RCA clean, the PMMA (A3), which is a very popular e-beam resist for high resolution, is coated on chips. In the project, both of single layer and bilayer are used. The thickness of PMMA is around 120nm for single layer and bilayer, as measured by a Dektak profilometer. The thickness is determined by the later step, at least five times the thickness of Au layer. That is very important for lift-off step, otherwise a quality lift-off cannot be achieved. A common way in Au deposition for bilayer is MMA (bottom layer) and PMMA (top layer). [See appendix]

Next, the prepared sample is loaded into the EBL system to write designed pattern, as shown in the Figure 3-10, at an acceleration voltage of 10 kV. Only dose and line elements are used during EBL process. The area doses is $200\mu C/cm^2$. The whole pattern consists arrays of holes with different diameters, 100 nm, 200 nm and 250 nm. The spacing between holes is at least $8\mu m$ to ensure no apparent influence among nanowires during the growing process in the CVD. The whole pattern is divided into three zones, holes in each zone have same diameter.

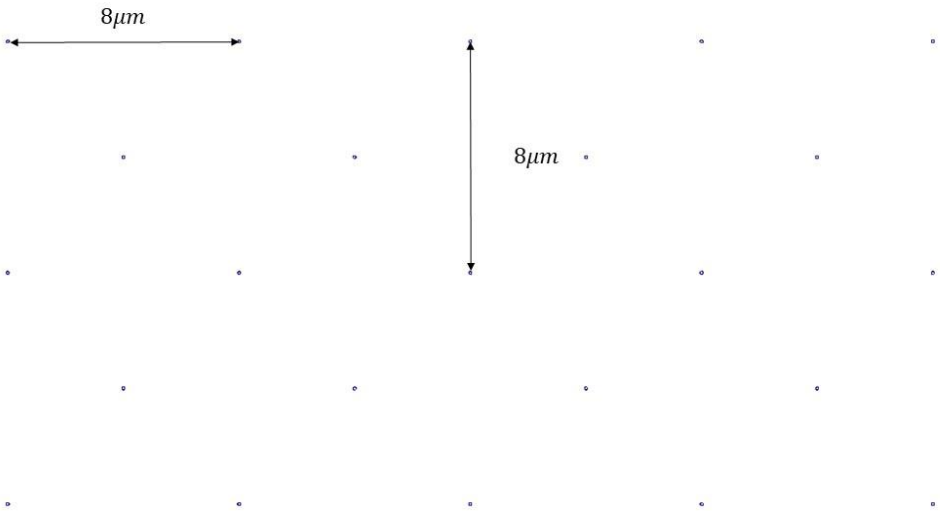


*Figure 3- 10 the EBL pattern design. The diameter of holes is 50nm, 100nm and 120nm. For each pattern, the holes are same with a constant periodic spacing,* 8 $\mu m$.

After the exposures, the sample was developed in methyl isobutyl ketone (MBIK): IPA (1:3) for 60 seconds at room temperature. Then immerse samples in IPA solution, which is a standard stopper for MBIK: IPA (1:3), for 60 seconds at room temperature to stop developing. Dry the chip with nitrogen gun as usual.

Before depositing gold layers on the sample, the silicon oxide layer should be removed first. It is easy to etch silicon oxide for native wafer since it is very thin. Buffered oxide etch (BOE), which is also known as buffered HF, is the one we used in this step. It is supplied in the clean room. Leave samples in the BOE solution for 15 seconds to etch silicon oxide. Longer time will lead to over-etching, which means the size of silicon circle would be larger than the size of pattern size. (Shown in figure 3-11) If the size of silicon circle is much larger than designed, multiple growths from one source would occur during CVD growth. In other words, the silicon oxide layer could hold the size and shape of gold disk. After etching step, the gold deposition step should be started immediately, at most in 20 minutes.

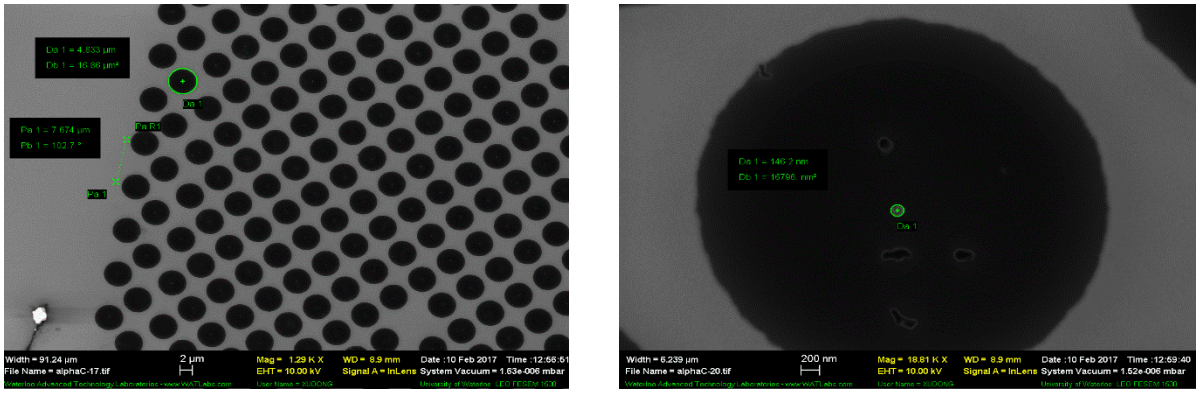

*Figure 3- 11 SEM images of over-etching at BOE step*

By using PVD in clean room in the University of Waterloo, a 5nm gold layer is deposited on the silicon chip. The deposition step is processing under $10^{-6}\ Torr$ at room temperature. The deposition rate is 0.5Å$/s$ (the slowest deposit rate for Au), and whole process is done automatically by PVD system.

Next, the sample was immersed in PG Remover, which is designed for removal of PMMA resist on Si or $SiO_2$ , for 2 days at room temperature. Alternatively, it can be removed by using PMMA at higher temperature (~80℃ ) for 90 minutes. However, we cannot promise gold deposited disk to be stable position at the situation. When the chip is taken from PG remover, the chip should be rinsed slowly by IPA, and then gently dried by nitrogen gun. The prepared samples is stored in vacuum bag to reduce contamination.

During the experiment, we found that it took around two days to remove 100 nm single layer of PMMA with 5 nm gold layers in the PG remover at room temperature. We even did not get a successful lift-off by using the acetone after two days. The acetone is abandoned because of its high volatility. Since the adhesion between gold and silicon is not strong, no heating and stirring during the lift-off to avoid any loss of gold. To save time, a bilayer, a common way to accelerate lift off, is attempted. The bottom layer is 120 nm MMA, and the top layer is 100 nm PMMA.

*Table 3- 2 The duration of lift-off with single layer and bilayer*

| | Single layer | Bilayer |
|---|---|---|
| Acetone | >2 Days | 2 Days |
| PG Remover | 2 Days | 1.5 Days |

According to the table above, the bilayer here is not as effective as we expected in our project. As a result, single layer is used continuously.

# Chapter 4 Growth in Chemical Vapor Deposition (CVD) System

## 4.1 Chemical vapor deposition system

For a commercial chemical vapor deposition system, it normally contains gas source & control section, reaction zone, temperature controller section, vacuum system and software system.[35] The gas source & control section includes gas sources, gas transport system and mass flow controller (MFC).[33] For reaction zone, the main parts are the load-lock chamber and the reaction tube. The temperature controller is not a relative separate section. In fact, it is attached to another hardware system, including thermal sensors and furnace temperature controller.[34] The CVD system contains pressure sensors, mechanical pumps, ionic pumps and isolation valves.[33]

## 4.2 Important Elements in CVD system

The whole CVD system is very complicated and intricate.[34] In a particular CVD process, engineers consider all different aspects, including reactant supply, substrate handing, reaction chamber, exhaust, monitoring and safety, heating and energy, abatement systems and so on.[33] The first important thing for a CVD system is the quality of products. Moreover, one of the best ways to get a good quality product is to use high purity reactant supply and make sure no contamination in the CVD system. As mentioned before, researchers should use the at least 99.9999% purity supply gas.[34] Most of the source of contamination are vapor and solid dust particle. Contamination in vapor is mainly due to outgassing and line supply leak.[34]

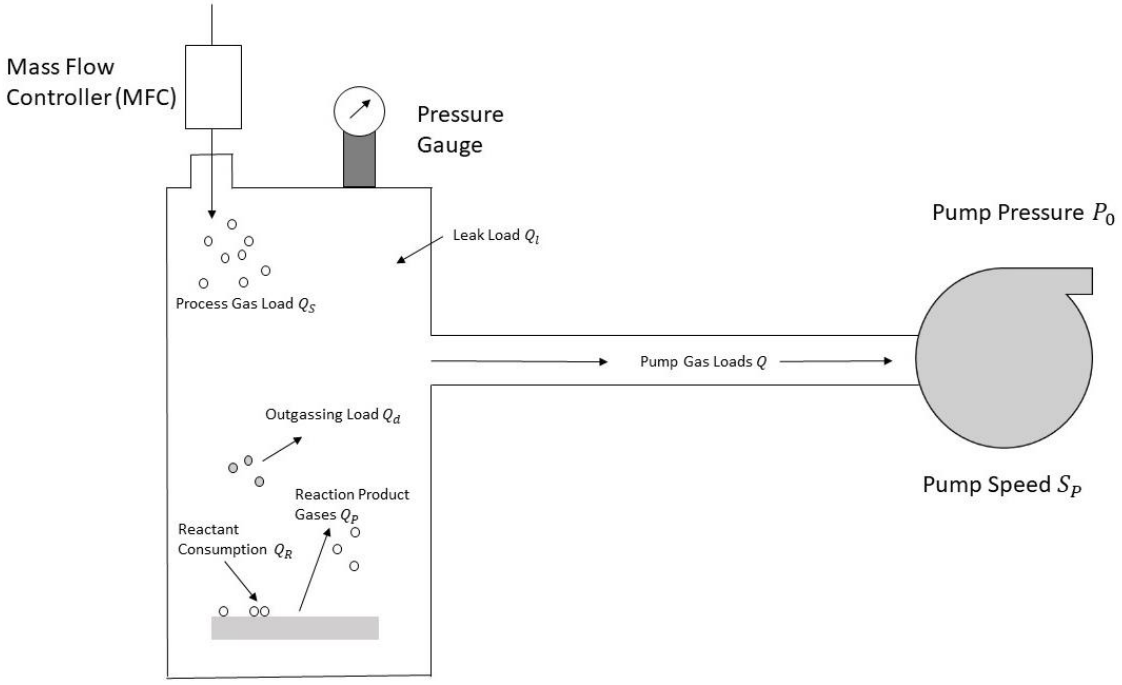


*Figure 4- 1 the schematic diagram of gas load of CVD system[34]*

It is a universal truth that vacuum technology and pump are the key elements for all types of CVD.[33–35] The Figure 4-1 shows the gas load of CVD system, we can know the sum of process gas supply $Q_s$, outgassing load $Q_d$, reaction product gasses $Q_p$ and leak load $Q_l$ should be equal to pump gas load Q, reactant consumption $Q_R$.[34]

$$Input + leaks + outgassing + generation = output + consumption$$

Normally, we will neglect the leaks, outgassing and consumption part. [34]

$$Q_s + Q_p = Q(= S_p P_0) \tag{4.1}$$

Although the CVD is a very complicated system, there is normally only one feedback, namely pressure measurement, for each part of system. Unfortunately, there is no one vacuum pressure gauges that can be used in whole pressure range. There are three kinds of pressure gauges, including mechanical gauges, gas property gauges and ionization gauges. The mechanical gauges cannot measure accurately below $10^{-5}$ Torr, but it has the advantage of being not sensitive to temperature. That means it is used for atmospheric environment and low vacuum. The gas property gauges are related to bulk properties, like

thermal conductivity. It can measure the range of $10^{-5}$ Torr to 10 Torr. The ionization gauges are used in high vacuum and UHV ranges. [33–35] Pirani gauges, which are suitable for measuring pressures between 0.5 Torr to $10^{-4}$ Torr, are used in our CVD system.

Another important device in the CVD system is the mass flow controller (MFC), which is used to measure and control the flow of reactants and precursors in the CVD system. The reason to say its importance is users could control the growth rate by controlling the flow of gases through mass flow controller (MFC). [35]

The next part is the heating strategies and thermal measurement device. With modern technology, heating should not be a difficult part, for example passing electronic current in a common conductor like Cu can product heat.[34] However, it is one of the most burdensome part in design since it is always related to the flow dynamics. Consequently, users always do some test process to decide the heating rate.[33–35] To do a well control of heating, a suitable thermocouple should be chosen. For special requirement, researcher would like to use the infrared non-contact optical pyrometer as the temperature measurement device to avoid touching the substrate. [34] In our project, we use a standard K-type thermal couple.

For control process, researchers control the CVD process in terms of reactor pressure, gas throughput and temperature. Suitable pumps and pressure gauges help users to control pressure. By using MFC, users adjust the gas flow of reactants. To control the temperature in the reaction zone, a suitable furnace is critical. [33–35]

The key part of the CVD cabinets is CVD reactor. In traditional, there are two different types of thermal reactors, hot-wall reactors and cold-wall reactors, in the industry. Over 40 years, the horizontal hot-wall tube reactor has been an industry standard, especially for low-pressure operation.[33–35] In order to reach no radial pressure gradient in flow, the tube should have a symmetric geometry. Therefore, the device could reach the requirement of uniformity.[34] Besides keeping the tube clean enough to get a high-quality produce, the thermal uniformity should also be considered.[34] To prevent the thermal gradient at the center part, the tri-zone furnace is equipped in our CVD system.

## 4.3 Gas dynamics and flow basics

All actions in the reaction zone are at the level of molecular. Unlike "macro-fabrication" process, it is difficult to control each molecule to do the deposition directly for us. The molecule behaviors are driven by the thermodynamics of the precursors, the chemical properties of precursors, the dynamics of heat and mass transport, the physics of surface adsorption and crystal growth. To repeatedly produce wires or films with high quality uniform, researchers need to consider all sections above seriously. In this section, some flow dynamics fundamentals will be shown to help understand the way to control the gas supply pressure.[34]

Before showing the details and functions, a new concept needs to be introduced, the Knudsen number, Kn, which is the ratio of the mean free path and the diameter of a tube.[34,115]

$$Kn = \frac{\lambda}{D} \tag{4.2}$$

The $\lambda$, is the mean free path, which is the average travel distance for a molecule, normally for gas molecules, between two collisions with others. This parameter is widely used in statistical mechanics and gas dynamics. D is the diameter of our tube in the CVD system, whose complete definition is the reactor dimension perpendicular to the flow direction. For better understanding, we use air as an example here. According to others' work, the mean free path of air at room temperature and atmosphere is $6.6 \times 10^{-3} m$.[116] Moreover, if the mean velocity of the molecule is $\bar{v}$, the average number of collisions is $\bar{Z}$ per unit time, then the mean free path is given by[115,117,118]

$$\lambda = \frac{\bar{v}t}{\bar{Z}t} \tag{4.3}$$

According to experiments and previous studies, for one kind of gas, we have

$$\bar{Z} = n\sigma v_{real} \tag{4.4}$$

where $\sigma$ is the effective cross-sectional area and $v_{\mathrm{real}}$ is real velocity. [117,118]

$$v_{real} = \sqrt{2}\bar{v} \tag{4.4}$$

Therefore,

$$\lambda = \frac{1}{\sqrt{2}n\sigma} \tag{4.4}$$

Base on the ideal gas equation of state, $PV = nRT$,

$$\lambda \propto \frac{T}{P} \tag{4.5}$$

where p is pressure and T is temperature.[117]

Therefore, when the pressure below $10^{-3}$ Pa, the mean free path of air molecules is larger than the diameter of most of tubes. That means that at room temperature and atmosphere, a carrier gas should be used in the CVD process, since the gas precursor is trapped in the transport lines. The molecules would be moving over one km per second. For some special growth process, like 3D structures in IC design, if the mean free path is large than the internal feature, the device would not get uniformly coated. Unfortunately, for this important parameter, we cannot control it directly. Controlling the pressure looks like the easiest way to change this parameter.

Someone might say that controlling the temperature of the gas is also a way to change the mean free path of precursors. However, it is almost impossible to control the temperature of fluent gases precisely in practice. At very low temperature, the temperature probe (thermocouple) cannot get to thermal equilibrium with environment gas. It actually reaches a thermal equilibrium with the wall of chamber and supply lines. What's more, the molecule flow is much more dependent on pressure than temperature. [34]

Back to the Knudsen number, it is a factor to show the mass transport characteristics of the reactor and exhaust system.[115] For one certain CVD system, the diameter of the tube is a constant. The value of Knudsen number is determined by the mean free path of precursors. Therefore, the Knudsen number is related to pressure. As shown in the figure below. According to the value of Knudsen number, people named three different states of gas at room temperature. For Kn < 0.01, the gas flow is called viscous flow, where the collisions between molecules dominate. For 0.01 < Kn < 1.0, people call it transition flow, where there are less intermolecular collisions than viscous flows. When Kn >1.0, the collisions between molecules are rare, and it is molecule flow.[34] For one turn CVD process, the precursor may be

under different conditions in different component since the pressures are different for each portion. As is known to all, the gas will flow from high pressure to lower. In the CVD system, we need the higher pressure source at the entrance of reactor zone, tube, and escaping from the reactor outlet by using the pumps. When Kn is larger than 1.0, the precursor molecules are most likely hitting the substrate directly, since they are in the molecule flow regime. This type of CVD saves much energy and get a relatively higher growth rate. [33–35,115]

## 4.4 Our CVD system

The software we use is $CVDWinPrC^{TM}$ process control software suite which is built on a National Instruments LabWindows TM software platform. Users could control the gas flow, pressure and temperature precisely by programming or setting parameters directly. This software suit contains four programs, CVD process Control, CVD data Viewer, CVD recipe Editor and CVD-config-Editor. All process date is saved by this software, and it could create real-time images for one or more variables. [119]

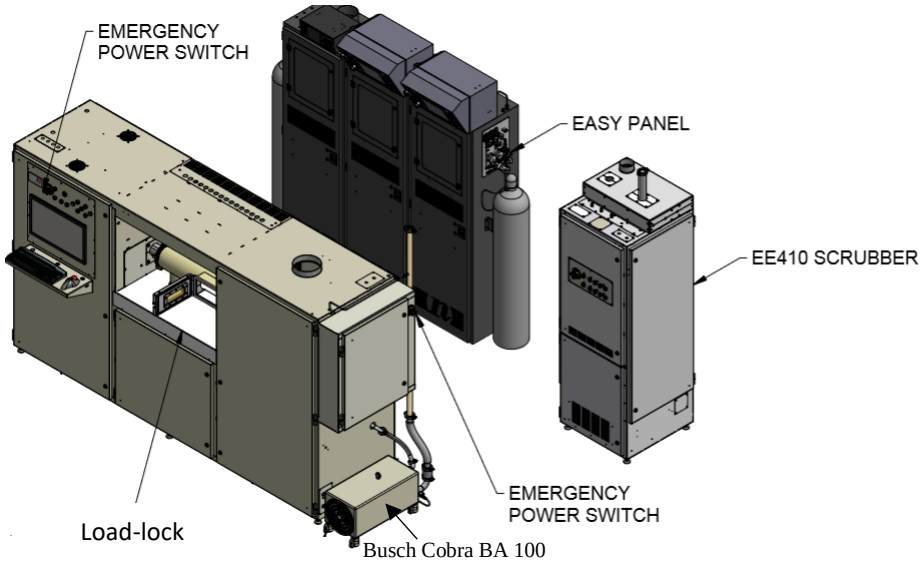


*Figure 4- 2 Diagram of our group's CVD system [119]*

*Figure 4- 3 Picture of CVD system in RAC2*

In our CVD system in RAC2, $SiH_4$, $HCl$, $H_2$ and $N_2$ are used for Si nanowires growth. Among them, the hydrogen chloride is definitely a toxic gas. According to the 40th Mechanical Working and Steel Processing Conference of the Iron and Steel Society in 1998, no stainless steel should be used in any system with hydrogen chloride. "The halogen gases, such as hydrogen chloride or hydrogen bromide, will corrode stainless steel when moisture level exceed a few ppm. Corrosion introduces the additional consequence of potential particle generation, which in turn may be responsible for yield reduction." [120] To produce good quality silicon nanowires, the ULSI Plus Six Nines ($\geq 99.9999\%$) should be used. In the CVD system, $EasyGas^{TM}$ 1000 and $EasyGas^{TM}$ 1500 are equipped as gas cabinets. Hydrogen chloride ($HCl$) plays a critical part in the growth process, especially for surface of silicon nanowires. There is a

touch screen on the top of gas cabinet, to control the gas flow and monitor the condition. Hydrogen chloride, which has a high saturated vapour pressure, is a gas at room temperature and ambient pressure.[121] In a sealed volume the hydrogen chloride will phase separate into liquid and vapour. They are in equilibrium when the chemical potentials of the two phases are equal.[122] The pressure of the hydrogen chloride cylinder is around 600 psi. That is why the pressure changes with room temperature but does not go down over time. There are three gas cabinets in this CVD system, using control panels to set and monitor the gas statements. For $N_2$, we use dewars to store and supply since it needs to be re-filled every week. There are two nitrogen dewars in the CVD system. One is for process using to flush the whole system all the time. Another is just to flush the Busch pump when it is needed. Another important part is exhaust gas cabinet (EGC). It is where all of gas goes from the output of the Busch pump and the output of the Venturi pumps from the gas cabinets. It mixes the process gasses with air at high temperatures to neutralize them. Shown in the Figure 4-4.

In the reaction zone, as mentioned before, it mainly contains load lock room and the reaction tube. The load lock room is a zone where to pump down incoming substrates for cleanness and to cool hot substrates prior to substrate unloading, users mounted and load samples here as well. To maintain neat in the tube, users would like to load sample in load lock room. Before transferring sample into tube, the pressure of load lock room is pumped down to 5 mTorr and back to atmosphere with $N_2$ in order to prevent contamination in CVD system. This is the reason why CVD engineers set a load lock room. The tube is brought form Firstnano, whose diameter is 100 mm. The Knudsen number for the system is around $10^{-3}\sim10^{-4}$. A mechanical arm is the only way to connect lock load room and glass tube.

Vacuum system consists of three pumps in our CVD system. The tube pump is Busch Cobra BA 100, which is scroll pump for corrosive gases. The base pressure is 0.01 mbar. The load lock pumps are Edwards nXDS 6i scroll pump and Edwards Turbovac SL80 turbo-molecule pump.

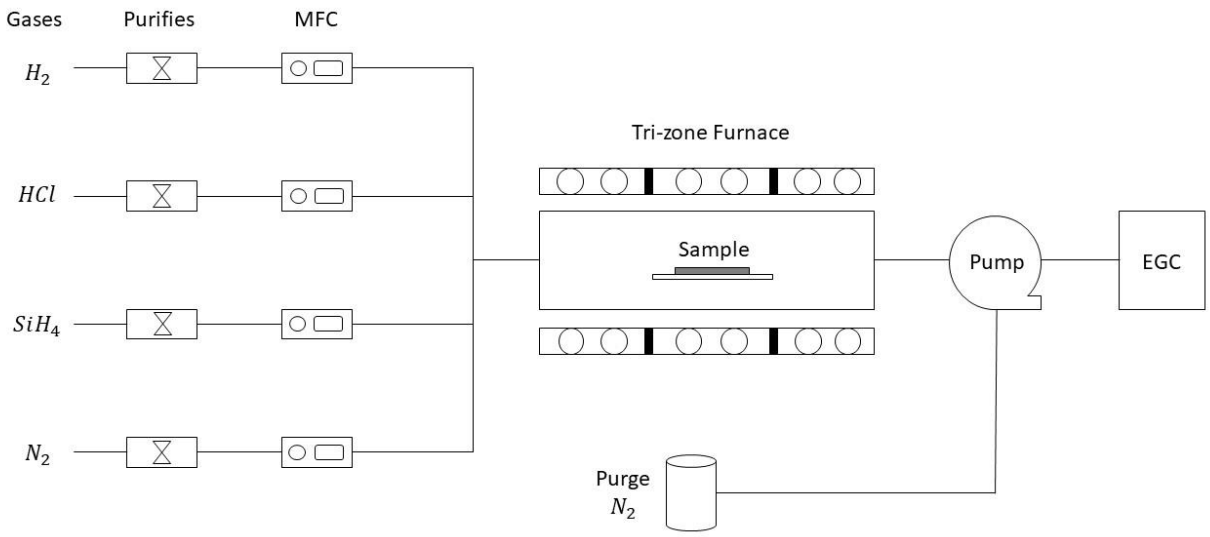


*Figure 4- 4 Diagram of CVD system in RAC*

## 4.5 Growth Recipe

The silicon nanowire growth is done in the thermal LPCVD. For our standard recipe, growth pressure is 4 Torr and growth temperature is 650℃. The recipe of growth gas is 20 sccm HCl, 1.0 slm $H_2$ and 10 sccm $SiH_4$ for 40min. Sccm is standard cubic centimeters per minute, slm stands for standard litre per minute. Both of them are mass flow unit. Under similar pressure and temperature conditions, the effective chemical potential of Si in silane ($SiH_4$) is higher than in $SiCl_4$; in other words, it is easier to grow silicon nanowires by using $SiH_4$ than $SiCl_4$, because the $SiH_4$ molecule is less stable. Therefore, we use $SiH_4$ as the Si source gas. The relationship of growth process and temperature in the reaction zone is shown in the Figure 4-5.

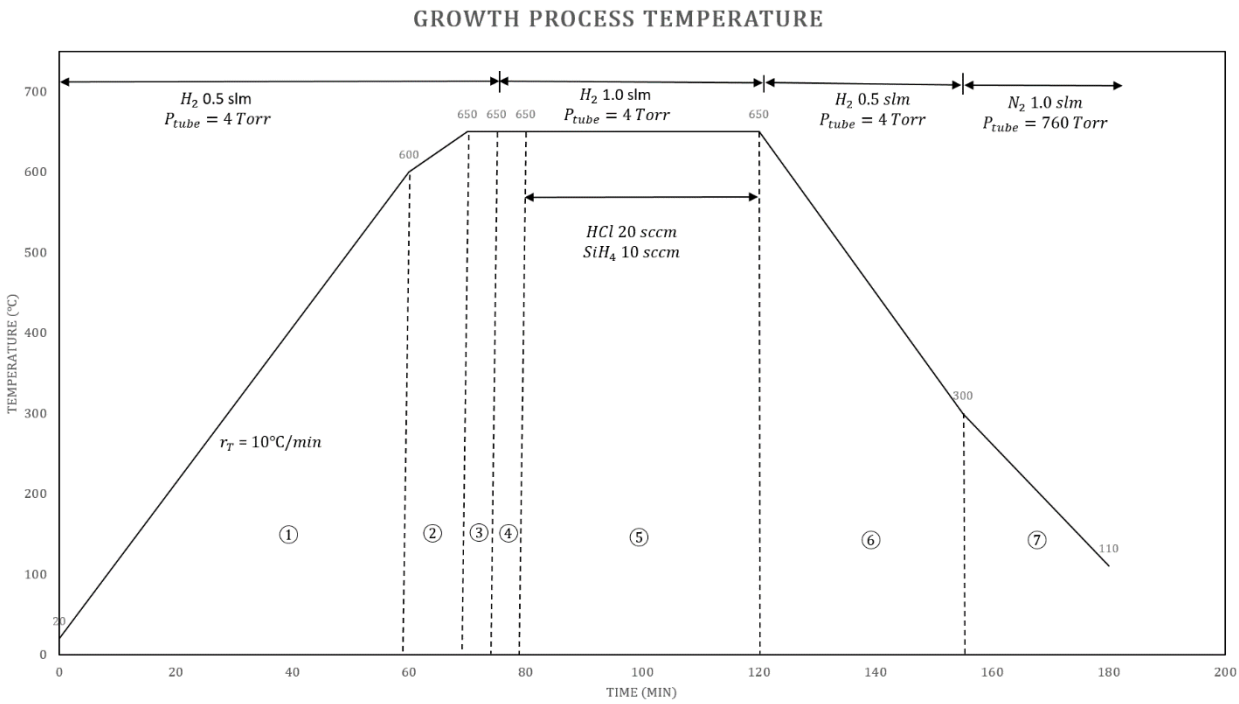


*Figure 4- 5 the furnace temperature profile for silicon nanowires growth recipe*

The sample is loaded in the load-lock firstly where $N_2$ is flushed all the time. To keep the cleanness of load-lock, the load lock is pumped down and back filled with $N_2$. To load the mechanical arm into tube (reaction zone), both load lock and tube are at atmospheric pressure when loading. The arm is transferred into tube, and then 50 mTorr is reached by using pumps to keep reaction zone clean for growth. Next, nitrogen is backfilled into reaction zone, and then pump down below 50mTorr again. The reaction zone is then flushed with hydrogen ($H_2$) to maintain the process pressure. The sample needs to be heated in hydrogen ($H_2$) environment, as $SiN_x$ would be produced if the Si substrate is heated in an environment with nitrogen ($N_2$). Moreover, the hydrogen ($H_2$) is helpful to stabilize the gold on the Si surface. To save cost during warm up, the rate of $H_2$ flow is 0.5 slm. When the temperature in the tube reaches 650℃, the flow of $H_2$ increases to 1.0 slm. HCl and $SiH_4$ start flowing in the gas line to the EGC at the same time. It takes 10 min to stabilize the flow of gases. Growth starts once $SiH_4$ and HCl vent to system. After the growth step, the sample is cooled down to 300℃ by fluxing hydrogen, and then the sample is cooled down to 110℃ in a nitrogen environment. The pressure of tube is kept at 4 Torr during the growth

process. In the last cooling down step, the nitrogen ($N_2$) pressure increases to atmosphere for later unloading.

# Chapter 5 Results and Discussion

To determine growth properties and fine tune the recipe, we first work with gold drop-cast catalyst particles. This is significantly less work than preparing patterned nanowires arrays and allowed us to make progress while developing the technique for fabricating arrays.

Gold nanoparticles are useful since they have a defined size and are cohesive and spherical. It makes them suitable for determining growth characteristics at the start of the growth process. By comparison, EBL patterned catalyst are formed as a disc, which has defects leading to multiple growths from one location.

## 5.1Drop-casting

In drop-casting, the positions of Au nanoparticles on the Si substrate are random (shown in Figure 5.1 (a) and (b)). It is easy to prepare and control the diameter of Si nanowires, which is mainly dependent on the size of Au nanoparticle. The different ratio prepared gold solutions give different densities of Si nanowires on the substrate. The original 100-nm gold nanoparticle solution is bought from Ted Pella with $5.6 \times 10^9$ particles/ml. And different sizes of gold have different densities of particles. However, based on our dozens of test, the 1:20 diluted gold nanoparticle solution is suitable for all gold sizes. Therefore, all SEM pictures in this section are from 1:20 diluted gold nanoparticles solution, and the silicon nanowires are grown in the 20 sccm HCl, 10 sccm $SiH_4$ and 1.0 slm $H_2$ for 40 minutes. The SEM images are taken by Zeiss Leo 1530 and UltraPlus FESEMs (with EDX/OIM).

### 5.1.1 50nm nanoparticles

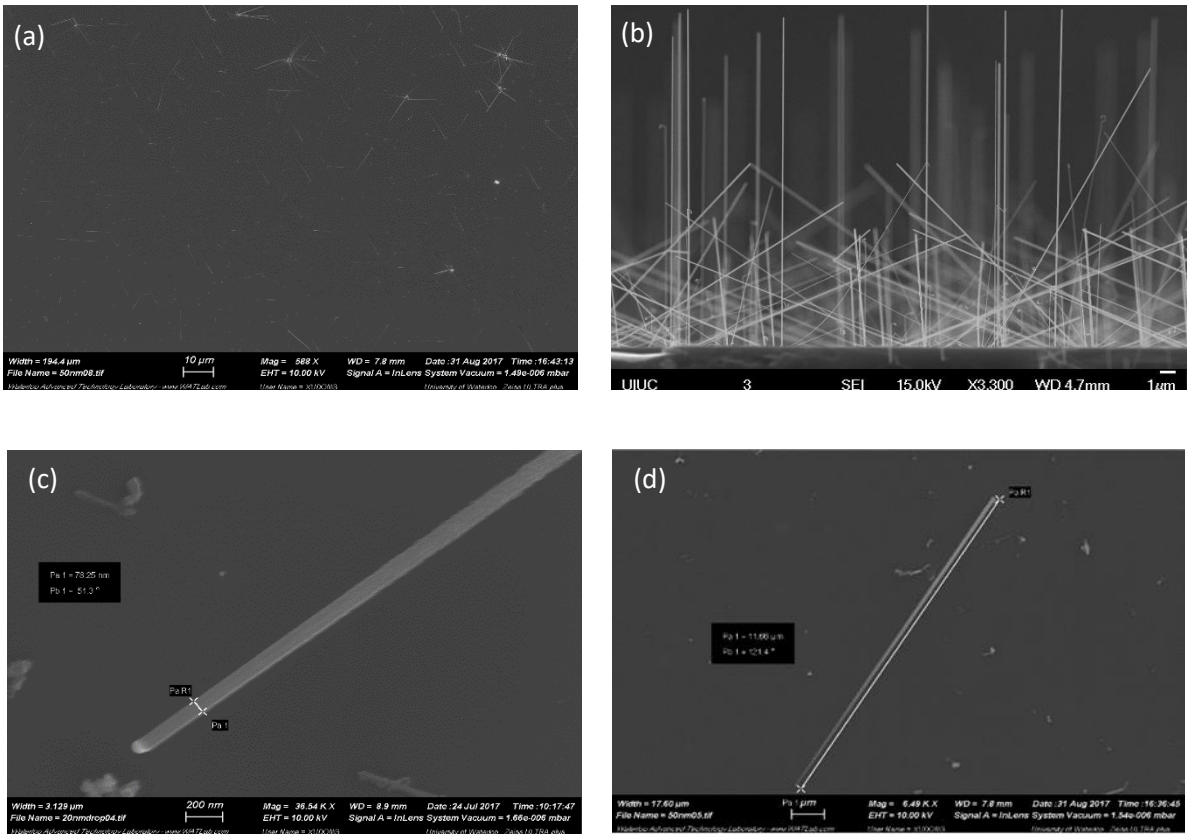


*Figure 5- 1 SEM images of 50nm growth by drop-casting. (a) top view of the drop-casting growth (b) side of the drop-casting growth (c) the measurement of tip for 50 nm SiNWs (d) the measurement of length for 50 nm SiNWs*

After 40min growth, the average length of 50 nm Si nanowires is 10.27$\mu m$. The size of Au nanoparticles are 50nm, and the average tip diameter is 67.73 nm, and the average bottom diameter is 87.19 nm. The taper is 0.95 nm/$\mu m$, which is the radial difference per micrometer length. The grow rate is 256.75 nm/min. The radial deposition rate, which is radial increasing rate per minute, is 0.24 nm/min. The Figure 5-1 are taken in top view.

### 5.1.2 100nm nanoparticles

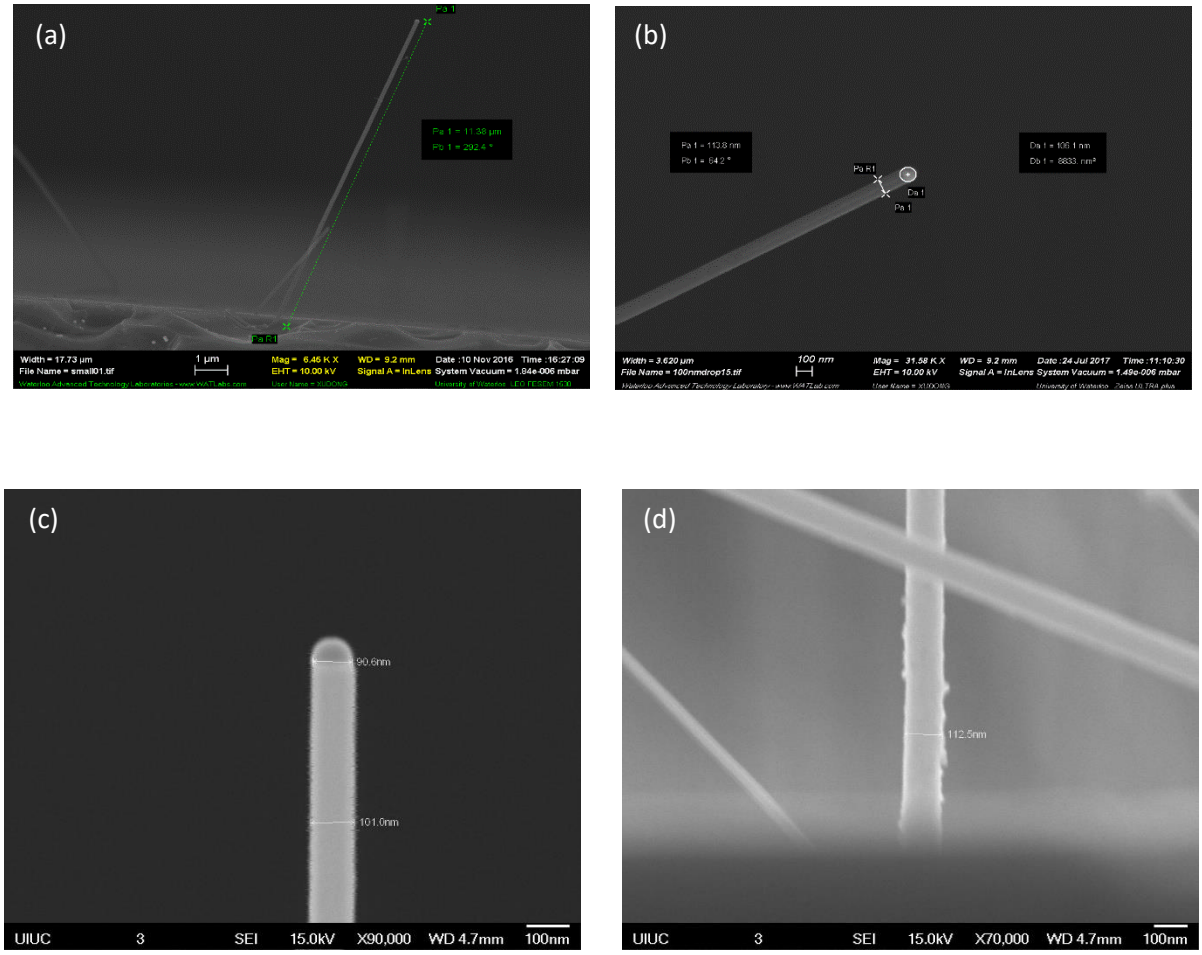


*Figure 5- 2 SEM images of 100nm growth by drop-casting. (a) the measurement of length for 50 nm SiNWs (b) and (c) the measurement of tip for 50 nm SiNWs (d) measuring base diameter of 100 nm SiNWs*

The average length of 100nm Si nanowire is 15.75$\mu m$. The size of Au nanoparticles are 100nm. The average tip diameter is 104.75nm, and the average bottom diameter is 128.4nm. Its taper is 0.75 nm/$\mu m$. The growth rate is 393.75 nm/min. The radial deposition rate is 0.30 nm/min. The diameter of Si nanowires decreases with time during the growth. The SEM images in figure 5-2 are taken in side view.

### 5.1.3 150nm nanoparticle

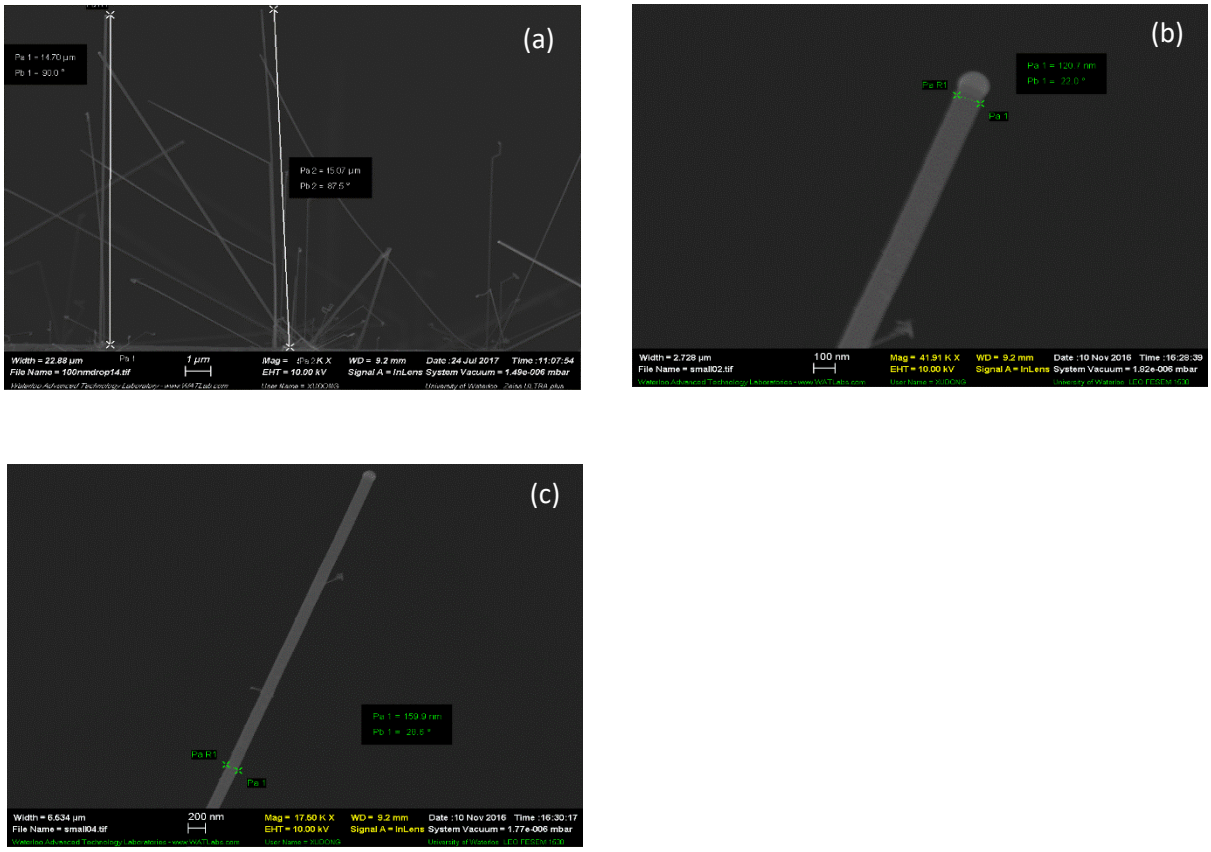


*Figure 5- 3 SEM images of measurement for drop-casting 150 nm SiNWs*

The average length of 150nm Si nanowire is 17.36$\mu m$. The size of Au nanoparticles are 150nm. The average tip diameter is 150.48 nm and the average bottom diameter is 177.03 nm, and the average bottom diameter is 177.03nm. The taper is 0.76 nm/$\mu m$. The difference is 36.55nm. The growth rate is 404 nm/min. The radial deposition rate is 0.33nm/min. The diameter of Si nanowires decreases with time during the growth as well. The SEM images in Figure 5-3 are taken in side view.

*Table 5- 1 Characteristics of drop-casting SiNWs*

| Au nanoparticles | Length | Growth rate | Tip diameter | Bottom diameter | Taper | Radial deposition rate |
|---|---|---|---|---|---|---|
| 50 nm | 10.27 $\mu m$ | 256.8 nm/min | 67.73 nm | 87.79 nm | 0.95 nm/$\mu m$ | 0.24 nm/min |
| 100 nm | 15.75 $\mu m$ | 393.8 nm/min | 104.75 nm | 128.40 nm | 0.75 nm/$\mu m$ | 0.30 nm/min |
| 150 nm | 17.36 $\mu m$ | 434.0 nm/min | 150.48 nm | 177.03 nm | 0.76 nm/$\mu m$ | 0.33 nm/min |

According to the table above, the tip diameter is close to the size of gold nanoparticles. That means the radical deposition rate is reliable. The taper is the radius changes per micrometer. As mentioned before, the HCl could prevent catalyst break up. The taper is much better than before, which is 7.06 nm/$\mu m$.[23]

High resolution images (like figure 5-3 b, c) show that the surface of the nanowires is not perfect. There are some branches on a few nanowires' sidewall. The length of nanowires increases as the diameters of Au nanoparticles increases. That means the growth rate of silicon nanowires by CVD with silane ($SiH_4$ ) varies with the size of Au droplet. The difference of tip diameter and bottom diameter suggests that the direct CVD growth of Si occurs on the sidewalls constantly during the VLS growth. Also, according to the high-resolution images, the surface of Si nanowires is relatively smooth. That shows the VLS growth is faster than the chemical vapor deposition growth on the sidewalls of silicon nanowires.

Based on the Figure 5-1 (b), the position of growth by drop-casting is random, and this makes it hard to isolate detect a single nanowire when the quality factor is measured. To avoid this situation, the location-controlled growth by using EBL pattern is necessary.

### 5.1.4 The mechanical properties of 100nm Si nanowires

As mentioned in the chapter one, the silicon nanowire is a suitable probe in the MRFM. As an important parameter of the cantilever, the quality factor is measured by Bill Rose at the University of Illinois at Urbana–Champaign (UIUC). It is in the range of $1.0 \times 10^4$ to $2.1 \times 10^4$. The resonance frequency is in the range of $2.1 \times 10^5$ Hz to $3.6 \times 10^5$Hz.

We can assume the silicon nanowire is a cylinder since the low taper. And the silicon nanowire can be treated as a cantilever beam. As a result, the theoretical spring constant, k, can be calculated. For a cantilever beam which has one fixed end, its spring constant follows the equation: $k = 3EI/L^3$. The E here is Young's Modulus, I is area moment of inertia and L is the length of cantilever. When the cross-

section is round solid, the area moment of inertia I is $\frac{\pi d^4}{64}$, where d is the diameter of the cantilever. Therefore, the spring constant of silicon nanowires is

$$k = \frac{3}{64}\frac{E\pi d^4}{L^3} \tag{4.1}$$

The Young's Modulus of silicon is 168.9 $GPa = 1.689 \times 10^{11} Pa$. The length of the silicon nanowire, which was measured by Bill, is 21.68 $\mu m$. The diameter is 105 nm. The resonance frequency is 212 kHz. Therefore, the theoretical value of spring constant is ~300 $\mu N/m$. By using the equation (1.3), the intrinsic dissipation is in the range of $6 \times 10^{-15}$ to $18\times 10^{-15}$kg/s. Compared with table 1-1, our result for the 100 nm Si nanowire, $6 \times 10^{-15}\ kg/s$, is as good as Nichol's work. Nichol's lowest dissipation is $5\times 10^{-15}$kg/s which is from a 44 nm Si nanowire.[14] It is also an improvement since the larger Si nanowires are easier for laser detection system to get a better signal.[22]

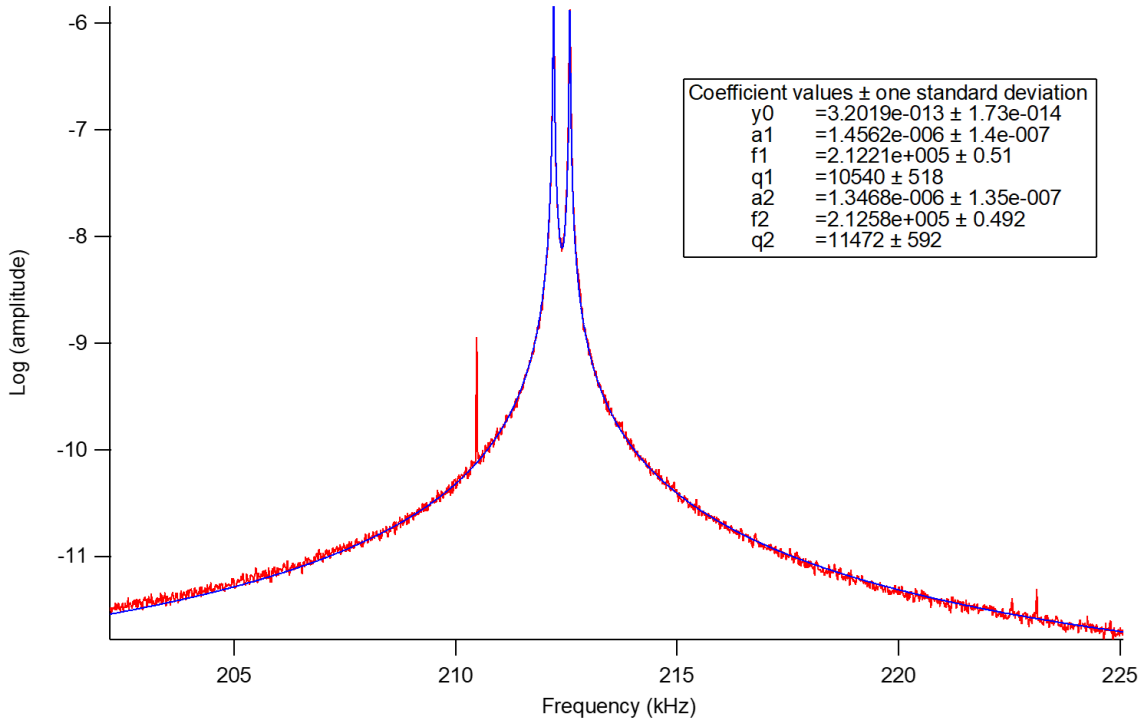


*Figure 5- 4 The measurement for quality factor and resonance frequency of SiNWs.*

## 5.2 EBL pattern

The purpose of growing silicon nanowires with EBL is to achieve location-controlled growth of vertically aligned silicon nanowires. As mentioned before, the growth on the Si (111) substrates uses Au as a catalyst. The substrate is patterned firstly by EBL, followed by depositing gold to the pattern. The excess gold is then lifted off. The SEM images are taken also by Zeiss Leo 1530 and UltraPlus FESEMs (with EDX/OIM).

At the initial stage of project, we followed the Park's technique to grow patterned silicon nanowires.[1] After EBL patterning, the gold seed is deposited on the silicon oxide layer directly. Unfortunately, no patterned gold seed is left after lift-off step, since the adhesion between Au and $SiO_2$ is weak. To avoid this situation, a BOE step before the gold depostion is added. BOE (buffered oxide etch), as an etching solution, creates pits for gold to reside and prevents the loss of gold during lift-off. Moreover, the native oxide layer with pits is acted as a secondary mask for pattern. The gold pattern survives after the lift-off with this additional BOE step. The duration of BOE is around 15 seconds for native silicon wafers after a number of test. Over etching is shown in section 3.2.4. The effective results are shown below.

Figures 5-5 is the top view of patterning under SEM. The spacing between one gold disk to another is $8\mu m$. The diameter of gold disk is around 230 nm, as shown in the Figure 5-5 (d). The total volume of the gold disk is $2.1 \times 10^5\ nm^3$. The diameter of the alloy ball is around 90 to 100 nm. The SEM pictures of growth are shown in the Figure 5-6. The average diameter at top of silicon nanowires is 95.20 nm. Therefore, at the high enough temperature condition, the disk will transform into the Au-Si alloy ball, whose volume is about 2.0 to 2.2 times that of the gold disk.

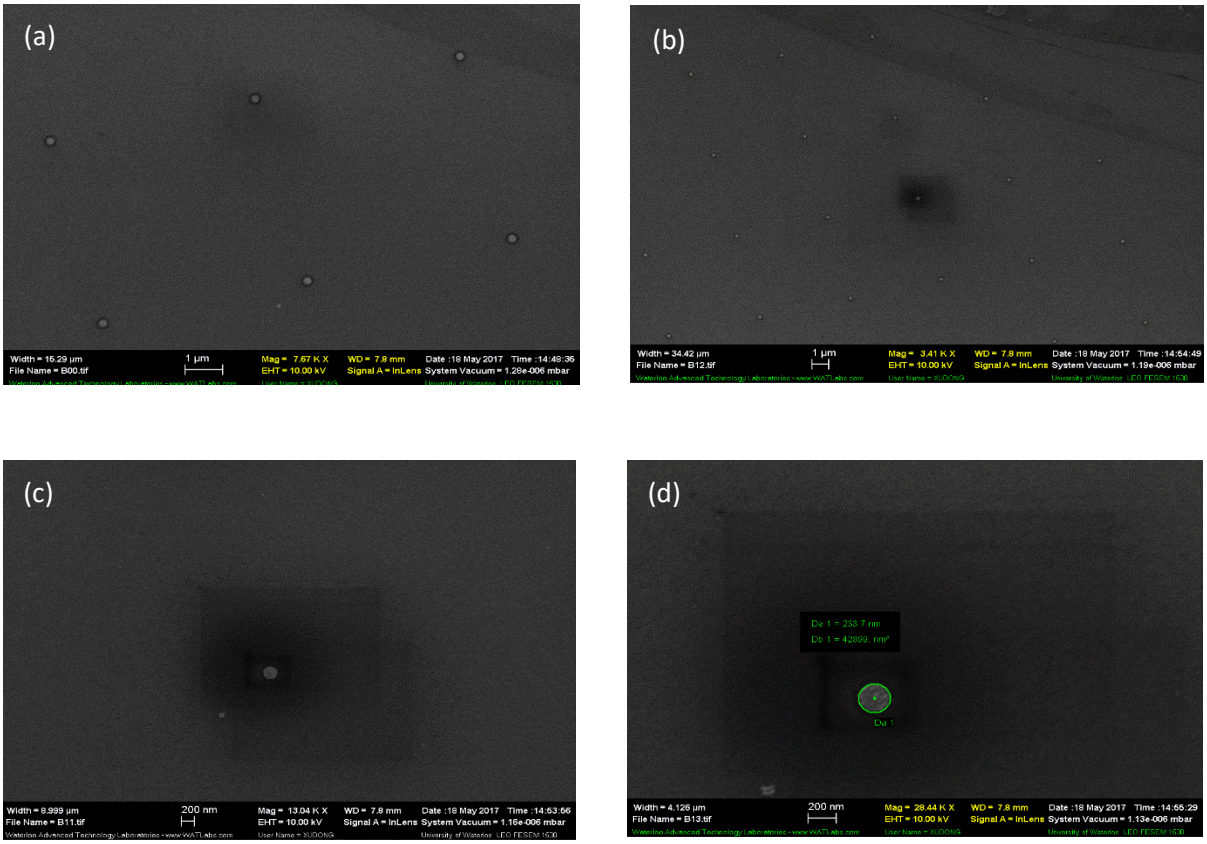


*Figure 5- 5 SEM images of EBL pattern*

In this recipe, we tried 3 different size of nanowires. The average length of 50nm Si nanowires is 11.68 μm, and the average length of 100 nm silicon nanowires is 11.98 $\mu m$. The average length of 120 nm Si nanowires is 11.89 $\mu m$. The apparent growth rate is defined by the length of Si nanowires divided by the total growth time, 40 min. Unlike the growth rates of drop-casting, which varies with the size of nanoparticle, these growth rates are close to each other. These results are in agreement with Schmid's work in 2008[123] and may be explained as follows. According to their work, the apparent growth rate is not necessarily the same as the actual growth rate. The latter excludes the time it takes for Au nanodisk nucleation. Since larger disks require more time to nucleate, the decrease in actual growth time is counteracted by the increase in nucleation time, resulting in similar apparent growth rates.[123] As with the drop-casting method, the diameter of Si nanowires decreases with time during the growth. The radial deposition rates are 0.37nm/min and 0.26nm/min for 50nm nanowires and 100 nm nanowires. Obviously,

the radial deposition rate is decreasing as the diameters of nanowires increasing. The SEM images in Fgure 5-6 are taken in side view.

*Table 5- 2 Characteristics of EBL SiNWs*

| Target diameter | Length | Growth rate | Tip diameter | Bottom diameter | Taper | Radial deposition rate |
|---|---|---|---|---|---|---|
| 50 nm | 11.68 $\mu m$ | 292.0 nm/min | 64.69 nm | 94.14 nm | 1.26 $nm/\mu m$ | 0.37 nm/min |
| 100 nm | 11.98 $\mu m$ | 299.5 nm/min | 95.20 nm | 115.85 nm | 0.86 $nm/\mu m$ | 0.26 nm/min |
| 120 nm | 11.89 $\mu m$ | 297.3 nm/min | 119.06 nm | 136.20 nm | 0.69 nm/$\mu m$ | 0.21 nm/min |

According to high resolution images, the surface of silicon nanowires is smooth. That means the VLS growth is faster than the chemical vapor deposition growth on the sidewalls of silicon nanowires during the growth time. The second picture shows the askew Au nanoball. This implied that the Au ball may has migrated over the nanowire sidewalls. It also suggests that the nanowire sidewalls may be covered by a few Au particles, which may lead a branch growth, shown in the Figure 5-6 (c).

Fiture 5-7 shows the Silicon nanowires axial growth rate in drop-casting method and EBL method. It is clear that the apparent growth rates stay stable, around 300nm/min, in EBL method. It is independent of the diameter of the nanowires. However, the growth rate in the drop-casting increases as the diameter increases.

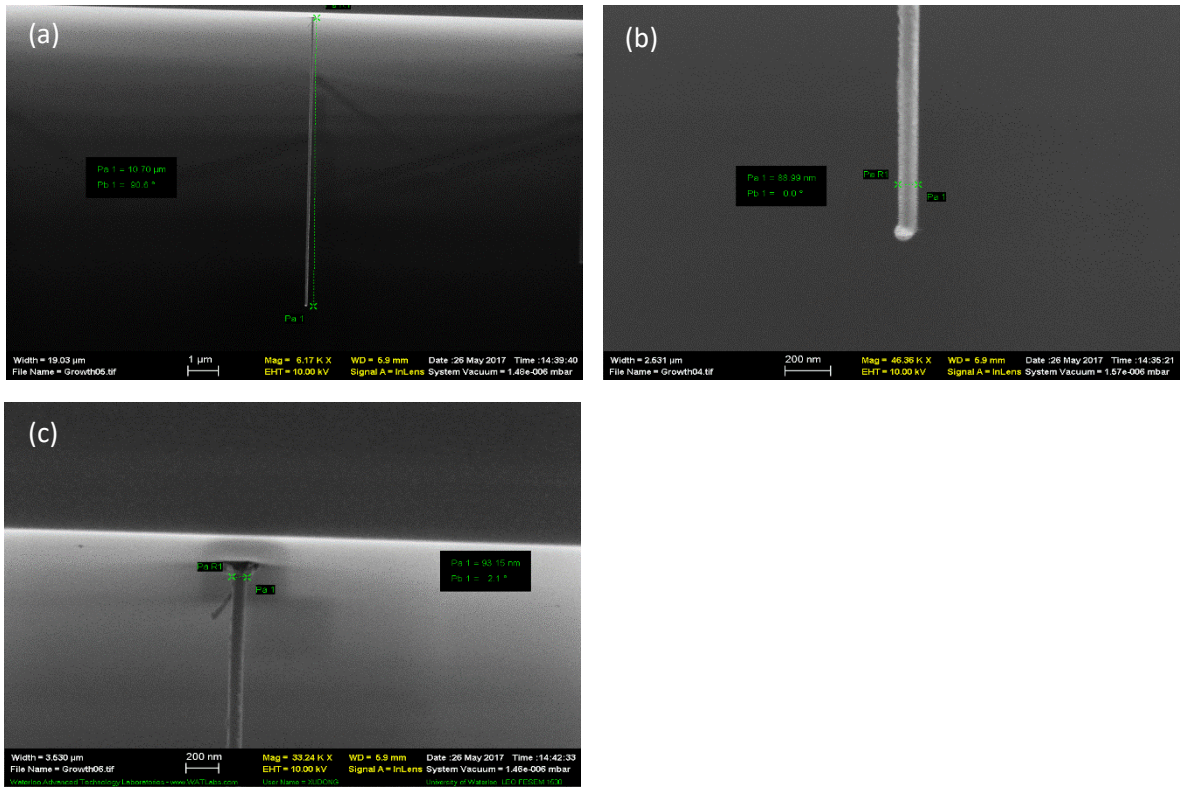


*Figure 5- 6 SEM images of EBL patterned SiNWs*

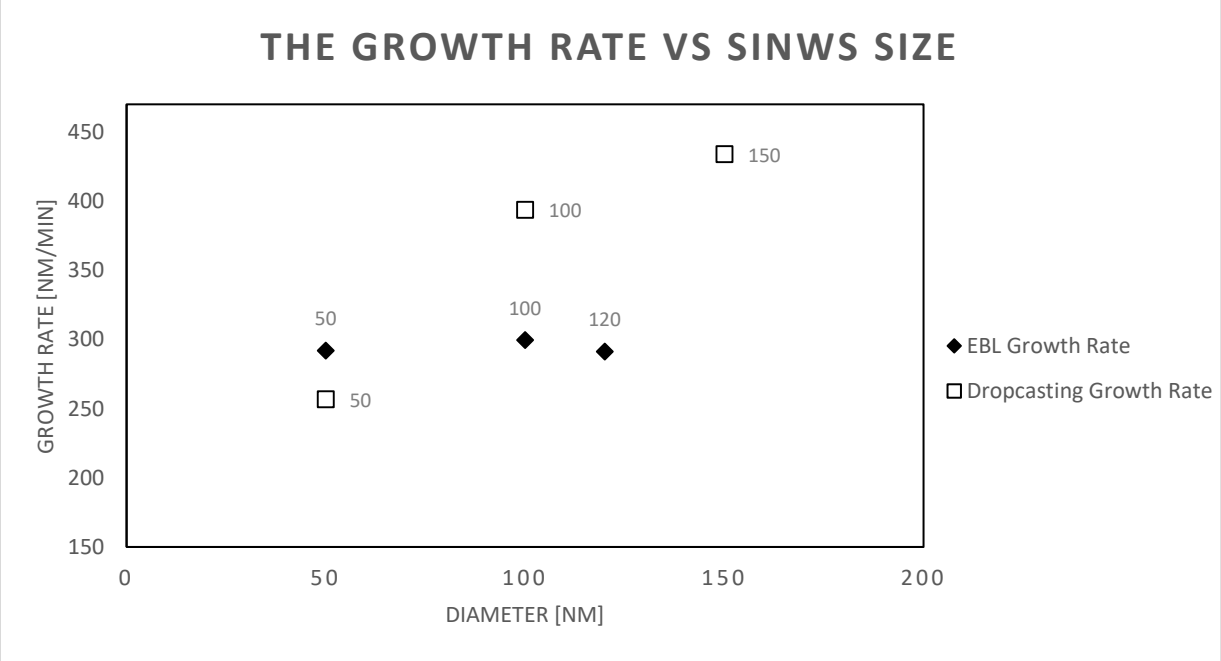


*Figure 5- 7 Growth rate vs sizes of silicon nanowires.*

## 5.3 Vertical yield

On the silicon (111) wafer, nanowires are mainly grown in the <111> direction. However, not all nanowires are in <111>, and kinking can sometimes be observed. It is important to control the growth direction and improve the vertical yield for applying it to MRFM. The Figure 5-8 (a) to (d) below show arrays of 50-nm-diameter, 100-nm-diameter and 120-nm-diameter Si nanowires grown in the <111> direction on the N-type (111) Si wafer. The kinking is observed in all samples. The yield of vertical epitaxial wires for different diameter, including 50 nm, 100 nm and 120 nm, is in the range of 60% to 90%. All samples have skew wires at the same growth environment. The chart shows 4 different silicon nanowires arrays consisting of 50-, 100-, and 120-nm-diameter wires grown at 650℃ and 4.00 Torr for 40 min. Based on the chart, the vertical yield is independent of nanowires diameter. This result agrees with Schmid's work.[123]

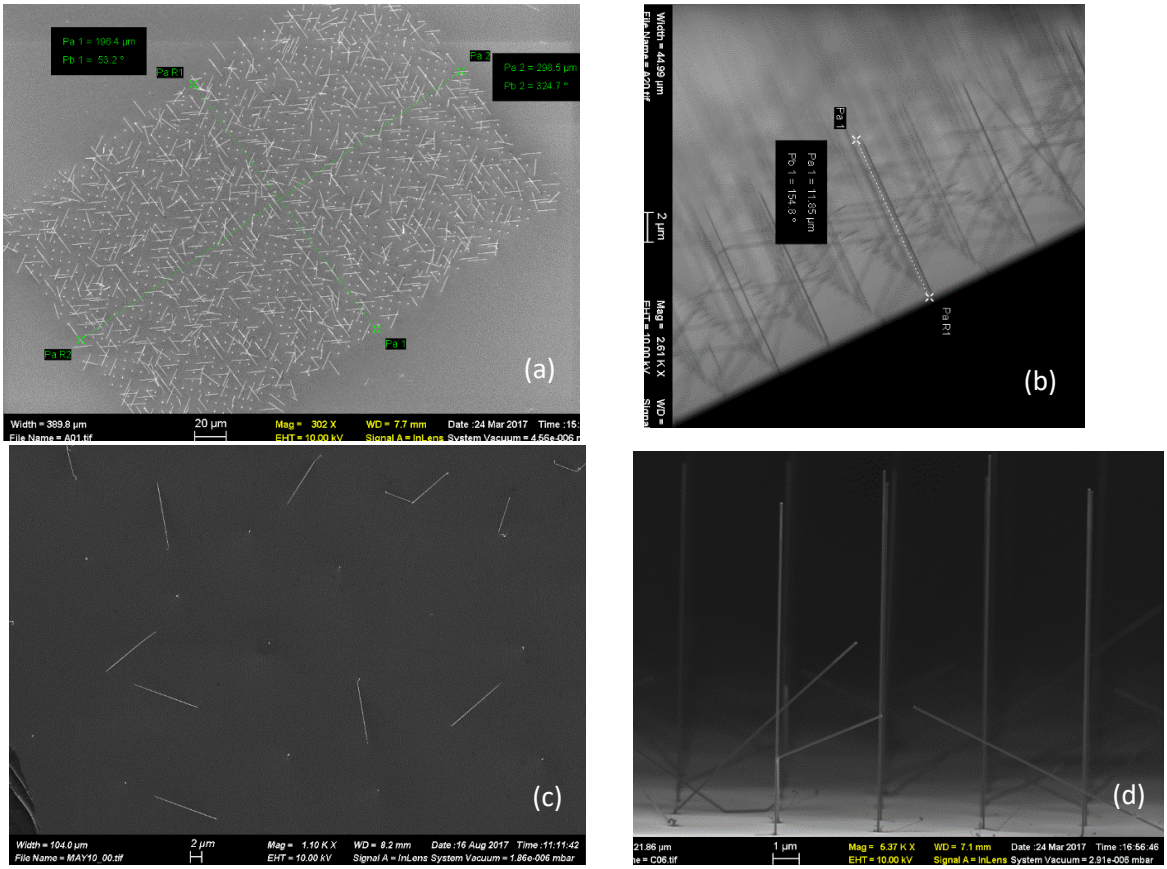


*Figure 5- 8 SEM image of 50 nm, 100 nm, 120nm EBL SiNWs in top and side view.*

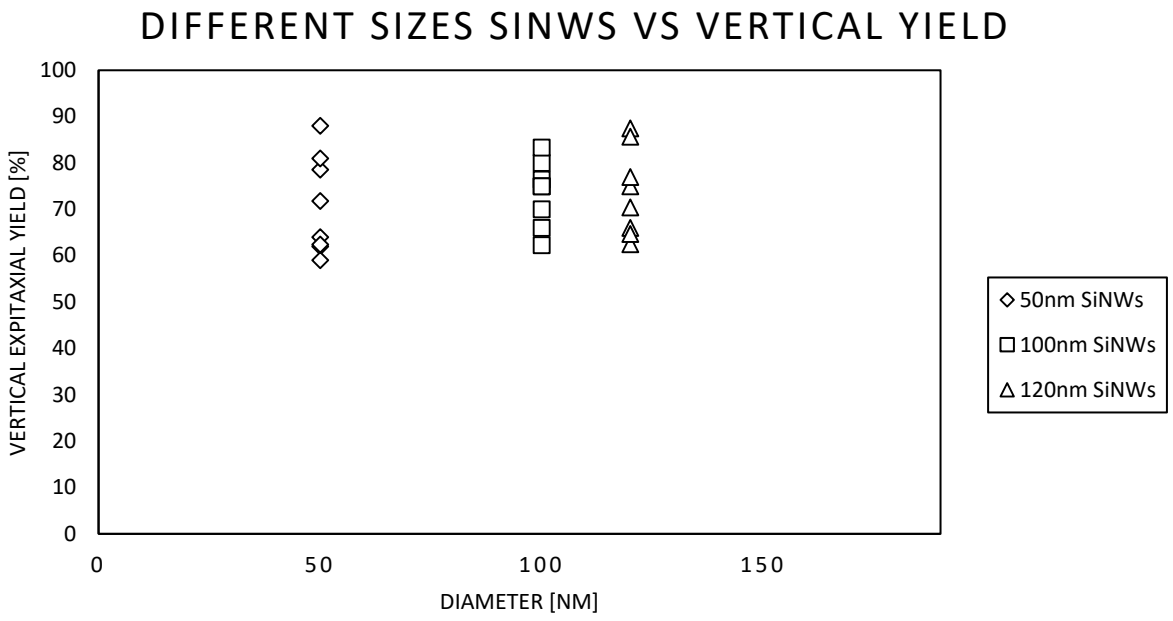


*Figure 5- 9 Yield of vertical epitaxial wires vs diameters of SiNWs ranging from 50nm to 150nm, obtain from ≃100wires*

## 5.4 Non-vertical Growth

The results below are observed with an insufficient BOE step. The native oxide layer is residual on the substrate. As shown in the Figure 5-10 (a), all the nanowires are not vertical. Based on the Figure 5-10 (b), at the beginning of growth, the wires are along the (111) direction, which is perpendicular to the substrate. Afterwards, the growth direction switches to other six (111) growth directions (as shown in the Figure 5-10 instantaneously, a process we call kinking.[123] The kinking occurs in each experiment, and it mainly happens close to the surface of substrates. It is rare that the kinking occurs immediately at the beginning of the growth. Moreover, the kinking usually occurs once, and then the direction of growth remains unaffected. Multiple kinking happens, only when two or more wires touch each other. These results point out that the growth defect is more sensitive at the beginning of nucleation phase. The growth condition is stable when the eutectic melt has reached the equilibrium point.[123] Multiple growth from one location is observed in the figures below. Compared with SEM images in the previous section, the difference, i.e. multiple growth, is due to the native oxide layer, which impedes a compact and uniform

contact between Au catalyst and Si (111) substrate. The adhesion between Au and $SiO_2$ is weaker than the Si. Without annealing step, the small gold nanoparticles around one big gold nanoparticles are still seeds for Si nanowires. Therefore, the native oxide layer should be removed before the gold deposition to reach a relative high vertical yield and high quality of silicon nanowires. However, the oxide layer should be reserved when the annealing is added before the growth.

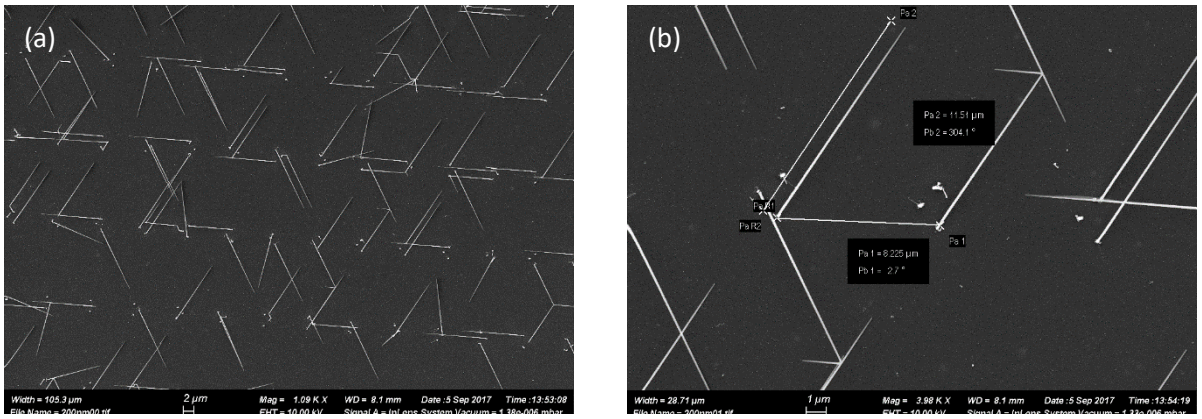


*Figure 5- 10 Top view SEM images of an array of 100 nm SiNWs*

A more detailed analysis and discussion of the kinking can be drawn from Figure 5-12. The possible kinking directions are shown in Figure 5-11. In the top view, there are 6 different direction which are separated by 60°. The chart below shows the percentage of wires growing in the six possible directions (based on over 60 nanowires). In the top right of chart, the definition of kinking directions are displayed and the vertical wires is at the center of circle. As shown in the chart, kinking of the silicon nanowires is possible in all 6 directions. In our growth condition, the kinking is most likely to occur at 60° direction (i.e. $(1\bar{1}1)$). One possible reason is that this is the direction of gas flow in the tube.

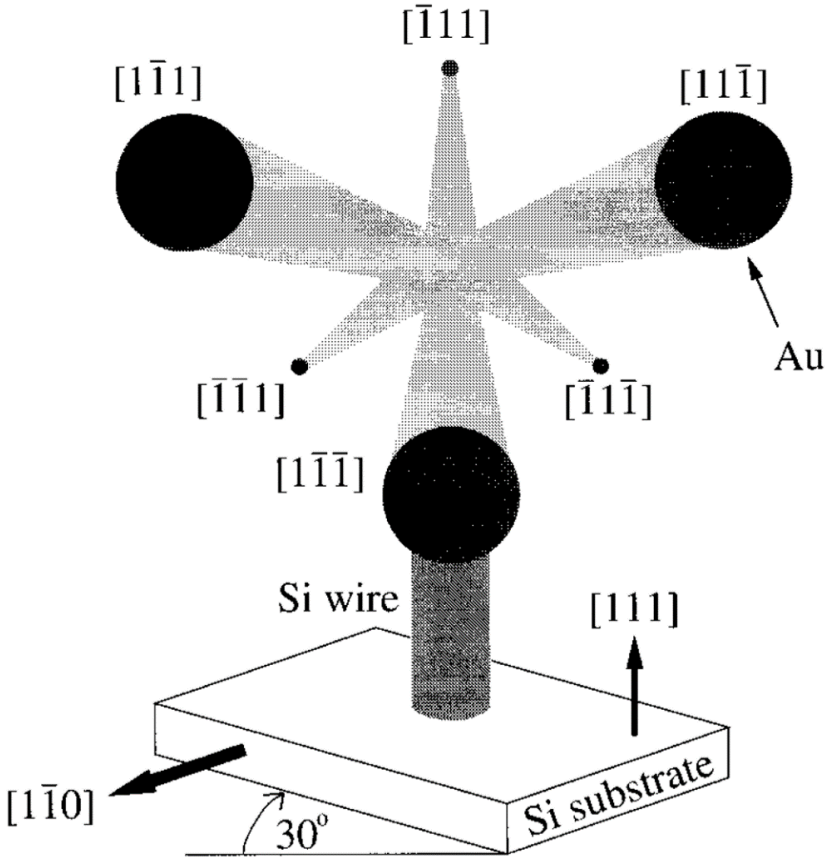


*Figure 5- 11 Possible growth directions of SiNWs on Si (111) substrate*[124]

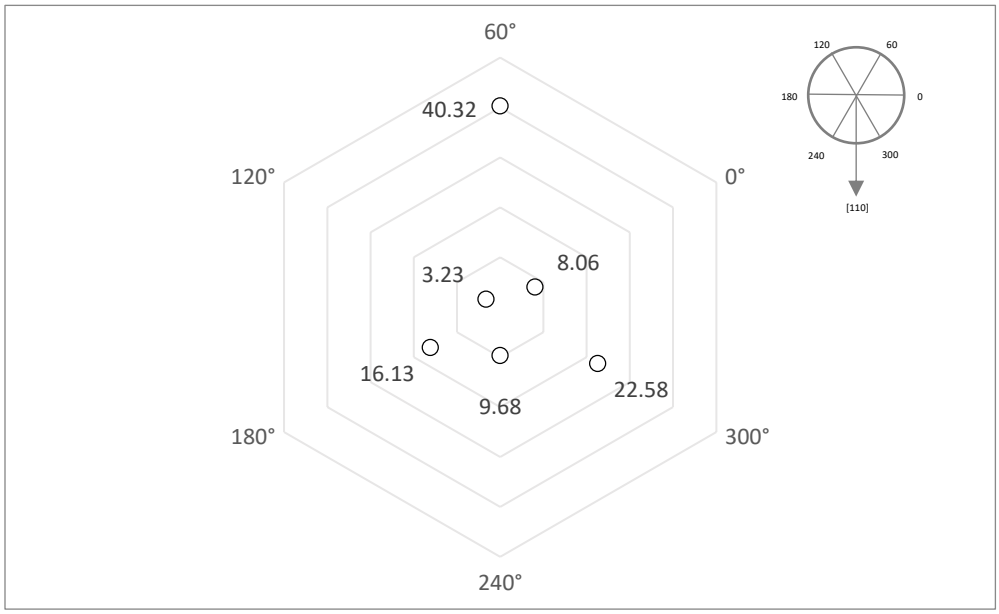


*Figure 5- 12 the percentage of wires growing in possible direction for 100 nm SiNWs on Si (111) substrate.*

# Chapter 6 Conclusion and Future Work

## 6.1 Conclusion

The project presented shows that patterned Au can be used as a catalyst to grow silicon nanowires at certain position. The hydrogen chloride could reduce the migration of gold and smooth Si nanowires' surface. The oxide layer should be removed before growth in order to avoid low vertical yield and the multi-growth from one location. The pattern is achieved by using electron beam lithography (EBL), which could be used in the range of nanometer scale in a large area ($cm^2$). The growth rates are different for different gold seed preparation. In the EBL method, the growth rate is independent of the diameter of silicon nanowires, whereas for drop-cast the growth rates increase with the diameter of silicon nanowires. The taper of our Si nanowires is around 1 nm/$\mu m$, which is much better than previous result.[23] The lowest intrinsic dissipation of the 100 nm drop-casting Si nanowire is $6 \times 10^{-15}$ kg/s.

## 6.2 Future work

To improve the vertical yield, the control of HCl flow during the growth is very important. Some evidences show that the HCl partial pressure plays an important role in growing vertical Si nanowires. Therefore, higher ratio of HCl in the recipe should be tried. Another way is to prepare a better and cleaner substrate. Growing a suitable thick oxide layer first and then removing it should be applied in the future. To shorten fabrication period, it is reasonable to heat lift-off solution (PG Remover) properly. Based on research, the annealing step is helpful to decrease the tapper. A study about annealing should be done in the future. For better understanding, studying the growth under different temperature is a common way to get apparent activation energy $E_g$ with the Arrhenius equation, which is helpful for analyzing the growth kinetics. Furthermore, the mechanical properties for EBL silicon nanowires should also measured. In addition, since the silicon nanowires will ultimately serve as the cantilever for the MRFM, it needs to be grown on a $1 \times 1.5$ mm chip, which is too small for usual mechanical operation. As a result, deep reactive-ion etching (DRIE) may be a suitable technique and should be looked into.

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# Appendix

## 1. Manual of Spin-coating

### 1.1 Spin-coating Shirley 1811

1. Load the sample on the hotplate at 180℃ for 5 minutes

2. Load the sample on the spin coater and drop a moderate mount of Shirley 1881

3. The spin-coating of Shirley 1811 is achieved by spinning at 5000 rpm with 1000 rpm/s for 60 seconds.

4. Put the sample on the hot plate for 5 minutes at 180℃.

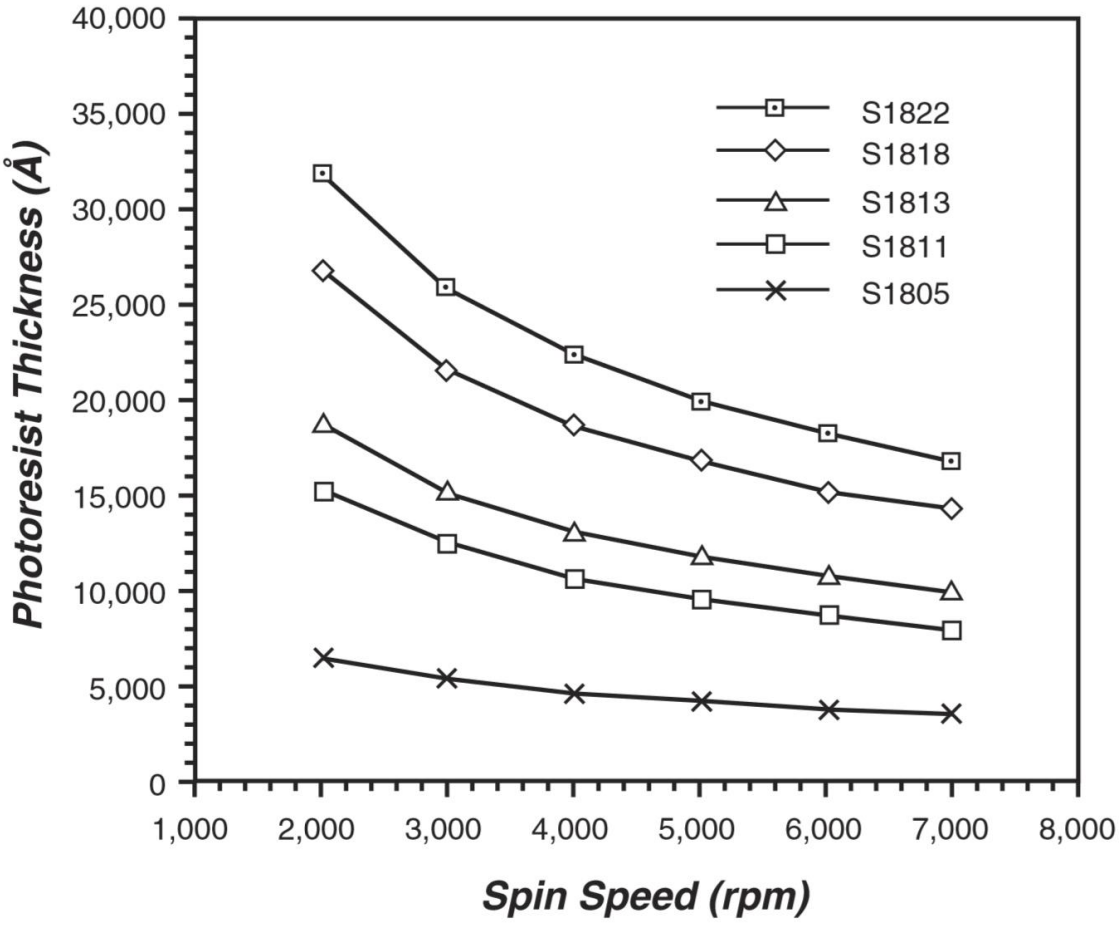


*Figure A- 1 The spin speed versus film thickness curve for Shirley 1811*[125]

## 1.2 Spin-coating PMMA A3

1. Load the sample on the hotplate at 180℃ for 3 minutes

2. Load the sample on the spin coater and drop a moderate mount of PMMA

3. The spin-coating of PMMA is achieved by spinning at 6000 rpm with 1000 rpm/s for 60 seconds.

4. Put the sample on the hot plate for 3 minutes at 180℃

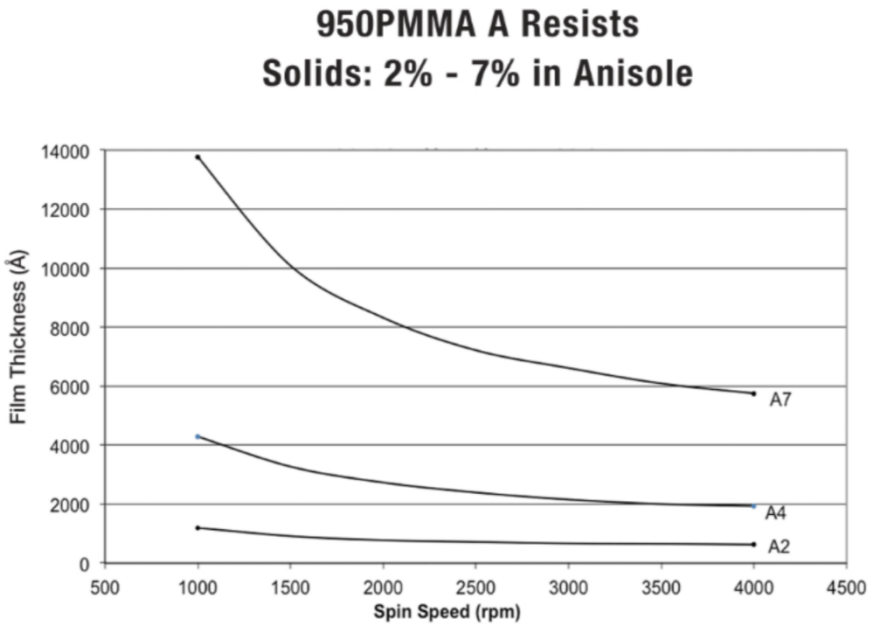


*Figure A- 2 the spin speed versus film thickness curve for PMMA 950*[126]

## 1.3 Spin-coating MMA for Bilayer

The MMA is spin-coated as a bottom layer when bilayer is applied. The coating of MMA is achieved by spin-coating the sample at 5000 rpm with 1500 rpm/s for 60 seconds. And PMMA is same with single one. The sample was baked for 5 mins at 180℃ after each layer coated. The total thickness is around 300nm.

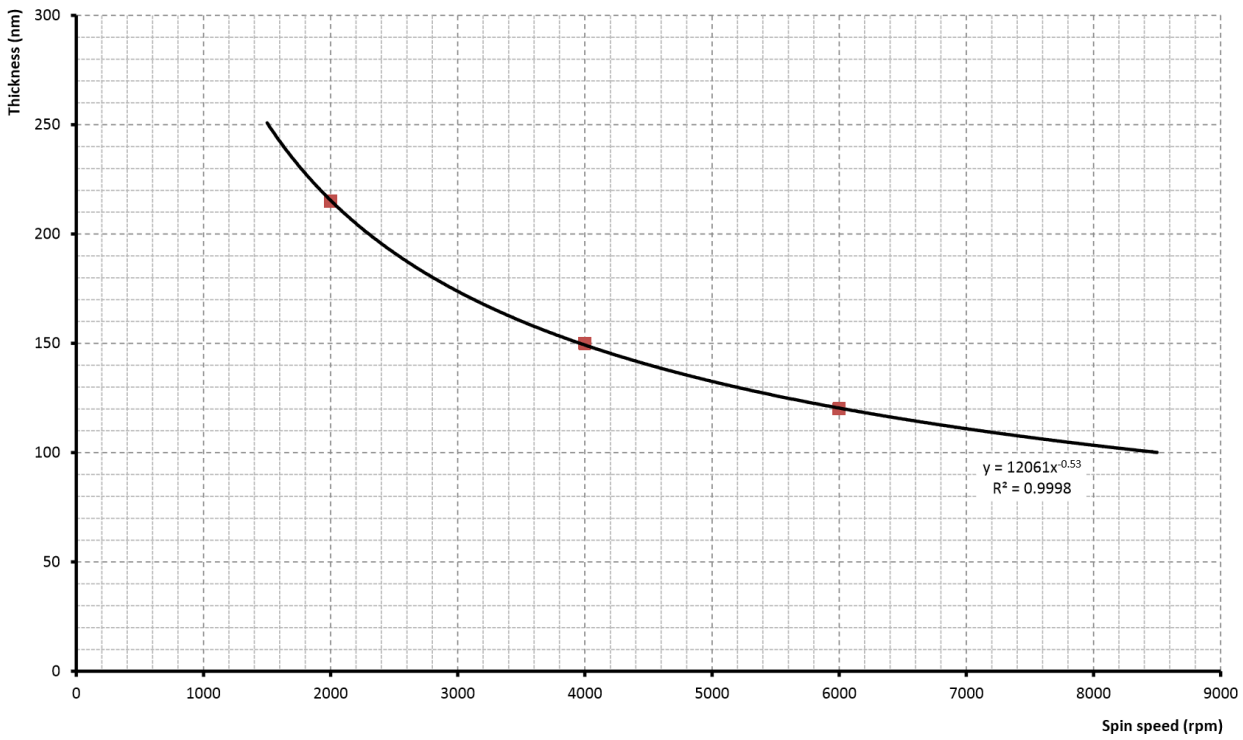


*Figure A- 3 the spin speed versus film thickness curve for MMA*[127]

## 2. Manual of dicing silicon (111) wafer by using DISCO DAD3240

First step is to coat the native silicon wafer by a few micrometers Shirley 1811 which is a kind of photoresist to protect the wafer surface. Second, cut the silicon wafer into 8mm by 8mm chips by DISCO DAD3240. The SOP could be found on the official website of Quantum nanofab of University of Waterloo official website.

## 3. Recipe of RCA clean

*Table A- 1 Standard Recipe of RCA Clean*

| RCA step | DI water (mL) | $NH_4OH$ (mL) | $H_2O_2$ (mL) |
|---|---|---|---|
| SC-1 (80℃) | 300 | 60 | 60 |
| RCA step | DI water (mL) | HCl (mL) | $H_2O_2$ (mL) |
| SC-2 (80℃) | 500 | 80 | 80 |

## 4. Recipe of Diluted Gold Nanoparticle Solutions

There is no 1M HF solution in the clean room, only 49% HF is provided. To configure 500ml 1M HF solution, 17.6 ml 49% HF is added into 482.4ml DI water. All operation should be done with mandatory personal protective equipment (PPE) which includes cleanroom nitrile gloves, safety glasses, tychem yellow apron, face-shield and green nitrile gloves.

*Table A- 2 Recipe of Diluted Gold Nanoparticle Solutions*

| Au nanoparticles solution | Ratio | 1M $V_{HF}$ $(\mu L)$ | $V_{H_2O}$ $(\mu L)$ | Volume of gold solution $(\mu L)$ |
|---|---|---|---|---|
| 50/100/150 nm | 1:10 | 500 | 4500 | 500 |
| | 1:20 | 500 | 4750 | 250 |
| | 1:50 | 500 | 11750 | 250 |

## 5. List of Parameters and Symbols

N: the number of spins in the detection volume

$\mu_N$: the magnetic moment of the nucleus of interest

G: magnetic field gradient at the position of the sample

$S_F$: the force noise spectral density

B: the bandwidth of the measurement

$k_B$: Boltzmann constant

Γ: the total cantilever dissipation

$\Gamma_0$: the intrinsic cantilever dissipation

T: temperature