Indium Thin Films in Multilayer Superconducting Quantum Circuits

by

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This thesis consists of material all of which I authored or co-authored: see Statement of Contributions included in the thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Corey Rae McRae designed the devices for this project.

Thomas McConkey and Corey Rae McRae performed device simulations.

Corey Rae McRae developed the device fabrication processes.

Carolyn Earnest and Corey Rae McRae fabricated the devices.

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Matteo Mariantoni and Corey Rae McRae wrote the first draft of the manuscript.

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Corey Rae McRae developed the device fabrication processes.

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Carolyn Earnest and Corey Rae McRae fabricated the devices.

Jérémy Béjanin, Thomas McConkey, John Rinehart, and Matteo Mariantoni performed measurement set-up and calibration.

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Abstract

The superconducting quantum computer is an implementation of the quantum computer and a current leader the field in terms of performance and potential for scalability to large systems. Its two main components are the superconducting microwave resonator and the quantum bit (qubit). In Chapter 1, the concept of quantum computing is introduced, and the superconducting microwave resonator is explained in depth, along with a glimpse at the qubit and a description of two level system loss, the most prominent form of loss in low-power superconducting quantum circuits.

Scalability is essential to the development of fault-tolerant quantum computing, as error correction requires a large array of quantum bits. The multilayer quantum circuit architecture is rising to the forefront as a solution to many of the scalability issues facing the field today. Chapter 2 summarizes some of these scalability issues, such as the suppression of unwanted modes and materials losses, and presents an overview of multilayer architectures applied to superconducting quantum circuits. The chapter further delves into indium bump bonding, an essential technique in multilayer circuit fabrication.

In Chapter 3, we experimentally demonstrate a thermocompression bonding technology between on-chip indium thin films and apply it to capped superconducting devices. These devices can be used as a building block towards a more scalable architecture: the multilayer quantum circuit. We characterize the dc and microwave performance of these bonded devices at room temperature as well as cryogenic temperatures. At 10 mK, we find a small but significant dc bond resistance of 49.2 $\mu\Omega\,\mathrm{cm}^2$. A tunnel-capped, bonded device shows minimal microwave reflections and clean transmission up to 6.8 GHz compared to a similar uncapped device, demonstrating good performance. As a proof of concept, we fabricate and measure a set of tunnel-capped superconducting resonators, demonstrating marginal deterioration in resonator performance due to the bonding procedure. This work demonstrates that thermocompression bonding between thin on-chip indium films is a useful addition to the multilayer quantum circuit toolbox, and that this technique, when applied to form the tunnel-capped superconducting device, shows a promising step towards more scalable architectures.

Indium is becoming ubiquitous in superconducting microwave circuits as it continues to be widely adopted as a bonding medium. However, the loss mechanisms in superconducting indium films have not been examined until now. In Chapter 4, we characterize microwave loss in indium and aluminium/indium thin films on silicon substrates by measuring superconducting coplanar waveguide resonators and estimating the main loss parameters at powers down to the sub-photon regime and at temperatures between 10 and 450 mK. We

compare films deposited by thermal evaporation, sputtering, and molecular beam epitaxy. We study the effects of heating in vacuum and ambient atmospheric pressure as well as the effects of pre-deposition wafer cleaning using hydrofluoric acid. The microwave measurements are supported by thin film metrology including secondary-ion mass spectrometry. For thermally evaporated and sputtered films, we find that two-level states (TLSs) are the dominating loss mechanism at low photon number and temperature. Thermally evaporated indium is determined to have a TLS loss tangent due to indium oxide of $\sim 5 \times 10^{-5}$. The molecular beam epitaxial films show evidence of formation of a substantial indium-silicon eutectic layer, which leads to a drastic degradation in resonator performance.

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Dedication

This work is dedicated to my brand new husband Mike and our brand new dog Gina.

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Chapter 1

Introduction

The classical computer has altered the way humans live in almost every aspect, from medical breakthroughs to social media to agriculture and manufacturing. Many of the contexts in which classical computers are used today were inconceivable to people living in the pre-digital world. It would have been impossible to predict all of the ways in which computers would become embedded into the world around us. Similarly, it is difficult to envision a world in which quantum computers[1] are ubiquitous. Currently, quantum computing is changing the way we face cryptography [2] and shows promise as a simulation tool in molecular chemistry [3] and machine learning [4]. If history is any indication, the full impact of the field of quantum computing will not be uncovered until long after the quantum computer becomes a reality.

The quantum computer is composed of a set of qubits. Each qubit can be in state $|0\rangle$, state $|1\rangle$, or a linear combination of these two states, $\alpha|0\rangle+\beta|1\rangle$ where α and β are complex values. Qubits can be initialized to the $|0\rangle$ or $|1\rangle$ state, can interact with themselves and one another through quantum gates, and can be measured, giving a classical output of 0 or 1. A measurement of the state $\alpha|0\rangle + \beta|1\rangle$ will give 0 with probability $|\alpha|^2$ and 1 with probability $|\beta|^2$.

A variety of quantum computer implementations are currently being considered and researched in depth. Types of physical realizations include [5] :

- Trapped atoms, where qubits consisting of isolated ions are manipulated using lasers;
- Quantum dots, where qubits consist of a single electron or hole isolated by impurities in a semiconductor, and control is achieved using microwave fields;

[1] Computers which use quantum bits (qubits) rather than classical bits to perform computations.

- Nuclear magnetic resonance (NMR), where qubits are defined as the nuclear spin of elements in a large molecule and subjected to a magnetic field, and gates are performed using radio-frequency (RF) pulses;
- Optical quantum computing, where individual photons act as qubits and manipulation is performed on an optical table;
- And superconducting quantum computing, where qubits are composed of a combination of LC circuits and nonlinear quantum oscillators called Josephson junctions and are controlled by microwave pulses.

In this thesis, we delve into the superconducting quantum computing realization of the quantum computer. This area is a leader in the field of quantum computing with high qubit coherence times, good control and measurement, and the promise of an implementable quantum error correction algorithm, the surface code [6, 7]. Architectures based on superconducting qubits are improving rapidly, and are approaching the realm of higher performance over the leading classical supercomputer [8].

In practice, the superconducting quantum circuit is a set of on-chip devices that are controlled using low power RF pulses and operated at temperatures near 10 mK. These circuits are made up of three major components: the transmission line, the resonator, and the qubit.

Qubits are the source of the quantum information, and are connected to input and output electronics through transmission lines and resonators. The experiments in this work are performed using superconducting quantum circuits with transmission lines and resonators only. Transmission lines act as a wire to propagate the microwave signal from one location to another, while resonators hold a signal of a specific frequency depending on their length and can couple to other devices to pass this signal along.

Resonators are a convenient tool to measure the performance of a circuit due to its material make-up or the processing it has undergone. The performance of an individual resonator is measured by its internal quality factor, Q_i. Q_i can be determined by fitting to the transmission of the resonator as a function of microwave frequency. By performing these fits at a variety of temperatures and powers, information can be determined about loss mechanisms within the circuit.

The upcoming sections in this chapter will introduce the resonator and the qubit as elements in the superconducting quantum circuit, and explain the concept of the nebulous two-level system and its effect on superconducting circuit performance.

1.1 The resonator

Superconducting microwave resonators are an essential part of the superconducting quantum circuit architecture. They are used as buses between qubits, short-term storage, and circuit control and readout. The most common type of resonator in superconducting circuits is the coplanar waveguide (CPW) resonator, which consists of a single surface supporting a centre conductor with ground planes on either side and dielectric below (see Sec. 1.1.5 for more details on the CPW).

Resonators can be designed in a lumped element circuit model (consisting of discrete capacitive, inductive and resistive components) or a distributed element model (consisting of a length of circuit with a capacitance, inductance and resistance per unit length) [9, 10]. We begin by examining the simpler lumped element model and use it to develop an intuition for the quality factor. Then we move to the distributed element model, which characterizes the CPW. We briefly introduce the concept of modes, as well as the quantization of the resonator circuit model. Finally, we explore CPW behaviour in detail [11].

1.1.1 The lumped element circuit

Many concepts crucial to the superconducting CPW resonator are shared with the lumped element circuit. Thus, we can build an intuition for the superconducting microwave resonator by exploring the behaviour of the lumped element circuit. In this section, two critical variables used to characterize a resonator are introduced: the resonant frequency and the quality factor. The Lorentzian behaviour of the resonator is also examined. This section is based on the treatment of the lumped element resonant circuit in Collin [9] and Mariantoni [10].

A circuit with resistive, inductive, and capacitive elements (an RLC circuit) can have connections in series or in parallel. The input impedance of a series RLC circuit (Fig. 1.1 (a)) is

$$Z_{in} = R + j(\omega L - \frac{1}{\omega C}) \tag{1.1}$$

where R is the resistance, L is the inductance, C is the capacitance, ω is the angular frequency, and $j = \sqrt{-1}$.

Z_{in} is exclusively real when the frequency is such that the imaginary component is zero, i.e.

$$\omega_0 = \frac{1}{\sqrt{LC}}. \tag{1.2}$$

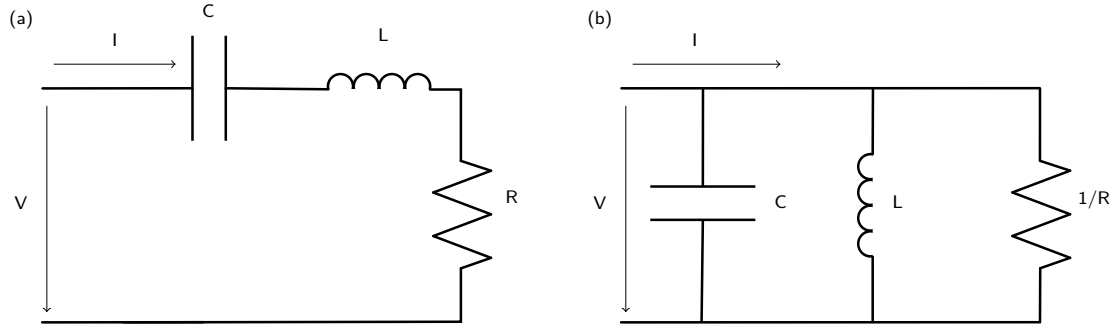

Figure 1.1: A series (a) and parallel (b) lumped element RLC circuit with capacitance C, inductance L, resistance R, voltage V and input current I.

This is the resonant frequency of the circuit. We can determine the time-averaged energies stored in the electric and magnetic field (i.e. in the capacitor and inductor) as

$$W_C = \frac{1}{4} C V_C^* V_C \tag{1.3}$$

$$W_L = \frac{1}{4} L I^* I \tag{1.4}$$

where I is the input current and V_C is the voltage across the capacitor. The total time-averaged energy of the system is $W = W_C + W_L$. By rewriting the input impedance in terms of W_C and W_L, it becomes evident that to achieve a real input impedance and circuit resonance, we must have $W_C = W_L$. Thus, at resonance, the time-averaged energy is shared equally between the capacitor and the inductor.

When considering resonant circuits, the quality factor Q becomes an important concept. Q indicates circuit performance and takes into account loss within the circuit. Broadly, we define

$$Q = \frac{2\pi\omega W}{P_R} \tag{1.5}$$

where

$$P_R = \frac{1}{2} R I^* I \tag{1.6}$$

is the power loss due to the resistor. Thus, in general terms, the quality factor describes the energy loss ratio of the system.

The quality factor for a series RLC resonator reduces to

$$Q^s = \frac{2\pi}{\omega RC} = \frac{2\pi\omega L}{R} \tag{1.7}$$

by substituting the average energy $W = W_C + W_L = 2W_C = 2W_L = \frac{1}{2}LI^*I$.

For frequencies close to resonance, $\omega = \omega_0 + \Delta\omega$ we can approximate $1/\omega \simeq (1 - \Delta\omega/\omega_0)/\omega 0$ which, when substituted, gives

$$Z_{in} = R + j(\omega_0 + \Delta\omega)L - j\frac{1 - \Delta\omega/\omega_0}{\omega_0 C}. \tag{1.8}$$

In terms of the quality factor and relative frequency shift, we can say

$$Z_{in} = \frac{1}{R}\left(1 + j2\frac{Q^s}{2\pi}\left(\frac{\Delta\omega}{\omega_0}\right)\right). \tag{1.9}$$

The inverse of the input impedance is called the input admittance, $Y_{in} = Z_{in}^{-1}$. For a series RLC circuit, Y_{in} is a complex Lorentzian function that illustrates typical resonance behaviour. The magnitude of Y_{in} is

$$|Y_{in}| = \frac{1}{R\sqrt{1 + 4(\frac{Q^s}{2\pi})^2(\frac{\Delta\omega}{\omega_0})^2}} \tag{1.10}$$

and its phase is

$$\angle Y_{in} = \arctan\left(-2\frac{Q^s}{2\pi}\left(\frac{\Delta\omega}{\omega_0}\right)\right). \tag{1.11}$$

$\angle Y_{in}$ and the normalized version of the magnitude, $|Y_{in}|/G^s$, where $G^s = 1/R$ is the conductance, are plotted in Fig. 1.2. We expect a similar response from superconducting microwave resonator measurements, as explained in Sec. 1.1.2.

By rearranging (1.9) and substituting $Q^s/2\pi = 1/R\omega_0 C$, we can obtain

$$Z_{in} = R + j2L\Delta\omega. \tag{1.12}$$

We can also define the quality factor in terms of its 3 dB bandwidth, $\kappa = \omega_2 - \omega_1$, where ω_1 and ω_2 are frequencies at which $|Y_{in}|/G^s$ is 3 dB lower than its peak value. Then:

$$Q^s = \frac{\omega_0}{\kappa}. \tag{1.13}$$

A similar derivation to the above can be shown for parallel RLC circuits. In contrast to (1.9),

$$Z_{in} = \frac{R}{1 + j2\frac{Q^p}{2\pi}(\frac{\Delta\omega}{\omega_0})} \tag{1.14}$$

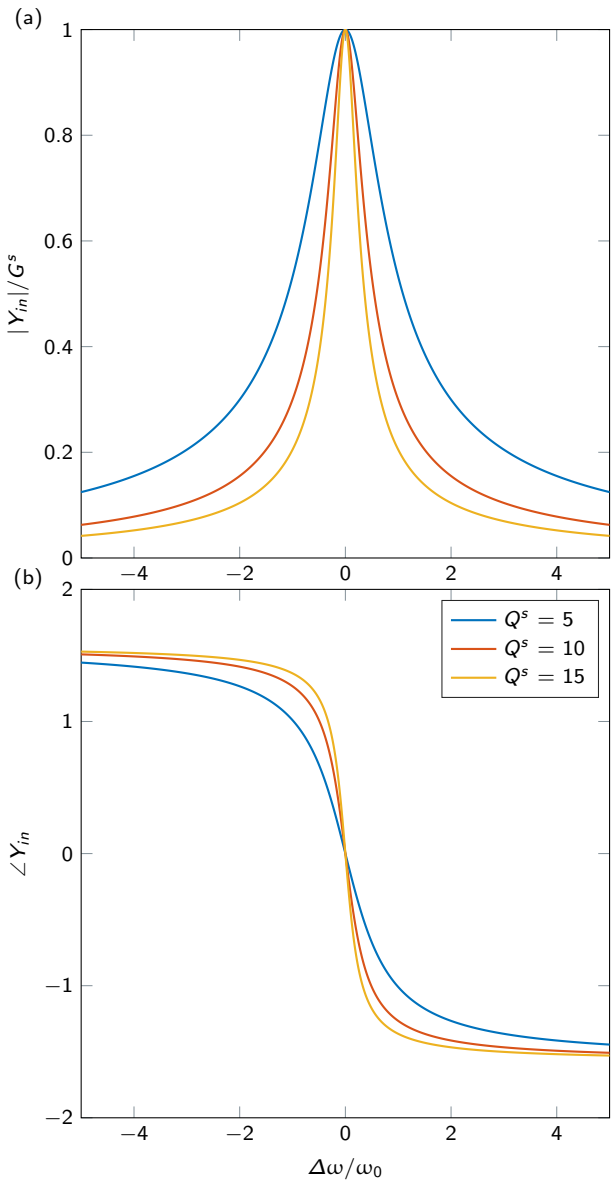

Figure 1.2: Normalized magnitude $|Y_{in}|/G^s$ (a), and phase $\angle Y_{in}$ (b), of the complex Lorentzian function laid out in (1.10) and (1.11) for increasing values of the quality factor Q^s. The magnitude of the Lorentzian curve peaks at the resonant frequency ω_0. This peak becomes sharper as Q_s increases, and the drop in phase near ω_0 becomes steeper.

for a parallel RLC circuit.

The quality factor can be broken down into components based on the source of loss that is represented in R. The internal quality factor, Q_i, is composed of loss within the circuit. This is the value we have been referring to in this chapter when using the general term *quality factor*. The coupled quality factor, Q_c, is added to the mix when the circuit is influenced by the presence of an external load resistor in series, which can represent coupling of the device to other systems such as an on-chip transmission line. The loaded quality factor, Q_l, takes into account both of these sources of loss, as:

$$\frac{1}{Q_l} = \frac{1}{Q_c} + \frac{1}{Q_i}. \tag{1.15}$$

1.1.2 The distributed element circuit

The distributed element circuit is defined by values of resistance, inductance and capacitance which are spread throughout the circuit rather than located at discrete points within it. In this section, we lay out the distributed element circuit model and explore the effect of various line terminations. We demonstrate how a shorted and an open distributed element circuit can be approximated to a series RLC lumped element circuit, confirming the validity of the simpler lumped model applied to a CPW. This introduction to distributed element circuits is based on information found in Collin [9] and Mariantoni [10].

To accurately study the transmission line, we must take into account that its capacitance, inductance and resistance is not concentrated at a single point but rather distributed over a length of material. Distributed element devices tend to be less lossy than their lumped counterparts, and are therefore more commonly used in superconducting quantum circuits [10].

A transmission line of length $z = \ell$ can be modeled as two wires, one conductor and one ground, separated by a length of dielectric and terminated at each end by load resistance Z_L (Fig. 1.3). For infinitesimal segment dz, the conductor has input current $I(z)$, output current $I(z+dz)$, and series inductance and resistance ldz and rdz. It also has a capacitance to ground cdz, parallel conductance gdz, and input and output voltages $V(z)$ and $V(z+dz)$. The line's characteristic impedance

$$Z_0 = \sqrt{l/c}, \tag{1.16}$$

attenuation constant

$$\alpha = \frac{1}{2}\left(r\frac{1}{Z_0} + gZ_0\right) \tag{1.17}$$

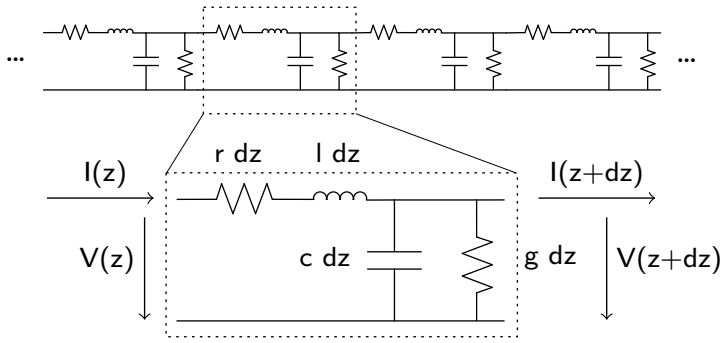

Figure 1.3: Distributed element circuit showing an expanded version of infinitesimal segment dz. Each segment has input current $I(z)$, output current $I(z+dz)$, series inductance ldz, series resistance rdz, capacitance to ground cdz, parallel conductance gdz, and input and output voltages $V(z)$ and $V(z+dz)$.

and propagation phase constant

$$\beta = \frac{\omega}{c_0} \approx \omega\sqrt{lc} \tag{1.18}$$

are used to characterize the properties of the line. Note that we assume nondispersivity[2] and low loss through the line.

For now we will assume negligible dielectric losses since dielectric materials common in superconducting quantum circuits are low loss.[3] In that case, $g = 0$ and

$$\alpha = r/2Z_0. \tag{1.19}$$

The input impedance of the line Z_{in} is affected by the terminating element Z_L as:

$$Z_{in} = Z_0 \frac{Z_L + Z_0 \tanh j\beta\ell + \alpha\ell}{Z_0 + Z_L \tanh j\beta\ell + \alpha\ell}. \tag{1.20}$$

This relationship is known as the transformation of impedances. We can use it to show the equivalence in behaviour between short-circuited transmission lines and series resonating circuits, and between open-circuited transmission lines and parallel resonating circuits.

[2] On nondispersive lines, signal speed is independent of frequency.

[3] Common dielectric materials used as substrates in superconducting quantum computing include silicon, with a low temperature loss tangent of less than 12×10^{-6} and sapphire with a loss tangent of less than 10×10^{-6} [12].

A short circuited transmission line has $Z_L = 0$ and thus the transformation of impedances reduces to $Z_{in} = Z_0 \tanh(j\beta\ell + \alpha\ell)$. Applying tanh identities,

$$Z_{in} = \frac{\tanh \alpha\ell + j \tan \beta\ell}{1 + j \tanh \beta\ell \tan \alpha\ell} \tag{1.21}$$

Shorted transmission line resonators are also called $\lambda/2$ resonators due to the fact that they support a resonance at the frequency for which the length of the line is $\ell = \lambda_0/2$, where $\lambda_0 = c_0/f_0 = 2\pi c_0/\omega_0$ is the resonant wavelength of the line.[4] We can confirm this behaviour by substituting $\ell = \lambda_0/2$ into (1.21) above. Assuming small deviations around ω_0[5] and low loss,[6] we eventually obtain

$$Z_{in} = \frac{1}{2} r\ell + jl\ell\Delta\omega \tag{1.22}$$

which is identical to (1.9) for a series resonant circuit.

We can determine a function for the quality factor in terms of transmission line parameters by substituting (1.19) and (1.18) into (1.7), noting that $L = l\ell$ and $R = r\ell$. Then:

$$Q^s = \frac{\beta}{2\alpha}. \tag{1.23}$$

Here, the quality factor is the ratio between propagation and attenuation. If we can determine the values of α and β for a transmission line, regardless of geometry, we can determine the internal quality factor.

A similar derivation can be performed for an open circuited transmission line, where $1/Z_L = 0$. We call these lines $\lambda/4$ resonators, and when substituting $\ell = \lambda_0/4$, the transformation of impedances reduces to

$$Z_{in} = \frac{1}{2} r\ell + jl\ell\Delta\omega \tag{1.24}$$

which is identical to the case of the short circuited $\lambda/2$ line.

[4] c_0 is the speed of light in the line material.

[5] If we assume small deviations $\Delta\omega$ around ω_0 so that $\omega = \Delta\omega + \omega_0$, we can say $\beta\ell = \ell\omega/c_0 = (\ell/c_0)(\omega_0 + \Delta\omega) = \pi(1 + \Delta\omega/\omega_0)$.

[6] For small losses, we can assume $\alpha\ell \ll 1$, so $\tanh(\alpha\ell) \approx \alpha\ell$. For small losses and small deviations from ω_0, $\tan\beta\ell \approx \pi\Delta\omega/\omega$.

1.1.3 Modes

In this section, we build an understanding of multimode systems so we can apply it to the CPW resonator. This section is based on the treatment of modes in Collin [9] and Mariantoni [10].

A resonant line sustains a set of sinusoidal standing waves whose node and antinode locations[7] are determined by its terminating elements. These sets of standing waves, or *modes*, are comprised of frequencies

$$f_{m-1} = mf_0, \tag{1.25}$$

$$m = 1, 2, 3, ...$$

for $\lambda/2$ lines, and

$$f_m = (2m + 1)f_0, \tag{1.26}$$

$$m = 0, 1, 2, ...$$

for $\lambda/4$ lines, where $f_0 = c_0/\lambda_0$ is the fundamental resonant frequency.

Lumped element resonators sustain only a single mode, whereas distributed element resonators sustain sets of modes.

Transmission lines often support modes that have some missing electric or magnetic field components. Transverse electromagnetic (TEM) modes have $E_z = H_z = 0$, whereas transverse electric and transverse magnetic modes have simply $E_z = 0$ and $H_z = 0$, respectively. These vanishing components simplify the associated Maxwell's equations and allow us to solve for electric and magnetic field propagation equations [9]. CPWs can be said to sustain quasi-TEM modes, which can be approximated as TEM modes in order to garner greater understanding of CPW behaviour [11].

1.1.4 Resonator quantization

Thus far, we have only considered classical resonators as models for the superconducting microwave resonator. In order to fully understand these devices, we must describe them

[7] A node is a position where the standing wave is stationary, i.e., $\sin \beta z = 0$. Conversely, an antinode is a position where the wave amplitude is at its maximum. Nodes and antinodes are useful tools in superconducting quantum computing, as they can be used to minimize or maximize the coupling between neighbouring devices.

using quantum concepts such as the quantum mechanical Hamiltonian. This section is based on the treatment of resonator quantization in Mariantoni [10].

The Hamiltonian for a lossless resonator, modeled as a lumped LC circuit, is

$$\hat{H} = \frac{1}{2}C\hat{V}^2 + \frac{1}{2}L\hat{I}^2 \tag{1.27}$$
$$= \frac{\hat{Q}^2}{2C} + \frac{\hat{\Phi}^2}{2L}$$

with charge on the capacitor $\hat{Q} = C\hat{V}$ and inductor flux $\hat{\Phi} = L\hat{I}$. In analogy to the momentum and position operators, the two observables follow the commutation relation

$$[\hat{Q}, \hat{\Phi}] = j\hbar. \tag{1.28}$$

If we define lowering and raising operators $\hat{a}$ and $\hat{a}^\dagger$ in terms of $\hat{Q}$ and $\hat{\Phi}$ as in

$$\hat{a} = \frac{1}{\sqrt{2C\hbar\omega}}(\hat{Q} + jC\omega\hat{\Phi}) \tag{1.29}$$

and

$$\hat{a}^\dagger = \frac{1}{\sqrt{2C\hbar\omega}}(\hat{Q} - jC\omega\hat{\Phi}) \tag{1.30}$$

with commutation relation $[\hat{a}, \hat{a}^\dagger] = 1$, we can rewrite (1.27) as

$$\hat{H}_{LC} = \hbar\omega(\hat{a}^\dagger\hat{a} + \frac{1}{2}) \tag{1.31}$$

which is the Hamiltonian for a one-dimensional quantum harmonic oscillator (QHO). Thus we have shown the transformation from LC resonant circuit to QHO.

The resonator eigenvalue n and eigenket $|n\rangle$ can be determined using

$$\hat{N}\,|n\rangle = \hat{a}^\dagger\hat{a}\,|n\rangle = n\,|n\rangle \tag{1.32}$$

since lowering operator

$$\hat{a}\,|n\rangle = \sqrt{n}\,|n-1\rangle \tag{1.33}$$

and raising operator

$$\hat{a}^\dagger = \sqrt{n+1}\,|n+1\rangle\,. \tag{1.34}$$

The energy levels can be found by

$$E_n = (n + \frac{1}{2})\hbar\omega \tag{1.35}$$

$$n = 0, 1, 2, ...$$

Unlike a classical resonator, the QHO has nonzero energy $E_0 = \hbar\omega/2$ in its ground state.

Each mode behaves as a QHO. For a $\lambda/2$ resonator,

$$\hat{H}_{\lambda/2} = \sum_{m=1}^{\infty} \hbar\omega_m(\hat{a}_m^\dagger \hat{a}_m + \frac{1}{2}) \tag{1.36}$$

$$m = 1, 2, 3, ...$$

where $\omega_m = m\omega_0$ is the frequency of mode m, and $\hat{a}_m^\dagger$ and $\hat{a}_m$ are the raising and lowering operators for mode m.

1.1.5 The coplanar waveguide

In this section, we will explore analytical descriptions of the characteristic impedance Z_0 and effective permittivity ϵ_{eff} of the CPW. These parameters are geometry-dependent and must be accounted for during device design. It is often important to design transmission lines to be $50\,\Omega$ matched, i.e. $Z_0 = 50\,\Omega$, as external wiring usually has the same impedance and reflections can result from impedance mismatches, leading to loss. Effective permittivity affects the internal quality factor of the device, and should be taken into account (see Chapter 3 for more details). This section is based on the sources of Simons [11] and Mohebbi [13].

The standard CPW

The standard coplanar waveguide (CPW) consists of a metallic thin film separated into centre conductor and ground planes on either side, all of which sits on top of a dielectric substrate (Fig. 1.4 (a)). As stated in Sec. 1.1.3, CPWs sustain quasi-TEM modes. These devices are simple to fabricate and have low radiation loss compared to other waveguides [11].

Using conformal mapping[8], we can determine formulae for the characteristic impedance Z_0 and effective dielectric constant ϵ_{eff} for a standard CPW. For a CPW [Fig. 1.4 (a)] made

[8] Conformal mapping is the mapping of one set of variables to another while preserving local angles. The CPW boundaries for the Laplace equation can be mapped to a set of boundaries where a solution is more easily found. Refer to Appendix III: Conformal Mapping Techniques in Simons [11] for more information.

of an infinitely thin superconductor with gap width w and conductor width s on a dielectric of some finite thickness h with dielectric constant ϵ_{rd}, [11]

$$\epsilon_{eff} = 1 + \frac{(\epsilon_{rd} - 1)}{2} \frac{K(k_1)}{K(k_1')} \frac{K(k_0')}{K(k_0)} \tag{1.37}$$

and

$$Z_0 = \frac{30\pi}{\sqrt{\epsilon_{eff}}} \frac{K(k_0')}{K(k_0)} \tag{1.38}$$

where $K(k_n)$ are complete elliptic integrals of the second kind[9] with inputs

$$k_0 = \frac{s}{s + 2w}, \tag{1.39}$$

which is the CPW aspect ratio, and

$$k_0' = \sqrt{1 - k_0^2} \tag{1.40}$$

$$k_1 = \frac{\sinh\left(\frac{\pi s}{4h}\right)}{\sinh\left(\frac{\pi(s + 2w)}{4h}\right)} \tag{1.41}$$

$$k_1' = \sqrt{1 - k_1^2}. \tag{1.42}$$

Assuming a substrate of infinite thickness, (1.37) and (1.38) become

$$\epsilon_{eff} = \frac{1 + \epsilon_{rd}}{2} \tag{1.43}$$

$$Z_0 = \frac{30\pi}{\sqrt{(\epsilon_{eff} + 1)/2}} \frac{K(k_0')}{K(k_0)}. \tag{1.44}$$

When $h < 2w$, there is a 10% - 15% error when using the assumption of infinite thickness. For the case of standard superconducting quantum circuits such as the ones used in this thesis, $h \simeq 500$um and $w \simeq 10$um, so we are free to use either set of equations.

[9] Complete elliptic integrals of the second kind can be expressed as an integral or as a power series, $K(k) = \frac{\pi}{2} \sum_{n=0}^{\infty} (P_{2n}(0))^2 k^{2n}$ where P_n are Legendre polynomials.

We can also use more accurate expressions which takes into account the superconductivity, and thus the surface impedance, of a CPW with superconducting thin film [13]. These expressions are

$$\sqrt{\epsilon^t_{ref}(f)} = \sqrt{\epsilon^t_{ref}(0)} + \frac{\sqrt{\epsilon_{rd}} - \sqrt{\epsilon^t_{ref}(0)}}{1 + g(f/f_{TE})^{-1.8}} \tag{1.45}$$

and

$$Z_0 = \frac{30\pi}{\sqrt{\epsilon^t_{ref}}} \frac{K(k'_0)}{K(k_0)} \tag{1.46}$$

where

$$\epsilon^t_{ref}(0) = \epsilon_{ref}(0) - \frac{0.7(\epsilon_{ref}(0) - 1)(t/w)}{\frac{K(k_0)}{K'(k_0)} + 0.7(t/w)} \tag{1.47}$$

$$\epsilon_{ref}(0) = 1 + q(\epsilon_{rd} - 1) \tag{1.48}$$

$$q = \frac{1}{2} \frac{K(k_1)K(k'_0)}{K(k'_1)K(k_0)}. \tag{1.49}$$

and

$$g = e^{u \ln(s/w) + v} \tag{1.50}$$

$$f_{TE} = \frac{c_0}{4h\sqrt{\epsilon_{rd} - 1}} \tag{1.51}$$

$$u = 0.54 - 0.64p - 0.015p^2 \tag{1.52}$$

$$v = 0.43 - 0.86p + 0.54p^2 \tag{1.53}$$

$$p = \ln \frac{s}{h} \tag{1.54}$$

where c_0 is the speed of light, f is the frequency, and t is the superconducting film thickness.

The capped CPW

Adding a cap to a CPW can suppress loss by shielding it from the environment. We can model the capped coplanar waveguide (described in Chapter 3) as a CPW with a second dielectric above the CPW (air) and a third ground plane above that (Fig. 1.4 (b)). The general form of this device is called a grounded CPW (GCPW). Simons [11] refers to this

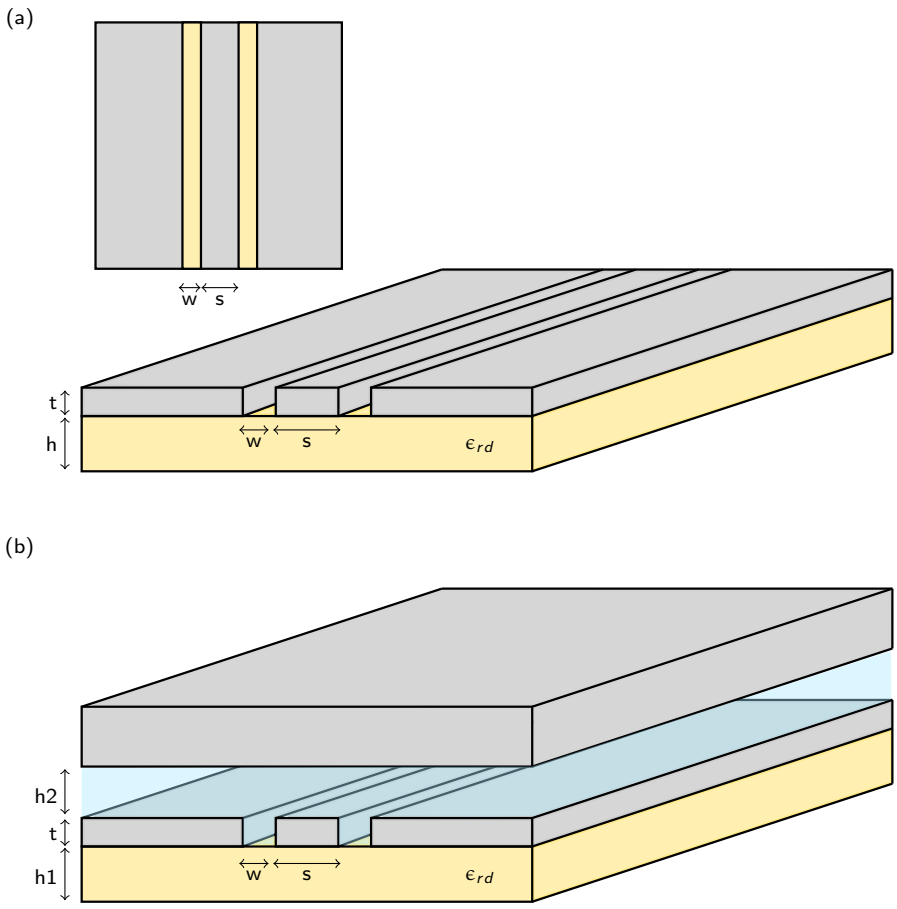

Figure 1.4: Diagram of standard CPW (a) with top and orthographic views and GCPW (b) with orthographic view. The substrate (yellow) is of thickness h (h_1) and dielectric constant ϵ_{rd}. The metal (grey) has thickness t and is patterned with gaps of width w and a conductor of width s. The GCPW also has a ground a height h_2 above the device.

device as a "conventional coplanar waveguide on a finite thickness dielectric substrate and with a top metal cover". Dielectric permittivity and characteristic impedance are given as

$$\epsilon_{eff} = 1 + q_3(\epsilon_{rd} - 1) \tag{1.55}$$

and

$$Z_0 = \frac{60\pi}{\sqrt{\epsilon_{eff}}} \frac{1}{\frac{K(k_0)}{K(k_0')} + \frac{K(k_4)}{K(k_4')}} \tag{1.56}$$

where

$$q_3 = \frac{\frac{K(k_1)}{K_{k_1'}}}{\frac{K(k_0)}{K(k_0')} + \frac{K(k_4)}{K(k_4')}} \tag{1.57}$$

$$k_4 = \frac{\tanh\left(\pi s/4h_2\right)}{\tanh\left(\frac{\pi(s+2w)}{4h_2}\right)} \tag{1.58}$$

$$k_4' = \sqrt{1 - k_4^2} \tag{1.59}$$

where h_2 is the height of the cap.

1.2 The qubit

The superconducting qubit is a circuit that consists of the combination of a resonator and a nonlinear inductive element, the Josephson junction. Adding a nonlinear element to a resonator changes its energy levels so that they are non-uniformly distributed, thereby allowing energy gaps to be addressed individually.

The Josephson junction, or Josephson tunnel junction, is the combination of two superconducting leads weakly connected by a constriction, a normal metal, or a thin insulator [14]. In superconducting quantum computing, the connection is most commonly formed from an insulator such as aluminium oxide.

The Josephson junction has a critical current I_{c0} which is the maximum dc current that can be supported by the junction. Within those bounds, the supercurrent I_s can be found by

$$I_s = I_{c0} \sin \Delta\varphi \tag{1.60}$$

where $\Delta\varphi$ is the superconducting wave function's phase difference across the junction. Above the critical current,

$$\frac{d}{dt}\Delta\varphi = \frac{2e}{\hbar}V \tag{1.61}$$

where V is the voltage drop across the junction.

We can use these relationships to show that the Hamiltonian for a qubit is

$$\hat{H} = \frac{\hat{Q}^2}{2C} + \frac{\hat{\Phi}^2}{2L} - E_J \cos\Phi \tag{1.62}$$

where the first two terms are due to the resonator (Sec. 1.1.4) and the last term is due to the Josephson junction.

1.3 Two level system loss

Superconducting quantum devices inevitably contain some amount of amorphous dielectric material. Common materials include native oxide (such as silicon, aluminium or indium surface oxide) and grown oxide (such as aluminium oxide grown to form a Josephson junction). At temperatures $T < 1$K, [15] these materials cause loss which can be modeled as two level system (TLS) loss. TLSs absorb photons and phonons from a superconducting device via electric field coupling and then spontaneously re-emit them. At high temperatures or high powers, these systems become saturated due to excess energy in the system, and therefore do not cause much loss[10]. However, at low powers, the interaction is quite significant. TLS loss is largely the limiting form of loss in superconducting quantum circuits at low temperature, [16] and by understanding TLS loss we can improve the performance of these circuits. TLS loss varies depending on the materials present, so modeling TLS loss is a method of characterizing materials in terms of their superconducting microwave performance.

We can determine the TLS component of loss for a superconducting CPW resonator by comparing its resonant frequency's temperature dependence or its loss tangent's power dependence to the same dependences for the TLS model. Below, the TLS model is looked at in greater depth, and the two dependences are derived, following the primary sources of Anderson [17] and Phillips [15, 18] and the secondary sources of Gao [19] and Pappas [20].

Amorphous materials have been theorized to contain atoms or atomic clusters that tunnel between pairs of locations, acting as a particle in an asymmetric double well potential

[10] Saturation of TLSs occurs when the rate of TLS excitation is greater than the rate of emission.

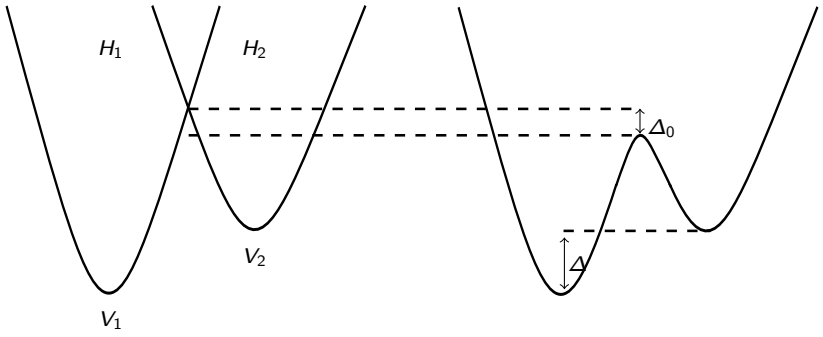

Figure 1.5: Potential energy diagram for a double well potential, showing each potential separately (left) and as a single merged potential (right). The wells have Hamiltonians H_1 and H_2, minimum potentials V_1 and V_2, asymmetry energy Δ, and tunneling matrix element Δ_0.

(Fig. 1.5). Under applied electric field $\vec{E} = E\hat{e}$, the double well potential has electric dipole moment $\vec{D} = d\hat{d}$ which characterizes its ability to couple to external photons. TLSs also have an elastic dipole moment which couples to the strain field of the system and allows phonon coupling.

Each of these double well potentials has a distinct asymmetry energy Δ (energy difference between the two potential wells) and tunneling matrix element Δ_0 (change in energy due to tunneling). These values are produced via the random structure of the amorphous material and are therefore part of a broad distribution. Commonly, Δ is assumed to have a uniform distribution and Δ_0 a logarithmic distribution. An in-depth discussion on the distribution of these variables can be found in Phillips [15].

1.3.1 The two level system Hamiltonian

For two single well potentials with Hamiltonians H_1 and H_2 and minimum potentials V_1 and V_2, the Hamiltonian of the double well potential is $H = H_1 + (V - V_1) = H_2 + (V - V_2)$ or, in a simplified matrix form,

$$H = \frac{1}{2}\begin{bmatrix} -\Delta & \Delta_0 \\ \Delta_0 & \Delta \end{bmatrix} \tag{1.63}$$

for the local basis consisting of ground states of the single well problems, ϕ_1 and ϕ_2. Defining $\theta = \frac{1}{2}\arctan\frac{\Delta_0}{\Delta}$, eigenstates are

$$\psi_1 = \phi_1 \cos\theta + \phi_2 \sin\theta \tag{1.64}$$

$$\psi_2 = \phi_1 \sin\theta - \phi_2 \cos\theta \tag{1.65}$$

with eigenenergies $\pm E/2$ where $E = \sqrt{\Delta^2 + \Delta_0^2}$. Diagonalizing the Hamiltonian with basis states ψ_1 and ψ_2, we obtain the usual two level system Hamiltonian,

$$H_0 = \frac{1}{2} E \sigma_z = \frac{1}{2} E \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix} \tag{1.66}$$

where σ_z is the Pauli z matrix. The interaction Hamiltonian with both an electric and strain field is

$$H_{int} = (\frac{\Delta}{E}\sigma_z + \frac{\Delta_0}{E}\sigma_x)\vec{d_0} \cdot \vec{E} \tag{1.67}$$

where $\vec{d_0}$ is the maximum dipole moment and $\vec{E}$ is the electric field. For a more detailed treatment of the two level system Hamiltonian, see Gao [19].

1.3.2 Dielectric contribution of TLSs

The TLS model's power v.s. loss and resonant frequency v.s. temperature relationships can be found through the TLS dielectric contribution term

$$\epsilon_{TLS}(\omega) = \int\int\int [\hat{e} \cdot \vec{\vec{\chi}}_{res}(\omega) \cdot \hat{e}] \frac{P}{\Delta_0} d\Delta d\Delta_0 d\hat{d} \tag{1.68}$$

where P is the density of states and $\vec{\vec{\chi}}$ is the magnetic susceptibility. With a change of variables and by integrating, we can modify this into

$$\epsilon_{TLS}(\omega) = \frac{Pd^2}{3\hbar} \int_0^{E_{max}} \chi_{res}(\omega) d\omega \tag{1.69}$$

where $\chi_{res}(\omega) = \chi_{res}^A \chi_{res}^B \chi_{res}^C$, a product of three terms. The first term

$$\chi_{res}^A = \tanh \frac{E}{2kT} \tag{1.70}$$

takes into account the difference in probability between the ground and excited states. The term

$$\chi_{res}^B = \frac{1}{\omega_E - \omega + i/T_2} \tag{1.71}$$

is the TLS single-pole response under the rotating wave approximation (RWA), where T_2 is the phase decoherence lifetime. For energy relaxation lifetime T_1 and Rabi frequency $\Omega = 2\vec{D}\dot{(}\vec{E}/\hbar)$, the third term is

$$\chi_{res}^{C} = \frac{1 + (\omega_E - \omega)^2 T_2^2}{1 + \Omega^2 T_1 T_2 + (\omega_E - \omega)^2 T_2^2}. \tag{1.72}$$

This term takes into account TLS saturation. When fields are weak, which is the case at low powers used in superconducting quantum computing, $\Omega^2 T_1 T_2 << 1$, and $\chi_{res}^{C} \sim 1$.

Considering only the imaginary component of $\epsilon_{TLS} = \epsilon' - i\epsilon''$, we eventually arrive at

$$\tan\delta = F \tan\delta_0 \tanh \frac{\hbar\omega_0}{2k_B T}. \tag{1.73}$$

where k_B is the Boltzmann constant, F is the filling factor of the TLS material, and $\tan\delta_0$ is the component of the loss tangent due to TLSs at a temperature of absolute zero. Considering only the real component, we see

$$f_0(T) = f_{0,i}\left(1 + p\left(\mathrm{Re}\Psi\left(\frac{\hbar\omega_0}{2\pi i k_B T} + \frac{1}{2}\right) - \ln\frac{\hbar\omega_0}{k_B T}\right)\right). \tag{1.74}$$

where $f_{0,i}$ is the resonant frequency of the resonator at absolute zero, Ψ is the complex Digamma function, and $p = F\tan\delta_0/\pi$.

These two relations can be fitted to determine $\tan\delta_0$ and $f_{0,i}$ in measured superconducting microwave resonators. We do just this in Chapter 4 of this thesis.

Chapter 2

Moving towards extensibility and scalability

The components necessary for a quantum computer are outlined in the DiVincenzo criteria, [21] the first being

> "A scalable physical system with well characterised qubits."

In this thesis, scalability is used loosely to refer to the ability to increase the number of elements, connections, and computing power of a system. Currently, many challenges lie in the path of further scaling of superconducting quantum circuits. Box modes due to sample holders, as well as chip modes, limit chip size, and crosstalk and slotline modes become are exacerbated when chips are densely covered with devices. Further, we do not fully understand the causes of loss in these devices, making it difficult to optimize device performance.

In this chapter, we begin by introducing the issue of unwanted modes and coupling in extensible superconducting quantum circuits. Next, we examine multilayer superconducting quantum architectures which could act as a solution to unwanted modes and coupling and allow us to further scale the superconducting quantum circuit. Finally, we introduce the study of materials used in superconducting quantum circuits, especially indium, an essential component to the multilayer architecture.

2.1 Understanding and suppressing unwanted modes and coupling

Resonances within the 4-8 GHz working frequency region that were not purposefully designed can be referred to as *unwanted modes*. [1] Unwanted modes can interfere with computations and measurements of a superconducting circuit, and can lead to decoherence and radiation loss [22, 23]. These modes originate from many different sources, including the sample holder geometry (box modes) and resonator meandering or uneven ground planes (slotline modes). Interactions between neighbouring devices (crosstalk) can have similar consequences. Suppression of the above modes has been attempted in various ways, both successfully and unsuccessfully. This section will elaborate on the nature and cause of commonly seen unwanted modes and coupling, and outline past and current attempts to suppress them in the field of superconducting quantum computing.

2.1.1 Slotline modes

Parasitic slotline modes, or simply slotline modes, are a type of odd mode that occur when ground planes are not electrically connected or are uneven in width, leading to a voltage differential across the coplanar waveguide.

Ground planes become disconnected from one another when the design of the chip is such that sections of ground are enclosed by transmission lines or other components. Disconnected ground planes become inevitable in a planar circuit growing in complexity. Uneven ground planes can be caused by a bend in the transmission line or an asymmetric circuit design where a device lays close to one side of a transmission line but not the other.

Some type of connection is necessary in order to eliminate loss due to slotline modes [24]. Two common crossover solutions are used: wire bonds and air bridges.

Wire bonds

It is common practice to ground a chip's ground planes by wire bonding them to a metal base below the chip (Fig. 2.1). However, due to the poor shielding of wire bonds, crosstalk between neighbouring wire bonds cause this type of ground connection scheme to fail for larger chip sizes [25].

[1] Modes that fall outside of the 4-8 GHz range will not couple to on-chip devices and thus will not affect the performance of the circuit.

Wire bonds can also be used within a chip to connect ground planes across transmission lines and resonators. The small physical size of wire bonds leads to local grounding only, so a dense, uniform covering of wire bonds is necessary for good grounding.[26] Wire bonds also add inductance to the line [25, 26].

Finally, wire bonding can be performed onto pads at the edges of each chip in order to connect to external electronics for qubit control and measurement. However, this method does not allow connections to qubits located within a qubit array or complex circuit, as connections can only be made near the edges [27].

Air bridges

Air bridges (Fig. 2.1) are metallized freestanding structures which connect the ground on one side of a transmission line or resonator to the other [24, 26, 28, 29]. They are fabricated using standard photolithography methods and are generally seen as a more convenient alternative to wire bonding. While wire bonds add inductance to the line, air bridges add shunt capacitance [26].

A density of 10 air bridges per nm has been shown to fully attenuate slotline modes.[24] Chen *et al.* [24] notes an air bridge success rate of $> 99.9\%$. Some studies suggest that air bridges are fragile, and can fail as a result of an ultrasonic bath [24, 29]. Extrapolating from loss experiments in Chen *et al.*, [24] a resonator fully covered by air bridges would have an internal quality factor limited to 120,000 at low power [24]. The source of this loss is unclear but it is considered to be TLS loss due to its power dependence.

2.1.2 Crosstalk

Crosstalk is the exchange of signals between neighbouring lines or devices. Unintended crosstalk can occur when devices are close together. Sufficient separation of devices spatially or in frequency can mitigate crosstalk. However, as circuits become larger and denser, sufficient separation becomes more difficult to achieve.

One possible solution to crosstalk is to add some kind of shielding element between devices to block the signal, as proposed by Abraham *et al.* [30–32] In this scheme, a metallized cap chip containing a cavity is placed over the device chip, grounding the device's ground planes through a large capacitance between the two metallized layers.

Martinis and Megrant [33] measured a nine qubit circuit with conductor width 3 µm, gap 1.5 µm, and line separation 200 µm, and measured microwave crosstalk in the range of -6 dB to -10 dB.

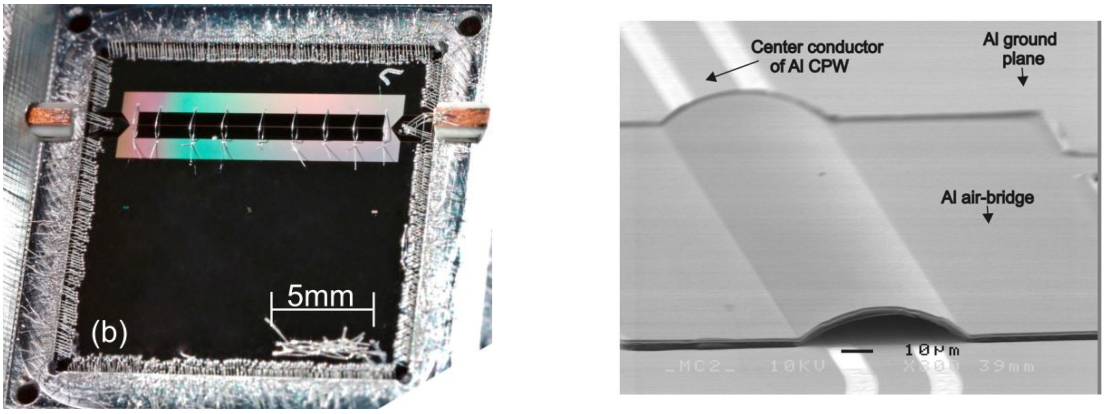

Figure 2.1: Physical implementations of two common solutions to parasitic slotline modes. Left: Photograph of a chip in a sample mount with wire bonds connecting to ground planes around the edges of the chip, and spanning an on-chip resonator, reproduced from [25]. Right: Scanning electron microscope image of an air bridge spanning a coplanar transmission line, reproduced from [26].

Crosstalk is also an issue between neighbouring wire bonds, as wire bonds are poorly shielded from the environment. This leads to significant loss in superconducting quantum circuits. Wire bonds are observed to have isolation[2] around 20 dB [27].

A possible solution to wire bond crosstalk is their replacement with another wiring scheme such as three-dimensional (3D) wiring [27]. By using 3D wiring and associated packaging (Fig. 2.2), crosstalk can be lowered to -45 dB in the dc to 10 GHz range. This set-up consists of a set of coaxial pogo pins embedded into the lid of the sample box. When the lid is put in place, the pins make contact with pads on the chip to connect to control and measurement electronics. The pin has a centre conductor which hits a pad connecting to an on-chip transmission line, while the outer ground of the pin makes contact with the on-chip ground plane. The package lid holds a washer spring at each corner which, when base and lid are assembled, make contact with the washer surrounding the chip and form a ground.

[2]Isolation is the opposite of crosstalk; it is the magnitude of the signal that does not leak to neighbouring devices.

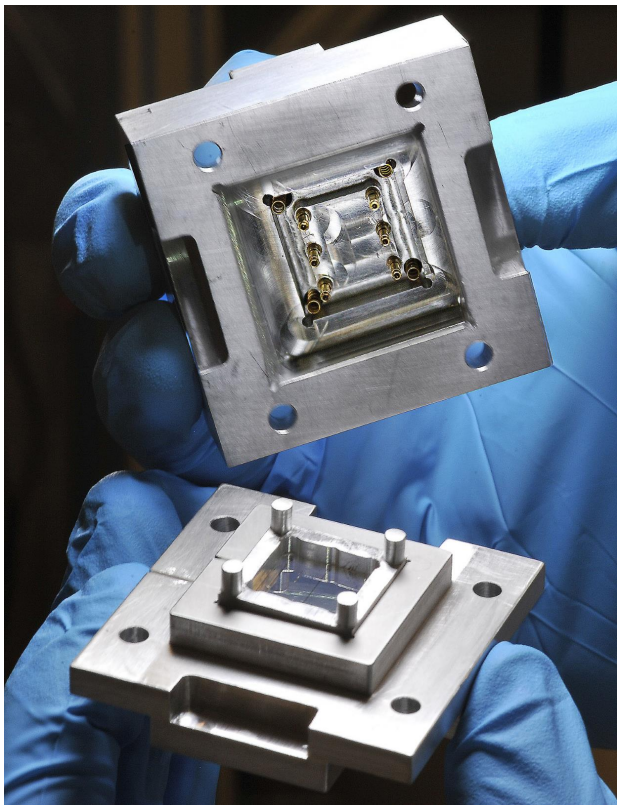

Figure 2.2: Image of a microwave package containing a set of six three-dimensional wires, reproduced from [27]. A chip is shown in the base under the washer, and four washer springs are located in the lid above each washer pillar. Six pogo pins are shown embedded in the package lid.

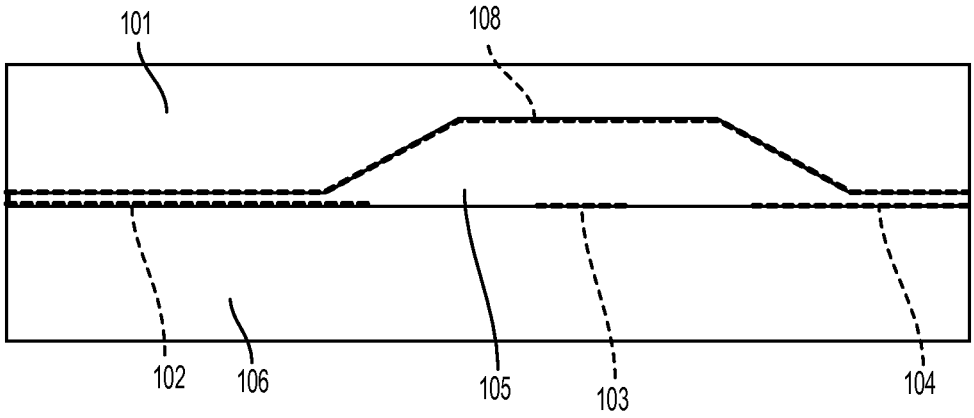

Figure 2.3: Cross-sectional diagram of a shielded coplanar transmission line designed to suppress unwanted modes and crosstalk, reproduced from [30]. 101: Cap chip. 108: Cap metallization. 105: Empty cavity. 106: Chip substrate. 102 and 104: Metallized CPW ground planes. 103: Metallized CPW centre conductor.

2.1.3 Box modes

Box modes are modes sustained within the free space in the sample box where the superconducting quantum circuit chip is held for cooldown and measurement (an example of a box used in cooldowns in this work is shown in Fig. 2.2). The frequencies of these modes depend on the geometry of the box. The fundamental frequency of the box is inversely related to its proportions: as the sample box grows in size, the fundamental frequency, and thus all of the modes associated with the box, become lower. If the box geometry is large enough, some box modes will fall within the superconducting circuit working range of 4-8 GHz and interfere with on-chip devices.

We can intentionally raise box mode frequencies by modifying the geometry or boundary conditions of the cavity. For example, adding an evacuated space below the chip (such as in Fig. 2.4) raises the box modes [27]. The addition of coaxial pogo pins has a similar effect by changing the electromagnetic boundary conditions [34]. Fig. 2.5 shows an architecture of 89 pogo pins of diameter 500 µm which increase the fundamental mode of the 72 mm × 72 mm × 3 mm sample box above 12 GHz.

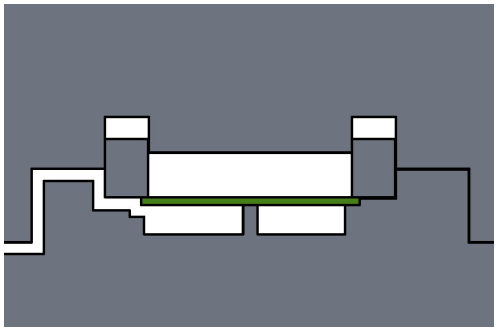

Figure 2.4: Cross-sectional diagram of a sample box (grey) and chip (green) with under-chip cavity for increasing the fundamental box mode frequency, and support pillar beneath the chip for stability. Vacancy line on the left is for pumping the chip cavity to vacuum. For scale, chip has a width of 15 mm. Photography of similar sample box can be found in Fig. 2.2. Image reproduced from [27].

2.1.4 Identifying unwanted coupling

Cavity modes such as box or chip modes (chip modes being modes sustained by the chip substrate) can be distinguished from other modes as they are visible in the spectrum both at room temperature when no superconductivity occurs and at low temperature, as they do not depend on superconductivity in order to exist. Box modes will be suppressed once the box cavity is interrupted (say, by being filled with material), but chip modes will not be affected by this as they are sustained by the chip and not the cavity. Thus, we can distinguish between these two types of modes by adding a filler within the empty space of the box [25].

Slotline modes and resonator frequencies can be distinguished experimentally by fabricating one chip with normal resonators and one where the resonators lack a centre conductor. Modes that occur in both samples are slotline modes, while modes that occur only in the first sample are designed resonances due to the coupled resonators [25].

2.2 Multilayer quantum devices

The expansion of superconducting quantum circuits into the third dimension can allow us to realize larger and denser qubit arrays, as well as facilitate more complex coupling schemes and architectures. As a solution to the scalability issues plaguing the superconducting quantum computer, Brecht *et al.* [35] proposed the multilayer microwave integrated

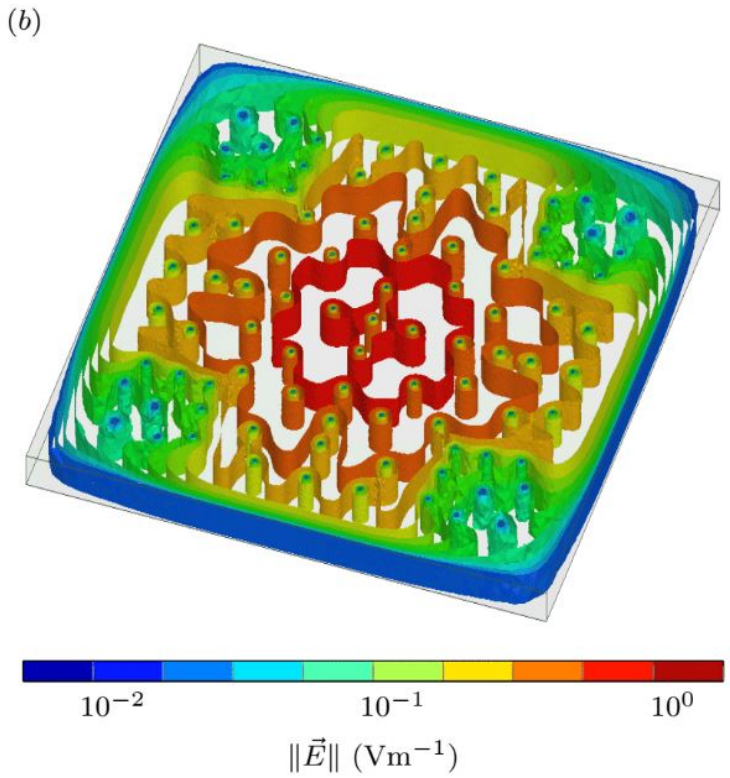

Figure 2.5: Simulation of the electric field magnitude $||\vec{E}||$ of the first box mode in a 72 mm $\times$ 72 mm $\times$ 3 mm sample box containing 89 coaxial pogo pins. Due to the pogo pins, the first box mode is raised to a frequency of 12.295 GHz. Image reproduced from [34].

quantum circuit (MMIQC), an architecture which takes advantage of the third dimension to lower the footprint of the quantum circuit.

The MMIQC architecture consists of stacked arrays of on-chip circuits enclosed within individual 3D cavities and connected by shielded superconducting transmission lines within the same layer and vias between layers (Fig. 2.6). First steps of this architecture have been demonstrated, with a micromachined resonant cavity [36] and a 3D transmon qubit inside a cavity [37].

Variations on this architecture have also been pursued. Rosenberg *et al.* [38] proposes a simpler near-term architecture in the same vein consisting of a base chip supporting qubits, and a cap chip supporting wiring and Josephson junctions for signal amplification. The two chips are connected through an interposer containing through-silicon vias and planar wiring using indium bump bonding. Initial testing of this architecture has been performed with transmon qubits on a separate chip as their control and readout lines.

Multilayer quantum devices have the advantage of being able to efficiently implement shielding of unwanted modes and crosstalk as shown in Fig. 2.3 and Fig. 2.6. This type of shielding can be performed by embedding a metallized cavity into the underside of a chip and placing it over the devices of interest. Multilayer quantum devices also have the benefit of being able to segregate devices to separate chips depending on their fabrication and performance requirements. For example, resonators, transmission lines, and other ancillary devices can be removed from the high performance qubit chip [38] in order to decrease the amount of processing and thus the likelihood of contamination of the qubits. This allows greater fabrication precision and the possibility of qubits with higher coherence times.

2.2.1 Indium in multilayer quantum circuits

With the rising interest in multilayer quantum circuits, indium has become a material of interest both for die bonding and for signal propagation purposes. Indium is a low temperature superconductor with a critical temperature $T_c = 3.4\,\mathrm{K}$. It is a commonly deposited thin film with high purity targets readily available for purchase. Due to its physical malleability and low melting point (157 °C compared to aluminium's 660 °C), indium is an ideal solder.

Indium bump bonds are a common bonding tool in the semiconductor industry that has recently been embraced by the field of superconducting quantum computing. This method is used to bond pairs of silicon wafers and electrically connect their on-chip circuits [38–

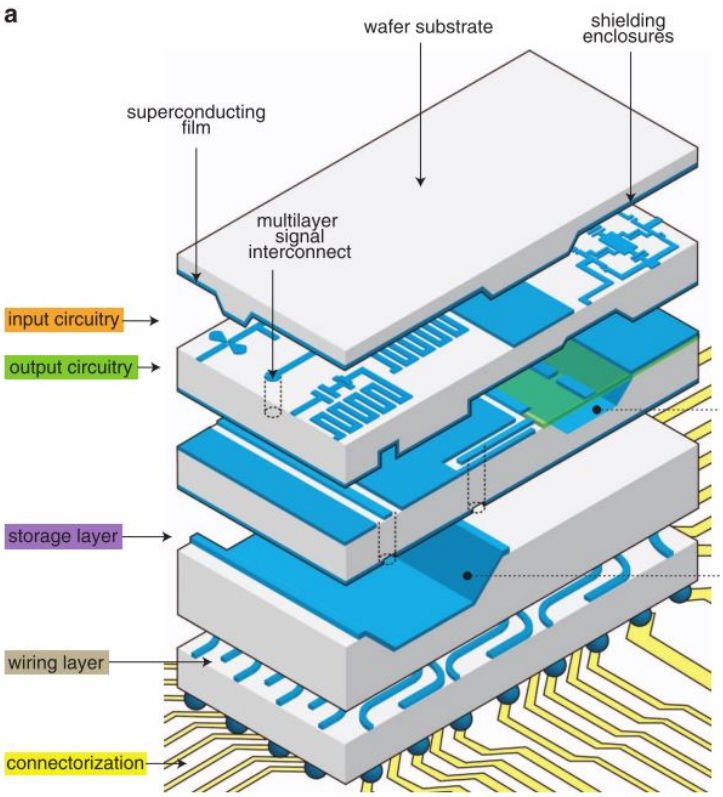

Figure 2.6: A diagram of the proposed microwave multilayer integrated quantum circuit consisting of metallized micromachined silicon cavities functioning as 3D resonators and shields, through-silicon vias for interconnection of layers, on-chip transmission lines and resonators, and qubits residing on a membrane (green), all connected by thin film bonding. Image reproduced from [35].

40]. Indium bump bonds are fabricated by patterning an indium film several microns thick. These bumps can then be used to cold bond two dies together under pressure.

Interdiffusion can occur between aluminium and indium films [41]. This phenomenon reduces the performance of devices, although the loss mechanism is unclear. Under bump metallization (UBM) is used in indium bump bonding in order to suppress diffusion between these metals [38]. Common UBM materials include titanium nitride, a non-oxidizing, high-Q superconductor, as well as stacks such as titanium/platinum/gold, [38] molybdenum/titanium, and titanium/palladium [39].

Rosenberg *et al.* [38] demonstrated 2,704 bump bonds in series with a resistance of 240 nΩ per bump at superconducting temperatures (< 1 K). In contrast, Foxen *et al.* [42] measured a resistance of < 3 nΩ per bump for a chain of 1,620 indium bumps, demonstrating what is essentially superconducting indium bump bonding. These bumps were bonded between a lower silicon substrate with aluminium circuits and titanium nitride UBM, and a silicon cap with indium wiring. O'Brien *et al.* [39] demonstrated a device capping method using indium bump bonds.

Chapter 3

Indium thin film thermocompression bonding for multilayer superconducting quantum circuits

The majority of this chapter was published on 2017 September 18 as [1] :

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The list of author contributions can be found in the Statement of Contributions within the front matter of this thesis.

As mentioned in Chapter 2, a large array of low error rate quantum devices is necessary in order to implement an extensible or scalable quantum computing architecture. Stacking microchips of various functionalities into multilayer superconducting quantum ciruits (Sec. 2.2) is a promising, up-and-coming method of scaling quantum processors.

The following section consists of the experimental demonstration of a thermocompression bonding technology that utilizes indium films as a welding agent to attach pairs of lithographically patterned chips. We perform chip-to-chip indium bonding in vacuum at 190 °C with indium film thicknesses of 150 nm. We characterize the dc and microwave performance of bonded devices at room and cryogenic temperatures. At 10 mK, we find a dc bond resistance of 49.2 $\mu\Omega\,\mathrm{cm}^2$. Additionally, we show minimal microwave reflections and good transmission up to 6.8 GHz in a tunnel-capped, bonded device as compared to a similar uncapped device. As a proof of concept, we fabricate and measure a set of tunnel-

capped superconducting resonators, demonstrating that our bonding technology can be applied to superconducting quantum computing.

3.1 Introduction

The field of quantum computing [5] is experiencing major growth thanks to the development of architectures with ten or more quantum bits (qubits) [43, 44]. The biggest challenge in the realization of a universal quantum computer is the implementation of extensible architectures where qubit operations can be performed with low error rates [45]. Among many promising qubit architectures, [46–49] those based on superconducting quantum circuits [50] are rapidly reaching a level of maturity sufficient to demonstrate the superiority in peformance of a digital quantum computer over the state-of-the-art classical supercomputer [8]. Elements of quantum error correcting codes [6, 7] have already been demonstrated in a variety of experiments using superconducting qubits [44, 51, 52] and a quantum memory has been realized with quantum states of microwave fields [53].

In order to build an extensible quantum computer, however, many technological advances must first be demonstrated. Among these, three-dimensional integration and packaging of superconducting quantum circuits is emerging as a critical area of study for the realization of larger and denser qubit architectures. This approach allows the departure from the two-dimensional confinement of a single microchip to a richer configuration where multiple chips are overlaid. Three-dimensional integration, thus, provides a flexible platform for more advanced classical manipulation of qubits and qubit protection from the environment. In this framework, an architecture based on multilayer microwave integrated quantum circuits has been proposed [54] and some of its basic elements realized, showing that high-quality micromachined cavities [35] can be used to implement three-dimensional superconducting qubits [37]. Leveraging the extensive body of work developed in the context of classical integrated circuits, flip chip technology has been adopted to bond pairs of microchips containing superconducting circuits [38, 40, 55]. Furthermore, high frequency through-silicon vias [56] and a quantum socket based on three-dimensional wires [27] have been developed to attain dense connectivity on a two-dimensional array of qubits.

In this work, we demonstrate the experimental implementation of a two-layer integrated superconducting circuit where two microchips are attached by means of thermocompression bonding in vacuum. The structures on the surface of the bottom chip (or *base chip*) and on the underside of the top chip (or *cap chip*) are fabricated using standard photolithography techniques. Instead of a discrete set of indium bump bonds, a continuous thin film of indium serves as bonding medium between the chips. A continuous film bond is more

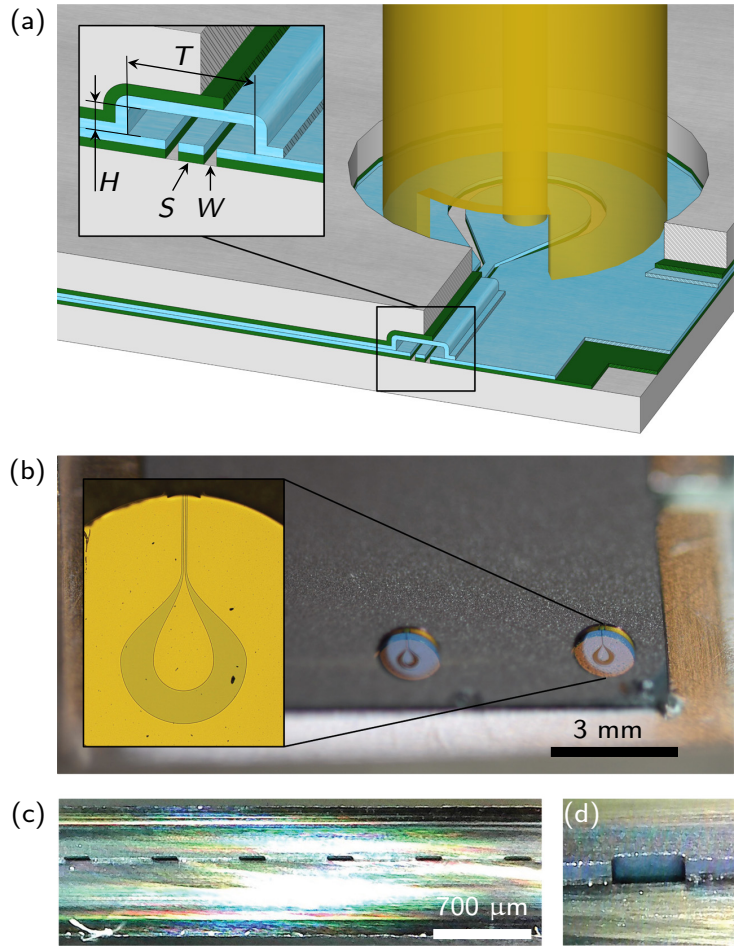

Figure 3.1: Capped devices formed using thermocompression bonding in vacuum. (a) Cutaway diagram of a capped device, exposing aluminium (dark green) and indium (light blue) films. The CPW transmission line features a center conductor of width $S = 12\,\mu\text{m}$ and gaps of width $W = 6\,\mu\text{m}$. The tunnel height is $H = 20\,\mu\text{m}$, with width $T = 175\,\mu\text{m}$ (see inset). Through holes in the cap allow electrical connection to the base chip by means of three-dimensional wires [27]. (b) Macrophotograph of a bonded sample. Inset: Microimage of a through hole showing a conductor trace aligned with a tunnel. (c) Cross section of a bonded sample showing six tunnels (dark gray rectangles). (d) Detail of a tunnel in (c).

practical than bump bonds for the electrical connection of ground planes, and can be seen as a complementary technique to bump bonds.

Using this method, an ideal bond would have very low or no dc resistance when measured at 10 mK. Bonded devices would have clean transmission spectra at microwave frequencies, and the internal quality factors Q_i of superconducting microwave resonators on bonded chips would be similar to those on otherwise identical unbonded chips.

In order to compare our bonding method to the ideal, we perform a detailed electrical characterization of a variety of bonded devices from room temperature to 10 mK at both dc and microwave frequencies, showing that the bonding technology can be used in quantum computing applications.

3.2 Sample fabrication

Fig. 3.1 (a) illustrates the geometric characteristics of a capped device. The base chip consists of a 500 µm thick intrinsic silicon substrate coated by a 150 nm thick aluminium film followed by an indium film of equal thickness. These films are sputtered *in situ* using a sputter system from AJA International, Inc., model ATC-Orion 5. The coplanar waveguide (CPW) transmission line visible in Fig. 3.1 (a) and other on-chip structures are defined by optical lithography followed by a wet etch in Transene A aluminium etchant. We find that Transene A works well to etch indium thin films as well as aluminium.

The cap chip consists of a 350 µm thick silicon wafer with tunnels trenched by isotropic reactive ion etching (RIE) and through holes formed using a deep RIE process. After etching, the cap chip is metallized with the same aluminium-indium process as the base chip. In this work, both base and cap chips have dimensions of 15 mm × 15 mm.

All silicon etching processes are performed with an RIE system from Oxford Instruments plc, model ICP380 (plasma-based dry etching). The tunnels are trenched with an isotropic RIE process based on sulfur hexafluoride (SF6) gas for 3 min. The through holes are formed using an OPT Bosch etch with 700 cycles (deep RIE process).

For the aluminium-indium films we resort to a wet etch due to the high vapor pressure of indium (about one order of magnitude higher than aluminium), making it ill-suited for most clean vacuum systems, including our RIE system.

Detailed recipes for these processes can be found in Appendix A.

Table 3.1: Aluminium and indium films deposition parameters. P: Dc power at sputter system cathode; $\dot{L}$: Deposition rate; d: Approximate throw distance, or distance between target and substrate; Size: Target size.

Metal	P (W)	$\dot{L}$ (Å s^{-1})	d (cm)	Size (inch)
aluminium	200	1.10	25	3
indium	50	1.85	25	3

3.3 Thermocompression bonding

The bonding procedure is realized in a custom-made vacuum chamber with the aid of an aligning and compressing fixture. The base and cap chips are aligned with a horizontal accuracy of less than 10 µm, significantly smaller than the device's maximum allowed tolerances [27]. The chips are subsequently compressed by applying vertical pressure with the fixture lid. At a system pressure of approximately 10^{-2} mbar, the chamber is placed for a typical time of 100 min on a hot plate at 190 °C, above the indium melting temperature (∼157 °C). Heating in vacuum prevents the formation of thick indium oxide and results in a strong mechanical bond without chemical or physical cleaning of the indium films prior to bonding. In fact, we found that bonded samples can withstand several minutes of high-power sonication and multiple thermal cycles to both 77 K and 10 mK. Refrigeration to 77 K is realized by dunking the samples in liquid nitrogen, demonstrating bond robustness to abrupt thermal stress. Images of a bonded sample are shown in Figs. 3.1 (b), 3.1(c), and 3.1(d).

3.3.1 Bonding details

Fig. 3.2 shows a computer-aided design of the custom-made vacuum chamber and aligning-compressing fixture used for the thermocompression bonding. The bottom of the chamber is made from a 10 mm thick copper plate, ensuring a high thermal conductivity and heat capacity. The bottom surface of the plate is mirror polished each time before placing the chamber on the hot plate. The top surface features a set of threaded screw holes, where aligning-compressing fixtures with different dimensions can be attached. The chamber is designed to process up to 3-inch wafers. The chamber wall is a 30 cm high, 3 mm thick hollow cylinder made from stainless steel, the low thermal conductivity of which ensures little or no heating of the top part of the chamber. The top edge of the cylindrical wall

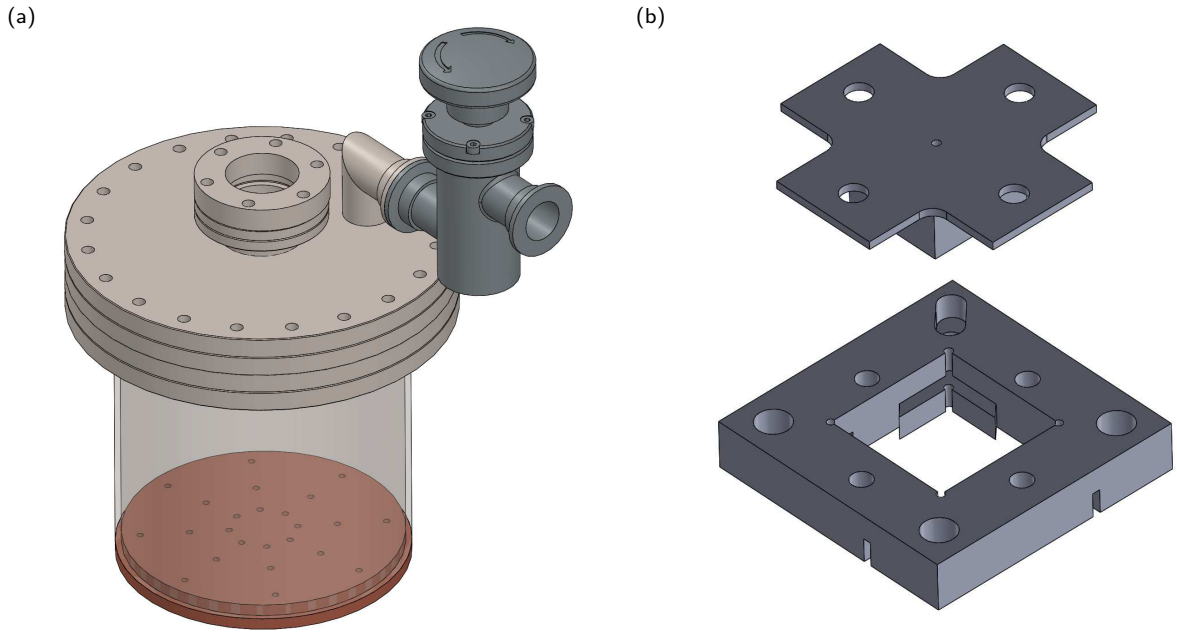

Figure 3.2: Thermocompression bonding setup. (a) Vacuum chamber. (b) Aligning-compressing fixture comprised of a square washer, an adjustable edge corner, and a lid. The channels used to evacuate the interior of the washer when tightened to the chamber base are visible.

is welded to a 6-inch ConFlat (CF) flange made from 304L stainless steel. The CF flange features a knife-edge seal mechanism. The sealing element is a fully annealed copper gasket made from 1/4 hard, high purity, oxygen-free (OFHC) copper, which allows for system pressures as low as 10^{-12} mbar at operating temperatures up to 450 °C. An ultra-high vacuum, temperature-resistant valve is used to connect the CF flange to a pump. A CF flanged Kodial glass viewport (sealed with a silver plated copper gasket) permits the observation of the chamber interior during processing.

The aligning-compressing fixture is a square washer with inner dimensions 16.5 mm × 16.5 mm made from stainless steel and featuring an adjustable edge corner. This corner can be moved along a groove at the bottom of the washer, allowing alignment between the base and cap chips. In this work, we use square chips with dimensions 15 mm × 15 mm. Note that the base chip is in direct contact with the copper plate, guaranteeing good thermalization.

3.3.2 Bonding recipe

The aligning procedure comprises three steps:

1. The base chip is placed inside the washer at the bottom of the chamber and pushed against the washer corner opposite to the adjustable corner;
2. The cap chip is manually dropped on the base chip, pre-aligning the chips as accurately as possible;
3. The two chips are aligned with the adjustable corner, which is fixed to the chamber with a screw.

The manual pre-alignment in step two is used to prevent damage of the on-chip structures due to relative dragging of the chips during step three. The lid shown in Fig. 3.2 is used to apply pressure on the aligned chips by means of four screws. We find that little pressure is required to obtain a mechanically strong bond.

After closing the chamber, we evacuate it with a molecular pump from Pfeiffer Vacuum GmbH for 30 min to reach a system pressure of 1.5×10^{-2} mbar, which is the lowest achievable pressure with this pump. While pumping we monitor the chamber leak rate, which is typically on the order of 1.0×10^{-10} mbar L s^{-1}. Once the chamber is placed on the hot plate, the temperature initially fluctuates reaching a steady state in approximately 10 min.

Table 3.2: Type and quantity of all bonded samples. dc: Samples used for bond characterization at dc; Microwave: Samples used for bond characterization at microwave frequncies. Resonators: Sample used for proof-of-concept quantum computing applications. Strength and alignment: Miscellaneous samples used for testing bond resilience to mechanical and thermal stress as well as alignment of base and cap chips. Bonded: Quantity of bonded samples per type. Good: Quantity of good samples (i.e., samples that we are able to measure). Yield: Percentage of good samples per bonded type [and weighted total yield (Total)].

Type	Bonded	Good	Yield (%)
dc	6	3	50
Microwave	3	2	67
Resonators	1	1	100
Strength and alignment	5	5	100
Total	15	11	73

After the temperature stabilizes, the chamber is left on the hot plate for about 100 min. Pumping continues during the entire heating process, as well as during a cooling period when the chamber is placed to rest on a thick aluminium plate.

3.3.3 Bonding results and next steps

Schoeller *et al.* [57] have demonstrated that heating indium in air leads to a native indium oxide layer at least five times thicker than in vacuum. Additionally, they have shown that the thickness of native indium oxide (i.e., an oxide present at ambient pressure and temperature) at the indium surface remains almost constant when heating indium at temperatures between 20 and 180 °C at an oxygen partial pressure of approximately 1.0×10^{-4} mbar for 120 min. The processing pressure reached with our Pfeiffer molecular pump is about one order of magnitude higher than in Schoeller's study. This could contribute to the further formation of indium oxide, deteriorating both bond homogeneity and contributing to bond resistance. We plan to upgrade to a higher-end pump that will make it possible to reach high vacuum ($\sim 1.0 \times 10^{-6}$ mbar) in future developments of this project.

Our bonding procedure is simple and reproducible, with a yield of $\sim 73\,\%$ for a total of 15 bonded samples. A detailed list of the various types of samples and their yield is reported in Table 3.2. Each sample type is characterized by a different layout. The layouts

for the base and cap chips are shown in the insets of Figs. 3.3 and 3.10. It is worth noting that several bonded samples are measured multiple times and at different temperatures. For example, the resonator sample is measured four times both at room temperature and 10 mK, each time obtaining similar results.

In future implementations, we are interested in including a cleaning step with either an acid buff or a hydrogen-nitrogen plasma to remove native indium oxide prior to bonding. Additionally, we will use slightly thicker indium films ($\sim$1 µm), a lower bonding pressure ($\sim 1.0 \times 10^{-6}$ mbar), *in vacuo* chip alignment and compression, as well as a higher and more homogeneous compression by means of a hydraulic press. Finally, we will add a titanium nitride interdiffusion barrier between the aluminium and indium films. See Chapter 2 for more details on aluminium/indium interdiffusion, and Chapter 4 for an in-depth look at interdiffusion in samples in this work.

3.4 Dc characterization of capped devices

The dc electrical behavior of a bonded device is characterized using the base and cap chip layouts shown in the inset of Fig. 3.3 (a). This design guarantees that a dc current flows through the bond region and the metallized tunnel when measuring the dc resistance between the two base-chip islands. Two samples are fabricated and measured: Samples dc01 and dc02. Sample dc02, however, is heated for a longer time, 180 min. All dc measurements are performed with a precision source-measure unit (SMU) from Keysight Technologies Inc., model B2911A (see Sec.3.4.1 for details). By applying a dc current through ports 1 and 4 and measuring the voltage across ports 2 and 3, we find a room temperature dc resistance $R \simeq 6.780\,\Omega$ for sample dc01 and $R \simeq 2.785\,\Omega$ for dc02. The difference between these two values can be attributed to the longer heating time, which leads to a stronger bond for sample dc02. We realize detailed numerical simulations of the device under test (DUT) by means of ANSYS Q3D Extractor [1] and find a theoretical $R \simeq 1.323\,\Omega$. As explained in detail in Sec.3.5, the discrepancy between the measured and simulated resistances is likely due to bond inhomogeneity. The current flows through the cross section of the sample, from the base to the cap chip. If only 50% of the sample area is bonded, the measured resistance is two times higher than for a fully bonded sample.

Fig. 3.3 (a) shows a four-point measurement of R as a function of temperature T for sample dc02. Below the superconducting transition temperature of aluminium, $T \simeq 1.2\,\mathrm{K}$, R is the resistance of the bond region (the *bond resistance*). The data points in the

[1] `http://www.ansys.com/Products/Electronics/ANSYS-Q3D-Extractor`

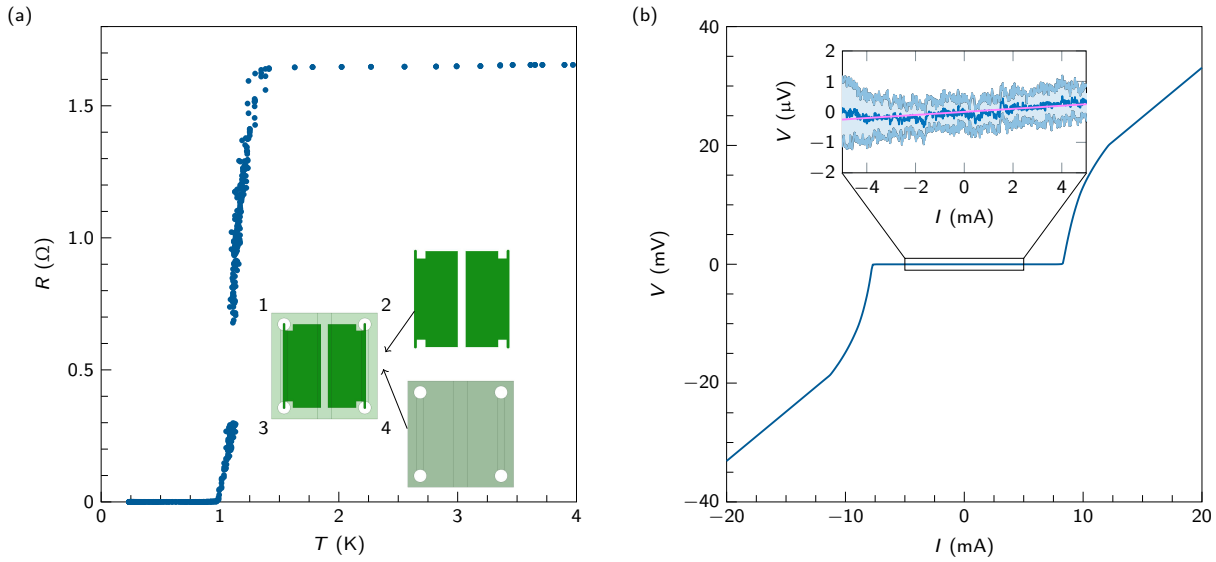

Figure 3.3: Bond characterization at dc. (a) Resistance R as a function of temperature T for the bonded device depicted in the inset (sample dc02). Inset: Base chip with two aluminium-indium islands separated by a dielectric gap. The fully metallized cap includes a tunnel which, when the chips are bonded, spans the gap on the base chip. The small resistance drop at the indium film transition temperature is discussed in Sec. 3.5. (b) I-V curve at $T \simeq 10\,\mathrm{mK}$ for dc02. Inset: Data and fit (magenta) below I_c. The $-10\,\mu\mathrm{V}$ offset voltage is due to the SMU.

figure are obtained by measuring the device current-voltage (I-V) characteristic curves at various temperatures and fitting their slope. Fig. 3.3 (b) shows the I-V curve measured at $T \simeq 10\,\mathrm{mK}$. We find a critical current of the aluminium-indium films, $I_\mathrm{c} \simeq 7.5\,\mathrm{mA}$, with a background series resistance due to the bond region. An ensemble of measurements well below I_c is reported in the inset of Fig. 3.3 (b). From the least-squares best fit we obtain a bond resistance $R \simeq 50 \mp 2\,\mu\Omega$, which corresponds to a specific bond resistance of less than $49.2\,\mu\Omega\,\mathrm{cm}^2$ assuming a 50 % bond area. This resistance is likely due to a mix of indium, aluminium, indium oxide, and aluminium oxide, preventing the bond region from becoming superconductive at low temperatures (see Sec. 3.5). The specific bond resistance for dc01 at $T \simeq 10\,\mathrm{mK}$ is about ten times larger than for dc02, while the critical current is about the same.

3.4.1 Measurement set-up and settings

In the set-up used for the dc characterization of bonded devices, the DUT is mounted in a package attached to a package holder that is anchored to the mixing chamber stage of a cryogen-free dilution refrigerator (DR) from BlueFors Cryogenics Ltd., model BF-LD250. A set of four three-dimensional wires [27] provides electrical contact to the DUT. Details on the package holder can be found in Béjanin *et al.* [27] The package holder is then connected to a set of phosphor bronze twisted pairs from Lake Shore Cryotronics, Inc., with gauge AWG 36 from 10 mK to 3 K and gauge AWG 32 from 3 K to room temperature. Extreme care is taken to avoid any thermoelectric effects by heatsinking the twisted pairs at all temperature stages of the DR by means of custom-made gold-plated OFHC copper bobbins. Each twisted pair is wound several times around a bobbin and glued to the bobbin using STYCAST 1266 A/B Epoxy from Emerson & Cuming Ltd. below the 3 K stage and STYCAST 2850 FT Black Epoxy with catalyst 24LV (also from Emerson & Cuming Ltd.) above the 3 K stage. The twisted pairs are finally connected at room temperature to a precision SMU from Keysight, model B2911A.

The SMU can generate dc currents in the 10 nA range, with a peak-to-peak noise of less than 1 pA; the voltage measurement resolution is 100 nV with an accuracy (% of reading + offset) of $\mp(0.015\,\%{+}225\,\mu\mathrm{V})$ for the $\mp 200\,\mathrm{mV}$ range (in a stable temperature and humidity environment, as is the case in our lab). The SMU settings for all dc measurements reported in this work are listed in Table 3.3.

We note that the I-V characteristic curve for sample dc02 at $T \simeq 10\,\mathrm{mK}$ below I_c [see inset of Fig.3.3(b)] shows a $-10\,\mu\mathrm{V}$ offset voltage, which is well within the offset accuracy of the SMU for the voltage measurement range being used ($\mp 200\,\mathrm{mV}$ range). Despite the

Table 3.3: Samples and relative SMU settings for all reported dc measurements. dc01 R: Resistance R for sample dc01 at room temperature; dc02 R: Resistance R for sample dc02 at room temperature; dc02 $R(T)$: Resistance R for sample dc02 as a function of temperature T [see Fig. 3.3 (a)]; dc02 I-V: I-V characteristic curve for sample dc02 at $T \simeq 10\,\mathrm{mK}$ [see Fig. 3.3 (b)]; dc02 I-V ($< I_\mathrm{c}$): I-V characteristic curve for sample dc02 at $T \simeq 10\,\mathrm{mK}$ below I_c [see inset of Fig. 3.3 (b)]; dc01 I-V ($< I_\mathrm{c}$): I-V characteristic curve for sample dc01 at $T \simeq 10\,\mathrm{mK}$ below I_c (data not shown; R and I_c reported in this work); dcAl $R(T)$: Resistance R for sample dcAl as a function of temperature T [see Fig. S2 (a)]; dcAl I-V: I-V characteristic curve for sample dcAl at $T \simeq 100\,\mathrm{mK}$ [see Fig. 3.4 (b)]; dcAl I-V ($< I_\mathrm{c}$): I-V characteristic curve for sample dcAl at $T \simeq 10\,\mathrm{mK}$ below I_c [see inset of Fig. 3.4 (b)]. N: Number of current points; S: Number of current sweeps (used for measurement ensemble average); NPLC: Number of power line cycles (i.e., voltage integration time in power line periods of $1/60\,\mathrm{Hz}$); $t_\mathrm{w}/t_\mathrm{m}$: Wait to measurement time ratio per current point; Δt: Wait time between current sweeps.

Sample	N	S	NPLC	$t_\mathrm{w}/t_\mathrm{m}$	Δt (s)
dc01 R [2]	50	-	1.0	-	-
dc02 R	201	5	2.0	0.1	2.0
dc02 $R(T)$	121	725	0.3	1.0	18.6
dc02 I-V	601	10	3.0	5.0	10.0
dc02 I-V ($< I_\mathrm{c}$)	601	10	1.0	10.0	10.0
dc01 I-V ($< I_\mathrm{c}$)	2001	30	1.0	2.0	0.1
dcAl $R(T)$	201	200	3.0	1.0	39.0
dcAl I-V	122	25	3.0	4.0	15.0
dcAl I-V ($< I_\mathrm{c}$)	101	60	3.0	4.0	5.0

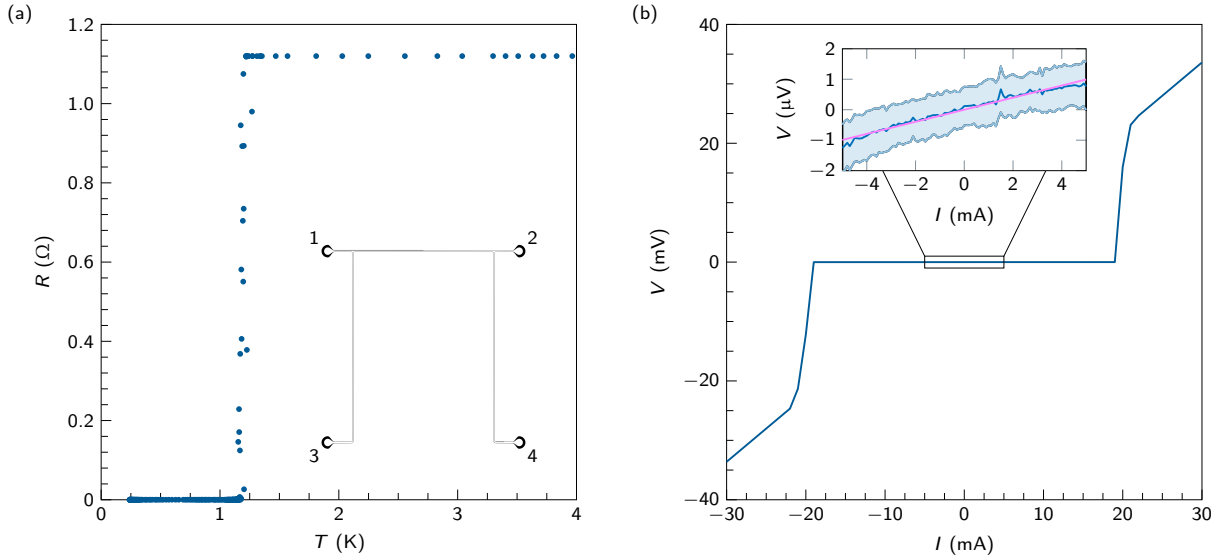

Figure 3.4: SMU characterization at dc with a superconducting aluminium sample. (a) Resistance R as a function of temperature T for the device depicted in the inset (sample dcAl). Inset: The device features an aluminium trace of 70 µm width and 8.3 mm length (between the two pad centers) and with 300 nm thickness; the thin film aluminium is grown by physical vapour deposition using a sputtering deposition system from AJA International, Inc., ATC Orion Series. Electrical contact to the four pads is realized by means of a set of four three-dimensional wires [27]. (b) I-V characteristic curve at $T \simeq 100$ mK. Inset: Data and fit (magenta) below I_c.

fact that the measurement parameters for the I-V curve data in the main panel and inset are slightly different (see Table 3.3), the offset voltage for the inset is consistent with the -12.7 µV offset voltage obtained by fitting the normal-state resistance of the I-V curve at large current bias (linear fit from -20 to -15 mA and from 15 to 20 mA) and finding the intercept with the voltage axis at zero bias current. In addition, the measurements are performed using a current-reversal method, i.e., by inverting the current polarity and combining the scans with opposite polarity. Considering the fast response speed and low noise of the voltmeter featured by our SMU, this method eliminates any possible thermoelectric electromotive forces. The -10 µV offset voltage, however, persists, indicating that it is due to an SMU stochastic voltage measurement error. The combination of these low-level measurement techniques and the meticulous wire thermalization discussed above allow us to safely conclude that the -10 µV offset voltage is not due to a thermoelectric effect.

In order to ensure that the bond resistance value reported for sample dc02 is not affected

by spurious effects due to the measurement setup, we perform a calibration measurement of a standard aluminium device with layout shown in the inset of Fig. 3.4(a). We realize four-point measurements by applying a dc current through ports 1 and 2 and measuring the corresponding voltage across ports 3 and 4. As shown in Fig. 3.4, we determine the superconducting transition temperature of the aluminium film to be $T \simeq 1.2\,\mathrm{K}$ and the critical current of the device, $I_\mathrm{c} \simeq 20\,\mathrm{mA}$. Below the transition temperature and critical current, the residual resistance of the device is $R \simeq 200\,\mu\Omega$. This corresponds to a specific resistance of approximately $42\,\mathrm{p}\Omega\,\mathrm{cm}^2$, which is about six orders of magnitude lower than the specific bond resistance for dc02. We thus conclude that our dc measurement setup and settings are adequate to resolve the bond resistance for the samples presented in this work.

3.5 Bond inhomogeneity

3.5.1 Interdiffusion and bonding

The five metal and metal-oxide layers of a bonded device from bottom to top are: Aluminium, indium, bond region, indium, and aluminium. From a set of preliminary secondary ion mass spectrometry data (Sec. **??**), it appears that our sputtered samples suffer from aluminium-indium interdiffusion [41]. Thus, each layer is not made of one single element, but rather a mix of elements. In particular, the bond region is likely a mix of indium, aluminium, indium oxide, and aluminium oxide.

The presence of oxides as well as aluminium at the interface between base and cap chips before bonding prevents parts of the sample surface from bonding at the processing temperature of 190 °C. In fact, aluminium melts at the much higher temperature of approximately 660 °C (assuming a mild processing pressure, as in our procedure). This effect is likely exacerbated by the compressing fixture lid that is designed to be smaller than the samples area (thus applying pressure mostly to the center of the chips and less to the edges), and by a tilt between base and cap chips. The combination of these factors leads to bond inhomogeneity.

3.5.2 Visual characterization of bond area

A qualitative analysis of bond inhomogeneity is realized by breaking apart a bonded device and optically inspecting the bond surface of the base and cap chips, as shown in Fig. 3.5.

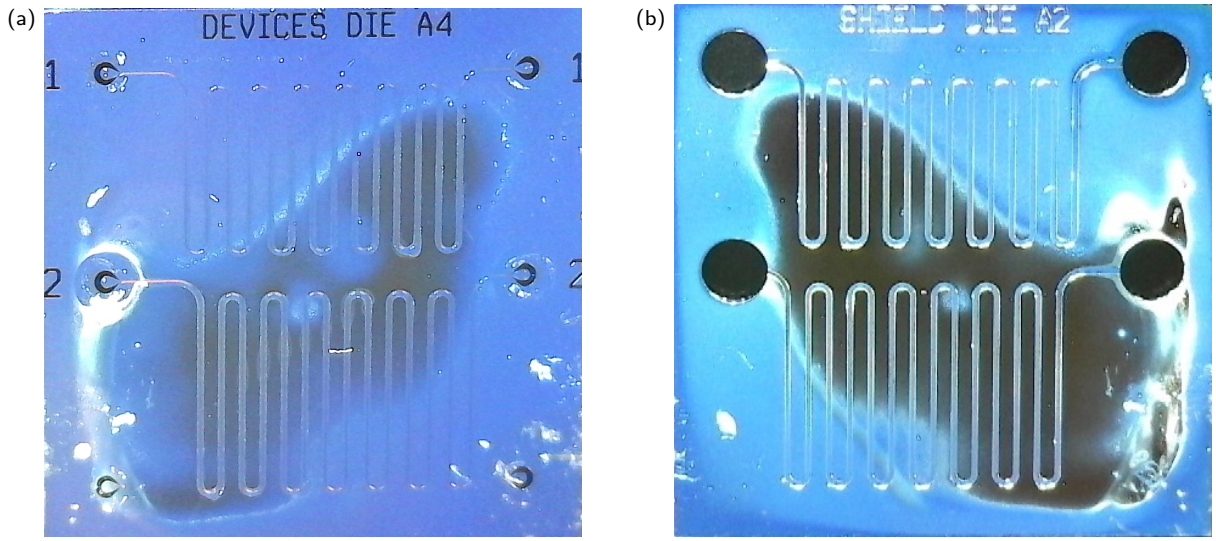

Figure 3.5: Optical characterization of bond inhomogeneity. (a) Image of the base chip after bonding. The marks left by the three-dimensional wires on trace 1 and 2 are clearly visible. (b) Image of the cap chip after bonding.

The images refer to the device outlined in the inset of Fig. 3.10 (c) and are taken by means of a handheld digital microscope. The film within the boundary of the through holes on the base chip [see Fig. 3.5(a)] is heated during the bonding process, but not bonded to the cap. We can thus use the color of the film in this region as a reference to discern bonded from unbonded regions. We determine that the region near the center of the base and cap chips is bonded well, whereas the area around the edges of the two chips is not bonded. In this case, approximately 50 % of the samples area is bonded well. We find similar results in other devices.

3.5.3 Scanning acoustic microscopy characterization

Scanning acoustic microscopy (SAM) is used to non-destructively image the bonding area of a capped test sample (Figs 3.6 and 3.7). SAM imaging in this work was performed by M.J. Moore of the Kolios Lab at Ryerson University. In these images, the change in contrast denotes a change in acoustic properties of the sample such as sound propagation speed or material density. Delaminations caused by unbonded regions within the sample are shown as light areas, and well-bonded regions are dark. Tunnels and through holes in the cap chip are also shown as light areas.

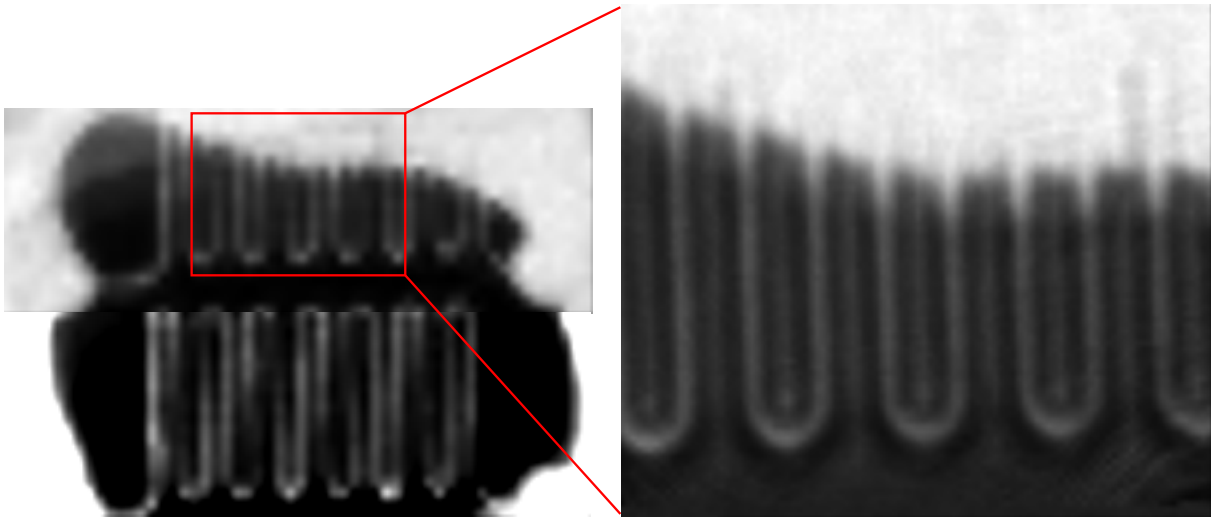

Figure 3.6: Scanning acoustic microscopy image of capped test sample with design reported in the inset of Fig. 3.10 (c). Bonded regions are visualized as dark pixels, while unbonded regions are light or white. Images thanks to M.J. Moore, Kolios Lab, Ryerson University.

100 % of the 5 samples imaged using SAM show significant delaminations around the edges of the sample. From the SAM images, we can conclude that the alignment washer's compressing lid is too small or not giving a homogeneous pressure, leading to delaminations around the chip edges. This agrees with the information from the device that was broken apart in Fig. 3.5.

3.5.4 The flux tube model

Bond inhomogeneity can be understood quantitatively by modeling the five metal and metal-oxide layers of a bonded device as a large set of adjacent flux tubes directed from the base to the cap chip. Here, the flux is unrelated to the magnetic flux or any property of superconducting films or devices, as we are considering room temperature devices. Each tube is a quasi-filiform parallelepiped with the square root of its cross-sectional area being much smaller than the tube length along its central axis; i.e., the tubes can be assumed to be thin wires. Tubes have constant flux of the current density vector $\vec{J}$ through every cross section of the tube along its central axis. The sum of all cross-sectional areas corresponds to the total area of the sample surface. At room temperature, each tube has a resistance R_{tube}; the total resistance R is the series of the parallel resistance of all flux tubes on the left

Figure 3.7: Scanning acoustic microscopy image of capped resonator sample with design reported in the inset of Fig. 3.10 (b) and measurements reported in Fig. 3.10 (b), Table 3.4, and Fig. 3.11. Bonded regions are visualized as dark pixels, while unbonded regions are light or white. Image demonstrates significant delaminated regions around the edges of the chips, with a well-bonded region in the centre. Images thanks to M.J. Moore, Kolios Lab, Ryerson University.

and right side of the cap tunnel, respectively. Flux tubes in an unbonded region are open circuits with resistance $R_{\text{tube}} \sim \infty$ and cause R to increase. Following this model, the ratio between measured and simulated resistances indicates that approximately 20 % of sample dc01 and 50 % of sample dc02 is bonded.

This analysis attributes the discrepancy between measured and simulated room-temperature resistance to bond inhomogeneity, indicating that the bond resistance is negligible compared to the aluminium and indium films resistance at room temperature. Thus, in order to measure the bond resistance the samples must be cooled below 1 K, where both the indium and aluminium films are in the superconducting state.

3.5.5 Bond superconductivity

We have shown in Fig. 3.3 that the bond region does not become superconductive. This effect cannot be attributed solely to a layer of indium oxide at the base-cap chip interface. In fact, if this was the case the base and cap chips would not bond to each other, or bond very weakly, which is contradicted by our bond mechanical robustness tests. Instead, the bond region is a complex mix of indium, aluminium, indium oxide, and aluminium oxide that behaves as a normal resistor, the resistivity of which cannot easily be determined from literature values for single metal or metal-oxide aluminium and indium layers.

3.5.6 Indium film transition temperature

Fig. 3.8 shows a detail of the four-point measurement in Fig. 3.3 (a) for a temperature range in proximity of $T = 3.4\,\text{K}$, which is the expected transition temperature of the indium films to the superconducting state. The resistance drop is much smaller than at the transition of the aluminium films to the superconducting state, as shown in Fig. 3.3 (a). This is likely due to aluminium interdiffusion into the indium layers, resulting in a pattern of indium films in the bond region consisting of small pockets of indium embedded among aluminium pockets. Because of this effect, and possibly the presence of indium oxide, only a very small part of the total bonded chip resistance becomes superconductive around 3.4 K. A very small resistance drop corresponding to the indium transition temperature for devices similar to ours has also been observed by O'Brien *et al.* [55]

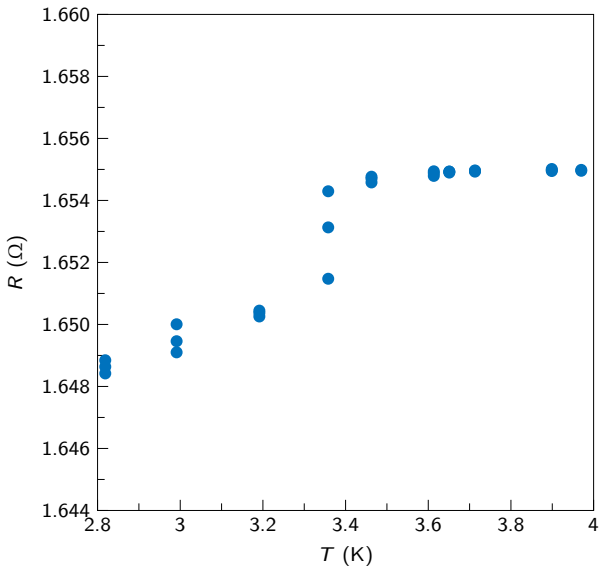

Figure 3.8: Resistance R as a function of temperature T for the capped device depicted in the inset of Fig. 3.3 (a) in proximity of $T = 3.4\,\mathrm{K}$. The resistance jump for indium is very small, likely due to aluminium interdiffusion.

3.6 Microwave characterization of capped devices

Fig. 3.10 displays the microwave characterization of three capped and uncapped devices with layouts shown in the insets. The measurements are realized by means of a vector network analyzer (VNA) from Keysight Technologies Inc., model PNA-X N5242A; details on the measurement setups are in Béjanin *et al.* [27] and on calibration in the following section.

3.6.1 Reflection measurements

The room temperature measurements in Fig. 3.10 (a) demonstrate that the bonding process and the addition of the cap do not noticeably increase the reflection coefficient. An area of specific interest is the *tunnel mouth region*, the edge of a through hole where the cap tunnel begins. This measurement is sufficient to characterize the tunnel mouth region which is likely the most significant source of reflections for a capped device. In fact, the microwave reflections due to the tunnel mouth are largely unaffected by the room temperature resistance of the subsequent aluminium-indium transmission line.

The calibration procedure for the measurement of reflection coefficients at ∼10 mK in a dilution refrigerator is a challenging task. This is due to the complexity of the measurement setup, which features a large number of attenuators in the input line leading to the DUT [27]. Each attenuator is characterized by a reflection plane that masks the reflection-coefficient measurement of the DUT. Thus, we perform these measurements at room temperature only. This allows us to maintain the DUT reference planes as close as possible to the VNA ports, making the measurement fast and reliable.

3.6.2 Reflection simulations of the tunnel mouth

The tunnel mouth represents a boundary condition for the electromagnetic field associated with a capped transmission line. The line shown in the inset of Fig. 3.10 (c) is characterized by two of such boundary conditions. In order to determine whether these conditions generate unwanted resonance modes, we simulate the transmission coefficient S_{21} for this line and compare it to that of an uncapped line and of a capped line without tunnel mouths (i.e., covered by an infinitely long tunnel). The numerical simulations are performed with ANSYS HFSS, [3] assuming perfect conductors and lossless CPW transmission lines with equal geometric characteristics.

The graphs displayed in Fig. 3.9 reveal almost perfect transmission for the three simulated configurations, with less than 0.1 dB of loss due to slight impedance mismatch. We can safely conclude that the unwanted resonances shown later in Fig. 3.10 (c) are not due to the presence of the tunnel mouths.

3.6.3 Crosstalk measurements

Fig. 3.10 (b) shows a measurement of the crosstalk coefficient between two adjacent transmission lines at room temperature. At microwave frequencies a signal injected at port 1 or 2 can leak to ports 3 and 4, generating crosstalk. The addition of the cap reduces crosstalk by more than 10 dB across the entire measurement bandwidth. We perform the same measurements at ∼10 mK and find that the crosstalk signal from the capped device is below the VNA noise floor. This result has important implications to quantum computing, where crosstalk has been identified as a major source of error [58].

The presence of many input attenuators, combined with the high isolation of our capped samples, makes the measurement of crosstalk coefficients at low temperatures challenging

[3] `http://www.ansys.com/products/electronics/ansys-hfss`

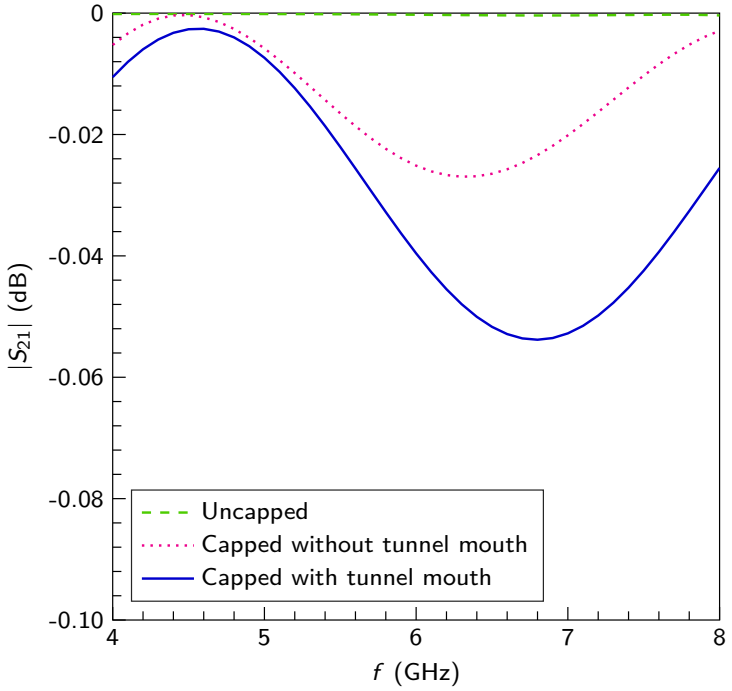

Figure 3.9: Magnitude of the simulated transmission coefficient $|S_{21}|$ as function of frequency f for an uncapped, capped without tunnel mouth, and capped with tunnel mouth CPW transmission line. The chosen frequency range is the same as in Fig. 3.10 (c).

as well. In fact, we refrigerate the bonded sample with layout shown in the inset of Fig. 3.10 (b) to ∼10 mK. We find that the power of the crosstalk signal from the output port of a capped device (e.g., port 4) is below the VNA noise floor, even for the highest VNA input excitation power of ∼10 dB-milliwatts (dBm). Detecting such a weak signal is possible, but requires a substantial amount of averaging as well as a very low VNA intermediate frequency bandwidth Δf_{IF} (e.g., $\Delta f_{\mathrm{IF}} \sim 1\,\mathrm{Hz}$). Therefore, it is extremely time inefficient and unreliable to perform a low-temperature crosstalk measurement with a broad bandwidth, similar to the room temperature measurement shown in Fig. 3.10(b).

3.6.4 Transmission measurements

Fig. 3.10 (c) displays transmission-coefficient measurements at ∼10 mK, where both the indium and aluminium films are in the superconducting state. Transmission is clean for both uncapped and capped devices up to $f \simeq 6.8\,\mathrm{GHz}$. At higher frequencies, we observe a series of pronounced resonances for the capped device. The simulations in Fig. 3.9 and the results in Fig. 3.10 (a) indicate that these resonances are not due to the presence of the tunnel. We believe they are caused by bond inhomogeneity, resulting in unwanted resonances similar to the slotline modes observed by Wenner *et al.* [25] due to the addition of extra disconnected ground planes on the cap.

As explained above, reflection-coefficient measurements at room temperature provide important insight into the behavior of key elements of capped devices. Nevertheless, the room-temperature series resistance of the CPW transmission line following the tunnel mouth region is sufficiently large to conceal any abnormalities in the transmission coefficient measurement.

In contrast to reflection and crosstalk measurements, it is rather simple to perform transmission measurements at $\sim 10\,\mathrm{mK}$, as no special calibration is required. This is because a transmission line in the superconducting state behaves as an almost lossless through, unveiling all possible anomalies due to the DUT itself. Fig. 3.10(c) shows a transmission coefficient measurement for both an uncapped and capped device at a temperature of $\sim 10\,\mathrm{mK}$. The excitation power at the input of each of the two devices is approximately −66 dBm. As a comparison, this power is at least six orders of magnitude higher than for the resonator measurements reported in Table 3.4.

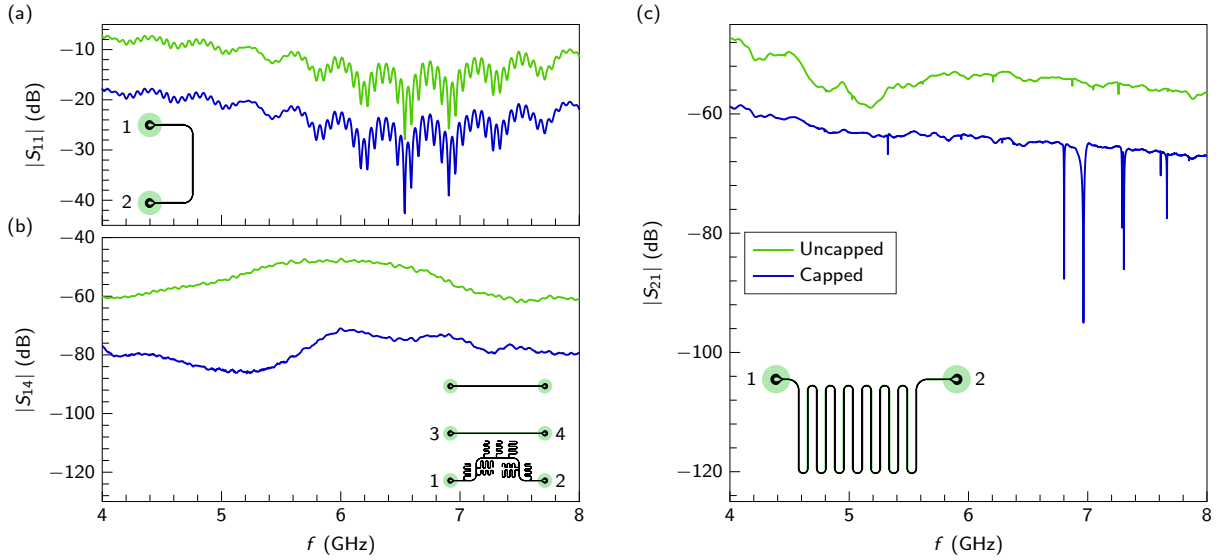

Figure 3.10: Characterization at microwave frequencies of the uncapped and capped CPW transmission lines shown in insets; black lines refer to structures on the base chip and light green shades indicate metallized tunnels and through holes in the cap chip. Data for uncapped devices is plotted in light green and for capped devices in dark blue. For clarity, the capped data in (a) and (c) are translated by an artificial vertical offset of $-10\,\mathrm{dB}$. (a) Magnitude of the reflection coefficient at port 1, $|S_{11}|$, as a function of frequency f. (b) Magnitude of the crosstalk coefficient between ports 1 and 4, $|S_{14}|$, vs. frequency f. (c) Magnitude of the transmission coefficient $|S_{21}|$ vs. frequency f.

3.7 Superconducting resonators

As a proof of concept for quantum computing applications, we compare similar capped and uncapped superconducting CPW resonators with layouts sketched in the inset of Fig. 3.10 (b). The base-chip layout is the same for both capped and uncapped devices and comprises a set of nine quarter-wave resonators capacitively coupled to feed line $1-2$ in a multiplexed design [27]. The resonators are labeled as $n = \{1, 2, \ldots, 9\}$ starting from port 1 of the feed line. Two identical base chips are fabricated, one of which is bonded to a cap chip. The capped and uncapped devices are measured in a dilution refrigerator at $\sim$10 mK using the setup in Béjanin *et al.* [27]

3.7.1 Resonator fitting

The resonators are characterized by measuring their quality factors for a mean photon occupation number $\langle n_{\mathrm{ph}} \rangle \simeq 1$, similar to the excitation power used in quantum computing operations. The main resonator parameters are reported in Table 3.4. Seven uncapped and four capped of the total 18 measured resonators yielded. The nonstandard etching process of the aluminium-indium films possibly contributes to the resonator failure for the base chip. The higher failure rate for the capped devices is likely due to the bonding process, causing open circuits (due to scratches) or short circuits (due to molten indium joining the CPW inner and outer conductors). The quality factors for a subset of measured resonators is not reported due to poor fitting at such a low excitation power. The measured data and fits for the $n = 1$ uncapped and capped resonators are shown in Fig. 3.11.

Fig. 3.11 shows data and fits for the $n = 1$ pair of uncapped and capped superconducting CPW resonators reported in Table 3.4. The displayed data for the capped resonator is the ensemble average of 2 measured traces, whereas only one trace is measured for the uncapped resonator. In both cases, each data point is obtained by setting the VNA to an intermediate frequency bandwidth $\Delta f_{\mathrm{IF}} = 1\,\mathrm{Hz}$.

3.7.2 Capped and uncapped resonator comparison

In Sec. 3.7.3, we determine that the internal quality factor of a capped resonator, $\widehat{Q}_{\mathrm{i}}$, should be approximately 1 % larger than that of an uncapped resonator, Q_{i}, due to the vacuum participation. However, we find that $Q_{\mathrm{i}} \simeq 2\widehat{Q}_{\mathrm{i}}$ (see Table 3.4). We measure the $n = 3$ uncapped resonator over a time period of 10 h and find a Q_{i} with a standard deviation as large as one quarter of the mean value. We find significant time variations in all resonator measurements, even for shorter time periods. These results are consistent with the findings in Neill *et al.* [59] and indicate that the internal quality factors of capped and uncapped resonators are approximately equal when accounting for time fluctuations. Hence, the thermocompression bonding process does not significantly deteriorate the resonator performance, which, instead, is largely affected by the addition of the sputtered indium film. In fact, the quality factors reported here are about one order of magnitude lower than our typical electron-beam evaporated aluminium-only resonators [27].

3.7.3 Vacuum contribution to capped resonators quality factor

The addition of a grounded cap above a CPW resonator forces some of the electric field lines to be distributed from the base to the cap chip, away from the base chip substrate.

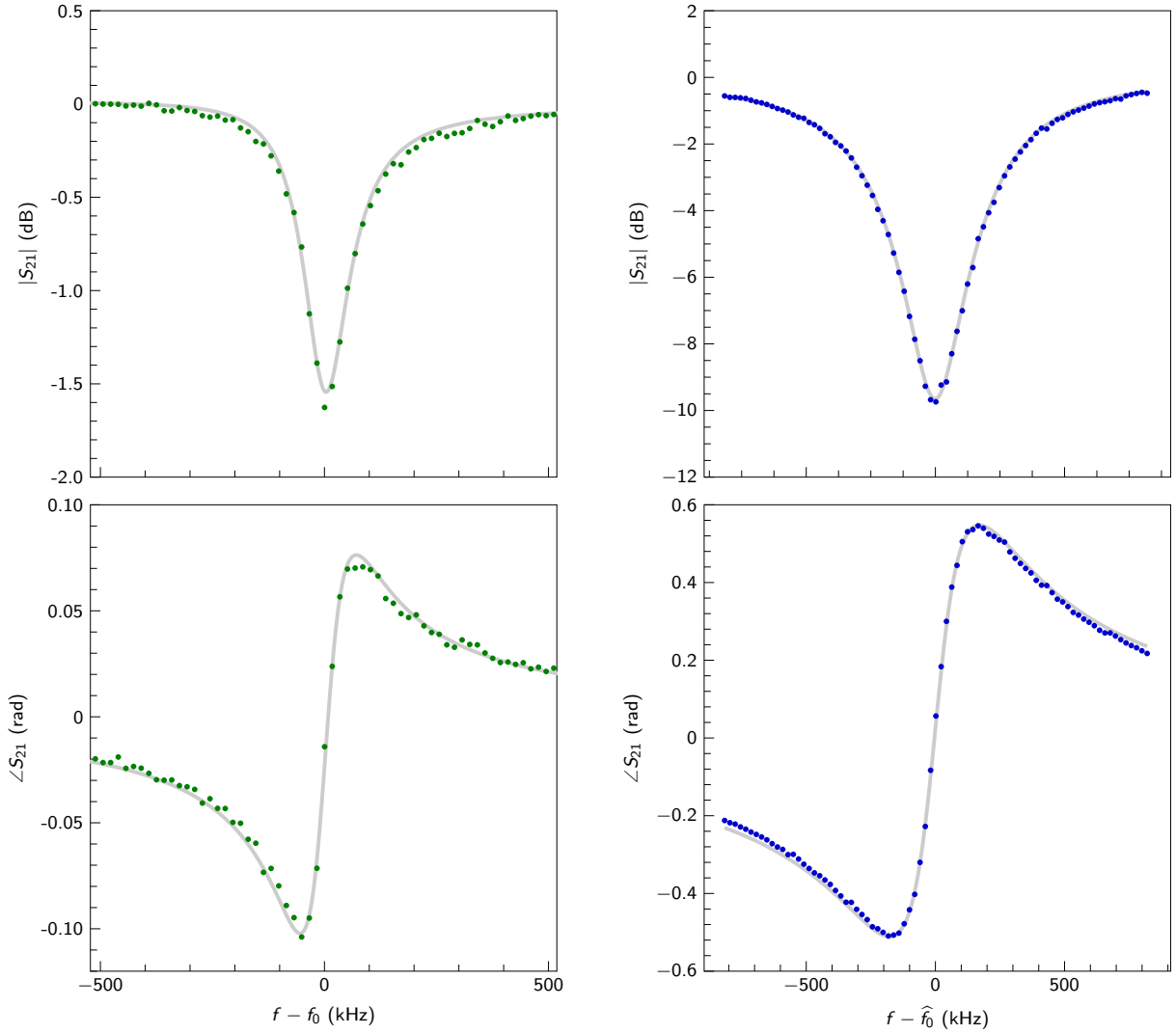

Figure 3.11: Uncapped (left panels) and capped (right panels) resonator measurements (dots) at low power (i.e., $\langle n_{\mathrm{ph}} \rangle \simeq 1$). The resonator transmission magnitude $|S_{21}|$ (above) and phase angle $\angle S_{21}$ (below) are plotted vs. the frequency departure from the resonance frequency, $f - f_0$ (uncapped) and $f - \widehat{f}_0$ (capped), and are fitted as in Béjanin *et al.* [27] (light gray). The resonance frequencies are reported in Table 3.4.

This increases the contribution of vacuum to the mode volume of a capped resonator compared to the case of an uncapped resonator. Assuming all metallic structures to be perfect conductors, the internal quality factor is solely due to dielectric losses and, thus, it can be found by inverting the loss tangent as, [11]

$$Q_{\mathrm{i}} = \frac{\varepsilon'_{\mathrm{e}}}{\varepsilon''_{\mathrm{e}}} \quad , \tag{3.1}$$

where $\varepsilon_{\mathrm{e}} = \varepsilon'_{\mathrm{e}} - j\varepsilon''_{\mathrm{e}}$ is the effective electric complex permittivity of the CPW transmission line with real and imaginary parts $\varepsilon'_{\mathrm{e}}$ and $\varepsilon''_{\mathrm{e}}$, respectively ($j^2 = -1$).

The effective electric permittivity of a capped CPW transmission line can be calculated using Eq. (2.39) in Simons [11]

$$\widehat{\varepsilon}_{\mathrm{e}} = 1 + q_3 \left(\varepsilon_{\mathrm{r1}} - 1\right) \quad , \tag{3.2}$$

where q_3 is the partial filling factor dependent on the device geometry [see Eq. (2.40) in Simons [11]] and $\varepsilon_{\mathrm{r1}} = \varepsilon'_{\mathrm{r1}} - j\varepsilon''_{\mathrm{r1}}$ is the relative electric complex permittivity of the base chip substrate (in our case silicon) with thickness h_1. Hereafter, we assume $h_1 \to \infty$ (a

Table 3.4: Resonator parameters. n: Resonator number. f_0, Q_{c}^*, and Q_{i}, and $\widehat{f}_0$, $\widehat{Q}_{\mathrm{c}}^*$, and $\widehat{Q}_{\mathrm{i}}$: Measured resonance frequency, rescaled coupling quality factor, and internal quality factor for uncapped and capped resonators, respectively. The fitting procedure is outlined in Béjanin *et al.* [27] The nominal frequencies of the uncapped resonators are $f_0 = \{4.2, 4.5, 4.7, 5.0, 5.2, 5.7, 6.2, 6.7, 7.2\}$ GHz. For all measured resonators $\widehat{Q}_{\mathrm{c}}^* \ll Q_{\mathrm{c}}^*$, indicating the capped resonators are coupled stronger to the feed line than the corresponding uncapped ones. Thus, we expect $\widehat{f}_0 < f_0$, denoting a frequency redshift.

n	f_0 (GHz)	Q_{c}^*	Q_{i}	$\widehat{f}_0$ (GHz)	$\widehat{Q}_{\mathrm{c}}^*$	$\widehat{Q}_{\mathrm{i}}$
1	4.252	186510	37433	4.033	9916	20212
2	4.448	46057	52250	-	-	-
3	4.722	140890	41780	-	-	-
4	4.913	49352	44551	-	-	-
5	5.388	-	-	4.982	5698	22501
6	5.853	-	-	5.872	-	-
7	6.320	-	-	-	-	-
8	-	-	-	6.921	-	-
9	-	-	-	-	-	-

reasonable approximation as the silicon substrates are 500 µm thick, much thicker than any of the other structures). Note that Eq. (3.2) is applicable as the tunnel sidewalls are much farther away from the conductor than the in-plane ground planes, $T \gg H$ (see Fig. 3.1).

Inserting Eq. (3.2) into Eq. (3.1), we obtain the capped internal quality factor

$$\widehat{Q}_\mathrm{i} = \frac{1 + q_3\,(\varepsilon'_\mathrm{r1} - 1)}{q_3 \varepsilon''_\mathrm{r1}} \quad . \tag{3.3}$$

In the case of an uncapped CPW transmission line, the effective electric permittivity is given by [11]

$$\varepsilon_\mathrm{e} = \frac{1 + \varepsilon_\mathrm{r1}}{2} \tag{3.4}$$

and the uncapped internal quality factor is given by

$$Q_\mathrm{i} = \frac{1 + \varepsilon'_\mathrm{r1}}{\varepsilon''_\mathrm{r1}} \quad . \tag{3.5}$$

The ratio between the uncapped and capped internal quality factors is thus

$$\frac{Q_\mathrm{i}}{\widehat{Q}_\mathrm{i}} = \frac{(1 + \varepsilon'_\mathrm{r1})\,q_3}{(\varepsilon'_\mathrm{r1} - 1)\,q_3 + 1} \quad . \tag{3.6}$$

Using the dimensions S, W, and $h_4 = H$ reported above and assuming $\varepsilon'_\mathrm{r1} = 11$ for silicon, we find $q_3 \simeq 0.4722$ and, thus, $Q_\mathrm{i}/\widehat{Q}_\mathrm{i} \simeq 0.99$. As a consequence, the increase in vacuum participation due to the addition of the cap increases the internal quality factor by approximately 1 %. This is a very small effect for the devices presented in this work, where other loss mechanisms such as aluminium interdiffusion, the presence of indium oxide (and likely aluminium oxide) on both the base and cap chips, the low quality of the sputtered thin films, and, possibly, the bonding procedure itself outweigh the benefits of a higher vacuum participation. However, a careful design and a suitable fabrication and cleaning process may be used to take advantage of this effect to make capped devices (e.g., qubits) with lower error rates than similar uncapped devices [55].

3.8 Conclusions and outlook

In conclusion, we develop and characterize a thermocompression bonding technology in vacuum using indium thin films as bonding agent. Our results show that this technology

can be readily used to implement an integrated multilayer architecture, combining the fabrication advantages of two-dimensional superconducting qubits [50] and the long coherence of micromachined three-dimensional cavities [35]. This bonding technology is compatible with the quantum socket design, paving the way toward the implementation of extensible quantum computing architectures as proposed by Béjanin *et al.* [27]

Chapter 4

Thin film metrology and microwave loss characterization of indium and aluminum/indium superconducting resonators

The majority of this chapter was submitted on 2017 December 22 as:

McRae, C.R.H., Béjanin, J.H., Earnest, C.T., McConkey, T.G., Rinehart, J.R., Deimert, C., Thomas, J., Wasilewski, Z.R., Mariantoni, M. Thin Film Metrology and Microwave Loss Characterization of Indium and Aluminum/Indium Superconducting Planar Resonators. *J. Appl. Phys.* (2017).

The list of contributions to this work can be found in the Statement of Contributions within the front matter of this thesis.

Scalable architectures characterized by quantum bits (qubits) with low error rates are essential to the development of a practical quantum computer. In the superconducting quantum computing implementation, understanding and minimizing materials losses is crucial to the improvement of qubit performance. A new material that has recently received particular attention is indium, a low-temperature superconductor that can be used to bond pairs of chips containing standard aluminum-based qubit circuitry. In this chapter, we characterize microwave loss in indium and aluminum/indium thin films on silicon substrates by measuring superconducting coplanar waveguide resonators and estimating the main loss parameters at powers down to the sub-photon regime and at temperatures between 10 and 450 mK. We compare films deposited by thermal evaporation, sputtering,

and molecular beam epitaxy. We study the effects of heating in vacuum and ambient atmospheric pressure as well as the effects of pre-deposition wafer cleaning using hydrofluoric acid. The microwave measurements are supported by thin film metrology including secondary-ion mass spectrometry. For thermally evaporated and sputtered films, we find that two-level states (TLSs) are the dominating loss mechanism at low photon number and temperature. Thermally evaporated indium is determined to have a TLS loss tangent due to indium oxide of $\sim 5 \times 10^{-5}$. The molecular beam epitaxial films show evidence of formation of a substantial indium-silicon eutectic layer, which leads to a drastic degradation in resonator performance.

4.1 Introduction

The experimental realization of a quantum computer [5] with hundreds of quantum bits (qubits), i.e., a medium-scale quantum processor, is on the cusp of becoming a reality. Superconducting quantum computing [50] has already demonstrated the low error-rate control and measurement of nine qubits [44] and has all the fundamental attributes required to progress to medium-scale integration in the near future [60].

As larger arrays of superconducting qubits become viable, multilayer architectures such as the multilayer microwave integrated quantum circuit [54] and the three-dimensional integrated quantum processor [61] become attractive options for extending current systems. Multilayer architectures are largely composed of two or more on-chip circuits connected by through-silicon vias [62, 63] and indium (In) bump bonds [42, 55, 61, 62]. Alternatively, pairs of chips can be attached by means of thermocompression bonding of thick film In in ambient atmospheric pressure below the In melting temperature [37] or thin film In in vacuum above the In melting temperature [1]. Indium is thus becoming an important material to create compact, densely connected, and environment-protected quantum systems. A detailed characterization of loss mechanisms of In thin films is therefore an important step toward a medium-scale quantum processor.

In this chapter, we study planar superconducting resonators made from In thin films deposited both by thermal evaporation and, separately, grown by molecular beam epitaxy (MBE), as well as resonators made from sputtered aluminum/indium (Al/In) thin films. All films are deposited on silicon (Si) substrates. We find that all devices except for the MBE samples are limited by two-level state (TLS) loss at the typical excitation power and temperature used in superconducting quantum computing applications. The MBE samples are limited by interdiffusion mechanisms and perform significantly worse than all other samples, which, instead, are likely limited by the intrinsic loss due to native In oxide.

This chapter is organized as follows. In Sec. 4.2, we give a brief historical excursus of the extensive body of work on dissipation in superconducting planar resonators and provide the motivation for this work. In Sec. 4.3, we describe the In and Al/In film deposition methods and planar resonator fabrication process. In Sec. 4.4, we present a detailed characterization of the samples by means of thin film metrology. In Sec. 4.6, we report the quality factor and resonance frequency as a function of both power and temperature for a set of resonators. In Sec. 4.7, we discuss the main results of this work. Finally, in Sec. 4.8, we draw our conclusions and outline possible future work.

4.2 Loss mechanisms and motivation

The pursuit of understanding loss mechanisms in thin film technology began in the early stages of superconducting qubit implementations [64] and has led to major improvements in the quality factor of planar superconducting resonators [65, 66] and coherence time of qubits [67–69]. Resonators are particularly amenable to the study of thin film dissipation, which can be quantified from simple transmission-coefficient measurements by estimating the resonator intrinsic (or internal) quality factor Q_i, [9, 70] where $1/Q_\mathrm{i} = 1/Q_\mathrm{c} + 1/Q_\mathrm{d}$. This quantity accounts both for conductor loss $1/Q_\mathrm{c}$ and for dielectric loss $1/Q_\mathrm{d} = \tan\delta$, also known as the *loss tangent*. Typically, $\tan\delta \simeq \epsilon''/\epsilon'$, where ϵ' and ϵ'' are the real (lossless) and imaginary (lossy) part, respectively, of the absolute complex electric permittivity of the dielectric [9]. For superconductors, $1/Q_\mathrm{c}$ is determined by effects such as quasiparticles, vortices, metal surface roughness, and radiative losses, while $\tan\delta$ is determined by effects such as dielectric relaxation and the distribution of TLS defects in the dielectric bulk or surface. The TLSs contribution to $\tan\delta$ has been identified as one of the dominant extrinsic dissipation channels in superconducting qubits operating at very low temperature ($T \sim 10\,\mathrm{mK}$) and low excitation power (equivalent to a mean photon number $\langle n_\mathrm{ph}\rangle \sim 1$) [64]. Under these conditions, the TLSs are unsaturated allowing for the interaction with the qubit states resulting in unwanted dynamics.

The investigation of TLSs in amorphous solids, glasses, and spin glasses at low temperature has occupied a prominent role in condensed matter physics [**Anderson1971**, 18, 71]. The models developed in those contexts have been adapted to examine loss due to TLSs in on-chip superconducting devices. Coplanar waveguide (CPW) resonators made from aluminum (Al) and niobium (Nb) conductors patterned on various dielectric substrates have been characterized in studies by Gao *et al.* [72] and Kumar *et al.*, [73] where TLSs were conjectured to be hosted in either the bulk substrate or native oxide at the substrate-metal (SM), metal-air (vacuum) (MA), and substrate-air (vacuum) (SA) inter-

faces. Experimental evidence for a TLS surface distribution has been later shown in works by Gao *et al.* [74, 75] While a series of studies initially pointed out that TLS loss can be mainly attributed to the MA interface (e.g., native metal oxides), [76–78] it has been later calculated that, for typical conditions, the filling factor F [9] for the SM and SA interfaces can be up to two orders of magnitude larger than that of the MA interface [79]. This suggests that the MA loss $F_{\mathrm{MA}} \tan\delta_{\mathrm{MA}}$ dominates the total loss $F \tan\delta$ only if the intrinsic MA loss $\tan\delta_{\mathrm{MA}}$ is significantly higher than all other intrinsic losses.

The theoretical estimates of Wenner *et al.* [79] have confirmed some of the findings in a previous work by Wisbey *et al.*, [80] where it has been reported that an oxide strip by means of hydrofluoric acid (HF) of a Si substrate prior to Nb deposition can significantly decrease the total TLS loss $F \tan\delta_{\mathrm{TLS}}$. Further evidence corroborating these results has been presented in the study by Megrant *et al.*, [65] where the fabrication process of Al CPW resonators was optimized to reduce any SM and SA interface contamination by way of thermal desorption and activated oxygen clean of sapphire substrates in an ultra-high vacuum (UHV) environment. The same work suggests that the MBE growth of Al on sapphire may also lead to slightly lower loss. Very detailed experiments on loss due to substrate interfaces have been recently reported both for qubits [69] and for resonators [66].

The main objective of this work is to characterize the loss mechanisms of In and Al/In CPW resonators on Si substrates. We study resonators with resonance frequency $f_0 \in (4, 8)\,\mathrm{GHz}$, both at high and low photon number (sub-photon regime) and operated at a temperature $T \in (10, 450)\,\mathrm{mK}$. Assuming

$$\frac{1}{Q_{\mathrm{i}}\left(\langle n_{\mathrm{ph}}\rangle, T\right)} = F \tan\delta_{\mathrm{TLS}}\left(\langle n_{\mathrm{ph}}\rangle, T\right) + \frac{1}{Q^*}\,, \tag{4.1}$$

we estimate $F \tan\delta_{\mathrm{TLS}}$ from the photon number dependence of Q_{i} at low temperature. Additionally, we estimate the total TLS loss at zero photon number and zero temperature, $F \tan\delta^0_{\mathrm{TLS}}$, by fitting the temperature dependence at low photon number of $1/Q_{\mathrm{i}}$ and f_0 to the TLS model of Eqs. (4.3) and (4.4), respectively. Finally, we compare the TLS loss to all other losses $1/Q^*$, which we obtain both as a constant offset fitting parameter of the TLS model in Eq. (4.3) and from $1/Q_{\mathrm{i}}$ at high photon number.

4.3 Film deposition and fabrication

A series of five In and two Al/In films are deposited and patterned for this study. A list of these films and their main features is reported in Table 4.1.

Thermally evaporated In films are deposited in a general-purpose custom thermal evaporator at the Nanotech Nanofabrication Facility of the University of California at Santa Barbara. This evaporator is also used to deposit gold, tin, and other materials with a low melting temperature or high contamination risk. The films are deposited from a 99.99 % pure In shot, with a filament voltage between 20 and 25 V, a deposition rate between 10 and 15 Å s^{-1}, and a wafer temperature during deposition of less than 100 °C. The deposition system is evacuated to $< 8 \times 10^{-8}$ mbar prior to deposition and allowed to cool down after deposition for 20 min before venting.

MBE In films are deposited in an UHV system from Veeco Instruments Inc., model GEN10 MBE System at the University of Waterloo. The wafers used for the growth are pre-cleaned by a two-stage outgassing process consisting of a 200 °C anneal in a load-lock followed by a 700 °C anneal in a preparation chamber. An oxide desorption process is conducted by further annealing the wafers in the growth chamber at 1040 °C, as measured by a thermocouple.

Table 4.1: Description of In and Al/In films characterized in this experiment. "Deposition and metal(s):" Type of deposition and metal or metals deposited onto sample, in order of deposition. "Other processing:" Extra steps performed on sample either before or after deposition. "Design:" CPW transmission line design type 1 or 2. "t_1; t_2:" Deposited film thickness for Al and In, respectively. "TE:" Thermally evaporated film (i.e., unprocessed film). "Heated:" Post-patterning heating in ambient atmospheric pressure. "HF:" Predeposition cleaning with RCA SC-1 and HF dip. "S:" Sputtered film (i.e., unprocessed film). "Heated Vacuum:" Post-patterning heating in vacuum. "MBE:" Molecular beam epitaxial film. "Annealed:" Post-deposition annealing in UHV. Thermally evaporated and sputtered films are deposited on high-resistivity ($> 10\,\mathrm{k\Omega\,cm}$) 500 µm thick 3-in. float-zone (FZ) undoped Si (100) wafers; MBE films are deposited on 3-in. Si (001) wafers.

Deposition and metal(s)	Other processing	Design	t_1; t_2 (nm); (nm)
TE In	—	2	0; 1000
TE In	Heated	2	0; 1000
TE In	HF	2	0; 1000
S Al/In	—	1	150; 150
S Al/In	Heated Vacuum	1	150; 150
MBE In	—	2	0; 1000
MBE In	Annealed	2	0; 1000

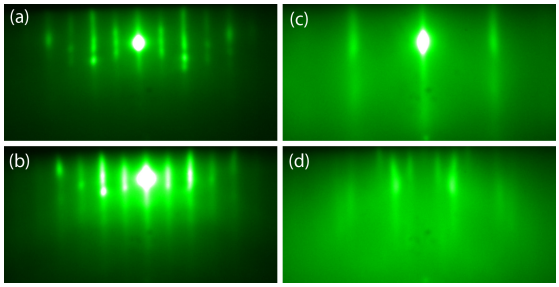

Figure 4.1: RHEED images. (a) Si wafer during oxide desorption at 1010 °C (after pre-cleaning). (b) Si wafer after oxide desorption and after cooling to $\sim$ 0 °C. (c) and (d) Immediately post-growth images for the MBE In and MBE In annealed films, respectively. The film in (d) shows a polycrystalline pattern during growth, with the shown image being captured after additional annealing. The hazy background may indicate the presence of a disordered phase in addition to the single-crystal phase.

During oxide desorption, the surface reconstruction is monitored by means of an *in situ* reflection high-energy electron diffraction (RHEED) apparatus comprising a 12 keV electron gun from STAIB INSTRUMENTS, Inc., model RHEED-12, and a RHEED monitoring element from k-Space Associates, Inc., model kSA 400. The latter allows us to capture diffraction images at selected azimuths during wafer rotation. After achieving a sharp and steady (2×1) surface reconstruction RHEED pattern [see Fig. 4.1 (a)], the wafer is annealed for another 15 min, then cooled to 400 °C and kept at this temperature for several hours until the background pressure in the growth chamber drops below $\sim 2 \times 10^{-10}$ mbar. The wafer is subsequently ramped to room temperature, at which point the power to the manipulator heater is interrupted and the manipulator is allowed to cool down overnight, resulting in a wafer temperature below 0 °C. This process leads to a mostly atomically clean Si starting surface, as confirmed by the clear Si $(001) - (2 \times 1)$ surface reconstruction [see Fig. 4.1 (b)].

The In films are deposited at a rate of 2 Å s^{-1}. Film growth is initiated with a wafer temperature below 0 °C; the wafer temperature rises to approximately room temperature during growth as a result of radiative heating from the In effusion cell. Notably, such a deposition temperature is (in Kelvin) more than 60 % of the In melting temperature (157 °C at ambient atmospheric pressure). This may lead to significant migration of In on the Si surface not only during growth, but also during storage in UHV. One of the two MBE films is annealed briefly at $\sim$ 100 °C immediately after growth, while still in the MBE chamber (see Table 4.1). The samples are kept in UHV overnight before being withdrawn from the MBE system, after which native In oxide begins to grow on the In film surface,

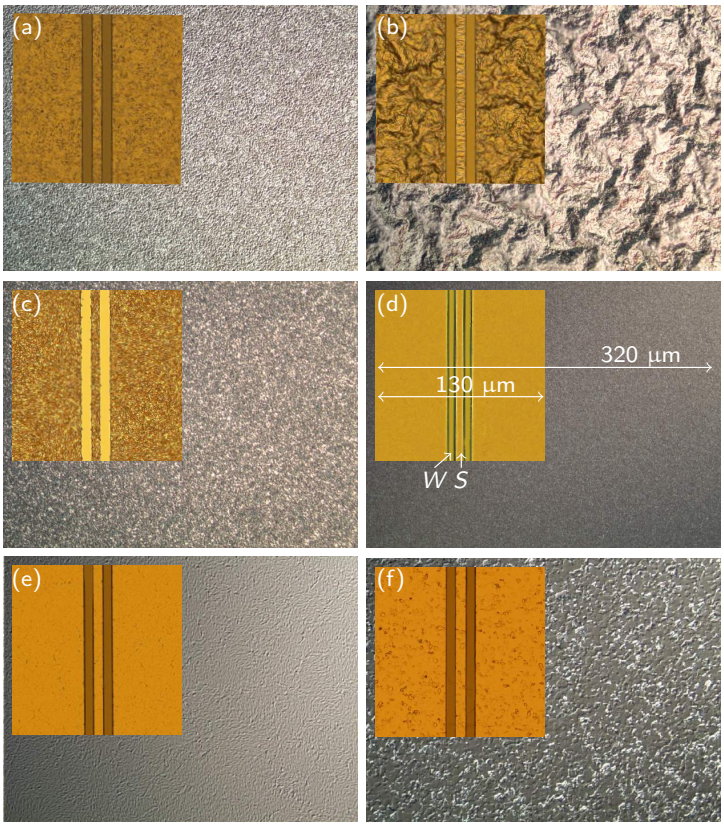

Figure 4.2: DIC microscopy (background) and standard optical microscopy (insets) of In and Al/In sample surfaces, showing surface and device edge roughness, respectively. Standard microscope images show a CPW transmission line running top to bottom with gaps exposing the Si substrate. Samples shown are thermally evaporated In in (a), thermally evaporated In heated in (b), thermally evaporated In HF in (c), sputtered Al/In in (d), MBE In in (e), and MBE In annealed in (f). Sample details are reported in Table 4.1.

preventing further atom migration and the morphological evolution associated with it. For all samples, no intentional post-growth oxidation is performed.

CPW transmission line and resonators are defined by optical lithography followed by a wet etch in Transene type A Al etchant, which successfully etches In as well as Al. Etch times are modified depending on the film type, with thermally evaporated films requiring a wet etch duration of 90 s and MBE films requiring a shorter etch of 60 s.

After patterning, the thermally evaporated In heated sample is processed by placement

on a hot plate at a temperature of 190 °C for 5 min in ambient atmospheric pressure.

Prior to film deposition, the thermally evaporated In HF sample is submitted to a cleaning of the Si wafer surface using a 15 min "RCA" Standard Clean-1 (RCA SC-1) process, [81] immediately followed by removal of the native Si oxide thin film with a 1 min bath in buffered oxide etchant containing 1 % HF acid (or *HF dip*). The sample is loaded into vacuum in the thermal evaporator within 20 min of the completion of the HF dip.

Sputtered Al/In films are deposited *in situ* in a sputter system from AJA International, Inc., model ATC-Orion 5 at the Toronto Nanofabrication Centre of the University of Toronto (deposition parameters can be found in Chapter 3).

The sputtered Al/In heated sample is processed in a custom-made vacuum chamber evacuated to 1×10^{-2} mbar that is placed for a time of 100 min on a hot plate at 190 °C, above the In melting temperature (details on the vacuum chamber in Chapter 3).

Each film is patterned to form a series of meandered quarter-wave resonators capacitively coupled to a feed CPW transmission line in a multiplexed design (see inset of Fig. 4.6) [27]. The resonators feature a center conductor of width S and gaps of width W, as illustrated in the inset of Fig. 4.2 (d). For the transmission lines and resonators in design 1, $S = 15\,\mu$m and $W = 9\,\mu$m, and in design 2, $S = 12\,\mu$m and $W = 6\,\mu$m.

Electrical contact to the input and output pads of the feed line occurs through three-dimensional wires [27]. Due to the low scratch hardness of In films, we deposit a $t_2 = 1\,\mu$m thick In film for the In-only samples to ensure a good electrical connection. In fact, samples featuring a single 150 nm thick In layer exhibit an exceedingly high contact resistance that makes microwave measurements impossible. The Al/In films, on the other hand, are comprised of a $t_1 = 150$ nm thick Al film and a $t_2 = 150$ nm thick In film; in this case, the presence of the Al layer guarantees a good electrical connection to the three-dimensional wires.

4.4 Thin film metrology

In this section, we study the surface morphology and crystallinity of the samples reported in Table 4.1 (see Subsec. 4.4.1), Si/In interdiffusion (see Subsec. 4.4.2), and surface oxides (see Subsec. 4.4.4).

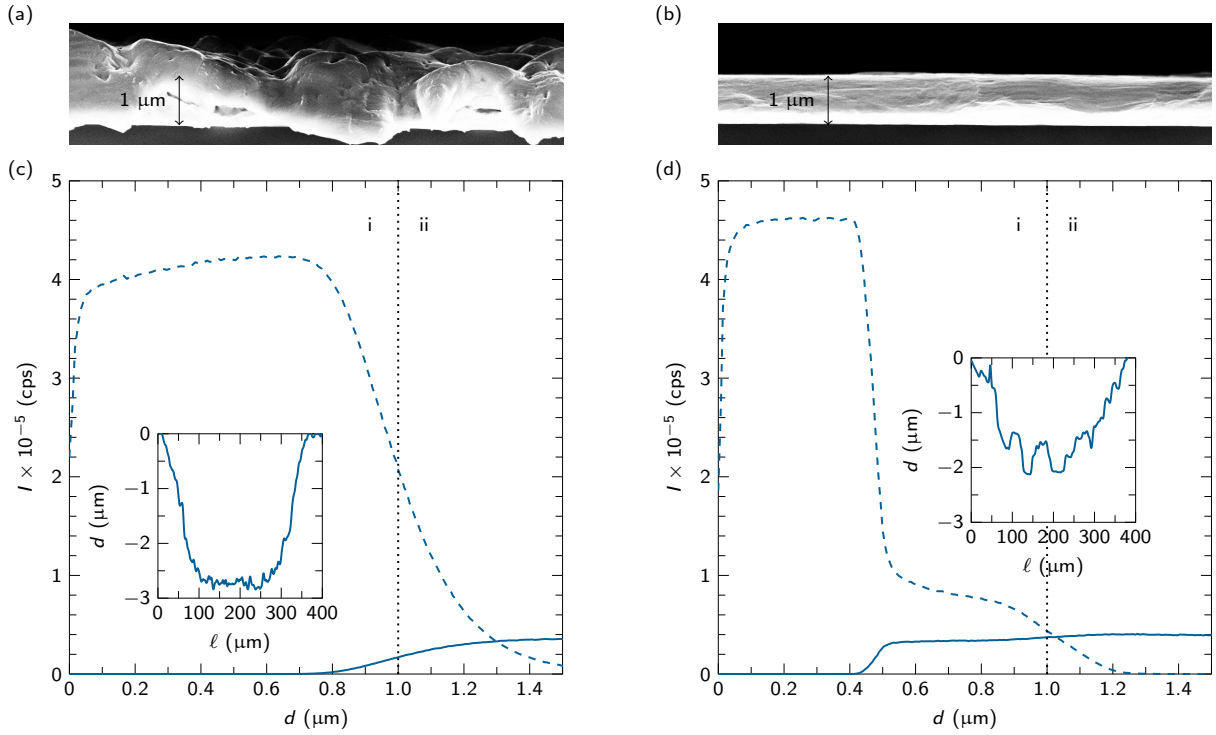

Figure 4.3: Characterization of In/Si interdiffusion. SEM image of a cleaved thermally evaporated In HF sample (a) and MBE In sample (b). D-SIMS depth profiling for the thermally evaporated In HF sample (c) and MBE In sample (d) showing measured intensity in counts per second (cps), I, vs. depth, d. Solid lines: Si counts; dashed lines: In counts. Layer i: 1 µm deep In layer; layer ii: Top part of Si substrate. Layer separation indicated by vertical dotted black lines. The insets show the D-SIMS crater profile plotted as depth d vs. crater diameter, ℓ.

4.4.1 Surface morphology and crystallinity

Both differential interference contrast (DIC) and standard optical microscopy of the surface of the samples in Table 4.1 (except for the sputtered Al/In heated vacuum sample) are performed, as shown by the images in Fig. 4.2. DIC microscopy allows the characterization of the surface roughness, whereas standard microscopy is used to verify the smoothness of the main features of CPW lines.

DIC surface microscopy shows extreme roughness on the surface of the thermally evaporated In heated film [see Fig. 4.2 (b)] and significant roughness on the MBE In film.

Roughness on the MBE In film indicates a resemblance to atomically flat insertions blended into a rough, highly textured granular surface. The thermally evaporated In and thermally evaporated In HF films show minor roughness, while the sputtered Al/In and the MBE In annealed films demonstrate very little roughness.

Standard optical microscopy shows signs of roughness on the device edges of the thermally evaporated In HF sample, likely due to the granularity of the film surface itself. Standard microscopy of all other samples shows smooth device edges.

The two MBE In films are extensively characterized throughout the growth by means of *in-situ* RHEED imaging. Pre- and post-growth surface diffraction patterns are displayed in Fig. 4.1. The RHEED beam footprint is 5 mm × 0.2 mm, with an angle of incidence of 2°.

RHEED imaging of the MBE In film shows a well-defined (1×1) reconstruction throughout the latter stages of the growth, indicating the presence of a single-crystal phase [see Fig. 4.1 (c)]. Measurements of the MBE In annealed film during growth, but before annealing, show a complex RHEED pattern indicative of polycrystalline growth. After annealing in the MBE UHV chamber, RHEED streaks appear although the background remains hazy and the overall intensity drops [see Fig. 4.1 (d)]. This is suggestive of a single-crystal phase coexisting with a disordered phase.

4.4.2 Silicon/indium interdiffusion

The interdiffusion of Si and In for the thermally evaporated In HF sample and MBE In sample is characterized by means of scanning electron microscope (SEM) imaging and dynamic-secondary-ion mass spectrometry (D-SIMS), as shown in Fig. 4.3. SEM allows us to examine a cross section of each sample, while D-SIMS provides information about the layer composition as a function of depth.

SEM images are taken by cleaving a sample and imaging it at a 90° angle, i.e., examining the sample cross section that nominally comprises an In layer above the Si substrate. We use a field-emission (FE) SEM from Carl Zeiss AG, model LEO FE-SEM 1530. All images are taken with a 10 kV acceleration voltage. The resulting images are shown in Fig. 4.3 (a) and (b). The thermally evaporated In HF film is significantly rougher than the MBE In film, which is extremely smooth. However, the thermally evaporated In HF film is still sufficiently homogeneous to allow for a reliable D-SIMS measurement.

We perform D-SIMS measurements in two different regions of each sample. For all samples, both measurements show similar results. The results for one region of each sample are shown in Fig. 4.3 (c) and (d). The samples are analyzed with an ion microprobe

from Cameca - AMETEK, Inc., model IMS 6f using a positive oxygen beam and monitoring positive secondary ions of interest. The plots show intensity as a function of depth, where the depth scales are obtained by measuring the D-SIMS craters with a surface profilometer from the KLA-Tencor Corporation, model P-10 (see insets). There appears to be substantial interdiffusion between In and Si in the thermally evaporated In HF sample.

The profile for the MBE In sample requires a more careful analysis. While there appears to be significant penetration of Si into the In layer, the profile is inconsistent with that of an interdiffusion process. SEM confirms the presence of a 1 µm In layer on the Si surface, yet D-SIMS shows an abrupt drop in the In count at $\approx 0.5\,\mu m$ followed by a plateau. This significantly reduced count could be attributed to a change in the SIMS matrix effect, which would in turn indicate an abrupt change in the layer composition and structure. We conjecture that, in fact, an In-Si eutectic of substantial thickness has formed at the interface. The appearance of such a distinct phase would explain the relatively flat SIMS plateaus for both Si and In from 0.5 µm to 1.0 µm. Furthermore, the abrupt drop in the In count indicates that the crater roughness [see inset of Fig. 4.3 (d)] is not present at that point in the sputtering process, but could have developed while sputtering an In-Si eutectic at the interface.

4.4.3 Si/Al/In interdiffusion

Figure 4.5 shows D-SIMS measurements of the two sputtered Al/In samples in Table 4.1. The results indicate significant diffusion of Si into the Al layer, possibly leading to dielectric relaxation within the Al layer. In addition, we notice extreme interdiffusion of Al into In up to the surface of the In layer. The sputtered Al/In heated sample shows a slightly higher level of Al diffusion into the Si surface, but otherwise the samples have similar D-SIMS profiles.

4.4.4 Surface oxides

Surface oxides on all unheated samples and non-annealed MBE sample are measured by means of X-ray photoelectron spectroscopy (XPS), with measurement results reported in Table 4.2. XPS allows for reliable measurements of thin oxide layers in the nanometer range, but not of the thicker oxides expected on heated samples.

The samples are analyzed using a spectrometer from Kratos Analytical Ltd, model AXIS Ultra. High-resolution In $3d$ spectra are obtained from a rectangular spot with dimensions $300\,\mu m \times 700\,\mu m$ with a pass energy of 10 eV. High-resolution Si $2p$ spectra are

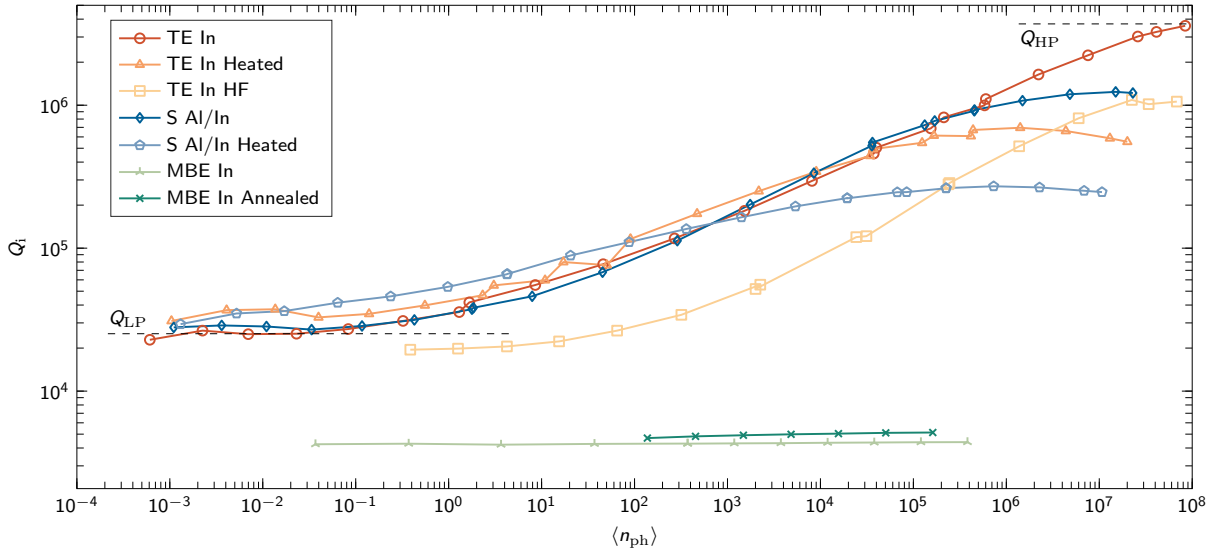

Figure 4.4: Photon number sweeps (S-curves). Intrinsic quality factor Q_i vs. mean photon number $\langle n_{ph} \rangle$ for samples described in Table 4.1. The horizontal dashed black lines indicate the estimated values of the high photon number quality factor Q_{HP} and low photon number quality factor Q_{LP} for the thermally evaporated In sample. The measurement setup and estimation of $\langle n_{ph} \rangle$ are the same as in [27].

obtained from a circular spot with diameter 110 µm with a pass energy of 10 eV; for the Si 2p spectra a region in the CPW gaps is used.

Table 4.2: Surface oxide analysis for all unheated samples and non-annealed MBE sample described in Table 4.1. "Sample:" Sample type (see Table 4.1). "t_{InO}:" Native In oxide thicknesses; "t_{SiO}:" Native Si oxide thicknesses. Two different spots [(A) and (B)] on the Si (gap) surface for the sputtered Al/In sample are measured.

Sample	t_{InO} (nm)	t_{SiO} (nm)
TE In	3.9	0.7
TE In HF	5.1	0.8
S Al/In	4.7	3.4 (A); 6.5 (B)
MBE In	3.1	0.7

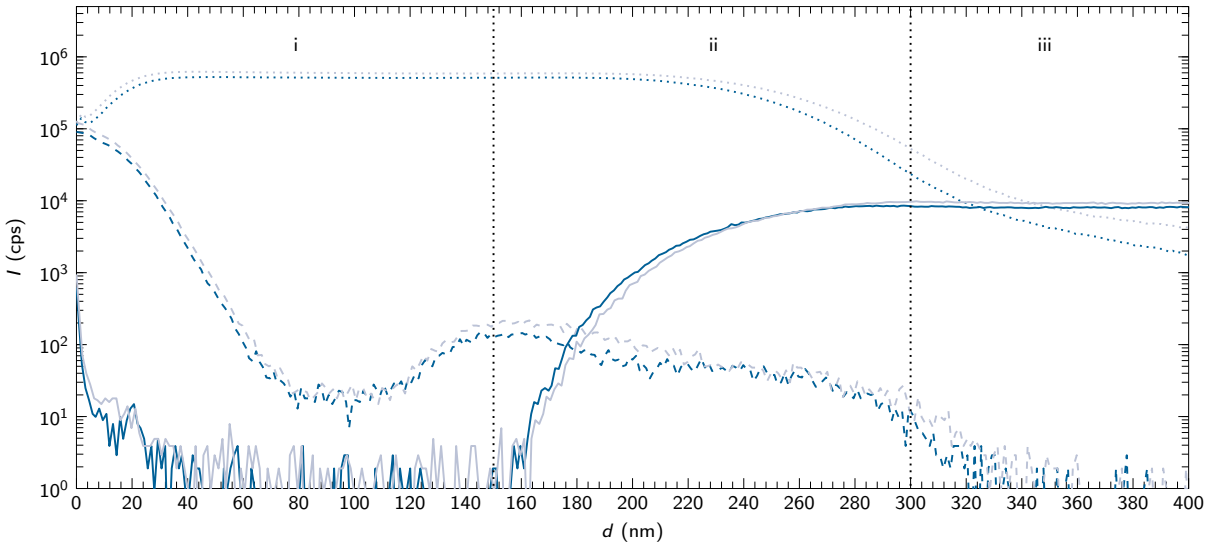

Figure 4.5: Characterization of Si/Al/In interdiffusion. D-SIMS depth profiling for the sputtered Al/In sample [dark blue (dark gray)] and sputtered Al/In heated sample [light blue (light gray)] showing measured intensity in counts per second (cps), I, vs. depth, d. Dashed lines: In counts; dotted lines: Al counts; solid lines: Si counts. Layer i: 150 nm deep In layer; layer ii: 150 nm deep Al layer; layer iii: Top part of Si substrate. Layer separation indicated by vertical dotted black lines.

Using a curve of In oxide thickness as a function of temperature in ambient atmospheric pressure as reported in studies by Kim *et al.* [82] and Schoeller *et al.*, [83] we can estimate the amount of In oxide on all unheated and MBE samples as $\approx 5\,\text{nm}$, confirming the XPS results in Table 4.2. The thermally evaporated In heated sample is heated in ambient atmospheric pressure to 190 °C, thus growing an estimated 20 nm layer of In oxide. The sputtered Al/In heated sample is heated to 190 °C, but at a pressure of $1 \times 10^{-2}\,\text{mbar}$, which likely results in an In oxide layer thinner than 20 nm but thicker than 5 nm. Note that the heated samples are particularly hard to measure directly due to the large surface roughness.

4.5 Circuit layout and transmission-coefficient measurements

For the samples with design 1, the circuit layout comprises a set of nine quarter-wave resonators capacitively coupled to the coplanar waveguide (CPW) transmission line between ports 1 and 2 in a multiplexed design, as shown in the inset of Fig. 4.6. The other two CPW transmission lines in this layout are not used in this work.

For the samples with design 2, the circuit layout comprises two sets of ten quarter-wave resonators, with one set of resonators capacitively coupled to the CPW transmission line between ports 1 and 2, also in a multiplexed design, as shown in the inset of Fig. 4.6. The second CPW transmission line in this layout is not used in this work.

Transmission-coefficient measurements in the frequency range $f \in [4, 8]\,\text{GHz}$ at $T = 10\,\text{mK}$ for each sample in Table 4.1 are shown in Fig. 4.6.

The measurements in Fig. 4.6 demonstrate a stark difference in performance between resonators on thermally evaporated In samples and the two MBE In samples. Out of the ten designed resonators, seven are successfully detected and fitted for thermally evaporated In samples, while only one and two are found for the MBE In and MBE In annealed samples, respectively.

We note that some of the $\|S_{21}\|$ traces of Fig. 4.6 show the presence of unwanted modes, particularly for the sputtered samples. These modes are probably slotline modes due to broken ground planes [25].

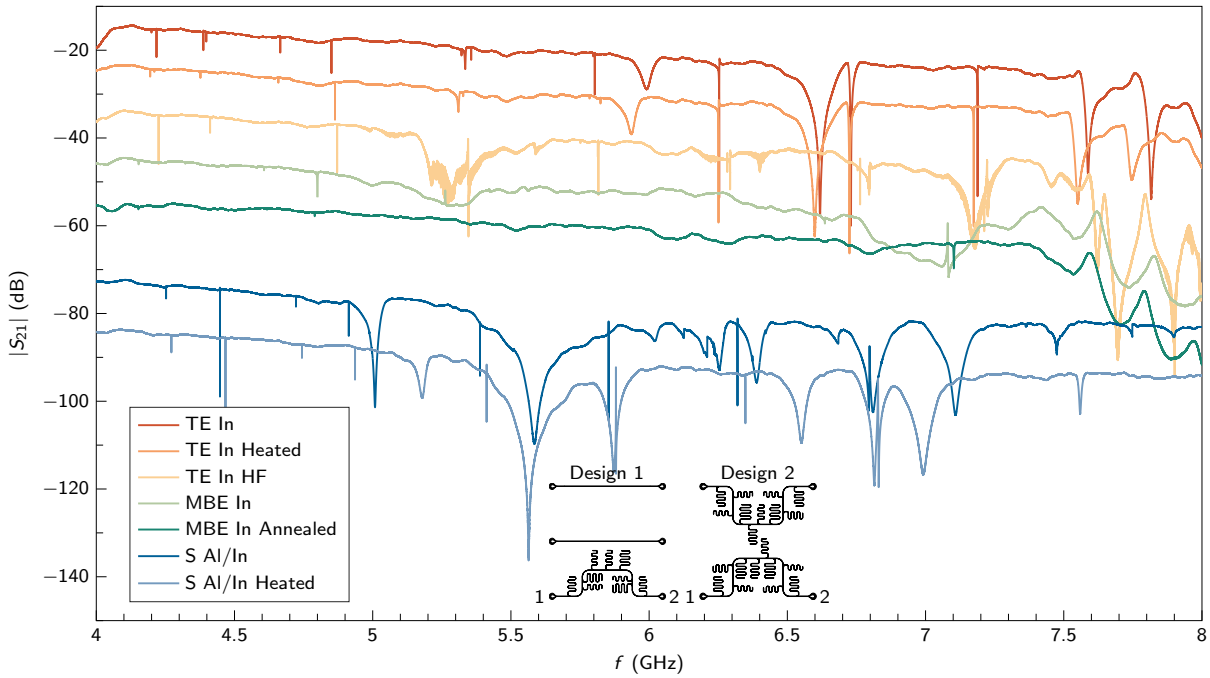

Figure 4.6: Transmission-coefficient measurements. Magnitude of the measured transmission coefficient $\|S_{21}\|$ vs. f. Inset: Circuit layout of design 1 (left) and design 2 (right). In both layouts, the measured CPW transmission lines are those between ports 1 and 2.

4.6 Resonator measurements

In this section, we show the measurement of Q_i and f_0 for comparable resonators on each sample in Table 4.1. The circuit layout for sample design 1 and 2 are drawn in the inset of Fig. 4.6. We present photon number sweeps of Q_i (see Subsec. 4.6.1) as well as temperature sweeps of $1/Q_\mathrm{i}$ and f_0 (see Subsec. 4.6.2), and introduce the TLS theoretical model.

4.6.1 Photon number sweeps

Figure 4.4 shows Q_i as a function of $\langle n_\mathrm{ph}\rangle$ for $T = 10\,\mathrm{mK}$, where Q_i and f_0 are estimated using the fitting procedure explained in [27, 65]. The resonators selected for the photon number sweep have resonance frequency at $T = 10\,\mathrm{mK}$, $f_0 \approx 4.387\,\mathrm{GHz}$ for the thermally evaporated In sample, $f_0 \approx 4.377\,\mathrm{GHz}$ for the thermally evaporated In heated sample, $f_0 \approx 4.412\,\mathrm{GHz}$ for the thermally evaporated In HF sample, $f_0 \approx 4.252\,\mathrm{GHz}$ for the sputtered Al/In sample, $f_0 \approx 4.272\,\mathrm{GHz}$ for the sputtered Al/In heated sample, $f_0 \approx 4.800\,\mathrm{GHz}$ for the MBE In sample, and $f_0 \approx 4.790\,\mathrm{GHz}$ for the MBE In annealed sample. All resonator measurements of thermally evaporated samples correspond to the same designed resonator, as do resonator measurements of sputtered and MBE samples.

At low temperature, where $k_\mathrm{B}T \ll hf_0$ (k_B and h are the Boltzmann and Planck constant, respectively), the functional dependence of $1/Q_\mathrm{i}$ on $\langle n_\mathrm{ph}\rangle$ in the presence of amorphous dielectrics is dictated by TLS saturation above a certain critical mean photon number $\langle n_\mathrm{ph}\rangle^\mathrm{c}$, [20]

$$F\tan\delta_\mathrm{TLS}(\langle n_\mathrm{ph}\rangle) \simeq \frac{F\tan\delta^0_\mathrm{TLS}}{\sqrt{1+\left(\dfrac{\langle n_\mathrm{ph}\rangle}{\langle n_\mathrm{ph}\rangle^\mathrm{c}}\right)^2}}\,. \tag{4.2}$$

Thus, we expect to observe a monotonic decrease of Q_i with $\langle n_\mathrm{ph}\rangle$, as confirmed by the plots in Fig. 4.4. For high $\langle n_\mathrm{ph}\rangle$, Q_i reaches a plateau due to the total saturation of the TLSs where other loss mechanisms dominate, $Q_\mathrm{i} \simeq Q_\mathrm{HP}$ (high photon number quality factor). For low $\langle n_\mathrm{ph}\rangle$, the curve plateaus at $Q_\mathrm{i} \simeq Q_\mathrm{LP}$ (low photon number quality factor) due to the domination of TLS loss in this region, resulting in an S-shaped curve (or *S-curve*). The term $1/Q^*$ in Eq. (4.1) is assumed to be a constant vertical offset of the S-curves.

4.6.2 Temperature sweeps of thermally evaporated In resonators

Figure 4.7 shows the temperature dependence of $1/Q_\mathrm{i}$ and $\Delta\tilde{f}$ at $\langle n_\mathrm{ph}\rangle \sim 1$ for all thermally evaporated samples. Similar plots for the sputtered samples is reported in Fig. 4.5.

At low photon number, $\langle n_\mathrm{ph}\rangle \sim 1$, the functional dependence of $1/Q_\mathrm{i}$ on T is due to the interaction between the resonator and TLSs with frequency distribution centered around f_0 (semi-resonant case), [20]

$$F\tan\delta_\mathrm{TLS}(T) \simeq F\tan\delta^0_\mathrm{TLS}\,\tanh\left(\frac{hf_0}{2k_\mathrm{B}T}\right). \tag{4.3}$$

It can be shown that this relationship is associated with the lossy part of the absolute complex electric permittivity, ϵ'' [20]. We expect to observe a monotonic decrease of $F\tan\delta_\mathrm{TLS}$ with T due to TLS partial saturation activated by thermal photons in the resonator. This behavior is confirmed by the data plotted in Fig. 4.7 (a) that was measured up to $T \approx 450\,\mathrm{mK} \sim T_\mathrm{c}/10$, for an In film superconducting transition temperature $T_\mathrm{c} = 3.4\,\mathrm{K}$; under these conditions the quasiparticle contribution to loss is negligible. Also in this case, $1/Q^*$ is assumed to be a constant offset. Notably, the data for the sputtered samples reveals quasiparticle loss for $T \gtrsim 200\,\mathrm{mK}$ due to the lower superconducting transition temperature of the Al film, $T_\mathrm{c} = 1.2\,\mathrm{K}$ (see Fig. 4.5).

Both at low and high photon number, TLSs with frequency distribution largely detuned from f_0 (dispersive case) have almost no contribution to loss. In this case, the TLSs result in a resonator frequency shift given by [18, 20]

$$\begin{aligned}\Delta\tilde{f}(T) &= \frac{f_0(T) - f^0_0}{f^0_0} = \\ &= \frac{F\tan\delta^0_\mathrm{TLS}}{\pi}\left\{\mathbb{R}\mathrm{e}\left[\Psi\left(\frac{1}{2}+\frac{hf_0}{2\pi k_\mathrm{B}T}\right)\right] - \ln\frac{hf_0}{k_\mathrm{B}T}\right\},\end{aligned} \tag{4.4}$$

where $f^0_0 = f_0(T=0)$, Ψ is the complex digamma function, and $^2 = -1$; the values of f_0 used in this equation are reported in Subsec. 4.6.1. This relationship is associated with the lossless part of the absolute complex electric permittivity, ϵ' [20]. In this case, we expect a non-monotonic relationship between $\Delta\tilde{f}$ and T, [74, 77] which is confirmed by the plots in Fig. 4.7 (b). To avoid any possible contribution to loss other than TLS loss, these measurements are taken at $\langle n_\mathrm{ph}\rangle \sim 1$, although similar results may be obtained at higher photon number [20].

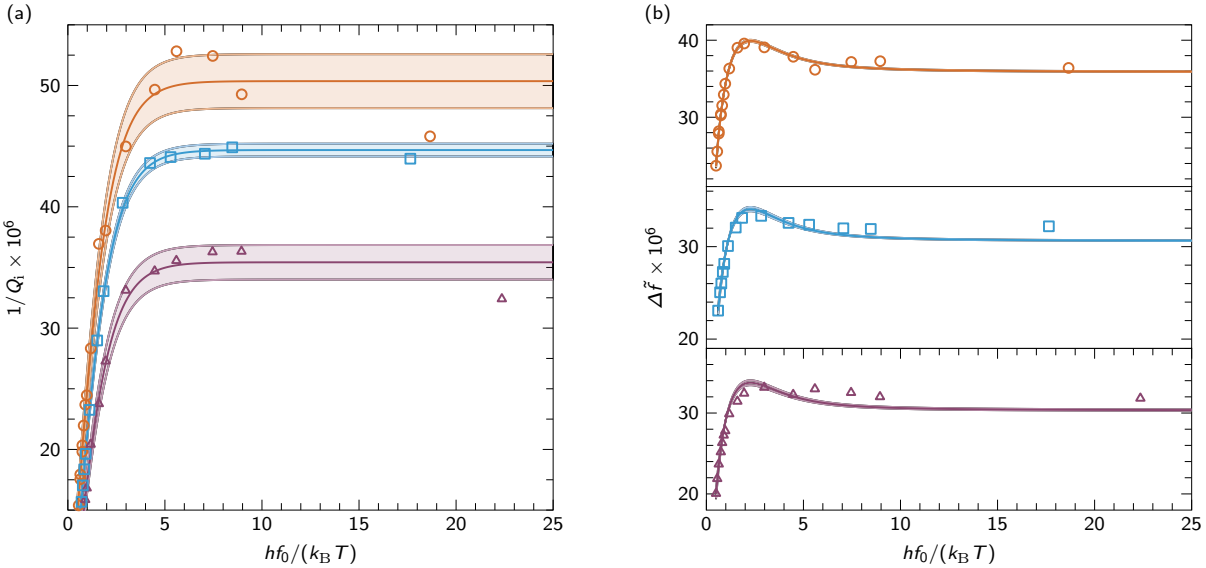

Figure 4.7: Temperature sweeps. Loss tangent $1/Q_\mathrm{i}$ (a) and normalized frequency shift $\Delta\tilde{f}$ (b) vs. $hf_0/(k_\mathrm{B}T)$ for the three thermally evaporated In samples presented in Table 4.1. The resonance frequencies at $T = 10\,\mathrm{mK}$ used in the x-axes are reported in Subsec. 4.6.1. TLS model fitting curves obtained from Eqs. (4.3) and (4.4) (solid lines) with standard deviation bands (shaded areas) are overlaid to data points for unprocessed (open circles), heated (open triangles), and HF (open squares) samples.

4.6.3 Temperature sweeps of sputtered Al/In resonators

Figure 4.8 shows the temperature dependence of $1/Q_\mathrm{i}$ and $\Delta\tilde{f}$ at $\langle n_\mathrm{ph}\rangle \sim 1$ for the two sputtered Al/In samples. The data is overlaid with fitting curves obtained using the TLS theoretical model of Eqs. 4.1, 4.4, and 4.4.

The sputtered Al/In samples do not fit well to the TLS model, possibly due to loss caused by significant interdiffusion of the In and Al layers and Si substrate.

4.7 Results and discussion

The resonator measurements shown in Sec. 4.6 allow us to estimate:

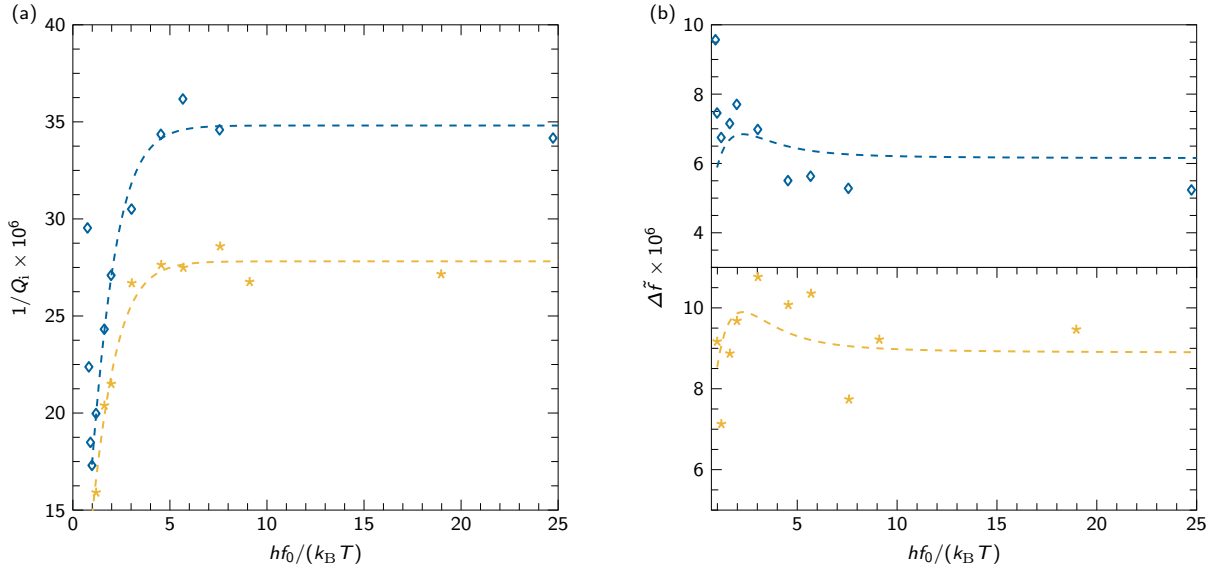

Figure 4.8: Temperature sweeps. $1/Q_\mathrm{i}$ (a) and $\Delta\tilde{f}$ (b) vs. $hf_0/(k_\mathrm{B}T)$ for the two sputtered Al/In samples presented in Table 4.1. TLS model fitting curves (dashed lines) are overlaid to data points for unprocessed (open diamonds) and heated (stars) samples.

1. $F\tan\delta_\mathrm{TLS}$ at $T = 10\,\mathrm{mK}$ as [66, 80]

$$F\tan\delta_\mathrm{TLS} \simeq \frac{1}{Q_\mathrm{LP}} - \frac{1}{Q_\mathrm{HP}}$$

and

$$\frac{1}{Q^*} \simeq \frac{1}{Q_\mathrm{HP}}\,;$$

2. $F\tan\delta^0_\mathrm{TLS}$ and $1/Q^*$ as fitting parameters in Eq. (4.1) with $F\tan\delta_\mathrm{TLS}(T)$ given by Eq. (4.3). This fitting procedure allows us to obtain the fitting curves overlaid to the data in Fig. 4.7 (a), which demonstrate a very good agreement with the TLS model;

3. $F\tan\delta^0_\mathrm{TLS}$ and f_0^0 as fitting parameters in Eq. (4.4). This fitting procedure allows us to obtain the fitting curves overlaid to the data in Fig. 4.7 (b), which also demonstrate a very good agreement with the TLS model.

The estimates for the three thermally evaporated In samples presented in Table 4.1 are reported in Table 4.3. As expected from the design of the samples, the fitted resonance frequencies of the three measured resonators are close to each other, allowing for a fair

comparison between different samples. The three estimated values of the TLS loss tangent for each film are in good agreement, demonstrating consistency between different type of measurements and fitting models. A similar argument applies to the two estimated values of other loss mechanisms for each film, where the only significant discrepancy is for the values of the thermally evaporated In film.

At high $\langle n_{\mathrm{ph}} \rangle$, we find that $1/Q^*$ ranges between $\approx 0.3 \times 10^{-5}$ and $\approx 0.3 \times 10^{-6}$ for all devices except for the MBE samples. The MBE resonators are characterized by low performance and display a practically constant Q_{i} for all values of $\langle n_{\mathrm{ph}} \rangle$. This indicates that the limiting loss mechanism is the presence of an In-Si eutectic phase (see Subsec. 4.4.2) rather than TLS loss. The presence of Si in the eutectic possibly results in dielectric relaxation even within the superconducting film.

At low $\langle n_{\mathrm{ph}} \rangle$, we find that all resonators made from thermally evaporated In films perform similarly, following the TLS model with $F \tan \delta^0_{\mathrm{TLS}} \sim 5 \times 10^{-5}$. This behavior persists for the HF dip devices, where the native Si oxide at the SM interface should be significantly reduced. In all of these devices, the $F \tan \delta^0_{\mathrm{TLS}}$ is approximately five to ten times higher than for the Si/Nb CPW resonators in the study by Wisbey *et al.*, [80] suggesting that the intrinsic loss $\tan \delta_{\mathrm{InO}}$ due to native In oxide at the MA interface is the dominating loss mechanism in all of our In-based resonators. In fact, $\tan \delta_{\mathrm{InO}}$ must be large enough to dominate native Si oxide loss at the SM and SA interfaces, which are characterized by a filling factor significantly larger than the filling factor of the MA interface [79]. It is surprising that devices heated in vacuum and ambient atmospheric pressure, for which the native In oxide layer at the MA interface is expected to be thicker (see Subsec. 4.4.4), are also characterized by $F \tan \delta^0_{\mathrm{TLS}} \sim 5 \times 10^{-5}$.

The resonators made from sputtered Al/In films are characterized by a Q_{i} at low $\langle n_{\mathrm{ph}} \rangle$ on the same order of magnitude as the thermally evaporated resonators. However, the Al/In resonators do not follow the TLS model well. This effect may be caused by Si/Al/In interdiffusion.

It is worth mentioning that our standard Si/Al resonators are characterized by $F \tan \delta^0_{\mathrm{TLS}} \sim 2 \times 10^{-6}$ at $\langle n_{\mathrm{ph}} \rangle \sim 1$, indicating our setup (with similar features as in [84]; see also [27]) is adequate to measure ultra-high quality factor resonators.

4.8 Conclusion

In conclusion, we deposit thermally evaporated In, sputtered Al/In, and MBE In films. We characterize the morphology and crystallinity of these films as well their interdiffusion

Table 4.3: Quantitative analysis of loss mechanisms for the three thermally evaporated In samples. "$1/Q_{\mathrm{i}}(\langle n_{\mathrm{ph}}\rangle)$:" S-curve measurements used to estimate $F\tan\delta_{\mathrm{TLS}}$ and $1/Q_{\mathrm{HP}}$. "$1/Q_{\mathrm{i}}(T)$ Fit:" Temperature sweep measurements used to estimate $F\tan\delta^0_{\mathrm{TLS}}$ and $1/Q^*$ as fitting parameters. "$\Delta\tilde{f}(T)$ Fit:" Temperature sweep measurements used to estimate $F\tan\delta^0_{\mathrm{TLS}}$ and f^0_0 as fitting parameters. Each fitting parameter is reported with its standard deviation.

	$1/Q_{\mathrm{i}}(\langle n_{\mathrm{ph}}\rangle)$		$1/Q_{\mathrm{i}}(T)$ Fit		$\Delta\tilde{f}(T)$ Fit	
	$F\tan\delta_{\mathrm{TLS}}$ $\times10^{-5}$	$1/Q_{\mathrm{HP}}$ $\times10^{-5}$	$F\tan\delta^0_{\mathrm{TLS}}$ $\times10^{-5}$	$1/Q^*$ $\times10^{-5}$	$F\tan\delta^0_{\mathrm{TLS}}$ $\times10^{-5}$	f^0_0 (GHz)
TE In	4	0.03	4.70 ∓ 0.10	0.33 ∓ 0.09	6.1 ∓ 0.1	4.665775
TE In Heated	3	0.20	3.34 ∓ 0.08	0.20 ∓ 0.06	5.2 ∓ 0.3	4.658910
TE In HF	5	0.09	4.36 ∓ 0.03	0.10 ∓ 0.02	5.2 ∓ 0.3	4.411837

and surface oxides. We fabricate CPW resonators and fit Q_{i} as a function of $\langle n_{\mathrm{ph}}\rangle$ and T from transmission-coefficient measurements as well as measure $\Delta\tilde{f}$ as a function of T. We find $F\tan\delta^0_{\mathrm{TLS}}\sim5\times10^{-5}$ and a behavior consistent with TLS dissipation due to the intrinsic loss of native In oxide for all resonators except for the MBE resonators. The MBE resonators do not follow the TLS model; their substantially reduced resonator performance is consistent with the formation of an In-Si eutectic at the interface. Elucidating this phenomenon will be a subject of a future dedicated study.

Further studies will focus on a more quantitative understanding of the native In oxide TLS intrinsic loss and on the role of the MA filling factor for In films. In addition, we plan a set of experiments where we vary both the deposition temperature and the deposition rate of thermally evaporated In films after HF dip. In the case of MBE In deposition on Si, the inclusion of an interdiffusion barrier between the Si and In layers (e.g., a very thin titanium nitride layer) may prevent the migration of Si and the formation of an In-Si eutectic, resulting in a substantial increase in the quality factor of the MBE resonators.

In conclusion, our results indicate that In components with exposed or buried In oxide in a superconducting quantum computer should be limited to the bare minimum and kept far enough from qubits in order to avoid possible qubit degradation.

Chapter 5

Conclusion

In this chapter, the main results of this thesis are summarized and put into the context of the field as a whole, and ideas for next steps are proposed.

5.1 Indium thin film thermocompression bonding for multilayer superconducting quantum circuits

A technique of thermocompression bonding between indium thin films has been developed and characterized. Mechanical bond characterization using scanning acoustic microscopy shows delaminations at the edges of bonded samples, demonstrating that a more homogeneous bonding pressure is required. DC measurements of the bond region show a small but significant residual resistance at superconducting temperatures, likely due to the presence of native indium oxide within the interface as well as significant interdiffusion between the aluminium and indium thin films as demonstrated by secondary ion mass spectrometry (SIMS) measurements.

In the next generation of indium thin film thermocompression bonding, a hydraulic press will be implemented in order to allow a uniform applied pressure and eliminate delaminations at chip edges. An acid buff or plasma clean to remove surface indium oxide, as well as the addition of a titanium nitride diffusion barrier, is expected to suppress the bond's residual resistance at superconducting temperatures and potentially lead to a superconducting bond.

In the future, qubits will be included in the capped quantum circuits and compared

with identical uncapped devices. As well, aluminium will be used for the transmission lines and resonators, with indium only present on ground planes for bonding purposes.

5.2 Thin film metrology and microwave loss characterization of indium and aluminum/indium superconducting resonators

Indium thin films deposited by thermal evaporation and molecular beam epitaxy (MBE) and sputtered aluminium/indium thin films were characterized using surface and cross-sectional imaging techniques as well as by fitting the internal quality factor Q_i of superconducting coplanar waveguide resonators at a variety of powers and temperatures and comparing to the two level system (TLS) model.

Using SIMS, MBE indium films were shown to be highly interdiffused with the silicon substrate surface and demonstrated a low, power-independent Q_i, indicating that loss due to interdiffusion was the dominant form of loss in MBE films. This is likely due to the atomic cleanliness of the silicon surface prior to MBE film deposition

Thermally evaporated indium and sputtered aluminium/indium thin films showed power-dependent behaviour characteristic of TLS loss, and had similar low-power Q_i values. Thermally evaporated indium was fitted to the TLS model and shown to have a TLS loss component of $\sim 5 \times 10^{-5}$, about an order of magnitude higher than similar devices fabricated with niobium [80].

In the future, diffusion barriers such as titanium nitride will be tested during MBE indium growth. Lower MBE growth temperatures and higher deposition speeds will also be tested in order to optimize MBE indium growth and compare to thermally evaporated indium films.

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APPENDICES

Appendix A

Nanofabrication and microfabrication

Fabrication is an essential pillar on which superconducting quantum computing rests. This appendix outlines the fabrication recipes and design techniques used in this work. All fabrication was performed in the University of Waterloo's Quantum NanoFab Facility, except where noted in the text.

A.1 Mask design tips

The photomask (or simply *mask*) is the component often used to introduce the circuit design during the process of photolithography. A mask consists of a glass plate with a thin film of chrome etched with the pattern of interest. During exposure in a mask aligner, the chrome blocks the light from reaching the resist on the wafer below, while the glass allows the light to pass through, thus transferring the pattern from the mask to the resist. 1:1 masks are needed when using a mask aligner. Masks with larger ratios can be used when a stepper is available. Direct writing can also be used, where the 1:1 mask file is written directly onto the sample using a laser, rather than onto a mask to be used with the sample. The following appendix assumes the use of an MA6 mask aligner (Suss-Microtech, Germany).

It is crucial to design photomasks in a thoughtful way in order to make fabrication, alignment, and measurement as straightforward as possible.

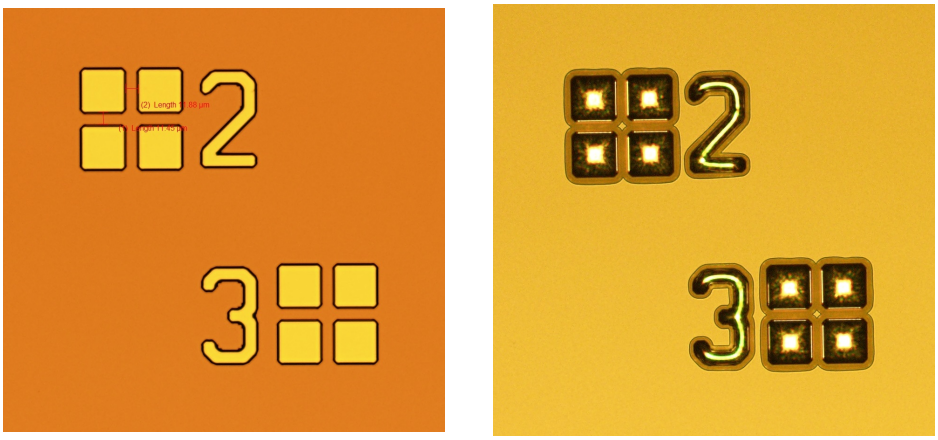

Figure A.1: Microscope images of on-chip alignment markers used to align the tunnels mask and through holes mask during cap chip fabrication (see Appendix A for more details on fabrication). Individual squares are approximately 50 µm long. Left: Alignment markers patterned in resist, post-development and pre-etch. Dark orange: AZ4620 photoresist. Yellow: Silicon wafer surface. Right: Alignment markers after an RIE isotropic etch and resist strip. Yellow: Silicon wafer surface. Black: Etched regions of silicon wafer surface.

A.1.1 Alignment marker design

Alignment markers should be drawn while taking into account the number, order and critical dimension of process layers, as well as the capabilities of the mask aligner. Examples of alignment markers used in experiments in Chapter 3 are shown in Fig. A.1.

Process details

Ensure that the first alignment marker will withstand the processing steps included between the creation of first and second marker. For example, the first alignment marker should be considered during etching and deposition to ensure it is not detroyed before use with the second marker.

There must be an unobstructed view available of the lower (first) marker during alignment with the next marker. If the mask around the second marker is mostly chrome, it will be difficult to find the first marker in order to perform alignment. A window in the chrome may be added around the second alignment marker to facilitate alignment.

Mask aligner details

There are two general types of alignment: local alignment, and global alignment. Local alignment is for lining up two patterns in one small area, while global alignment is used to line up patterns on two full samples.

If alignment markers are intended for global alignment, they should be located strategically in order to take advantage of the MA6's split screen feature. The two cameras on the MA6 have limited mobility, so not every point on a sample's surface may be viewed at the same time as any other. However, alignment becomes closer to trivial if two markers can be aligned in unison.

The MA6 has a viewing area of about 300 µm× 300 µm, and each alignment marker should fit within this area.

A.1.2 Wafer and die manipulation

The cleanroom user will be manipulating the sample (likely with tweezers, but sometime with other tools or even a gloved hand) both as a full wafer and as a diced piece. The mask must reflect this by allowing room to grip the sample without damaging devices or other essential pattern components. It is essential to design each die with a blank area near the edge for gripping, as well as to design a wafer with devices far from the main flat, to leave room for tweezers.

A.1.3 Compatibility with measurement set-up

In order to measure our devices, they must be aligned to the pogo pins in our sample boxes (see the Quantum Socket paper [27] for more details). Alignment is performed by fitting a sample into a box with precise dimensions and securing the box lid which holds the pins. These pins must make contact with pads attached to each circuit. Therefore, the precision of the dicing alignment and cutting must be better than the threshold required for the pins to make contact with the pads. Dicing markers must be designed by taking into account both the precision required and the capabilities of the dicing saw available.

A.2 Silicon wafers

The devices in this work are all fabricated on silicon wafers. Silicon has the advantage of being ubiquitous in the semiconductor industry and thus having many standardized nanofabrication processes and techniques associated with it. Compared to sapphire, another common dielectric used in superconducting quantum computing, silicon is soft and therefore can be easily trenched and diced.

Three different categories of silicon wafers are used in the development and fabrication of devices in this work: device wafers, test wafers, and carrier wafers. The wafers in this work are sourced from El-Cat Inc.[1]

Also called prime wafers, device wafers are the wafers that will be used to fabricate our devices. These wafers have strict requirements in terms of amount of impurities, doping, crystalline orientation, and resistivity, as well as more practical requirements such as diameter, thickness, polishing, and number of flats.

Ideally, one side of the wafer is polished and one side is alkaline etched in order to distinguish between sides of the wafer. One flat is preferred for ease of use of the Teflon claws used in this work to cleanly and precisely submerge wafers and agitate them in liquid. 3 inch wafers are used in this work as they are compatible with all necessary instruments (with the implementation of a carrier wafer in some instances) as well as the chuck used in the molecular beam epitaxy chamber.

Test wafers are cheaper, lower quality wafers used to test fabrication processes. They may also be used for simple electronics testing and room temperature measurements. Test wafer requirements are more lax; they consist of mainly practical requirements such as diameter and thickness. The device and test wafers must be the same thickness when testing through hole fabrication.

Carrier wafers are used in cases where a required instrument cannot hold the wafer or piece size that we have. The sample of interest is attached to the carrier wafer, a low quality wafer of the correct size for the chuck available, before insertion into the instrument. When performing a long etch, the carrier wafer must be thick enough to withstand the full etch without a resist barrier while maintaining its physical stability. 4 inch wafers are used as carrier wafers in order to fit 3 inch wafers into the Oxford reactive ion etch systems.

Wafers are stored on a shelf in the cleanroom or in a nitrogen-filled dessicator in order to avoid contamination.

[1] https://www.el-cat.com/

A.2.1 Intrinsic silicon

Intrinsic silicon (i.e. i-type, or pure, silicon) is silicon that is not doped with any other element such as boron, phosphorous, or arsenic. In intrinsic semiconductors, $n = p$, i.e., the number of excitations n is equal to the number of holes p. Device wafers used in superconducting quantum circuits require a high resistivity substrate ($> 10\,000\,\Omega\,\mathrm{cm}$ at minimum) and impurities such as the above increase dielectric conductivity. At low temperature, intrinsic silicon acts almost as a perfect insulator.

A.2.2 Silicon ingot growth methods

Silicon ingots are grown and melted into various single-crystal orientations. Below are explanations of two common growth methods.

Czochralski zone method

In the Czochralski zone (CZ) method, polycrystals are melted in a container. A seed crystal is introduced which has the desired crystal orientation. The seed is attached to a rod. The rod is slowly pulled out of the melted silicon while rotating.

Float zone method

For our device wafers, float zone (FZ) silicon is necessary. This method creates very pure silicon. It uses a method known as *vertical zone melting* to convert a polycrystal into a single crystal. A polycrystal with a seed crystal on one end is passed vertically through an RF heater. The ingot zone inside the heater melts and reforms into a single crystal with the same orientation as the seed. The melted section is held together by surface tension. This method produces a purer dielectric than the CZ method because it does not require a container for melted silicon, lowering the chance of contamination.

A.3 Appropriate glassware

Pyrex glassware is the cheapest and most commonly used glassware option in cleanroom wetbench processing. However, certain metal-containing solutions known as *alkalis* are known to cause leaching in Pyrex glassware which could lead to sample contamination.

Quartz glassware is used as an alternative for such solutions. However, both Pyrex and Quartz can be deteriorated by hydrofluoric acid, and thus Teflon or PVDF/PFA containers are substituted for use with this liquid.

A.4 Aluminium/indium superconducting quantum circuit process

Distributed element resonators, transmission lines, and bond test pads were fabricated using the aluminium/indium superconducting circuit recipe. Although dry etching of a metallized layer usually produces a more accurate circuit with less roughness, wet etching was used for these samples due to the volatility of indium that prevents it from being allowed in most vacuum systems.

Prior to this recipe, 150 nm aluminium and 150 nm indium are sputtered onto a silicon wafer *in situ*.
A. Circuit photolithography:

1. Spin Shipley MICROPOSIT S1811 Positive Photoresist (S1811) at 500 rpm for 4 sec with a 100 rpm/s acceleration, followed by 5000 rpm for 60 sec with a 500 rpm/s acceleration. This achieves a resist thickness of 1.4 µm.
2. Soft bake at 120 °C for 90 sec on a hot plate.
3. Cool and rehydrate for 10 min.
4. Vacuum contact exposure using Suss-Microtec MA6 Mask Aligner (Suss-Microtec, Germany) for 4 sec.
5. Develop in MICROPOSIT MF-319 Developer for 45 sec, submerge in deionized water (DI) for 1 min, then blow dry immediately and thoroughly with nitrogen gas.

B. Circuit etch:

1. Perform a wet etch with Transene Al Etchant Type A at 50 °C for 60 sec.
2. Submerge sample in DI for 30 sec and rinse, then dry immediately and thoroughly with nitrogen.

3. Do not strip resist, and proceed straight to dicing.

C. Dicing:

1. Tape both sides of wafer with dicing tape. Dicing tape was shown to preserve the delicate aluminium/indium film better than soft-baked resist.

2. Use thorough alignment and precise dicing markers to perform dice to within 10 µm accuracy. This is crucial for sample alignment to 3D wiring.

3. Perform a long UV exposure to remove tape (at least 1800 sec).

D. Photoresist strip:

1. Strip individual dies in acetone for 6 min, then IPA for 30 sec, and then dry immediately and thoroughly with nitrogen.

A.5 Indium superconducting quantum circuit process

The indium-only variation of the recipe in Sec. A.4 begins with a 1 µm thick indium film deposition. Depending on the type of deposition method used, the wet etch time will vary between 60 and 95 seconds. The dicing process is modified to use a second soft-baked coat of S1811 as a protective layer during dicing rather than tape.

A.6 Aluminium/indium cap process

Th caps bonded over the superconducting quantum circuits were fabricated using the below recipe. These samples consist of two layers of design: tunnels and through holes.

For this recipe, a 350 µm thick Si wafer is used. A thinner wafer decreases the Bosch etch time for the through holes, but also leads to a decrease in the mechanical stability of the wafer. During process testing, wafers consistently shattered when using 250 µm thick samples.

A. Sample prep:

1. Perform a hexamethyl disilizane (HMDS) deposition to form a layer of 5 Å.

B. Tunnel photolithography (adds about 2.4 µm to feature width):

1. Spin Microchemicals AZ4620 Positive Photoresist at 500rpm for 8 sec, followed by 3000rpm for 60 sec, achieving a thickness of 8 µm.
2. Soft bake at 90 °C for 20 min in a convection oven.
3. Cool and rehydrate for 30 min.
4. Soft contact exposure with mask aligner for 30 sec.
5. Develop in Microchemicals AZ400K 1:4 Developer for 100 sec, followed by DI for 1 min. Rinse with DI hose and blow dry with nitrogen.

C. Tunnel etch:

1. Perform an isotropic SF6 only Si etch for 3 min in the Oxford Instruments ICP380 Deep Reactive Ion Etcher (Oxford Instruments, UK).

D. Strip and prep:

1. Sonicate in acetone beaker 1 for 5 min, then in acetone beaker 2 for 5 min, then in IPA for 5 min, and dry with nitrogen immediately.
2. Ash sample three times to remove resist residue.
3. Perform an HMDS deposition to form a layer of 5 Å.

E. Through hole photolithography:

1. Spin a 14 µm thick layer of AZ4620 by spinning at 300rpm for 3 sec, and then at 1000rpm for 60 sec.
2. Soft bake at 90 °C for 20 min in a convection oven.
3. Cool 1 min.
4. Spin another 14 µm thick layer of AZ4620 by spinning at 300rpm for 3 sec, and then at 1000rpm for 60 sec.
5. Soft bake again at 90 °C for 20 min in a convection oven.

6. Cool and rehydrate for 30 min.

7. Perform a proximity exposure at 5 µm for 2 min using the mask aligner.

8. Develop in Microchemicals AZ400K 1:4 Developer for 5 min, followed by DI for 1 min. Rinse with DI hose and blow dry with nitrogen.

9. Hard bake at 120^0C for 20 min on a hot plate.

F. Through hole etch:

1. Perform a 700-cycle Bosch etch in the Deep Reactive Ion Etcher with an etch rate greater than 2 µm/ min. This step takes 2.5 h.

G. Strip:

1. Sonicate in acetone beaker 1 for 5 min, then in acetone beaker 2 for 15 min, then in IPA for 10 min, and dry with nitrogen immediately.

2. Ash sample if needed.

H. Sputter 150 nm aluminium followed by 150 nm indium in-situ onto the sample surface.
I. Dicing:

1. Tape both sides of wafer with dicing tape, and use thorough alignment and precise dicing markers to perform dice to within 10 µm accuracy. This is crucial for sample alignment to 3D wiring.

2. Perform a UV exposure for at least 600 sec to remove tape.

A.7 Aluminium superconducting quantum circuits process

Start with an aluminium thin film, whether it be sputtered, e-beam evaporated or MBE, deposited on a silicon substrate.
A. Circuit photolithography:

1. Spin Shipley MICROPOSIT S1811 Positive Photoresist (S1811) at 500 rpm for 4 sec with a 100 rpm/s acceleration, followed by 5000 rpm for 60 sec with a 500 rpm/s acceleration. This achieves a resist thickness of $\sim 1.4\,\mu m$.
2. Soft bake at 120 °C for 90 sec on a hot plate.
3. Cool and rehydrate for 10 min.
4. Vacuum contact exposure using Suss-Microtec MA6 Mask Aligner (Suss-Microtec, Germany) for 4 sec.
5. Develop in MICROPOSIT MF-319 Developer for 45 sec, submerge in deionized water (DI) for 1 min, then blow dry immediately and thoroughly with nitrogen gas.

B. Circuit etch:

1. Using an Oxford Instruments ICP380 Reactive Ion Etcher, perform a 10 min preclean with O_2 and SF_6.
2. Attach wafer to a carrier wafer with pump oil. Using a clean, nonshedding swab, add dots of pump oil to the surface of the carrier wafer and place sample wafer over dots, pressing into place.
3. Load wafer into RIE.
4. Perform an aluminium ICP etch with BCl_3 and Cl_2 gases for 30 sec at 50 °C.
5. Unload wafer from instrument.
6. Quickly remove from carrier and wipe back with acetone to remove pump oil.
7. Immerse in DI water immediately.

C. Photoresist strip:

1. Strip wafers in acetone for 5 min, then a second beaker of acetone for another 10 min, then finally IPA for 5 min, and then dry immediately and thoroughly with nitrogen.

D. Dicing:

1. To create a protective resist coating, spin Shipley MICROPOSIT S1811 Positive Photoresist (S1811) at 500 rpm for 4 sec with a 100 rpm/s acceleration, followed by 5000 rpm for 60 sec with a 500 rpm/s acceleration. Hard bake at 140 °C for 5 min on a hot plate. Repeat for a double coat.

2. Cool for 10 min.

3. Use thorough alignment and precise dicing markers to perform dice to within 10 µm accuracy. This is crucial for sample alignment to 3D wiring.

E. Photoresist strip:

1. Strip wafers in acetone for 5 min, then a second beaker of acetone for another 5 min, then finally IPA for 5 min, and then dry immediately and thoroughly with nitrogen.

A.8 RCA silicon wafer surface cleaning

Wafer cleaning is a crucial step in achieving high quality factor resonators. Clean interfaces free of oxide minimize two level systems which limit device lifetimes at low power. More background about TLSs can be found in Sec. 1.3.

Silicon wafers, which are the most common substrate used in contemporary superconducting quantum circuits, have a native oxide that is often removed prior to film deposition in order to create a clean interface. The region below the oxide can contain implanted metal ions due to the process of wafer formation from ingots, and the oxide surface is often contaminated with organics. More information about silicon wafers can be found in Appendix A.

Three common cleaning processes using in silicon wafer cleaning are the RCA SC-1 process, the hydrofluoric acid (HF) dip, and the RCA SC-2 process. This section will explain the purpose and effects of each cleaning process, as well as some broad process information. For a more detailed process on each of these cleans, see Appendix A.

The *RCA* in RCA clean stands for Radio Corporation of America. The RCA cleans are a set of two cleans, with an optional HF dip between them, developed by Werner Kern. [81, 85] These steps are part of a standard body of processes in the semiconductor industry.

RCA SC-1 description

RCA Standard Clean 1 (SC-1) is used to remove organics and some metals, such as gold, copper, and nickel, from the sample surface. Oxide on the silicon surface prevents the removal of contaminants on the actual wafer surface during this clean.

This process consists of a bath of hydrogen peroxide (H_2O_2), ammonium hydroxide (NH_4OH) and deionized water, heated to 75 °C. It is imperative that quartz glassware is used for this process, as other forms of glassware may leach during this process and further contaminate the sample during submersion. [86]

While hydrogen peroxide works to form a native oxide layer, ammonium hydroxide etches oxide. The total effect is a very slow oxide removal of a few monolayers per minute. [87] The combination of oxide etching and growth is considered to remove impurities from the sample surface as well as slightly below the sample surface. [86]

HF dip description

An HF dip usually consists of a diluted bath of buffered oxide etchant (BOE). BOE is a combination of HF and a buffering agent such as ammonium fluoride (NH_4F), used to increase process control.

The goal of an HF dip is to remove the 1 to 1.5 nm thick native oxide layer present on surface of silicon wafers. HF is also known to slow the regrowth of silicon oxide post-dip. This is due to the passivation of the silicon surface with hydrogen. [88]

Despite passivation, silicon becomes highly reactive after exposure to HF. The collection of organics and other contaminants from liquids and air will begin as soon as the native oxide layer is removed. [85] An HF dip can also lead to direct contamination of the silicon with iron. [81] Finally, although the silicon surface becomes largely hydrogen-terminated, a significant amount of Si-CH_2 bonds are also formed. [88]

RCA SC-2 description

The RCA SC-2 process removes metal ions such as aluminium, iron, and gold from the silicon surface that is now exposed due to the HF dip. Wafers could be exposed to these materials through the diamond saw that is used for cutting silicon ingots into individual waters, or during the wafer surface polishing procedure.

RCA SC-2 consists of a heated bath of hydrogen peroxide (H_2O_2), hydrochloric acid (HCl), and deionized water at 75 °C. This process grows a clean, passivated oxide film that can protect the wafer from future contamination. [81]

Depending on how quickly a silicon wafer can be introduced to a vacuum chamber for thin film deposition, a naked HF-dipped surface or a passivated oxide-covered surface may be more appealing.

A.8.1 RCA SC-1 process

The RCA SC-1 solution consists of 5 parts DI water, 1 part H_2O_2, and 1 part NH_4OH.

Glassware required:

- RCA SC-1 vessel (600 ml beaker)
- H_2O_2 beaker, 600 ml
- H_2O_2 beaker, 25 ml
- NH_4OH beaker, 600 ml
- NH_4OH beaker, 25 ml
- DI water graduated cylinder

The recipe is as follows:

1. Turn on hot plate.
2. Measure 125 ml of water into RCA SC-1 vessel and set aside.
3. Pour H_2O_2 into large beaker, if doing both RCA SC-1 and RCA SC-2, pour enough for both ($\sim$ 50 ml), decant 25 ml into small beaker and add to RCA SC-1 vessel. Set extra H_2O_2 in the back of the wet bench, out of the way.
4. Pour NH_4OH into large beaker, then decant 25 ml into small beaker. Add this to RCA SC-1 vessel and place on a hot plate with the thermometer.
5. Once vessel has reached 75 °C, immerse sample for 10 min.
6. Remove solution from heat and give wafer a quick rinse in DI water bath before transferring it to the HF dip. Sample will be very hydrophilic. It is not necessary for it to be totally dry before transfer to HF because HF solution is mostly water.

A.8.2 HF dip process

The HF dip can consist of 1 - 2% HF for 15 sec to 1 min, or a 1 min bath in 10:1 BOE. 1 min is overkill as the oxide etch rate is quite high compared to the thickness of native silicon oxide, but the etch will essentially terminate at the silicon surface.

HF causes the silicon surface to become hydrophobic, whereas oxidized surfaces are hydrophilic. Therefore, we can determine when oxide no longer remains by observing this transition.

This recipe uses 1% BOE (1 parts 10-1 BOE, 9 parts water).

1. Pour DI water into DI baths and 100 ml graduated cylinder (measure out 90 ml which can then be immediately transferred to the HF vessel).
2. Pour a little more BOE than needed into the empty Teflon beaker.
3. Pour from this beaker into the 10 ml graduated cylinder which is then poured into the vessel.
4. Set timer for 1 min and immerse wafer and Teflon claw in HF. Check wafer to see hydrophilic-phobic visual change. More time is better as silicon is etched very slowly but silicon oxide is etched quickly.
5. Remove wafer and immerse in first DI bath for 2 min. Repeat for other two DI baths.
6. NI dry sample.

A.8.3 RCA-2 process

The RCA SC-2 solution consists of 6 parts DI water, 1 part H_2O_2, and 1 part HCl.

Glassware required:

- RCA SC-2 vessel (600 ml beaker)
- H_2O_2 beaker, 600 ml
- H_2O_2 beaker, 25 ml
- HCl beaker, 600 ml

- HCl beaker, 25 ml
- DI water graduated cylinder

The recipe is as follows:

1. Pour 150 ml DI water into vessel.
2. Turn on hot plate.
3. Pour chemicals into beakers.
4. Pour H_2O_2 then HCl into vessel.
5. Put vessel on hot plate at 70 °C.
6. Immerse sample for 10 min. Remove solution from heat to let cool.
7. Remove sample.
8. Soak sample in 3 successive DI water baths for 2 min each. Dry sample with N2 gun, ensuring no water evaporates off surface.