Design and Fabrication of a Nanofluidic Cell System for High-Resolution Electron Microscopy of in-Liquid Samples

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

The transmission electron microscope (TEM) has been an important characterization tool since its invention in 1932. [1] The ability to achieve atomic resolution imaging and collect real-time movies, combined with the availability of electron energy loss spectroscopy (EELS) and energy dispersive X-Ray spectroscopy (EDX) within the same instrument, make the TEM an indispensable tool for the study of dry solid samples. [1, 2] The use of a nanofluidic system (NFS) extends the applications of TEM to include wet solid, liquid, and gaseous samples, opening up a world of possibilities for the direct study of solution or gas phase reactions, dynamics of particles in liquids, cellular structure in its natural state, and more. [3]

In this project, I led the development of a complete NFS for transmission electron microscopy (TEM) of wet samples and flowing liquid samples. The system consists of a nanofluidic cell to enclose the sample, and a sample holder arm which allows flow of liquid into and out of the TEM. Unlike the typical commercial NFSs available, this system will feature true, controlled liquid flow. The design of the fluidic cell is distinct from other existing designs, and is supported by both the results of flow simulations and experiments performed with larger analogous fluidic cells. All microfabrication was performed by myself and another lab member (Ariel Petruk) in the University of Waterloo's Quantum NanoFab. The sample holder was designed in collaboration with Hitachi High Technologies Canada (HTC), who provided feedback on dimensions to ensure compatibility with Hitachi electron microscopes (EMs) and manufactured the prototype holder. The completed NFS will soon be used in our lab to perform a variety of in-liquid TEM and electron diffraction studies, and will be commercialized by HTC.

The immediate goal of this project is to prove that the NFS works as anticipated:

initial experiments will include nanoparticle (NP) uptake in E. coli, using flow conditions to maximize the lifespan of the bacteria in the nanofluidic cell. The study of living (or recently-living) biological cells has the potential to reveal information which cannot be obtained by studying fixated cells. A longer term goal is to use the NFS to study the structure and NP uptake behaviour of brain tumour initiation cells (BTICs); this research would involve collaboration with Dr. Shelia Sing at McMaster University, and would require modification of the electron source of our scanning transmission electron microscope (STEM), which is outside the scope of this thesis. Other future work will include the incorporation of fast mixing and electrochemical functionality in the nanofluidic cell.

Acknowledgements

The design of the nanofluidic holder was completed in collaboration with HTC, specifically with Stas Dogel: his expertise in the design of sample holders for Hitachi EMs was crucial for ensuring success. The support of HTC in manufacturing the nanofluidic holder is greatly appreciated.

The University of Waterloo's Quantum NanoFab was used for this work. This infrastructure would not be possible without the significant contributions of the Canada Foundation for Innovation, the Ontario Ministry of Research & Innovation, Industry Canada and Mike & Ophelia Lazaridis. Their support is gratefully acknowledged. Thank you to NanoFab members Nathan Nelson-Fitzpatrick, Brian Goddard, and Rodello Salandanan for training, support and advice regarding fabrication techniques, and (in the case of Rodello) removing many wafers stuck in the reactive ion etcher.

Thank you to Catherine Van Esch for all of her hard work in keeping the Chemistry department running smoothly. Many instances of confusion were resolved after coming to her saying, "Cathy, I have a problem!" Knowing there was such a supportive figure in the department has allowed me to persevere through difficult times.

This work was performed as part of the Ultrafast electron Imaging Lab (UeIL), headed by my supervisor Germán Sciaini. His vision has been, and will continue to be, the driving force behind this research. Thank you to everyone involved in the UeIL, and most especially to Ariel Alcides Petruk, whose dedication and talents were vital to the project. His work with Nicolàs Rivas on analogous (but larger) fluidic cells provided many insights on the design of the nanofluidic cell, and he has been an important part of every stage of this work. I would also like to acknowledge Germán for his support and supervision, and his assistance with LaTeXformatting, and Kristina Lekin for her advice and support.

Dedication

For science!

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List of Abbreviations

3D	three-dimensional
ALD	atomic layer deposition
$\alpha-Al_2O_3$	alpha-aluminum oxide
BSA	back side alignment
BTIC	brain tumour initiation cell
COMSOL	COMSOL Multiphysics 5.2
cryo-EM	cryo (cryogenic) electron microscopy
CVD	chemical vapour deposition
DI	deionized
DLC	diamond-like carbon
DNQ	diazonaphthoquinone
EBE	electron beam evaporation
EDX	energy dispersive X-Ray spectroscopy

EELS	electron energy loss spectroscopy
EM	electron microscope
EM	electron microscopy
ETEM	environmental transmission electron microscope
ETEM	environmental transmission electron microscopy
GLC	graphene liquid cell
hBN	hexagonal boron nitride
H_2O_2	hydrogen peroxide
H_2SO_4	sulphuric acid
HTC	Hitachi High Technologies Canada
ID	inner diameter
IPA	isopropyl alcohol
IR	infrared
KOH	potassium hydroxide
LayoutEditor	LayoutEditor Basic Version
LPCVD	low-pressure chemical vapour deposition
N_2	nitrogen gas
NFS	nanofluidic system
NH_3	ammonia

NP	nanoparticle
O_2	oxygen gas
OD	outer diameter
PECVD	plasma-enhanced chemical vapour deposition
PEEK	polyether ether ketone
PMMA	poly(methyl methacrylate)
PS	polystyrene
QDR	quick dump rinse
RIE	reactive ion etching
RSE	relative standard error
SEM	scanning electron microscope
SF_6	sulphur hexafluoride
$SiCl_2H_2$	dichlorosilane
Si_3N_4	stoichiometric silicon nitride
Si_xN_y	silicon nitride
SiO_2	silicon dioxide
SOP	standard operating procedure
SPM	sulphuric acid:peroxide mixture
STEM	scanning transmission electron microscope
STEM	scanning transmission electron microscopy

STS	Science Technical Services
SW	SolidWorks Education Edition 2013
TEM	transmission electron microscope
TEM	transmission electron microscopy
TMAH	tetramethylammonium hydroxide
TSA	top side alignment
UeIL	Ultrafast electron Imaging Lab
UV	ultraviolet
VLM	visible light microscope

Chapter 1

Introduction

Since the main focus of this work is the design and fabrication of a closed flow system for the study of in-liquid samples by TEM, the following introductory sections will highlight the challenges and current state of affairs when trying to obtain atomically resolved electron images of fully hydrated specimens, samples that present moderate vapour pressure or, going to an extreme, require a liquid environment.

1.1 Transmission Electron Microscopy

Over the last two decades, the advances in high-resolution TEM have been tremendous. The advent of aberration-corrected magnetic lenses in combination with brighter and better electron sources brought the spatial resolution of TEMs below 0.5 Å. There are two basic approaches to obtain atomically resolved structures in TEM: conventional TEM and scanning transmission electron microscopy (STEM). In conventional TEM, the specimen is illuminated by a near-collimated electron beam and the image is formed on a detector

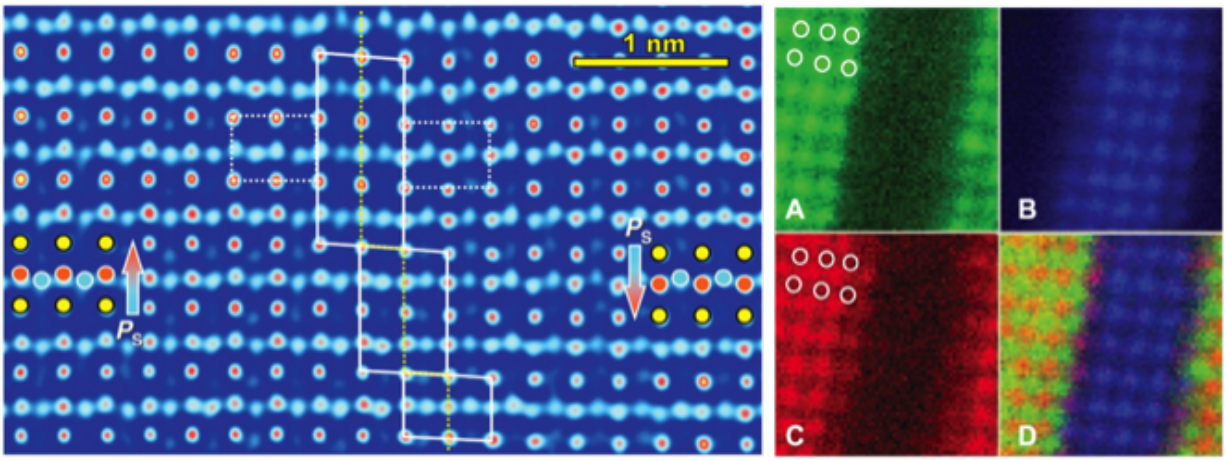

Figure 1.1: From Urban, K.W. Studying atomic structures by aberration-corrected transmission electron microscopy. *Science*, 321: 506-510, 2008. [4] Reprinted with permission from AAAS. **Left:** Transversal inversion polarization-domain wall in ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$. Arrows give the direction of the spontaneous polarization, which can be directly inferred from the local atom displacements. The shifts of the oxygen atoms (blue circles) out of the Ti/Zr-atom rows (red circles) can be seen directly, as well as the change of the Ti/Zr-to-Pb (yellow circles) separation. **Right:** Spectroscopic imaging of $La_{0.7}Sr_{0.3}MnO_3/SrTiO_3$ multi-layer, showing the different chemical sublattices in a 64 × 64 pixel spectrum image extracted from 650 eV–wide electron energy-loss spectra recorded at each pixel. **(A)** La M edge; **(B)** Ti L edge; **(C)** Mn L edge; **(D)** red-green-blue false colour image obtained by combining the rescaled Mn, La, and Ti images.

(screen) by a sequence of lenses similar to a visible light microscope (VLM). In STEM, the electron beam is focused to a small spot in the sample plane and the image is formed by scanning the specimen while monitoring various signals that usually depend on the atomic occupancy.

High-resolution images obtained by conventional and scanning TEM are shown in figure 1.1 left and right panels, respectively. As can be observed, both techniques provide similar atomic spatial resolution. TEM and STEM are powerful techniques for obtain-

ing high-resolution structural information. However, the requirements of high vacuum and ultrathin samples have mostly limited the application of both techniques to metals, semiconductors and different ceramic-like materials. Samples must be vacuum-compatible (allowing the sample chamber to be kept at a pressure of around 10^{-5} Pa or less), and they must be sufficiently electron transparent. Meeting these criteria ensures that the electron beam of the TEM can reach the detector. [1] For solid samples, a variety of techniques are available to thin the material until it is suitably electron transparent (typically to 100 nm or less). Wet, liquid, or gaseous samples are inherently challenging due to the necessity of maintaining high vacuum in the TEM column. In addition, the small probed volume and intense electron beam limit the exposure time for radiation sensitive specimens. Obtaining high resolution images of samples such as polymers, organic compounds and biological systems is therefore extremely difficult.

1.1.1 TEM studies of biological specimens

This section will discuss methods of modifying biological samples to suit the microscope. The following techniques are not appropriate for liquid or gaseous samples.

Vitrification for cryo-EM

A popular method for preparing hydrated biological samples is vitrification: the sample (typically in buffer solution or water) is flash-frozen to below −135 °C, such that the water in the sample forms vitreous ice (i.e. amorphous ice, rather than crystalline). [5, 6] For specimens up to 1 μm thick, immersion in liquid cryogens (e.g. liquid ethane or nitrogen) is an appropriate rapid freezing method. In 1976, Taylor and Glaeser were able to achieve 11.5 Å resolution TEM of vitrified bovine liver catalase using this technique. [7] The main

limitation of cryo (cryogenic) electron microscopy (cryo-EM) (i.e. electron microscopy (EM) of samples at cryogenic temperatures) is that vitrified samples must be kept below −135 °C at all times to avoid the formation of ice crystals; this includes while the sample is being sliced, handled, and imaged in the TEM (or scanning electron microscope (SEM)). [6] While a dedicated microscope is not required, a specialized sample holder is needed to maintain low temperatures. Cutting vitrified specimens to an appropriate thickness requires a cryo-ultramicrotome, and can introduce artefacts to the structure. [6] If the sample heats up too much at any point, ice crystals will form and (in the case of cells) cause the sample to rupture. In addition, the contrast of vitrified biological specimens is often poor. [5] Though the limitations may sound severe, cryo-EM is a viable and very useful technique for study of biological samples when performed with appropriate equipment.

Chemical fixation

An alternative method is chemical fixation: it requires no specialized equipment (beyond what is typically needed for TEM sample preparation), and produces samples which can be stored in ambient conditions. A chemical fixative is introduced to the sample, causing cross-linking between the proteins. While this allows the sample to be dehydrated without deforming, it does also introduce non-trivial changes to the structure. [6] Heavy metal salts are often added to the specimen in order to increase contrast; the resolution achieved is based on how well the stain can penetrate the sample, and is typically limited to around 20 Å. [5] After dehydration (and optional staining), the sample can be embedded in resin and sectioned into thin slices with a microtome. The sliced samples can then be loaded into a standard TEM sample holder for analysis.

1.1.2 Environmental TEM

The environmental transmission electron microscope (ETEM) provides another possible route to the study of hydrated samples: beginning with work in 1942, open cell ETEMs (or modified standard TEMs) have used differential pumping to produce a region of relatively high pressure around the sample, allowing the study of gas/solid interfaces and wet samples. [3] Pairs of apertures on the polepieces above and below the sample region restrict gas flow, but not the passage of the electron beam; gas is pumped into the space around the sample (between the innermost apertures), and evacuated before reaching the rest of the sample chamber; refer to figure 1.2 on page 6 for an example. [8] Standard TEM sample holders can generally be used, reducing cost and permitting the use of tilting, heating, cooling, and biasing holders. [9] While the apertures, pumping lines, and sample area can be packaged into an interchangeable unit, incorporating this unit into a standard TEM still requires disassembly and reassembly of the instrument. [8] Open cell environmental transmission electron microscopy (ETEM) is particularly useful for the study of gas/solid catalytic reactions, and is still used today; however, the resolution is limited relative to a non-environmental TEM. In addition, an open cell is not suitable for liquid samples, unless they have low vapour pressure and high viscosity; even then, a specialized holder would be needed. [3, 9]

Another approach is the closed environmental cell: this is the predecessor of modern liquid TEM cells, with examples dating back to a 1944 closed cell using nitrocellulose windows. [3] A more advanced example, in this case used for studying hydrated cement, is shown in figure 1.3 on page 7. [10] Containing the relatively high pressure environment within the sample holder allows standard, unmodified TEMs to be used for environmental studies, thus avoiding the cost associated with a dedicated ETEM or the time required

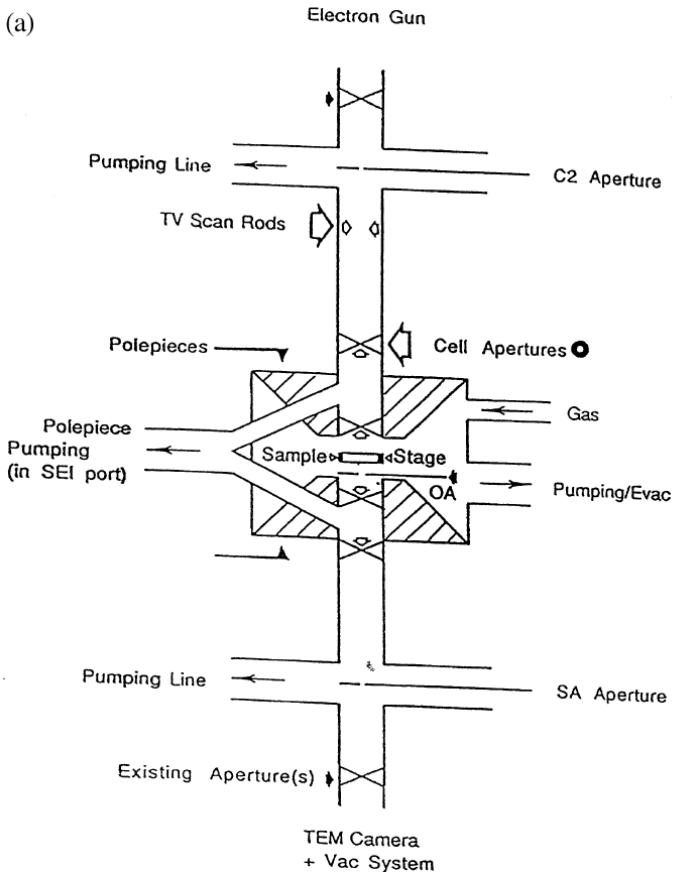

Figure 1.2: Example of an ETEM schematic, reprinted with permission of Springer: Topics in Catalysis, Developments in *in-situ* Environmental Cell High-Resolution Electron Microscopy and Applications to Catalysis, Vol 21, 2002, pp 161-173, P.L. Gai, (© Plenum Publishing Corporation 2002). [8] Original caption: Schematic of the basic geometry of the aperture system in the *in-situ* atomic-resolution ETEM development of Gai and Boyes to probe dynamic catalysis at the atomic level. The objective polepieces, pumping lines, cell apertures, sample stage, condenser (C2) and selected area diffraction (SA) apertures are illustrated.

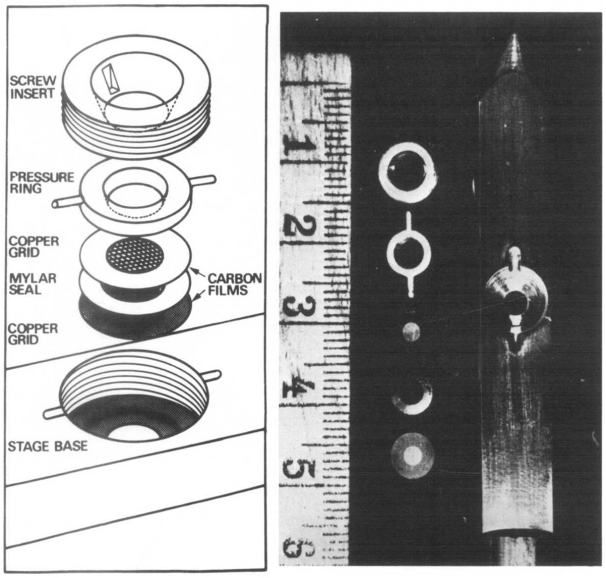

Figure 1.3: An environmental TEM cell with a custom holder. Reprinted from Materials Science and Engineering, Vol 12, D.D. Double, Some studies of the hydration of Portland cement using high voltage (1 MV) electron microscopy, Pages No. 29-34, Copyright (1973), with permission from Elsevier. [10] Original caption: The environmental cell specimen stage for the A.E.I. E.M.7 1 MV electron microscope.

to modify a TEM for environmental functionality. However, the performance of these early environmental cells was limited by the materials and fabrication techniques available: thicker windows are more likely to survive electron beam irradiation and pressure differentials, but also require higher voltages for the electron beam to penetrate. [9] Choosing a window material with appropriate properties is challenging; see section 1.2.1 on page 8 for further discussion. Overall, the resolution of closed environmental cells in the 1970s was only slightly better than that of a VLM. [3]

The common thread among all of the techniques described thus far for difficult TEM samples is that the specimen is either converted into a dry solid, or is isolated from the vacuum chamber. With the development of new closed cell systems based on reliable and

ultrathin window materials and microchips that fit within the geometrical boundaries of a conventional electron microscope sample holder, the popularity of expensive ETEMs declined. An increasingly popular method is to enclose a liquid or wet sample between two Si microchips, each with a thin, electron transparent window. The chips are separated by a spacer and sealed to prevent leakage. [11] This style of liquid cell is referred to as a "sandwich cell," and is the method pursued in this work. Sandwich cells can either be fully closed (a "stationary cell"), or closed to TEM column but allowing liquid to flow through (a "flow cell"); sections 1.2.2 and 1.2.3 will describe stationary and flow cells, respectively, in greater detail. For further reading on liquid cells for EM, refer to the 2017 book "Liquid Cell Electron Microscopy" by Frances M. Ross. [12]

1.2 Nanofluidic cell systems

Innovative closed cell designs can literally transform any conventional TEM into an ETEM by providing capabilities to study in-liquid samples. Commercial NFSs are available from companies such as Protochips Inc. and Hummingbird Scientific. Costing around $120,000 per holder and around $200 per replacement cell, these systems are still relatively inexpensive in comparison to an ETEM. However, these systems use either stationary or pseudo-flow liquid cells (further discussed in section 1.2.3 on page 18) that feature very primitive designs with little, if at any, control of liquid flow.

1.2.1 Ultrathin window materials

The most important aspect in the design and fabrication of nanofluidic cells is the availability of ultrathin window materials suitable for TEM. The properties of the window

membrane are crucial for designing a successful sandwich cell. The window is what keeps the sample isolated from vacuum, and is often a limiting factor in obtainable resolution and appropriate pressure conditions. A good window must be strong enough to withstand the pressure difference between the cell interior and vacuum (around 1 atmosphere for stationary cells, and potentially a few times that for flow cells); rigid enough to prevent excessive flexing, without being brittle enough to fracture during use; it must be as electron transparent as possible, by a combination of material choice and thickness; and large enough to provide a good field of view, but small enough to limit flexing. Rectangular windows with a high aspect ratio (4:1 or longer) have deformation behaviour limited by their narrow dimension, so window shape should be considered as well as size. [13] Additionally, the window material must be chemically compatible with both the desired samples and the fabrication procedure.

The most popular window material for TEM fluidic cells is silicon nitride (Si_xN_y): it is compatible with many Si device fabrication techniques, can be used as an etch mask for KOH etching of Si (a highly convenient feature), and has reasonably good mechanical and chemical properties. [11,14–16] Low-pressure chemical vapour deposition (LPCVD) is used to produce Si_xN_y windows; LPCVD Si_xN_y is amorphous, composed of tetrahedral SiN_4 and trigonal NSi_3 units connected without long-range order. [16] The ratio of Si to nitrogen can be varied by changing LPCVD conditions, ranging from Si-poor (0.625:1 Si:N) to stoichiometric silicon nitride (Si_3N_4) to Si-rich (2:1 Si:N). [11,16] Si-rich nitride is referred to as "low-stress" Si_xN_y, due to its lower residual stress; it is more flexible than Si_3N_4, and less prone to fracture.

While Si_xN_y is the most commonly used window material for nanofluidic cells, it is not the only option. Graphene has been successfully used to create stationary sandwich cells with monolayer-thick windows; the Alivisatos group at the University of California Berkeley

(and at the Lawrence Berkeley National Laboratory) first developed graphene liquid cells (GLCs), and has performed a variety of studies using them. [17,18] Unfortunately, graphene membranes are not compatible with mainstream cleanroom techniques, which prevents mass-production of GLCs and greatly complicates the incorporation of features such as electrodes, controlled spacers, or liquid flow. Similar problems exist for hexagonal boron nitride (hBN) and graphene oxide, two other potentially useful materials for extremely thin membranes. [11] SiO_2 has significantly reduced residual stress compared to Si_3N_4, and is reasonably compatible with microfabrication techniques; however, unlike Si_xN_y, SiO_2 reacts with KOH and cannot be used as an etch mask for Si. [11,19] While it is possible to work around this constraint (as done by Liu *et al.* in [20]), it is less convenient than using Si_xN_y. For further discussion of window materials, refer to section 6 on page 85.

1.2.2 Stationary cells

Stationary sandwich cells are the modern descendants of closed ETEM cells. Beginning with Williamson *et al.* in 2003 [21] (see figure 1.4 on page 11), microfabrication techniques have allowed a variety of encapsulated liquid cells for TEM to be produced. The basic components of a stationary sandwich cell are two Si wafers, each with an electron transparent window, separated by some kind of spacer and sealed together to contain liquid. [11] The spacer is one of the most variable design features: it might enclose all four sides of the cell as shown in figure 1.4 on page 11, with materials such as In [22, 23], Si_xN_y [24], or SiO_2 [15, 21, 25]; a more minimal spacer might cover only two sides of the cell with photoresist (as in figure 1.5 on page 14) or a material deposited by chemical vapour deposition (CVD) [26–28], or might be deposited only on the corners of a microchip (for example Au pillars [29] or polystyrene (PS) [30]). Some designs have no spacer at all, relying on

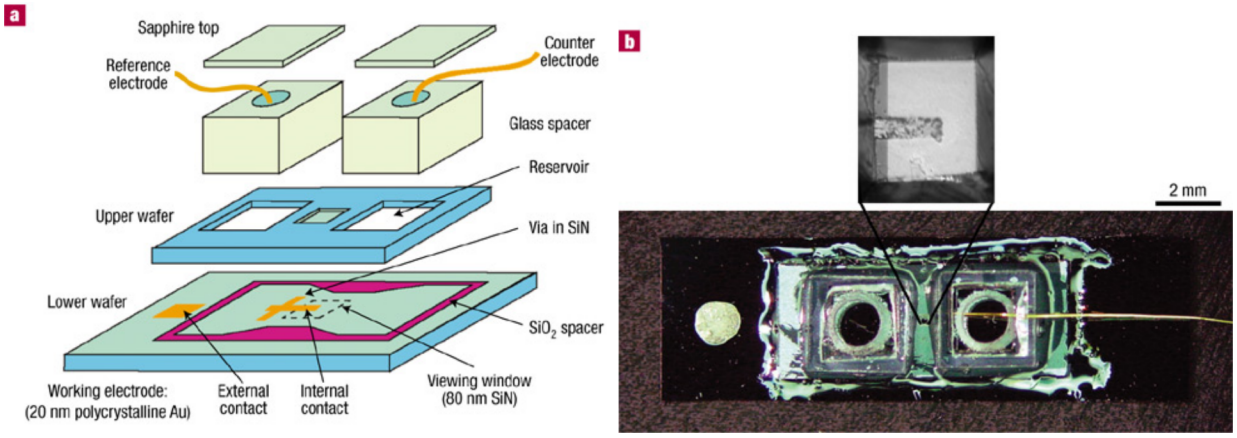

Figure 1.4: The first encapsulated liquid cell for TEM, developed by Williamson *et al.* Reprinted by permission from Macmillan Publishers Ltd: Nature Materials, copyright 2003. [21] Original caption: **a**, Components of the cell. The viewing window is enlarged for clarity. **b**, Photograph of a two-electrode cell with an optical micrograph of the viewing window.

the roughness of features on the microchips to provide separation. [31] The height of the spacer must be appropriate for the desired sample and type of study; for observation of biological cells or other large structures, the spacer must be tall enough to accommodate the sample height, while for liquid phase studies the height can typically be minimized to improve resolution. Design choices for spacers will be discussed further in section 1.2.3, with some designs illustrated in figure 1.10 on page 22.

Table 1.1: Stationary sandwich cell designs

Cell	Window	Spacer	Sealing and Features	Holder
Williamson *et al.* electrochemical cell [21]	Si_3N_4, 100 nm thick	SiO_2 along each side of the bottom chip, $0.5 - 1$ μm thick	See figure 1.4 on page 11. Bottom chip has a 20 nm Au electrode. Top chip has two reservoirs, covered with sapphire lids and sealed with epoxy. Au (counter electrode) and Cu (reference electrode) wires attach through the reservoirs.	Custom holder required
Zheng *et al.* cell; used for results in figure 1.8 on page 19. [22, 23]	Si-rich Si_xN_y, $10 - 30$ nm	In metal along each side of the top chip, $0.1 - 0.25$ μm thick	The top and bottom chips are aligned, and then baked to melt the In slightly and seal the chips. Top chip has two reservoirs, which are covered by a standard Cu lid (sealed with epoxy).	Fits into a standard sample holder
Zheng *et al.* electrochemical cell [32]	Si-rich Si_xN_y, 35 nm thick	In metal along each side of the top chip, 1.5 μm thick	Bottom chip has two 120 nm thick Au electrodes. Top chip has two reservoirs, through which Au wires were connected to the electrodes.	Custom holder with electrical contacts was used
White *et al.* electrochemical cell [31]	Si_3N_4, 19 nm thick, with a thin layer of SiO_2	No spacer; chips are separated by the electrode (0.3 μm space)	Bottom chip Au electrodes. Cell was sealed with epoxy.	Hummingbird Scientific holder with temperature control

Table 1.1: (continued)

Cell	Window	Spacer	Sealing and Features	Holder
Liu *et al.* cell [20]	SiO_2, 9 nm thick	Epoxy mixed with 1 μm PS beads applied to corners of the cell; final height of $2 - 5$ μm	Cell was sealed with epoxy, as described for the spacer	Fits into a standard sample holder (after being adhered to a Cu grid)
Hummingbird Scientific electrochemical cell [24]	Si_xN_y (stoichiometry unknown), 100 nm thick	Si_xN_y along each side of one chip, $0.2 - 0.5$ μm thick	See figure 1.7 on page 17. Bottom chip has 5 nm Ti/20 nm Au working electrode, top chip has two reservoirs. Cell was sealed with epoxy.	Hummingbird sample holder was used
Protochips Inc. custom cell. Also used with flow; see table 1.2 on page 20. [26]	Si-rich Si_xN_y, 50 nm thick	Patterned SU8 photoresist along two sides of the top chip, 5 μm thick	See figure 1.6 on page 15 and figure 1.5 on page 14. Cell was sealed with epoxy.	Used with a modified standard sample holder

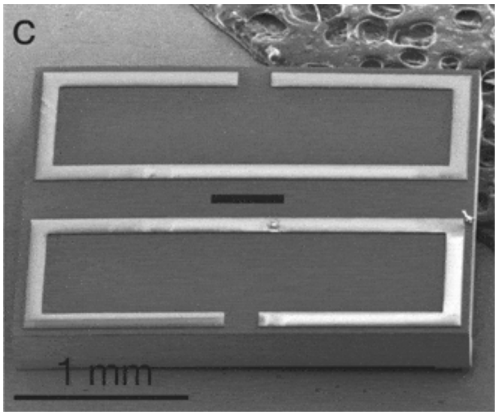

Figure 1.5: Protochips Inc. custom cell with spacer patterned via photolithography. This cell was used both with and without flow; refer to tables 1.1 and 1.2. Adapted from [33] with permission. Original caption: SEM images of the microchips. The SEM images were recorded at 10 kV (S4700 Hitachi). Image of the Si_xN_y side of the microchip showing the shape of the SU8 spacer; charging effects distort the image at the positions of the spacer. The Si_xN_y window is the dark shape.

Stationary Si_xN_y sandwich cells comprised of two Si microchips, each with some type of Si_xN_y window (usually 50 nm in thickness), spaced apart and sealed, will now be described in greater detail. See table 1.1 for references and important features of each design. With the exception of the White *et al.* and Protochips Inc. stationary cells, reservoirs with lids are often included to increase the available liquid volume. The benefit of stationary cells is that these can be designed to fit into a standard TEM sample holder. Stationary cells are easier to make than flow cells: they are easier to seal (a coating of epoxy as shown in figure 1.6 on page 15 suffices), windows don't need to handle as much pressure, and having fewer features simplifies the fabrication process by reducing the number of steps. Specialized sample holders can be developed to incorporate extra features such as electrical contacts (see figure 1.4 on page 11) or temperature control. Adding electrochemical functionality to stationary cells still remains very popular (see figure 1.7 on page 17). In all

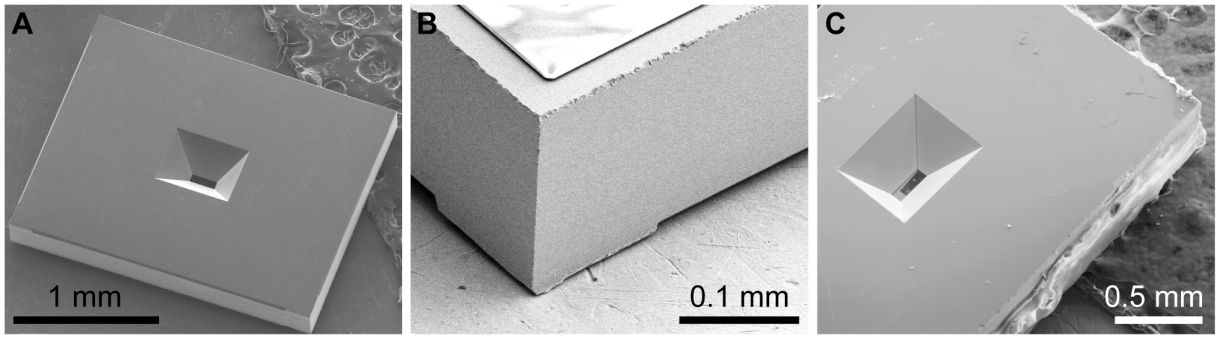

Figure 1.6: Example of a stationary liquid cell (produced by Protochips Inc.) sealed with epoxy. Reprinted from [26] with permission. Original caption: Scanning electron microscopy (SEM) images of the Si microchips. The SEM images were recorded at 10 kV (S4700 Hitachi). **A**, Image of the backside of a microchip showing the opening for the Si_xN_y window. **B**, Close-up of the diced edge of the microchip. The SU8 spacer layer is visible at the top (the layer charges under the influence of electron beam irradiation). **C**, Image of a liquid enclosure assembled from two microchips and closed at all sides with epoxy. The bottom microchip is visible through the Si_xN_y window confirming the alignment of the top- and the bottom window.

cases, stationary cells meant to be disposed of after a single use. This is to avoid removal of already cured epoxy and other possible sources of contamination. Disposal of microchips is not a problem however, since they are fabricated in large quantities (typically about 500 units per 4" wafer).

The basic fabrication process for Si_xN_y sandwich cells is fairly consistent. [11, 21, 25, 34–37] First, {100} Si wafers ($100 - 350$ μm thick, lightly doped for conductivity) are cleaned, and a layer of Si_xN_y is deposited on both sides of each wafer by LPCVD. The thickness and stoichiometry of the Si_xN_y vary based on design. For an electrochemical cell, electrodes could be applied at this stage, using a lift-off process: the wafers are patterned with negative photolithography, the desired metal is deposited (typically by electron beam

evaporation (EBE)), and the photoresist is removed, along with the excess metal. The wafers are then patterned with positive photolithography, followed by reactive ion etching (RIE) of the exposed Si_xN_y in the features. Wet chemical etching, done with KOH or tetramethylammonium hydroxide (TMAH), etches away the Si to form the windows and any other features (e.g. reservoirs). During wet etching, the Si_xN_y acts as the etch mask. If SiO_2 was added on top of the Si_xN_y (as in the White *et al.* cell), the excess can be removed via buffered oxide or hydrofluoric acid etch. [31] The spacer is typically fabricated after wet etching of Si, though this may vary depending on spacer material and design choices. For metal spacers, a lift-off procedure can be used, as described for electrodes. SiO_2 spacers are deposited via plasma-enhanced chemical vapour deposition (PECVD); either a lift-off process can be used, or excess SiO_2 can be removed after PECVD using a buffered oxide etch. Photoresist spacers are simple to fabricate: the wafers are patterned with negative photoresist, and the spacer is complete. If PS (or other polymer) microbeads are used as the spacer, they are applied later on in the process.

Once the spacer (excepting polymer microbeads) and chip features are complete, the wafers are separated into individual chips. This can be done by hand, or with a dicing saw. A protective layer of photoresist is useful to protect the delicate windows during separation. If used, the protective photoresist is removed prior to loading the cell. Additional steps might be performed at this stage, such as plasma cleaning or coating to change the hydrophilicity of the surface. If polymer microbeads are used as the spacer, they would be deposited with a micropipette immediately prior to cell loading. For the Zheng *et al.* design, each cell is assembled and baked at 120 °C to slightly melt the In spacer, which bonds the two halves of the cell together as it cools. [34] Liquid samples are deposited as a droplet of solution onto one microchip. For biological cells, these are either deposited or grown directly on the chip. Once samples are loaded, the microchips are sealed: if ap-

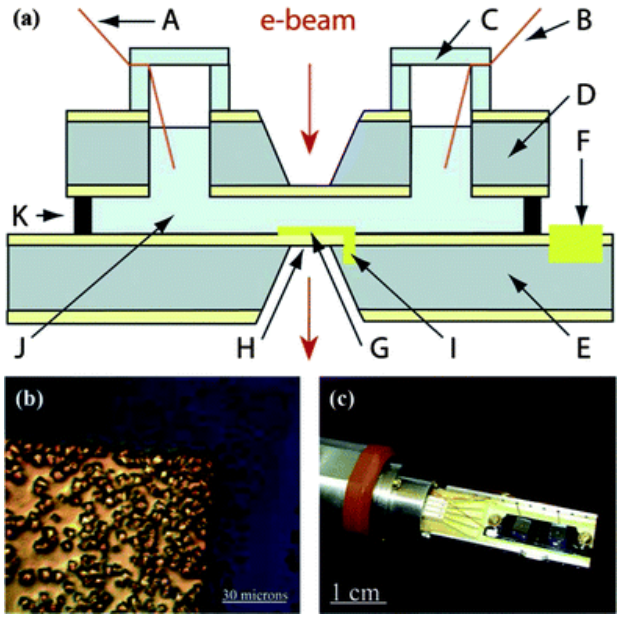

Figure 1.7: A stationary electrochemical liquid cell, produced by Hummingbird Scientific. Reproduced from [24] with permission of The Royal Society of Chemistry. Original caption: **a**, Schematic cross-section of fluid cell. A, B: reference and counter electrodes, C: glass cap, D, E: 100 nm Si_xN_y/300 μm Si(100)/100 nm Si_xN_y wafers, F, G: 5 nm/20 nm Ti/Au working electrode, H: Si_xN_y window, I: electrical contact between Si(100) and Au, J: solution reservoir, K: $200 - 500$ nm Si_xN_y spacer.

plicable, the reservoirs are covered with lids, and the cells are sealed with epoxy (typically ultraviolet (UV) cured epoxy, if it is to be applied after the sample is loaded).

As illustrated in figure 1.8 on page 19, stationary cells have provided great insights into reactions and processes triggered by electron beam irradiation, including evaporation from imperfectly sealed cells [22], NP formation and growth [17, 23, 34, 39, 40], tracking NP motion and dynamics [18, 22, 41], and their uptake by biological cells [26].

1.2.3 Flow cells

Experiments performed using stationary fluidic cells can also be performed with flow cells, which provide additional features. With a flow cell, the flow conditions (and therefore the sample pressure) and the sample composition can be varied without removing the fluidic cell from the TEM sample chamber. Table 1.2 on page 20 describes a variety of flow cell designs. All of the designs described in this section have 50 nm thick Si_3N_4 windows; the spacer and flow channel are typically the distinguishing features.

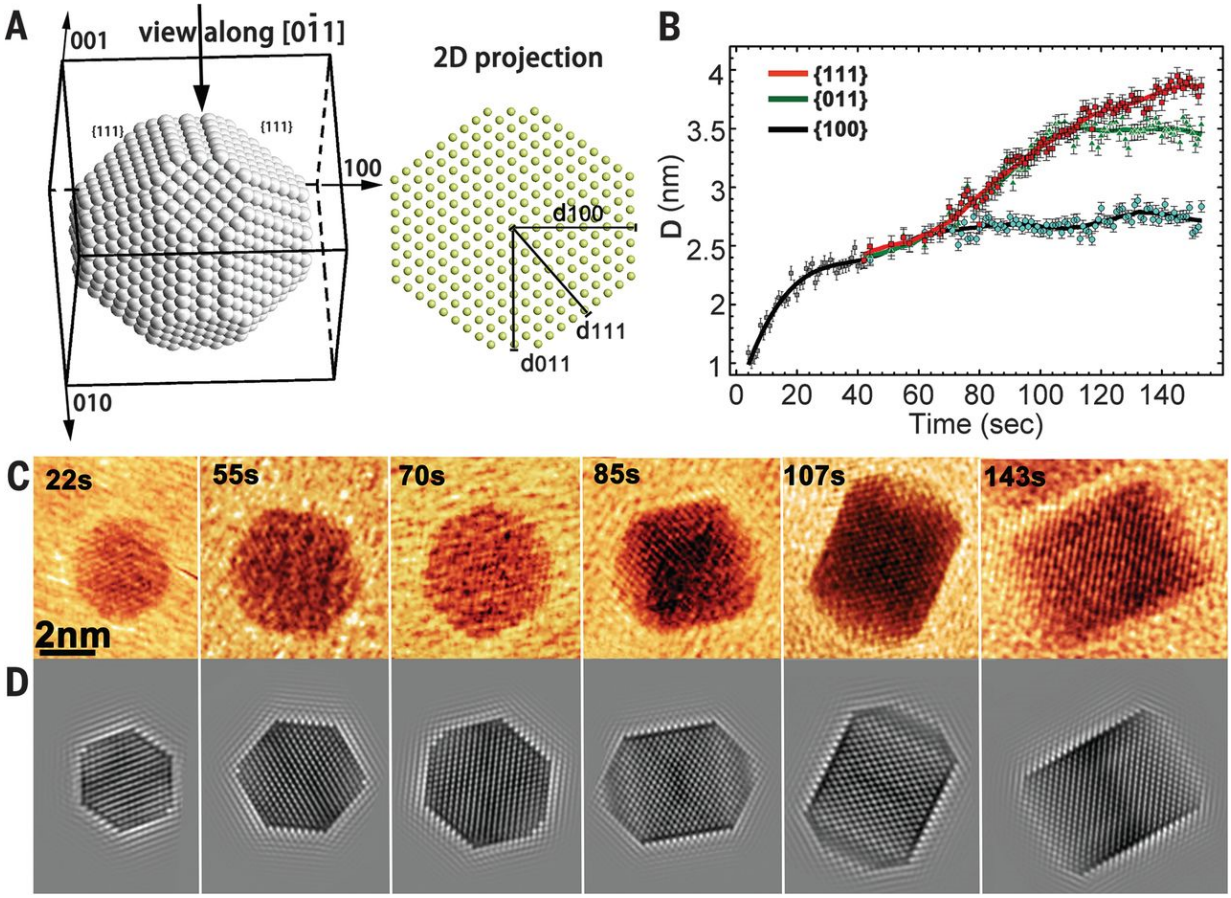

Figure 1.8: Example of high resolution TEM results obtained using a stationary liquid cell. From H.-G. Liao *et al.* Facet development during platinum nanocube growth. *Science*, 345: 916-919, 2014. [38] Reprinted with permission from AAAS. Original caption: The facet development of a Pt nanocube viewed along the [0$\bar{1}$1] axis. (**A**) The atomic model of a truncated Pt nanocube and its projection along the [0$\bar{1}$1] view zone axis. The distances from the crystal center to each of the (100), (011), and (111) facets are highlighted. (**B**) The measured average distances from the crystal center to each facet as a function of time. Error bars indicate the standard deviation. (**C**) Sequential images show the growth of the Pt nanocube extracted from movie S2. (**D**) Simulated TEM images of the Pt nanoparticle in (**C**).

Table 1.2: Sandwich cell designs with flow

Cell	Spacer	Sealing and Flow	Holder and Features
Protochips Inc. custom flow cell [30]	10 µm PS microbeads deposited on corners of the cell	Flow is around and through the cell. Sealed with O-rings around the entire cell.	Used with a flow holder (either Protochips Inc. or Hummingbird Scientific)
Protochips Inc. custom cell. Also used without flow; see table 1.1 on page 12. [33]	Patterned SU8 photoresist along two sides of the top chip, 5 µm thick	See figure 1.6 on page 15 and figure 1.5 on page 14. Flow is around and through the cell. Sealed with O-rings around the entire cell.	Hummingbird Scientific continuous flow holder, which has a single inlet line
Hummingbird Scientific dual flow cell [27]	SiO_2/Si_xN_y along two sides, $250 - 500$ nm thick	See figure 1.11 on page 24. Flow is around and through the cell. Sealed with O-rings around the entire cell.	Hummingbird Scientific dual flow holder, which has two inlet lines (mixing just before the cell)
Hummingbird Scientific single flow cell [29]	Au metal on the corners, $50 - 200$ nm thick	Flow is around and through the cell. Sealed with O-rings around the entire cell.	Hummingbird Scientific continuous flow holder, which has a single inlet line
Nanoaquarium, Grogan and Bau *et al.* [25]	Annealed and polished SiO_2 along all sides, 100 nm thick	See figure 1.9 on page 21. True flow: cell has inlet and outlet, forcing liquid to flow past window. Top and bottom chips are bonded together; O-rings seal the inlet and outlet.	Optional 4 nm Ti/22 nm Au/4 nm Ti electrodes. Custom holder.
Miller group cell [15]	SiO_2 along all sides, 100 nm thick	See figure 1.12 on page 25. True flow: cell has inlet and outlet, forcing liquid to go past the window. Sealed by pressure from the holder.	Grooves in one of the chips increase the size of the flow channel, reducing resistance. Custom holder.

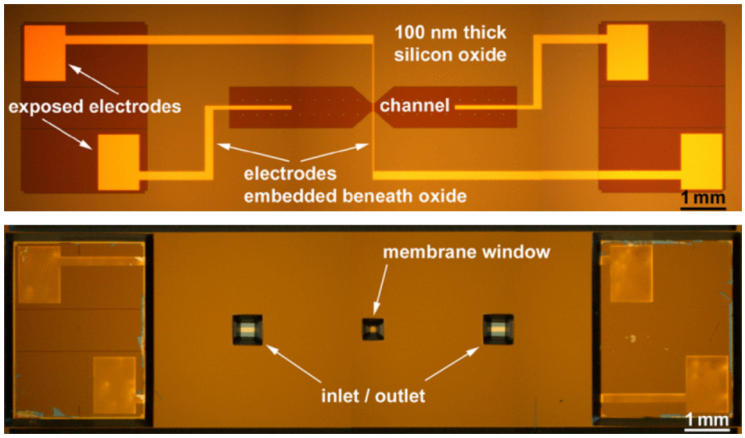

Figure 1.9: The "Nanoaquarium" flow cell developed by Bau *at al.*, as described in table 1.2 on page 20. The cell is fully sealed (aside from the inlet and outlet) via direct bonding of the top and bottom chips. Adapted from [25] with permission. ©2010 IEEE. Original captions: (**Top**) Top view of a single device on the bottom wafer prior to capping with the top wafer. (**Bottom**) Top view of a completed single device (18 mm × 5 mm × 0.6 mm).

The design of the spacer is crucial for flow cells, even more so than for stationary cells; figure 1.10 on page 22 shows several possible spacer designs. A common choice for flow cells (and also stationary cells) is a spacer completely surrounding the sample area, lining all four walls. [15, 21, 24, 25, 34] Other typical choices include a spacer along two of the four walls (leaving a flow channel across the length of the cell) or a spacer on each corner of the cell, leaving an opening on each side. [26, 27, 29, 42] The choice of spacer material should be considered based on the desired properties, such as compatibility with fabrication techniques, price, chemical properties of the desired samples, and the complexity of the spacer design.

It is critical to note that with most of the spacer designs shown in figure 1.10 on page 22, the flow is not controlled precisely; with the exception of spacers fully surrounding the cell, there is no way to control how much of the flow goes through the cell rather than around

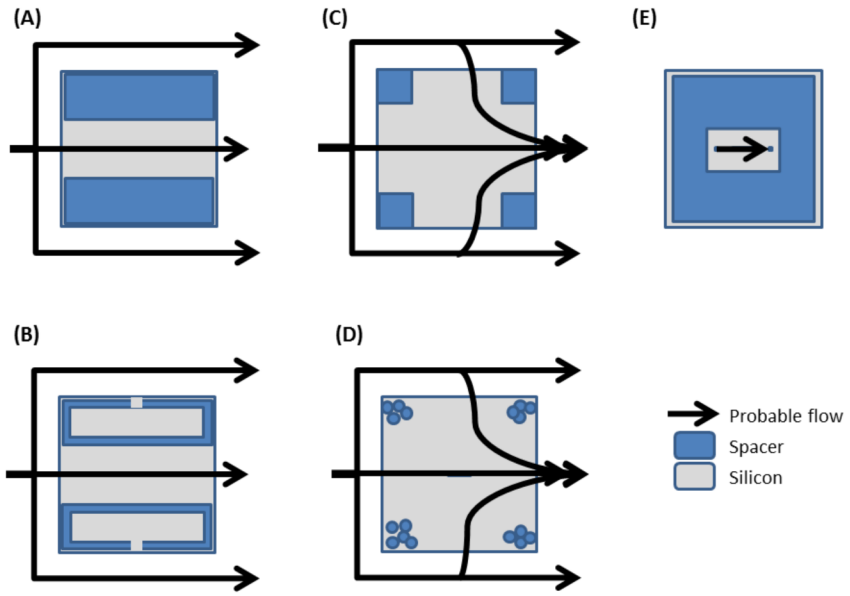

Figure 1.10: Illustration of several different spacer designs used in sandwich cells. While possible liquid flow paths are indicated (for flow cells), these designs could be also be used for appropriately sealed stationary cells. **(A)** Spacer material (e.g. SiO_2 [27,28]) along two sides, as in the dual-flow cell from Hummingbird Scientific. **(B)** Hollow spacer along two sides, as used by the de Jonge group to study cellular samples with [33] and without [26] flow. The spacer (made from SU8 photoresist) is shaped to prevent excess sample from forcing the chips too far apart. **(C)** Pillars of spacer material (e.g. Au [29]) on only the corners of the cell, as in continuous (single) flow cells from Hummingbird Scientific. **(D)** Polymer microbeads/microspheres deposited on the corners as a spacer; de Jonge *et al.* and Chee *et al.* each used flow cells with PS microspheres applied in a droplet of solution, with particle sizes of 10 μm and 0.96 μm, respectively. [30,43] Liu *et al.* mixed PS microspheres with epoxy in order to seal a stationary cell. [20] **(E)** A spacer completely surrounding a cell ensures that any flowing liquid is forced to travel past the window, as in the cells designed by Mueller *et al.* and Grogan *et al.* [15,25] This shape of spacer, made out of materials such as SiO_2, Si_xN_y, and In, is also common for stationary cells. [21–24,32]

it. Due to the TEM imaging requirement of thin samples, even relatively tall spacers are typically 1 μm or less; in comparison, the thinnest Si wafers used in any design covered here are 100 μm, giving a total cell height of at least 200 μm. This is demonstrated in figure 1.11 on page 24. As a result, the effective resistance of the flow channel through the cell will be higher than that of the path around the cell, and the fraction of the flow through the cell itself may be small. The designs by the Miller group (figure 1.12 on page 25) and by Grogan *et al.* (figure 1.9) avoid this predicament by incorporating an inlet and outlet directly into the fluidic cell, forcing all of the liquid flow to travel through the cell, and giving true control over the flow rate past the windows. For clarity, fluidic cells with true, controlled flow (i.e. fluid must travel only from inlet to outlet) will be referred to as "true flow cells," while fluidic cells in which some of the flow is around the cell will be referred to as "pseudo-flow cells." Pseudo-flow cells still have advantages over stationary cells: changing the flow rate changes the pressure in the cell, which controls the deformation of the cell windows. This type of cell can also be simpler to design than a true flow cell.

Si_xN_y sandwich cells with and without flow typically have very similar fabrication processes. Wafers with a layer of Si_xN_y on each side are patterned with photolithography to allow selective dry etching of the Si_xN_y, followed by wet etching of silicon (masked by the Si_xN_y) to create features. Deposition of the spacer and electrodes (if applicable) might occur before or after wet etching, or in between multiple wet etching steps. The processes used to fabricate the nanofluidic cells designed in this work follow the general pattern; see chapter 5, beginning on page 67.

The design by Mueller *et al.*, initially presented in Harb's 2009 PhD thesis, features a well-controlled flow path which forces all of the fluid to travel past the cell windows (see table 1.2). [35] By stopping and starting the liquid flow during the experiment, Mueller *et al.* characterized both the diffusion-limited and pressure-driven motion of Au NPs, Au

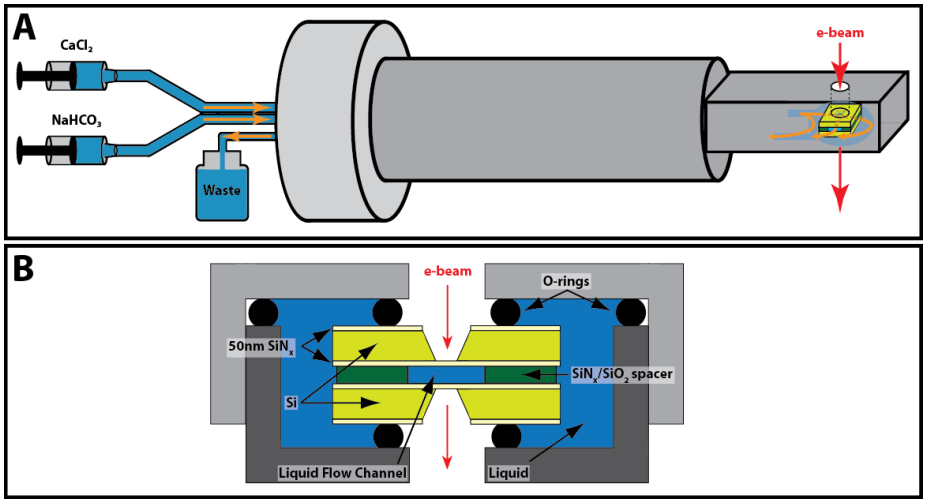

Figure 1.11: Dual-flow fluidic holder and cell, from Hummingbird Scientific. The diagram is not to scale, with the spacer height being greatly exaggerated. Note that there is no mechanism to force the liquid to flow through (rather than around) the cell; in fact, due to the lower resistance of the larger channels, the flow is significantly more likely to pass around the outside of the cell than to pass the window. Details about the cell are given in table 1.2. From M.H. Nielsen *et al.* In-situ TEM imaging of $CaCO_3$ nucleation reveals coexistence of direct and indirect pathways. *Science*, 345: 1158-1162, 2014. [27] Reprinted with permission from AAAS. Original caption: Schematics of experimental set-up. Overview of the liquid stage set-up (A) shows separate inlets for the two reagent solutions, that mix shortly before reaching the liquid cell. Proprietary stage details regarding inlet mixing not shown. The combined liquid stream flows through the flow channel of the cell as well as around the external sides of the cell, and exits the stage through a single outlet tube that empties into a waste container. Side-view schematic of the liquid cell on the stage (B) shows liquid in the cell's flow channel, as well as external to the cell. From this perspective, liquid would flow into/out of the plane of the image as it passes through the cell. O-rings keep the liquid separated from the vacuum of the TEM column.

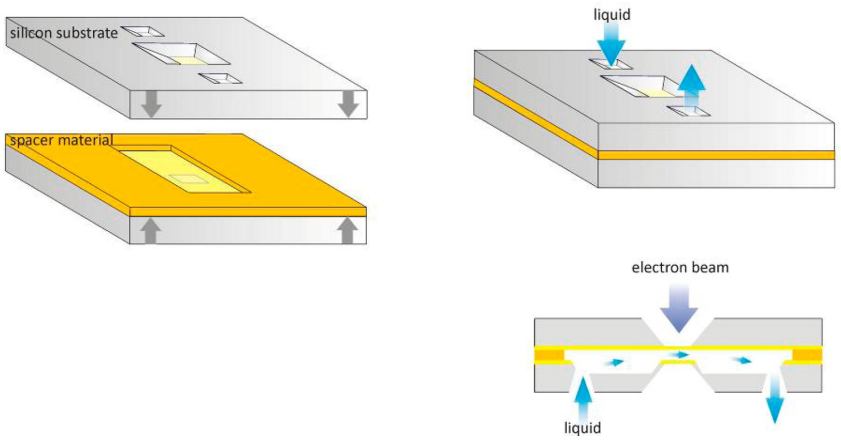

Figure 1.12: The fluidic cell designed in the Dwayne Miller group at the University of Toronto, as described in table 1.2; this design was originally presented in Harb's 2009 PhD thesis. [35] This design is a true flow cell, i.e. one in which all of the liquid must flow through the cell, past the window. Adapted with permission from C. Mueller *et al.* Nanofluidic cells with controlled path length and liquid flow for rapid, high-resolution in-situ imaging with electrons. *J. Phys. Chem. Lett.*, 4: 2339-2347, 2013. [15] Copyright 2013 American Chemical Society. Original caption: Nanofluidic sample cell as presented in this work containing a defined flow path, inlet and outlet ports implemented into the cell, and a liquid layer thickness defined by the rigid spacer material (orange).

nanorods, and polymer NPs in an aqueous surfactant solution. [15]

After reviewing the fluidic cells designed by other groups, and testing the concept of Miller group cell [15] (fully enclosed sandwich cell, with Si_xN_y windows and an inlet, outlet, and flow channel grooves), it was decided to pursue flow simulations in order develop our own microchip concept to attain true, controlled high flow, with minimal window deformation. The chip fabrication procedures were based on the common procedures used by many groups (LPCVD deposition of Si_xN_y; positive photolithography, RIE, and KOH etching for etched features, and an EBE lift-off process for the spacer). The final NFS presented in this work simply represents the most advanced design and it is expected to substitute those commercially available in the very near future.

Chapter 2

First generation nanofluidic system: development and testing

The sample holder and the nanofluidic cell were designed in tandem: the machining limitations and required outer dimensions of the holder provided a framework for the cell design, which in turn decided the detailed features of the holder. The NFS was designed to be compatible with the HD2000 STEM owned by the UeIL.

2.1 Basic design of sample holder arm

The first step of developing the sample holder was to determine the requirements. The basic single-tilt sample holder shown in figure 2.1 on page 28 was carefully measured, and was then reproduced as a three-dimensional (3D) model in SolidWorks Education Edition 2013 (SW). The most important details obtained were the distances between the sample area (where the electron beam passes through) and each end of the holder, and the maximum

dimensions of the holder tip (figure 2.2).

Figure 2.1: A basic Hitachi sample holder (for bulk samples with the HD2000 STEM in scanning mode) used as the basis for the fluidic holder design.

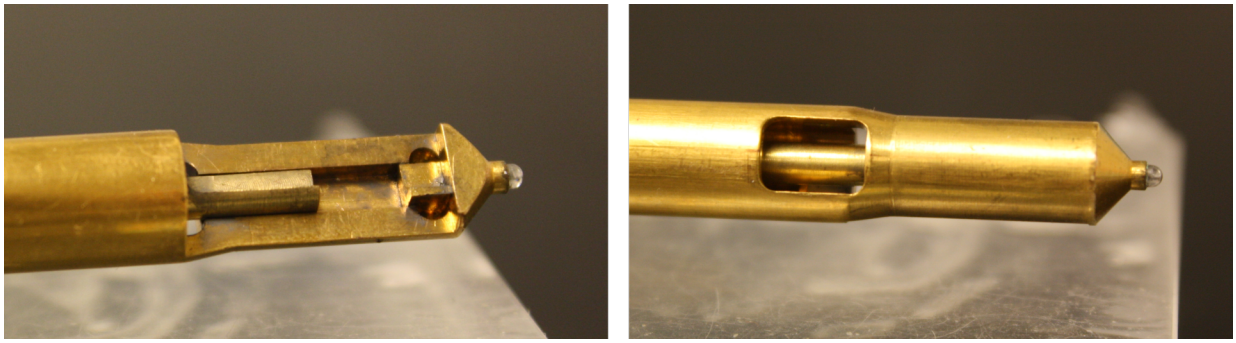

Figure 2.2: Tip of the standard Hitachi sample holder used as the basis for the fluidic holder design; note the tapered shape. The diameter of the tip (7 mm) was assumed to be the maximum allowable size for a holder tip (given a cylindrical shape).

Originally, the nanofluidic sample holder was to be manufactured by Science Technical Services (STS) at the University of Waterloo, and as such they were consulted for machining limitations (smallest size for drilled holes, required clearance between features, chamfer requirements, etc.). After this consultation, it was decided that metal capillary tubing would run through the interior of a hollow sample holder arm and connect to short channels drilled directly into the holder tip, produced as a separate piece; figure 2.3 on page 29 shows

a render of the basic holder at this stage of the design (without the tip). Appropriate tubing with an inner diameter (ID) of 250 µm, made from 316 stainless steel (durable, relatively inert) was sourced and purchased.

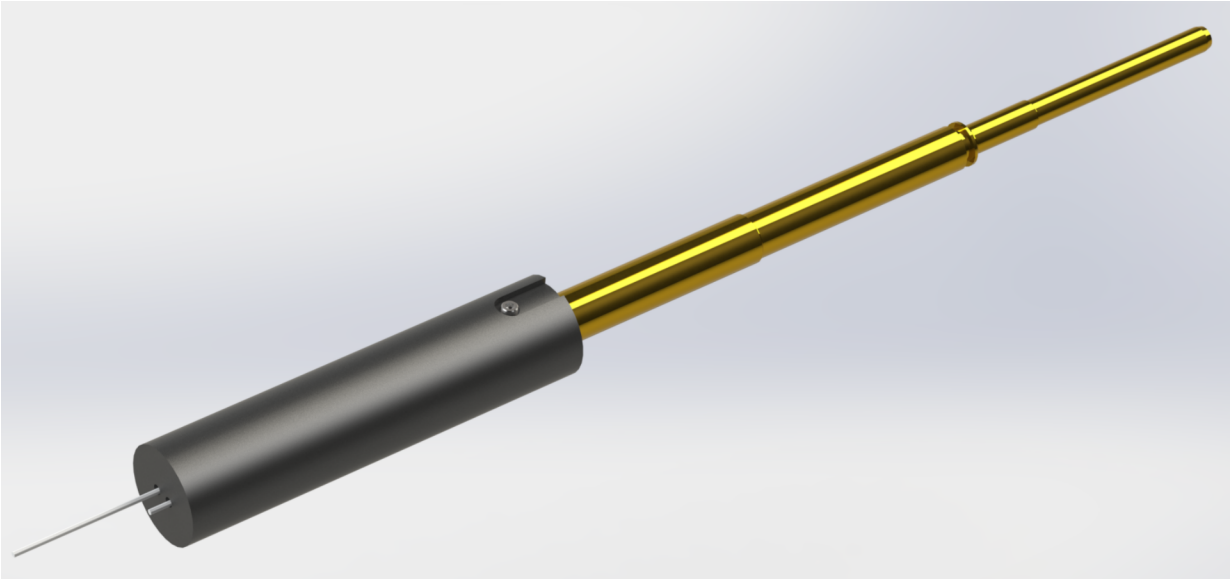

Figure 2.3: Rendered depiction of the basic design for the sample holder arm (tip not shown). The handle (black) contains connections for the fluidic tubing, protected by a cover. The interior of the handle is shown in figure 2.7 on page 34.

2.2 Nanofluidic cell and holder tip development

The basic design features for the fluidic cell were chosen after a detailed literature review, summarized in section 1.2 on page 8; the first generation cell design is based on the cell developed by the Miller group at the University of Toronto. [15, 35] The overall size of the cell was constrained by the maximum size of the sample stage and the machining limits declared by STS: a cylinder with diameter 7 mm and length 16 mm was taken to be the

maximum size of the tip, including the cell, fluid channels, lid, screws, and sealing. The inlet and outlet features in the chips were sized to match the minimum size for the drilled channels in the tip (508 μm in diameter). The cell cross-section and the bottom chip plus spacer are shown in figure 2.4.

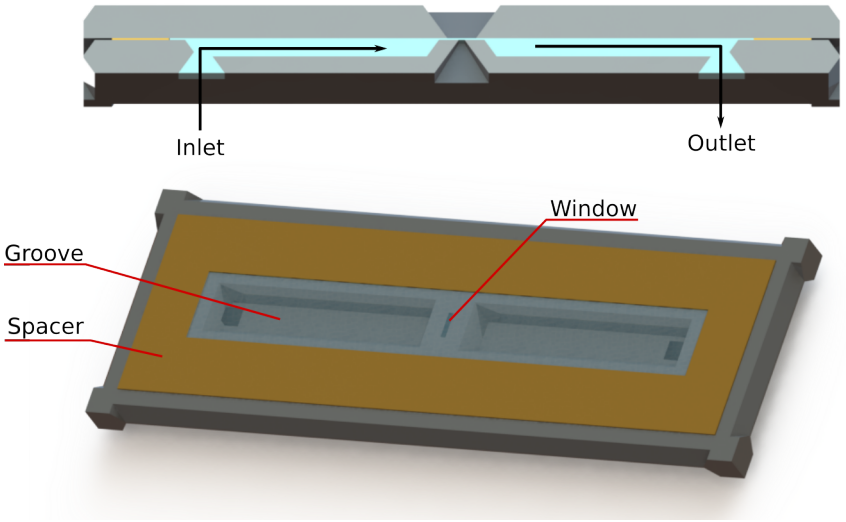

Figure 2.4: (**Top**) Cross-section of the nanofluidic cell, with arrows indicating flow direction. (**Bottom**) Depiction of the bottom chip, with spacer and fluid. Note that the flow path is much narrower in the vicinity of the window; this allows the sample thickness at the electron beam to be small, while reducing resistance to flow in the rest of the cell. Each chip is 2.5 mm wide by 6.8 mm long, and is made from 0.300 mm thick Si.

300 μm thick {100} Si was chosen as the wafer material for the cell, with Si_3N_4 windows. Si_3N_4 was chosen rather than low-stress Si_xN_y in order to minimize window deformation. [36] Unlike the square windows used in the Mueller *et al.* design, the windows were rectangles with an aspect ratio of at least 5:1; this ensured that the window deformation would be limited by the narrow dimension. [13,15] Three different window sizes were tested: 250 μm by either 10, 25, or 50 μm, with a thickness of 20 nm or 50 nm. 10 nm thick windows

were also considered originally, but work led by Ariel Petruk on analogous cells revealed that 10 nm Si_3N_4 did not survive the KOH etching conditions used. To aid in alignment, the windows on the top and bottom chips were perpendicular to each other (forming a + shape when aligned). Of the ten available metals for EBE deposition, Ti was chosen for its inertness, non-ferromagnetic properties, and its relatively low melting point, which would allow the cells to be baked and form a seal, similarly to the Zheng group stationary cell. [34]

O-rings were chosen as the main method of sealing the nanofluidic cell: one O-ring to seal each of the inlet and outlet, one O-ring surrounding the entire cell, and an O-ring around each window to distribute pressure and to help stop any leaks from reaching the vacuum chamber of the STEM. The grooves for the O-rings have no internal wall (with the exception of the O-ring surrounding the entire cell), to avoid problems with machining. When the lid is fully screwed on (and touching the top surface of the tip), all O-rings should be compressed approximately 25 % and the microchips should not touch either the lid or the tip. The entire assembly is shown in figure 2.5 on page 32.

2.2.1 Photomask design for first generation cells

Before the nanofluidic cells could be fabricated, a set of masks had to be designed for photolithographic patterning of the features. In order to account for the anisotropic KOH etching step (discussed further in section 5.1.2 on page 69), a pair of equations was derived from the etching geometry shown in figure 2.6 on page 33. Once feature sizes were calculated, the photomasks were designed using LayoutEditor Basic Version (LayoutEditor), and were manufactured by the University of Alberta nanoFAB. All of the finished mask designed are shown in appendix B on page 136.

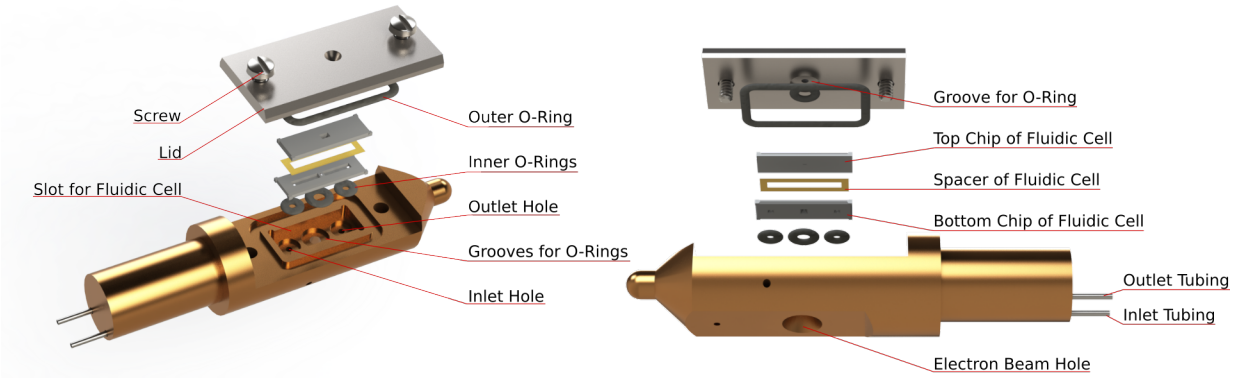

Figure 2.5: Depiction of the holder tip assembly, exploded to show each component. The inlet and outlet tubing would be longer in reality, travelling the entire length of the sample holder. The slot for the fluidic cell is sized such that the chips should fit snugly; the round "ears" extending from the corners of the slot allow space for pointed tweezers to remove the cell, as well as making the machining easier. The O-ring grooves in the slot and in the lid are designed such that the O-ring will compress primarily towards the centre of the groove; all O-rings used in the design have the same cross-section, and should therefore compress at the same rate. The electron beam holes (both in the lid and the tip) have conical profiles to allow tilting of the holder up to 20° without occluding the beam. The outer O-ring is actually round when not held in place by its groove. The small holes visible on the sides of the tip are from drilling the inlet and outlet channels, and would be filled in during manufacturing.

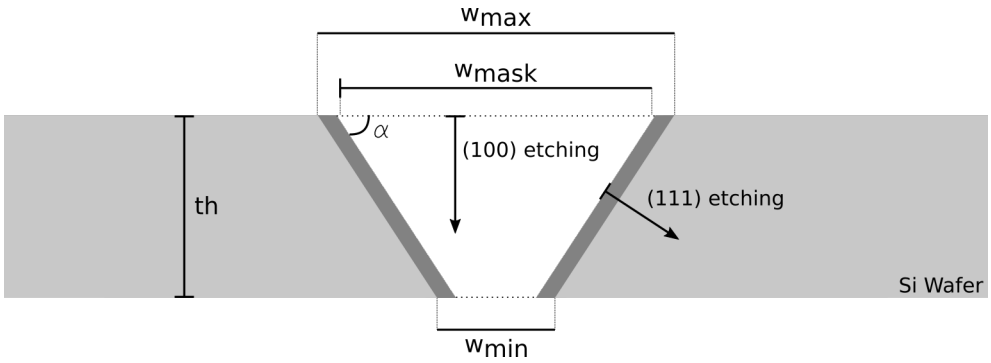

Figure 2.6: KOH etching geometry, showing a cross-section along a silicon (110) plane. Equations (2.1) and (2.2) were derived from this figure.

$$w_{\text{mask}} = w_{\text{max}} - 2\,th\,x, \qquad \text{where } x = \frac{s_{(111)}}{s_{(100)}} \tag{2.1}$$

$$w_{\text{mask}} = w_{\text{min}} - 2\,th\,(x - y), \qquad \text{where } y = \arctan(\alpha) \tag{2.2}$$

Where w_{mask} is the required mask feature size for an etched feature with maximum size w_{max} and minimum size w_{min}, th is the feature depth (typically equal to the wafer thickness), α is the angle between the {100} and {111} silicon crystal planes (54.74°), and s is the etch rate for the indicated plane. Note that for a given set of etching conditions (i.e. solution concentration and temperature), x and y are both constant. Either equation can be used to calculate the appropriate mask feature size for a given chip feature; whichever equation was more convenient was used.

2.3 Sample holder handle design

The handle of the sample holder, shown in figure 2.7 on page 34, houses the connections between the steel capillary tubing and the standard polyether ether ketone (PEEK) tubing used outside of the STEM. PEEK tubing sleeves on the ends of the capillary tubing increase

its outer diameter (OD) to 1/32", which allows the use of reducing unions to convert to 1/16" OD tubing (a very common size for fluidic applications). This design allows the PEEK tubing to be easily changed without damage to the steel capillary tubing. As suggested by STS, the handle will be made of Delrin (a light-weight, durable, easy to machine plastic).

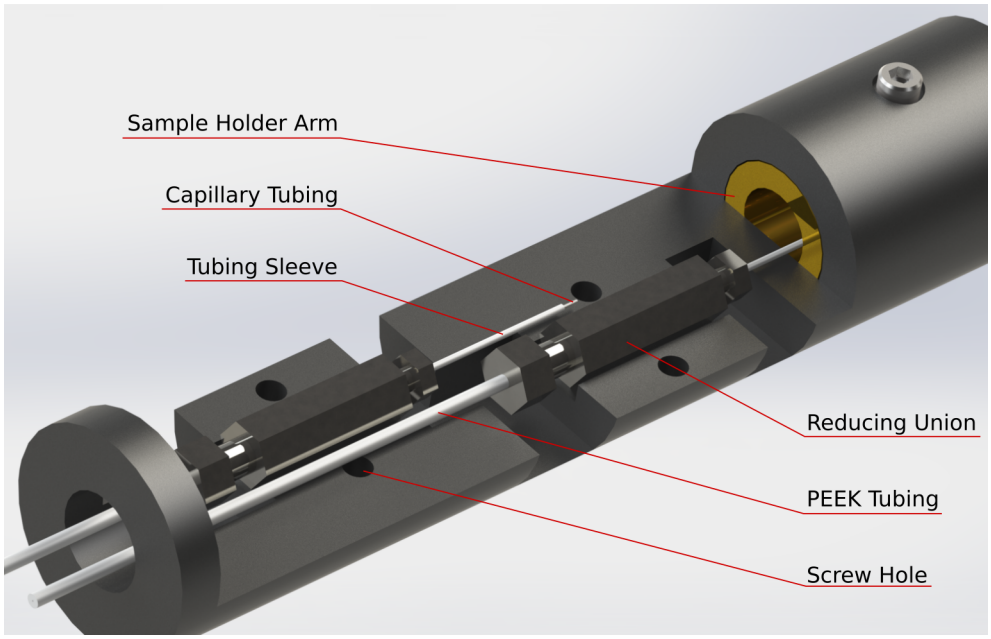

Figure 2.7: The handle (made of Delrin, a plastic material) slides over the end of the metal holder arm, and is secured in place with a screw. Two capillary tubes (316 stainless steel, 250 μm ID) run through the holder arm, from the inlet and outlet of the tip to the reducing unions in the handle. Tubing sleeves (PEEK) are placed over the ends of the capillary tubes to increase their OD to 1/32". The reducing unions (stainless steel, purchased from Valco) connect 1/32" tubing to 1/16" tubing, which is a standard size. Small brackets (not shown) would hold the reducing unions in place, and screw into the holes shown. The cover slides over the outside of the handle, and is secured by another screw.

2.4 Putting it all together

At this stage, a "model holder" was commissioned from STS: a brass block approximately 5 cm by 5 cm by 1 cm, with inlet and outlet channels leading to the same features as the sample holder tip (slot for nanofluidic cell, O-ring grooves, screw holes). Each flow channel terminates in a threaded port, which accepts a standard nut and ferrule tubing connection. The main function of the piece is to perform bench top tests with the fluidic cell, including flow tests to ensure that no leaks occur. Machining the tip features into an easily handled block was significantly less difficult than manufacturing the full sample holder, but allowed for much of the same bench top testing to be done. Photographs of the model holder are shown in figure 2.8.

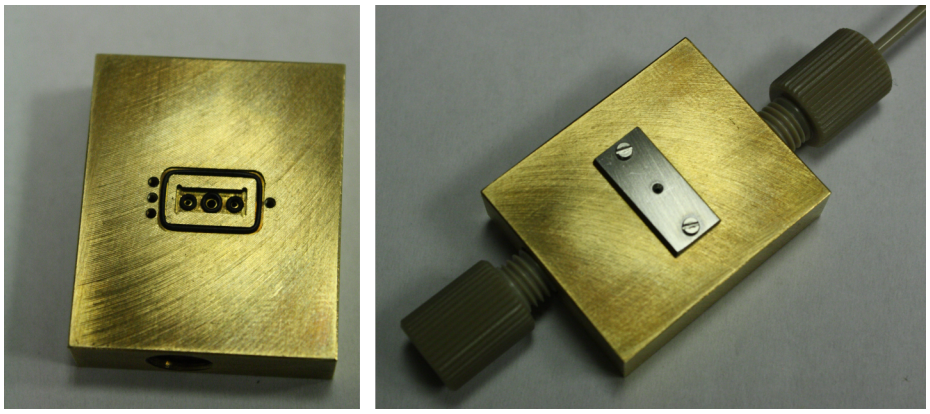

Figure 2.8: This model holder has the same detailed features as the holder tip design (e.g. the inlet and outlet channels, O-ring grooves, and lid), contained in a block large enough to handle easily. The extra screw holes visible on the left side of the left-hand photograph were placed to accommodate a lid with three screws (two on one side, one on the other side), in case one screw per side was found to be insufficient. The piece itself is brass, with stainless steel lid and screws. It also features a 10-32 threaded port for each flow channel, allowing standard fluidic tubing to be connected. Machining was done by University of Waterloo STS.

The deformation behaviour of the windows was examined by Ariel Petruk, using a surface profiler. The model holder was used to apply air pressure inside the cell to study window deformation, and also to secure chips for stress tests of the windows (i.e. increasing the force from the profiler tip until the window fractured). The deformation profiles for 50 nm thick windows are shown in figure 2.9 on page 37. As expected, window deformation increases as the pressure inside the cell increases. Deformation towards negative values is caused by the force applied by the profilometer tip. Assuming that the effects are additive, at a relative pressure of 150 kPa the window bulged outwards by approximately 110 nm without breaking.

Flow of liquid through the cell was tested by assembling the cell in the model holder and connecting a syringe pump filled with deionized (DI) water. Unfortunately, leaks occurred during all tests run. Due to the lack of appropriate microchip storage at the time (chips stored loose in a wafer cassette), many windows were broken before tests began. Given the small window size, the integrity of the windows could not be visually confirmed in the lab; as such, it was unclear if the cell windows were broken by the flow of water, or if they were already broken when the test began. After appropriate storage trays were purchased, wafers were inspected with a VLM upon completion, after cleaning (if applicable), and after separation into individual chips. The status of each window examined was recorded in a "map" for each wafer. Comparison of different wafer maps suggested that sonication of fully etched wafers caused windows to break; table 2.1 presents this data.

In order to avoid sonication of wafers once wet etching was complete, it was decided that the spacer should be deposited onto the top wafers before KOH etching, as the lift-off process used for spacer deposition requires sonication. Of the metals available for EBE deposition, only Au was known to resist KOH etching. [19] A batch of wafers with Au spacers was fabricated; while the Au did survive etching, there were small, round defects

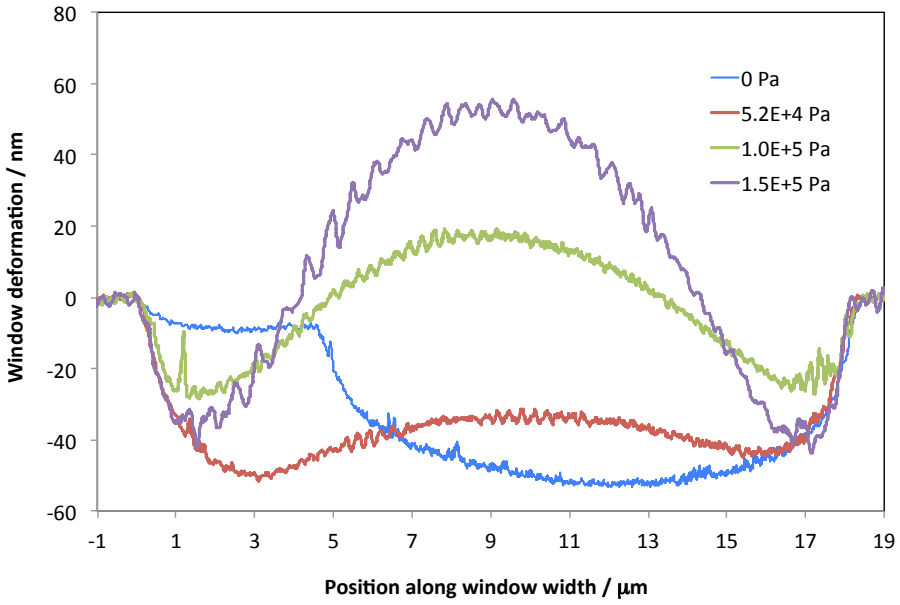

Figure 2.9: Window deformation profiles, collected by Ariel Petruk. Windows measured were approximately 18 µm by 250 µm in size, made from 50 nm thick Si_3N_4. Measurements were made with a Veeco Dektak 150 surface profiler, using a tip force of 0.3 µN, with a 5 nm lateral step size. The pressure listed for each series indicates the interior pressure of the cell relative to ambient conditions. Pressure was adjusted by pumping air into the system with a syringe.

Number of chips	Top wafer	Bottom wafer
Total	241	255
Initially intact	140	196
Intact after cleaning	5	189
% Broken initially	42	23
% Broken by cleaning	96	4

Table 2.1: A comparison of the number of broken windows on two different wafers, each with 20 nm thick Si_3N_4. Cleaning method for the top wafer: rinse with DI water and then isopropyl alcohol (IPA), sonicate in IPA for 6 min, rinse with DI water, and dry with N_2. The top wafer was also sonicated during the lift-off process, after KOH etching. Cleaning method for the bottom wafer: rinse with DI water, IPA, rinse again with DI water, and dry with N_2. The bottom wafers were not sonicated after being etched to completion. Note that a full wafer should contain 388 microchips; the missing chips are due to sections of the wafer breaking off due to damage during fabrication.

visible by eye. Surface profilometry and VLM results led to the conclusion that these defects were bubbles, caused by KOH penetrating the Au layer and etching the underlying Si. See figure 2.10 on page 39 for a sample surface profile. The bubbles were not evenly distributed: on a given wafer, some areas had no visible defects while other areas had many, and the wafers were not equally affected.

As evident in figure 2.10 on page 39, some of the defects were significantly larger than the desired spacer height. Consultation with Nathan Nelson-Fitzpatrick (senior process engineer in the University of Waterloo NanoFab) and literature review suggested a possible method to eliminate this problem: increase the surface energy of the Au adatoms by incorporating ion beam bombardment and/or heating during EBE, thus improving the film quality. These solutions were not tested, as an alternate (and more generally applicable) spacer method was developed for the second generation of the nanofluidic cell; refer to section 5.3.2 on page 81 for more details.

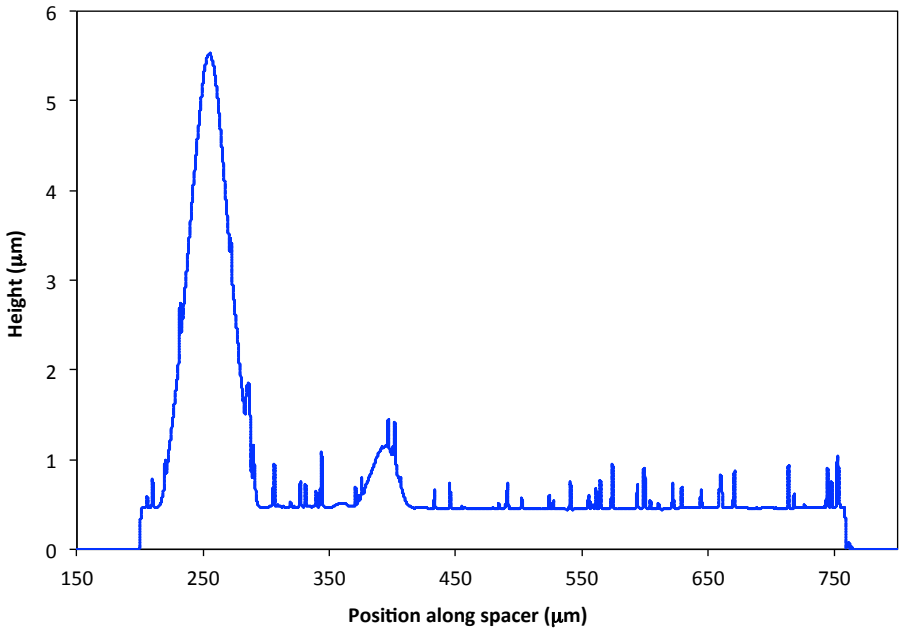

Figure 2.10: Surface profile of defects in Au spacer after KOH etching. The two large peaks (at approximately 250 µm and 400 µm position, respectively) show bubbles under the spacer. Similar bubbles were visible by eye at various locations on the wafer. Measurements were made with a Veeco Dektak 150 surface profiler, using a tip force of 10 µN, with a 44 nm lateral step size.

Chapter 3

Flow simulations

Simulations of the flow behaviour inside the first generation nanofluidic cell were performed to better understand the system, and to search for ways to achieve the best possible microchip design. This work was initiated before the switch in spacer materials for the first generation cells, and resulted in the transition from the first generation NFS to the second generation. All simulations were performed using the commercial physics modelling software COMSOL Multiphysics 5.2 (COMSOL).

3.1 Geometries and mathematical models

3D models of the interior volume of the nanofluidic cell were used to simulate the fluid behaviour; these shapes (referred to hereafter as "geometries") represent only the fluid itself, without including any part of the nanofluidic cell. It should be noted that due to a minor error when initially reconstructing the first generation cells in SW, the geometry used is slightly different from the actual shape. In reality, the inlet and outlet have a

smaller footprint, and the flow channels are less narrow at the bottom. The effect of this error should be minimal, as the inlet and outlet themselves were not simulated and the overall shape of the actual flow channels is similar to that used. In addition, the more critical results came from simulations of the "viewing area" (figure 3.3 on page 42), whose shape was correct. The same coordinate system was used in all simulations, as indicated

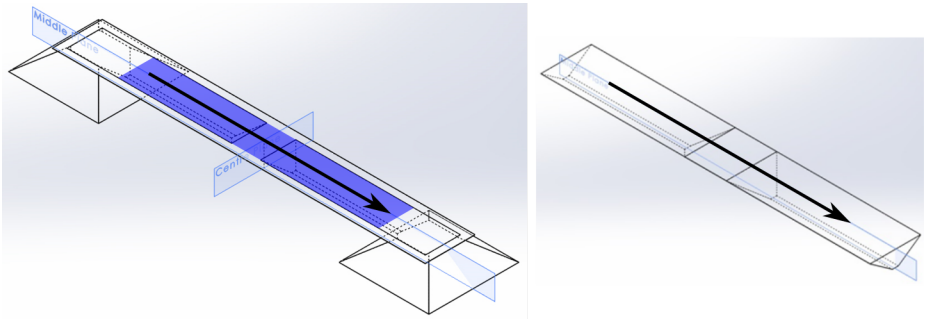

Figure 3.1: (**Left**) Shape of the fluid inside the first generation cell, as used for simulations. The area highlighted in blue is the fluid geometry used for some COMSOL simulations, referred to as the "reduced fluid area." (**Right**) Highlighted area, which includes most of the flow channel grooves and the area immediately surrounding the window. Arrow indicates flow direction.

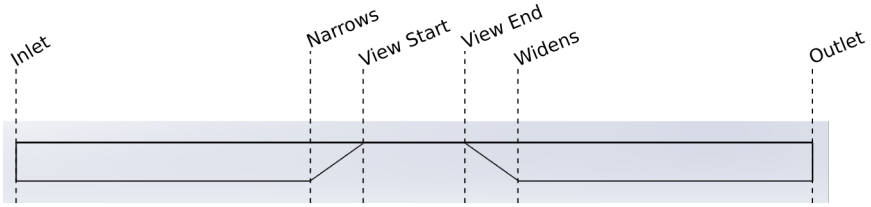

Figure 3.2: A side view of the reduced fluid area (as shown in figure 3.1). "Narrows" and "Widens" refer to where the grooves in the flow channel slope to meet the viewing area, which is denoted by "View Start" and "View End." These labels will be used to annotate and discuss results in the following sections.

on 3D results from COMSOL. All Cartesian coordinate values are given in units of μm.

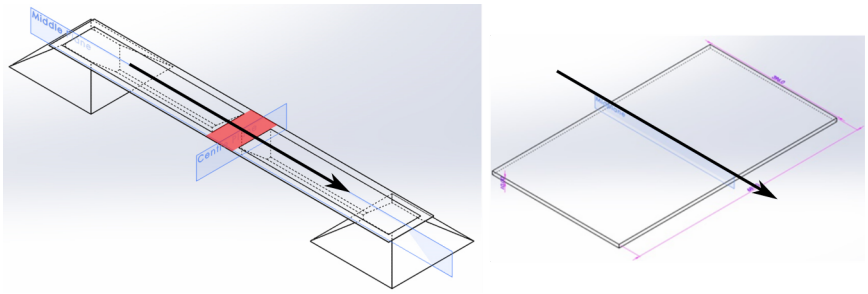

Figure 3.3: **Left**) Shape of the fluid inside the first generation cell, as used for simulations. The area highlighted in red is the fluid geometry used for some COMSOL simulations, referred to as the "viewing area." (**Right**) Highlighted area, which includes the area immediately surrounding the window. The shape is a simple rectangular prism. Arrow indicates flow direction.

Flow travels from the inlet plane towards the outlet plane; both are yz planes, and the inlet plane is always located at $x = 0$. Note that the planes referred to the inlet and outlet will vary based on the geometry used, but are always located at $x = 0$ and the maximum x value. The $\hat{y}$ axis describes the width of the cell, with $y = 0$ being the flow path (in the $\vec{x}$ direction) either through the middle of the cell (for the reduced fluid area) or along one wall (for the viewing area). The $\hat{z}$ axis describes the height of the cell, with the maximum z value being the height of the spacer (i.e. up to the top window), and $z = 0$ being the plane corresponding to the bottom window.

For fluidic systems with a Reynolds number much less than one (R_e, defined by equation (3.1)), inertial forces have a negligible contribution to the fluid dynamics, while viscous forces are the dominant factor. This allows the inertial term of the Navier-Stokes fluid dynamics equation to be neglected, leaving only the Stokes equation. [44] So-called Stokes flow (or creeping flow) is simpler to calculate, and therefore can be simulated more quickly

and easily.

$$R_e = \frac{\rho L U}{\mu} \tag{3.1}$$

Where ρ is fluid density, L is a characteristic length of the fluidic system, U is a characteristic velocity of the system, and μ is dynamic viscosity. [44] Due to the height of the spacer (variable depending on desired sample height, but typically 0.5 μm or less), the fluid geometries used were all well within the creeping flow regime. The Reynolds number was calculated as an output for each study, and was confirmed to be sufficiently small; the maximum Reynolds numbers for each simulation were generally below 10^{-3}. Studies of each geometry (figure 3.1 on page 41 and figure 3.3 on page 42) were replicated with laminar flow (described by the Navier-Stokes equation), albeit with a coarser mesh; the results confirmed that the creeping flow model was sufficient. Equations (3.2) and (3.3) describe the mathematical model used for creeping flow in COMSOL.

$$\nabla \cdot \overbrace{\left[-p\mathbb{I} + \mu\left(\nabla\vec{u} + (\nabla\vec{u})^{\mathrm{T}}\right)\right]}^{\mathbb{P}} + \vec{F} = 0 \tag{3.2}$$

$$\rho\nabla \cdot (\vec{u}) = 0 \tag{3.3}$$

Where p is pressure, $\mathbb{I}$ is an identity matrix, $\vec{u}$ is fluid velocity, and $\vec{F}$ is applied body force. $\mathbb{P}$ is a Cauchy stress tensor, representing viscous and pressure stresses. [44] For the creeping flow model, ρ is assumed to be constant (i.e. incompressible fluid).

A no-slip boundary condition was used, which set the fluid velocity to zero at each wall (i.e. the fluid does not slide along the walls). This is appropriate for most systems. [44] The pressure values were always calculated relative to a reference pressure, $p_{\mathrm{ref}} = 101.325$ kPa. The outlet pressure, p_{out}, was set to zero as an initial condition, indicating that the fluid was exiting the cell at the ambient system pressure. The initial flow velocity at the inlet

plane, u_0, was always in the $\vec{x}$ direction and was set as an initial condition.

3.2 Simulation results

All of the results shown were simulated with creeping flow at a steady state.

3.2.1 Results in reduced fluid area

Simulation of flow through the entire reduced fluid area (figure 3.1 on page 41) provided an overall picture of the flow behaviour. As shown in figure 3.4 on page 45 and figure 3.5 on page 46, the pressure is nearly constant in each of the inlet and outlet channels, with linear decrease in pressure across the viewing area.

The flow velocity in the inlet channel is shown in figure 3.6 on page 47; figure 3.7 on page 48 shows the flow velocity in the inlet channel as it narrows into the viewing area. As the flow was much faster across the viewing area (due to the decreased cross-section), the scale was capped (or the viewing area was excluded) to preserve details in the inlet and outlet.

The results from this simulation indicated that the most critical behaviour occurs in the viewing area, and that the pressure in the outlet channel is very low relative to the inlet pressure.

3.2.2 Parametric sweep of initial flow velocity

A series of four studies was done to investigate the effect of initial flow rate on the pressure drop across the viewing area. The flow rates used were 0.0025 m/s, 0.005 m/s, 0.010 m/s,

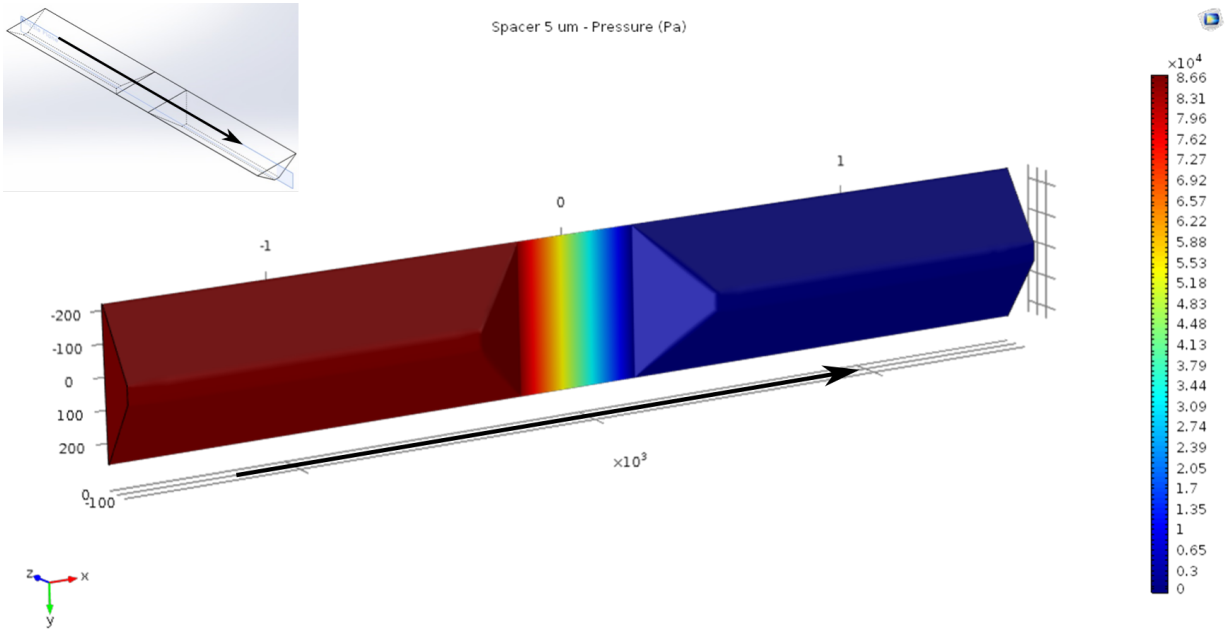

Figure 3.4: Pressure in the reduced fluid area (shown at top left) at steady state, with an initial flow velocity of 0.025 m/s in the $\vec{x}$ direction. The arrow indicates flow direction. Spacer height was 5 µm. The scale bar on the right hand side ranges from 0 Pa (dark blue) to 86.6 kPa (dark red).

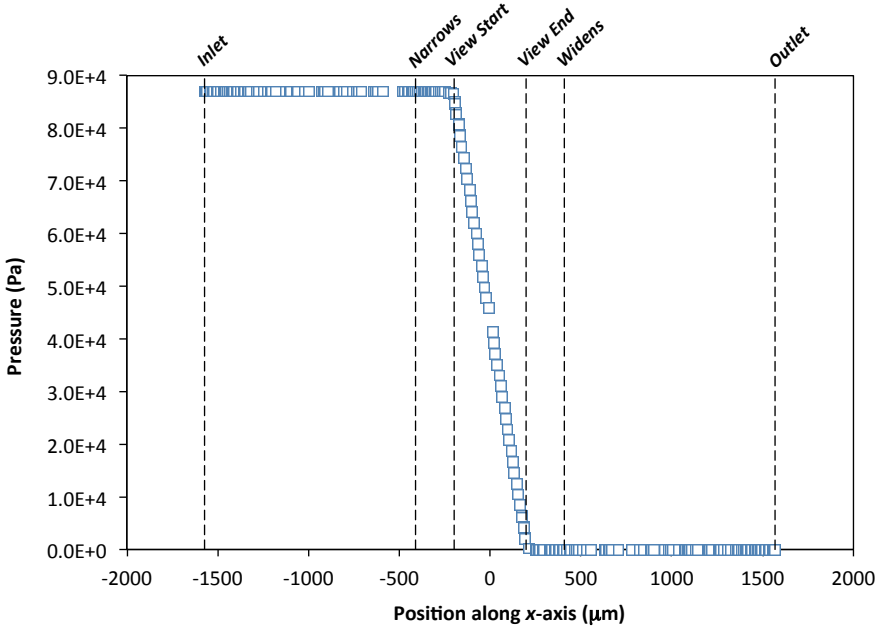

Figure 3.5: Profile of pressure vs. position along the flow path in the reduced fluid area. This graph represents a slice along the centre line of figure 3.4 on page 45, showing only data points with y values in the range of -0.11 µm to $+0.11$ µm. Refer figure 3.2 on page 41 for the definitions of the labels. The spacer height was 5 µm, and the initial flow velocity was 0.025 m/s normal to the inlet. Note that the pressure in the inlet and outlet sections (where the flow channel shape is constant) is linear and, to a good approximation, constant. In the viewing area section, demarcated by "View Start" and "View End," the pressure decreases linearly from inlet to outlet. This profile was consistent across three different slices: $y \simeq 0$ (center, shown here), $y \simeq -100$ (halfway between the centre and edge), and $y \simeq -200$ (near the edge). Figure 3.4 clearly shows the y-axis at the inlet.

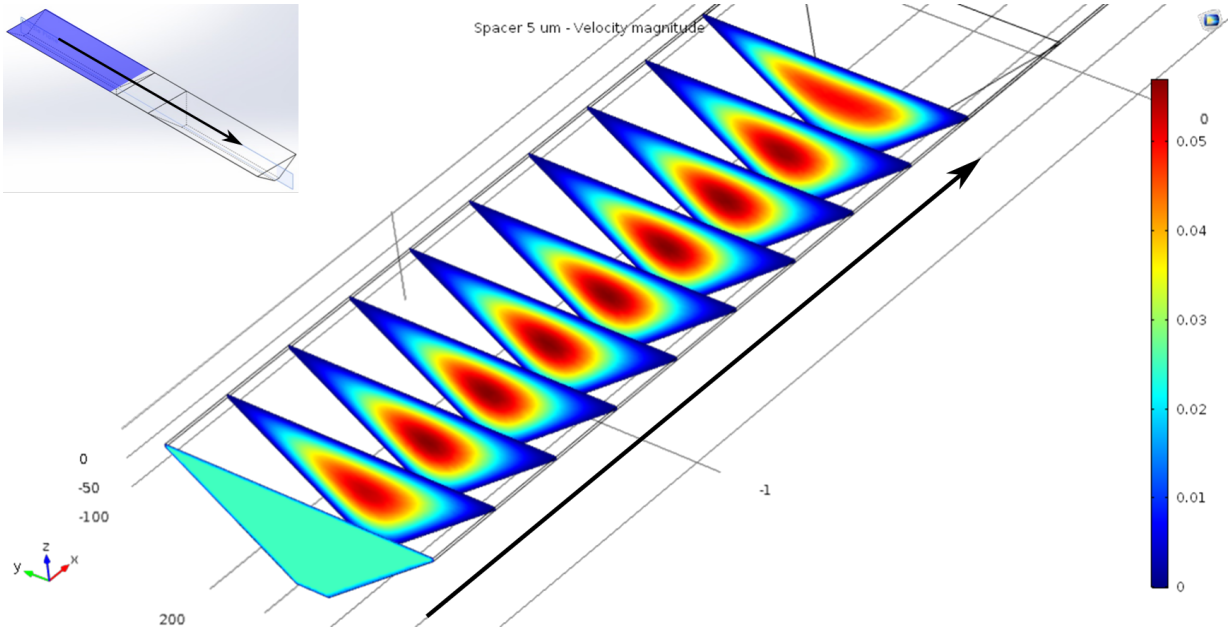

Figure 3.6: Flow velocity in the reduced fluid area (shown at top left, with the displayed area highlighted in blue) at steady state, with an initial flow velocity of 0.025 m/s. The arrow indicates flow direction. The scale bar ranges from 0 m/s (dark blue) to approximately 0.0575 m/s (dark red). Note that the flow rate goes to zero along the channel walls, as per the no-slip boundary condition.

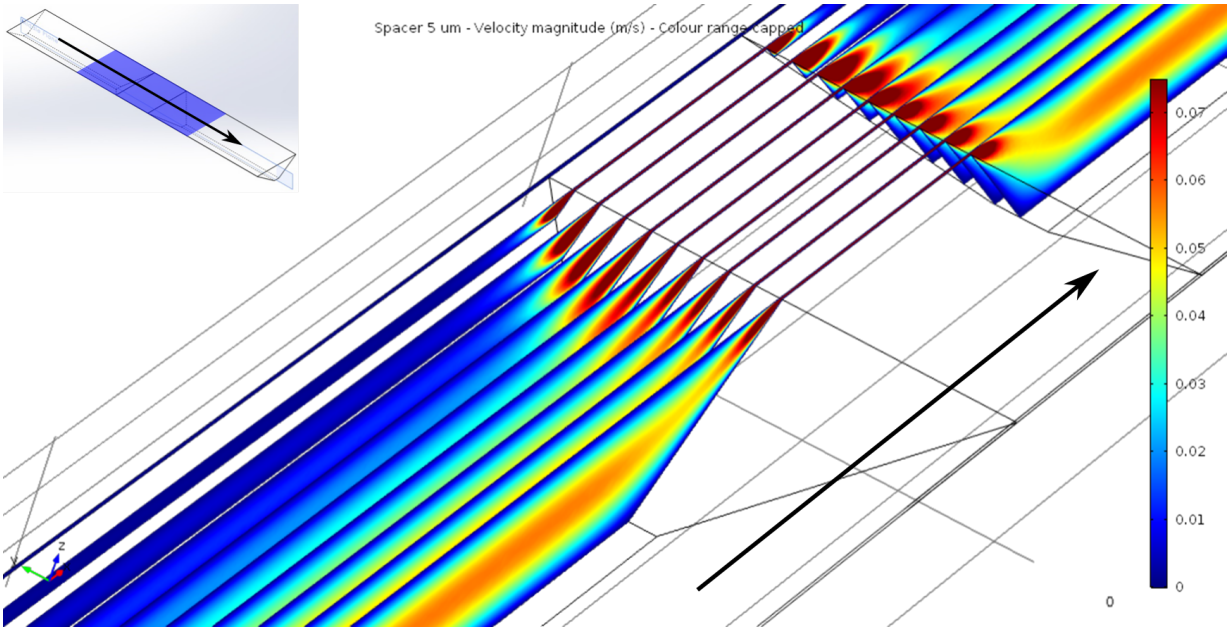

Figure 3.7: Flow velocity in the reduced fluid area (shown at top left, with the displayed area highlighted in blue) at steady state, with an initial flow velocity of 0.025 m/s. The arrow indicates flow direction. The scale bar ranges from 0 m/s (dark blue) to approximately 0.075 m/s (dark red); the velocity values in the viewing area were higher, but the scale was capped in order to preserve lower-flow details. Note that the flow rate goes to zero along the channel walls, as per the no-slip boundary condition.

and 0.025 m/s. An example of the 3D pressure results in shown in figure 3.8. The appearance of this graph was very similar for each initial flow velocity, and in all cases the results can be well represented by a slice taken from the middle of the volume, as shown in figure 3.9 on page 50.

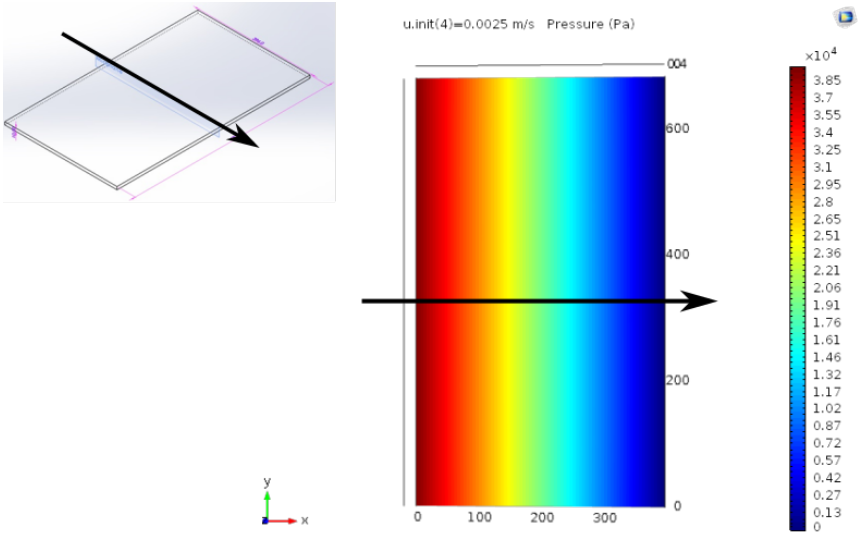

Figure 3.8: Pressure in the viewing area, from a study comparing four different initial flow rates. Initial flow velocity was 0.0025 m/s in the $\vec{x}$ direction (normal to the inlet). Spacer height was 0.5 µm, flow channel path length was 396 µm, and the width was 681 µm (in the $\vec{y}$ direction). Scale bar ranges from 0 Pa (dark blue) to approximately 38.5 kPa (dark red). The pressure decreased linearly from inlet to outlet.

As expected from the data in figure 3.5 on page 46, the pressure decreased linearly across the width of the viewing area. A plot of the pressure drop vs. the initial flow rate is shown in figure 3.10 on page 51, with the linear regression result given in equation (3.4). From these results, it can be seen that the magnitude of the pressure drop increases with

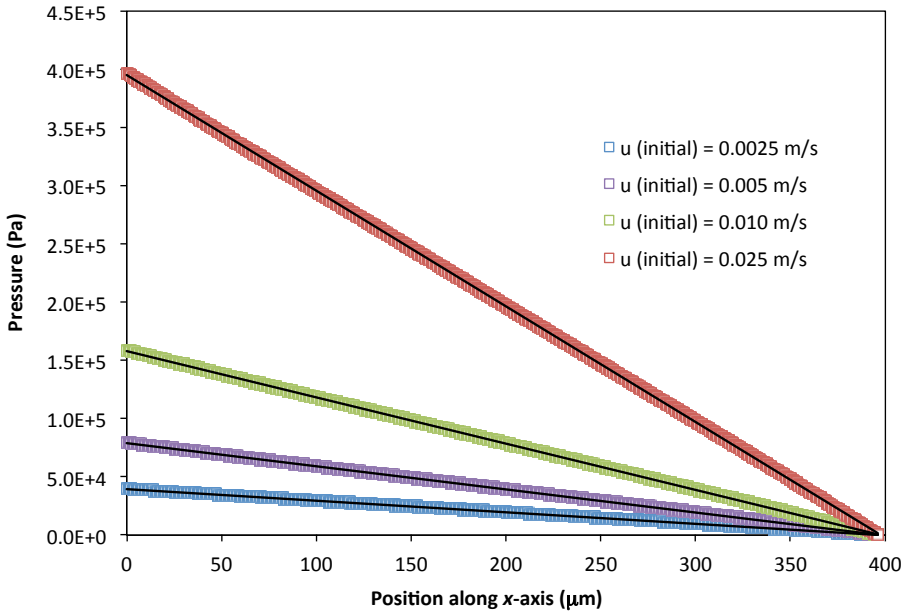

Figure 3.9: Pressure vs. position along flow path with varying initial flow rate. Each data series includes only data points with y values in the range of 339.75 µm to 341.25 µm (a slice across the middle of the viewing area, as pictured in figure 3.8 on page 49). Linear regression data is presented in table 3.1.

Table 3.1: The linear regression values for each series in figure 3.9, with their relative standard errors (RSEs). Note that the intercept is equal to the pressure at the inlet.

$\vec{u_0}$ (m/s)	Slope (Pa/µm)	RSE (%)	Intercept (Pa)	RSE (%)	R^2
0.0025	-99.341	0.007	39513	0.004	0.99998
0.005	-198.69	0.007	79027	0.004	0.99998
0.010	-397.36	0.007	158053	0.004	0.99998
0.025	-993.41	0.007	395133	0.004	0.99998

increasing initial flow rate.

$$\Delta P[\mathrm{Pa}] = -1.58617 \cdot 10^7 \left[\frac{\mathrm{Pa}\cdot\mathrm{s}}{\mathrm{m}}\right] \cdot \vec{u_0} \left[\frac{\mathrm{m}}{\mathrm{s}}\right] = -15.8617 \left[\frac{\mathrm{Pa}\cdot\mathrm{s}}{\mu\mathrm{m}}\right] \cdot \vec{u_0} \left[\frac{\mu\mathrm{m}}{\mathrm{s}}\right] \tag{3.4}$$

Where ΔP is the pressure drop across the viewing area ($p_{\mathrm{out}} - p_{\mathrm{in}}$), and $\vec{u_0}$ is the initial flow rate. The RSE of the slope is 0.0001 %.

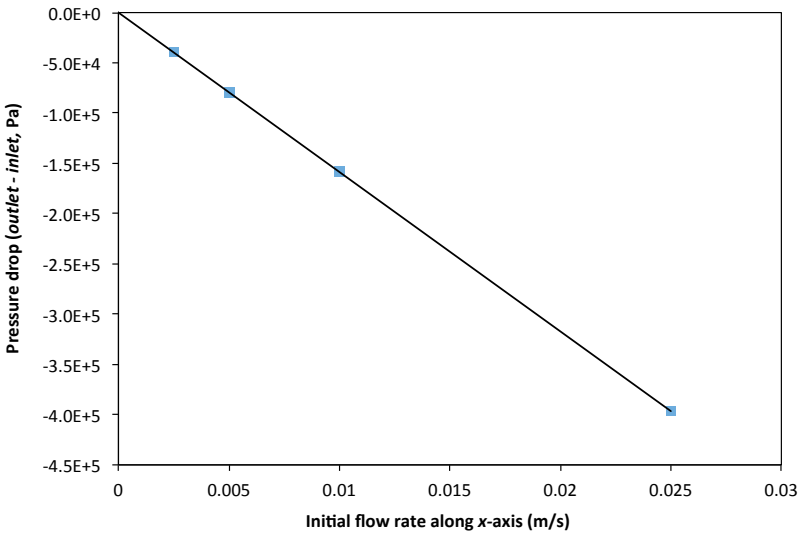

Figure 3.10: Pressure drop across the viewing area vs. the initial flow rate: the difference between the final and initial pressures from each series in figure 3.9 on page 50 was plotted against the initial flow rate for that series. A linear regression gave the function in equation (3.4).

3.2.3 Parametric sweep of flow path length

Flow through the viewing area (with an initial flow rate of 0.025 m/s) was simulated for four different path lengths (i.e. changing the length of the viewing area, in the $\vec{x}$ direction).

The path lengths ranged from 40 µm to 396 µm, the actual length of the viewing area in the first generation cells. The width (Δy) and height (Δz) of the viewing area were kept constant at 681 µm and 0.5 µm, respectively. The 3D graphs of pressure throughout the simulated area were all visually similar to both each other and to figure 3.8 on page 49; as such, they will not be shown here. The pressure profile along the middle of the viewing area is shown for each length in figure 3.11 on page 52.

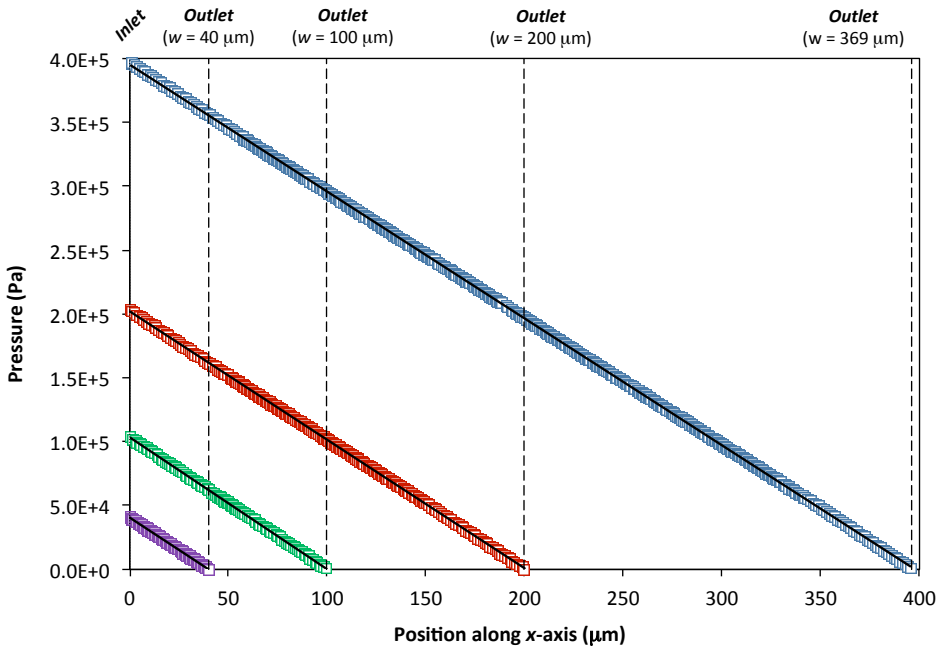

Figure 3.11: Pressure vs. position along the flow path for different path lengths, with an initial flow rate of 0.025 m/s. Each data series includes only data points with y values in the range of 340.25 µm to 340.75 µm (a slice across the middle of the viewing area, as pictured in figure 3.8 on page 49). The slope was approximately equal for each series; linear regression data is presented in table 3.2.

As indicated by the data in figure 3.11 and in figure 3.12 on page 54, the pressure drop across the viewing area increases with viewing area length. Upon analysing the linear

Table 3.2: The linear regression values for each series in figure 3.11 on page 52, with their RSEs. Note that the intercept is equal to the pressure at the inlet. For a given initial flow rate (in this case 0.025 m/s), the slope is equal to $-P_{\text{in}}/\Delta x$.

Length (µm)	Slope (Pa/µm)	RSE (%)	Intercept (Pa)	RSE (%)	R^2
40	-1013.93	0.005	40565	0.003	0.999998
100	-1032.8	0.01	103406	0.01	0.999993
200	-1005.5	0.03	202020	0.01	0.99994
396	-993.3	0.01	395120	0.01	0.99998

regression data from figure 3.11 (shown in table 3.2), it was found that the slope of each regression is equal to the initial pressure divided by the path length. The linear regression for the data in figure 3.12 on page 54 is given in equation (3.5).

$$\Delta P[\text{Pa}] = -1003 \left[\frac{\text{Pa}}{\mu\text{m}}\right] \cdot \Delta x[\mu\text{m}] \tag{3.5}$$

Where ΔP is the pressure drop ($p_{\text{out}} - p_{\text{in}}$) in Pa, and Δx is the path length (i.e. length of the viewing area) in µm. The RSE of the slope is 0.4 %.

3.3 Lessons learned from simulations

From the simulation results, it was determined that the thinnest part of the flow channel (where the windows are) is the most critical to flow behaviour in the fluidic cell. The inlet channel (before narrowing) has an approximately constant, relatively high fluid pressure, while the outlet channel (after widening from the viewing area) has a pressure approximately equal to the pressure outside of the cell. The pressure decreases linearly across the viewing area for all conditions explored. The pressure drop across the cell increases (via increasing inlet pressure) with the length of the viewing area, and also with increasing

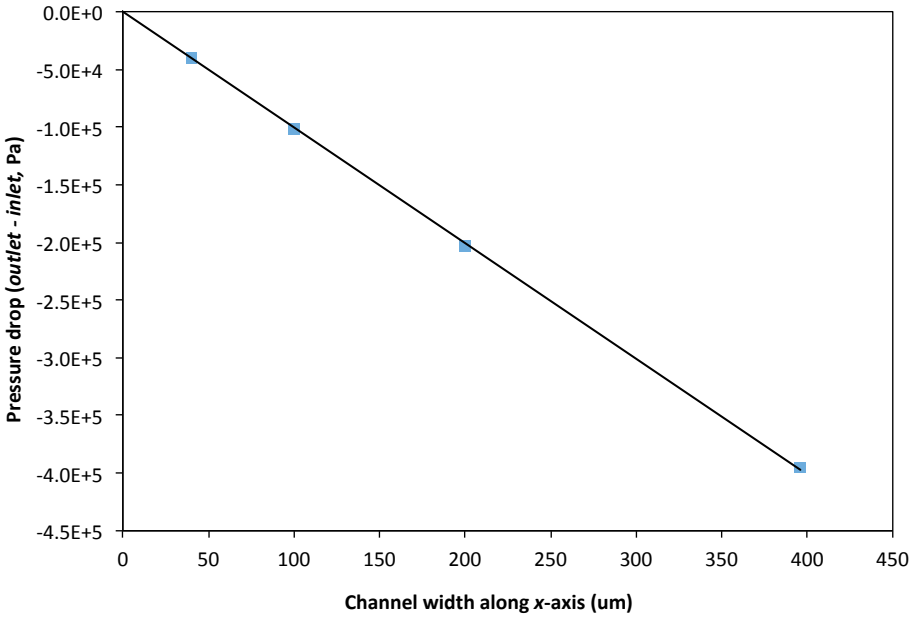

Figure 3.12: Pressure drop across the viewing area vs. viewing area length: the difference between the final and initial pressures from each series in figure 3.11 on page 52 was plotted against the path length for that series. A linear regression gave the function in equation (3.5).

initial flow rate. To minimize the fluid pressure in the cell, the flow rate should be kept low (within reason), and the portion of the flow channel with a small cross-section should be kept short. These design choices will help to prevent excessive pressure on the windows (and thus reduce the chance of window breakage), and also reduce the forces pushing the top and bottom chips apart.

Equations (3.4) and (3.5) provide the following relations:

$$\Delta P \propto \vec{u_0} \tag{3.6}$$

$$\Delta P \propto \Delta x \tag{3.7}$$

By combining these two relations, we obtain:

$$\Delta P = C \cdot \vec{u_0} \cdot \Delta x \tag{3.8}$$

Where C is a constant for a given liquid with creeping flow. Multiplying and dividing by the cross-sectional area of the flow channel, A, allows the pressure drop to be calculated in terms of volumetric flow rate, $\vec{Q}$.

$$\Delta P = \frac{C(A \cdot \vec{u_0})\Delta x}{A} = \frac{C \cdot \vec{Q} \cdot \Delta x}{A} \tag{3.9}$$

The value of C for water (with the default properties assigned by COMSOL) was calculated by setting equation (3.9) equal to each of equations (3.4) and (3.5) and averaging the

resulting constants.

$$C_u = \frac{\left(-15.8617 \left[\frac{\text{Pa}\cdot\text{s}}{\mu\text{m}}\right]\right)}{\Delta x[\mu\text{m}]} = -0.04005488 \pm 0.00000005 \left[\frac{\text{Pa}\cdot\text{s}}{\mu\text{m}^2}\right] \tag{3.10}$$

$$C_{\Delta x} = \frac{\left(-1003 \left[\frac{\text{Pa}}{\mu\text{m}}\right]\right)}{u_0 \left[\frac{\mu\text{m}}{\text{s}}\right]} = -0.0401 \pm 0.0002 \left[\frac{\text{Pa}\cdot\text{s}}{\mu\text{m}^2}\right] \tag{3.11}$$

$$C = -0.04009 \pm 0.00009 \left[\frac{\text{Pa}\cdot\text{s}}{\mu\text{m}^2}\right] \tag{3.12}$$

Chapter 4

Second generation nanofluidic system: development and testing

The fluidic cell design presented in figure 4.1 on page 58 incorporates the lessons learned from the flow simulations and the larger, analogous chips into the first generation design (chapter 2). The inlet and outlet in the bottom chip are far larger than previously shown, leaving large areas of the flow path open directly to the holder (or more accurately, to the silicone mat sealing the system). Overall, the flow channel is more open, narrowing only in the immediate vicinity of the windows; this helps to reduce the pressure in the cell. The other important benefit of leaving large openings to the holder surface is that much of the force pushing the two chips apart is now directed onto the holder instead. The relatively tall angled walls of the inlet and the narrow "shelf" in the outlet were also designed take advantage of the in-flow to help press the cell together, while minimizing the area acted on by force pushing the chips apart.

The final version of the second generation nanofluidic cell is conceptually very similar

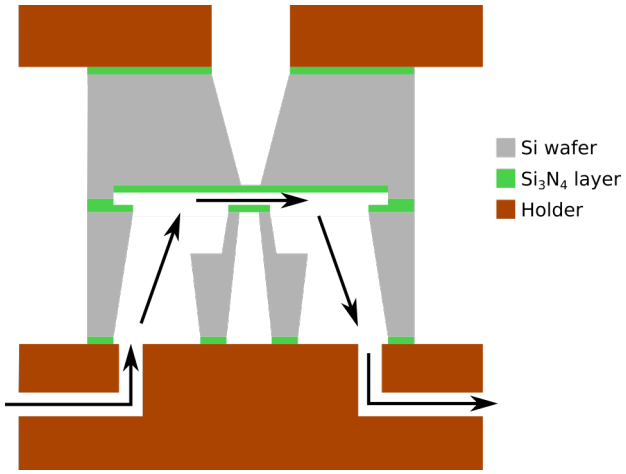

Figure 4.1: Cross-section of a variant cell design, representing an intermediate between the first and second generation designs. Note that this drawing is not to scale, and that sealing (e.g. O-rings) is not shown. The arrows represent liquid flow. The most important feature of this design is that the majority of the force exerted by fluid pressure either acts directly on the holder (due to the large inlet and outlet openings), or presses the two halves of the cell together (due to the slanted walls resulting from KOH etching).

to the design in figure 4.1 on page 58. The changes described in the following section stemmed from the requirements of the holder, rather than from problems with the cell design itself.

4.1 Meeting commercial standards

The first generation fluidic holder was designed with the assumption that a cylindrical holder tip was acceptable. In reality, the thickness of the sample holder tip is limited by the shape of the objective lens in the EM; what previously thought to be the maximum allowable *diameter* for the tip is in fact the maximum *width*. A typical STEM objective lens contains two conical polepieces with a gap between them, located just above and just below the sample (respectively). The polepieces are delicate, and the gap between them is an important factor in the focusing action of the lens; the sample holder must be carefully designed to avoid damage to the polepieces. [1] From consultations with HTC, the HD2000 STEM can accept holders with a tip with a maximum thickness of 2.2 mm above the sample plane and 2.0 mm below the sample plane, for a total thickness of 4.2 mm. The current standard for commercial TEMs and STEMs is a maximum tip thickness of 2.0 mm, centred vertically about the sample plane.

While a holder similar in style to the first generation holder could be made thin enough for use in the HD2000 STEM, it would not be feasible for modern commercial TEMs. In order to minimize the tip thickness, the shape of the nanofluidic cell was stretched asymmetrically as shown in figure 4.2 on page 60, allowing the inlet and outlet channels of the holder to terminate further from the end of the tip; figure 4.3 on page 61 shows the resulting holder design. Rather than connecting the outlet of the cell directly to the outlet channel of the holder (as in the first generation NFS), liquid will flow around the outside

of the cell to the outlet channel.

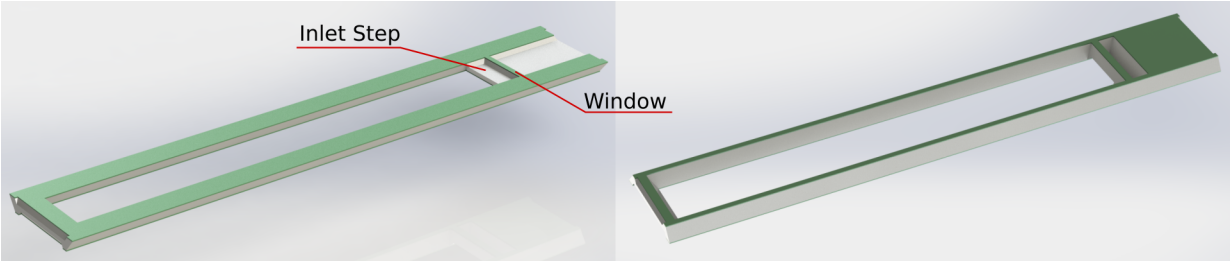

Figure 4.2: Renders of the bottom chip; the green layer represents the Si_3N_4. (**Left**) Window side (i.e. interior of the cell). (**Right**) Exterior of the cell. Note how the inlet extends throughout most of the cell length.

As tip thickness decreased and the length of the cell (and therefore the lid) increased, the strength of the lid became a greater concern. Ridges protruding downwards from the long sides were added (as seen in figure 4.6 on page 65) to provide more strength without increasing the overall thickness of the tip. Rounded ears on the short sides of the tip correspond to the curved walls of the tip, allowing the lid to be easily aligned and giving more space for the screws while removing less material from the holder.

Due to the extended inlet opening, a compressible silicone mat was chosen to seal the bottom of the nanofluidic cell. As can be seen in figure 4.6 on page 65, the mat is similar in size to the microchips, with two holes: the smaller hole corresponds to the inlet channel of the holder, while the larger hole aligns with the edge of the etched window feature and extends over most of the outlet length. A large O-ring surrounds the outside of the cell, as before. One smaller O-ring is placed around the top window, with a second O-ring placed symmetrically on the other end of the top chip for pressure distribution. To further distribute the pressure on both the lid and the fluidic cell, a graphite shim with the same desired thickness as the compressed O-rings could be used (as shown in figure 4.6 on page 65).

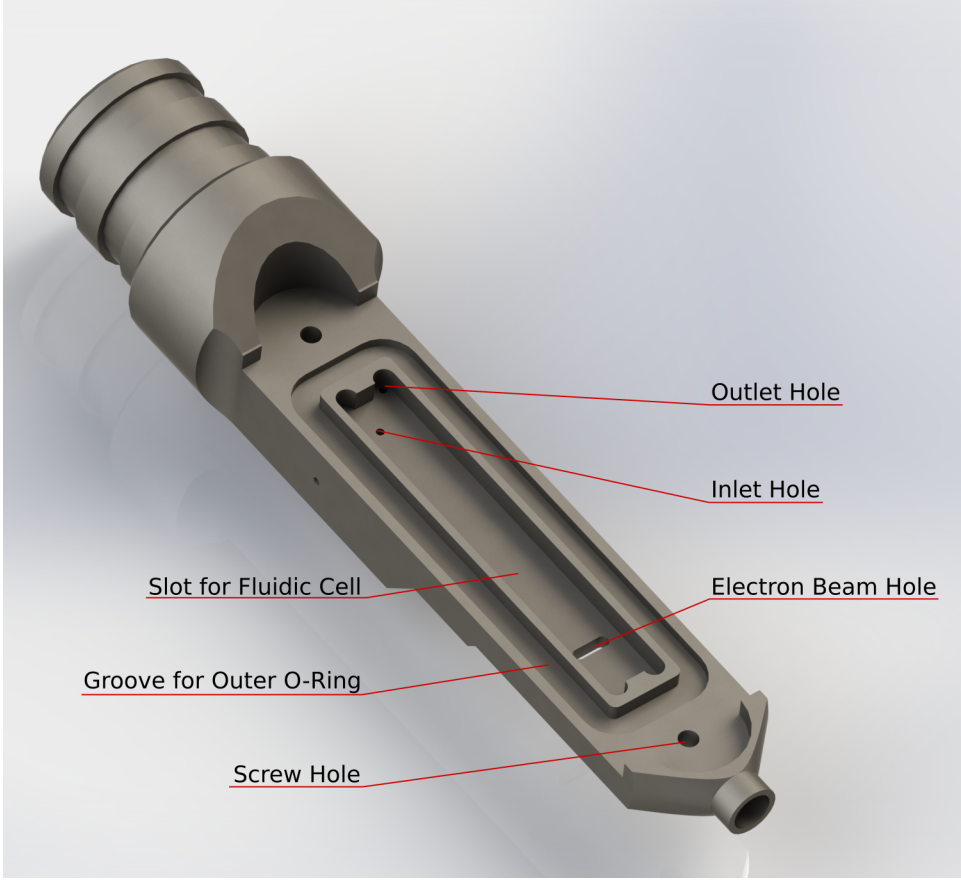

Figure 4.3: Render of the sample holder tip. Liquid from the inlet hole would flow up into the cell, and after passing through would travel around the outside of the cell from the cell outlet to the outlet hole of the tip. The edges of the chips are angled (due to KOH etching), which leaves space for liquid to flow. The outlet hole is located in the "ear" of the slot, ensuring it is not covered by the cell or the sealing mat (not shown). Note that the wall surrounding the slot for the fluidic cell is taller than the surface around the outside of the outer O-ring groove; this corresponds to an indentation in the lid, and allowed the edges of the lid to be thicker. The rounded cut-outs concentric with the screw holes accept the protruding ends of the lid, ensuring its proper alignment. The small hole visible on the side of the tip is from drilling the outlet channel, and would be filled in during manufacturing.

4.2 Nanofluidic cell development

As in the first generation NFS, 300 µm thick {100} Si wafers with 20 nm or 50 nm thick Si_3N_4 were used. In order to check the feasibility of a very long microchip, multiple exposures with photomasks from the first generation fluidic cell were made on a single wafer, using foil to cover some of the horizontal mask features. The result was a wafer with columns of chips, each column completely separated from its neighbours. It was not excessively fragile, and so the microchip design was considered feasible.

Figure 4.4: Render of the top chip, with a metal spacer. Note how the spacer covers the majority of the chip; this is simpler to produce than a spacer covering only the edges.

Two different spacer options were pursued simultaneously. The first option, a Ti spacer as shown in figure 4.4, is equivalent to the Ti spacer used for the first generation cell. The fabrication process was slightly different however, such that no photolithography would be required after wet etched was completed (as this was found to cause issues previously). Ti was chosen rather than the more expensive Au because the spacer is not required to survive KOH etching. Refer to section 5.3.1 on page 79 for the fabrication details. The second spacer option is quite different, as the spacer is not deposited; it also involves the least processing after wet etching is completed, when the wafers are at their most fragile. Rather than depositing a spacer, the area of the top chip which is *not* part of the spacer is etched with RIE at the very beginning of fabrication. Section 5.3.2 on page 81 explains the process details. With this method, the total thickness of the nanofluidic cell will stay the same, regardless of the spacer height. The Si wafers are 300 µm thick, and so reduction

by a few μm or less will not weaken the chip appreciably. To ensure that this method was workable, a blank Si wafer was patterned and etched 1 μm with RIE, and then inspected with the VLM embedded in the mask aligner (used for photolithography). The etched features were confirmed to be visible and sufficient for aligning to the photomasks.

As in previous designs, the windows are long rectangles, and the top and bottom windows are perpendicular to each other. The top window is 250 μm long and either 10 μm or 25 μm wide; the bottom window is 1200 μm wide, and either 10 μm or 25 μm long. Narrower windows will deform less, but also offer a smaller viewing area. On the bottom chip, there is only a small amount of material on either side of the window before the surface slopes down to form the inlet and outlet steps; this area can be seen clearly in the centre of figure 4.5 on page 64, and the inlet step is labelled in figure 4.2 on page 60. The small section of material on either side of the window will be referred to hereafter as the "window step." For chips with a 10 μm long window, the window step was chosen to be 10 μm per side. For chips with a 25 μm long window, there are three options for window step size: 25 μm, 50 μm, or 100 μm per side. Based on the results of the flow simulations, smaller window step size should result in lower interior pressure. However, a smaller window step also means less material supporting the window, which may make the chip more fragile. Chips with different window step sizes will be fabricated and tested.

In figure 4.5 on page 64, it can be clearly seen that the outlet step extends to the end of the cell, rather than opening to an outlet on the exterior face of the chip. If there was an outlet opening on the bottom of the cell, it would not be possible to seal the cell with a mat. The continuous flat surface of the bottom chip after the window enables the holes in the holder and mat to be larger than the etched window feature, and still maintain sufficient contact area between the mat and bottom chip.

Prior to designing the masks for photolithography, the {111} etch rate of Si in KOH

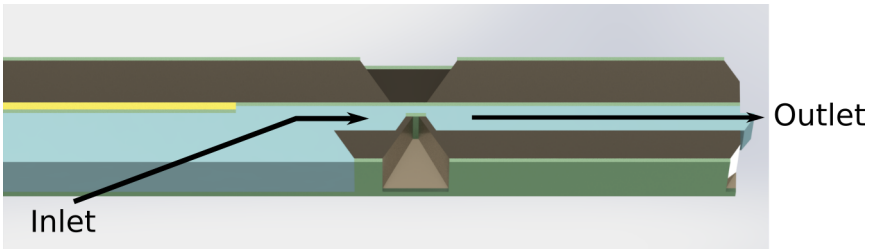

Figure 4.5: Depiction of the cell in cross-section; only part of the cell is shown. An approximate flow path is indicated with arrows. Note that the height of the spacer shown here (yellow) is greatly exaggerated.

was determined by comparing measured feature sizes (the length and width of windows) to the sizes calculated using an etch rate from literature. Ten windows from each of two wafers were measured with a VLM, and equation (2.2) was used to calculate the actual {111} etch rate. This value was then used to determine appropriate mask feature sizes for the second generation design, as done previously (section 2.2.1 on page 31). The final photomask designs are shown in appendix B, section B.2 on page 141; as before, masks were manufactured by the University of Alberta nanoFAB.

4.3 Putting it all together

Once the photomasks were completed, the designs for the holder tip and lid were finalized and checked by HTC for compatibility (figure 4.6 on page 65). HTC then manufactured a prototype of the fluidic holder: the tip and lid were made from stainless steel, and the remaining part of the holder (standard for Hitachi TEMs, designed by HTC) was made from phosphor bronze. The screws are Ti. Photographs of the finished piece are shown in figure 4.7 on page 66.

Bench top flow tests were done in a cell with windows nominally 25 μm wide, with an

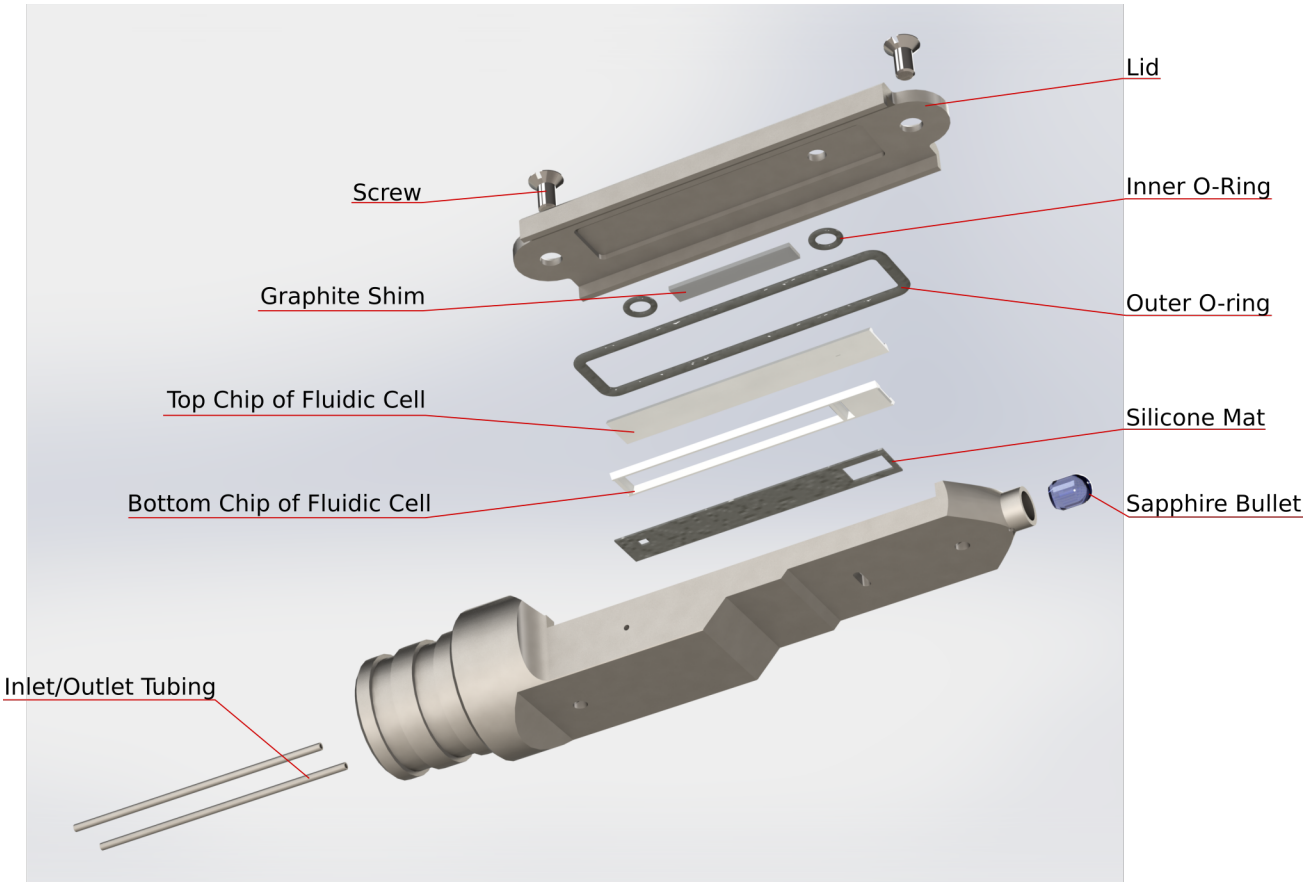

Figure 4.6: Depiction of the components in the tip assembly. The sapphire bullet is the contact point between the sample holder and a point inside the sample chamber; it is glued in place. The silicone mat (for sealing around the cell) has openings for the inlet flow, and around the window and outlet sections of the cell. The graphite shim and inner O-rings rest on top of the cell and distribute the pressure from the lid; the graphite may be omitted. The ridges on the sides of the lid extend partway down the sides of the tip. The stepped thickness of the tip ensures that the front section is narrow enough to avoid contact with the pole pieces, while providing additional strength for the rear section. The inlet and outlet tubing, shown here as short pieces, would be soldered inside the end of the tip and extend throughout the length of the sample holder.

Figure 4.7: The holder prototype manufactured by HTC, shown with and without the lid. Note that before use in a TEM, a sapphire bullet would be added, and the screws would be countersunk (i.e. not protruding). The small circular feature visible in the left and right photos is level with the end of the inlet channel.

actual width of 12 µm. The silicone mat used for sealing was made in-house from a sheet of silicone rubber. After flowing DI water through at a rate of 0.1 mL/min for several hours, no visible leaks were observed. In another test, Rhodamine B (a fluorescent dye) in ethanol was flowed through the cell while the absorbance was measured. The absorbance results showed that the Rhodamine entered the cell, which confirms flow past the window. The integrity of the NFS will be definitively tested in a vacuum test station provided by HTC, followed by experiments in a TEM.

For pump-probe experiments, it is useful to calculate the refresh rate, i.e. the rate at which the solution in the observed volume is completely replaced. A flow rate of 0.1 mL/min past a 12 µm window in a channel 0.71 µm tall by 1500 µm wide gives a refresh rate of approximately 130 kHz. This is fast enough to be useful for time-resolved experiments, which are typically run at repetition rates below 10 kHz in our lab. For TEM imaging, the flow rate could be reduced significantly, as flow is mainly used to transport the sample to the viewing area or to refresh the solution surrounding a stationary sample; flow must be stopped during image acquisition to avoid blur.

Chapter 5

Fabrication of the nanofluidic cells

All fabrication of fluidic cells was performed in the University of Waterloo's Quantum NanoFab, with the exception of the KOH wet etching, which was performed in the UeIL. The Si wafers used for every fabrication process (unless otherwise specified) were 300 μm thick {100} Si, lightly p-doped (with B) to a resistivity of $1 - 10\ \Omega$cm, 4" in diameter, and polished on both sides. The fabrication techniques used will be briefly described in the following sections; for detailed methods, refer to appendix A on page 102.

5.1 Fabrication techniques

5.1.1 Deposition of silicon nitride and metal films

The Si_3N_4 window membranes were deposited onto wafers via LPCVD, using NH_3 and $SiCl_2H_2$ as the feed (i.e. reactant) gases; refer to reaction (5.1). [45]

$$3\,SiCl_2H_2 + 4\,NH_3 \longrightarrow Si_3N_4 + 6\,HCl + 6\,H_2 \tag{5.1}$$

As with all types of CVD, vapour-phase reactants flow over a hot surface to form a solid film. While this process involves various transport and reaction mechanisms, the two possible rate-limiting steps are reactions in the gas phase (often the formation of undesirable byproducts), or reactions of adatoms on the solid surface (the formation of the desired film). Operating at a low pressure (in this case around $25 - 50$ Pa) increases the diffusivity of the reactant gases, thus increasing the rate at which reactants are transported to the wafer surfaces. [45] Faster mass transport of gases to the surface reduces the opportunity for gas phase reactions to occur, and solid phase reactions become the rate limiting step. Compared to other types of CVD, LPCVD has excellent uniformity, purity, and conformal step coverage (i.e. the film thickness is consistent, even inside small features); large batches of wafers can be treated simultaneously without reducing deposition quality. However, high temperatures (above 500 °C) are required, the inside of the horizontal reactor tube is also coated in the deposited material, and the deposition rate is low. [45]

Deposition of metal films (used as the spacer in most of the processes) was done using EBE. This technique involves placing the wafer (masked with either negative photoresist or a physical mask; refer to sections 5.1.3 and 5.3.1) onto a rotating sample stage in a vacuum chamber, along with a crucible containing a pure target of the metal to be deposited. A high energy electron beam (in this case $6 - 10$ kV) strikes the metal target, causing local melting and evaporation of the metal. The evaporated metal atoms travel throughout the chamber, adsorbing onto the relatively cool surfaces they come into contact with. [45] This deposition is not limited to the sample; the metal atoms travel outwards from the crucible in all directions, forming a thin film on all surfaces in their path. EBE is a type of thermal evaporation, and is a physical process (rather than chemical).

5.1.2 Cleaning and etching

Wafers were cleaned before use by immersion in a Piranha solution (sometimes referred to as sulphuric acid:peroxide mixture (SPM)), which consisted of four parts 18 mol/L H_2SO_4 to one part 30 % H_2O_2. Addition of the H_2O_2 causes the mixture to self-heat to boiling. The Piranha cleaning process removes organic contaminants from the wafer via the formation of Caro's acid (H_2SO_5, as shown in reaction (5.2)), a strong oxidizing agent of organic compounds. [46]

$$H_2SO_4 + H_2O_2 \longrightarrow H_2SO_5 + H_2O \tag{5.2}$$

RIE was used for dry etching of Si_3N_4 in preparation for bulk Si etching, and for creating the spacer described in section 5.3.2 on page 81. In RIE the surface to be etched (a single Si wafer) is bombarded with a plasma generated from the feed gases; in this case, SF_6 was used as the feed gas, and the resulting plasma contained electrons, photons, $F^\bullet$ radicals, SF_5^+ cations, F^- anions, and neutral SF_6. [47] Etching occurs through both physical and chemical mechanisms: ion bombardment physically dislodges surface atoms, creating dangling bonds and dislocations. This process is not very chemically selective (i.e. will etch different materials at similar rates), but does introduce anisotropy as the ion beam damage "activates" the surface; activation can also be induced by electron and photon impact. Chemical etching occurs preferentially on the activated surface, and introduces holes and volatile species. Chemical selectivity is based on the choice of feed gas: O_2 removes photoresists, while SF_6 etches Si and Si_3N_4. [45, 48] This selectivity decreases with increasing temperature. [47]

Bulk etching of Si was done via wet etching with KOH, as per reaction (5.3). [46, 49] The Si etching rate does not simply increase with increasing KOH concentration; because OH^- and H_2O are both involved in the reaction, excessively high KOH concentrations

result in insufficient water and the reaction rate slows. The maximum etching rate occurs at 22 wt% KOH in water. It is important to note this etching is highly anisotropic; the relative etch rates of {100}, {110}, and {111} Si are 200, 400, and 1, respectively. [46] As a result, etching progresses along the {111} planes, giving etched features with walls sloping inwards at an angle of 54.74° downwards from the wafer surface. [46, 50] The geometry is illustrated in figure 2.6 on page 33.

$$\mathrm{Si_{(s)}} + 2\,\mathrm{OH^-_{(aq)}} + 2\,\mathrm{H_2O_{(l)}} \longrightarrow \mathrm{Si(OH)_2O^{2-}_{2(aq)}} + \mathrm{H_{2(g)}} \tag{5.3}$$

Si_3N_4 masked the areas which were not etched; the etch rate of {100} Si in KOH is on the order of a few μm/min, whereas Si_3N_4 has a negligible etch rate in KOH. [47, 50]

5.1.3 Photolithography

In this work, photolithography was the primary patterning technique used. Photoresist, consisting of photosensitive polymers and resin in an organic solvent, is spin-coated onto the Si wafer to make a uniform layer. Note that the final height of the photoresist layer is quite consistent between wafers, as it depends on the resist properties (viscosity and solute concentration) and the spinning speed, but not on the spin duration (past an initial period) or the wafer size. [51] The resist-coated wafer is then exposed to near-UV light through a photomask, made of glass with a thin layer of metal on one side to block transmission of light in the desired areas. Exposure to the near-UV light initiates physico-chemical reactions in the resist, changing the solubility of the exposed areas in some way; the result is that some areas (either only the exposed or only the unexposed areas) are soluble in the developer solution. For positive-tone photoresists the exposed areas are soluble in developer, while for negative-tone photoresists the unexposed areas are soluble. [45, 48]

The wafer is developed by immersing it in the appropriate developer (an alkaline solution, specific to the photoresist being used) and agitating gently, followed by a soak in DI water. The result is a wafer with a polymer reproduction of the mask pattern, with precision on the order of a few micron or better.

The negative-tone photoresist used in this work, maN-1410, is based on bisazide compounds and novolac resin. [52] Commonly used in many kinds of photoresist, novolac resin consists of linear cresol-formaldehyde condensation polymers of varying lengths. [53] Exposure of bisazide/novolac resist to near-UV light (365 nm, the i-line of a Hg lamp) causes the azide groups to break down into nitrene radicals and molecular nitrogen; the nitrene radicals can then attack the hydroxyl groups and the sp^3 carbons of the resin, producing iminoradicals (i.e. a nitrene radical with a proton) and leaving the oxygen and carbon of the resin as radicals. This reaction can repeat with new polymer units, converting the iminoradicals to primary amines. The iminoradicals can also form covalent bonds with the carbon radicals and phenoxyradicals, producing polymeric secondary amines. Radicals in the polymer units can also react with other parts of the polymer, forming cross-links. [52,53] The overall result of this process is that the exposed areas become less soluble in the developer, due to the additional covalent bonds, while the unexposed areas remain soluble. [45,48]

While there are a variety of different positive-tone photoresists with distinct chemical mechanisms, only diazonaphthoquinone (DNQ) based resists will be discussed here. Of the two positive photoresists used in this work, one consists of DNQ sulphonic esters in novolac resin (AZ P4620), and the other (S1811) could not be identified beyond "diazo compounds in novolac resin." [54, 55] When exposed to near-UV light (405 nm, the h-line of a Hg lamp), DNQ sulphonic esters undergo photolysis. The subsequent products are hydrophilic and ionizable, whereas DNQ is relatively hydrophobic. [53] As a result,

the exposed areas of the photoresist become much more soluble in the alkaline developer solution than the unexposed areas. [45, 48, 53]

5.2 Fabrication of the first generation chips

5.2.1 Titanium spacer

A schematic of the fabrication procedure is given in figure 5.1 on page 73. The wafers for the top and bottom microchips were processed in parallel until the first wet etching step. Blank Si wafers were cleaned with Piranha solution and thoroughly rinsed with DI water, first by immersion in a water bath, and then with automated spin-rinse-dry equipment. Within an hour of cleaning, a film of Si_3N_4 was deposited onto the wafers via LPCVD. The target film thickness was either 20 nm or 50 nm; both were used, depending on the type of testing planned. Deposition of Si_3N_4 was typically done with large batches of wafers (usually 10-20) for convenience, while subsequent stages of the fabrication process were typically done in batches of one to three wafers each for the top and bottom chips. Positive photolithography was used to pattern the wafers prior to etching. All wafers to be patterned were heated in a N_2 atmosphere to remove adsorbed water, and each wafer was removed from the oven immediately before depositing photoresist. AZ P4620 positive resist was applied to individual wafers by spin coating, followed immediately by a short soft baking step on a hotplate. Both sides of each wafer were coated with resist before being allowed to cure for a few hours. Once cured, one side of each wafer was exposed to near-UV light through the appropriate photomask; the mask used for the top wafers includes a window for each chip, while the mask used for the bottom wafers includes inlet and outlet features in addition to windows. Each wafer was individually processed in

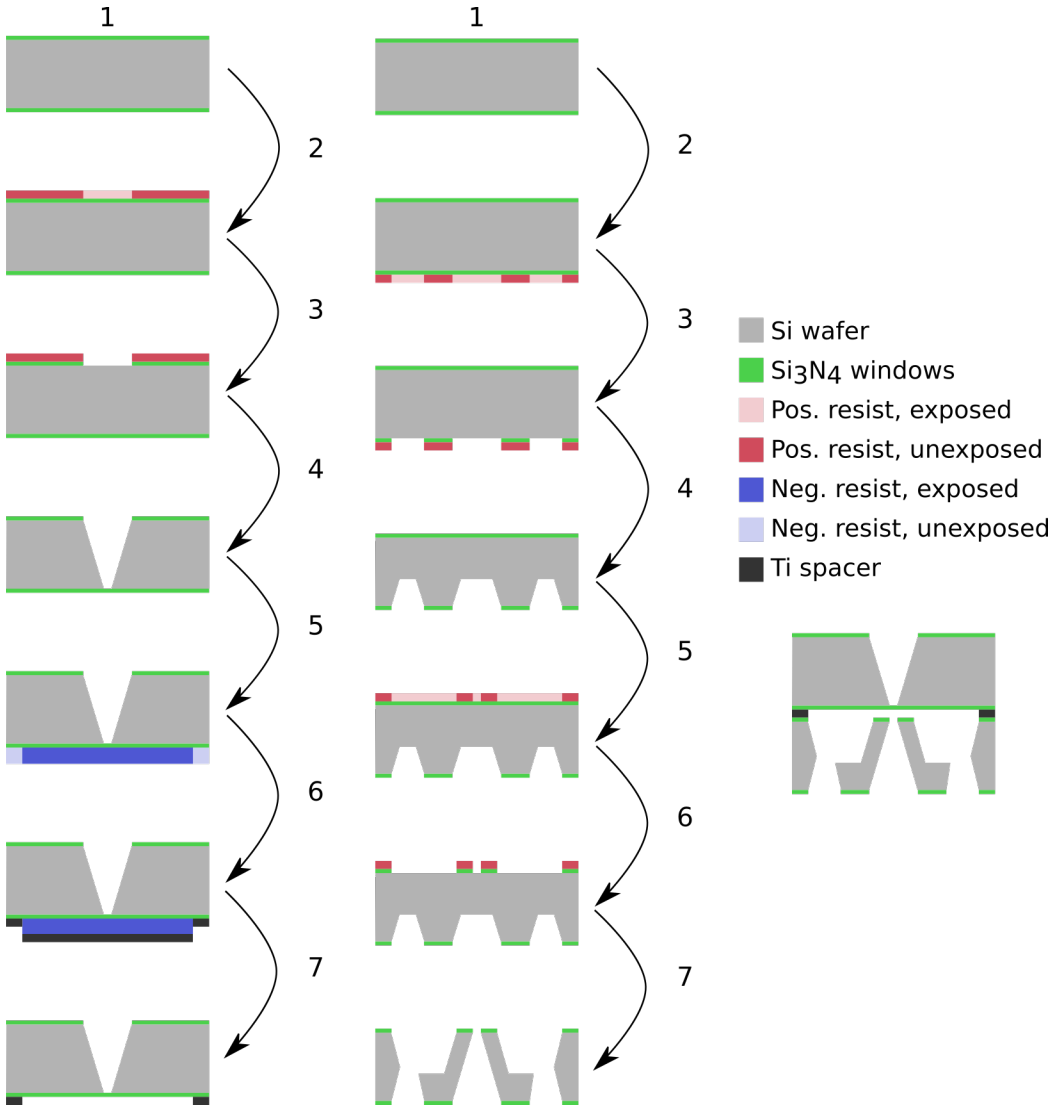

Figure 5.1: Procedure for first generation chips with Ti spacer; top chip is shown on the left, bottom chip is shown on the right. 1) Start from Si wafer with layer of Si_3N_4. 2) Apply positive photoresist, expose. 3) Develop resist, and etch Si_3N_4 via RIE. 4) Remove resist, etch Si with KOH (to completion for tops, only halfway for bottoms). Top: 5) Apply negative photoresist, expose. 6) Develop resist, deposit Ti via EBE. 7) Remove resist. Bottom: 5) Apply positive photoresist, expose. 6) Develop resist, and etch Si_3N_4 via RIE. 7) Remove resist, etch Si with KOH (to completion).

photoresist developer solution. After rinsing thoroughly with DI water and drying with N_2, the patterned wafers were ready for etching, with a photoresist layer approximately 10 µm thick masking the areas between features. The first etching stage was RIE of the unmasked Si_3N_4 to expose the Si beneath it. After RIE, the remaining resist was dissolved in photoresist remover solution, and the wafers were rinsed with IPA and DI water.

At this point, the procedures for the top and bottom wafers diverged. Both sets of wafers underwent KOH etching, but the bottom wafers were etched only about halfway through the wafer thickness, while the top wafers were etched to completion. After KOH etching, the wafers were rinsed thoroughly with DI water and dried with N_2.

The bottom wafers were patterned again, following the same procedure as before: drying to remove water, spin coating AZ P4620 positive photoresist, exposure (this time using a photomask with groove features, to form channels for the inlets and outlets), development, reactive ion etching of Si_3N_4, removal of resist, and finally KOH etching, this time until completion. The top wafers instead underwent a lift-off process to create the spacers: after KOH etching, the top wafers were dried in a N_2 atmosphere, and then each wafer was individually spin coated with a layer of maN-1410 negative photoresist on the intact side. Each wafer was baked on a hotplate immediately after spin coating. As with the positive photolithography, each wafer was exposed and developed, rinsed with DI water, and dried with N_2, leaving a layer of resist about 1.3 µm thick. The spacer, a layer of Ti with a target thickness of $0.5 - 1$ µm, was then deposited via EBE. The photoresist was removed, along with the excess Ti. At this stage the top and bottom wafers were ready to be separated into individual chips.

Initially, chips were separated with an automatic dicing saw. A wafer, along with a metal frame, was attached to an adhesive film for support; the dicing saw was then used to cut the wafer into individual chips. With the film still holding all pieces of the

wafer together, the chips were cleaned with DI water and dried. The film was then cured under UV light, causing it to lose its adhesion and allowing the individual chips to be removed. Using the dicing saw for separation without any protective measures was not feasible. During operation of the saw, a jet of water is pumped onto the blade to prevent overheating; the force of the water is enough to break the windows in the chips. As an alternative to the dicing saw, a set of Teflon supports were machined by Ariel Petruk to enable wafers to be separated by hand. The first of the two supports, as shown in figure 5.2 on page 76, is for breaking sections of wafer into individual columns of chips. The support features a series of troughs with the same spacing as the rows of windows, and a ridge to hold the wafer section against to ensure proper positioning. A glass slide is used to hold the wafer section flat against the support, as a second glass slide is used to press down on the column extending over the edge, breaking it off. The troughs ensure that the windows do not come into contact with anything as the wafer piece is slid from side to side. The second support is used to separate columns of chips; see figure 5.3 on page 76. Similarly to the first support, there is a trough and a ridge to isolate the chip windows. Operation is also equivalent, with a glass slide used to hold the column of chips in place while tweezers or a second glass slide are used to break off each chip. Separating chips by hand is time-consuming and has a non-trivial failure rate, requiring each chip to be inspected to check if its window is intact. In addition, the Teflon supports tend to accumulate static, causing wafer fragments and dust to adhere.

5.2.2 Gold spacer

The fabrication procedure for the first generation chips with a Au spacer is very similar to the procedure used for the chips with a Ti spacer: the only significant change (aside from

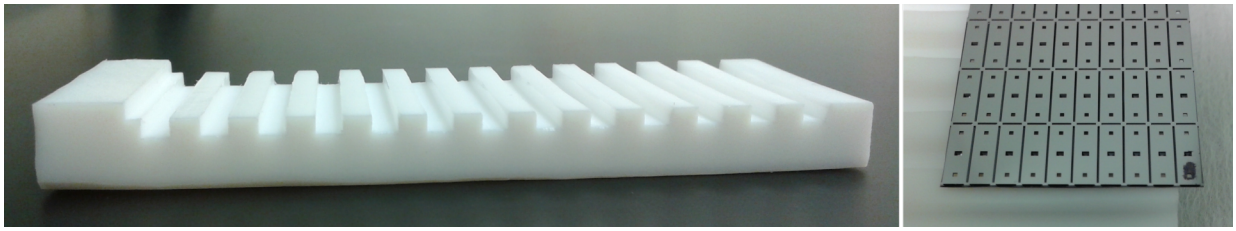

Figure 5.2: First Teflon support made by Ariel Petruk, used to separate wafer sections into individual columns of chips. (**Left**) The support; note the troughs, and the ridge on the left had end. (**Right**) Support in use. A section of wafer was placed onto the support, with the top edge pressed against the ridge. The wafer piece was aligned such that a single column of chips was overhanging the edge, and a glass slide was used to hold the piece in place. A second glass slide was placed on top of the overhanging column and pressed down sharply, causing the column of chips to break off.

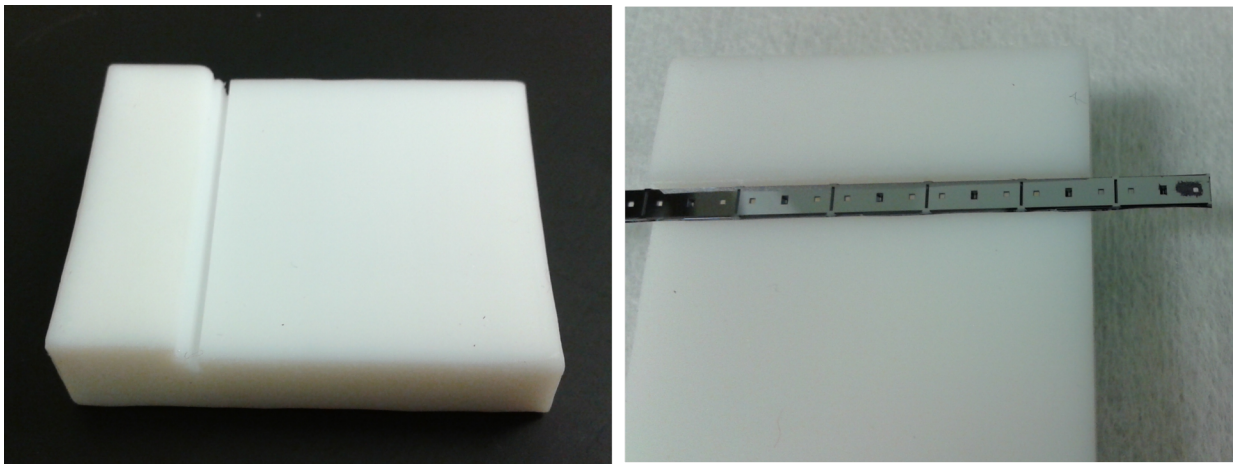

Figure 5.3: Second Teflon support made by Ariel Petruk, used to separate columns of chips into individual chips. (**Left**) The support, with trough to isolate windows. (**Right**) Support in use. The column of chips, held in place against the ridge, was aligned such that one chip was overhanging the edge. A glass slide was used to hold the column in place while tweezers were used to press down sharply on the overhanging chip, breaking it off.

the difference in spacer material) is that the spacer is deposited before wet etching rather than afterwards. See figure 5.4 on page 78 for a schematic of the process. Note that the method for fabrication of the bottom wafers was not changed.

As before, fresh Si wafers were cleaned with Piranha solution, and a layer of either 20 nm or 50 nm thick Si_3N_4 was deposited via LPCVD. Wafers were patterned with positive photolithography, using AZ P4620 resist and exposing through the same set of photomasks used previously. RIE was used to etch Si_3N_4 in the patterned features. In preparation for depositing the spacer, the top wafers were patterned with negative photolithography, using maN-1410 resist and the appropriate photomask. EBE was then used to deposit a layer of Au, with thickness $0.5 - 1$ μm. The excess Au was removed along with the photoresist. Both sets of wafers were etched together in KOH; the bottom wafers were removed after approximately 1.5 hours, while the top wafers were etched until completion (3 hours). The bottom wafers underwent a second round of patterning with positive photolithography, RIE, and KOH etching, as described previously. Once all wafers were complete, they were separated into individual chips by hand as described in figure 5.2 on page 76 and in figure 5.3 on page 76.

5.3 Fabrication of the second generation chips

Two different methods were considered for the spacer: method 1 involves depositing a metal spacer onto the top wafer at the end of fabrication, while method 2 involves etching the spacer directly into the top chip wafer at the very beginning of fabrication. In both cases, the process for the bottom wafer is the same, and is very similar to the method used for the first generation chips; see figure 5.5 on page 80. The procedure for the bottom chips is as follows: blank Si wafers were cleaned by immersion in Piranha solution and

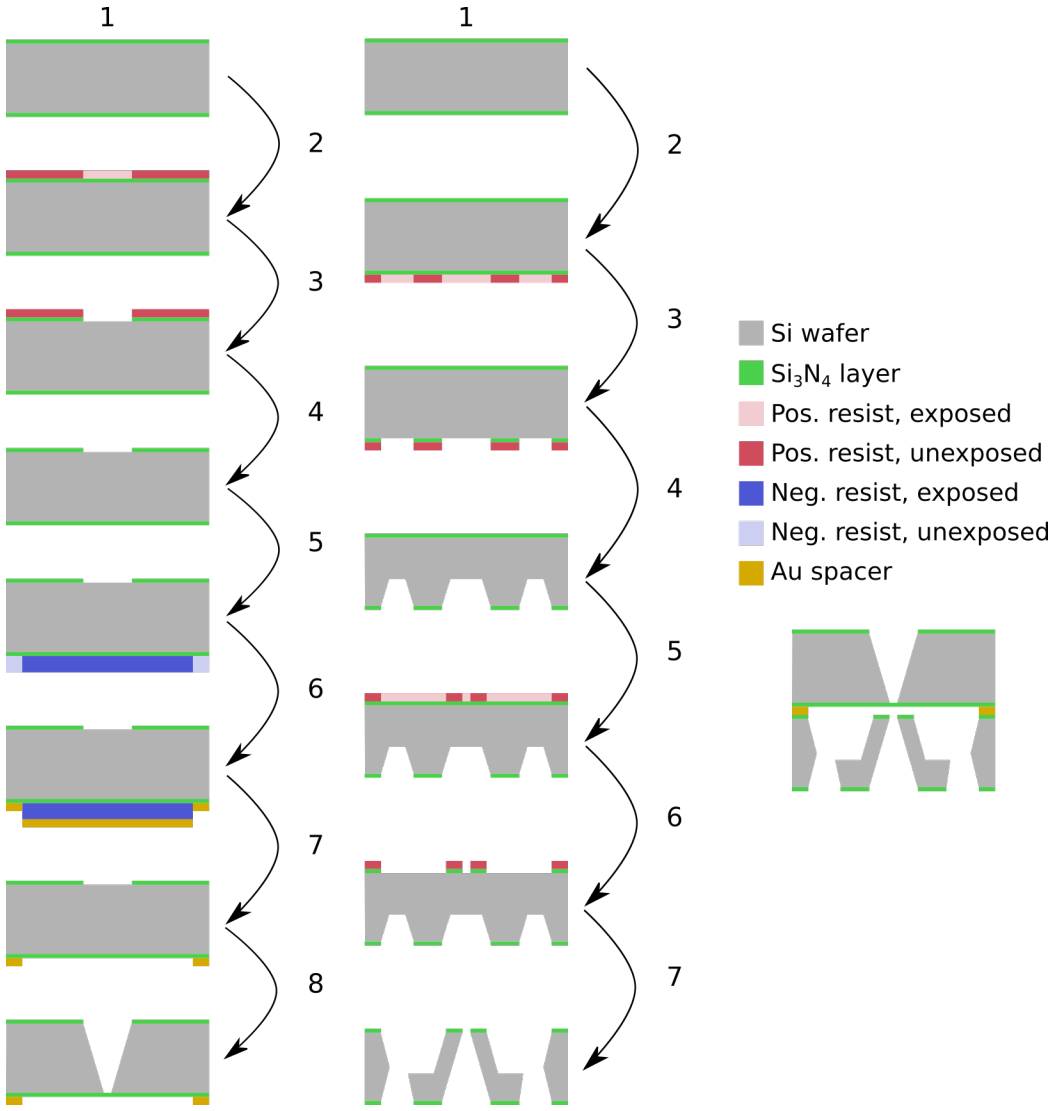

Figure 5.4: Procedure for first generation chips with Au spacer; top chip is shown on the left, bottom chip is shown on the right. 1) Start from Si wafer with layer of Si_3N_4. 2) Apply positive photoresist, expose. 3) Develop resist, and etch Si_3N_4 via RIE. Top: 4) Remove resist. 5) Apply negative photoresist, expose. 6) Develop resist, deposit Au via EBE. 7) Remove resist. 8) Etch Si with KOH to completion. Bottom: 4) Remove resist, etch Si with KOH (approximately half of the thickness). 5) Apply positive photoresist, expose. 6) Develop resist, and etch Si_3N_4 via RIE. 7) Remove resist, etch Si with KOH to completion.

thoroughly rinsed with DI water; a film of Si_3N_4 with target thickness 20 nm or 50 nm was then deposited using LPCVD. After Si_3N_4 deposition, the inlet, outlet, and window features were patterned onto the wafers with positive photolithography. Wafers were dried in a N_2 atmosphere until immediately before a layer of Shipley S1811 positive photoresist was applied to both sides of each wafer via spin coating, follow by a short soft baking step. Unlike the AZ P4620 resist used previously, no curing time was required between spin coating and exposure for the S1811 resist. Wafers were exposed to near-UV light through the appropriate mask and developed. The exposed Si_3N_4 was etched with RIE, and the photoresist was removed with remover solution, IPA, and DI water. Wafers were wet etched in KOH approximately two thirds of the way through (about 110 minutes), rinsed thoroughly with DI water, and dried with N_2. To form the flow channel, the process was repeated from photolithography, to RIE, and finally to wet etching, this time to completion.

5.3.1 Method 1 - titanium spacer

While the finished Ti spacer on this type of second generation chip is equivalent to that of the first generation style, the fabrication process for the spacer is slightly different. Instead of using a negative photolithography lift-off method, a separate physical mask was used. This allows for the spacer to be deposited after wet etching, while still minimizing the amount of handling of the (now delicate) etched wafers. Refer to figure 5.6 on page 82.

Initially, the mask for spacer deposition was to be made from a clean {100} Si wafer, 500 µm thick. The wafer would be patterned with photolithography using AZ P4620 positive photoresist, as previously described in other processes. After exposure and development, RIE would be performed to etch almost entirely through the wafer thickness; at

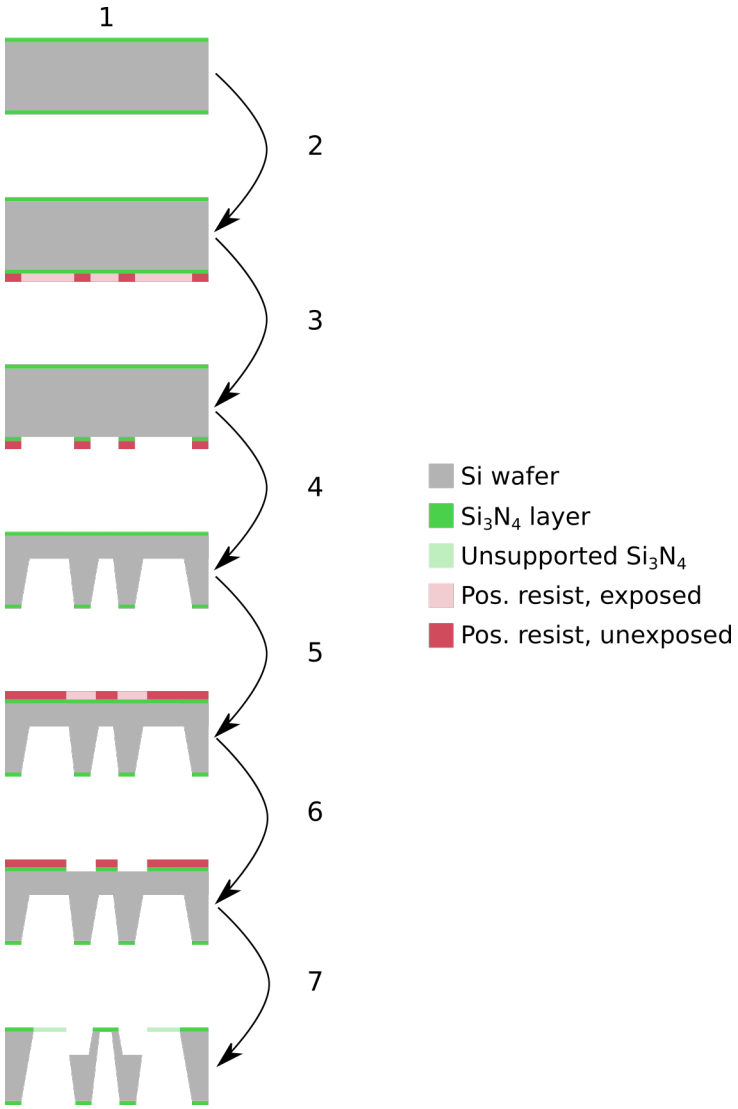

Figure 5.5: Procedure for second generation bottom chips. 1) Start from Si wafer with layer of Si_3N_4. 2) Apply positive photoresist, expose. 3) Develop resist, and etch Si_3N_4 via RIE. 4) Remove resist, etch Si with KOH (approximately 2/3 of the thickness). 5) Apply positive photoresist, expose. 6) Develop resist, and etch Si_3N_4 via RIE. 7) Remove resist, etch Si with KOH (to completion). Note that the unsupported sections of the Si_3N_4 should break away during handling.

approximately $20 - 50$ μm from completion, etching would be stopped. A swab soaked in acetone would be used to carefully remove the photoresist from the "teeth" of the mask (refer to figure B.9 on page 146), after which RIE would continue to completion. The purpose of this step was to create a step in the mask, such that the portion corresponding to the delicate Si_3N_4 windows would not come into direct contact. When the resist was removed, and the mask wafer would be complete. Unfortunately, this process was unsuccessful, and the wafer broke during each attempt. Instead, a metal mask with the same features was machined by Ariel Petruk.

Similarly to the first generation chips with Ti spacer, blank Si wafers were cleaned in Piranha solution and thoroughly rinsed with DI water prior to LPCVD of 20 nm or 50 nm thick Si_3N_4. The window features were patterned via positive photolithography, using S1811 resist and exposing to near-UV light. After photoresist development, the exposed Si_3N_4 was etched with RIE, and the remaining resist was removed. Wet etching in KOH was performed to etch the windows. Each wafer was secured to a physical mask, such that the areas requiring a spacer were exposed. The wafers and masks were loaded into the electron beam evaporator in batches of four, and a layer of Ti was deposited to the desired thickness (much less than the thickness of the mask). With this method, no excess Ti was deposited onto the wafer itself, and "lift-off" consisted of simply removing the wafer from its mask. Once the spacer deposition was completed, the wafers were ready to be separated into individual chips.

5.3.2 Method 2 - spacer etched into wafer

The fabrication process for the second generation chips with a spacer etched directly into the wafer is notably different from the other procedures used, with patterning and etching

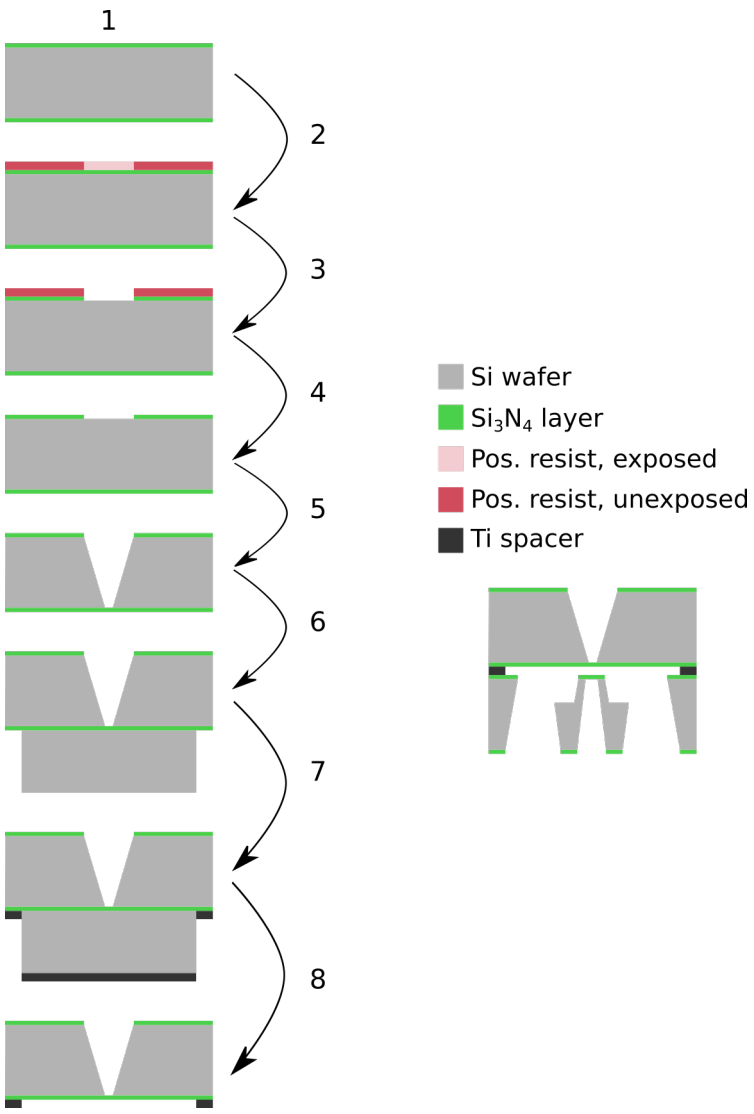

Figure 5.6: Procedure for second generation top chips, with Ti spacer. 1) Start from Si wafer with layer of Si_3N_4. 2) Apply positive photoresist, expose. 3) Develop resist, and etch Si_3N_4 via RIE. 4) Remove resist. 5) etch Si with KOH to completion. 6) Secure wafer and mask together on sample stage of electron beam evaporator. 7) Deposit Ti. 8) Separate mask and wafer.

steps occurring *before* Si_3N_4 deposition. See figure 5.7 on page 84 for a schematic of the procedure. Fresh Si wafers were cleaned thoroughly with DI water and IPA and dried under N_2 atmosphere. AZ P4620 positive photoresist was deposited via spin coating, followed by a short soft bake. After allowing the resist to cure in ambient conditions for a few hours, the wafers were exposed to near-UV light through the "spacer" photomask, and then developed. RIE was used to etch the exposed Si, similarly to the other fabrication procedures; however, the etching time was significantly longer, and the Si was etched to a depth of $0.5 - 1$ μm. At this point, the remaining photoresist was removed, and the process continued as was typical: Piranha cleaning, LPCVD of Si_3N_4, and positive photolithography (this time with S1811 resist) to pattern the window features. The exposed Si_3N_4 was dry etched with RIE, and the photoresist was removed as usual prior to KOH wet etching. The wafers were etched to completion and separated into individual chips.

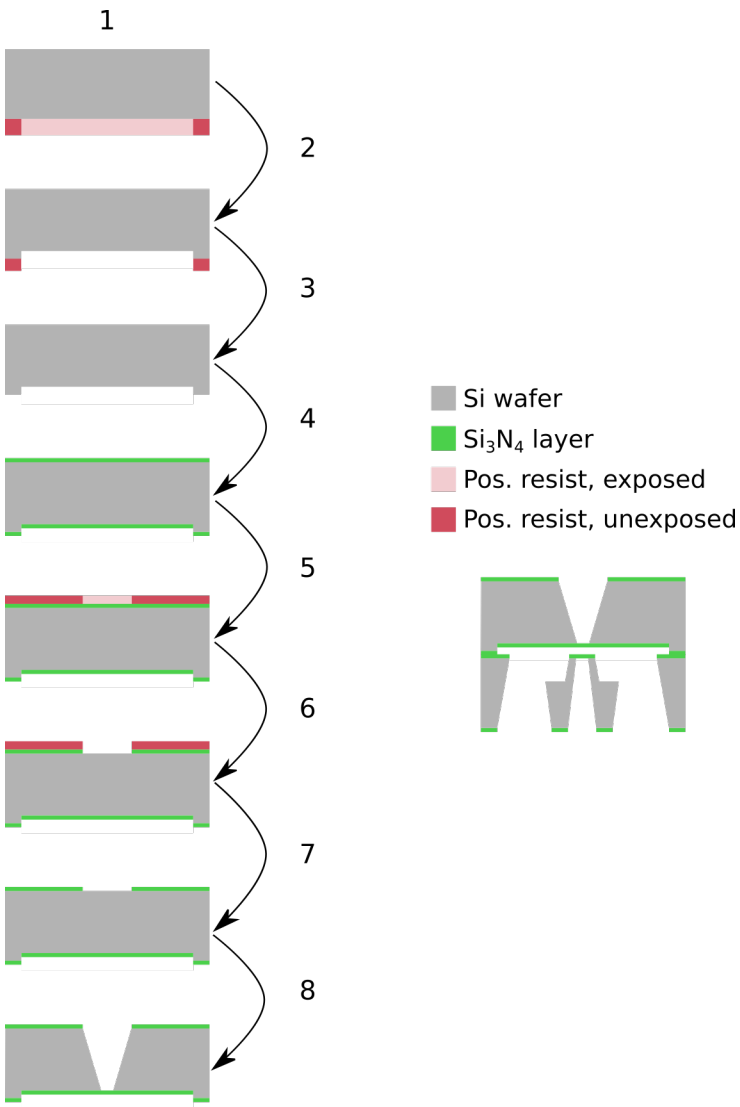

Figure 5.7: Procedure for second generation top chips with spacer etched directly into the chip. 1) Start with bare Si wafer; apply positive photoresist and expose. 2) Develop resist and etch Si to desired depth using RIE. 3) Remove resist, do Piranha clean. 4) LPCVD of Si_3N_4. 5) Apply positive photoresist, expose. 6) Develop resist, and etch Si_3N_4 via RIE. 7) Remove resist. 8) Etch Si with KOH, to completion.

Chapter 6

Summary and future work

In summary, this project has met the challenge of developing a NFS with true, controlled flow. While commercial NFSs already exist, they lack the full control over the flow path which was achieved here. The first generation of our NFS was developed through literature review and reverse engineering of a basic sample holder; after testing, fluid dynamics simulations, and consultations with HTC, the second generation of the design was produced. Our finalized design features a novel asymmetric nanofluidic cell, with a large inlet open to the holder. The cell can withstand high flow rates without bulging apart, breaking, or leaking, and has windows thinner than any other flow cell currently existing (20 nm, as opposed to the 50 nm standard). With a total thickness under 2.0 mm at the tip (including holder, cell, and lid), our system meets the current commercial standards for TEM and STEM sample holders. Bench-top experiments with a prototype holder are already in progress, and arrangements are being made with HTC to run tests in a vacuum test station and, finally, in a TEM. We expect to commercialize our NFS in the near future.

The second generation NFS is ready for use, but more optimization is always possible.

While experiments are being carried out with the prototype holder, design improvements and additional features can be investigated. Implementing some of the recommendations and features discussed below prior to commercialization would lead to a stronger, more competitive product.

Perhaps the simplest way to improve performance of the NFS is to adjust the window thickness: the current set of photomasks and holder will still be appropriate, and window thickness directly impacts achievable resolution. Up to this point, our chips have been fabricated with either 20 nm or 50 nm thick Si_3N_4 windows. When 10 nm thick Si_3N_4 was tested, it did not survive KOH etching; however, Zheng *et al.* reported success with 10 nm thick Si-rich Si_xN_y windows for a stationary sandwich cell. [38] In two other papers from the same group (albeit with 20 nm and 25 nm thick windows, respectively) their wet etching conditions were stated as 33 wt% KOH at 80 °C; for comparison, this work used 25 wt% KOH at 90 °C. [32, 34] While this is a more concentrated solution than was used in this work, it should actually etch more slowly (as per [46], which found the maximum Si etch rate to occur at a concentration of 22 wt% KOH in water). A deposition of 10 nm Si_3N_4 should be tested under different KOH etching conditions, to determine whether the success of Zheng *et al.* was due to gentler etching conditions or the use of Si-rich Si_xN_y.

In contrast, all of the designs reviewed which had flow (including both pseudo-flow and true flow) had 50 nm thick Si_3N_4 windows; even if 20 nm is found to be the limit for windows with our fabrication process, it will still be an improvement over existing designs. [15, 28, 56–58]

Furthermore, adding a second inlet channel to the holder would increase the range of possible applications for the NFS, and in principle would not require any modification to the nanofluidic cell itself. Another flow channel would need to be drilled in the holder tip, and another steel tube welded in place. The handle of the holder would need to be redesigned;

however, because the handle is outside of the EM, there are far fewer restrictions on its design. Dual inlets would allow reagents to be mixed as they enter the cell, where their reaction could be observed in real-time. Studies of liquid-phase reactions would not be restricted to those triggered by external factors (primarily electron beam irradiation, but also temperature conditions and electrical stimuli), but could also include reactions which begin immediately upon mixing. From a commercial standpoint, this would allow our NFS to compete with existing systems, such as Hummingbird Scientific's dual flow cell. [27, 28] Experiments requiring a single inlet could still be performed with a dual flow holder, by simply flowing the same solution through both inlets.

The placement of the flow channels in the holder tip was made under the assumption that the tip should be 2.0 mm thick for its entire length. However, the conical shape of the polepieces allows for a stepped thickness, as seen in figures 4.7 and 4.6. The flow channels could be extended further towards the end of the tip, taking advantage of the extra material and allowing the fluidic cell (and associated tip features) to be shorter. The microchips, particularly the bottom chips, would then be easier to handle without breaking; more chips could also be fabricated per wafer, improving efficiency.

The cell windows themselves can be functionalized for various applications. One important case is the hydrophilicity of the windows: de Jonge *et al.* found that untreated Protochips stationary cells were hydrophobic after their protective photoresist was removed (poly(methyl methacrylate) (PMMA), stripped with acetone and ethanol). [30, 37] A hydrophobic environment is not conducive to the study of aqueous or cellular samples. Plasma cleaning was found to make the chips hydrophilic for about one day, and immersing the cleaned chips in a solution of 0.01 % poly-L-lysine kept them hydrophilic for a longer period (duration not reported). [30, 37] The hydrophilicity of our chips after fabrication should be tested via contact angle measurements, and different methods of controlling the

hydrophilicity should be investigated; for example, we had previously found that the microchips were hydrophilic after Piranha cleaning. The desired window surface properties will depend on the sample being studied.

Going a step further, procedures exist for affinity capturing of biological assemblies on membranes, as done by Dukes *et al.* with Protochips stationary cells. [59] In this case, a multi-stage procedure was used to cause the target biological molecules to bind to the viewing window, preventing diffusion of the sample and improving resolution.

Moreover, electrodes are a powerful addition to a NFS. Applications include electrochemical deposition of materials such as Cu [2, 21], Pb dendrites [60], and $CaCO_3$ [24]; formation of bubbles via resistive heating [2, 31]; increasing the pH of solutions [24, 61]; studies of Li ion battery chemistry [32]; and many voltammetry experiments [2, 32, 43]. All of the electrochemical cells referenced above used Au electrodes; in two cases, a thin Ti layer was added to one or both sides of the Au electrodes (likely to improve adhesion of the Au to the wafer). [24, 25] If the electrodes are to be deposited before KOH etching, Au is the most appropriate choice. It is important to ensure that if electrodes and a metal spacer are both used, they do not come into contact with each other; this can be avoided most easily in our design by using the etched spacer method (i.e. is a part of the Si wafer itself).

Another avenue for possible improvement of the nanofluidic cell is the window material: Si_xN_y is used in all commercial NFSs, and in the vast majority of designs made by other researchers. [11] Several window material options for nanofluidic cells were described in section 1.2.1 on page 8; table 6.1 on page 89 summarizes the properties of various window materials, including both those mentioned previously, and new materials. Additional details for some of the entries in table 6.1 are given below.

Table 6.1: Comparison of possible window materials.

Material	Advantages	Disadvantages
Si_xN_y	Highly compatible with mainstream fabrication techniques, and can be used to mask Si during KOH and TMAH etching. [11,19] The ratio of Si to N can be tuned to influence mechanical properties. [11,16]	Insulating. [62] Minimum thickness of approximately $10-15$ nm for use as a window. [22]
hBN	Can be made as a monolayer. [63] Has good thermal stability and oxidation resistance; is highly transparent in the visible and near-infrared (IR) range. [64]	Highly insulating. [64] Not compatible with mainstream fabrication techniques. [11]
Graphene	Has been successfully used as a monolayer window. [17] Conductive, highly electron transparent. [62]	Not compatible with mainstream fabrication techniques. [11]
SiO_2	Reasonably compatible with mainstream fabrication techniques, can be made thinner than Si_xN_y. [11,20]	Insulating. Is etched by KOH and TMAH. [19]
$\alpha-Al_2O_3$	Can be deposited (by atomic layer deposition (ALD)) as an extremely uniform film with thickness control on a nm scale. [17] Very chemically inert. [19]	Insulating. [65] Not commonly used as a free-standing membrane.
DLC	Better electron transparency than Si_xN_y of the same thickness. [62] Electronic, mechanical, and optical properties can be adjusted by changing the film characteristics (hydrogen content, proportions of sp^2 and sp^3 carbon); can be conductive. [66]	Fabrication method and conditions heavily influence film properties; not fully compatible with mainstream fabrication techniques. [66]

HBN is an isoelectronic analogue of graphene, with similar mechanical and thermal properties. Monolayers of hBN have been isolated, and can also be synthesized. [63, 64] In bulk, the interlayer spacing is 0.33 nm.

As mentioned previously, SiO_2 has been successfully used for a 9 nm thick window in the stationary cell by Liu *et al.* [20]; it would be possible to follow a similar fabrication process with the tools available in the University of Waterloo NanoFab. Due to its lower residual stress and Young's modulus, SiO_2 is more flexible than Si_xN_y and thus more prone to bulging. [11]

Alpha-aluminum oxide ($\alpha-Al_2O_3$), also known as sapphire or corundum, has a trigonal crystal structure. [65] It is often used as a substrate for other applications. [19]

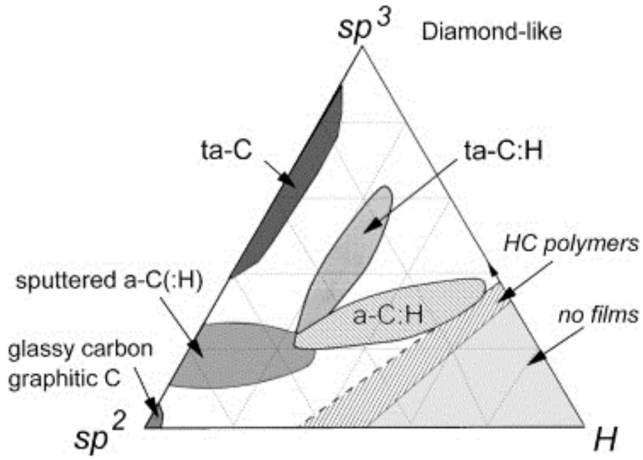

Figure 6.1: Phase diagram of diamond-like carbon and related materials. Reprinted from Materials Science and Engineering R, Vol. 37, Robertson, J., Diamond-like amorphous carbon, pp 129-281, Copyright 2002, with permission from Elsevier. [66] Original caption: "Ternary phase diagram of bonding in amorphous carbon-hydrogen alloys."

Diamond-like carbon (DLC) can refer to a variety of amorphous carbon films, with or without hydrogen. The exact structure, along with the density, reactivity, and many other

properties depend on the composition and on the deposition method. These materials can be described (as in figure 6.1) by hydrogen content, and by the ratio of sp^3 carbon to sp^2 carbon. As an example of how structural changes can impact properties, DLC with high sp^2 content is more conductive, while DLC with high sp^3 content typically has a large band gap. [66] Theoretically, DLC with the appropriate properties could be an excellent window material: it can be deposited onto Si wafers by PECVD, can potentially survive KOH etching, is highly transparent, and can be conductive and very thin. However, finding the exact deposition recipe required would be a time-consuming and expensive process.

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APPENDICES

Appendix A

Detailed fabrication procedures

This appendix describes all of the microfabrication procedures used to produce the nanofluidic cells. In the following section, each individual process is described; section A.2 on page 126 gives instructions organized by the chip design being produced. Unless otherwise specified, all fabrication (with the exception of KOH etching) was performed in the University of Waterloo Quantum NanoFab. Specific NanoFab equipment will be referred to by the label used in the Badger lab management software, e.g. (XXXXX-xxxx). The theory behind the majority of the techniques used is described in section 5.1 on page 67.

A.1 Procedures by process

These procedures are written as a supplement to the standard operating procedures (SOPs) available for each tool in the NanoFab; not all details of standard instrument operation are included. For every procedure, proper tweezers for handling wafers and wafer fragments are required. Some stations in the NanoFab have tweezers available, but not all. It is advisable

to also have a permanent marker at all times for labelling, and a cleanroom notebook for checking and recording notes. When describing materials and equipment required for a process, items typically available at the relevant NanoFab station will not be explicitly listed.

A.1.1 Piranha cleaning of wafers

NanoFab tools used:

- (PIRANHA) - wet bench designated for Piranha; must have a "buddy" present in the NanoFab to use.
- (SRD-PIRANHA) - Automated spin-rinse-dry equipment.

Method:

1. Obtain the following:
    - Blank wafers to be cleaned (up to 22 at a time), in storage box.
    - 4 L beaker and modified wafer rack; stored in Solvent 2 wet bench cupboard.
2. Place wafers into the modified rack (starting from the bottom end) and place the rack into the 4 L beaker.
3. Observe what volume of Piranha solution would be required to cover the wafers, then remove the rack from the beaker.
4. Calculate the required amounts of 18 mol/L H_2SO_4 and 30 % H_2O_2, with 4 parts H_2SO_4 to every 1 part H_2O_2.

5. As soon as you begin working at the Piranha fume hood, put on the protective apron, then the face mask, and then the protective gloves. Remember to remove these in reverse order any time you leave the fume hood!

6. Measure the H_2SO_4 and H_2O_2 into separate beakers; marking the correct fill line with a marker makes this faster and easier.

7. Pour the H_2SO_4 into the (empty, dry) 4 L beaker.

8. Slowly pour the H_2O_2 into the beaker with the H_2SO_4.

9. Place the rack of wafers into the solution and wait 15 min; the solution self-heats to boiling.

10. Remove rack of wafers and place in the (empty) quick dump rinse (QDR) bath and press the start button. When finished, drain with the F4 button.

11. Dry wafers with N_2 and transfer into the standard wafer rack.

12. Put wafers into the (SRD-PIRANHA) and run the cycle (DI water rinse, N_2 purge, two stage drying under N_2).

13. Put wafers away in storage box and ensure station is clean; leave Piranha solution at the back of the fume hood, labelled with date, time, and name of user.

A.1.2 LPCVD of silicon nitride

NanoFab tools used:

- (TYSTAR2-nitride) - Tytan 4600 mini four-stack horizontal furnace.

Wafers must undergo appropriate cleaning immediately before LPCVD. Up to 50 wafers can be processed simultaneously. This process is only done under supervision, so instructions are not given. The deposition conditions are as follows: feed gas is three parts NH_3 to one part $SiCl_2H_2$ at a pressure of 200 - 400 mtorr and temperature of $800 - 850$ °C.

A.1.3 Positive photolithography with AZ P4620

NanoFab tools used:

- (FISHER-oven) - Thermo Scientific 3490M Class 100 Cleanroom Convection Oven; for applying resist.
- (REYNOLDSTECH-twincoater) - Headway Research PMW32-PS spinner, in fume hood with two hotplates; for applying resist.
- (SUSS-align) - Karl Suss MA6 mask aligner; for exposing resist.
- (DEVELOPUV) - wet bench designated for development of UV photoresists; for developing resist.
- (SOLVENT1) - general wet bench; for removing resist.

Method for applying resist:

1. Turn on the (FISHER-oven) to 150 °C
2. Obtain the following:
    - Wafers to be patterned.
    - Storage cassette for each wafer.

- Carrier wafer(s), one per hotplate in use - cassettes labelled “Hotplate.”
- Aluminium foil and scissors.

3. Dry wafers in the (FISHER-oven) for at least $10 - 15$ min, using the metal rack; remove wafers to process one at a time.

4. Cut a piece of foil approximately 30 cm per side, and make a small hole in the centre. Use the foil to line Spinner #2 (on the right hand side of (REYNOLDSTECH-twincoater) bench).

5. Put the large round chuck in place on the spinner.

6. Turn on the hotplate(s) to 115 °C, and place the carrier wafer(s) on the hotplate(s).

7. Set the recipe on the spinner:

   - 5 s at 500 rpm, with a ramp of 100 rpm/s
   - 30 s at 2000 rpm, with a ramp of 200 rpm/s
   - Ensure all remaining steps are empty.

8. Pour an appropriate amount of AZ P4620 photoresist into a small beaker (a few mLper wafer), and cover with a larger beaker when not in use. Make sure to reseal the bottle with Parafilm.

9. Use tweezers to remove a single wafer from the oven, place it onto the chuck (centred as much as possible); run a dummy spin (i.e. run the recipe without resist to ensure the wafer stays in place).

10. Pour resist onto the centre of the wafer until approximately two-thirds of the surface is covered, and start the spinner.

11. After spinning, carefully move wafer onto the carrier wafer (leave them offset for easy removal); bake for 3 min.

12. Set wafer aside to dry; repeat from step 9 for each wafer. Turn off the oven after all wafers are removed.

13. Add a layer of protective resist to the back of each wafer (ensure the resist on the first side is fairly dry first).

14. Using a cotton swab and small beaker of acetone, remove resist from the edge of each wafer to approximately 3 mm in (only relevant on the side of the wafer which will be etched by RIE).

15. Put each wafer into a cassette with the lid partially closed, and allow to cure for $1.5 - 2.5$ h.

16. Ensure station is clean; excess resist is rinsed down the cup-sink with acetone.

Method for exposing resist:

1. Obtain the appropriate photomask(s).

2. Check the parameters on the (SUSS-align):

    - Light source on CH2 (405 nm UV light, 25 mW/cm^2 intensity).
    - Align at 30 μm separation.
    - Expose in vacuum mode, 5 s duration for each step.
    - Exposure time is 29.5 s.
    - Top side alignment (TSA) mode is enabled.

3. Ensure the appropriate chuck (for 4” wafers) is loaded.
4. Load the appropriate mask, chrome side towards the wafer, as per the SOP.
5. Load the wafer as per the SOP, and align to the alignment features on the mask.
6. Expose, remembering to look away.
7. Store exposed wafer in a labelled cassette, and repeat process for remaining wafers.

Method for developing resist:

1. Rinse the two Petri dishes with AZ 400K developer (waste to cup-sink), and fill them with enough developer to cover a single wafer.
2. Rinse and then fill two larger dishes with DI water.
3. Quickly place a wafer into each Petri dish (exposed side up), and immediately start the timer (set to 3 min).
4. Gently agitate the dishes by hand for the duration of development.
5. After 3 min, transfer each wafer to a water bath, and let soak at least 1 min.
6. Rinse each wafer with the DI water spray gun and check features; if some features are not clearly visible, develop again.
7. Dry wafers with N_2 and store in labelled cassettes.
8. Repeat for all remaining wafers; replace developer with fresh solution after every two or three uses.

Method for removing resist:

1. Obtain the following:
    - 4 L beaker and modified wafer rack; stored in Solvent 2 wet bench cupboard.
    - Large bottle of IPA.
    - Large bottle of Remover PG or Baker PRS-3000.
2. Place wafers in modified rack, and place rack in the 4 L beaker.
3. Add enough Remover PG or Baker PRS-3000 to cover the wafers.
4. Place the beaker in the sonication bath (use the largest metal basket) and sonicate for 15 min.
5. Set rack of wafers aside (in a dish or on a wipe) and dispose of remover solution (cup-sink).
6. Return wafers to beaker and add enough IPA to cover; let soak for 5 min (or until all resist is gone).
7. Rinse each wafer with DI water and dry with N_2; place in cassette.
8. Ensure station is clean.

A.1.4 Positive photolithography with S1811

NanoFab tools used:

- (FISHER-oven) - Thermo Scientific 3490M Class 100 Cleanroom Convection Oven; for applying resist.

- (REYNOLDSTECH-twincoater) - Headway Research PMW32-PS spinner, in fume hood with two hotplates; for applying resist.
- (SUSS-align) - Karl Suss MA6 mask aligner; for exposing resist.
- (DEVELOPUV) - wet bench designated for development of UV photoresists; for developing resist.
- (SOLVENT1) - general wet bench; for removing resist.

Method for applying resist:

1. Turn on the (FISHER-oven) to 150 °C.
2. Obtain the following:
    - Wafers to be patterned.
    - Storage cassette for each wafer.
    - Carrier wafer(s), one per hotplate in use - cassettes labelled "Hotplate."
    - Aluminium foil and scissors.
3. Dry wafers in the (FISHER-oven) for at least $10 - 15$ min, using the metal rack; remove wafers to process one at a time.
4. Cut a piece of foil approximately 30 cm per side, and make a small hole in the centre. Use the foil to line Spinner #2 (on the right hand side of (REYNOLDSTECH-twincoater) bench).
5. Put the large round chuck in place on the spinner.

6. Turn on the hotplate(s) to 120 °C, and place the carrier wafer(s) on the hotplate(s).
7. Set the recipe on the spinner:
    - 4 s at 500 rpm, with a ramp of 100 rpm/s
    - 60 s at 5000 rpm, with a ramp of 500 rpm/s
    - Ensure all remaining steps are empty.
8. Pour an appropriate amount of S1811 photoresist into a small beaker (a few mLper wafer), and cover with a larger beaker when not in use. Make sure to reseal the bottle with Parafilm.
9. Use tweezers to remove a single wafer from the oven, place it onto the chuck (centred as much as possible); run a dummy spin (i.e. run the recipe without resist to ensure the wafer stays in place).
10. Pour resist onto the centre of the wafer until approximately two-thirds of the surface is covered, and start the spinner.
11. After spinning, carefully move wafer onto the carrier wafer (leave them offset for easy removal); bake for 1.5 min.
12. Set wafer aside to dry; repeat from step 9 for each wafer. Turn off the oven after all wafers are removed.
13. Add a layer of protective resist to the back of each wafer (ensure the resist on the first side is fairly dry first).
14. Using a cotton swab and small beaker of acetone, remove resist from the edge of each wafer to approximately 3 mm in (only relevant on the side of the wafer which will be etched by RIE).

15. Put each wafer into a labelled cassette.
16. Ensure station is clean; excess resist is rinsed down the cup-sink with acetone.

Method for exposing resist:

1. Obtain the appropriate photomask(s).
2. Check the parameters on the (SUSS-align):
    - Light source on CH2 (405 nm UV light, 25 mW/cm^2 intensity).
    - Align at 30 μm separation.
    - Expose in vacuum mode, 5 s duration for each step.
    - Exposure time is 4.0 s.
    - TSA mode is enabled.
3. Ensure the appropriate chuck (for 4" wafers) is loaded.
4. Load the appropriate mask, chrome side towards the wafer, as per the SOP.
5. Load the wafer as per the SOP, and align to the alignment features on the mask.
6. Expose, remembering to look away.
7. Store exposed wafer in a labelled cassette, and repeat process for remaining wafers.

Method for developing resist:

1. Rinse the two Petri dishes with MF-319 developer (waste to cup-sink), and fill them with enough developer to cover a single wafer.

2. Rinse and then fill two larger dishes with DI water.
3. Quickly place a wafer into each Petri dish (exposed side up) and begin gently agitating each dish by hand.
4. Watch the wafers; continue agitating until very little resist can be seen still developing (approximately $45 - 60$ s).
5. Transfer each wafer to a water bath, and let soak at least 1 min.
6. Rinse each wafer with the DI water spray gun and check features; if some features are not clearly visible, develop again.
7. Dry wafers with N_2 and store in labelled cassettes.
8. Repeat for all remaining wafers; replace developer with fresh solution after every two or three uses.

Method for removing resist:

1. Obtain the following:
    - 4 L beaker and modified wafer rack; stored in Solvent 2 wet bench cupboard.
    - Large bottle of IPA.
    - Large bottle of Remover PG or Baker PRS-3000.
2. Place wafers in modified rack, and place rack in the 4 L beaker.
3. Add enough Remover PG or Baker PRS-3000 to cover the wafers.
4. Place the beaker in the sonication bath (use the largest metal basket) and sonicate for 15 min.

5. Set rack of wafers aside (in a dish or on a wipe) and dispose of remover solution (cup-sink).

6. Return wafers to beaker and add enough IPA to cover; let soak for 5 min (or until all resist is gone).

7. Rinse each wafer with DI water and dry with N_2; place in cassette.

8. Ensure station is clean.

A.1.5 Dry etching of silicon nitride

NanoFab tools used:

- (OXFORD-metalRIE) - Oxford ICP380 Reactive Ion Etcher

Method:

1. Obtain the following:
    - Patterned wafers to be etched.
    - Cleaning wafer (a blank, clean Si wafer).
2. Ensure that at least 3 mm around the edge of each wafer is completely cleaned of photoresist; if not, the wafer may get stuck inside the RIE.
3. Place the wafer into the sample loading bay, patterned side up. Carefully align the wafer such that the flat is centred between the alignment posts.
4. Select and run the "OPT-SiNx Etch" recipe, as per the SOP.

- Si_xN_y etch rate is 121.0 nm/min, the etching step is 1 min long.
- Feed gas is SF_6 with a flow rate of 45.0 sccm, backing gas is 10.0 sccm He.
- Chamber temperature is 5 °C.

5. After etching five wafers or when finished all etching, run the "O2/SF6 clean" recipe with the cleaning wafer loaded.
   - Etching time is 10 min.
   - Feed gases are 50.0 sccm O_2 and 20.0 sccm SF_6.
   - Chamber temperature is 40.0 °C.

A.1.6 Wet etching of silicon

KOH etching is carried out in the UeIL wet lab. A detailed SOP, including the procedure for preparing KOH solution, is available in the lab. Wet etching should not be performed alone; at least one other person should be present in the immediate area and aware that etching is taking place.
Materials and equipment required:

- Wafers to be etched, up to 18 at a time.
- Etching apparatus, as shown in figure A.1 on page 116.
- 25 wt% KOH solution.
- 4 L Pyrex beaker.
- Large crystallization dish.

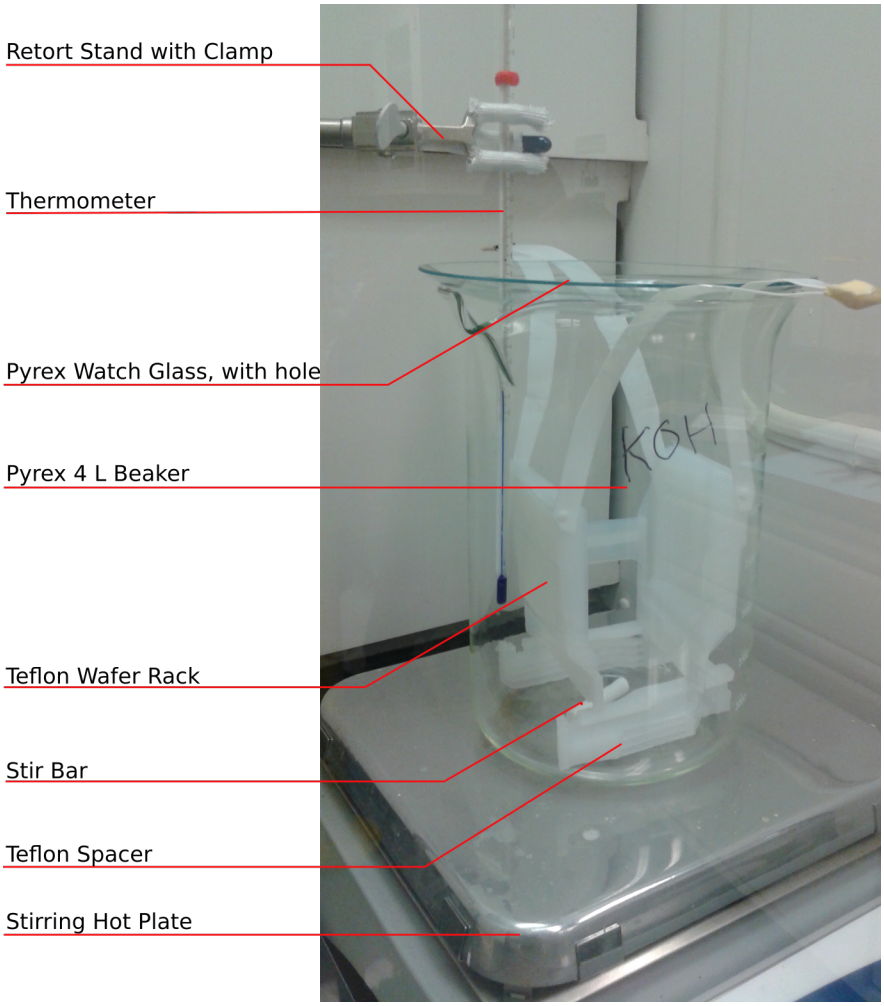

Figure A.1: KOH etching apparatus, consisting of a 4 L Pyrex beaker and watch glass (with a hole drilled for the thermometer) on a stirring hotplate, with a large Teflon stir bar and a Pyrex thermometer clamped to a retort stand. A modified Teflon wafer rack with handles sits on a Teflon spacer (the cut off end of the rack), to allow the stir bar to move freely. Note that the thermometer bulb should be approximately half-way up the wafer rack. DI water from a wash bottle can be added via the spout of the beaker if needed (to replace water which boiled away).

When working with KOH solution (and especially hot KOH solution), wear appropriate protective equipment and clothing, including a face shield and thick gloves. Keep the sash of the fume hood lowered as far as possible.
Method:

1. Set up the etching beaker with stir bar and spacer on the hot plate and add 3 L of KOH solution.
2. Cover with watch glass and clamp thermometer in place.
3. Begin stirring and heating; target temperature is 90 °C.
4. Place wafers into modified rack, beginning in the centre and spacing them as far apart as possible. Track the location of each wafer so they can be identified after etching.
5. Once solution temperature is stabilized at 90 °C, transfer the rack of wafers into the etching beaker and begin timing.
6. During etching, monitor the temperature and solution volume; add DI water as needed.
7. Fill the second 4 L beaker with a few litres of DI water; this is the rinse bath.
8. When etching is complete, remove the wafers and rinse:
    - Transfer the wafer rack to the rinse beaker and submerge a few times.
    - Move the rack to the crystallization dish to gently rinse individual wafers.
    - If only some of the wafers are completed, transfer them to another wafer rack and return the remaining wafers to the etching beaker.

9. Carefully and gently dry each wafer using the N_2 gas tap in the fume hood before storing in labelled wafer cassettes.

10. Allow the KOH solution to cool (with stirring) to 40 °C or lower before transferring to a storage or waste bottle.

A.1.7 Negative photolithography with maN-1410

NanoFab tools used:

- (FISHER-oven) - Thermo Scientific 3490M Class 100 Cleanroom Convection Oven; for applying resist.
- (REYNOLDSTECH-twincoater) - Headway Research PMW32-PS spinner, in fume hood with two hotplates; for applying resist.
- (SUSS-align) - Karl Suss MA6 mask aligner; for exposing resist.
- (DEVELOPUV) - wet bench designated for development of UV photoresists; for developing resist.
- (SOLVENT1) - general wet bench; for removing resist.

Method for applying resist:

1. Turn on the (FISHER-oven) to 150 °C.
2. Obtain the following:
    - Wafers to be patterned.

- Storage cassette for each wafer.
- Carrier wafer(s), one per hotplate in use - cassettes labelled “Hotplate.”
- Aluminium foil and scissors.

3. Dry wafers in the (FISHER-oven) for at least $10 - 15$ min, using the metal rack; remove wafers to process one at a time.

4. Cut a piece of foil approximately 30 cm per side, and make a small hole in the centre. Use the foil to line Spinner #2 (on the right hand side of (REYNOLDSTECH-twincoater) bench).

5. Put the large round chuck in place on the spinner.

6. Turn on the hotplate(s) to 110 °C, and place the carrier wafer(s) on the hotplate(s).

7. Set the recipe on the spinner:

   - 5 s at 500 rpm, with a ramp of 100 rpm/s
   - 60 s at 3000 rpm, with a ramp of 500 rpm/s
   - Ensure all remaining steps are empty.

8. Pour an appropriate amount of maN-1410 photoresist into a small beaker (a few mLper wafer), and cover with a larger beaker when not in use. Make sure to reseal the bottle with Parafilm.

9. Use tweezers to remove a single wafer from the oven, place it onto the chuck (centred as much as possible); run a dummy spin (i.e. run the recipe without resist to ensure the wafer stays in place).

10. Pour resist onto the centre of the wafer until almost the entire wafer is covered, and start the spinner.

11. After spinning, carefully move wafer onto the carrier wafer (leave them offset for easy removal); bake for 1.5 min.

12. Set wafer aside to dry; repeat from step 9 for each wafer. Turn off the oven after all wafers are removed.

13. Put each wafer into a labelled cassette.

14. Ensure station is clean; excess resist is rinsed down the cup-sink with acetone.

Method for exposing resist:

1. Obtain the appropriate photomask(s).

2. Check the parameters on the (SUSS-align):

    - Light source on CH1 (365 nm UV light, 10 mW/cm^2 intensity).
    - Align at 30 µm separation.
    - Expose in vacuum mode, 5 s duration for each step.
    - Exposure time is 35 s.

3. Load the appropriate mask, chrome side towards the wafer, and follow the SOP for back side alignment (BSA).

4. After BSA procedure is complete (image is grabbed), ensure the appropriate chuck (for 4" wafers) is loaded.

5. Load the wafer as per the SOP, and align following the BSA SOP.
6. Expose, remembering to look away.
7. Store exposed wafer in a labelled cassette, and repeat process for remaining wafers.

Method for developing resist:

1. Rinse the two Petri dishes with ma-D 533/S developer (waste to cup-sink), and fill them with enough developer to cover a single wafer.
2. Rinse and then fill two larger dishes with DI water.
3. Quickly place a wafer into each Petri dish (exposed side up), and immediately start the timer (set to 2 min).
4. Gently agitate the dishes by hand for the duration of development.
5. After 2 min, transfer each wafer to a water bath, and let soak at least 1 min.
6. Rinse each wafer with the DI water spray gun and check features; if some features are not clearly visible, develop again.
7. Dry wafers with N_2 and store in labelled cassettes.
8. Repeat for all remaining wafers; replace developer with fresh solution after every two or three uses.

Method for removing resist:

1. Obtain the following:

- 4 L beaker and modified wafer rack; stored in Solvent 2 wet bench cupboard.
- Large bottle of IPA.
- Large bottle of acetone.
- Large bottle of Remover PG.

2. Place wafers in modified rack, and place rack in the 4 L beaker.
3. Follow steps 4 through 7 for each of the following phases:
   (a) Acetone
   (b) Remover PG
   (c) Acetone
   (d) IPA
4. Add enough solvent (or solution) to cover the wafers.
5. Place the beaker in the sonication bath (use the largest metal basket) and sonicate for 5 min at 50 °C.
6. Set rack of wafers aside (in a dish or on a wipe) and empty beaker into cup-sink.
7. Return wafers to beaker.
8. Rinse each wafer with DI water and dry with N_2; place in cassette.
9. Ensure station is clean.

A.1.8 Metal film deposition

NanoFab tools used:

- (INTLVAC-Ebeam) - Intlvac Nanochrome II-UHV system/e-beam evaporator, with SQC-310 Thin Film Deposition Controller and Inficon CI-100 Indexer.

Method:

1. Obtain the following:
    - Wafers (up to four at a time).
    - Appropriate sample stage.
2. Vent the chamber and remove the sample stage (which may or may not be the appropriate stage for this process).
3. Secure the wafers to the sample stage:
    - Arrange the wafer on the stage, window side up.
    - Use the wire clips to secure each wafer, covering as little area as possible.
    - If a separate physical mask is being used (rather than a lift-off process with negative photoresist), secure each wafer and mask pair to the stage together, ensuring they are well aligned.
4. Place the sample stage back in the chamber.
5. Nudge the shutter to one side to check that the correct crucible is in place.
6. Close and lock the chamber door and begin pumping; target pressure is $4 \cdot 10^{-6}$ torr or less.

7. Choose a deposition recipe and check its parameters; for both Ti and Au, the deposition rate can be $0.5 - 3.0$ Å/s, with 1.0 Å/s being typical.
    - "Deposit Ti" for Ti; crucible is made of W.
    - "Deposit Au" for Au; crucible is made of Fabmate-VC.
8. Start the profile, then turn on DC, then the sweep, then start layer.
9. Check the beam alignment through the chamber window, adjust if needed.
10. Monitor the power during deposition, and complete the instrument log.
11. When deposition is finished, turn off emissions and then DC.
12. Remove samples, close and lock the chamber, and begin pumping down.

A.1.9 Manual chip separation

The Teflon supports used for manual separation are shown in figures 5.2 and 5.3, on pages 76 and 76 respectively. This process is typically carried out in the sample preparation lab associated with the NanoFab.
Method:

1. Obtain the following:
    - Teflon supports and glass slides.
    - Chip storage trays.
    - Fully etched wafer.
    - Cleanroom wipes to place under wafers and wafer pieces.

2. Break off the rounded sections along at least two sides of the wafer, leaving a squared corner; gentle pressure with tweezers is often sufficient.

3. Place the wafer section (window side down) on the long Teflon support such that the windows align with the troughs (as shown in figure 5.2 on page 76).

4. Slide the wafer section until a single column of chips protrudes past the edge of the support.

5. Hold the wafer section in place by pressing down with a glass slide, and use another glass slide to snap off the protruding row (keep the slides flat against the wafer to distribute the pressure).

6. Set aside the column of chips and continue from step 4 until the desired number of chips has been reached.

7. Place a single column of chips (window side down) on the short Teflon support, aligning the edge of the column with the ridge (as shown in figure 5.3 on page 76).

8. Slide the column along until a single chip protrudes past the edge; hold the column in place by applying pressure with a glass slide.

9. Use either a glass slide or the flat of a pair of wafer tweezers to break off the protruding chip.

10. Place the chip in a storage tray (window side up) and continue from step 8 until all columns of chips are separated.

11. If desired, use the visible-light microscope to inspect the chips and identify broken windows. For best results, use dark field mode and turn off the room lights.

12. Dispose of broken chips and wafer fragments in the glass waste.

A.2 Procedures by chip design

The following sections briefly outline the procedures which were used for each style of chip; refer to section A.1 on page 102 for detailed instructions for each individual process. All wafers used were 300 μm thick {100} Si, lightly p-doped (with B) to a resistivity of $1 - 10\ \Omega$cm. The wafers were 4" in diameter, polished on both sides, and were purchased from University Wafer. When describing wafer orientation, the "window" side refers to what will be the interior of the fluidic cell, with an intact Si_3N_4 membrane.

A.2.1 First generation chips with Ti spacer

Section 5.2.1 on page 72 also describes this procedure, as shown in figure 5.1 on page 73. These chips can be produced with windows 10, 25, or 50 μm wide (always 250 μm long). For any photomask labels including "XX," XX can be 10, 25, or 50. The desired window size should be chosen before beginning fabrication.

- Before beginning fabrication, ensure that the booking is made for the LPCVD (TYSTAR2-nitride); contact Nathan Nelson-Fitzpatrick (or another NanoFab senior staff member) and consult with him before booking.
- Top and bottom wafers processed together:
    1. Obtain blank Si wafers.
    2. Clean wafers with Piranha solution for 15 min (section A.1.1 on page 103).

3. As soon as possible after the Piranha clean, deposit 50 nm of Si_3N_4 via LPCVD (section A.1.2 on page 104).
4. Pattern the wafers with AZ P4620 positive photoresist (section A.1.3 on page 105) in preparation for etching.
   - Top wafers: use the mask for the windows (figure B.3 on page 139), labelled "TopXXum."
   - Bottom wafers: use the mask for the windows, inlets, and outlets (figure B.1 on page 137), labelled "BotXXum."
5. Dry etch the patterned side of each wafer via RIE (section A.1.5 on page 114) to reveal bare Si inside the features; ideally this should be done within a day or two of the lithography.
6. Remove photoresist (section A.1.3 on page 105); this should be done shortly after RIE if possible. The sooner the resist is removed, the easier it is to do so.
7. Take wafers to the C2-079 lab; wet etch the features with KOH (section A.1.6 on page 115). Etch the bottom wafers for about 1.5 h, and etch the top wafers to completion (approximately 3 h; you should be able to see through the windows). Typically all wafers were loaded into the rack at the beginning of etching, with the bottom wafers removed after 1.5 h.

- Bring the wafers back to the NanoFab.
- Top wafers only:
  1. Pattern the window side of each wafer with maN-1410 negative photoresist (section A.1.7 on page 118) in preparation for spacer deposition. Use the mask with the spacer pattern (figure B.4 on page 140), labelled "spacer."

2. Deposit the Ti spacer (section A.1.8 on page 123).
3. Remove the resist (section A.1.7 on page 118) as soon as possible after metal deposition.

- Bottom wafers only:
  1. Pattern the window side of each wafer with AZ P4620 resist (section A.1.3 on page 105) in preparation for etching. Use the mask labelled "grooves," figure B.2 on page 138.
  2. Dry etch the exposed Si_3N_4 on the window side of each wafer with RIE (section A.1.5 on page 114).
  3. Remove photoresist (section A.1.3 on page 105); this should be done shortly after RIE if possible.
  4. Wet etch the wafers to completion, about 1.5 h (section A.1.6 on page 115).
- Separate the wafers into individual chips as needed.

A.2.2 First generation chips with Au spacer

The chip design is identical (with the exception of spacer composition) to the first generation chips with Ti spacer; the process is somewhat different. Section 5.2.2 on page 75 also describes this procedure, as shown in figure 5.4 on page 78. These chips can be produced with windows 10, 25, or 50 μm wide (always 250 μm long). For any photomask labels including "XX," XX can be 10, 25, or 50. The desired window size should be chosen before beginning fabrication.

- Before beginning fabrication, ensure that the booking is made for the LPCVD (TYSTAR2-nitride); contact Nathan Nelson-Fitzpatrick (or another NanoFab senior staff member) and consult with him before booking.
- Top and bottom wafers processed together:
    1. Obtain blank Si wafers.
    2. Clean wafers with Piranha solution for 15 min (section A.1.1 on page 103).
    3. As soon as possible after the Piranha clean, deposit 50 nm of Si_3N_4 via LPCVD (section A.1.2 on page 104).
    4. Pattern the wafers with AZ P4620 positive photoresist (section A.1.3 on page 105) in preparation for etching.
        - Top wafers: use the mask for the windows (figure B.3 on page 139), labelled "TopXXum."
        - Bottom wafers: use the mask for the windows, inlets, and outlets (figure B.1 on page 137), labelled "BotXXum."
    5. Dry etch the patterned side of each wafer via RIE (section A.1.5 on page 114) to reveal bare Si inside the features; ideally this should be done within a day or two of the lithography.
    6. Remove photoresist (section A.1.3 on page 105); this should be done shortly after RIE if possible. The sooner the resist is removed, the easier it is to do so.
- Top wafers only:
    1. Pattern the window side of each wafer with maN-1410 negative photoresist (section A.1.7 on page 118) in preparation for spacer deposition. Use the mask with the spacer pattern (figure B.4 on page 140), labelled "spacer."

2. Deposit the Au spacer (section A.1.8 on page 123).
3. Remove the resist (section A.1.7 on page 118) as soon as possible after metal deposition.

- Bring all wafers to the C2-079 lab for wet etching.
- Top and bottom wafers processed together:
  1. Wet etch the features with KOH (section A.1.6 on page 115). Etch the bottom wafers for about 1.5 h, and etch the top wafers to completion (approximately 3 h; you should be able to see through the windows).
- Bottom wafers only:
  1. Pattern the window side of each wafer with AZ P4620 resist (section A.1.3 on page 105) in preparation for etching. Use the mask labelled "grooves," figure B.2 on page 138.
  2. Dry etch the exposed Si_3N_4 on the window side of each wafer with RIE (section A.1.5 on page 114).
  3. Remove photoresist (section A.1.3 on page 105); this should be done shortly after RIE if possible.
  4. Wet etch the wafers to completion, about 1.5 h (section A.1.6 on page 115).
- Separate the wafers into individual chips as needed.

A.2.3 Second generation chips with Ti spacer

The bottom chips for this design are also described in section 5.3 on page 77, and shown in figure 5.5 on page 80. The top chips are also described in section 5.3.1 on page 79, and in

figure 5.6 on page 82. These chips can have windows either 10 or 25 μm wide; photomasks corresponding to 10 μm windows have "10" added into their name (for example, "tt10_2" vs. "tt_2").

- Before beginning fabrication, ensure that the booking is made for the LPCVD (TYSTAR2-nitride); contact Nathan Nelson-Fitzpatrick (or another NanoFab senior staff member) and consult with him before booking.
- Top and bottom wafers processed together:
  1. Obtain blank Si wafers.
  2. Clean wafers with Piranha solution for 15 min (section A.1.1 on page 103).
  3. As soon as possible after the Piranha clean, deposit 50 nm of Si_3N_4 via LPCVD (section A.1.2 on page 104).
  4. Pattern the wafers with S1811 positive photoresist (section A.1.4 on page 109) in preparation for etching.
     - Top wafers: use the mask for the windows (figure B.7 on page 144), labelled "tt_2" or "tt10_2."
     - Bottom wafers: use the mask for the windows, inlets, and outlets (figure B.5 on page 142), labelled "bb_2" or "bb10_2."
  5. Dry etch the patterned side of each wafer via RIE (section A.1.5 on page 114) to reveal bare Si inside the features; ideally this should be done within a day or two of the lithography.
  6. Remove photoresist (section A.1.4 on page 109); this should be done shortly after RIE if possible. The sooner the resist is removed, the easier it is to do so.

7. Take wafers to the C2-079 lab; wet etch the features with KOH (section A.1.6 on page 115). Etch the bottom wafers for about 110 min, and etch the top wafers to completion (approximately 165 min; you should be able to see through the windows).

- Bring the wafers back to the NanoFab.
- Top wafers only:
  1. Clip the deposition mask (patterned as in figure B.9 on page 146) to the window side of the wafer, and attach the assembly to the sample stage of the Intlvac e-beam evaporator.
  2. Deposit the Ti spacer (section A.1.8 on page 123).
- Bottom wafers only:
  1. Pattern the window side of each wafer with S1811 resist (section A.1.4 on page 109) in preparation for etching. Use the mask labelled either "bt_2" or "bt10_2" (figure B.6 on page 143), and either apply a thick protective resist to the etched side (section A.1.3 on page 105) or use a carrier wafer.
  2. Dry etch the exposed Si_3N_4 on the window side of each wafer with RIE (section A.1.5 on page 114).
  3. Remove photoresist (section A.1.4 on page 109); this should be done shortly after RIE if possible.
  4. Wet etch the wafers to completion, about 55 min (section A.1.6 on page 115).
- Separate the wafers into individual chips as needed.

A.2.4 Second generation chips with etched spacer

The bottom chips for this design are also described in section 5.3 on page 77, and shown in figure 5.5 on page 80. The top chips are also described in section 5.3.2 on page 81, and in figure 5.7 on page 84. These chips can have windows either 10 or 25 μm wide; photomasks corresponding to 10 μm windows have "10" added into their name (for example, "tt10_2" vs. "tt_2").

- Top wafers only:
  1. Obtain blank Si wafers for the top chips.
  2. Pattern the wafers with S1811 positive photoresist (section A.1.4 on page 109) in preparation for etching; use the mask patterned with the spacer (figure B.8 on page 145), labelled "tbA_2."
  3. Dry etch with RIE (section A.1.5 on page 114) to the desired spacer depth (typically $0.5 - 1$ μm).
  4. Remove photoresist (section A.1.4 on page 109); this should be done shortly after RIE if possible. The sooner the resist is removed, the easier it is to do so.
- Before continuing fabrication, ensure that the booking is made for the LPCVD (TYSTAR2-nitride); contact Nathan Nelson-Fitzpatrick (or another NanoFab senior staff member) and consult with him before booking.
- Top and bottom wafers together:
  1. Obtain blank Si wafers for the bottom chips.
  2. Clean all wafers (the fresh ones and those etched for the top chips) in Piranha solution for 15 min (section A.1.1 on page 103).

3. As soon as possible after the Piranha clean, deposit 50 nm of Si_3N_4 via LPCVD (section A.1.2 on page 104).
4. Pattern the wafers with S1811 positive photoresist (section A.1.4 on page 109) in preparation for etching.
   - Top wafers: use the mask for the windows (figure B.7 on page 144), labelled "tt_2" or "tt10_2."
   - Bottom wafers: use the mask for the windows, inlets, and outlets (figure B.5 on page 142), labelled "bb_2" or "bb10_2."
5. Dry etch the patterned side of each wafer via RIE (section A.1.5 on page 114) to reveal bare Si inside the features; ideally this should be done within a day or two of the lithography.
6. Remove photoresist (section A.1.4 on page 109); this should be done shortly after RIE if possible. The sooner the resist is removed, the easier it is to do so.
7. Take wafers to the C2-079 lab; wet etch the features with KOH (section A.1.6 on page 115). Etch the bottom wafers for about 110 min and etch the top wafers to completion (approximately 165 min; you should be able to see through the windows).

- Bottom wafers only:
  1. Pattern the window side of each wafer with S1811 resist (section A.1.4 on page 109) in preparation for etching. Use the mask labelled either "bt_2" or "bt10_2" (figure B.6 on page 143), and either apply a thick protective resist to the etched side (section A.1.3 on page 105) or use a carrier wafer.
  2. Dry etch the exposed Si_3N_4 on the window side of each wafer with RIE (section A.1.5 on page 114).

3. Remove photoresist (section A.1.4 on page 109); this should be done shortly after RIE if possible.

4. Wet etch the wafers to completion, about 55 min (section A.1.6 on page 115).

- Separate the wafers into individual chips as needed.

Appendix B

Photomasks

This appendix contains images of each photomask used for photolithography. All masks designs were made using LayoutEditor, and all masks were fabricated by the University of Alberta nanoFAB. Equations (2.1) and (2.2), derived from figure 2.6 on page 33, were used to calculate the mask features sizes.

B.1 First generation photomasks

The first generation chips are 6.8 mm long by 2.5 mm wide, and are made from 300 μm thick Si wafers; each wafer contains 388 individual chips. These chips can be produced with windows 10, 25, or 50 μm wide (always 250 μm long). For photomask labels including "XX," XX can be 10, 25, or 50. Refer to section A.2.1 on page 126 and section A.2.2 on page 128 for fabrication procedures.

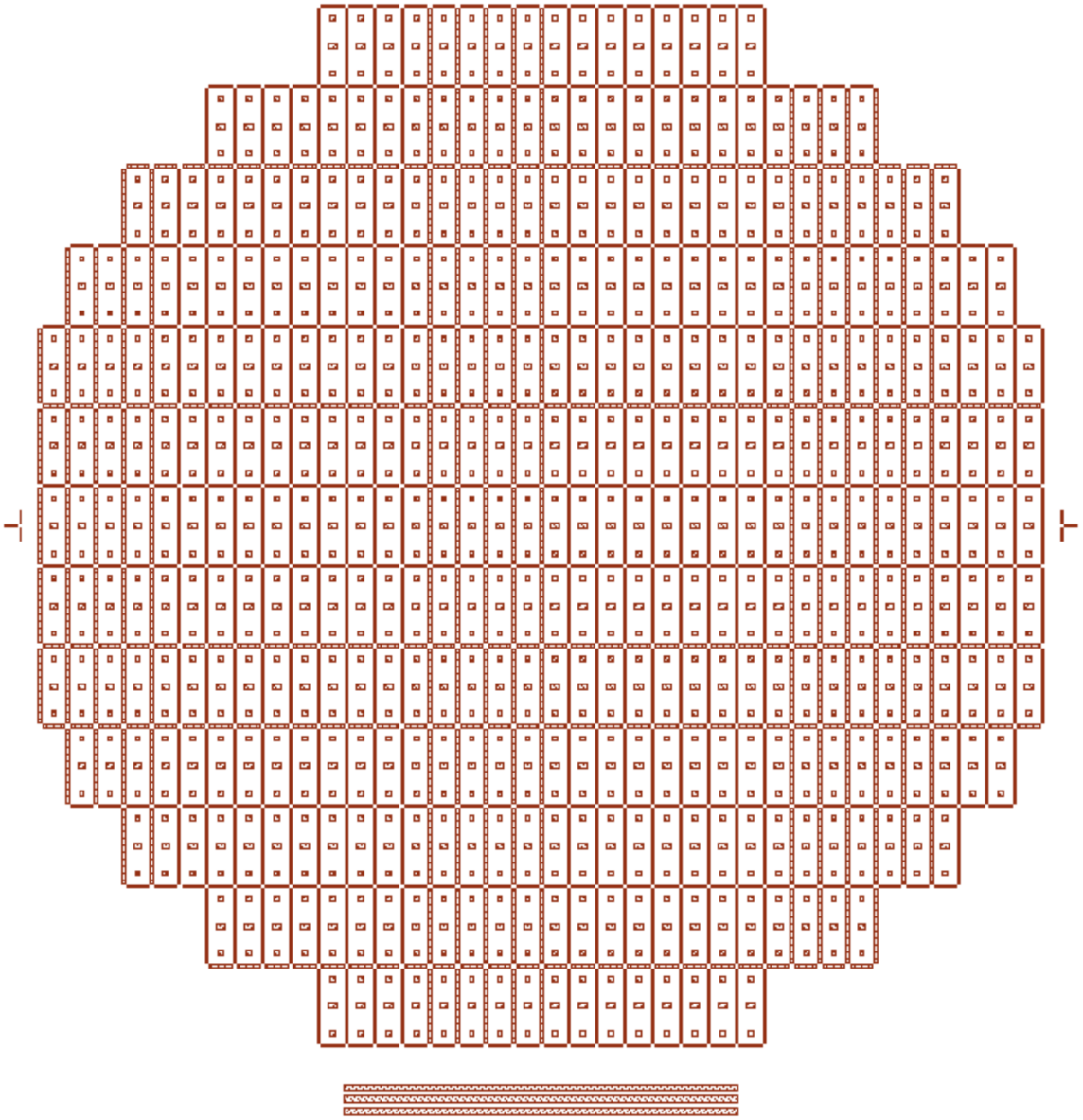

Figure B.1: Photomask for first generation bottom chips; has alignment features, windows, inlets and outlets, and lines separating the individual chips. This is the first mask used for the bottom wafers, and is labelled "BotXXum." Mask features correspond to areas where Si_3N_4 will be etched.

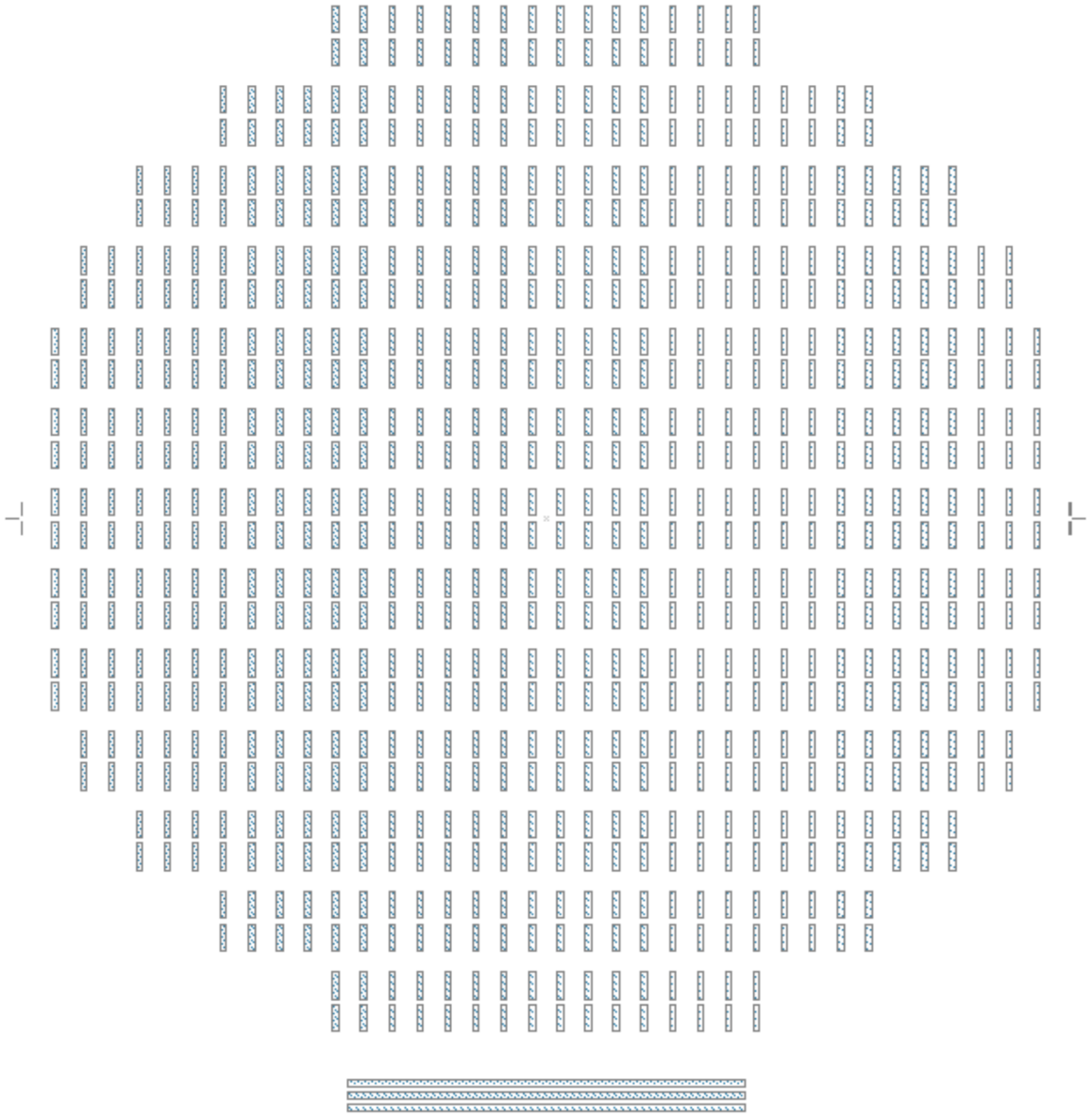

Figure B.2: Photomask for first generation bottom chips; has alignment features and grooves (for increasing the size of the flow channel). This is the second mask used for the bottom wafers (labelled "grooves"), after the initial KOH etching. Mask features correspond to areas where Si_3N_4 will be etched.

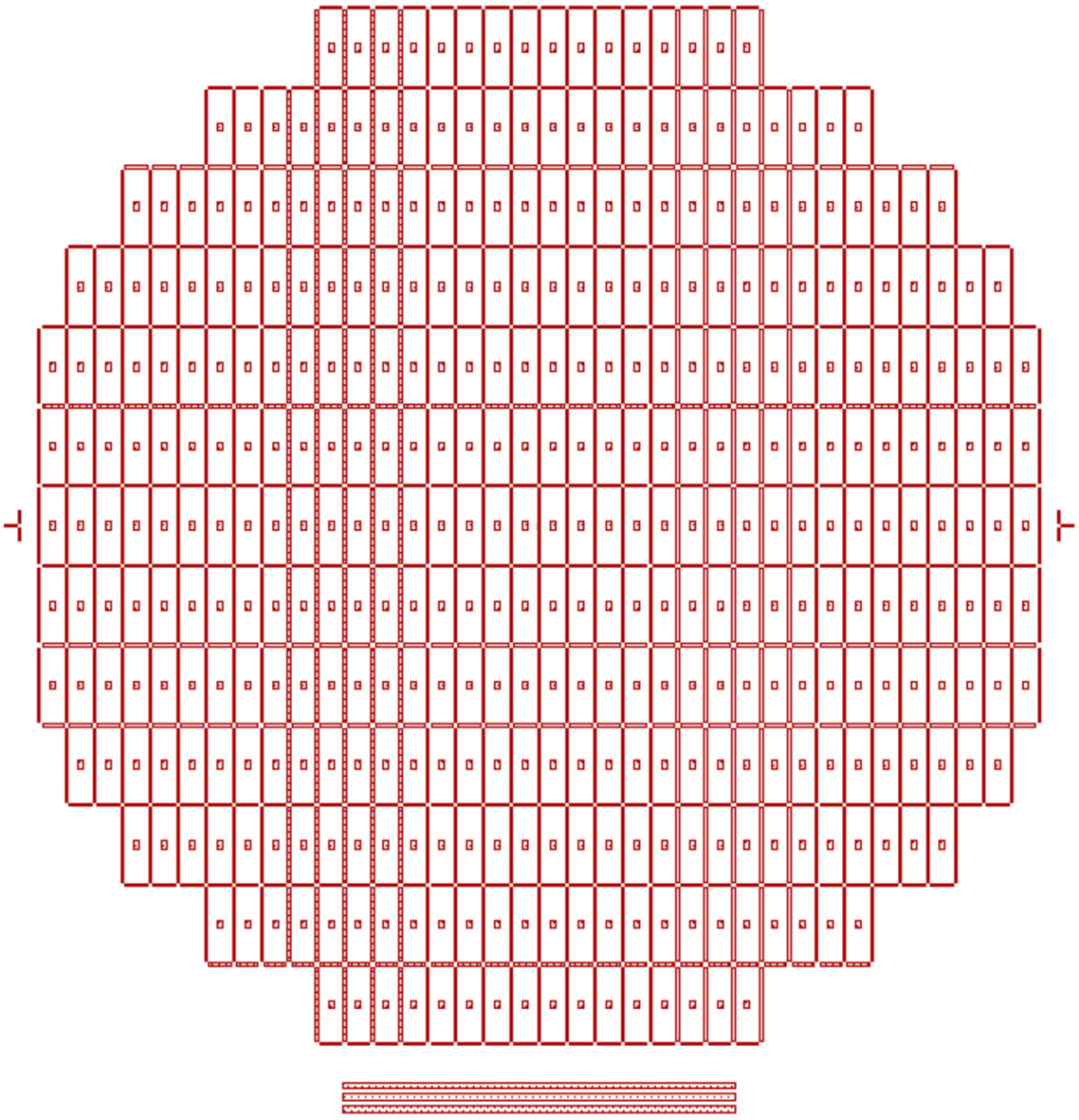

Figure B.3: Photomask for first generation top chips; has alignment features, windows, and lines separating the individual chips. This is the first mask used for the top wafers, and is labelled "TopXXum." Mask features correspond to areas where Si_3N_4 will be etched.

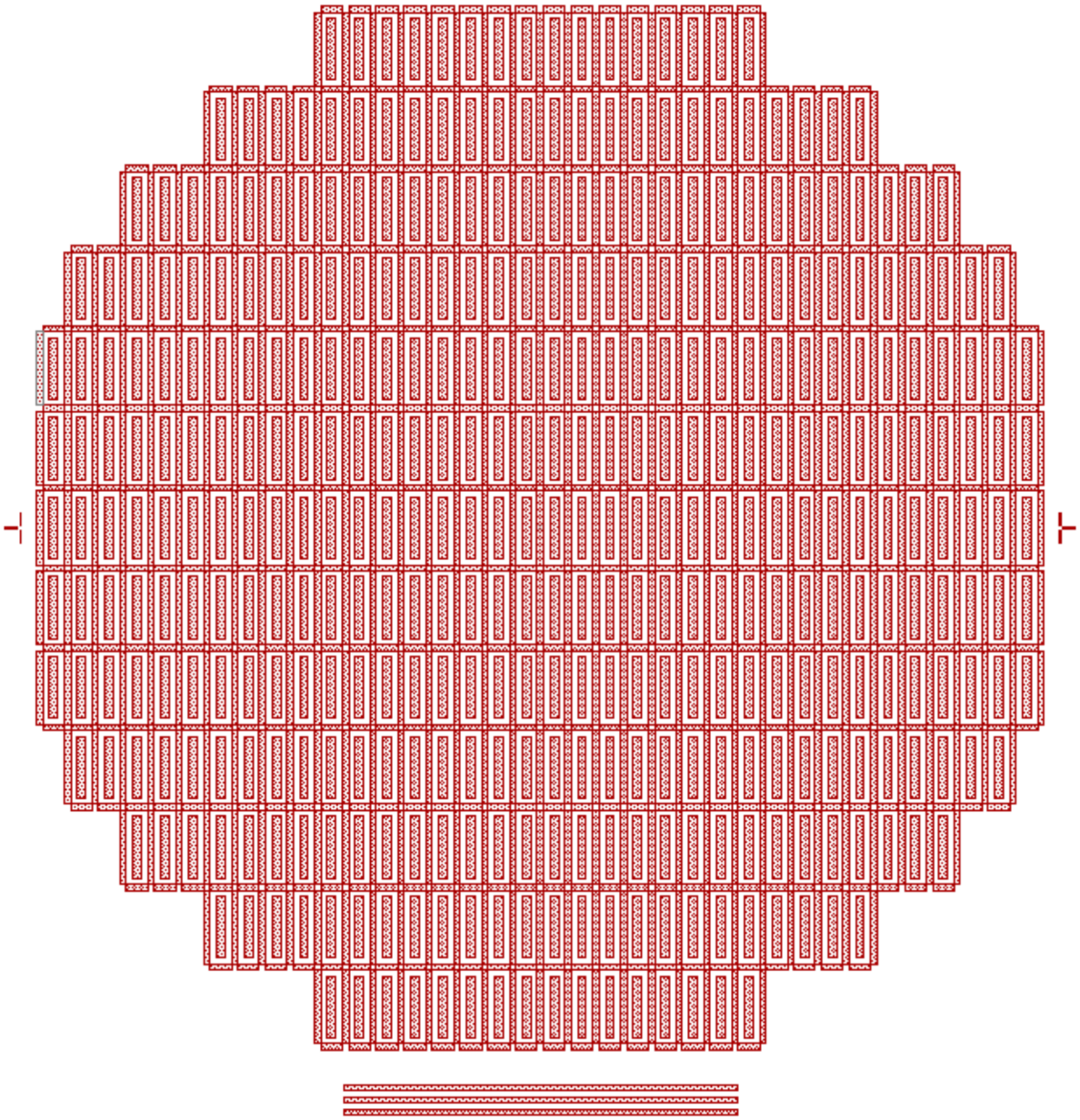

Figure B.4: Photomask for first generation top chips; has alignment features and the spacer pattern. This is the second mask used for the top wafers, and is labelled "spacer." Mask features correspond to areas where the spacer will *not* be deposited.

B.2 Second generation photomasks

The second generation chips are 15 mm long by 2.3 mm wide, and are made from 300 μm thick Si wafers; each wafer contains 135 individual chips. There are a few options for window and step sizes: for the top chip, the window is 250 μm long, and either 10 μm or 25 μm wide. The bottom chips either have windows 10 μm long with a 10 μm long step on either side, or have windows 25 μm long with one of three possible step sizes (25 μm, 50 μm, or 100 μm on each side of the window). The bottom chip windows are always 1200 μm wide. Adjacent chips are connected only along the narrow side, which is etched halfway through. Refer to section A.2.4 on page 133 and section A.2.3 on page 130 for fabrication procedures. All of the masks for the second generation cell are to be used with positive photolithography.

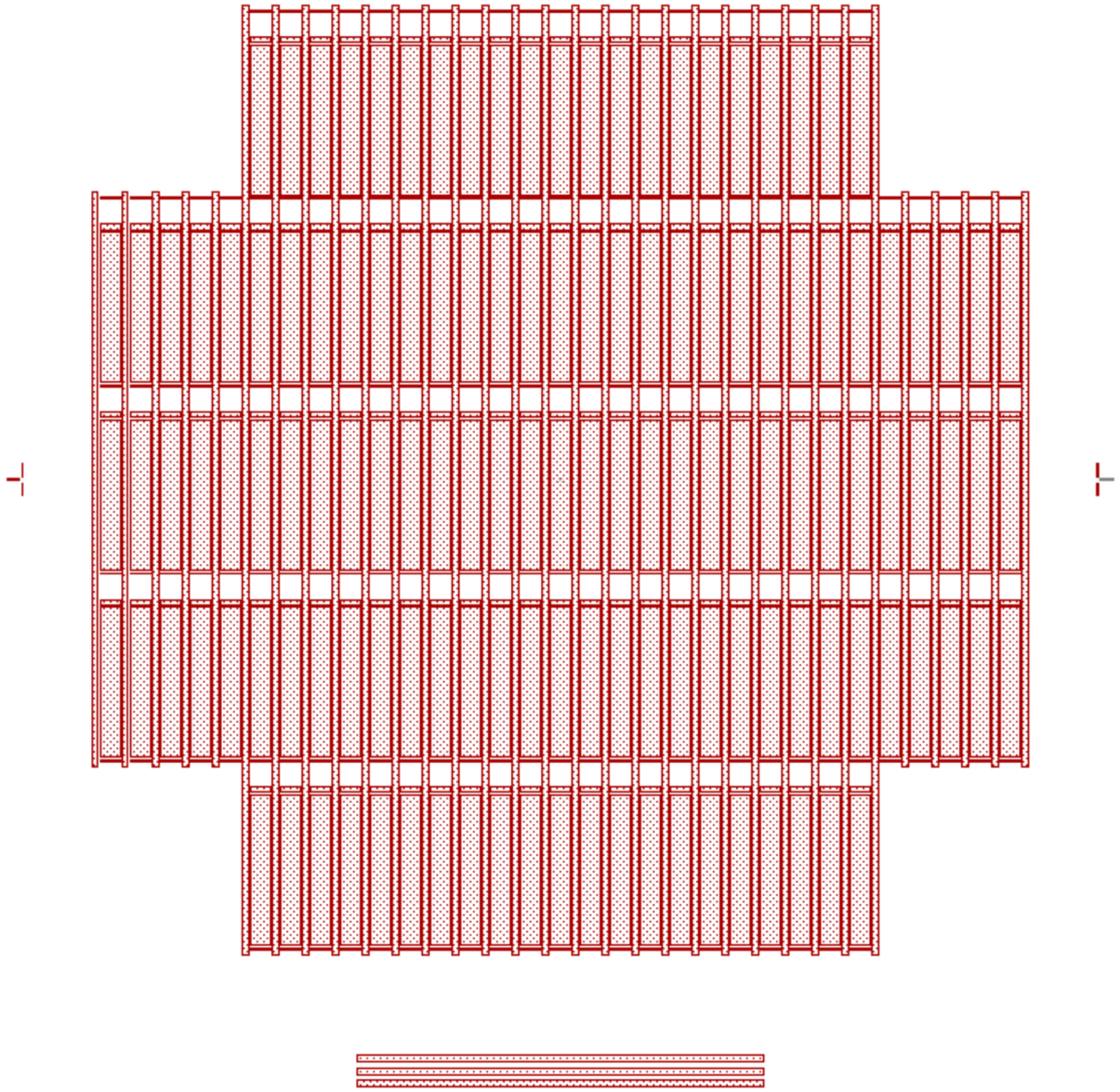

Figure B.5: Photomask for second generation bottom chips; has alignment features, windows, inlets, and lines separating the columns of chips. This is the first mask to be used on the bottom wafers, and is labelled "bb_2" for 25 μm wide windows, or "bb10_2" for 10 μm wide windows. Mask features correspond to areas where Si_3N_4 will be etched.

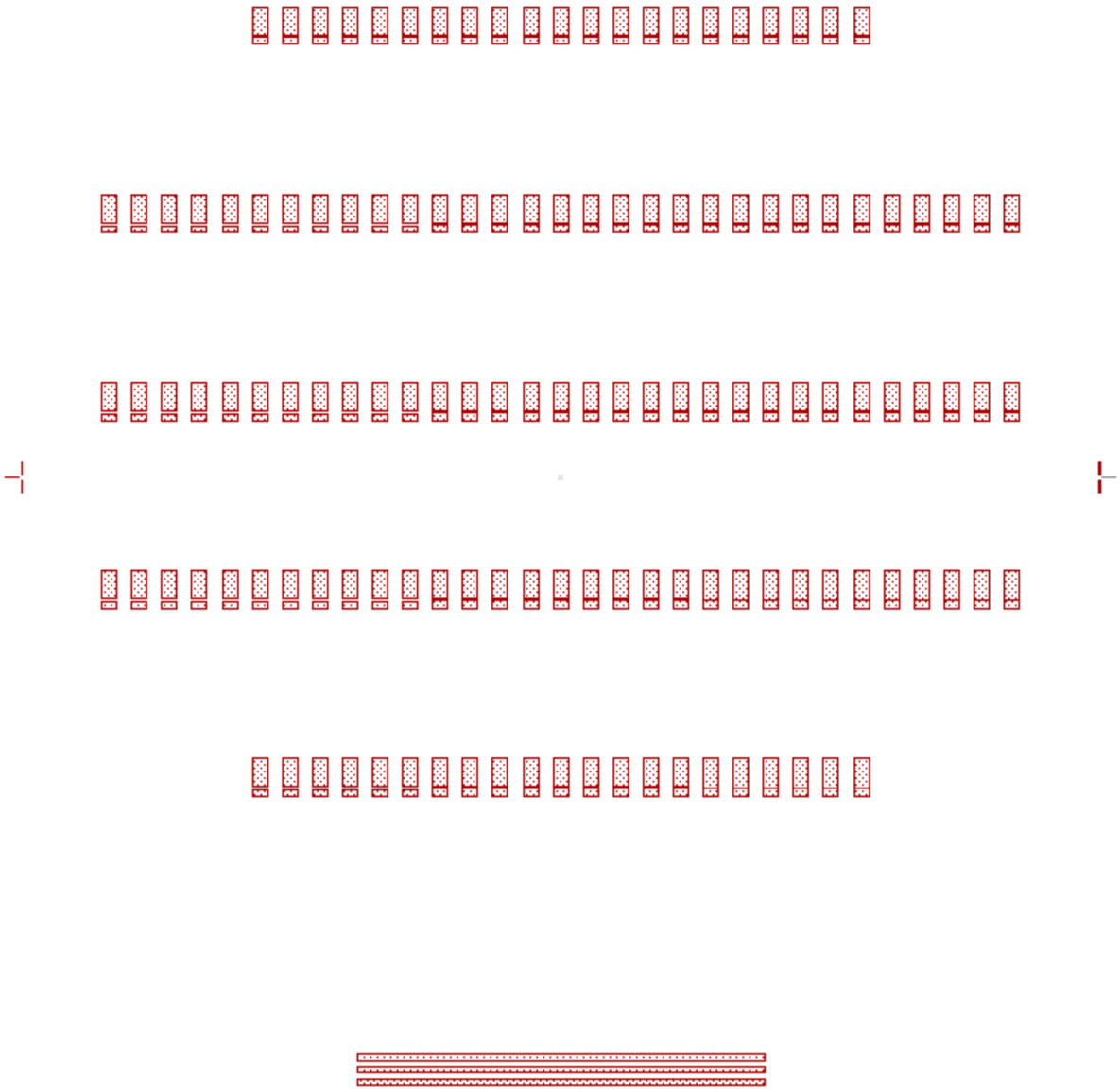

Figure B.6: Photomask for second generation bottom chips; has alignment features and "steps" for the inlet and outlet. Note that for 25 μm wide windows three different sizes of step are present in the mask (25, 50, and 100 μm), with 45 chips for each size; the mask is labelled "bt_2." For 10 μm wide windows, only one step size (10 μm) is present, and the mask is labelled "bt10_2." This is the second mask to be used on the bottom wafers. Mask features correspond to areas where Si_3N_4 will be etched.

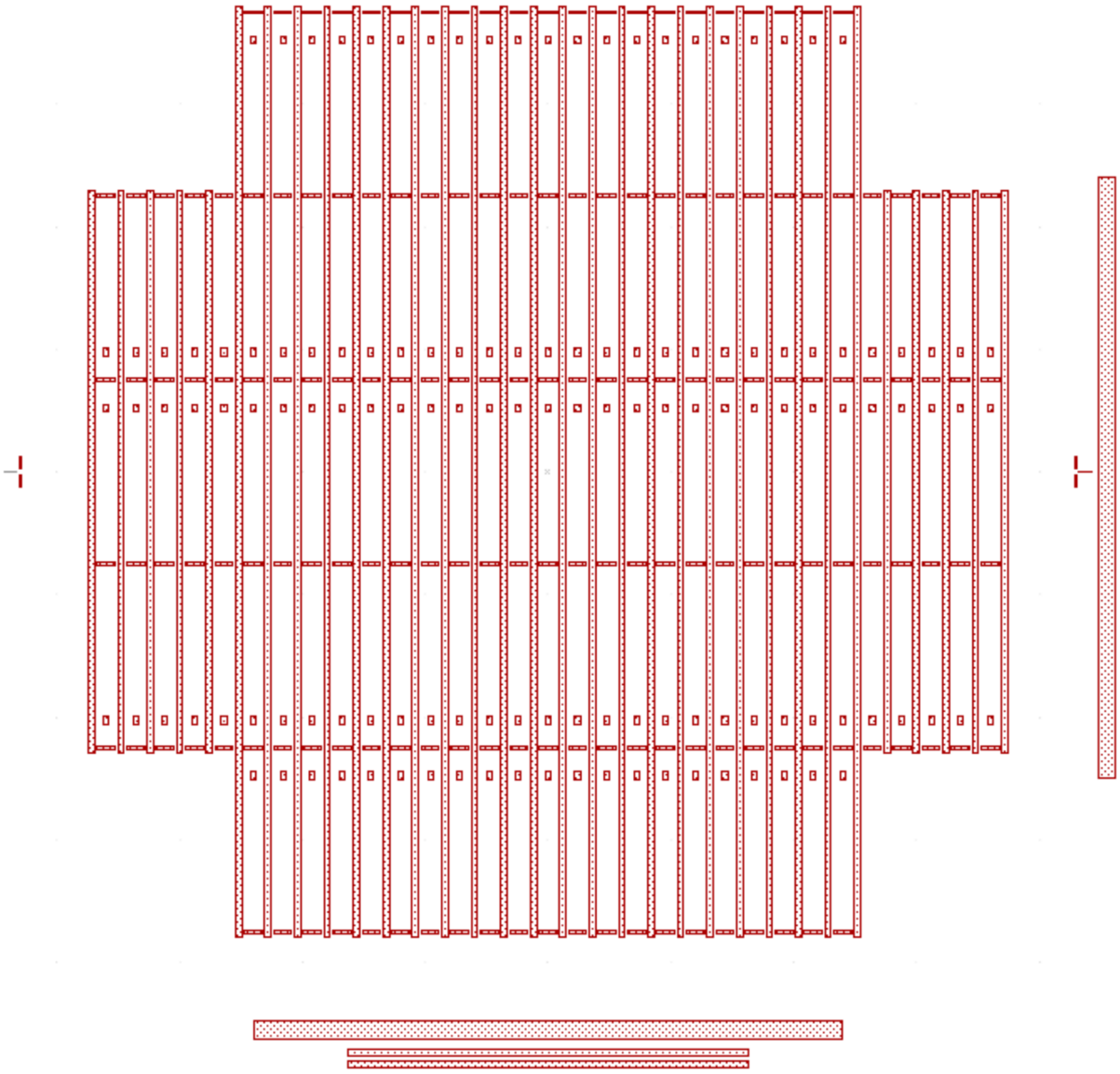

Figure B.7: Photomask for second generation top chips; has typical alignment features, additional alignment features (for aligning with the physical spacer mask), windows, and lines separating the columns of chips. Depending on which spacer method is used, this is either the first or second mask for the top wafers. It is labelled "tt_2" for 25 μm wide windows, or "tt10_2" for 10 μm wide windows. Mask features correspond to areas where Si_3N_4 will be etched.

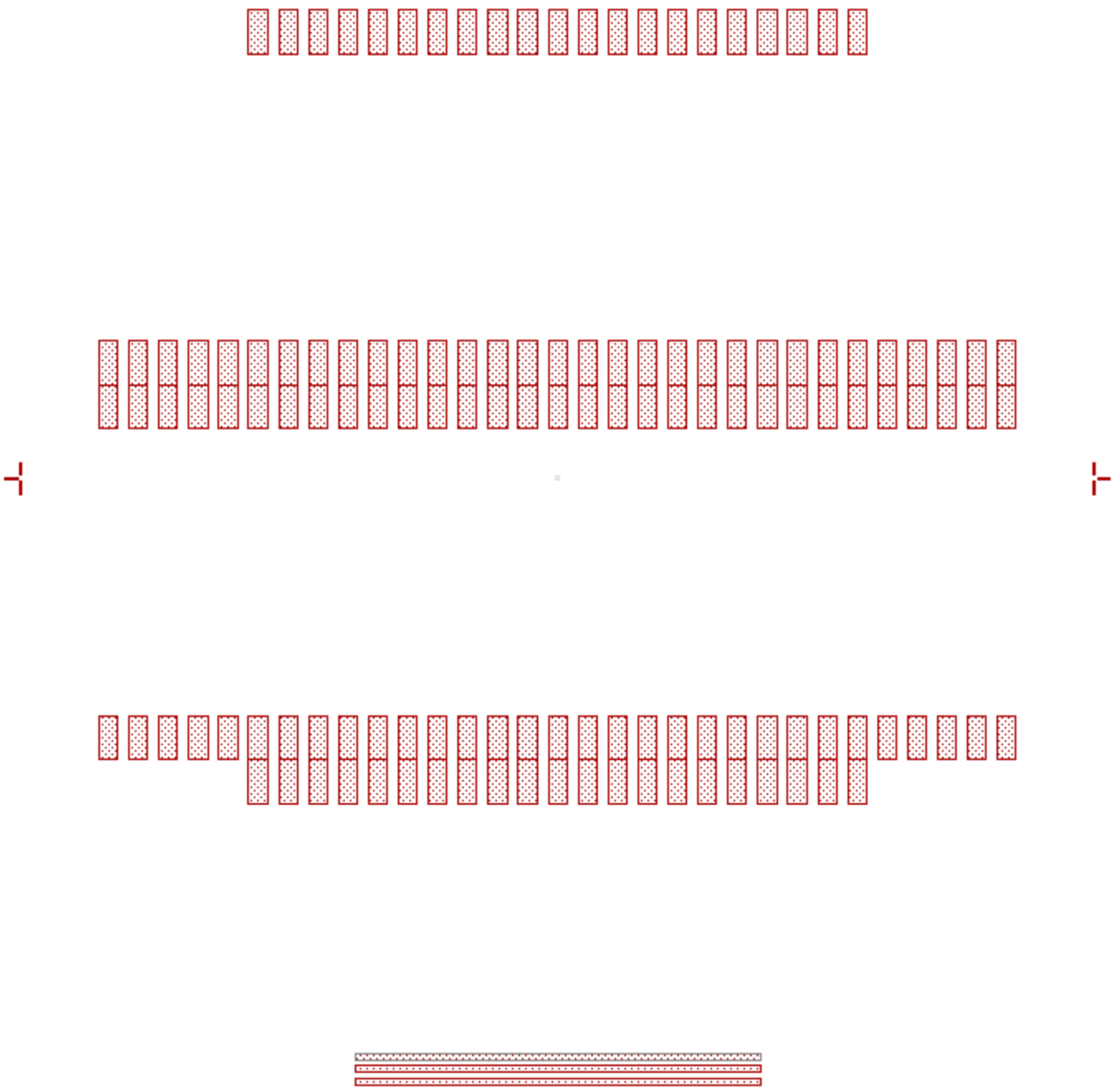

Figure B.8: Photomask for second generation top chips, with spacer etched directly into wafer; this mask is labelled "tbA_2." If this spacer method is used, this mask is used at the beginning of fabrication, with mask areas corresponding to the areas *not* encompassed by the spacer (i.e. the areas of Si to be etched).

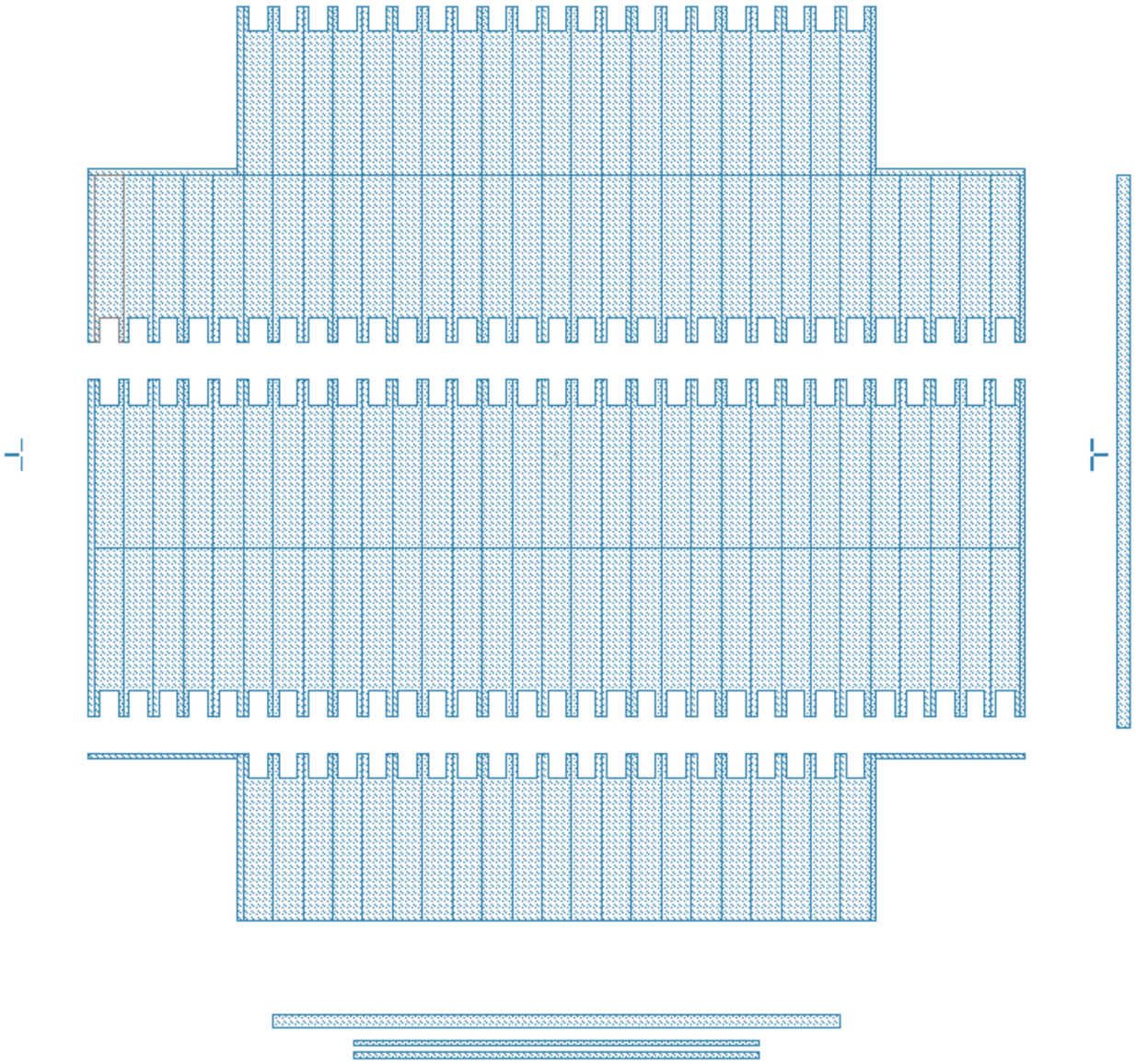

Figure B.9: Photomask for making physical mask to be used during deposition of a Ti spacer. Note the rectangular "tooth" on the centre-line of each chip: these are to mask the window and surrounding area during the deposition. Originally, the physical mask was to be etched from a bare Si wafer; however, this technique proved unsuccessful.