A Novel 8x8 CMOS Sensor Array for Thermal Compression Bonding with in-situ XYZ Force and Temperature Measurement

by
Ariel Laor

A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement of the dregree of
Masters of Applied Science
in
Mechanical Engineering

Waterloo, Ontario, Canada, 2016
© Ariel Laor 2016

Author's Declaration

I hereby declare I am the sole author of this thesis. This a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

____

Ariel Laor

Abstract

Flip chip is an electronic packaging technology that is becoming more popular in first level electronic packaging as the need for high density electrical interconnects becomes more relevant. The parallel nature of flip chip and harsh thermomechanical treatment introduces stress to the microchip and substrate. This is primarily caused by the application of high forces and mismatch in the thermal coefficient of expansion among the materials in the system. Other noise factors like misalignment, parallelism mismatch, warpage, pillar height variation, and temperature variation can weaken the bonding process. Unlike wire bonding, there is a lack of tools available for quality assessment of the flip chip process in-situ locally at the interconnect sites. There are however some existing wire bonding sensor tools which can be modified to be useful for optimization of flip chip equipment and processes.

A 4x3 mm CMOS chip is designed to record XYZ force and temperature profiles in-situ on a 2-dimensional surface during a simulated flip chip process. This was done as a low risk proof of concept to evaluate if the wire bonding tools can be adapted for a flip chip application. 95 µm square Al bond pads arranged in a square 8x8 array with 400 µm pitch have embedded piezoresistive force sensors and local top metal resistive temperature detectors. The chip is packaged with auxiliary wire bonds to deliver power and capture signals while operating under a bond head. Ball bumps 73 µm in diameter are deposited onto the sensor pads using 4N Au wire. Z sensors are calibrated using a modified automatic wire bonder. A normalized sensitivity of SN=1.39 mV/V/N is measured. Temperature sensors are calibrated at 50 °C using Kelvin probing yielding 186.94 Ω. A 3x3 mm Si wafer with Al patterning is used as a dummy pressure plate for touchdowns on the sensor chip with an experimental setup advanced process bond head. Force and temperature signals are recorded locally at each bump. 80 N force with 200 °C temperature ramps ups are applied.

Evidence of tilt and thermal expansion are detected. The prototype is demonstrated successfully and identified the most stressful stage of the bonding which occurred during thermal transients, i.e. during the short lived overshoot period of maximum stress in the force signals observed immediately after the application of heat to the system.

Acknowledgements

This work was funded by Kulicke & Soffa Industries. Special recognition and thanks is given Matt Wasserman and Tom Colosimo for their mechanical support on site in Fort Washington with their Advanced Process machine. Additional thanks for assistance with the CMOS design goes to Prof. David Nairn, Dr. Adam Neal, graduate students Stanley Ituah, and Dan Frebrowski of the ECE department at UW. Michael Hook of UW CAMJ for wire bonding assistance. Matt Scott and Nathan Nelson-Fitzpatrick of the IQC at UW for use of the Tresky Die bonder to develop the experimental process. Also thanks to CMC Microsystems for support with CMOS fabrication. Last, but not least, my supervisor Dr. Michael Mayer. He is an excellent research supervisor to have, an expert in his field, and it was a pleasure working with him on this project.

Table of Contents

Author's Declaration ii
Abstract iii
Acknowledgements iv
Table of Contents v
List of Figures vii
List of Tables x
1 Introduction & Background 1
1.1Wire Bonding 1
1.2Destructive Wire Bonding Tests 3
1.3Non Destructive & In-Situ Wire Bonding Tests 4
1.4Minioven Arrays 5
1.5Flip Chip 6
1.6Sensor Design Requirements 9
2 CMOS Design 10
2.1Previous CMOS Sensors 10
2.2Motivation for this Design 11
2.3AMS 0.35 µm CMOS 11
2.4N+ & P+ Piezoresistive Radial Stress Sensors 13
2.5Force Sensors Cross Talk 16
2.6RTD Sensor 17
2.7NAND Gate Multiplexer 18
2.8Logical Effort 20
2.9Transmission Gates 21
2.10Antenna Rules & Long Transmission Line Buffers 25
3 Experimental Setup 28
3.1Thermal Compression Bond Emulation 28
3.2Die Attach Information 29
3.3 Wire Bonding and Au Ball Bump Information 30
3.4 Pressure Plates 36
3.5Fixture Mounting & Parallelism 37
3.6Hardware Setup 39
4 Post Processing 46
4.1Raw Unparsed Data from Oscilloscope 46
4.2Sample Rates and Requirements 47
4.3Averaging and Interpolation 4 8
5 Sensor Integrity 50
5.1Force Sensor Integrity and Calibration 50
5.2Force Sensor Warpage 53
5.3RTD Sensor Integrity and Calibration 54
6 Example Results & Applications 57
6.1Tilt or Parallelism Mismatch 57
6.2Thermal Delay and Gradient 58
6.3Thermal Expansion 59
6.4True Chip Boundaries 62

6.5Over Coined Bumps “Pancaking” 62
7 Conclusions and Outlook 65
References 66

List of Figures

Figure 1 (a) ESEC 3088 automatic wire bonder in CAMJ facility. (b) Zoom of 3088 (c) Au wire spool (d) human hair vs. Au wire (e) capillary 2
Figure 2 Ultrasonic ball-wedge wire bonding cycle to create one ball-wedge bond. From (a) starting with a wire tip to (h) the breaking of a wire after the tail or wedge bond is formed. Typically the entire process is done on a heated down holder at temperatures ranging up to 200-300 °C. 2
Figure 3 (a) Shear test diagram. (b) Pull test Diagram. (c) Pull or Shear Tester available in CAMJ micro joining lab. (d) SEM cross section view of a ball bond [7]. 4
Figure 4 (a) SEM of contact resistance measurement setup. (b) Schematic view. 5
Figure 5 (a) Minioven array system. (b) A drawer showing two miniovens. 6
Figure 6 General Flip Chip Process (a) 3D view (b) 2D view 7
Figure 7 Aspects of wire bonding and flip chip. [22] 8
Figure 8 Samuel Kim's PMV1 chip layout. [3] 10
Figure 9 CMOS Sensor Layout. 64 Sensor pads, all pads with local RTD in top metal. There are 30 of the pads with Z stress sensors, 17 with X sensors and 17 with Y sensors available. 14
Figure 10 (a) Z sensor layout (b) Y sensor layout (X is identical but rotated 90°) (c) Schematic view of force sensor Wheatstone bridge (d) Z sensor radial stress (e) Y sensor radial stress [27] 15
Figure 11 N+ Sensor with bulk Si contacts. The P type bulk Si is grounded to reverse bias the P-N junctions and keep them "off". The complementary setup exists for the P diffusions. 16
Figure 12 Sensor Pad Legend or X, Y & Z force sensor locations. Includes 30 Z, 17 X, and 17 Y sensors. 64 sensor pads total, all with a local resistive temperature sensor. 17
Figure 13 (a) RTD sensor layout around the 95 µm square pad. (b) Micrograph of RTD sensors with Au bump on pad. (c) Schematic view of RTD sensor. 18
Figure 14 64 (0 to 63 inclusive) Address Locations. 6 address bits (M0-M5) Apply 3.3V binary code to address the desired pad. 19
Figure 15 3to8bit Decoder with enable bit schematic. Output is driven by an inverting buffer chain ("Invert Buffer") 19
Figure 16 Address decoder schematic. Consists of 9 3to8 decoder blocks. 20
Figure 17 Transmission gate schematic. An individual on resistance of 1024 Ω per gate was extracted. Off resistance was extracted at 10.2 MΩ 22
Figure 18 Transmission gate switch block layout for individual pad. 23
Figure 19 Model of the RTD sensor leakage. 24
Figure 20 Leakage model of PN Junction, Subthreshold and Gate leakages. 24
Figure 21 Antenna effect. a) A situation where a long metal line is attached to a gate. Charge will build up and damage the gate oxide during manufacturing. b) A short line is connected to the gate oxide which eliminates the antenna rule violations. Not enough charge builds up to cause damage. 25
Figure 22 (a) Unit length transmission line. (b) By diving the line in two equal parts with a buffer in between, the delay is effectively cut in half. 27
Figure 23 TCB emulation diagram. 29
Figure 24 (a) Hand die attach equipment. 30
Figure 25 Wire bonding diagram to used for the new TCB sensor array chip. 31
Figure 26 Gold ball bump before coining procedure with 69 µm. diameter used as emulation solder bumps in the experimental. Bonded Ball Height = 36 µm 34
Figure 27 (a) 3088 automatic ball bonder recipe. (B.) packaged TCB chip in active custom fixture

for in-situ operation on a the wire bonding machines. 34
Figure 28 Coining setup on the ESEC 3088. This setup was also used for Z force calibrations..35
Figure 29 Gold ball bump after coning procedure with a Mean Diameter = 73.16 µm, STD = 1.60 µm and bonded ball height = 29.73 µm with STD = 2.27 µm 35
Figure 30 (a) PCB V2 schematic for die attachment with conveniently routed signals. (b) The fabricated pcb with another similar sensor die attached. 36
Figure 31 (a) An earlier version of our pressure plate, CMOS chips with un-patterned Al deposited and diced to 2.9x2.9 mm. Multiple plates were stacked in early iterations of the experiment. b) The 3.5 mm x 3.5 mm x 700 µm K&S wire bonding test die with Al wire bonding test pattern that was used in the final experimental. 37
Figure 32 Tresky Die Bonder setup used in the Quantum Nano Center of Waterloo. 38
Figure 33 Corresponding Tresky Die Bonder schematic diagram showing parallelism mismatch. 38
Figure 34 K&S Advanced Process setup. 40
Figure 35 Procedure for making the sensor parallel with the metal chuck. 41
Figure 36 Steps to mount the sensor on the K&S advanced process machine. 41
Figure 37 Hardware schematic. 42
Figure 38 Sensor circuit diagrams. A general purpose AD620 instrumentation differential amplifier and a 250x custom high speed amplifier, designed by Aashish Shah and built by MME electronics technician Andy Barber are used. 43
Figure 39 UNO arduino code example. This code will poll all 64 pads, holding for 1 ms at each pad. 45
Figure 40 A photo of the DS0-3014A with raw data capture during a TCB emulation event. 46
Figure 41 Matlab plot of mux trace. The out-of-sequence increases are glitches. 47
Figure 42 A single pad measurement on pad 0. 49
Figure 43 Deformation Event from a wire bonder with a 75 µm flat tip coining capillary. A 2-stage bond profile is applied, 500mN impact, 250mN bond force 1, 500mN bond force 2. 50
Figure 44 A possible offset change explanation. (a) before coning (b) after coining. 51
Figure 45 An initial bump calibration with deformation and subsequent impacts without further deformations. 52
Figure 46 Z raw signals over a 90°C temperature sweep without force. 55
Figure 47 Y raw signals over a 90° C temperature sweep without force. 55
Figure 48 X raw signals over a 90°C temperature sweep without force. 56
Figure 49 A multi-step force profile (bold blue) overlaid on top of 30 Z force sensor signals in time. The deltas are not all at an equal magnitude, agreeing with the non-parallel contact achieved in this. Bond head and chuck are held at constant 50 °C in this event. 57
Figure 50 Tilt skews X and Y sensors. This information can also be used to detect chip tilt mismatch.The Y sensor effectively sees components of the Z force. 58
Figure 51 RTD values during a TCB emulation with bond head reaching 200°C. 59
Figure 52 Plots (a,b,c,d), show sensor & bond head vs. time for RTD sensor, Z force, X force, Y force, respectively. Corresponding spatial visualizations for time = 2.93 s (e,f,g,h), time = 3.58 s (i,j,k,l), time = 7.16 s (m,n,o,p) and time = 8.70 s (q,r,s,t). Plastic deformation region denotes sensors that may have altered force sensitivities. We may have over coined those bumps, deforming them during tilt corrections and suspect we are not making good contact in that area as shown in 60
Figure 53 SEM of Au bumps after aprox. 40 TCB emulations of up to 100 N and 200°C. Normal bumps (a,c,e). Heavily deformed bumps (b,d,f) which correspond to the denoted region in

Figure 53. The patterns on some of the bumps are from the 1-2 µm thick Al patterned pads on the pressure plate. It was in fact a reproposed wire bonding test chip with daisy chained Al pads...63
Figure 54 Spacial visualization of time when 15% change in 64 XYZ force signal was first detected. The top right region's bumps are over coined and deformed. 64

List of Tables

Table 1: Noise Factors for Flip Chip Process and Possible Causes.. 12
Table 2: Process and Library Information..13
Table 3: Estimated Switch On Resistance..22
Table 4: ESEC 3088 Parameters 33
Table 5: Parts List...44

1 Introduction & Background

1.1 Wire Bonding

Wire bonding is a popular and well established first level electronic packaging methodology commonly used to establish chip to substrate connectivity. Typically, this involves 18-100 μm diameter metal wires, which are joined to metal bond pads on microchips [1][2][3]. These wires are about 3-4 times thinner than a human hair and they are delicate, often requiring tweezers and specialized equipment to handle. The 3088 is an industrial automatic ball-wedge bonder (Figure 1). It is the wire bonder available in the CAMJ facility and was used in the research presented in this thesis. Using a computerized vision and alignment system, it is able to accurately and quickly place wire bonds to electrically connect a chip to the outside world. Figure 2a describes the wire bonding cycle. The general ball-wedge bonding process starts with a 25 micron diameter wire which is threaded into the wire bonder's bond head. This threading part of the process is not automated, a human operator will do this. The wire is carefully placed by hand through a wire feed mechanism with a tensioner, then a clamp and finally through a capillary (Figure 2a) initializing the wire position so that the automatic cycle can begin. An electrode is then used to spark the wire, called electrical flame off (EFO), which melts it forming a free air ball (Figure 2b). This ball is then bonded, typically to a top metal bond pad, usually Al on CMOS chips. The addition of force, heat and ultrasonic energy (Figure 2c) is used to form a ball bond (Figure 2d). The wire is not broken at this stage, as the machine must now loop to the package lead and create the second bond (Figure 2f). This is called a wedge or tail bond (Figure 2g).

After the second bond is made, the wire is broken, leaving wire tip similar to the one what the process started with (Figure 2h). This allows for the process to be repeated automatically along a pre-

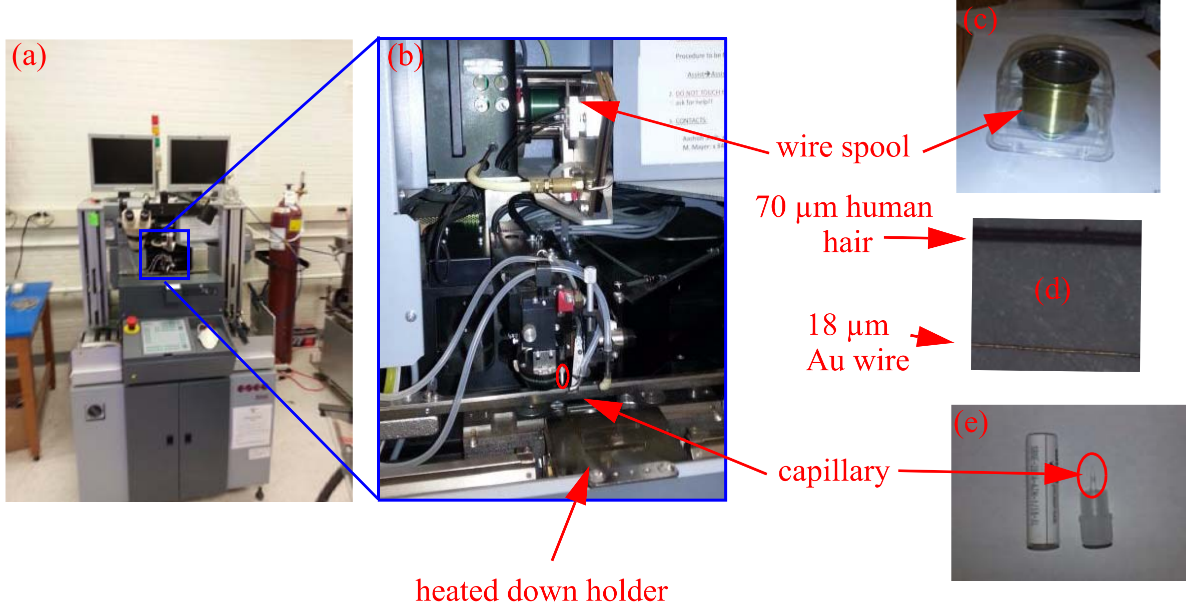


Figure 1:(a) ESEC 3088 automatic wire bonder in CAMJ facility. (b) Zoom of 3088 (c) Au wire spool (d) human hair vs. Au wire (e) capillary

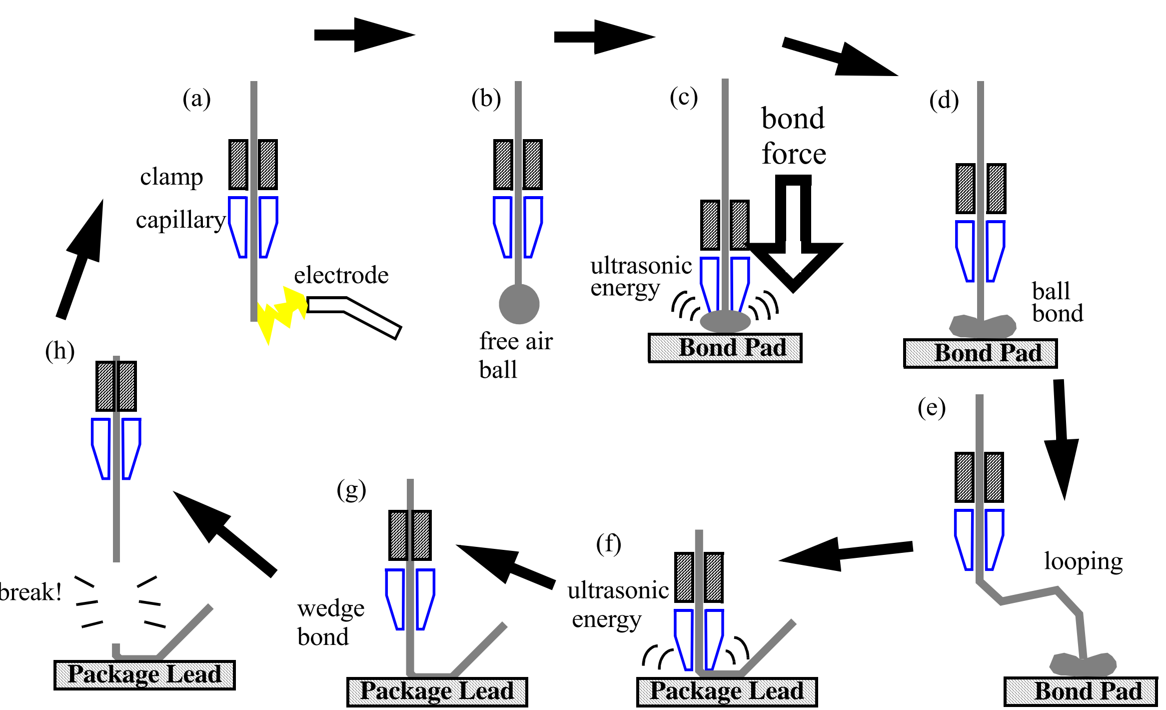


Figure 2:Ultrasonic ball-wedge wire bonding cycle to create one ball-wedge bond. From (a) starting with a wire tip to (h) the breaking of a wire after the tail or wedge bond is formed. Typically the entire process is done on a heated down holder at temperatures ranging up to 200-300 °C.

programmed wire bond layout without re-threading the wire or any human intervention. Thousands of wire bonds can be created in rapid succession this way [1][3]. These wire bonds are made sequentially, one at a time. The resulting force and thermal stress on the chip is localized to the immediate area around the bond site. It can be treated as a function of time at a single point in space.

1.2 Destructive Wire Bonding Tests

There are two categories of tests for quantifying the reliability of wire bonds, the first of which is the catagory of destructive tests. Examples are the shear test and pull test. These are well accepted in the wire bonding industry and have established JEDEC standards [4][5][6]. Shear testing involves using a shear tool to scrape a ball bond off of its pad and measure the required force (Figure 3a). Pull testing uses a hook to pull the wire and record the force necessary to break the wire or lift off the bonded ball (Figure 3b). Various pull and shear testing equipment is available in the CAMJ facility and QNC packaging lab at the University of Waterloo (Figure 3c). Another destructive test that can be used to inspect wire bonds is cross sectioning [1]. The process involves encapsulating a bonded sample in epoxy, curing it, cutting it in half near the bonds, and then grinding it down to produce a cross sectional view of the ball bumps. Samples can then be inspected with microscopy equipment like scanning electron microscopes (Figure 3d).

These destructive tests are done after the wire bonding process is completed. Only the final result of the bonding process is available for inspection. Some of the interesting process effects that happen in-situ go undetected. This gives motivation for designers to develop non-destructive methods of quantifying wire bond quality in-situ during a bonding event.

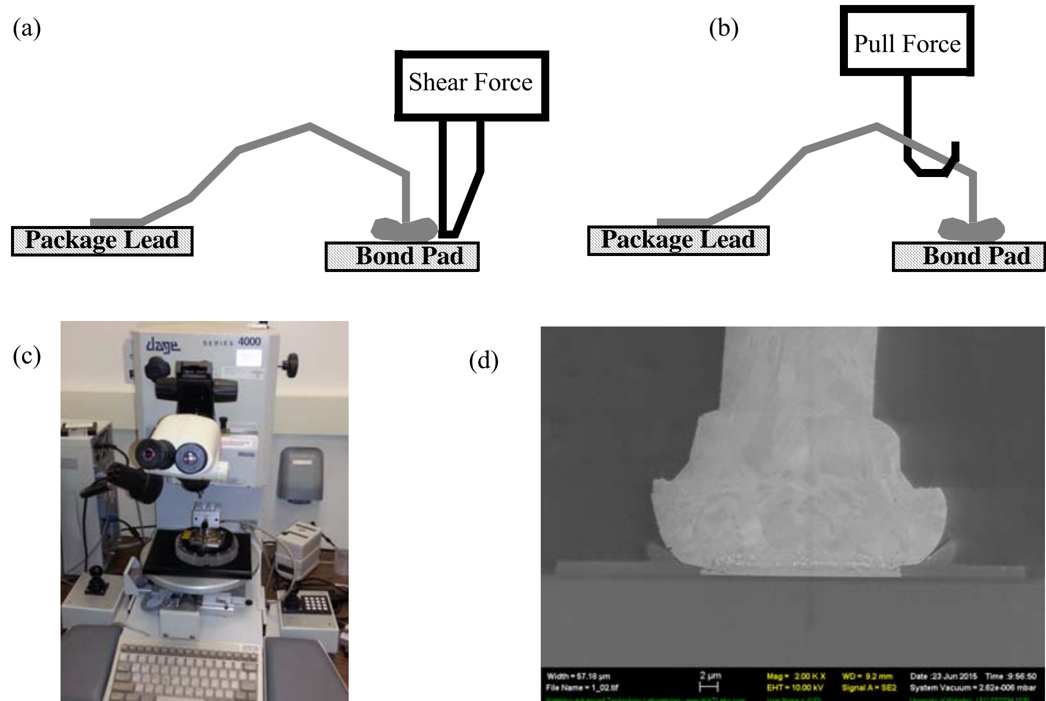


Figure 3:(a) Shear test diagram. (b) Pull test Diagram. (c) Pull or Shear Tester available in CAMJ micro joining lab. (d) SEM cross section view of a ball bond [7].

1.3 Non Destructive & In-Situ Wire Bonding Tests

The second type of tests for wire bond reliability quantification are the non-destructive tests. One such example is the use of contact resistance measurements. Figure 4 shows a wire bond configuration that allows for contact resistance measurement of ball bonds. The method is based on Kelvin probing or 4 wire measurement techniques [8][9]. In Figure 4 a defined current is passed into wires 5 and 4, and out through wires 2 and 3. Wires 1 and 6 can then be used to measure the voltage at the ball bond to pad interface. This information can be used to calculate the contact resistance without the lead resistance. The method requires specific placement of wire bonds, but it is otherwise repeatable and non-destructive. The contact resistance correlates to the wire bond quality, with weaker ball bonds exhibiting higher contact resistance. Failure can be defined when the

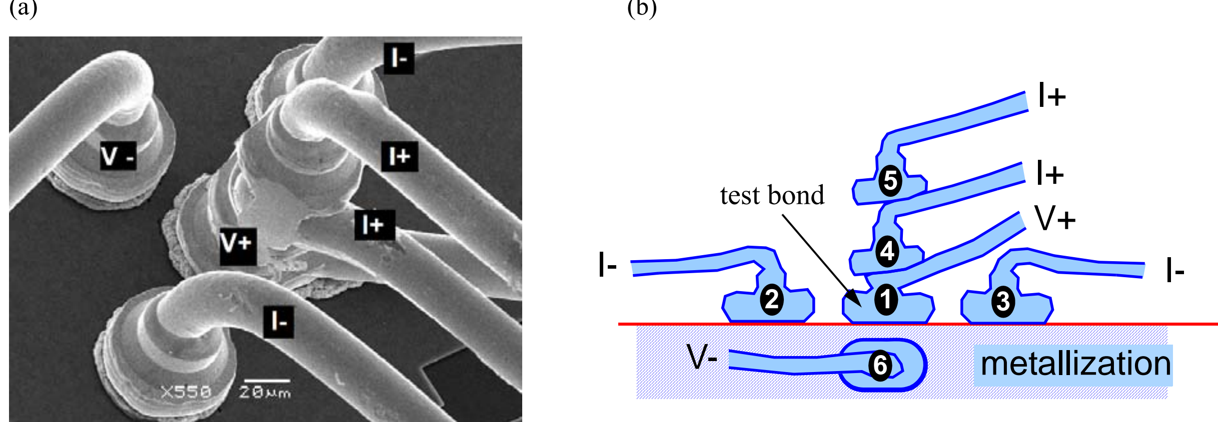


Figure 4:(a) SEM of contact resistance measurement setup. (b) Schematic view.

contact resistance increases past a defined threshold value during an accelerated aging experiment [9].

There are also some CMOS sensors [3][10][11][12] that use piezoresistive elements introduced in [15] and metal RTDs to measure the force and stress in-situ under bonding pads during a wire bond process. There are advantages of these designs over the destructive tests. The quantification of the wire bonds can be done during the actual bond process and as a continuous process. Additionally, data collection can continue after packaging is completed, which can be extended for long term reliability and aging studies.

1.4 Minioven Arrays

A mini oven tool was developed in 2010 to rapidly age active microelectronic devices [16]. It involves symmetric heating element with a Pt100 RTD symmetrically placed in a dual inline package (DIP) socket. Using control software and d-sub connectors for signal I/O, the oven can apply temperatures up to 200 °C for thousands of hours while monitoring samples. Nanovolt

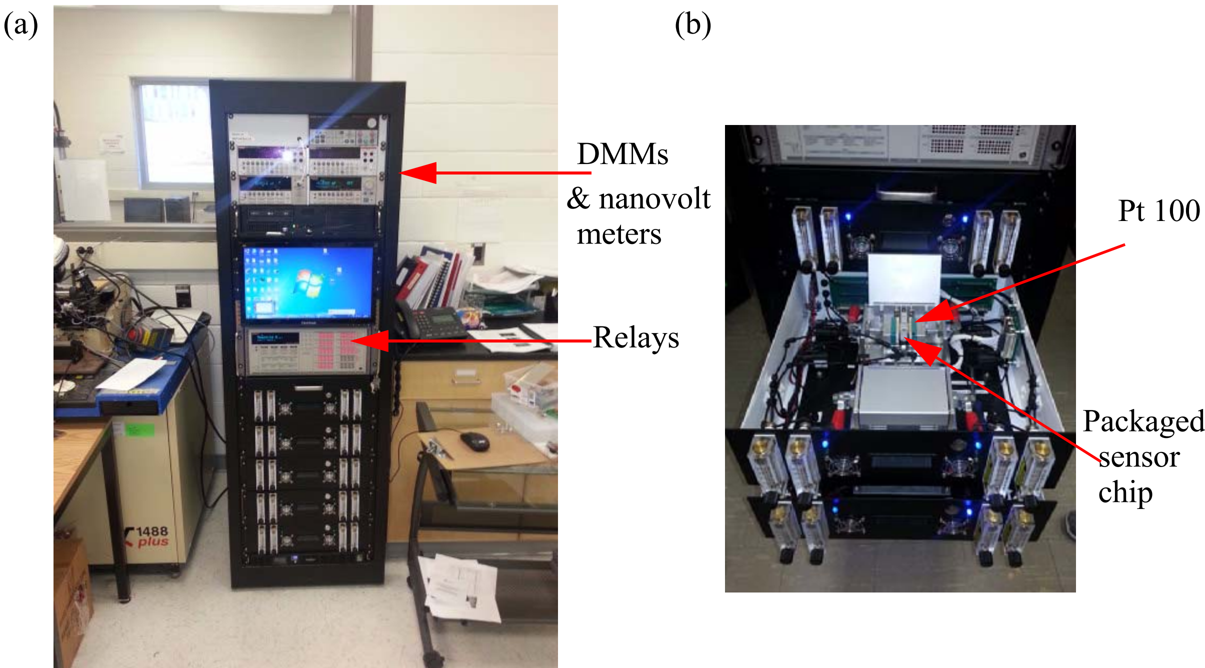


Figure 5:(a) Minioven array system. (b) A drawer showing two miniovens.

meters and other electronic measurement equipment are used for measurements as demonstrated in [10][11][17]. This tool (Figure 5) was further developed into an industrial product with an array of 10 miniovens that incorporate compressed air for rapid thermal cycling [18]. This is a very convenient setup for long term aging studies.

1.5 Flip Chip

Flip chip is an advanced IC interconnection technology. One of its variations uses Thermal Compression Bonding (TCB). The evolution of denser and smaller form factors in microelectronics introduces a desire for denser and faster first level packaging techniques [2][22]. Unlike wire bonding processes, flip chip bonding connects all chip pads to the substrate non-sequentially, in parallel (Figure 6). The original process of flip chip is called C4 collapse (Controlled Collapse Chip Connect [2]) and first appeared in the mid 1960's and was developed by IBM as an

advanced packaging process. This early process involved the deposition of high lead solder balls, typically with a height of 100 µm onto a chip's bond pads. The solder is melted to form joints (wires) to a substrate [2]. An underfill epoxy is sometimes injected between die and substrate after the bonds are formed. [2] Similar processes with Au ball bumping (sometimes called stud bumping) have also been developed in Japan during the 1980s [2]. This Au process uses temperatures in the 230 °C range or higher. More recently TCB processes are shifting towards the use of Cu pillars [19][20][21][24].

The process of flip chip generally involves the application of rapid heat (200-300 °C) and force to establish bonds. There are advantages realized in this process. Reducing die and package size and achieving denser interconnect arrays is made possible. Interconnect "wires" are physically

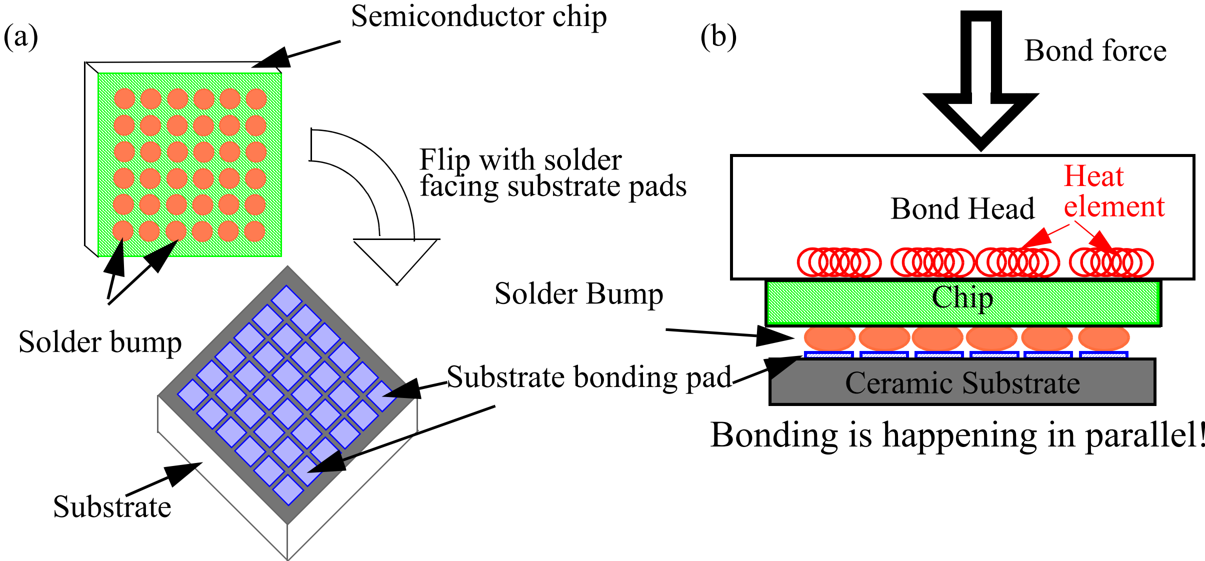


Figure 6:General Flip Chip Process (a) 3D view (b) 2D view

smaller, reducing the electrical parasitics and minimizing propagation delay which is critical to many electronic applications like microwave and radio communication systems [2]. These improvements are not without trade offs. The thermal coefficient of expansion between package and substrate can introduce thermal stress and eventual failures. The temperature profile and stress associated with the bonding process can be described as a function of time and space. When a system is rapidly heated up, the chip and substrate expand, not necessarily by the same amount or at the same rate. This can lead to the process parameters varying from bump to bump, and therefore to unsuccessful bonding. These challenges must be addressed by optimizing the process. Figure 7 highlights the major differences between flip chip and wire bonding.

.

Wire Bonding	Flip Chip
-1 dimensional, sequential bonding	-2 dimensional, parallel bonding
-Veteran process	-Denser I/O available with arrays
-Well optimized costs	-Smaller package size / form factor
-Established reliability	-Lower stress over active area
-Existing mature infrastructure	-Better power and ground distribution
	-Reduced parasitics (important for RF)
	-Device speed improvements
	-Existing developing infrastructure

Figure 7:Aspects of wire bonding and flip chip. [22]

1.6 Sensor Design Requirements

As far as this author is aware, no CMOS sensor tools for in-situ measurement of stress and temperatures currently exist for flip chip methodologies where the sensor is embedded in the system. A 4x3 mm size was selected as a low risk prototype before committing to a larger design reflective of real chips. There are two major goals for this work. The first is to identify and understand the challenges of setting up a CMOS sensor to operate within the harsh thermomechanical environment of a flip chip machine. The second is to demonstrate a working prototype and determine if any process optimizations can be extracted from the resulting data. This was planned as a proof of concept before moving forward a higher risk and more expensive 12x10 mm sensor array design in future work. At the beginning of this project it was not known what useful information this tool could give or if operation under a flip chip bond head was even possible.

The RTD sensor differs from other wire bonding senor designs previously reported from CAMJ [3][11][12]. This RTD is an absolute sensor and is intended to give absolute temperatures and is not apart of a Wheatstone bridge. This design decision was made because there is an interest in verifying that we reach defined temperatures of interest during the process.

The Force sensor differ from the CAMJ wire bonding senor tools as well. In this situation ball bumps are used instead of actual wire bonds. The new sensors are exposed to harsher thermomechanical stress compared to their wire bonding predecessors.

2 CMOS Design

2.1 Previous CMOS Sensors

Part of this work is based on Samuel Kim's [3] and Michael McCracken's [11] previous chip designs. Samuel Kim's "PM Version 1 chip" (PMV1) for wire bonding applications is available in the CAMJ facility at the University of Waterloo. This design (Figure 8) consists of 56 standard library bond pads (provided with the AMS kit) with embedded piezoresistive force elements. There are also contact resistance traces available at each pad to setup double ball bonds for four-wire measurement configurations. A multiplexer is used to select pads onto the data bus. In addition there is a single top metal RTD located in the bottom left region of the chip. This RTD element is not switched on the multiplexer. Auxiliary bond pads around the left and right sides of the chip are available to deliver power and get signal to and from the chip.

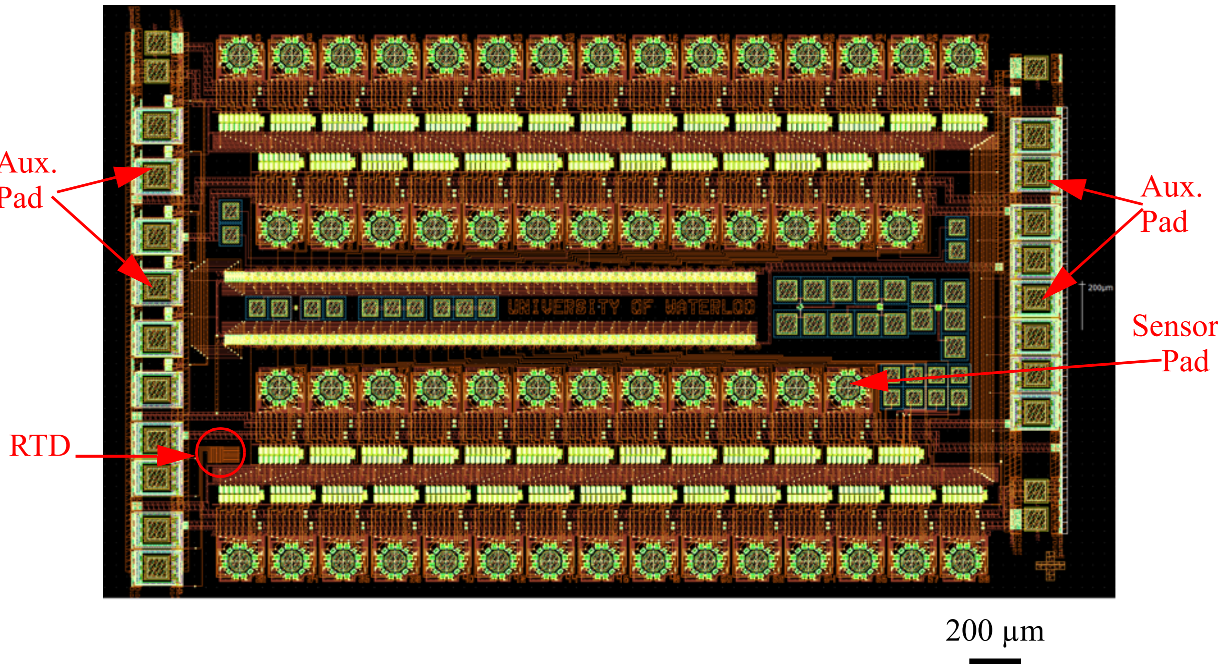


Figure 8:Samuel Kim's PMV1 chip layout. [3]

PMV1 was designed for wire bonding applications. The sensor pitch and locations were implemented with a 1 dimensional process in mind. The auxiliary bond pads at the chip's sides and make the layout unsuitable for a flip-chip like process.

2.2 Motivation for this Design

The design in this thesis was motivated by a desire to take the 1-dimensional wire bonding sensor tools and re-implement them to include compatibility with a 2-dimensional process like flip chip. Table 1. introduces some of the noise factors for a flip chip process and possible causes. The goal of the new TCB design is to create a proof of concept prototype that combines an array of RTDs and wire bonding force sensors to detect and quantify the noise factors in-situ.

2.3 AMS 0.35 µm CMOS

The AMS 0.35 µm process available through CMC is selected to build a prototype. Table 2 gives information about the process and standard libraries used in the TCB sensor design. This was one of the older and more cost effective processes available through CMC's academic runs. A 4x3mm area was requested for the prototype design. The importance of the physical location of bond pads had to be considered in this design. Additional clarification about the research objective was needed to justify the large area to CMC before the academic area was granted for the mask.

The standard library's 95 µm square Al pad was selected as the standard test pad for the TCB sensor array design. These pads consist of a top metal area, that is slightly larger than 95 µm, but only has 95 µm x 95 µm square pad openings. Figure 9 shows the submitted layout. The sensor pads were arranged in an 8x8 array with a 400 µm pitch. The sensor pads occupy a 3 mm x 3 mm square area of the mask allocation. The sensor pads are numbered from 0 to 63, starting from the

Table 1: Noise Factors for Flip Chip Process and Possible Causes.

Description of Noise Factor	Illustration	Possible Causes
1) **Misalignment** between chip and sub-strate.	chip substrate	-equipment
2) Chip and substrate do not have **parallelism**.	flip chip substrate	-equipment -chip -substrate
3) Chip and/or substrate exhibit **warping**.	chip substrate	-chip -substrate -temperature gradients
4) **Pillar height variation.**	chip substrate	-chip
5) **Temperature Variation** during bonding.	Bond Head hot hotter hot substrate	-heating elements -any of the other noise factors (1)-(4)

Table 2: Process and Library Information

Process	**AMS 0.35 µm C35C4B3** through CMC Additional info available at: http://www.cmc.ca/en/Help/Licensing/AMSDesignKits.aspx
Digital Library	**3.3V "CORELB"** INV<X>, NAND4<X>
Primitive Library	"**PRIMLIB**" nmos4, pmos4, rdiffn3, rdiffp3
Digital IO PAD Library	**"IOLIB_4M"** ICP, VDD3ALLP, GND3ALLP
Analog IO PAD Library	**"IOLIB_ANA_4M"** APRIO50P
Orientation	**<100>**
Operational Voltage	3.3 V (Maximum VGS / VDS = 3.6 V)
# of metals	4 metals

top left corner and progressing from left to right and then top to bottom. The remaining 3 mm x 1 mm area on the left is for digital logic and auxiliary wire bond pads. The bond pads are deliberately placed on only 1 edge of the chip, ensuring that they do not interfere with a flip chip process.

2.4 N+ & P+ Piezoresistive Radial Stress Sensors

This type of force sensor design is first introduced in [13][14] and are discussed in detail in J. Schwizer's book [15]. They consist of specially arranged piezoresistive n+ and p+ diffusions which are used in CMOS processes. These are in fact the same active diffusions available for use to create transistors and other CMOS devices, which makes the fabrication process a convenient one-stage process; one foundry produces the entire sensor chip.

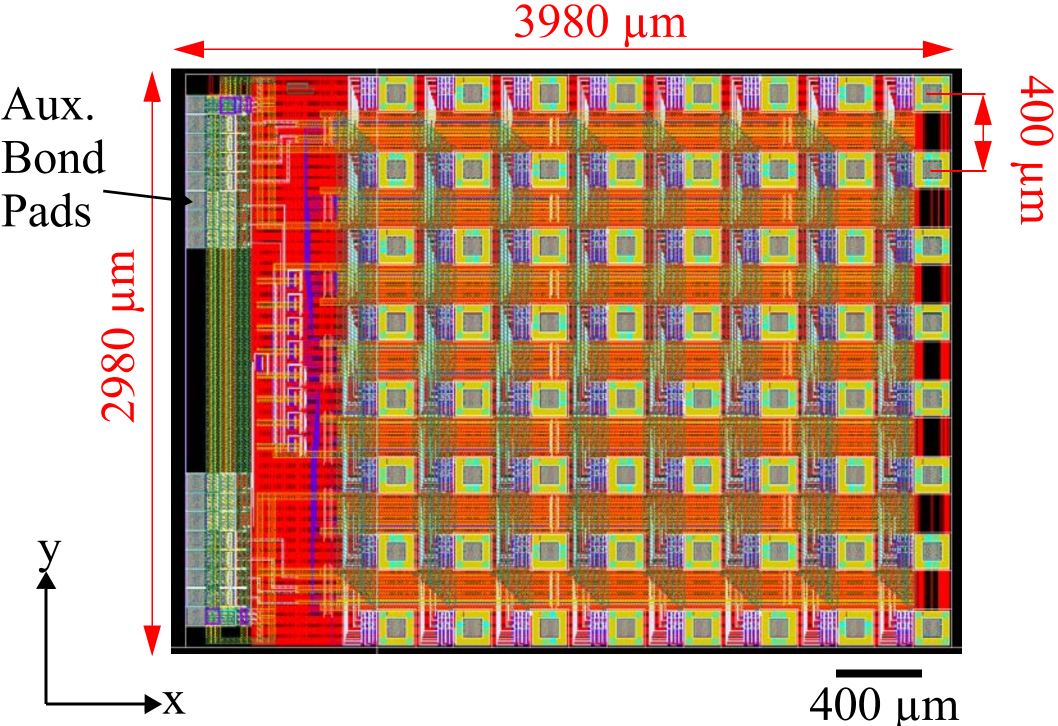


Figure 9:CMOS Sensor Layout. 64 Sensor pads, all pads with local RTD in top metal. There are 30 of the pads with Z stress sensors, 17 with X sensors and 17 with Y sensors available.

Piezoresistivity is defined as change in electrical resistance caused by mechanical stress fields. Schwizer's book [15] discusses how to sensitize the diffusion element along a specified axis by arranging them in a Wheatstone bridge configuration. Figure 10a shows the Z sensor case, where R_a and R_d are rotated 90° with respect to opposing elements R_b and R_c. Figure 10b shows the Y sensor case, with opposing elements having 180° of rotation. Figure 10c shows the schematic representation of the Wheatstone bridge. Force applied at the enclosed bond pad induces a piezoresistive change at the elements which the system translates to a voltage difference between $+V_F$ and $-V_F$. Global changes in temperature are effectively muted from the voltage signal by this con-

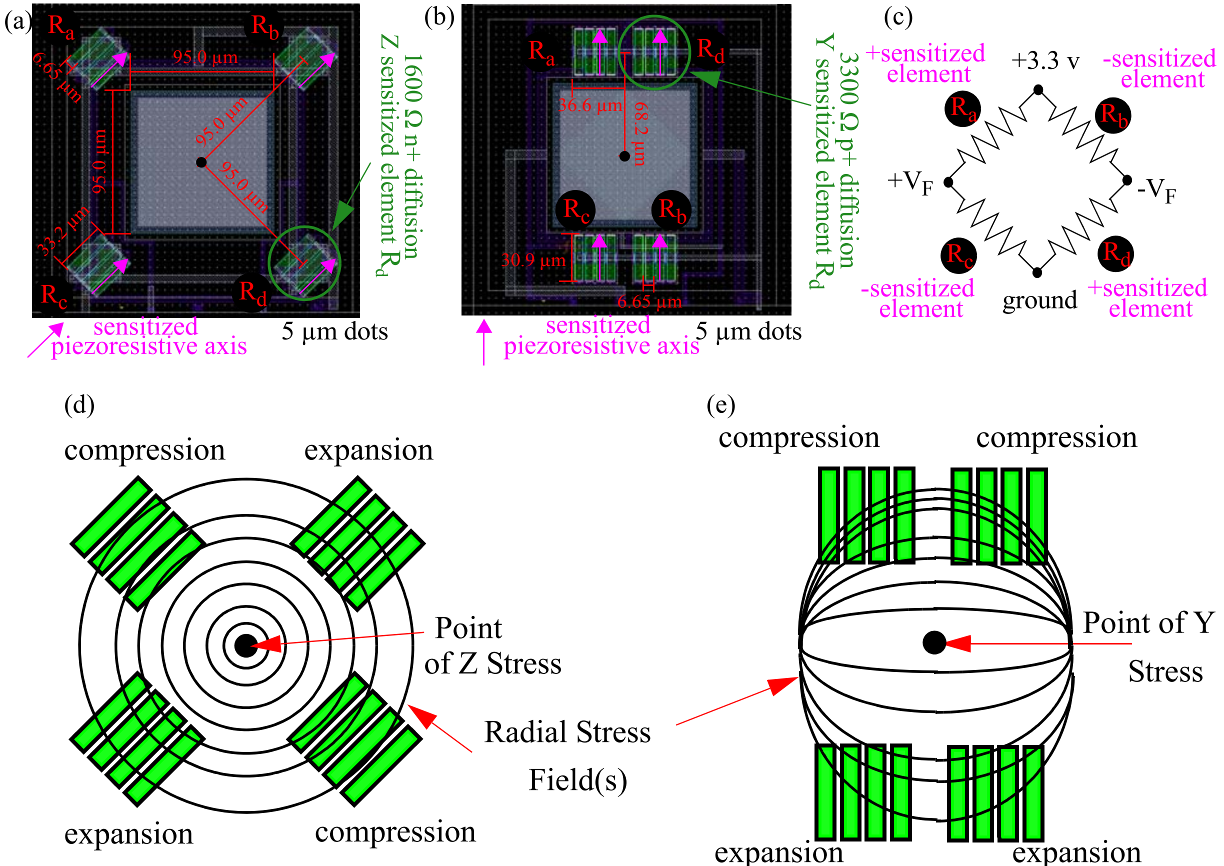


Figure 10:(a) Z sensor layout (b) Y sensor layout (X is identical but rotated 90°) (c) Schematic view of force sensor Wheatstone bridge (d) Z sensor radial stress (e) Y sensor radial stress [27]

figuration. This type of arrangement also sensitizes each bridge to only one of the X Y or Z force changes.

For the Z sensor, n+ diffusions are embedded around a standard library 95 CMOS bond pad. A consequence of depositing n+ diffusions in the p-type bulk Si is the creation of PN junctions. These diodes are undesired parasitics, and must be biased in the off state for successful operation, and the bulk Si is therefore held at the lowest available potential, ground. This ensures that these

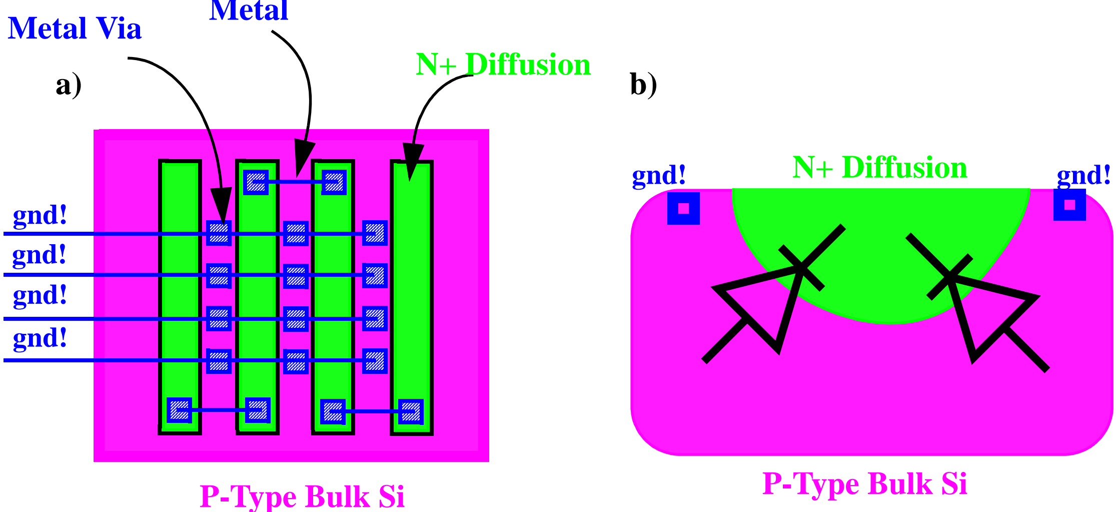


Figure 11:N+ Sensor with bulk Si contacts. The P type bulk Si is grounded to reverse bias the P-N junctions and keep them “off”. The complementary setup exists for the P diffusions.

devices remain reverse biased, and off (Figure 11). The complementary situation occurs with the p-type elements which sit inside an n-well. These are handled in a complementary fashion, holding PNP transistor’s n-well at VDD, the highest available potential. This will reverse bias it so that it remains off. For the final design, Cadence extracts the Z elements at 1600 Ω each at room temperature. For the X and Y sensors, p+ diffusion is used and extracted as 3300 Ω each. Figure 12 gives a force sensor legend for each pad location on chip.

2.5 Force Sensors Cross Talk

The design of the force sensors and their proximity to adjacent force sensors could potentially create cross talk effects. This is undesirable during a high force, 2-dimensional process like flip chip. Before the layout was finalized, the PMV1 chip was tested. A wire bonder with a flat tip capillary was used to apply up to 1500 mN of force onto a ball bumped pad. The neighboring pads were scanned for force signal changes. It was determined experimentally that these pads do not see force events at their neighbors. Schwizer’s book offer’s a possible explanation. Using a finite ele-

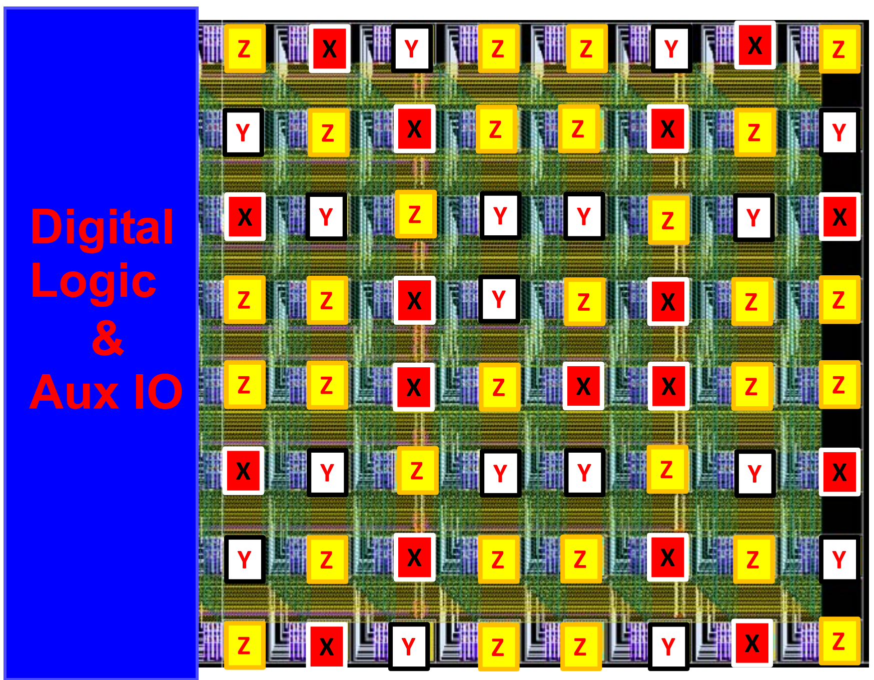


Figure 12:Sensor Pad Legend or X, Y & Z force sensor locations. Includes 30 Z, 17 X, and 17 Y sensors. 64 sensor pads total, all with a local resistive temperature sensor.

ment model (FEM), and applying force at the center point of a pad, it was shown the resulting stress field becomes negligible with radial distance increasing beyond less than 40 µm. Schwizer reported a 40 µm increase in radial distance yielded an order of magnitude decrease in the stress field's magnitude for X and Y stresses, and four orders of magnitude decrease for the Z stress [15]. PMV1 and the new TCB design are similar and have experimentally shown the same behavior.

2.6 RTD Sensor

Each of the 64 test pads has its own local RTD sensor. The sensor consists of a serpentine pattern of 2.5 µm wide top metal (Figure 13). The metal thickness is rated to carry a maximum of 2.5 mA of current. This current limit minimizes self heating in the RTD sensor. An external current source can be used to bias the RTD, and a volt meter can measure the voltage drop across it. The result is

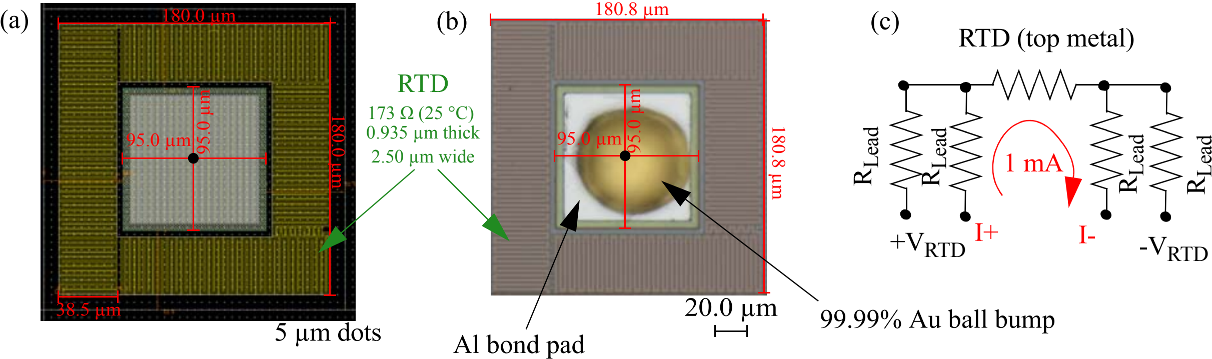


Figure 13:(a) RTD sensor layout around the 95 µm square pad. (b) Micrograph of RTD sensors with Au bump on pad. (c) Schematic view of RTD sensor.

a Kelvin probe or four wire setup which gives an accurate reading of the metal's resistance. From references [1][8][23] it is shown that the resistance of a metal is a linear function of temperature. The RTD's resistance therefore correlates to the average temperature in the 180 µm square area surrounding the bond pad.

2.7 NAND Gate Multiplexer

There are 64 sensor pads available on the TCB sensor chip. The pads can be selected onto the data bus with the onchip multiplexer. Figure 14 shows the location of the address bit auxiliary pads and how to select sensor pads with 3.3 volt digital control signals.

The digital control circuitry is made up of minimum size, standard library, 4 input NAND gates. They preform logical NAND ("Not" "And") operations on 3 inputs and an additional enable signal. Figure 15 shows a schematic view of a single 3 to 8 NAND decoder block. The input signals, A,B,C and Enable are first inverted so that their compliments are made available to the system.

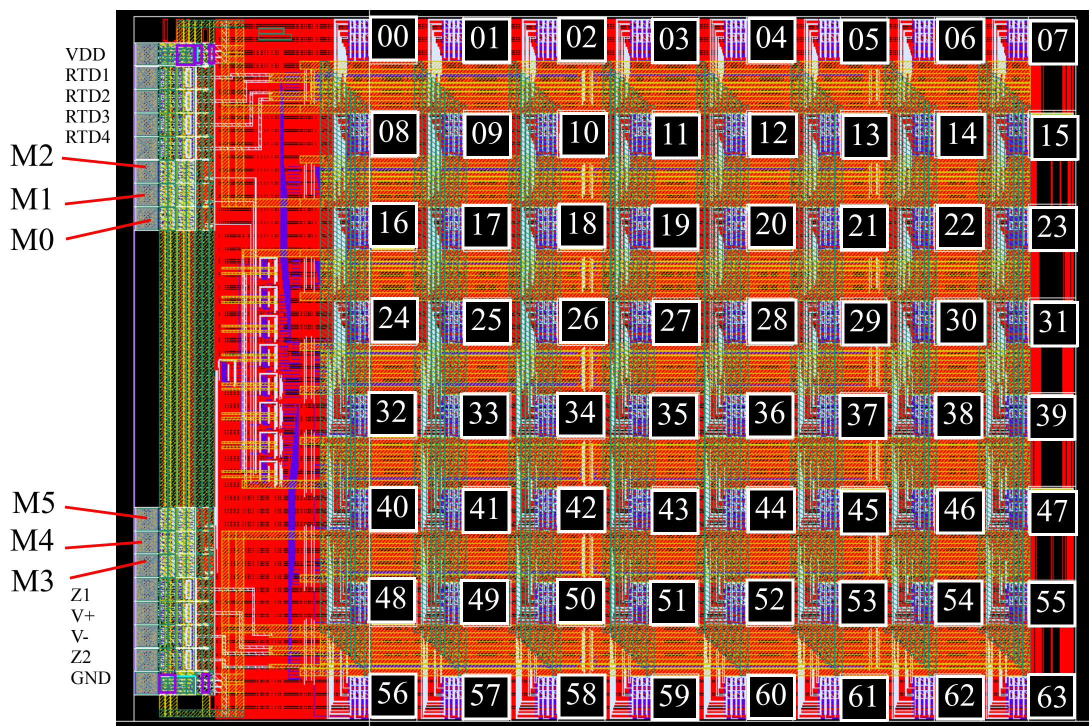


Figure 14:64 (0 to 63 inclusive) Address Locations. 6 address bits (M0-M5) Apply 3.3V binary code to address the desired pad.

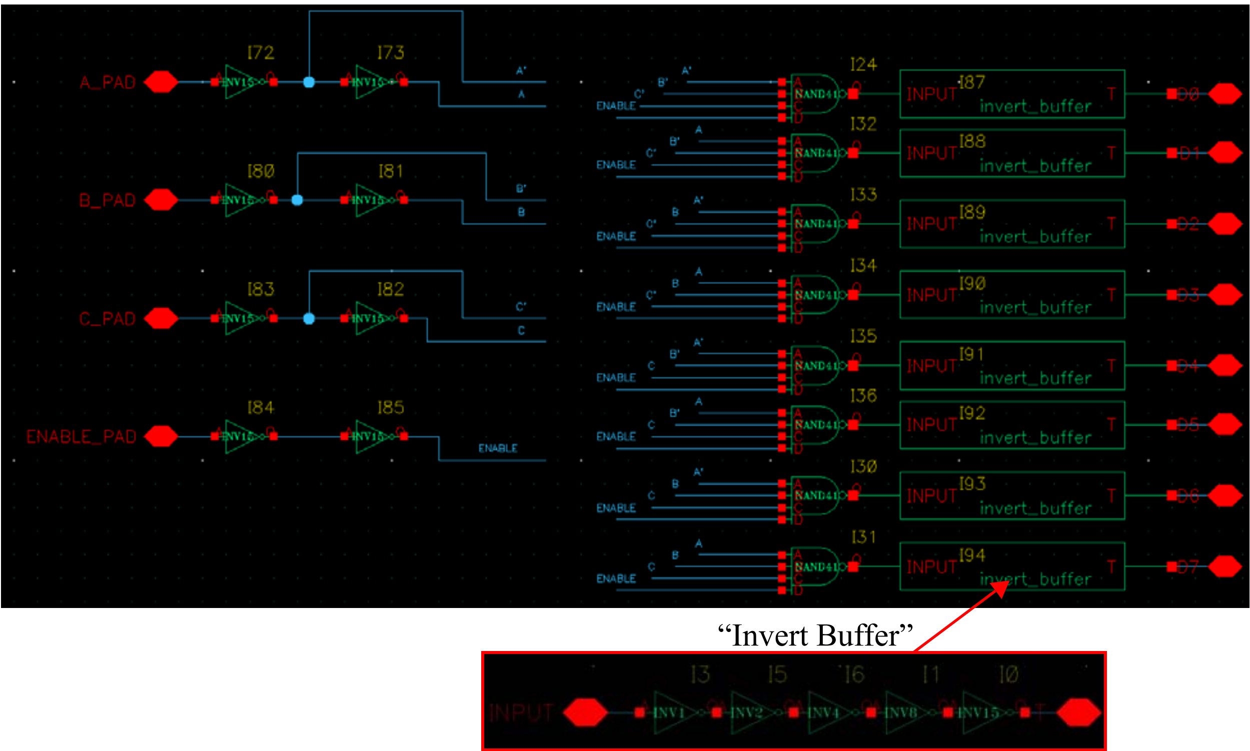


Figure 15:3to8bit Decoder with enable bit schematic. Output is driven by an inverting buffer chain (“Invert Buffer”)

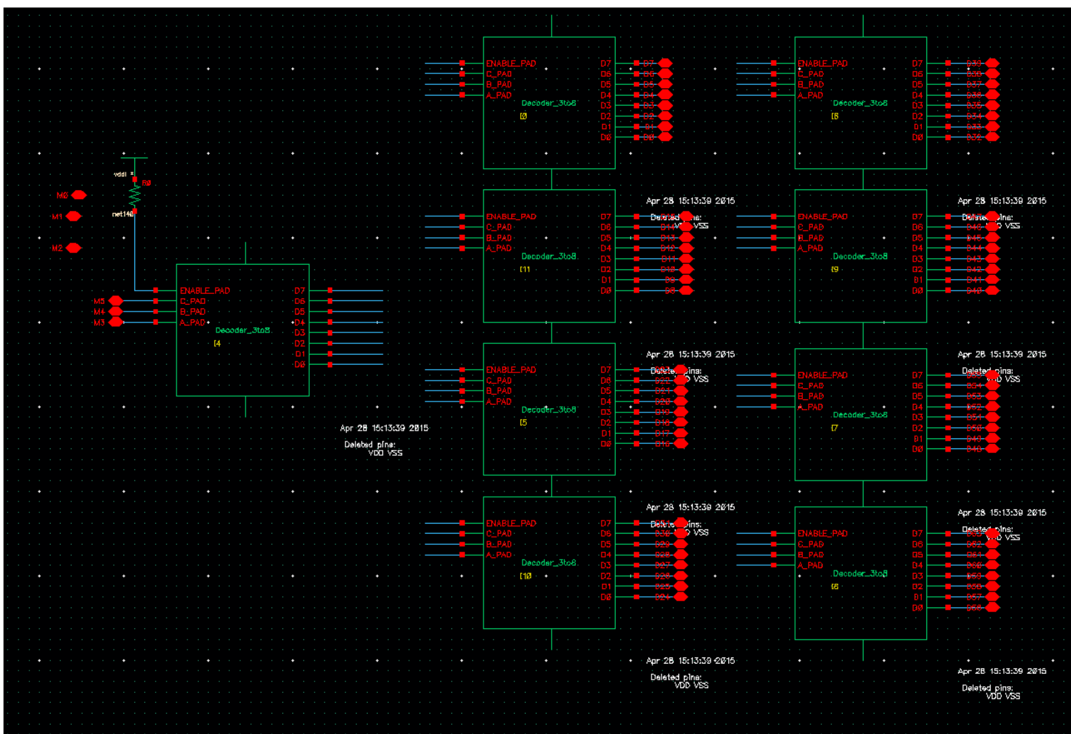


Figure 16:Address decoder schematic. Consists of 9 3to8 decoder blocks.

The signals are then passed through 8 of the 4 input NAND gates passing 8 control signals to the output buffers. Figure 16 gives a schematic view of 9 decoder blocks linked together, creating for a 6 to 64 multiplexer. The digital layout and routing was done by hand without the use of a synthesis tool.

2.8 Logical Effort

The standard libraries have NAND and inverter logical gates available in multiple standard sizes. For example, there is a 1x NAND gate, and a 15x NAND gate, both of which preform the same logical operation, but with the latter being 15x larger. The gate size affects the magnitude of current which the gate can drive, sometimes called drive strength. Bigger logic gates have more drive strength at the cost of increased gate capacitance [26]. This means that these larger gates can drive a circuit faster, but they themselves take longer to drive. The digital multiplexer was implemented

with the minimum size NAND gates. This minimized the area consumed by the digital logic. However, this also introduced a problem, driving the 3000-4000 μm transmission lines across the chip with minimum size gates was not optimized for speed and slows down operation.

The solution is to use buffer stages between the logic output and load. The buffer stage uses the concept of logical effort [26] to optimize the delays. The propagation delay of the logic gates can be decreased by looking at the ratio of input capacitance to output capacitance and finding the input capacitance of the next stage of logic that minimizes the overall propagation delay of the system. Reference [26] discusses how fan out or logical effort is best optimized with successive logic stages increasing by a factor near four. In the TCB design, logical effort was optimized, though a compromise was found between the available area, speed requirements and most importantly, what standard library device sizes were readily available. Consequently, the exact ratio of four times was not realized. In future designs a full custom implementation may produce further optimized multiplexer performance at the cost significant time investment and complexity. The performance gains of logical effort optimizations have diminishing returns [26].

2.9 Transmission Gates

Transmission gates [26] are used as switches at the sensor pads. A transmission gate schematic is given Figure 17. It consists of a NMOS and PMOS transistor with their drains and sources shorted respectively. The complimentary gates are attached to complimentary toggle signals. The result, is a logical switch. When toggle is high, the transmission gate is on and passes signal. When toggle is low, the transmission gate is off. Several transmission gates are employed in parallel (Figure 18) at each pad to switch the various signals. Table 3 gives the extracted spice model [26]

estimations of the on resistance for each sensor channel. The gates were sized to fit inside the available area under the pad sensors. An 180 µm x 180 µm area of space was left below each pad sensors for the switch circuitry.

An idealized room temperature leakage model of the system during operation is given in Figure 19. The “off” gates have an extracted parasitic resistance of 10.2 MΩ in parallel 63 times

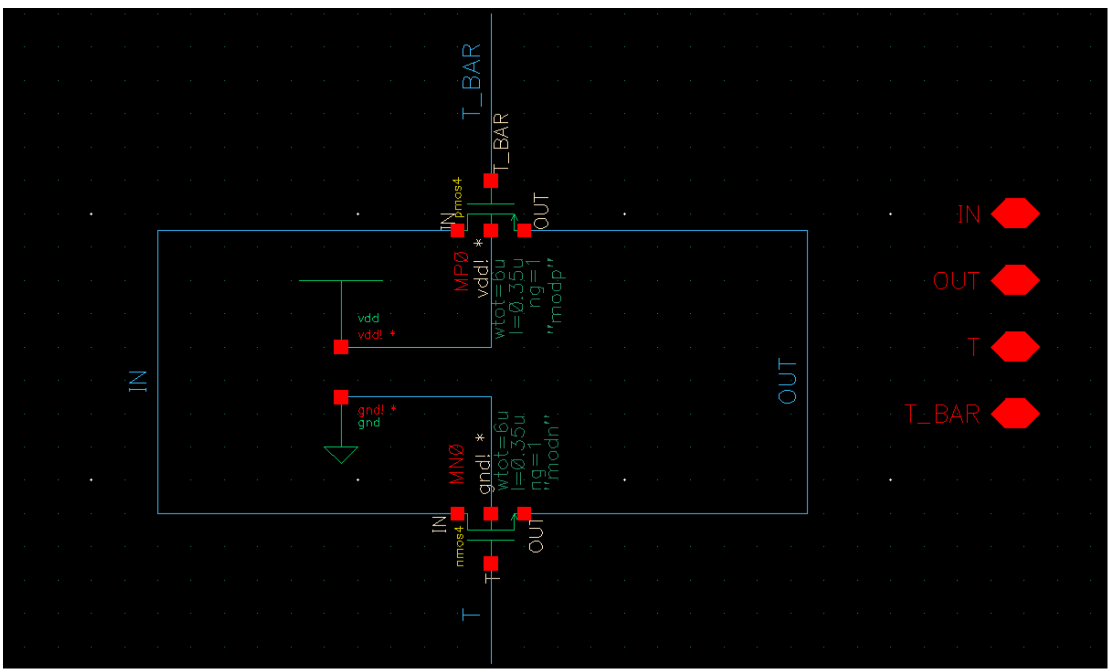


Figure 17:Transmission gate schematic. An individual on resistance of 1024 Ω per gate was extracted. Off resistance was extracted at 10.2 MΩ

Table 3: Estimated Switch On Resistance

Signal	On Resistance
X/Y/Z V+/V-	16 Transmission Gates: 64 Ω
Z1/Z2	8 Transmission Gates: 128 Ω
RTD Current (1&4)	4 Transmission Gates: 256 Ω
RTD Voltage (2&3)	1 Transmission Gates: 1024 Ω

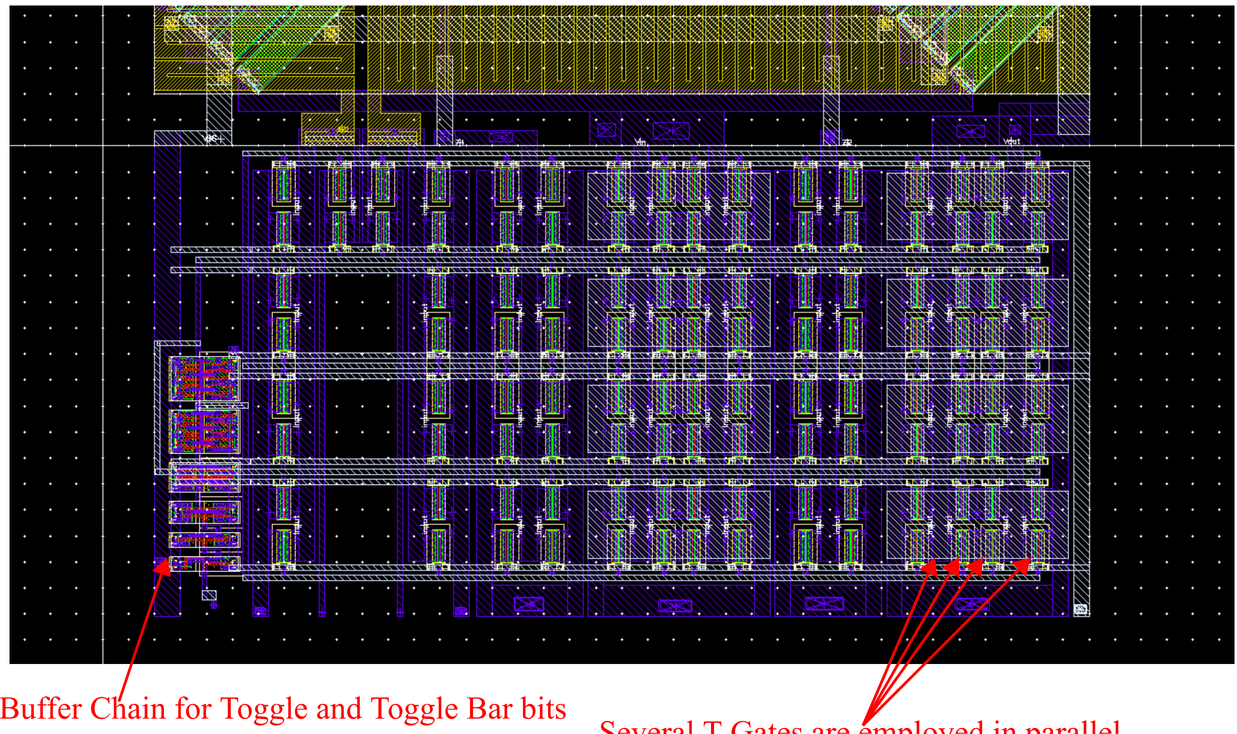


Figure 18:Transmission gate switch block layout for individual pad.

giving 0.1619 MΩ. The ideal subthreshold currents are expected to be more than 4 order of magnitude smaller than the “on” current. However in reality, the leakage is worsened by parasitic leakage effects like subthreshold conduction, gate oxide leakage and junction leakage [6]. Figure 20 shows the location of these effects in an NPN MOSFET. Given a fixed geometry, these parasitics generally increase with temperature [26]. The linear models provided with the AMS kit are only valid in simulation up to 120 °C after which the parasitics start to exhibit non-linear behavior. Future designs should include test structures that allow for leakage measurements and quantification.

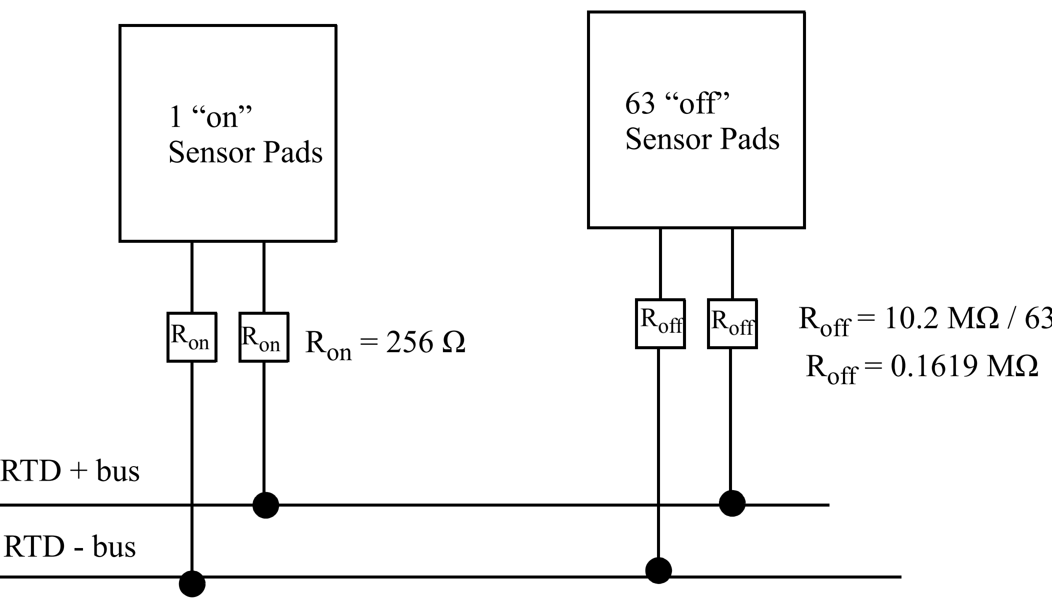


Figure 19:Model of the RTD sensor leakage.

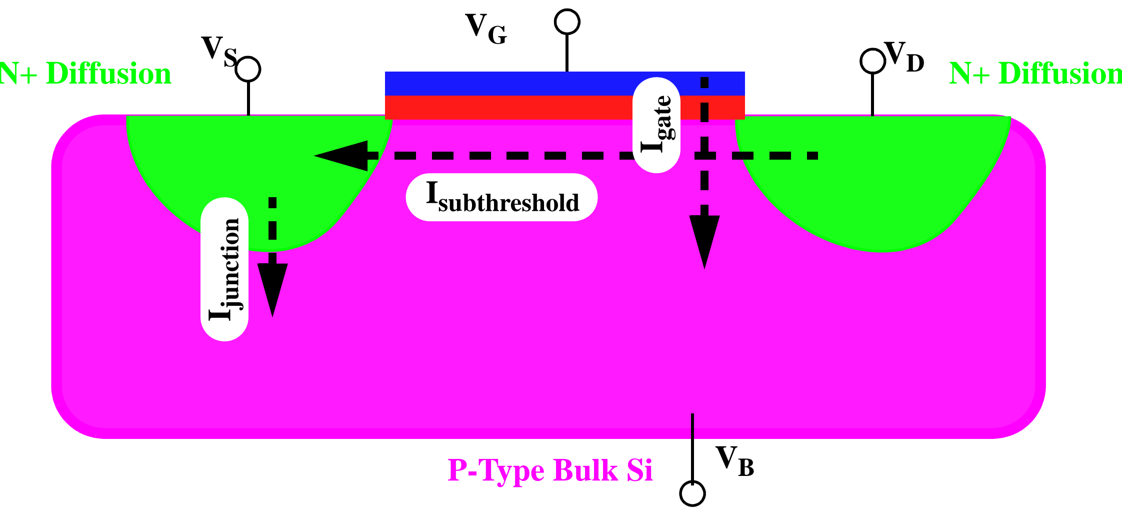


Figure 20:Leakage model of PN Junction, Subthreshold and Gate leakages.

2.10 Antenna Rules & Long Transmission Line Buffers

The large area scale of the TCB design introduces some challenges specific to large area circuit design. The first of which is the need for large transmission lines which can violate the antenna design rules. The metal lines in a CMOS process are deposited after the semiconductor diffusions are put in place. Typically this metal is deposited with a sputtering process during which it can build up charge. This may damage a CMOS gate oxide if too much charge builds up along the metal line during the deposition process with nowhere to dissipate [26]. Figure 21 shows how to

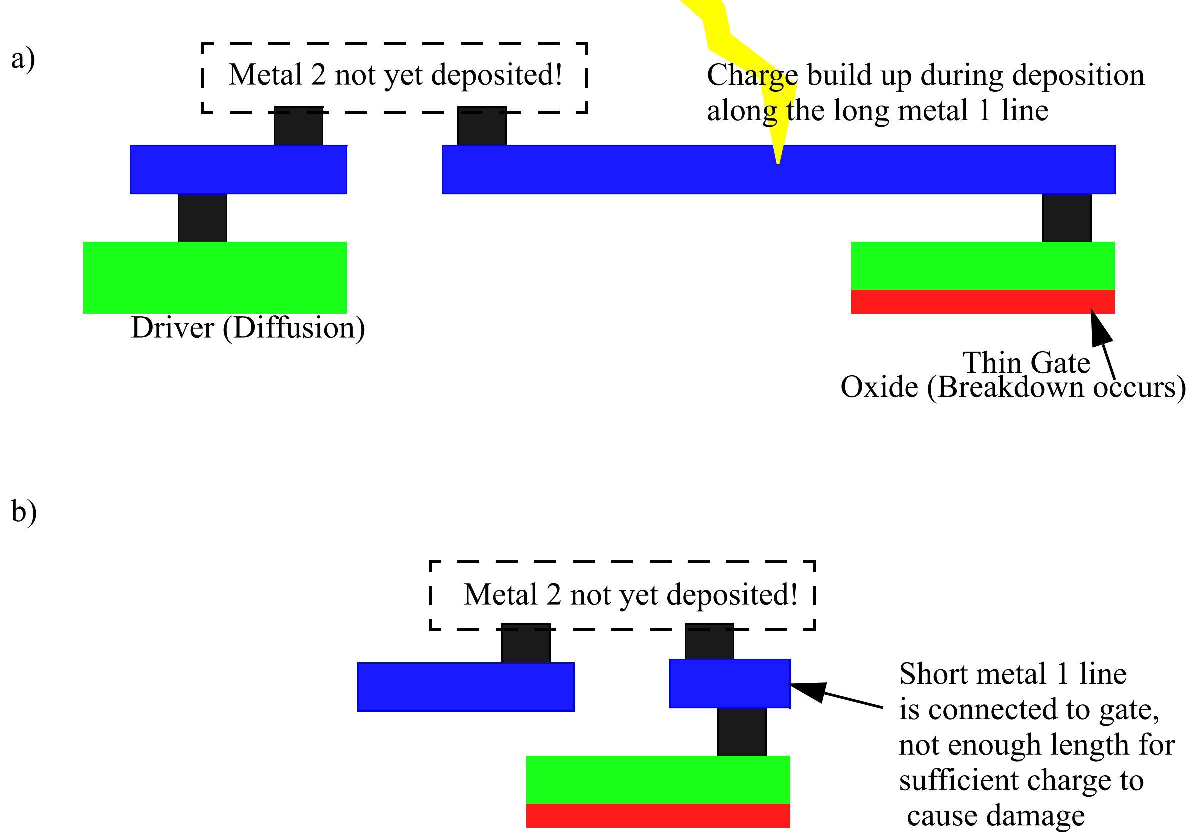


Figure 21:Antenna effect. a) A situation where a long metal line is attached to a gate. Charge will build up and damage the gate oxide during manufacturing. b) A short line is connected to the gate oxide which eliminates the antenna rule violations. Not enough charge builds up to cause damage.

limit the length of metal lines connected to active gates. This technique can be used to avoid antenna rule violations.

Another challenge with large area CMOS is the propagation delay of transmission lines. The delay is a function of the resistance and capacitance, or an RC time constant [26]. The transmission line thickness is fixed by the CMOS process that is selected. The line width and length are the only components designers can vary. Width is left up to the designer, but there is a caveat. Making a line wider will reduce line resistance but also increase the capacitance by an equal factor. The RC delay effectively remains the same, regardless of the line width. Therefore a width sufficient to carry the expected current levels was selected in the TCB design. The only other transmission line parameter a designer can play with is length. It is desirable to minimize transmission line length, as length increases the resistance and capacitance of the line. The TCB design strived to minimize the transmission line length for this reason. Another helpful technique was to divide long transmission lines into multiple sections. RC delay grows quadratically with transmission line length. Therefore, the total delay of two half length transmission lines is effectively half that of single unit length transmission line (Figure 22). Using repeater buffers costs a relatively small amount of area, delay and power compared to the improvement in RC delay.

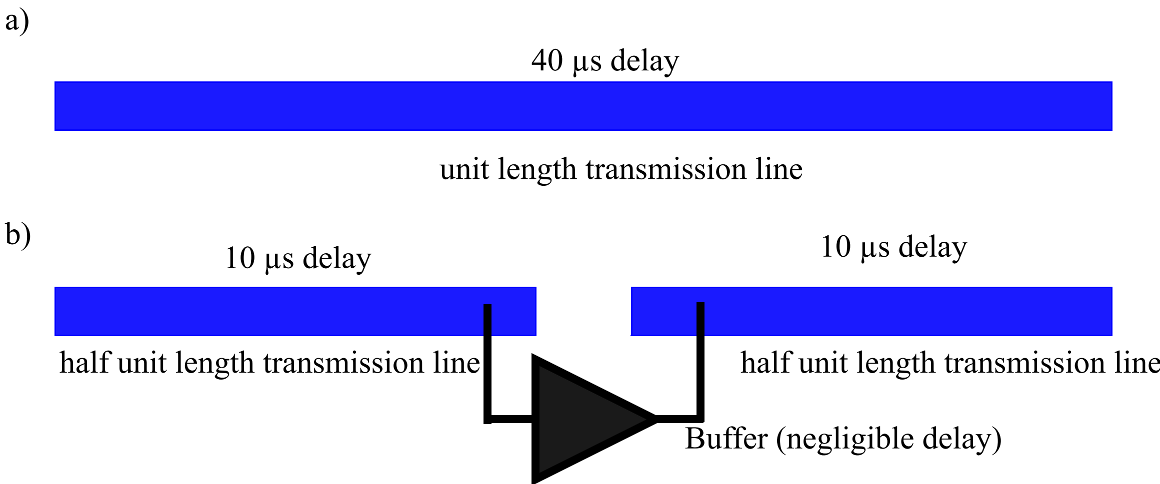


Figure 22:(a) Unit length transmission line. (b) By diving the line in two equal parts with a buffer in between, the delay is effectively cut in half.

3 Experimental Setup

3.1 Thermal Compression Bond Emulation

The following chapter is written as an overview guide of the entire TCB emulation process. This is written for those who intent to reproduce this experiment. The uniqueness of this sensor application made developing a test stand setup a unique electrical and mechanical challenge.

The experimental procedure discussed was developed to emulate the stressful environment that a die would experience during a flip chip thermal compression bonding event. We call this emulation because we intentionally do not create real bonds. Instead a pressure plate is used to do touchdowns while applying appropriate temperature and force up to 80 N and 100-200 °C. That is not say this sensor could not be used while creating real bonds. However, doing so introduces a dilemma. Real bonds are destructive, they use up the sensor chip, i.e. it needs to be replaced with another sensor chip for the next TCB emulations. The value of this sensor is greatly increased if it can be repeatedly used. An acceptable compromise is found by performing touchdowns with the application of realistic TCB environmental conditions while not using any substrate metallization and solder material that would melt and create a permanent bond between bumps and substrate. Figure 23 depicts an overview sketch of the TCB emulation experimental setup. The sensor chip is packaged in a 28 pin sidebrazed ceramic DIP with active auxiliary wire bonds to capture in-situ signals off the sensor die during the bonding emulation. A 3.5 mm square Al mirror chip is used as a pressure plate to do the touch down. The pressure plate was made from a standard 4” Si with a 1 µm thick patterned Al deposited onto its surface. Au ball bumps were deposited on the sen-

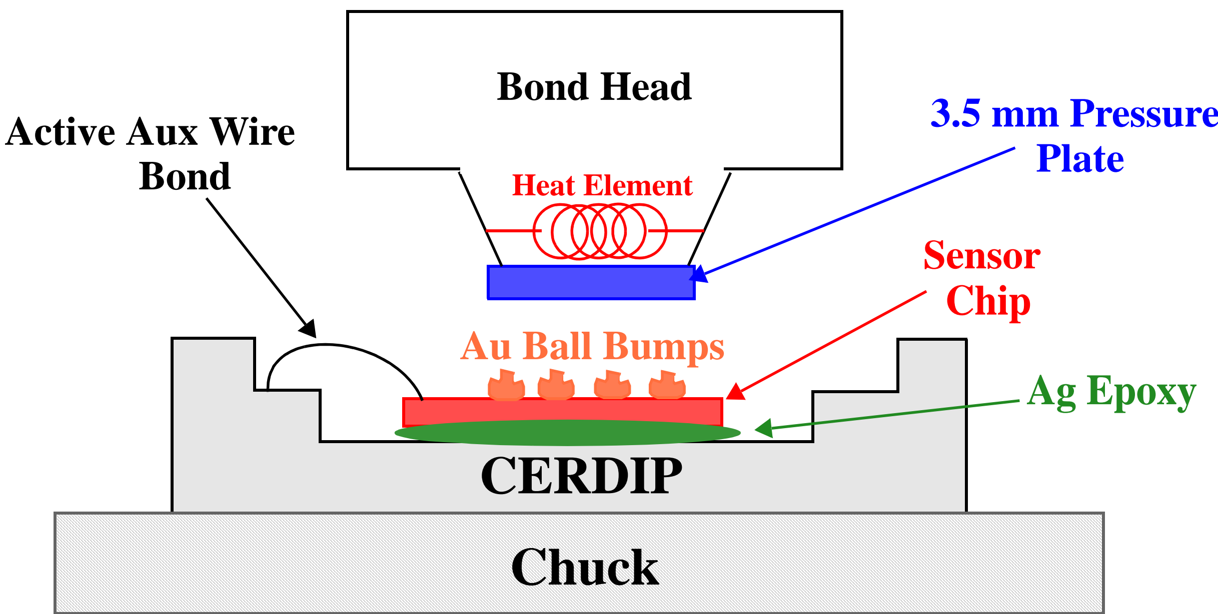


Figure 23: TCB emulation diagram.

sor's bond pads with an automatic wire bonder to emulate Cu pillars. Au bumps were bonded to the sensor chip with the available wire bonder in the CAMJ wire bonding lab.

3.2 Die Attach Information

The first few TCB sensors were die attached by hand with a hand suction tool using a dip stick to apply an Ag die attach epoxy, Ablebond 84 (Figure 24). The samples were then cured in an oven for 2 h at 200 °C. It was found that this hand die attach procedure was not ideal for the experiment. Die attach slopes as much as 100 µm/mm were measured using this method. Later this was upgraded to using the Tresky automatic die attach machine available in the Quantum Nano Center at the University of Waterloo. The tilt was reduced to within 30 µm/mm and the sensor chips were sufficiently compliant and parallel with respect to the DIP package for the experimental purpose. Note the Tresky automatic epoxy dispenser was not yet available in 2015 when this experimental

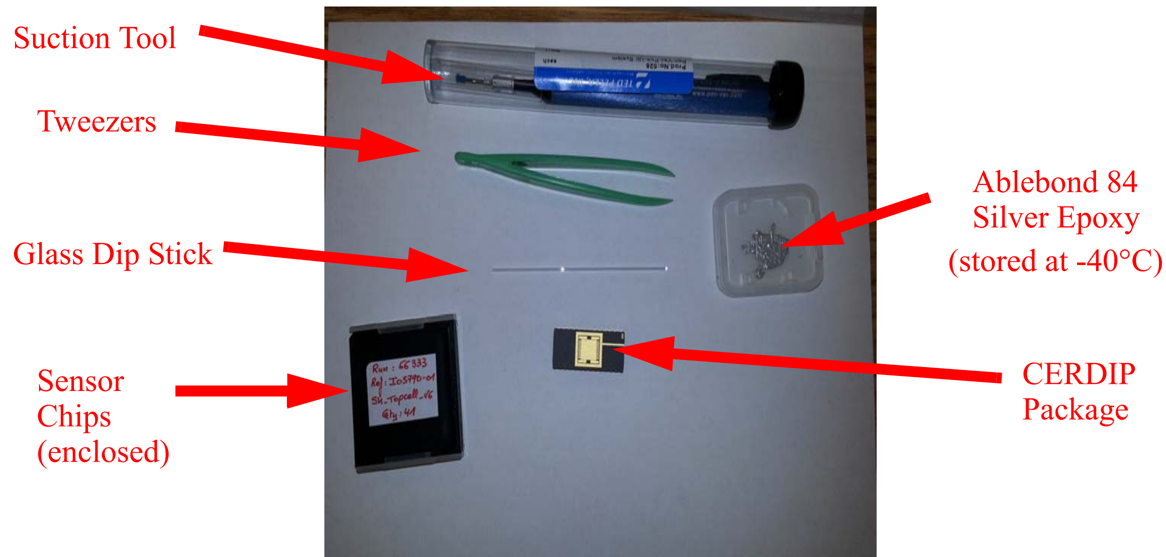


Figure 24:(a) Hand die attach equipment.

setup was in development. Consequently the procedure still ended up using a dip stick to hand apply the epoxy. This resulted in non-uniform and non-ideal epoxy smears under the die attachments. Using a suitable die attach tape instead of epoxy is expected to give more consistent results in future experiments. The importance of a flat and uniform die attach was underestimated. This caused some complications that are discussed in later sections.

3.3 Wire Bonding and Au Ball Bump Information

A 28 pin gold sidebrazed ceramic DIP substrate available in our lab was selected to package the sensor die. This package was selected because it is compatible with our specialized minioven sockets, our established electronic fixtures and our automatic wire bonder's heater plates/downholders. Figure 25 depicts the wire bonding scheme selected for packaging the new TCB sensor chip. Standard 25 µm 4N (99.99% pure gold) wire was used for the auxiliary wire bonds with

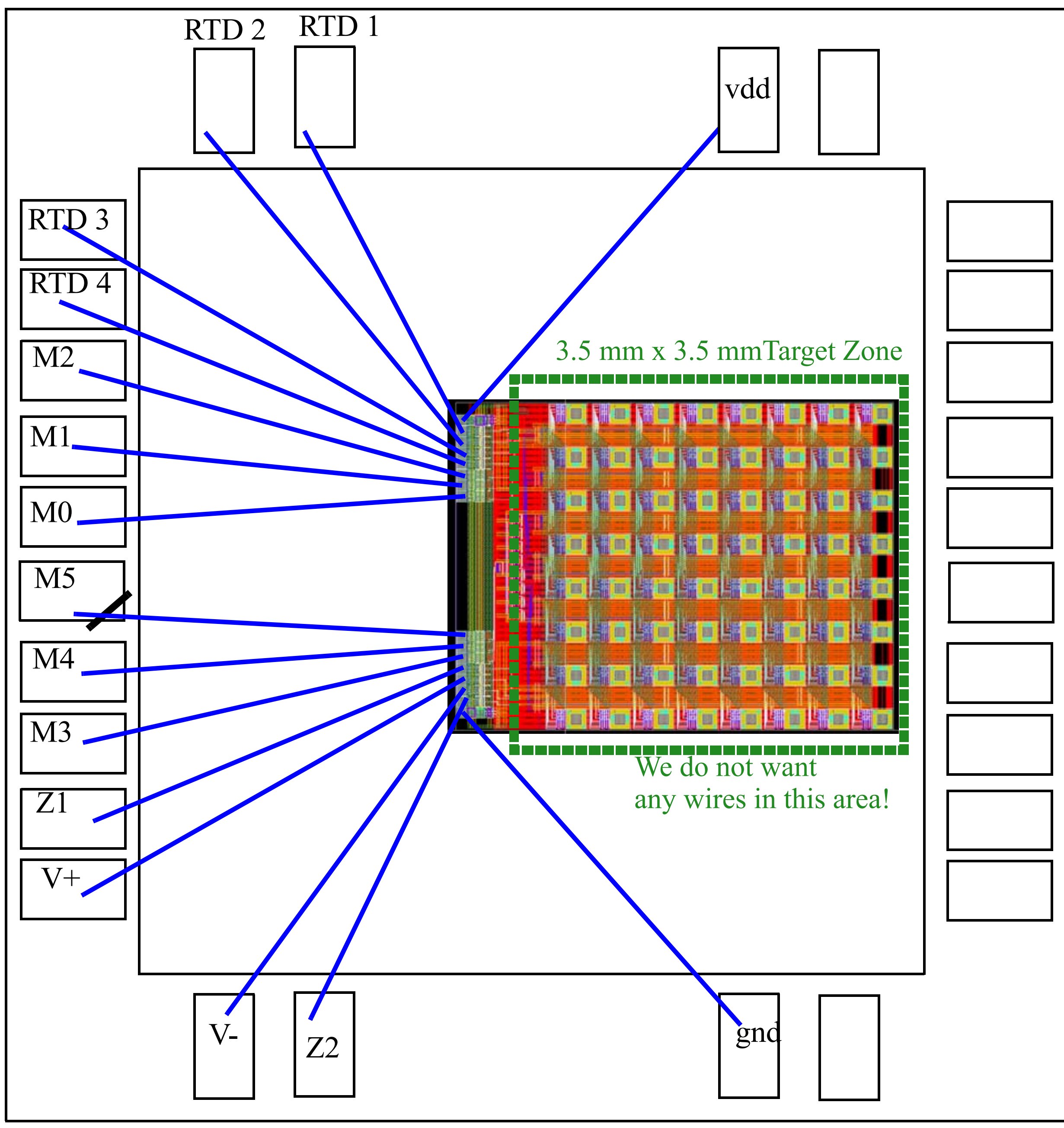


Figure 25:Wire bonding diagram to used for the new TCB sensor array chip.

parameters given in Table 1. Figure 27 depicts the wire bonding recipe as seen on the ESEC 3088 automatic ball bonder's software and a photograph of the auxiliary bonded sensor chip. The wire bonds are intentionally arranged in such a manner that they would not interfere with a bond head or placement tool during the planned experiments to press onto the sensor array area. The VDD and GND wires do come within 200-300 µm of the target touchdown zone but this is well within the placement accuracy range of the Tresky die bonder or the K&S advanced packaging machine. to be used for the planned experiments. The auxiliary wires were not a problem with careful operation of the die placement equipment. Note that some bond wires on some samples required gentle adjustments with a pull tester tool to move the wires away from the target zone, or otherwise prevent them from shorting to neighboring wires. After auxiliary bonding, Au ball bumps were bonded with the same ESEC 3088 to emulate solder bumps in a TCB process (Figure 26). Using a flat tip custom coining tool on a modified automatic wire bonder (Figure 28), the ball bumps were flattened on top. The ball bumps had a wire neck after being deposited by the automatic wire bonder, so they were coined to ensure they were flat (Figure 29). The coining setup employed was also useful for Z force calibrations which is discussed in section 6.1.

.

Custom PCBs were developed and discussed as replacements for the DIP packages. Ultimately they were not implemented due the limited number of prototype sensors dies available and concerns over wire bonding onto the silver PCB metallizations. Figure 30 shows these designs. The PCB approach can be developed further for future experiments using this sensor chip.

Table 1: ESEC 3088 Parameters

	Parameter	Value
Aux. Ball Bond	Ball Impact Force	424 mN
	Ball Bond Force	185 mN
	Ball Bond Time	9.8 mS
	Ball US Power	25.01 %
	Ball Pre US	10.01 %
Aux. Wedge Bond	Wedge Impact Force	400 mN
	Wedge Bond Force	400 mN
	Wedge Bond Time	9.8 mS
	Wedge US Power	17.98 %
	Wedge Pre US	12.02 %
	Tail Length	350 µm
EFO Parameters	EWD	450 µm
	EFO Current	20.04 mA
	EFO Time	2.2 ms
	Tail Length	350 µm
Bump Wedge	Wedge Impact Force	150 mN
	Wedge Bond Force	100 mN
	Wedge Bond Time	9.8 mS
	Wedge US Power	4.98 %
	Wedge Pre US	8.01 %
Bump Ball	Ball Impact Force	424 mN
	Ball Bond Force	185 mN
	Ball Bond Time	9.8 mS
	Ball US Power	30.01 %
	Ball Pre US	10.01 %
Bump Looping	Loop Factor A	0.700
	Ball Security Height	0.05 mm
	Reverse Length 1	0 mm
	Reverse Height 1	0.05 mm
	Reverse Length 2	0 mm
	Reverse Height 2	0 mm
	Loop Height	70 µm
	Horizontal Pull	0
	Loop Mode	“4 Engineering”
Down-holder	Temperature	200 °C

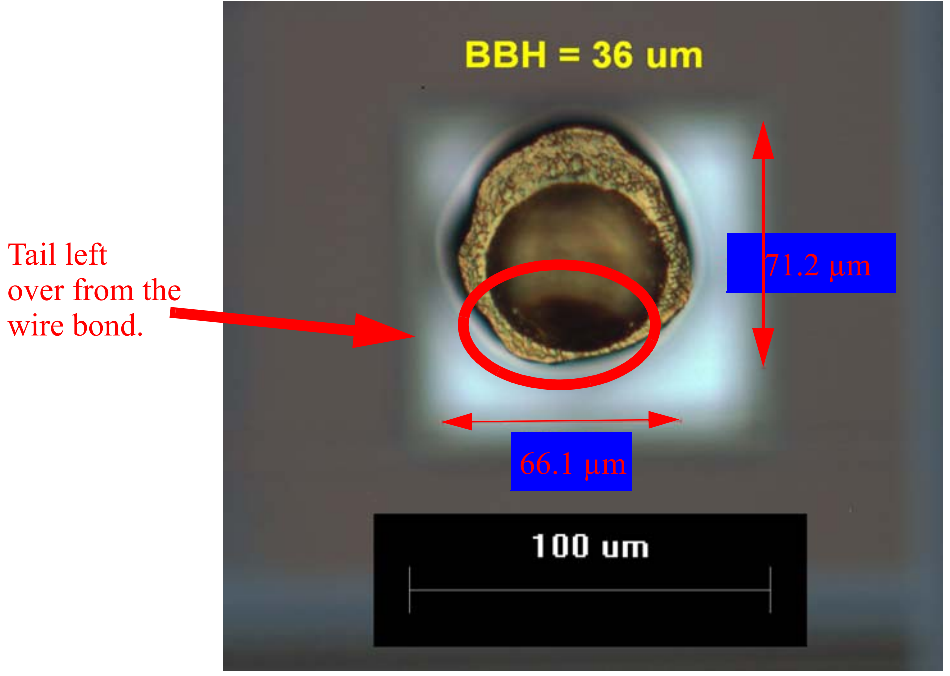


Figure 26:Gold ball bump before coining procedure with 69 µm. diameter used as emulation solder bumps in the experimental. Bonded Ball Height = 36 µm

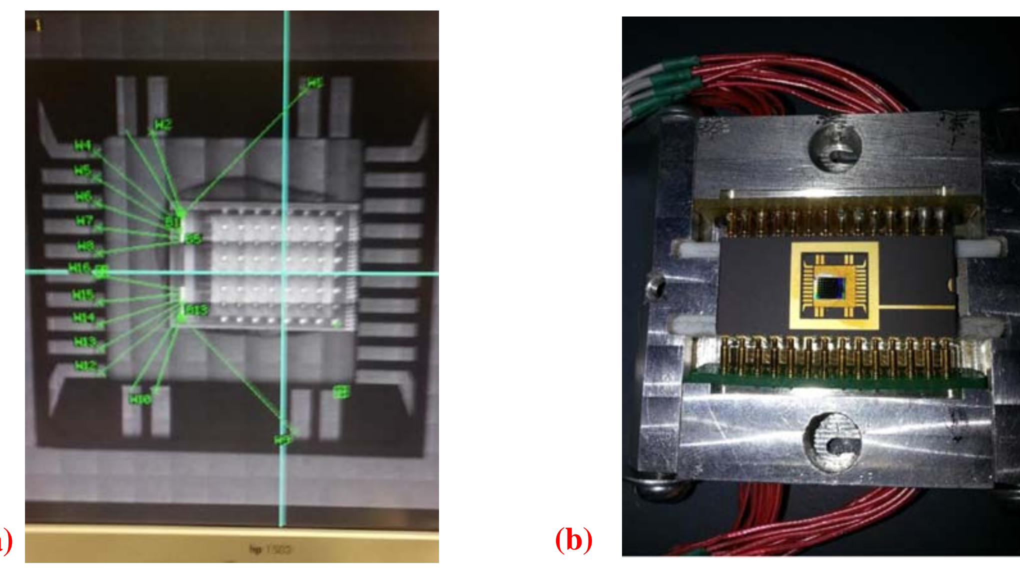


Figure 27:(a) 3088 automatic ball bonder recipe. (B.) packaged TCB chip in active custom fixture for in-situ operation on a the wire bonding machines.

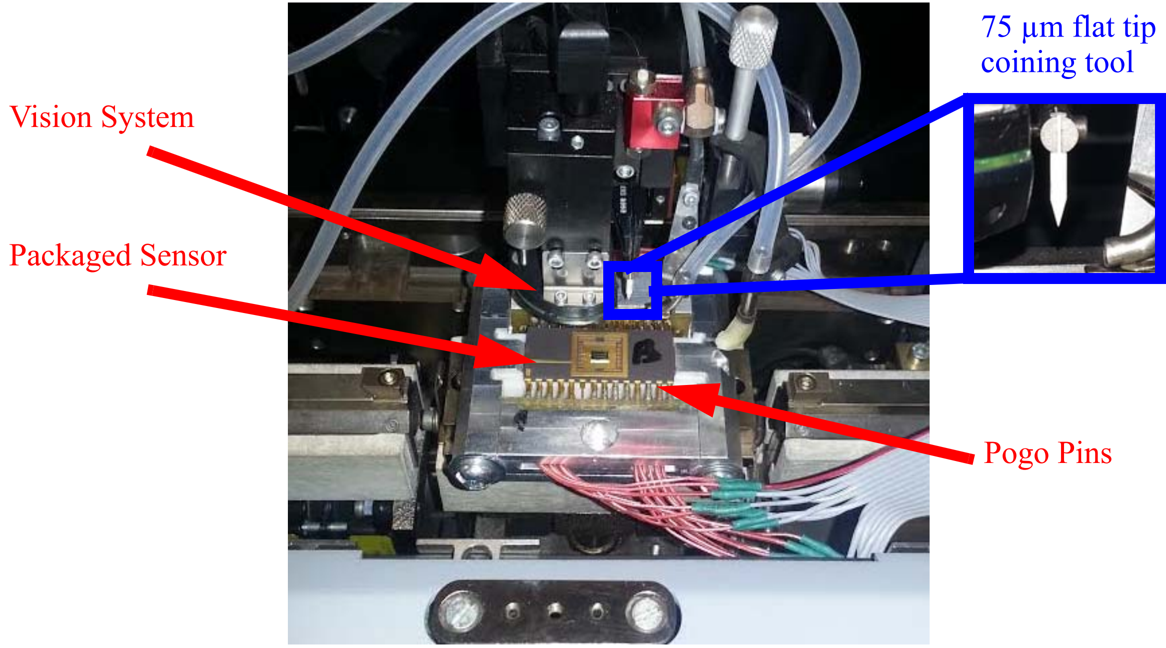


Figure 28:Coining setup on the ESEC 3088. This setup was also used for Z force calibrations.

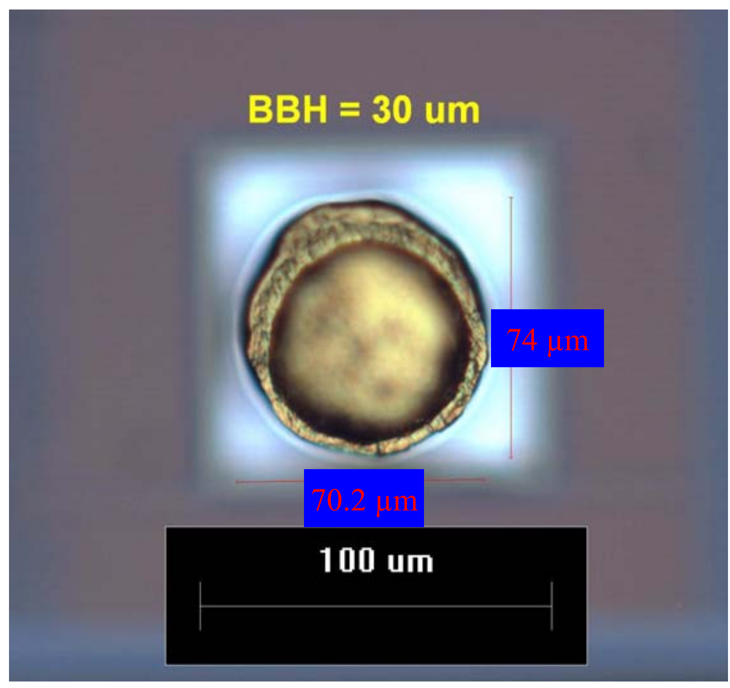


Figure 29:Gold ball bump after coning procedure with a Mean Diameter = 73.16 µm, STD = 1.60 µm and bonded ball height = 29.73 µm with STD = 2.27 µm

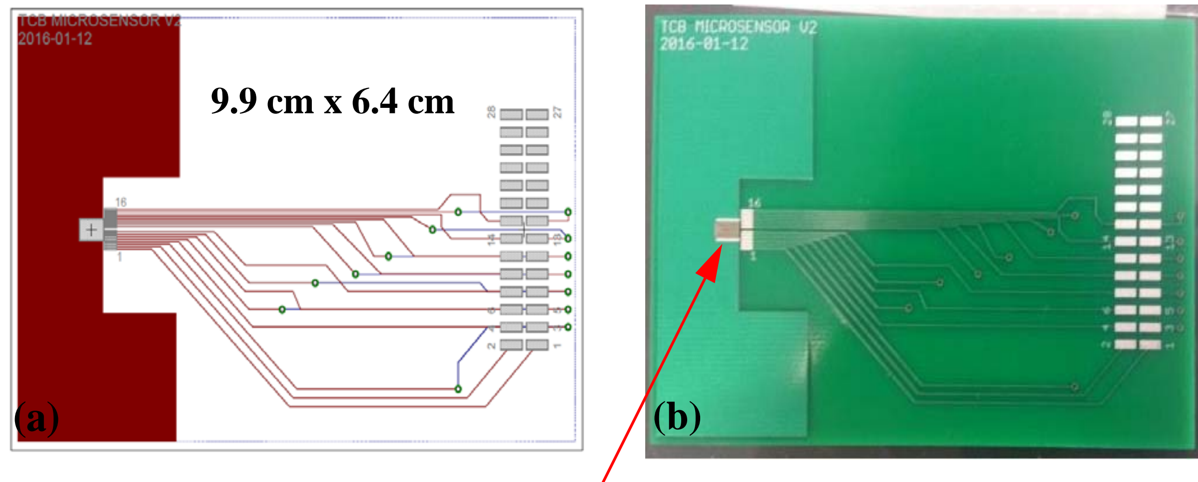
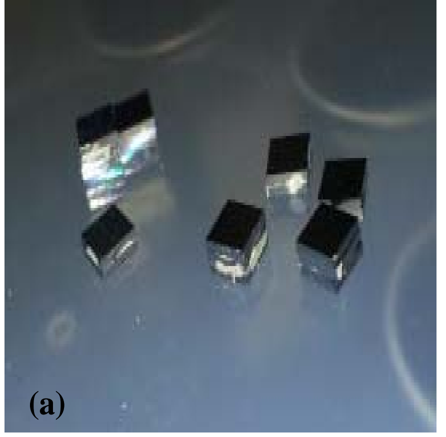


Figure 30:(a) PCB V2 schematic for die attachment with conveniently routed signals. (b) The fabricated pcb with another similar sensor die attached.

3.4 Pressure Plates

To emulate the process, flipping a chip and bonding to a substrate is replaced with a flat pressure plate being pressed with a defined force from above onto a stationary sensor chip. This is upside down to what would happen in a conventional flip chip process. The forces and stress are sufficiently equivalent to get useful information about the thermomechanical effects of the process. The advantage here is that we are not risking our active wire bonds when flipping the substrate. Figure 31 depicts the pressure plates selected for the experimental. Originally a 2.9 mm square pressure plate for force application was selected. This was a standard Si with 1 µm smooth Al mirror finish deposited onto the surface. Initially multiple 2.9 mm plates were stacked and glued together with epoxy to ensure the setup did not touch the bond wires with the bone head bezel. These pressure plates did not have alignment markers and proved difficult for the camera software to place accurately. The experiment switched to a patterned 3.5 mm square wire bonding test chip.



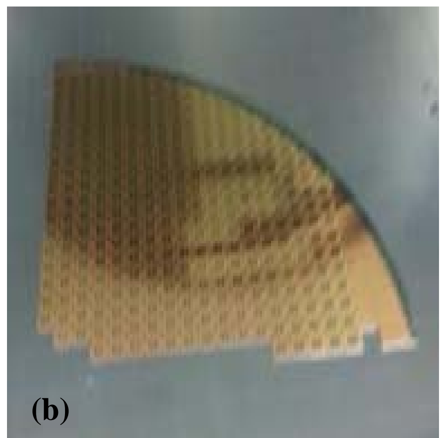


Figure 31: (a) An earlier version of our pressure plate, CMOS chips with un-patterned Al deposited and diced to 2.9x2.9 mm. Multiple plates were stacked in early iterations of the experiment. b) The 3.5 mm x 3.5 mm x 700 µm K&S wire bonding test die with Al wire bonding test pattern that was used in the final experimental.

This test chip has sufficient alignment markers to be placed accurately by the die placement software. Only one test chip was needed as pressure plate once the operation of the placement software was sufficiently practiced.

3.5 Fixture Mounting & Parallelism

A variety of methods were developed to mount the packaged sensor to the various TCB equipment used in this experimental procedure. For the Tresky die bonder machine, a green DIP socket mounted on a bread board was used. A photograph of the setup is given in Figure 32 and Figure 33 is a corresponding schematic depicting the parallelism challenge this approach introduced. Each level of the mounting equipment, particularly the green socket and bread board stages added an unacceptably high amount of parallelism mismatch. These were convenient for inserting multiple samples, but every time users inserted the DIP package it would create a unique planarity mismatch with the bond head. Early attempts to achieve parallel touchdowns with the

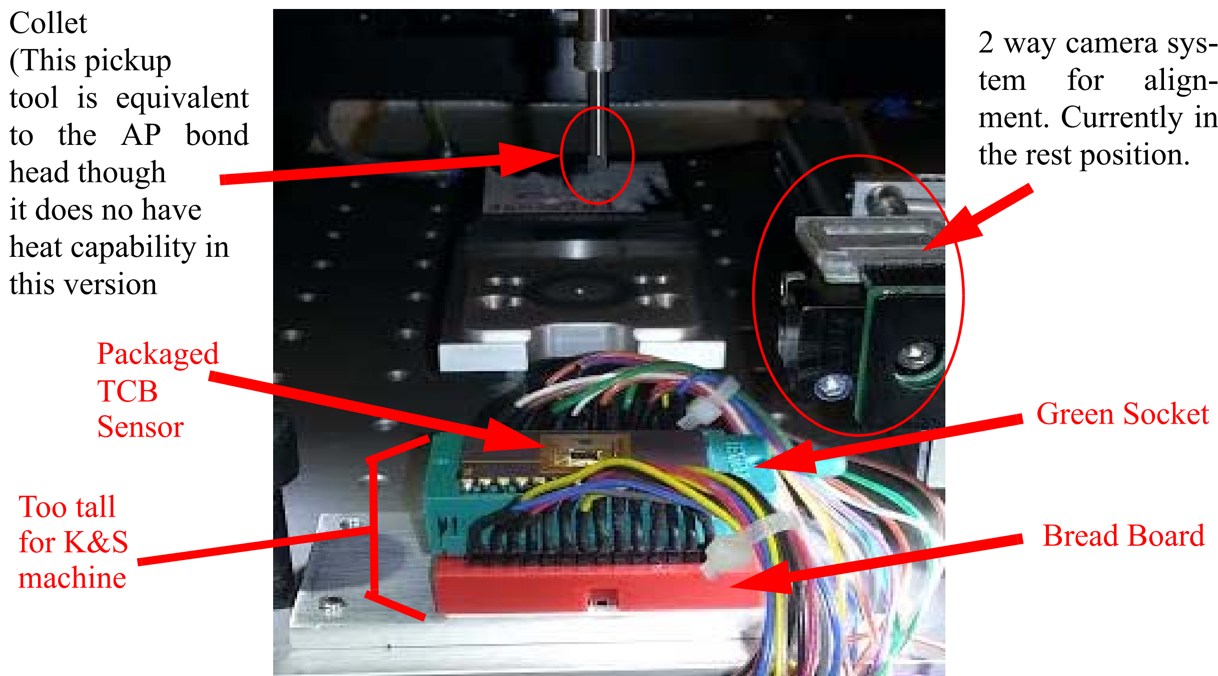


Figure 32: Tresky Die Bonder setup used in the Quantum Nano Center of Waterloo.

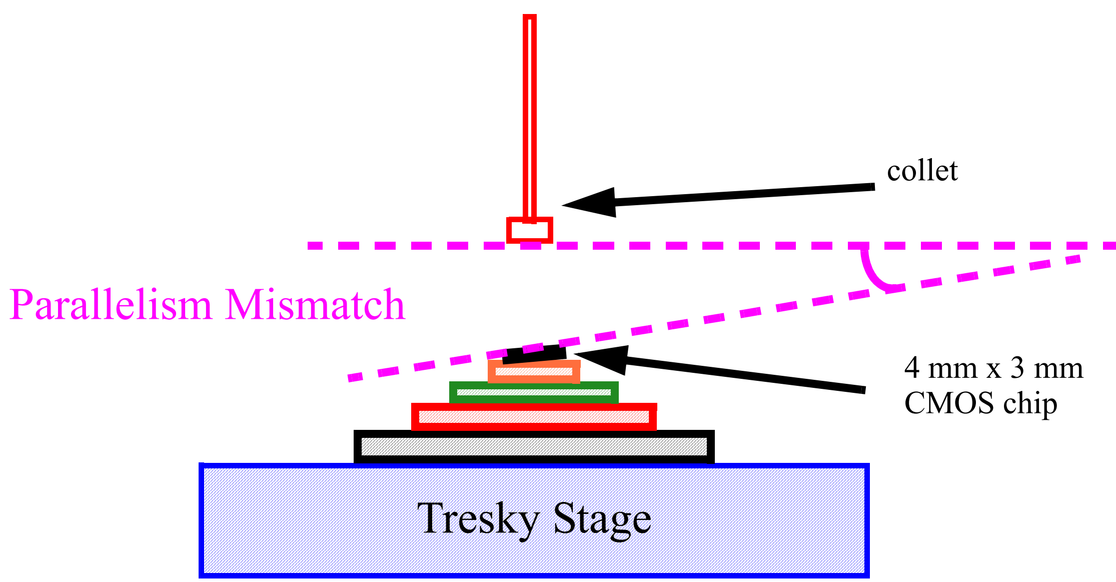


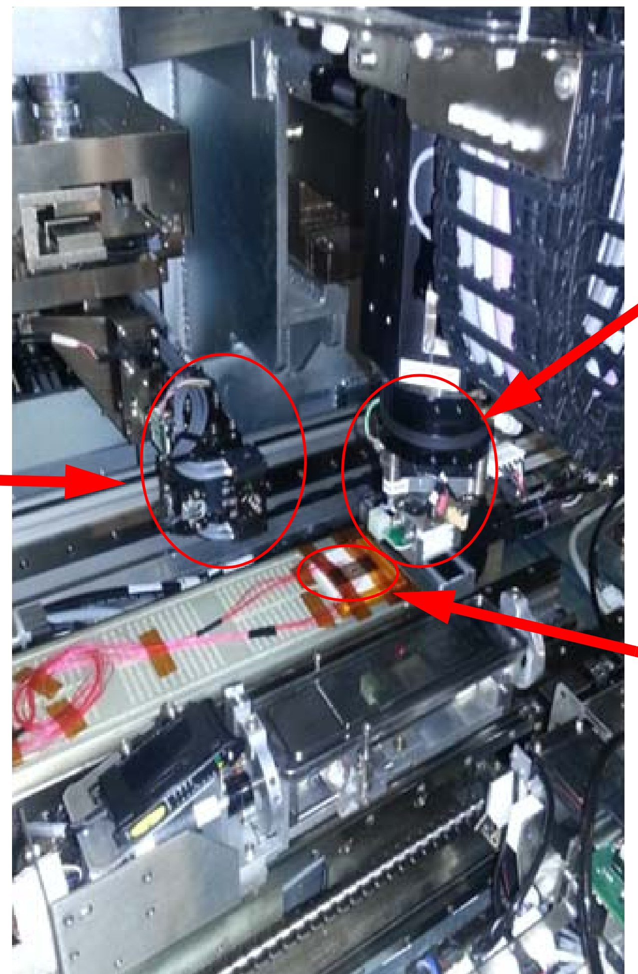
Figure 33: Corresponding Tresky Die Bonder schematic diagram showing parallelism mismatch.

Tresky die bonder were foiled by mismatches of more than 200 µm/mm. The disadvantage of such a large mismatch is that the Tresky die bonder does not have a Z height microscope or imaging capability to assist correcting this mismatch. The final experiment on the K&S advanced packaging machine had the ability to touch and measure the parallelism of the bond head with respect to the destination surface, meaning this bond head could normalize or correct itself to be parallel to a targeted surface. Even with the corrections available in the K&S bond head, the green socket approach was still not appropriate. It was too tall (>10mm) including the bread board. This height interfered with the focal distances of the two way camera system. In addition the green socket approach introduced parallelism mismatch well beyond the limits of the K&S bond head's correction capabilities. Figure 34 shows the K&S advanced packaging setup. In order to address the setup height limitations and fit everything on the K&S machine, the gold coated sidebrazed pins were cut off from the package and then wires were soldered directly to the remaining stumps as shown in Figure 35. This eliminated the green socket and bread board components. The stripped DIP package was mounted to a thin ceramic spacer and then stainless steel shims were used under the spacer to shim and flatten the die with respect to the chuck. This allowed the K&S bond head to first set itself parallel or normalize itself to the chuck. As long as the die was compliant with the chuck, sufficiently parallel touchdowns could be made.

3.6 Hardware Setup

The major hardware components used in this experiment are depicted in Figure 36. A schematic representation of the sensors with differential amplifiers is given in Figure 37. Table 2 gives the exact parts used in the lab to verify the TCB chip.

2 way vision system. This automatically positions itself before touchdown to align the bond head and target zone on the sensor chip, then returns to rest position before bonding.



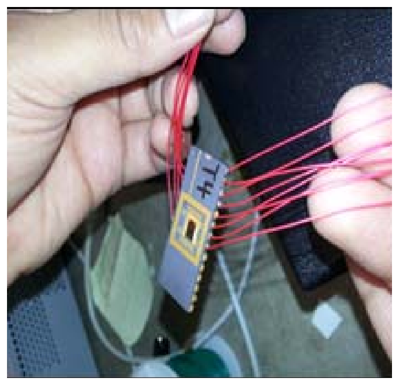
Bond Head. Unlike the Tresky setup, we can apply heat with this tool.

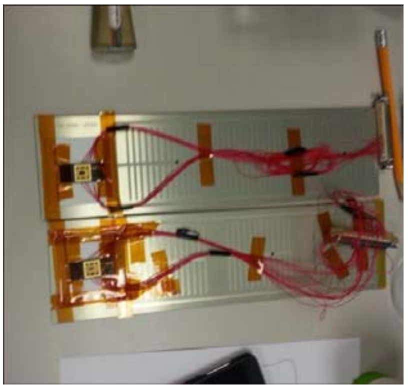
Packaged sensor chip sitting on a white ceramic spacer and then on top of a metal bond chuck. Secured with high temperature tape.

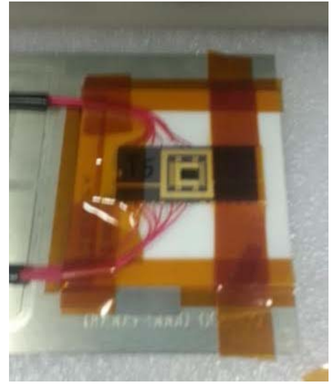
Figure 34: K&S Advanced Process setup.

A 5 V UNO Arduino with the ATmega328P micro controller was selected for this experiment. For this prototype setup, the 16 MHz basic Arduino was chosen. The Arduino response time is shorter than the 100 μs settling time of the onchip multiplexer. The Arduino was programmed to wait for a start command from the serial port and then to cycle non-stop through the preselected

pads. The multiplexer hold time t_{pad} was set to 1000 μs. Example code to run an Arduino controller through every pad address with 1000 μs t_{pad} is given in Figure 38. The Arduino has a 3.3V power supply with up to 50 mA when powered by standard USB. The digital mux bits of the Arduino are 5 V signals. A logic translator chip, SN74LVC245A was needed to down-and-outer from 5 V to the 3.3 V expected by the sensor chip. Digital CMOS power consumption (includes logic converter chip) was 1mA - 5mA depending on TCB chip multiplexer state. Both the RTD and Force channels are differential signals. They need a differential scope or otherwise should be fed into differential amplifiers, the range of which is defined by the application. For the force signal case, the same differential amplifier which was designed by UW staff Michael Althaus, Dominique Leung, and Andy Barber, used by Aashish Shah for the PMV1 chip and assembled by Andy







Step 1:
Remove dip pins and solder wires directly to the package.

Step 2:
Mount the package on a ceramic spacer on the bond chuck. This can be removed and taken to a microscope for Z height measurements.

Step 3:
Add stainless steel 500 μm shims as needed until the sensor is parallel to the chuck. Then secure with more tape.

Figure 35:Steps to mount the sensor on the K&S advanced process machine.

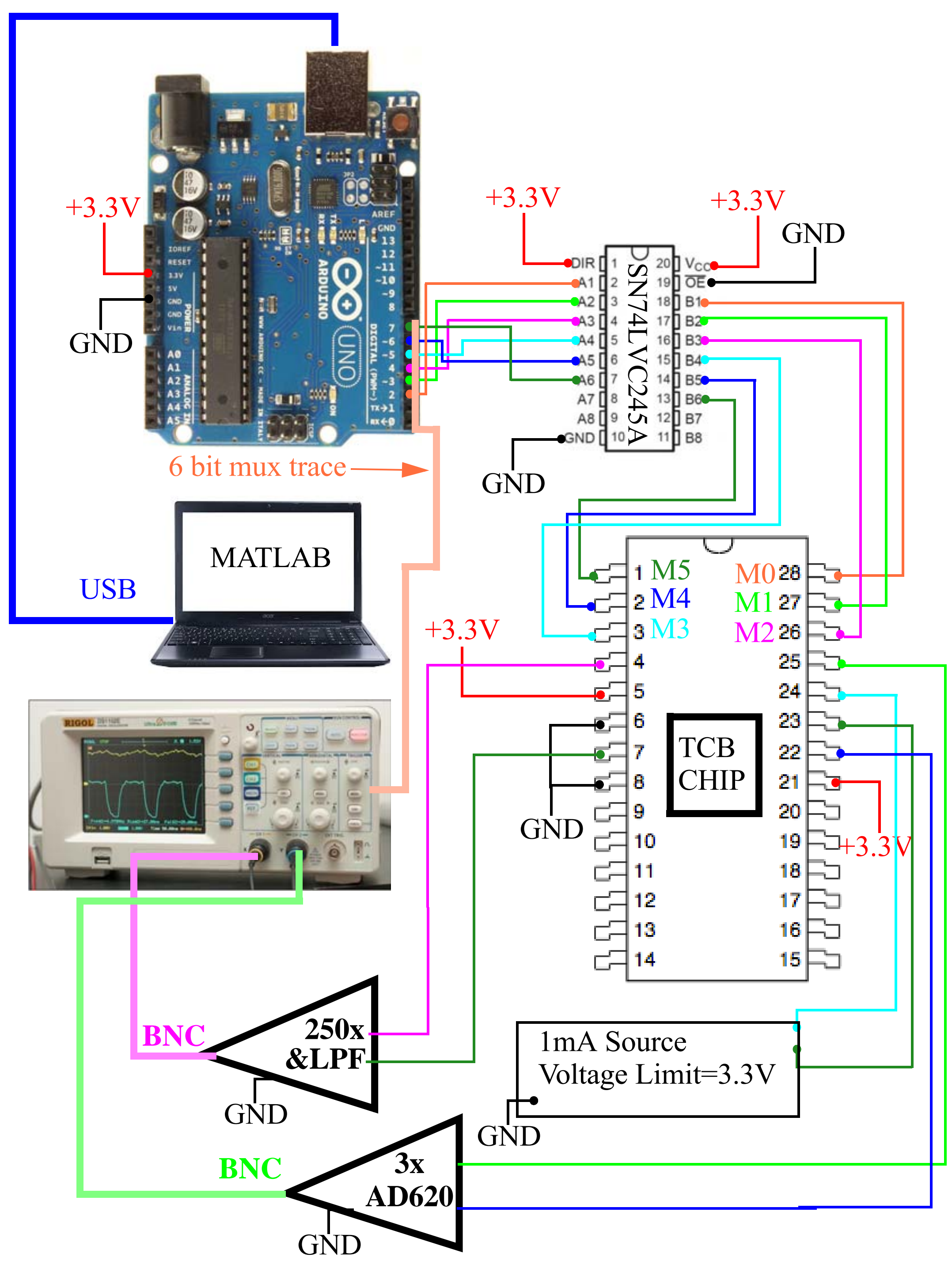


Figure 36:Hardware schematic.

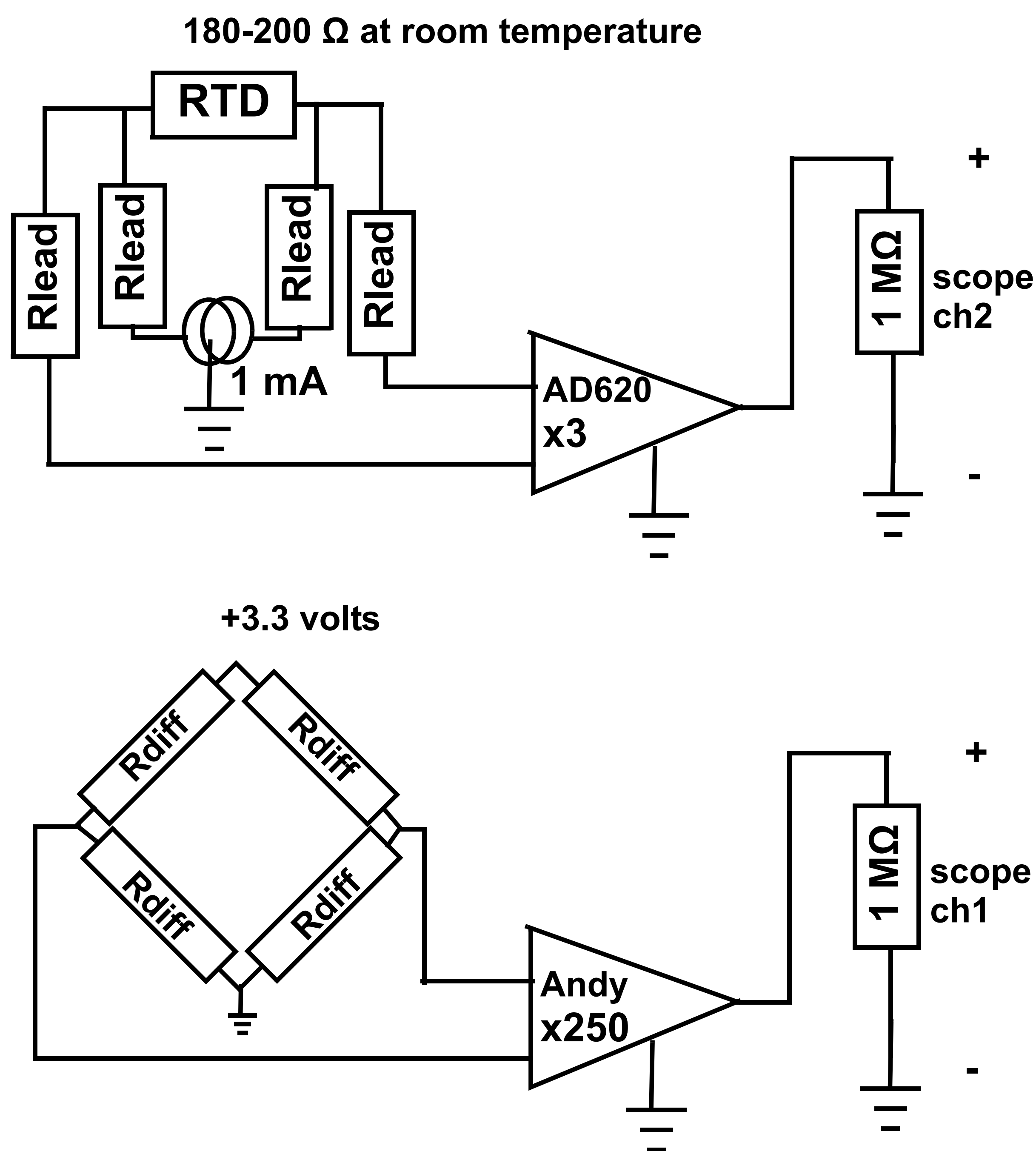


Figure 37:Sensor circuit diagrams. A general purpose AD620 instrumentation differential amplifier and a 250x custom high speed amplifier, designed by Aashish Shah and built by MME electronics technician Andy Barber are used.

Table 2: Parts List

Part	Specific Part used in Dec 2015 at UW
Control Board	Arduino UNO Board
Logic Translator	Texas Instruments SN74LVC245A
Oscilloscope	RIGOL DSE1102C
1mA Source	Agillent B2911A Precision Current
Amplifier	250x black amplifier box designed by Andy Barber
Laptop	Toshiba laptop with Matlab and USB port
TCB package	28 pin cerdip package

Barber. This was used in Samuel Kim's thesis work [3] to capture the ultrasonic harmonics introduced by the ESEC 3088 automatic wire bonder. The gain was measured at 250x (24 dB) with a 6th order Buttersworth filter with a cutoff frequency of approximately 600 kHz.

The RTD amplifier was an off the shelf AD620 general purpose instrumentation amplifier. This can be tuned by referring to the data sheet and changing the gain resistor. It was a coinvent, cheap and simple to use component that could be replaced on the fly during the visit to K&S at Fort Washington. Future work can better optimize this component in order to reduce noise on the RTD signal. Particularly the cutoff frequency of the amplifier, which was in fact well above the cut off frequency of the scope. This was amplifying the full range of noise while looking at an almost DC signal giving motivation to add a low pass filter stage and or better design this component.

```
byte command = 0;
byte code = 0;
byte pads[64] =
{0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,
39,40,41,42,43,44,45,46,47,48,49,50,51,52,53,54,55,56,57,58,59,60,61,62,63};

void setup() {
 /* Start serial */
 Serial.begin(115200);   /* Msut match this baud rate in matlab in order to communicate*/
 delay(2500); /* wait 2.5 seconds after power up for everything to settle*/

 /*this will set the digital pins to output mode and preserve the mode of serial tx and rx bits*/
 DDRD = DDRD | B11111100;
  byte odd = (3<<2);  /*set output to odd, since we are triggering data on the fall of the M0 bit.*/
  PORTD = (PORTD & B00000011) | (odd & B11111100);
}

void loop(){/*this will run in a loop waiting for serial commands from matlab*/
 if (Serial.available() > 0)
 {
    /*matlab should bitshift the address twice before sending with bitshift(command,2)*/
  command = Serial.read();
  if (command == 115) /*if a serial byte, ascii code 115 = ‘s’*/

  {
    while(1)
    {
     for (int i = 0; i<64; i++ )
     {
       code = pads[i];
       code = code<<2; /*bitshift the address twice, since we dont write to the first two (tx/rx pins)*/
       PORTD = (PORTD & B00000011) | (code & B11111100); /*  PORTD & B00000011 preserves tx and rx
bits, code & B11111100 takes only the command*/
       delayMicroseconds(1000);
     }
    }
  }
 }
}
```

Figure 38:UNO arduino code example. This code will poll all 64 pads, holding for 1 ms at each pad.

4 Post Processing

4.1 Raw Unparsed Data from Oscilloscope

The experimental setup used included a mixed signal oscilloscope. Figure 39 depicts the Agilent DS0-3014A oscilloscope with mixed signal card available that was used to collect the raw data. The information on screen contains interleaved data for all 64 sensor pads. Using the mux trace and Matlab script “ProcessAllPads.m” can post-process the data and parse the RTD and Force signals. The information can be saved as a a binary wave format. Other formats like CSV may be more convenient but do not contain all of the data points and clip information. The program

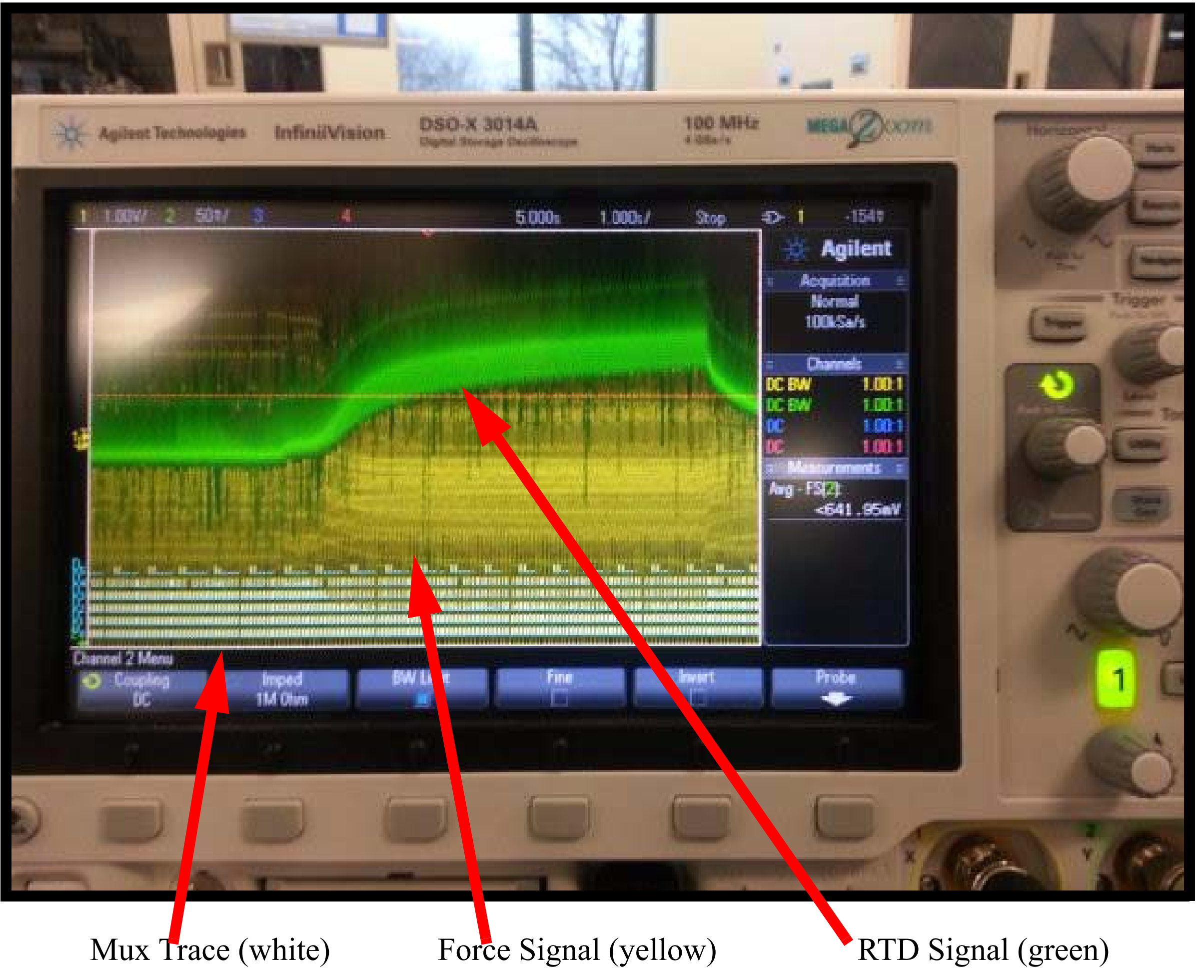


Figure 39:A photo of the DS0-3014A with raw data capture during a TCB emulation event.

“importAgilentBin.m” provided on the Agilent web site is suitable to read these binary file formats into Matlab. Depending on the hardware setup used, the mux trace can contain glitches. It is therefore recommended to always visualize the raw data in Matlab to identify and remove these glitches as shown in Figure 40.Notice the non-sequential increases in the mux trace from 0:63. During processing data associated with these time indexes is deleted. As a general rule of thumb, removing the first 100 μs after every transition guarantees that only good and fully settled data is used. Once these glitches are removed, the data can be de-interleaved for further processing.

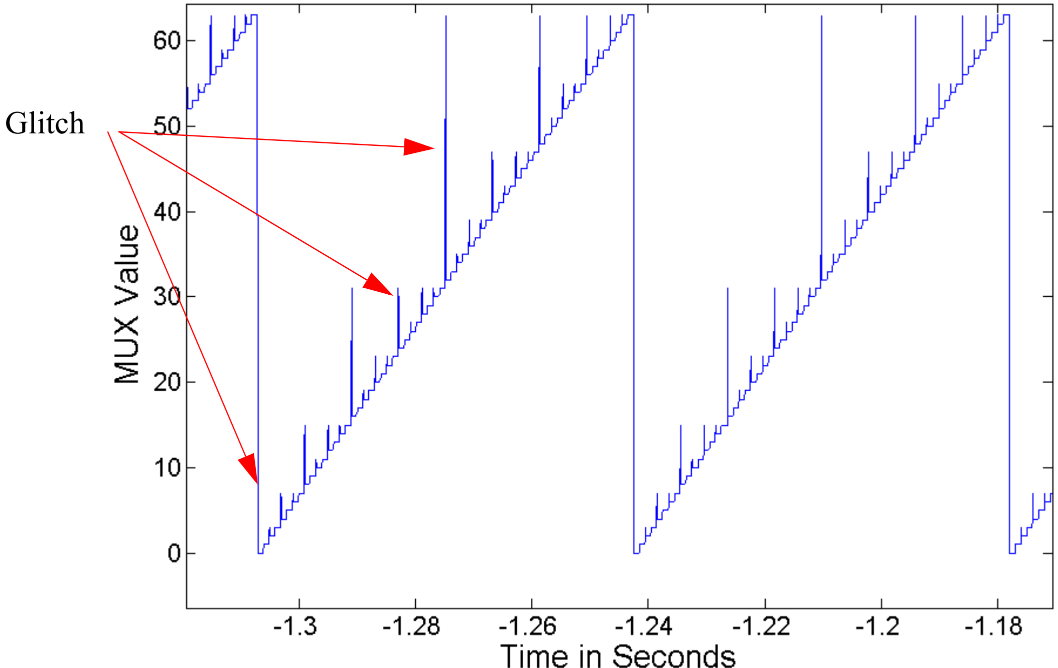


Figure 40:Matlab plot of mux trace. The out-of-sequence increases are glitches.

4.2 Sample Rates and Requirements

Let N be defined as the number of pads to be sampled, T_{pad} as the hold time period of the multiplexer at each pad. The system sample period, T_{system} is given as

$$T_{system} = T_{pad} \times N \quad (1)$$

If $N = 64$ and $T_{pad} = 1$ ms then the systems samples each pad once every 64 ms. According to Nyquist-Shannon criterion [25], this sets an upper bound on what can be detected with the sensor. The sensor needs to sample at no less than twice the frequency of the fastest event. This means a T_{system} of 64 ms is not suitable to resolve ultrasonic vibrations in the 10-20 kHz range which is typical for the ultrasonic transducer included on the Tresky flip chip equipment. Users can reduce the number of pads sampled or the multiplexer hold period to accommodate faster events. There are pragmatic limits to the improvements that can be made. The scope has a maximum sample rate and finite memory. The settling time of the onchip multiplexer is also measured at worst case as 100 µs with the 16 MHz basic Arduino driving it.

4.3 Averaging and Interpolation

Because of the way the data is sampled in a serial sequential format, a timing skew is introduced. The setup samples pad n at time = 0 ms with T_{pad} = 1 ms. With oscilloscope at 100 kHz sample rate this means 100 data points are captured for a each individual pad during one cycle. After throwing away the glitches, this number is reduced to 80-90 data points. In order to remove high frequency components of thermal (white) noise, post processing must average these 80-90 data points for pad n to get what is referred to as a single pad measurement (Figure 41). The next pad is sampled at time = 1 ms for a period of 1 ms. Again, the pad measurement is the mean of 80-90 data points but it is delayed. So if 64 pads are sampled, the 64th pad will be sampled 64ms later. This presents a problem if 3D surface visualizations of the signals at an instantaneous point in time are desired. The solution to this problem is to use linear time interpolation of all parsed pad data vectors to translate them to be all on the same time vector base. This solution is only valid

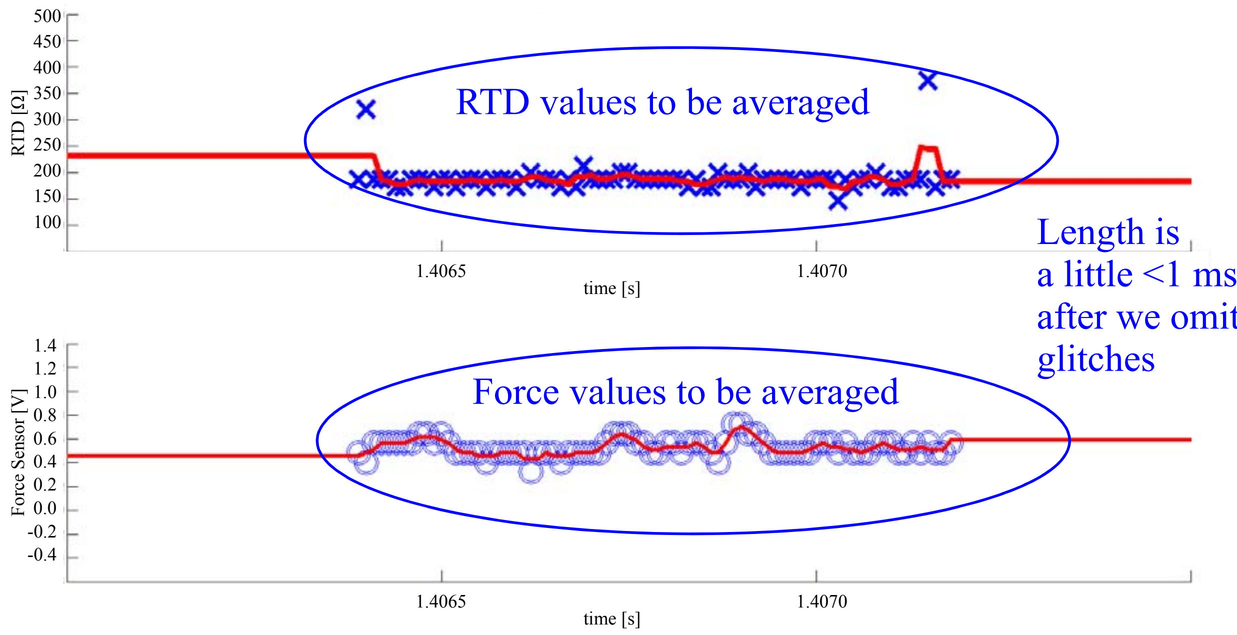


Figure 41:A single pad measurement on pad 0.

with the assumption that data is linear in the T_{pad} intervals. For the RTD data, an additional moving time average filter is applied to clean up noise and smooth the signals.

After parsing the data, smoothing it and removing timing skews, a surface fit (see Matlab package "gridfit") is applied to create visualizations of the 3D surface corresponding to a set of pad measurements for an instantaneous point in time. For the RTD sensor, of which there are 64 available, an 8x8 contour surface without any interpolation / extrapolation is used. However, for the Z force, of which there are only 30 sensors, a linear space interpolation is needed to fit a surface to all 64 pads filling in the gaps. Similarly for the X and Y sensors a linear space interpolation is used, with linear space extrapolation to account for the perimeter of the sensor chip where the X or Y sensors do not cover the 3 mm x 3 mm sensor area.

5 Sensor Integrity

5.1 Force Sensor Integrity and Calibration

The force sensor sensitivity depends on the shape and size of the ball bumps as well as their placement location on the bond pads [15]. The setup introduced in section 3.3 Figure 28 was used to calibrate the Z force sensors and determine sensitivities. A defined force profile is programmed into the automatic wire bonder and then used with the 75 µm flat tip capillary to apply the defined force onto the individual ball bumps. The sensor measurement during a two stage coining force profile is given in Figure 42. After the first 500 mN impact, the bump experiences a permanent shift in the neutral voltage offset of it's embedded sensor. A possible explanation for this permanent offset change is given in Figure 43. The neutral state of the sensor changes permanently

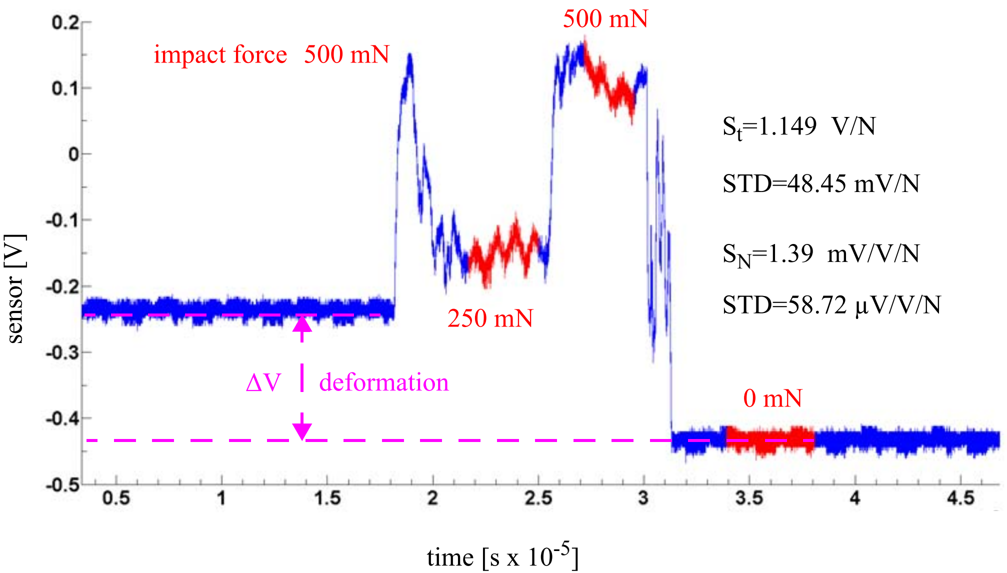


Figure 42: Deformation Event from a wire bonder with a 75 µm flat tip coining capillary. A 2-stage bond profile is applied, 500mN impact, 250mN bond force 1, 500mN bond force 2.

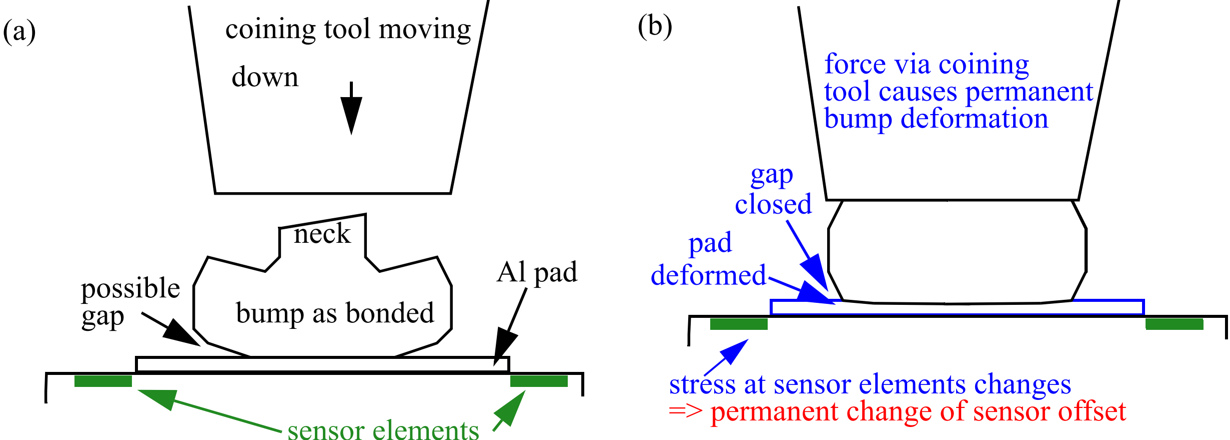


Figure 43:A possible offset change explanation. (a) before coning (b) after coining.

when the bump is coined and plastically deformed. The change is reflected in the stress voltages detested at the nearby embedded sensor elements.

Subsequent impacts of equal or lesser force magnitude did not cause significant voltage offset changes or further bump deformation as shown in Figure 44. Therefore calibrations are valid unless the bumps are plastically deformed again.

The X &Y sensors can be more difficult to calibrate and such a calibration is not reported here. A possible approach for the future is to use a shear tester tool to apply defined forces along the horizontal axes [15].

A differential amplifier with 250x gain was used to capture the force signals with a 3.3 V bias across the bridge. We define the amplified signal force sensitivity as

$$S_t = \frac{\Delta V}{F} \tag{2}$$

with ΔV as the change in voltage over a defined force F. For the Z sensors the mean S_t was measured at 1.49 V/N with a standard deviation of 48.45 mV/N. This can be normalized using

$$S_N = \frac{S_t}{3.3\,V} \times \frac{1}{250} \tag{3}$$

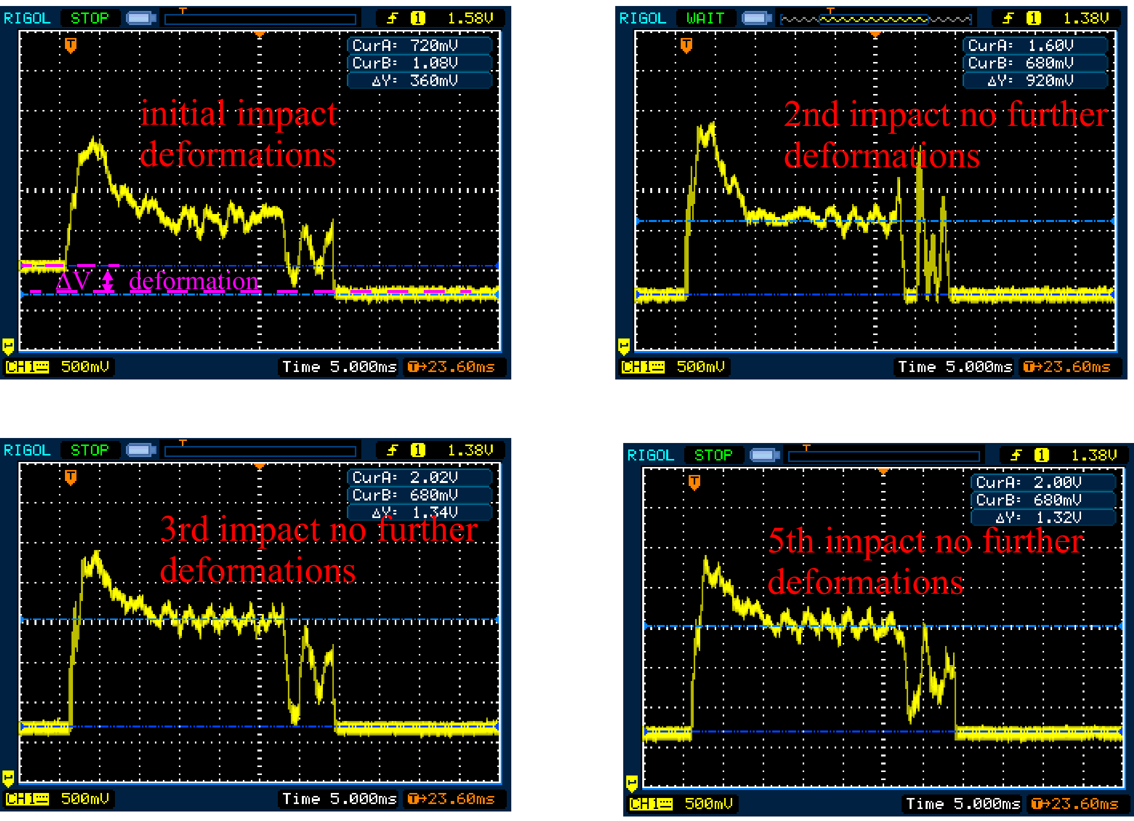


Figure 44:An initial bump calibration with deformation and subsequent impacts without further deformations.

yielding mean S_N of 1.39 mV/V/N with standard deviation of 58 μV/V/N. Reference [15] reports a Z sensor with a sensitivity in the same order of magnitude, 2.24 mV/V/N. The calibrated Au ball bumps were measured at 73.16 μm diameter with standard deviation of 1.60 μm and were 29.73 μm tall with standard deviation of 2.27 μm. We make the assumption that variability in the bump dimensions has negligible impact on sensitivity for variations of 2-3 μm or less.

5.2 Force Sensor Warpage

While the Wheatstone bridge configuration is designed to cancel out temperature effects, the sensor readings still change with temperature because of thermomechanical stress due to the thermal expansion mismatch between pad metal and Si chip. The thermal coefficients of expansion for Al bond pads, 22.2 ppm /K, [1] and the surrounding Si bulk, 3 ppm/K [1] are substantially different. The Al bond expands, causing stress, which is what the Z sensor is designed to detect. Globally, the system experiences further warpage introduced by the mismatch of the ceramic package, 5.4 ppm /K [1], and the Si chip. They are bonded together with a thin film of Ag filled Epoxy with an estimated thermal coefficient of expansion of 100 ppm/K. Additional effects of the die attach are discussed in [15]. These changes only effect the voltage reference level (offset) of the sensors, $V_i(t_0)$, measured when no force is applied. Therefore, if we look at the change in voltage with respect to a known reference we can determine the applied force

$$F_i(t) = \frac{V_i(t) - V_i(t_0)}{S_t} \tag{4}$$

with i = 1,..., 64 the multiplexer index.

The self warpage of the Z sensor is illustrated in Figure 45. All 30 raw Z voltage signals experience a uniform 0.51 V shift in voltage offset when no force is applied over a 90 °C temperature sweep. The temperature was programmed inside the K&S AP machine on the metal chuck. We use the loose assumption that the K&S AP machine's reported chuck temperature is the same as the temperature on the surface of the sensor chip. A contact thermal probe was used on the surface of the package, (the ceramic portion, not the sensor) to verify the reported chuck temperature was within 2 °C during the measurements.

The Y signal, Figure 46, however are split into three distinct groups which correlate to the Y sensors located in the central region of the chip. These central Y sensors experience less stress as a result of the Y component of thermal expansion. And those Y sensors in the North and South regions, which experience greater magnitudes of stress as result of the Y component of thermal expansion Figure 47 shows the X signals. Like the Y case these split into three groups, West, East, and Central, though the West side is dampened because of the digital logic CMOS and aux bond pads which occupy a large area between sensors and chip edge, so the sensors on that side have a difference mechanical neighborhood compared to the sensors adjacent to the other edges.

5.3 RTD Sensor Integrity and Calibration

The RTD sensor is biased with a constant 1 mA current so we can measure the voltage and calculate resistance using Ohm's law. The relationship of resistance of metal and temperature is linear. [1],[15] which leads to

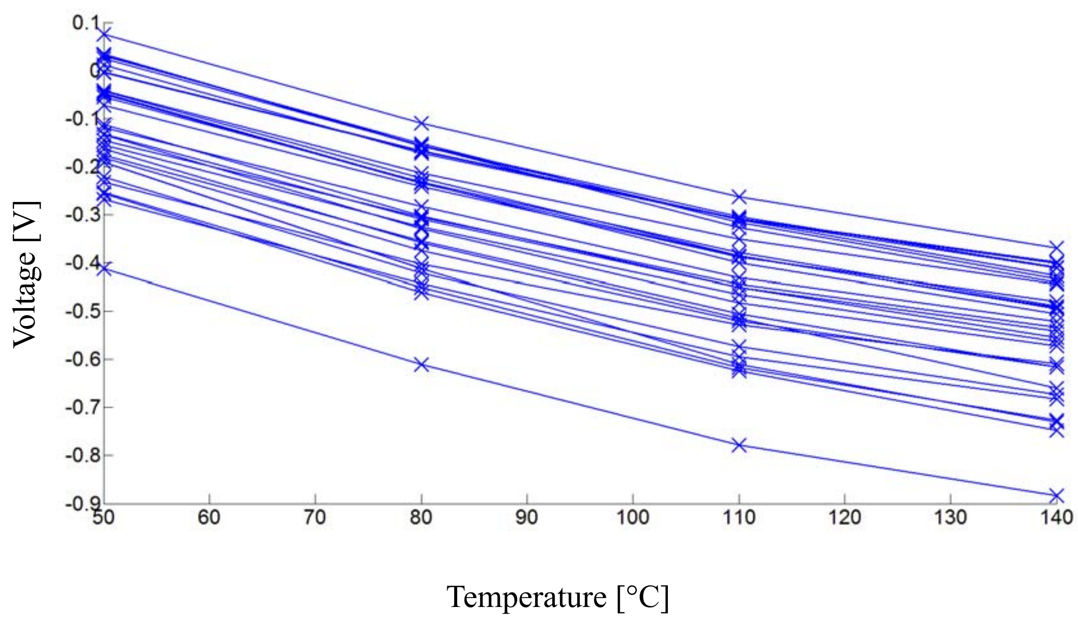


Figure 45:Z raw signals over a 90°C temperature sweep without force.

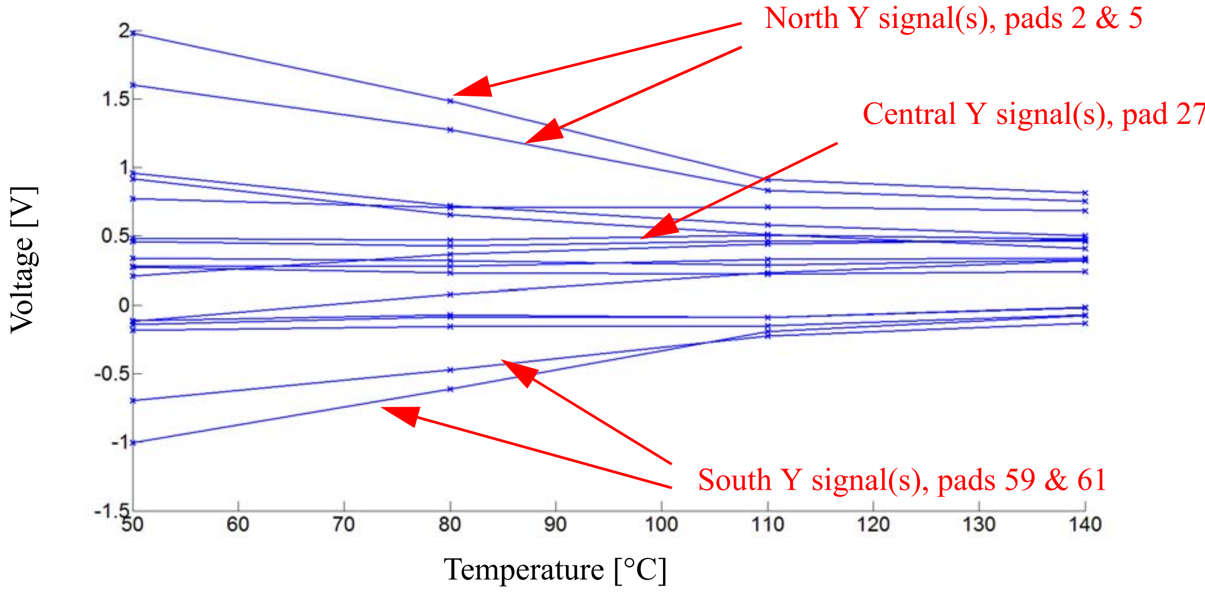


Figure 46: Y raw signals over a 90° C temperature sweep without force.

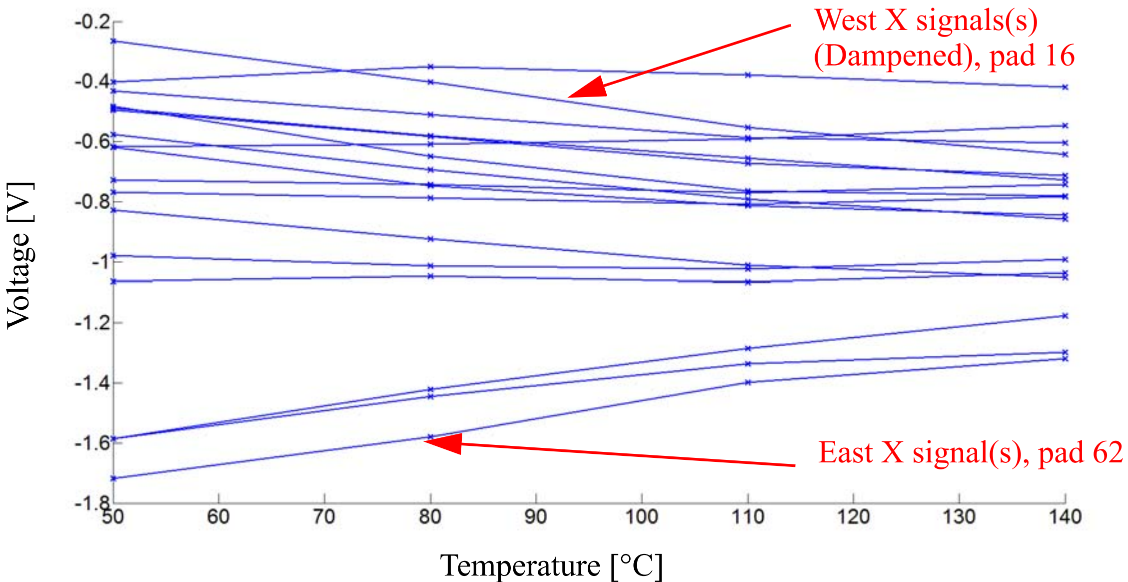


Figure 47:X raw signals over a 90°C temperature sweep without force.

$$R(T) = R_{50°C} + R_{50°C}\alpha_{50°C}(T - 50°C) \tag{5}$$

Using the temperature coefficient of resistance at 50 °C from a similar CMOS top metal, $\alpha_{50°C}$ = 0.00277 K-1 [12], and the known RTD values for a defined temperature of 50 °C, we can derive the absolute temperature for the 64 RTDs as

$$T_i(t) = \frac{1}{\alpha_{50°C}}\left[\frac{R_i(T)}{R_{i50°C}} - 1\right] + 50°C \tag{6}$$

with T = temperature, R = resistance and t = time, and i = 1,..., 64 the multiplexer index. The mean value of $R_{50°C}$ is measured as 186.94 Ω with a standard deviation of 0.89 Ω.

6 Example Results & Applications

6.1 Tilt or Parallelism Mismatch

A two stage force only (no heat) profile was used, with phase 1 ramping from 5 N to 80 N in one step, and phase 2 ramping from 40 N to 80 N in 10 N steps. Figure 48 shows the nominal force profile programmed to the K&S TCB bonder and presents the results of 30 Z sensors when we pressed. The packaged chip was measured with an optical microscope to have tilt in the X-Y axis in the order of 10-20 μm/mm with respect to the substrate and bond head. This agrees with the sensor measurements of the top right corner, the highest area of the die attach with respect to the bond head. As the bond head came down in phase 1, it first made contact with that elevated corner region before contact was distributed amongst the neighboring sensors. The bumps were plastically deformed in this top right corner region. The detection of tilt mismatch is further demonstrated during phase 2. Some of the sensors appear to follow the bond head force profile more

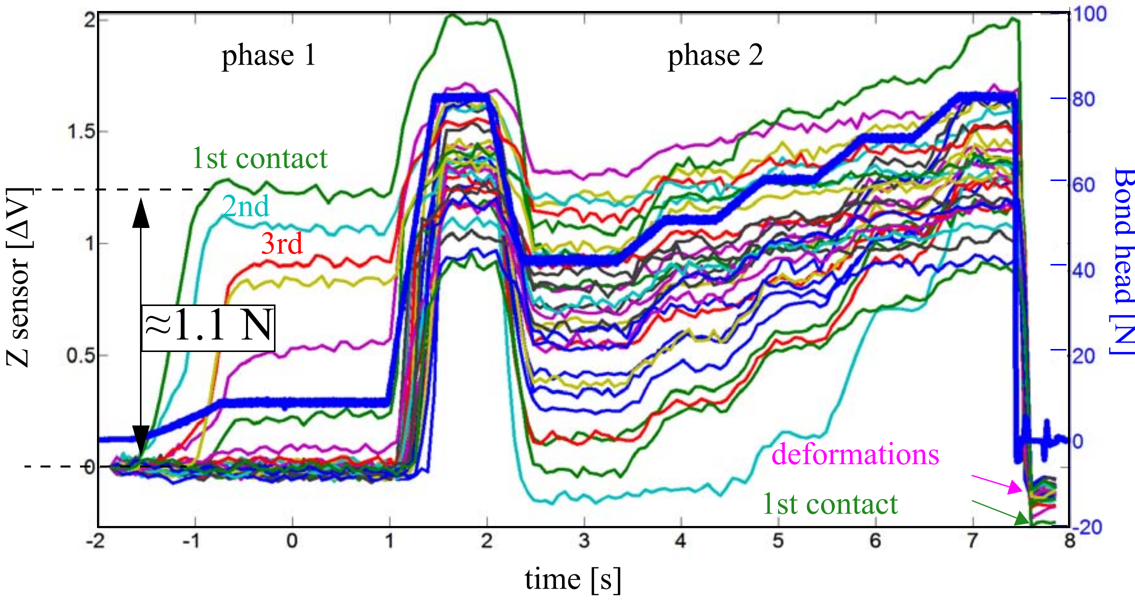


Figure 48:A multi-step force profile (bold blue) overlaid on top of 30 Z force sensor signals in time. The deltas are not all at an equal magnitude, agreeing with the non-parallel contact achieved in this. Bond head and chuck are held at constant 50 °C in this event.

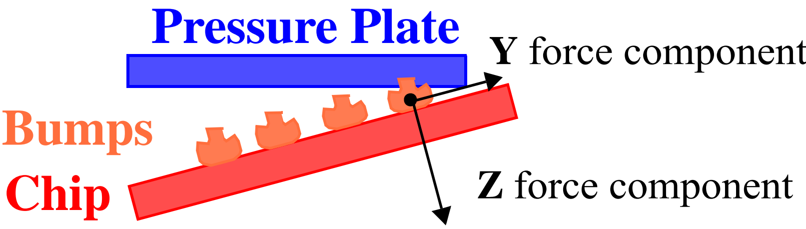


Figure 49:Tilt skews X and Y sensors. This information can also be used to detect chip tilt mismatch.The Y sensor effectively sees components of the Z force.

strictly than others. This is explained by some of these sensors not seeing load until sufficient net force is applied to make contact. If we had parallel contact, we would expect the Z signals to increase more similarly to each other with time.

Further effects of tilt caused some components of Z force to be detected by the XY sensors. Figure 49 illustrates the explanation that components of Z force are seen by the Y sensors when tilt is present.

6.2 Thermal Delay and Gradient

Figure 50 compares the known bond head temperature profile to the temperatures measured by the RTD sensors undergoing a heating experiment. In this data set, an 80 N profile is applied twice to the sensor array, resulting in press #1 with constant temperature at 50 ºC and press #2 with bond head ramping from 50 °C to 200 °C at a rate of 350 °C/s. The RTDs heat up with an approximate 1 s delay after the bond head ramp. The delay can be explained by the time it takes for the thermal energy to propagate from bond head down through the pressure plate and Au bumps to the top metal RTD sensors. There is also a gradient horizontally across the chip during the thermal

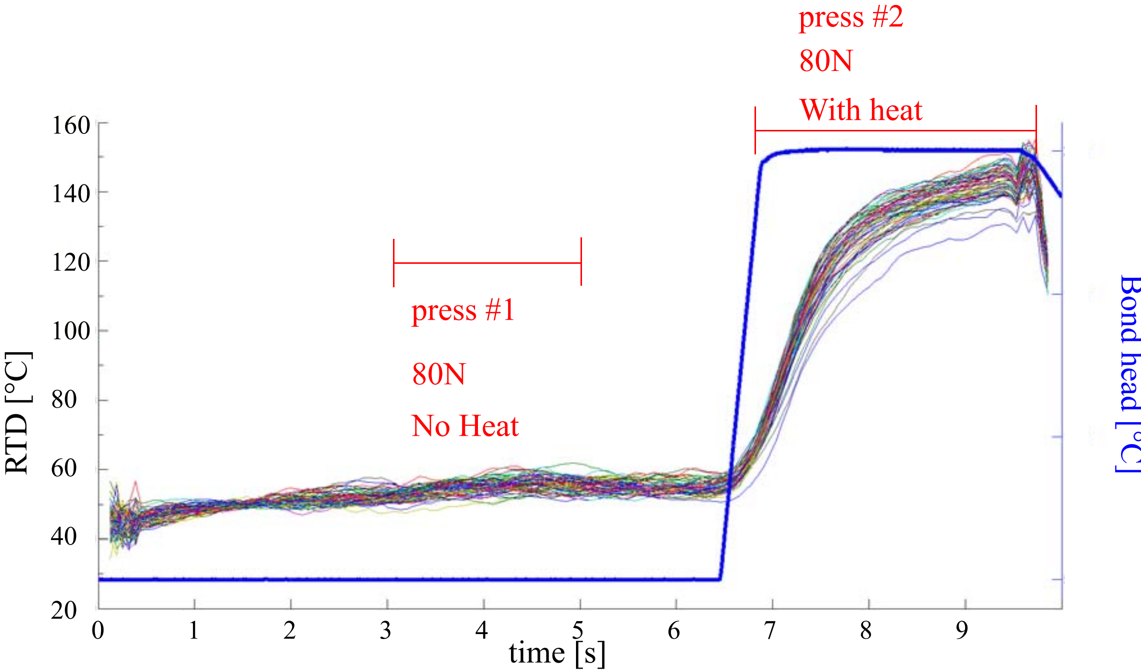


Figure 50:RTD values during a TCB emulation with bond head reaching 200°C.

ramp. The same tilt discussed in section 6.1 contributes to a thermal difference near 15-20 °C across the chip. Initially, conductive heat transfer only occurs with greater magnitude at the top right corner area of the chip where there is more force and thus more conductive contact reducing thermal contact resistance locally.

6.3 Thermal Expansion

Evidence of thermal expansion a characteristic X-Y stress pattern is seen in the data set presented in Figure 51. In this data set, two touchdowns are made, first 80 N without bond head heat followed by 80 N with bond head temperature ramping from 50 °C to 200 °C. During the force steady state (Figure 51 e,f,g,h) and force transient (Figure 51 i,j,k,l) the spacial distribution of force and temperature are artifacts of the pressure plate's contact only. Y tilt was dominant in our

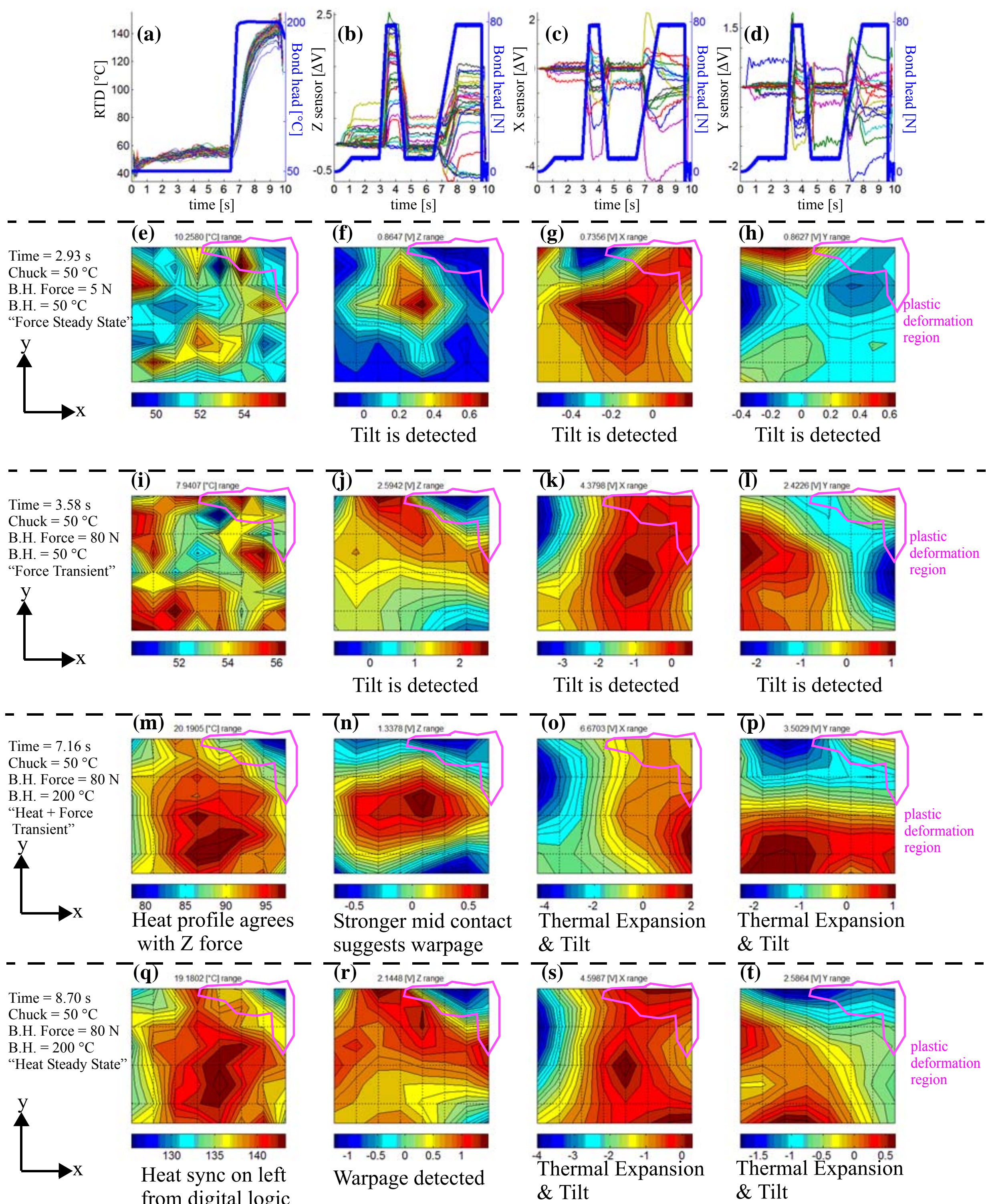


Figure 51: Plots (a,b,c,d), show sensor & bond head vs. time for RTD sensor, Z force, X force, Y force, respectively. Corresponding spatial visualizations for time = 2.93 s (e,f,g,h), time = 3.58 s (i,j,k,l), time = 7.16 s (m,n,o,p) and time = 8.70 s (q,r,s,t). Plastic deformation region denotes sensors that may have altered force sensitivities. We may have over coined those bumps, deforming them during tilt corrections and suspect we are not making good contact in that area as shown in

parallelism measurements taken with a microscope and the data in these events agrees. Stronger contact was established in the top regions which where physically higher.
At a later time, the heat and force transient (Figure 51 m,n,o, and p), force profiles are more symmetrical. In the Y force case, symmetry can be seen about the Y axis in Figure 51p which corresponds to the physical center of the Y axis. This is characteristic of thermal expansion, which is only expected when the system is under thermal stress. The tilt effect on the signal is still present, but thermal expansion components dominate.

The heat steady state (Figure 51 m,n,o, and p), exhibits properties from the force transient and the thermal transient cases. Thermal expansion and pressure plate are both contributing to the force signal. At this stage in the bond profile, the system is no longer rapidly heating up, and the pressure plate component of stress returns as the dominant contributor to the force signals.

It is worthwhile to discuss how heat propagates from the bond head through the system. We expect that the pressure plate heats and expands first due to the better thermal contact it has with the heat source (the bond head). In Figure 51 b,c and d there are overshoots in the signals immediately following the thermal and force transients. The force transient situation can be explained by the presence of tilt dominating the stress signals. The overshoot occurs because some of the bumps are contacted before others. These bumps experience a short lived period of greater force until the neighboring bumps are contacted, re-distributing the load over them.

The thermal transient's overshoot case however is more pronounced and exhibits greater absolute magnitudes. A 40% larger voltage range was measured in the thermal transient Y signals com-

pared to the earlier force transient or following heat steady state. This larger overshoot can be explained by an additional component of thermal expansion in the system. The pressure plate is heating up rapidly, faster than the sensor chip, and there is a short lived period where the system experiences a maximum thermal mismatch. Once sufficient time has passed for the heat to propagate down to the sensor chip, the differences in thermal expansion and resulting stress are relaxed. The period following the application of heat is measured as the most stressful part of the TCB emulation.

6.4 True Chip Boundaries

The positive signals in force event #2 of the X case are slightly dampened during thermal transient. This is explained by referring to the layout where an extra 1 mm area in the left was needed for digital logic and auxiliary wire bonds. Consequently we are measuring only one "true chip boundary" in the X case. The Y expansion case does not have such limitations and the Y force signal is more pronounced and symmetrical. The effect of the digital logic region is also seen in the temperature data. The extrusion of space acts like a heat sink on the West side during temperature transient and steady state.

6.5 Over Coined Bumps "Pancaking"

SEM images in Figure 14 show excessively deformed Au bumps on this sensor chip versus bumps from other regions on the sensor. We were iteratively using the Z signal as feedback with the addition of shims and software corrections to the bond head tilt. Earlier non-parallel contacts over-coined the top right region of the chip and caused those sensor bumps to experience massive plastic deformation or "pancaking". Thus, the sensitivity calibrations was rendered invalid and

the level of contact was substantially altered. The temperature data which would not be impacted by the bump deformations agrees, showing a corresponding cold spot in the same region.

The time of contact can be extracted from the stress sensor signals. Figure 15 shows the first time at which a 15% change was detected, visualizing all 64 XYZ force signals in space. This is further evidence that the top right region was over coined and support the tilt. The pressure plate is contacting the bumps in this region at later times, There is motivation for further development of this sensor and the experimental process.

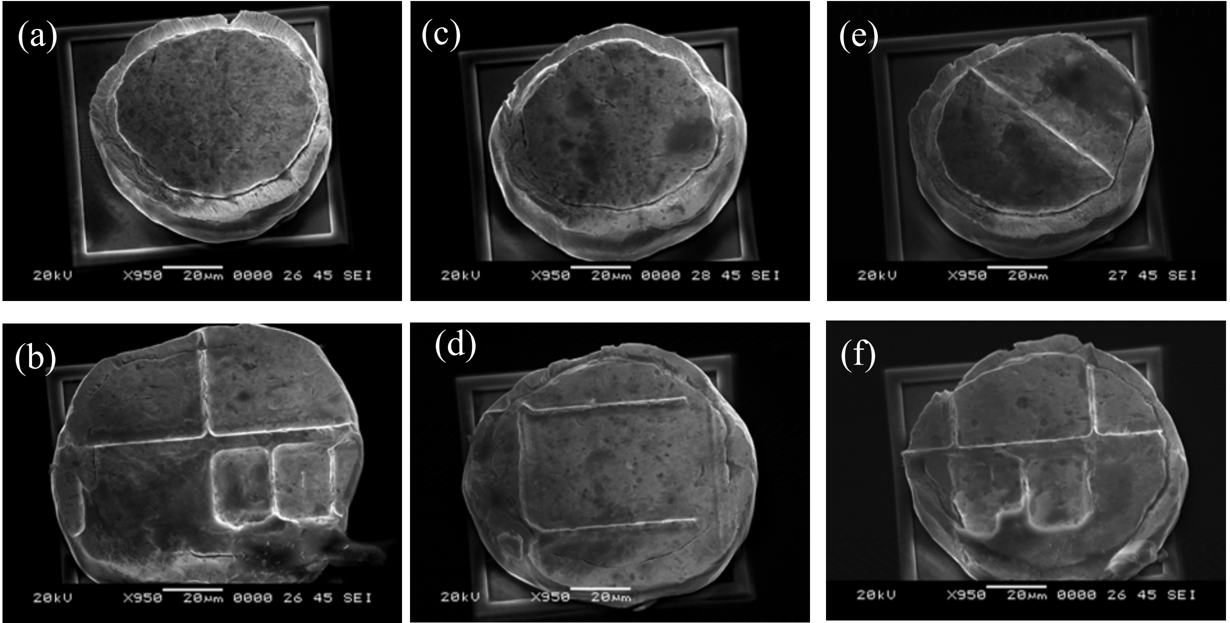


Figure 52:SEM of Au bumps after aprox. 40 TCB emulations of up to 100 N and 200°C. Normal bumps (a,c,e). Heavily deformed bumps (b,d,f) which correspond to the denoted region in Figure 53. The patterns on some of the bumps are from the 1-2 µm thick Al patterned pads on the pressure plate. It was in fact a reproposed wire bonding test chip with daisy chained Al pads.

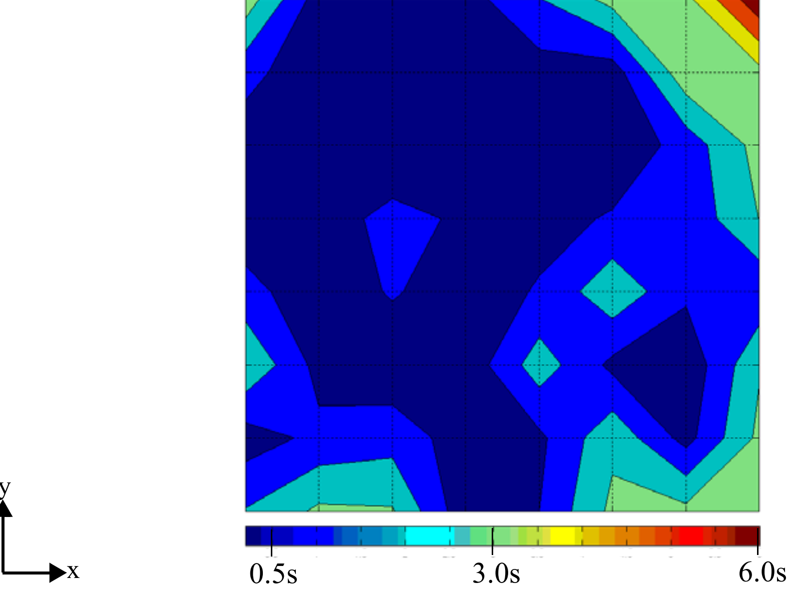


Figure 53:Spacial visualization of time when 15% change in 64 XYZ force signal was first detected. The top right region's bumps are over coined and deformed.

7 Conclusions and Outlook

A novel CMOS sensor array for in-situ measurement during an emulated flip chip event is developed. Procedures to setup, package and mount this new sensor design inside a flip chip machine are presented. An auxiliary wire bond recipe and procedure are developed deliver power and communicate with the chip while it is under a bond head during operation.

This new sensor chip is a reusable tool for non-destructive process studies to understand and improve existing flip chip methodologies. Applications such as tilt detection, thermal gradient characterization, and thermal expansion measurements are demonstrated. For this first time, as far as this author is aware, the effects of thermal expansion on a 3x3 mm chip are measured in-situ during a flip chip process with 200° C of heat applied with a sensor embedded locally at the flip chip bond sites. The thermal transient is measured as the most stressful period of this flip chip process, where the maximum thermal mismatch, and thus maximum stress occurs across the system.

Future work should look to further develop and improve the calibration procedure outlined in this manuscript. Harder bumps, perhaps Cu pillars, should be used to reduce plastic deformation effects to improve the reusability of the sensor chip. Other options for flip chip emulation can explore bumping the substrate / pressure plate instead of bond pads. Further development of the experimental setup is also needed. The importance of parallelism should not be underestimated. Shimming only allowed correction to the 10-20 µm / mm range which was not ideal for bumps in the order of 10-100µm in size. The alternative packages like the PCBs developed in this research can also help with parallelism.

References

[1] Harman, George. Wire bonding in microelectronics, 3/E. McGraw Hill Professional, 2009.
[2] Ulrich, Richard K., ed. Advanced electronic packaging. Wiley-Interscience/IEEE, 2006.
[3] Kim, Samuel. "Novel Methods in Ball Bond Reliability Using In-Situ Sensing and On-Chip Microheaters." (2013).
[4] Standard Test Methods for Destructive Shear Testing of Ball Bonds,Standard ASTM F1269-13, 2013.
[5] Wire Bond Shear Test Method, Standard EIA/JESD22-B116, 1998
[6] Bond Strength (Destructive Bond Pull Test),Standard MIL-STD-883E 2011.7, 1989.
[7] Xu, Di Erick, et al. "Thermal Aging Behavior of Fine Pitch Palladium Coated Silver (PCS) Ball Bonds on Al Metallization." International Symposium on Microelectronics. Vol. 2015. No. 1. International Microelectronics Assembly and Packaging Society, 2015.
[8] Laor, A., Herrell, P. J., Mayer, M., A Study on Measuring Contact Resistance of Ball Bonds on Thin Metallization, (2015) IEEE Transactions on Components, Packaging and Manufacturing Technology, Volume:5 , Issue: 5, pp. 704 - 708.
[9] Blish, R. C., and L. Parobek. "Wire bond integrity test chip." Reliability Physics Symposium, 1983. 21st Annual. IEEE, 1983.
[10] Effect of Au ball bond geometry on bond strength and process parameters, and assessing reliability on Al bond pad using integrated stress sensors
[11] McCracken, Michael James, et al. "Explaining nondestructive bond stress data from high-temperature testing of Au-Al wire bonds." Components, Packaging and Manufacturing Technology, IEEE Transactions on 3.12 (2013): 2029-2036.
[12] Mayer, Michael. "Microelectronic bonding process monitoring by integrated sensors." (2000) PhD thesis, Technische Wissenschaften ETH Zürich, Nr. 13685; also: Hartung-Gorre, Konstanz, Germany, ISBN 3 89649 620 4, 2000.
[13] Daniel Bolliger Michael Mayer Oliver Paul Zeno Stössel, "Process and chip for calibrating a wire bonder", European Patent Application EP0953398A1, 1999.
[14] Schwizer, J., Mayer, M., Brand, O., & Baltes, H. (2001). Analysis of ultrasonic wire bonding by in-situ piezoresistive microsensors. Proc. Transducers ‘01/Eurosensors XV, 1426-1429.
[15] Schwizer, Jürg, Michael Mayer, and Oliver Brand. Force sensors for microelectronic packaging applications. Springer Science & Business Media, 2006.
[16] McCracken, Michael, et al. "Symmetric miniaturized heating system for active microelectronic devices." Review of Scientific Instruments 81.7 (2010): 075112.
[17] Mayer, Michael, Oliver Paul, and Henry Baltes. "In-situ measurement of stress and temperature under bonding pads during wire bonding using integrated microsensors." Proc. 2nd Int. Conf. Emerging Microelectr. and Interconn. Technol. EMIT. Vol. 98. 1998.
[18] M. Mayer, J. Gomes, "Accelerating Reliability Assessment with Multi-Oven Racks and Sensor Chips for Wire Bonds", Presentation at IMAPS New England 42nd Symposium and Expo, Boxborough, MA, USA, May 5th 2015
[19] Qin, I., et al. "Effect of process parameters on pad damage during Au and Cu ball bonding processes." Electronics Packaging Technology Conference, 2009. EPTC'09. 11th. IEEE, 2009.
[20] Ebersberger, Bernd, and Charles Lee. "Cu pillar bumps as a lead-free drop-in replacement for solder-bumped, flip-chip interconnects." Electronic Components and Technology Conference, 2008. ECTC 2008. 58th. IEEE, 2008.

[21] Gerber, Mark, et al. "Next generation fine pitch cu pillar technology—enabling next generation silicon nodes." Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st. IEEE, 2011.
[22] Elenius, Peter, and Lee Levine. "Comparing flip-chip and wire-bond interconnection technologies." Chip Scale Review 4 (2000): 81.
[23] Shackelford, James F. Solutions Manual: Introduction to Materials Science for Engineers. Macmillan, 1985.
[24] Ebersberger, Bernd, and Charles Lee. "Cu pillar bumps as a lead-free drop-in replacement for solder-bumped, flip-chip interconnects." Electronic Components and Technology Conference, 2008. ECTC 2008. 58th. IEEE, 2008.
[25] Shannon, Claude E. "Communication in the presence of noise." Proceedings of the IRE 37.1 (1949): 10-21.
[26] Jan, M. Rabaey, Chandrakasan Anantha, and N. Borivoje. "Digital Integrated Circuits–A Design Perspective7." (2002).
[27] Huang, Y., Shah, A., Mayer, M., Zhou, N. Y., & Persic, J. (2010). Effect of ultrasonic capillary dynamics on the mechanics of thermosonic ball bonding. Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on, 57(1), 241-252.