Silicon Nanowire Based Photodetectors: Modeling and Fabrication

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

This research is focused on investigating the role of silicon nanowires in designing high gain, high sensitivity photodetectors, and is based on both device modeling and fabrication. We demonstrate that the superior electrostatic control within the nanowires enables us to effectively engineer the energy band and design novel photodetector architectures. This is due to the high surface to volume ratio in nanowires which allows for the ability to change the electrical properties of a nanowire device in response to a voltage applied to the gate contact.

In the first part of the thesis, two photodetector geometries are proposed and theoretically studied. The first geometry is a Metal Oxide Semiconductor (MOS) device with nanowires incorporated in its channel. The next geometry is a junction-less phototransistor, e.g. a photo-conductor with a third terminal as the gate. Both geometries are important due to their ability to generate optical gain. For both cases, first the role of nanowire parameters and their pros and cons on the device photo-response is investigated. Afterwards, we propose modifications to the device geometry in order to improve the performance of the device in terms of optical gain and sensitivity.

The first modification is allocating a wide region for light absorption in the channel, since single nanowire based photodetectors suffer from lack of efficient absorption, due to their small cross sectional area. Use of phototransistors also helps the photocurrent increase, due to the device's internal gain. The second modification incorporates two nanowire/ gate geometries to improve the device photo-response, in terms of both dark- and photo-current. The charge flow in each nanowire is controlled by a gate, which changes the energy band within the nanowire. This band engineering allows for both increasing the optical gain of the phototransistor, and keeping the dark current low. We report nanowire based phototransistors that are potentially able to detect low levels of light intensity (photon rate of less than $50s^{-1}$).

The second part of the thesis is devoted to the fabrication of the nanowire based structures. Top-down approach is used, mainly due to the better control on the nanowire size and position, and repeatability of the processes involved. Fabrication process includes several steps of electron

beam lithography, dry and wet etching, metal and dielectric deposition and annealing. Pre-developed recipes are used when available. New recipes are also developed to better suit the specific needs of the devices. The measurement results of the fabricated structures verify most of the concepts proposed in the modeling phase.

In the third part of this thesis, we characterize MOS capacitors with and without illumination, based on Silicon on Insulator (SOI) structures used in the previous chapters. Here, we report the first observation of photon induced negative capacitance in a conventional Metal Oxide Semiconductor (MOS) capacitor without the use of ferroelectric materials. Design and implementation of this phenomenon is presented in a capacitor where an aluminum oxide layer serves as the gate dielectric, and the capacitor is in depletion mode. Through extensive modeling, we establish that trap states at the semiconductor-oxide interface, coupled with the injection of photo-generated electrons are responsible for the negative capacitance. We find that varying the trap density and/or light intensity can tune the value of the negative capacitance. We show that in the presence of photons, the experimentally measured quasi-static capacitance in depletion is almost twice the value without photons. Further, the measured capacitance is larger than the values in accumulation and inversion.

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To *Daryoush*

and to my parents:

Aghdas Asrar and *Bahram Fadavi*

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List of Abbreviations

ALD	Atomic Layer Deposition
APD	Avalanche Photodiode
APS	Active Pixel Sensor
BOX	Buried Oxide
BHF	Buffered Hydrofluoric acid
CCD	Charge Coupled Device
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nanotube
CT	Computerized Tomography
DUT	Device Under Test
FF	Fill Factor
FPN	Fixed Pattern Noise
GND	Ground
HBT	Heterojunction Bipolar Transistor
HF	Hydrofluoric acid
HMDS	hexamethyldisilazane
I^2E	Impact Ionization Engineering
ICPRIE	Inductively Coupled Plasma Reactive Ion Etch
IPA	IsoPropyl Alcohol
MIBK	Methyl IsoButyl Ketone
MIS	Metal Insulator Semiconductor
MOS	Metal Oxide Semiconductor
MRI	Magnetic Resonance Imaging
NEP	Noise Equivalent Power
PMGI	Polymethylglutarimide
PMMA	Poly(methyl methacrylate)
PMT	Photomultiplier

PECVD	Plasma Enhanced Chemical Vapor Deposition
PPS	Passive Pixel Sensor
QSCV	Quasi-Static Capacitance-Voltage
RF	Radio Frequency
RTA	Rapid Thermal Annealing
SC-1	Standard Clean 1
SC-2	Standard Clean 2
SEM	Scanning Electron Microscope
SMU	Source Monitor Unit
SOI	Silicon on Insulator
SOS	Silicon on Sapphire
SRH	Shockley Read Hall

Chapter 1

Introduction

Photodetectors are abundantly found in scientific and industrial instrumentations, consumer products, and even household appliances. Different members of this family detect a wide frequency range from Terahertz and far infrared up to gamma rays, and operate at different speeds [1]. Automatic door openers and household remote controls for example, are rather slow and less sensitive detectors that normally work in the infrared and microwave range [2–4]. Optical communication sensors on the other hand, require extremely fast and highly sensitive detectors to receive a large capacity of information in infrared spectrum (wavelength: 1.3μm and 1.55μm) [5–8]. In the field of astronomy the wavelength range is quite vast, from sub-millimetre far infrared up to very high energy X- and gamma rays; and also in some cases, the device must be capable of detecting a single photon. This wide frequency range requires different types of detectors [9–12]. Process controls in factories need detectors in the range of either infrared or UV, based on the type of application. They might be used in a simple position sensor or an intensity meter, or a more complicated imaging system. Photodetectors are also being widely used in television and cable broadcasting systems and digital cameras, as well as in biomedicine and military applications [1, 13–15].

Photoelectric emission and photon absorption in semiconductors are both quantum events. Both require a minimum level of photon energy which depends on the band-structure of the material, as well as the type of absorption (inter- or intra- band) [16]. During photoelectric emission, that takes place in vacuum photodiodes and photomultipliers (PMT), the absorbed light in a metal excites the electrons and gives them enough energy to overcome the surface barrier potential and escape from the metal surface. The emitted electrons in photomultipliers are then accelerated by a series of electrodes to create secondary electrons [16]. This gives PMTs the ability of detecting very weak signals. In fact, some PMTs are able to detect a single photon.

They are however expensive and usually bulky devices that require very high voltages (in the range of kV) [17]. Even the most recent fingertip size device, known as μPMT, operates at 900V [18].

In semiconductors, on the other hand, the absorbed photon can give enough energy to an electron to jump from the valance band into the conduction band. The photo-generated electron-hole pairs would in turn change other properties of the semiconductor, such as its conductivity, which can be observed in the device output terminals by measuring the output current or voltage [1, 16].

Research on enhancing the performance of photodetectors is still in progress. Designing photodetectors that consume less power, or operate faster, or improving photodetector designs to detect lower light intensities are examples of the research areas. Exploring the use of nano-structures such as carbon nanotubes (CNT), silicon and germanium nanowires is also actively pursued by different groups around the world [19–21]

This chapter is devoted to the introductory review of semiconductor based photon detectors and details about their operation. First we explain the concept of inter-band photon absorption in semiconductors and then briefly introduce the important sources of noise and figures of merit in such devices to facilitate comparing different structures together. Next, the two mainstream technologies of imaging industry, Charge Coupled Devices (CCD) and Complementary Metal Oxide Semiconductor (CMOS) devices, are introduced and their advantages and disadvantages are discussed. Finally, a selected family of photodetectors, specifically those with nanowires within their geometry, are explained and different aspects of their performance are discussed and compared together.

1.1 Absorption of Light

Part of the light that strikes a semiconductor is reflected due to the difference in the refractive indices of the air and the semiconductor material. The penetrating part excites the atoms and creates electron-hole pairs inside the semiconductor, provided that the light wavelength is larger than the semiconductor bandgap. It is possible to obtain the optical power of the incident light at a depth x inside the semiconductor, by solving the decaying equation described by Beer-Lambert Law $\frac{d}{dx}P_{opt}(x) = \alpha P_{opt}(x)$, where $P_{opt}(x)$ is the optical power at position x, and α is the material absorption coefficient [1]. The solution is exponential, as shown below. The surface reflection R is also included, and P_{in} denotes the optical power at the interface x=0.

$$P_{opt}(x) = (1 - R)P_{in}e^{(-\alpha x)} \qquad (unit : W) \qquad (1.1)$$

The photo-generation rate $G_L(x)$ (unit: $(cm^3s)^{-1}$) is then obtained by derivation of the optical power.

$$G_L(x) = \frac{-1}{Ah\nu}\frac{d}{dx}P_{opt}(x) = (1-R)\frac{P_{in}}{A}\frac{1}{h\nu}\alpha e^{(-\alpha x)} \tag{1.2}$$

In equation 1.2, A is the total area that light is shining through; and h and ν are the Planck constant and the frequency of the light, respectively [1]. Please note that $P_{opt}(x)$ is substituted from equation 1.1. Assuming the semiconductor thickness is D, one can calculate the average of the photo-generation rate, $\bar{G}_L$.

$$\bar{G}_L = (1-R)(1-e^{-\alpha D})\frac{P_{in}}{AD}\frac{1}{h\nu} \tag{1.3}$$

Equations 1.2 and 1.3 both put a limit on the semiconductor thickness. The exponential term suggests that in order to convert most of the photons into carriers, the thickness of the absorbing layer must be at least greater than α^{-1}. The absorption coefficient α strongly depends on semiconductor bandgap energy, bandgap type (direct or indirect), wavelength of the incident light, and also the symmetry of the electronic states at conduction and valance bands.

1.2 Noise in Photodetectors

Noise is a randomly varying signal observed at the output of all electrical circuits, regardless of the existence of any signal at the input. In a photodetector, it affects the device performance by limiting the weakest source of radiation that can be detected. This detection limit is specified by a figure of merit called detectivity (defined later in this chapter). Noise originates from the optical source, the photodetector itself, or even the circuit which later amplifies the electric signal [1]. Assuming that $I_n(t)$ is the random process representing the noise current as a function of time t, the noise power can be defined as [22].

$$< I_n^2 >= \lim_{T\to\infty}\int_{-T}^{T}I_n^2(t)dt \qquad (unit:A^2) \tag{1.4}$$

Shot Noise

This type of noise originates from the discrete nature of photons and carriers that generate the current in a device. As the time passes, photons impinge the detector in a random manner rather than at uniformly spaced time intervals. Similarly, the number of carriers passing through the device electrodes fluctuates over the time, and as a result of this randomness, the device current shows some fluctuations. The shot noise can be calculated as [1]

$$< I_{sh}^2 >= 2qIB \tag{1.5}$$

where q is the electron charge and I is the average current passing through the device; and B represents the frequency bandwidth of operation, which is normally determined by the receiver bandwidth.

Generation-Recombination Noise

The rate of carrier generation, either thermal or optical, and also the rate of carrier recombination are both random processes, resulting in fluctuations in carrier concentration. The noise that originates from thermal generation depends on the material bandgap; for bandgaps close to k_BT (k_B: Boltzmann constant, T: temperature) the generation-recombination noise can be quite large, unless the device is used at low temperatures [16]. Generation-Recombination noise is the main noise source in photoconductors. The noise power within the frequency range f to $f + \Delta f$ can be calculated as [16]

$$< I_{GR}^2 >= \frac{4qIG}{1 + (2\pi f \tau_c)^2} \Delta f \tag{1.6}$$

In equation 1.6, I denotes the total current; and τ_c and G are the minority carrier lifetime and the photoconductor gain, respectively. The expression shows that noise is almost frequency independent at low frequencies when $f \ll (2\pi\tau_c)^{-1}$; otherwise it decreases with frequency.

Thermal (Johnson) Noise

This type of noise originates from the random velocity of electrons in a resistor. The random motion of electrons creates small fluctuations in the potential (and therefore the current) of the resistor, that is present even when no external voltage is applied. At the frequency bandwidth B smaller than $\frac{k_BT}{h}$ (h is the Planck constant), thermal noise can be written as [16]

$$< I_T^2 >= \frac{4k_BTB}{R} \tag{1.7}$$

where R is the resistance. As revealed from its name, thermal noise increases at higher temperatures due to the increased random motion of electrons.

Flicker $(1/f)$ Noise

Flicker noise is not very well understood. It is believed that this noise is due to the random distributions of the traps in semiconductors. The power spectrum of flicker noise shows an inverse dependency on frequency [16]. At higher frequencies this noise is much lower than thermal noise and can be ignored. The flicker noise power is [23]:

$$< I^2_{(1/f)} >= \frac{K I^\alpha_B B}{f^\beta} \tag{1.8}$$

In equation 1.8, K is a constant; and I_B and f are the bias current and the operating frequency, respectively. The two other parameters, α and β depend on device characteristics [23].

The overall noise in a linear system is the sum of the noise sources. Assuming the noise sources are uncorrelated, then the overall noise power, or $< I^2_n >$, is simply a summation over the noise powers [22].

$$< I^2_n >=< I^2_{sh} > + < I^2_{GR} > + < I^2_T > + < I^2_{(1/f)} > \tag{1.9}$$

1.3 Figures of Merit in Photodetectors

Figures of merit, the quantities that help to characterize the performance of a device, allow us to compare different photodetectors together. Some of the most important figures of merit of photodetectors are introduced in this section.

Responsivity (R)

The responsivity of a photodetector is defined as the ratio of the photocurrent I_{ph}, to the optical power.

$$R = \frac{I_{ph}}{AP} \qquad (unit : AW^{-1}) \tag{1.10}$$

The photocurrent I_{ph} is generated by a light source with intensity of $P(W cm^{-2})$ that is shined through a window with area A (The optical power $P_{opt} = PA$) [1].

External Quantum Efficiency (η_e)

This parameter determines the number of collected carriers per each incident photon. Quantum efficiency, η_e, is defined

$$\eta_e = \frac{\frac{I_{ph}}{q}}{\frac{P_{opt}}{h\nu}} = R\frac{h\nu}{q} \qquad (unit:1) \qquad (1.11)$$

In equation 1.11, q is the electron charge, R is the responsicvity, and $h\nu$ denotes the photon energy [1].

Noise Equivalent Power (NEP) and Detectivity

NEP determines the minimum incident power that the device is able to detect. It is defined as the power of the optical signal that creates a signal to noise ratio of 1 at the detector output [23]. The signal power P_{opt} can be described as the photocurrent divided by responsivity (equation 1.10). Substituting the photocurrent with the root mean square (r.m.s) of the noise or $<I_n^2>^{0.5}$, based on definition of NEP, one finds [1, 23]

$$NEP = \frac{<I_n^2>^{0.5}}{R} \qquad (unit:W) \qquad (1.12)$$

The inverse of NEP is called detectivity (unit: W^{-1}) which in fact shows the device ability in detecting small optical signals [1].

1.4   Imagers: CCD versus CMOS

Photodetectors are widely used in digital imaging devices. Imagers are found in a variety of applications including wireless handheld devices, scanners and fax machines, biometrics and medical devices as well as industrial, security and household cameras. There are two leading technologies in manufacturing image sensors: Charge Coupled Device (CCD) and Complementary Metal Oxide Semiconductor (CMOS) technologies; and although both of them were introduced almost at the same time in the late 60s and early 70s, CCDs won the competition for years, mostly due to the limitations of lithographic techniques required for fabricating CMOS based sensors [14, 24].

In a typical CCD or CMOS imager, photons are first collected by a lens and then passed through filters for wavelength discrimination. Next, a detector converts the absorbed photons to
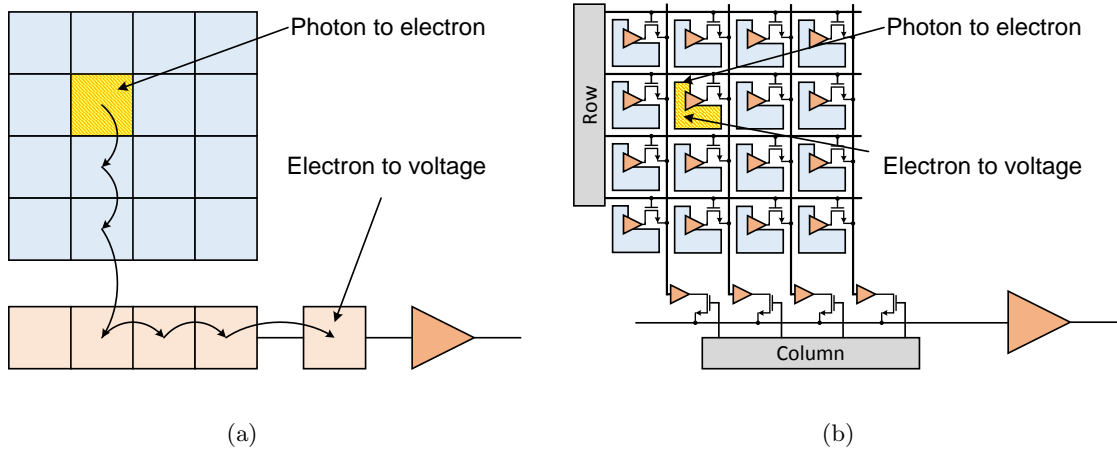
Figure 1.1: Block diagram of (a) a CCD imager; and (b) a CMOS imager [14].

electrons; the electrons are later read, amplified and converted to a digital signal. Other circuit blocks are used for timing, signal processing and controlling the system [25].

The block diagrams of CCD and CMOS image sensors are shown in figures 1.1(a) and (b), respectively [14]. Both image sensors are composed of several metal-oxide-semiconductor pixels in which the charge (resulted as the conversion of photons to electrons) is accumulated. The readout process in a CCD sensor is such that the accumulated charge in each pixel is transferred sequentially to a common output; where it is converted to voltage. The voltage is then buffered and sent out of the imager. In a CMOS imager on the other hand, the photo-generated charge is converted to voltage in each pixel. The voltage at the pixels is then accessed via row-column matrix selection techniques, which is buffered and sent off chip [24]. As a result, the complexity of the sensor in a CMOS imager is higher in comparison with a CCD imager.

The photodetector in a CCD imager is in fact a Metal Oxide Semiconductor (MOS) capacitor. Assuming the semiconductor is p-type, a positive voltage on the gate contact creates an electric field that creates a depletion region. When illuminated, the photo-generated pairs are separated as a result of the electric field; and the electrons get trapped in the potential well created under the gate. The trapped charge, which is proportional to the number of the absorbed photons, is then sequentially transferred along a line of detectors by applying a programmed voltage sequence to the gates. As pictured in figure 1.2 [16], the charge is first accumulated underneath the positively biased gate G_i, while the adjacent gate G_{i+1} is zero biased. Now, if G_{i+1} is biased positively, the charge would be shared between the two gates. Next G_i is zero biased while G_{i+1} is still positive; this way the charges is transfered and accumulated under G_{i+1}. The sequence is repeated by
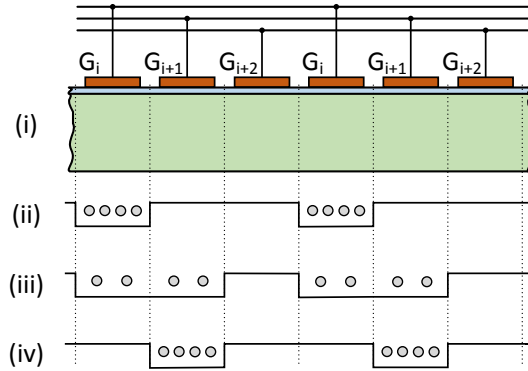
Figure 1.2: Read out process in a CCD imager. (i) Line of detectors; VG_i is positive; gates G_{i+1} and G_{i+2} are zero biased and screened from the light. (ii) Charge is trapped under G_i. (iii) VG_{i+1} is positive and charge is shared between G_i and G_{i+1}. (iv) VG_i is zero and charge is moved under G_{i+1} now [16], page 297.

appropriately biasing the gates, until the charge is transferred to the end of the line [16].

The pixels designed for CMOS imagers usually belong into two categories: Passive Pixel Sensors (PPS) and Active Pixel Sensors (APS). PPS sensors, which were introduced first, are composed of a photodiode and a transistor for row-column addressing. The charge integrated in the photodetector is read via connection of the row and the column buses when the row signal is selected. The photodetector is then reset by opening the row select transistor. The advantage of a PPS sensor is that only a small area of the pixel is devoted to the readout circuitry. The drawback is that connecting a small capacitance pixel to a larger capacitance bus reduces the amount of charge transfer and degrades the sensitivity and performance of the sensor [17, 26].

APS sensors contain a buffer in each pixel to improve the signal-to-noise ratio of the sensor. However, increasing the pixel circuitry leads to a smaller area for the detector itself, which reduces the fill factor (FF). In addition, the possible non-uniformity of the buffer transistors in different pixels introduces a noise, called Fixed Pattern Noise (FPN) [17, 26]. Two of the most important photodetectors that are used in CMOS pixels are photodiodes (for mid-low performances) and photogates (for higher performance applications demanding a lower noise) [26].

Different read out methods in CCD and CMOS imagers result in certain advantages and disadvantages in comparison with each other. CCDs are normally superior in case of fill factor, dynamic range, noise, and uniformity due to their simpler structure and lower level of noise [17, 24]. CMOS imagers on the other hand consume much lower power due to the use of a single, low bias voltage source [26, 27]. In terms of speed, CMOS imagers are also the winners; as the entire camera

functions can be placed on the image sensor [24]. Another capability of CMOS imagers comes from the readout method of these imagers that allows for easy access to all pixels. CCDs generally have difficulties in providing this property [24, 27]. Over-exposure can also create blooming effect in CCDs, where the extra charge generated by intense light spreads out, and the resulting image shows a larger exposed area [28]. While CMOS imagers are naturally immune to blooming effect, suppressing this problem in CCDs usually comes at the price of reducing the fill factor [24, 27].

Since the overall quality of the images from CCDs is superior than those from CMOS imagers, one can find CCD imagers in high end applications such as digital photography and high performance industrial, scientific and medical imaging [24, 27]. CMOS imagers are also found in high performance professional and industrial cameras. However, they can mostly be observed in applications with lower image quality demands, such as security cameras, wireless hand-held devices, scanners, fax machines, and toys [24].

1.5   Photoconductors

Among the photons that strike a semiconductor, those with energy of greater than semiconductor bandgap can give enough energy to the valance band electrons and move them into the conduction band. The photo-generated carriers increase the semiconductor conductivity; and this is the basic operating mechanism in photoconductors. The photoconductor can be simply placed in series with a load resistance. The change in the device conductivity (as a result of illumination) changes the voltage across the load resistance, which can be detected by a high impedance voltmeter [1,16].

When illuminated, the total current that passes through a lightly doped semiconductor can be easily calculated. The photoconductor of figure 1.3 is p-type with length, width and thickness of L, W and D, respectively. Under illumination, the current passing through the device is [1]

$$I = q(n_0\mu_n + p_0\mu_p)\frac{WD}{L}V + q(\mu_n + \mu_p)G_L\tau_n\frac{WD}{L}V \qquad (1.13)$$

In equation 1.13, q represents the electric charge; μ_n (μ_p) and n_0 (p_0) are the electron (hole) mobility and the initial electron (hole) concentration, respectively. τ_n is the minority carrier life time, and V represents the voltage applied to the device.

The first term in equation 1.13 represents the dark current of the photoconductor, where $q(n_0\mu_n + p_0\mu_p)$ is its conductivity. The conductivity of a photoconductor can be quite large even in the absence of a light source. As a result, the device generates a high level of dark current, which is perhaps the most important disadvantage of photoconductive detectors [1].
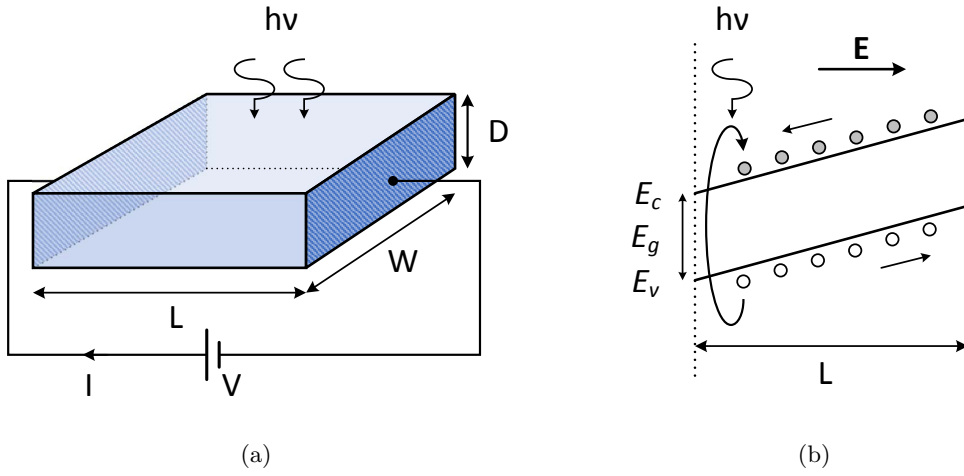
Figure 1.3: (a) A photoconductor with length L, width W and thickness D. (b) The photo-generated electron-hole pairs drift towards the contacts in response to the electric field.

The second term in equation 1.13 is the device photocurrent, where G_L can be replaced from equation 1.3. Comparing the device photocurrent with the primary photocurrent $q(WDL)G_L$ [1] shows that photoconductors are in fact detectors with optical gain.

$$G = \frac{I_{photo}}{qWDLG_L} = (\mu_n + \mu_p)\tau_n \frac{V}{L^2} \tag{1.14}$$

The photoconductive gain, G, is proportional to the ratio of the recombination time, to the transit time $(L^2/(\mu V))$. G represents the number of electrons or holes that are collected per impinging photons and can be greater than one. The fact that one can obtain gain from such simple structures is perhaps the most important advantage of photoconductors. A shorter device (smaller L) or a larger applied voltage V would help G to increase; keeping in mind that there is a maximum limit for this, due to the saturation of the electric field. Increasing the carrier lifetime will improve the gain as well; the drawback is that the response time of detector will also increase, which may result in a poor transient response [1, 16].

Materials with different bandgaps are used in photoconductor design to cover different wavelengths. Cadmium sulphide (CdS) and cadmium selenide (CdSe), for example are used to detect visible light [29, 30]. Lead sulphide (PbS), lead telluride (PbTe) and lead selenide can detect near-infrared wavelengths from 1 to 7 μm [31]. Indium antimonide (InSb), and doped semiconductors such as germanium (Ge) with a light doping of boron (B), beryllium (Be) or gallium (Ga)

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[1]It is assumed that all of the photo-generated pairs are converted into carriers [1].

can be used to detect longer wavelengths. These long wavelength detectors, useful for applications like infrared astronomy, normally operate at low temperatures to the reduce background noise [16, 32, 33].

1.6 Photodiodes

As discussed earlier, the main drawback of photoconductors is their large level of dark current. This disadvantage encourages people to use junction photodetectors [1]. This section briefly reviews the photodiodes.

1.6.1 *pn* Junction Photodiodes

When a *pn* junction diode (figure 1.4(a)) is illuminated by a light source, electron-hole pairs are generated inside the device. The pairs that are created in the depletion region are separated and drifted by the electric field. These carriers diffuse into the quasi-neutral regions and together with other carriers that are generated in the quasi-neutral regions, contribute to the device photocurrent. Assuming a one dimensional device biased at voltage V, and also a uniform photo-generation rate G_L, one can write the carrier continuity equations in the quasi-neutral regions for minority carriers under steady state conditions, to obtain the device current under illumination [2] [1, 16]

$$I = I_0(e^{q\frac{V}{k_B T}} - 1) - qAG_L(L_n + L_p + W) \tag{1.15}$$

In equation 1.15, q represents the carriers charge and A is the diode cross sectional area. L_n and L_p are the diffusion lengths on *p*- and *n*- side, respectively; and W is the depletion width. k_B is the Boltzmann constant and T is the temperature. The first term in this equation is independent of illumination; it represents the device dark current which is normally kept low by reverse biasing the device. In the second term, the photocurrent, the depletion width W creates an unfavourable dependence on the applied voltage. However, if W is kept very small in comparison with $L_n + L_p$, the photocurrent will be independent of the voltage, as plotted in figure 1.4(b). It is however important to note that unlike the photocurrent originating from the depletion region, the photocurrent from the quasi-neutral regions has a diffusive nature and therefore a much slower time response. The junction capacitance of the structure can slow down

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[2]The equation is simplified under the assumption of low level injection in the quasi-neutral region. The quasi-neutral region is assumed to be longer than the minority carrier diffusion length.

(a)   (b)
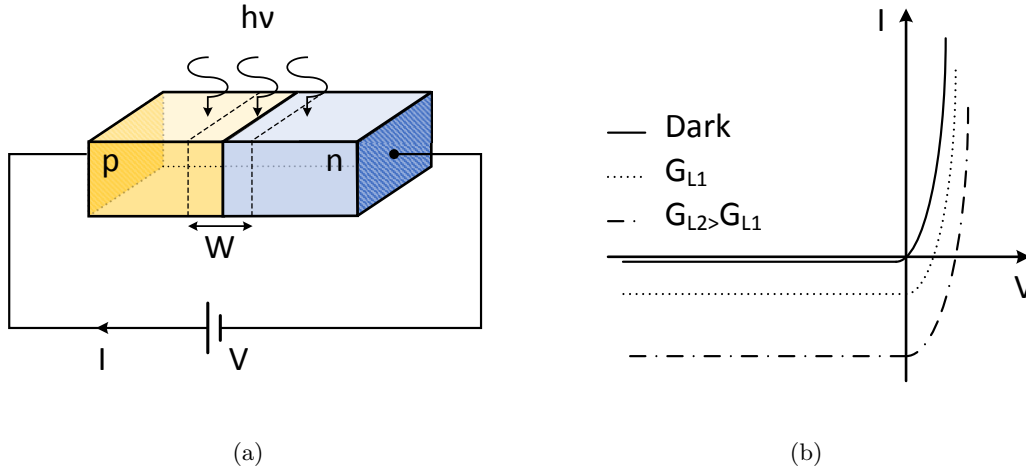
Figure 1.4: (a) A *pn* junction photodiode biased at a DC voltage V. (b) Device current versus applied voltage under different light intensities.

the device response even more. As a result, *pn* junction photodiodes are not good candidates for high speed photo-detection applications [1, 16]. In addition, only those electron-hole pairs that are in an average distance of L_n on the *p*-side, and L_p on the *n*-side can contribute to the photocurrent. If the diode is longer than $L_n + L_p$, the rest of the photo-generated pairs will eventually recombine [1].

1.6.2   *pin* Junction Photodiodes

To speed up the operation of photodiodes, an intrinsic region is placed between the *p* and *n* regions as the major absorption Layer. The resulting device, called *pin* photodetector, is reverse biased so that the intrinsic region is entirely depleted. Figure 1.5(a) shows a typical structure used as a *pin* photodetector. The ultimate goal is to ensure that the light is mostly absorbed in the undoped *i*-layer. Therefore when possible, the p^+ layer is made from a material that is transparent to the wavelength range aimed to be detected [3]. Similar to *pn* junction photodiodes, the photocurrent in a *pin* detector is composed of two parts; this time however the primary current is determined by carriers drift in the depletion region, as shown in figure 1.5(b). The secondary part of the photocurrent (that is usually negligible) comes from the carriers generated in the quasi-neutral regions; specifically the bottom *n* layer if the top *p* region is transparent. Assuming a light source with intensity of P and frequency of ν is illuminated over a *pin* detector

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[3]In the actual *pin* photodiodes the layers are stacked on top of each other. The p^+layer is above the intrinsic layer and the light comes from the top.
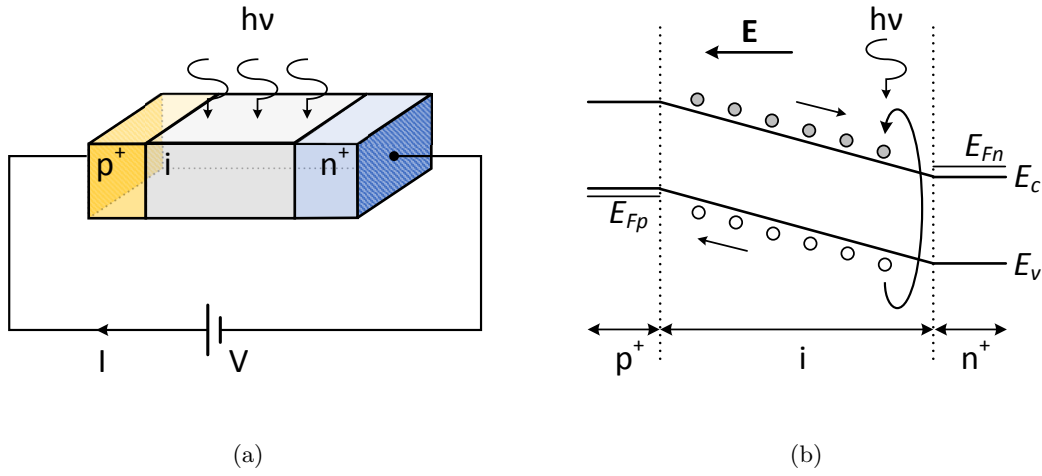
Figure 1.5: (a) A *pin* Photodiode. (b) Energy band diagram of the photodiode; most of the photons are absorbed in the intrinsic region.

with cross sectional area of A and depletion width of W, the total photocurrent due to the absorption in the intrinsic region can be obtained from equation 1.16 [1].

$$I = -q\frac{PA}{h\nu}(1 - e^{-\alpha W}) \tag{1.16}$$

where α is the absorption coefficient. Similar to *pn* junction photodiodes, in a *pin* photodetector each photon is able to generate at most one electron-hole pair, and the optical gain is never greater than one. However, since the intrinsic region in a *pin* photodiode is normally chosen to be longer than the carriers' diffusion lengths, the dominant component of the total photocurrent is determined by drift of the photo-generated carriers in the intrinsic region, resulting in a fast responding photodiode.

pin photodetectors are made of different materials to detect different wavelengths. Silicon (or Germanium for longer wavelengths) detectors are good for low speed communication applications such as local area networks, to detect the photon energies of around 1.45eV [1]. Silicon *pin* detectors have also been reported in imaging applications. Examples are CMOS image sensors on Silicon On Sapphire (SOS) substrate, and arrays of *pin* photodiodes replacing photomultipliers in radiometric and spectrometric devices such as mammography systems [34–37]. For high speed applications normally direct bandgap materials like InGaAs are used. Other materials such as InAs and InSb are useful in detectors for night vision applications. Since the bandgap in these materials is very narrow, they are usually cooled down to decrease the level of dark current [1].

The intrinsic layer is required to be highly pure to reduce the density of traps and the recombination henceforth. Selecting the width of the intrinsic region requires design optimization. It is necessary to increase the depletion width to maximize the absorption efficiency. A thick absorption layer is also favourable for decreasing the device capacitance, and improving the device speed. However, it increases the carriers' transit time and degrades the device performance for high speed applications. In fact, it is shown that the product of the $-3dB$ frequency and the quantum efficiency is constant, provided that the junction capacitance of a *pin* detector does not put any limitation on the device bandwidth [1, 38].

In an approach to overcome the speed and absorption dilemma, the path where the light is absorbed is separated from the path where the carriers travel. This can be achieved using a travelling waveguide structure. Therefore, it is possible to reduce the thickness of the absorption region; and at the same time obtain a good level of quantum efficiency by adjusting the length of the waveguide [38, 39]. This is normally achieved by illuminating the junction from the side of a waveguide structure. The absorbing layer is thin, and the cladding layers confine the propagating light into the absorbing layer. The path of conducting current is perpendicular to the path of light illumination. Therefore the quantum efficiency and bandwidth can be controlled almost independently [5, 39].

1.6.3 Avalanche Photodiodes (APD)

Avalanche photodiodes are high responsivity detectors with an internal gain. While the maximum gain in a *pin* photodetector is unity, an APD can generate a large gain by means of impact ionization. Briefly explaining, in a reversed biased *pn* (or *pin*) junction the minority carriers that enter the depletion region are swept away by the electric field to the other side of the junction. During this journey the carriers collide with the semiconductor lattice and lose energy. At low reverse biases this energy transfer just causes lattice vibration and local heat. At higher reverse voltages close to a value called breakdown voltage, the energy transfer is high enough to force an electron from valance band to jump to the conduction band. The resulting carriers can also contribute to high energy collisions and create more electron-hole pairs. As a result of this process (impact ionization), the revere biased current can theoretically go to infinity [40].

The APD normally operates near the avalanche breakdown point. If the APD is biased below the breakdown voltage, it is known to be working in the linear mode; since the average photocurrent is proportional to the incident light. The APD can also be biased in another mode of operation, called Geiger mode; which is achieved when it is biased at a voltage above the breakdown voltage [41]. APDs are fabricated from different materials including Si, Ge and III-V

compound semiconductors. APDs made from InGaAs on InP substrates and those made from Ge are widely used in fiber optics telecommunications [1, 40]. It is also shown that photomultipliers can be replaced with APDs in medical imaging applications such as Computerized Tomography (CT) imaging and Magnetic Resonance Imaging (MRI) [42–44].

The photocurrent in an APD is proportional to the number of the carriers. In practice however, an experimental multiplication factor, M, is used. M is multiplied to the un-multiplied photocurrent, generated as a result of photo-generation, to give the total APD photocurrent [45].

$$M = \frac{1}{[1 - (\frac{V}{V_B})]^n} \tag{1.17}$$

V and V_B are the applied and the breakdown voltages, respectively. n is an empirical parameter depending on the design of the device, and is usually between 2 and 7 [45]. The equation suggests that the gain is infinity if the device is biased at $V = V_B$. In practice however, the APDs are normally biased at a few volts below the breakdown voltage to reduce the multiplication noise [45]. The source of this noise is the statistical nature of the impact ionization itself; the more the variations in the number of the generated electron-hole pairs per absorbed photon, the more the variance of the multiplication factor M, and the higher the multiplication noise. When the reverse bias voltage moves towards the breakdown voltage, it increases the gain fluctuations and strengthens the noise up to a point where the signal to noise ratio degrades to an unacceptable value [41]. In addition, APDs need to be cooled by heat sinks. Since once the multiplication starts, the temperature of the device increases and reduces the ionization coefficient of carriers. At higher temperatures, the thermal vibration of carriers forces them to scatter more and as a result they do not gain enough speed to excite and ionize the lattice atoms [45].

It is common to separate the absorption and avalanche regions in APDs, usually due to the difficulties of maintaining a constant and high electric field within a long region. Among the photo-generated pairs, either electrons or holes can be used to enter the avalanche layer; it is however popular to choose the carrier that ionizes more carriers per unit distance, or in other words has a larger ionization coefficient (unit: cm^{-1}). If the ionization coefficient of electrons, normally referred as α, is larger than that of the holes, or β, the structure would be designed in order to not incorporate the holes in impact ionization process [1, 45].

The reason that only one carrier is used to start the avalanche process is because of the stochastic nature of impact ionization which is noisy. The fluctuation in multiplication is more when both carriers are involved in initiating the impact ionization [45]. In fact, according to the local avalanche noise model, in order to get a better performance in APDs, the ionization

coefficient of the carrier used to initiate the ionization must be considerably larger than that of the other carrier [46, 47]. In an APD with electrons as ionization initiators for example, the ratio of $k = \beta/\alpha$ must be much smaller than unity. The factor k is a property of the APD material; it is between 0.02-0.1 for Si, but larger for other semiconductors such as Ge and GaAs. Hetero-structure materials provide the opportunity to control the dynamics of electrons and holes separately, leading to a more effective way of controlling k [48, 49]. For example, $Al_xGa_{1-x}As$ APDs with $0.8 < x < 0.9$ have shown k factors of around 0.1. Research on $Hg_{1-x}Cd_xTe$ (x=0.3) have reported a much lower value for k, almost zero [50].

Another way of decreasing the noise in APDs is to reduce the thickness of the multiplication layer to sub-micron scales. This is reported to be effective for a wide variety of materials, including Si, GaAs, $Al_xGa_{1-x}As$, and other III-V materials [51–54]. Due to the stochastic behaviour of the impact ionization process, the multiplication factor experiences a large variation in thick avalanche layers. For thinner layers, the impact ionization process is more deterministic and as a result there would be fewer variations in the multiplication factor; the noise level will therefore decrease [53].

Impact ionization engineering (I^2E) is another proposed method that aims to reduce the noise in APDs by using hetero-structure materials. The device is made of a thin layer of a narrow bandgap material adjacent to a layer of a wider bandgap material. The bandgap difference leads to a difference in the threshold energy that the lattice atoms of each layer need for ionization. The energy of the carriers in the wide bandgap layer is not enough to ionize many carriers in this region. When the carriers enter the lower bandgap layer, they can ionize more carriers. As a result of this localized ionization in the thin layer the avalanche noise would be small [55–57]. While k factor of commercial APDs is about 0.4-0.5, the noise level obtained by I^2E method is almost as low as the noise of materials with k factor of 0.1 and lower [53].

1.7   Phototransistors

Bipolar transistors are used to detect photons as well. The transistor's amplifying action provides optical gain; and in contrast to APDs, bipolar transistors produce a lower level of noise. In the *npn* bipolar phototransistor of figure 1.6(a), the emitter-base junction and the collector-base junction are forward and reverse biased, respectively. Under this circumstance, if a small current is injected into the base contact, it slightly reduces the base-emitter barrier height; which in turn causes a large number of electrons to be injected from the emitter towards collector, resulting in the output current. If the device is used as a photodetector, normally the base contact is
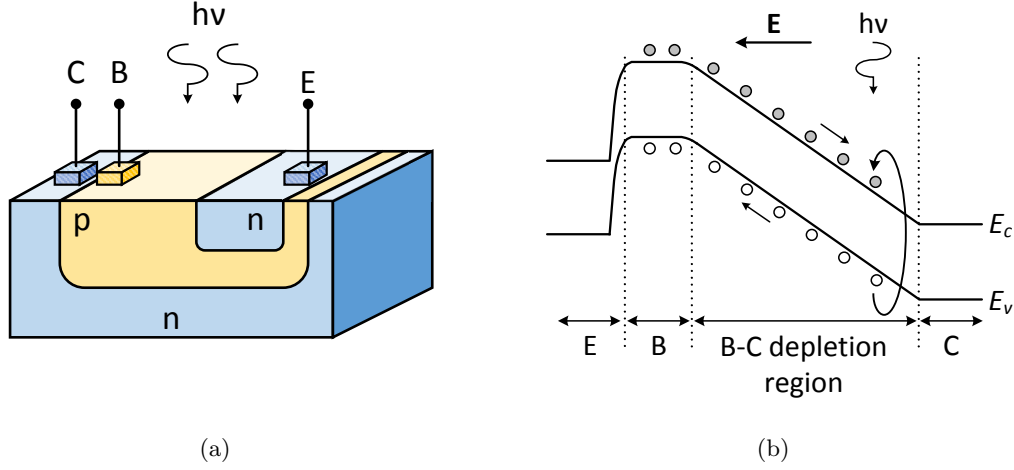
Figure 1.6: (a) A bipolar phototransistor. (b) Energy band diagram of the structure; photo-generated holes are accumulated in the base region and act as the base signal.

removed. The barrier change in this case occurs when the electron-hole pairs are generated as a response to the striking photons, as shown in figure 1.6(b). The holes, especially those created in the collector-base reverse biased junction, travel to the base region and play the role of the base current signal [1, 40].

Similar to a normal bipolar transistor, to achieve a high optical gain in a phototransistor the base width should be small. The base must be fabricated from a high quality material with very low defects. In addition, the doping levels of the junctions are such that the emitter-base depletion region is small, while the collector-base depletion region is large to absorb almost all of the photons. Assuming that each absorbed photon creates a hole that contributes to the base current, the base current is [1]

$$I_B = \eta q \frac{PA}{h\nu} \tag{1.18}$$

where q is the electric charge, and η is the quantum efficiency. P and $h\nu$ denote the light intensity and photon energy, respectively; and A is the illumination area. The optical gain G_{opt} is defined as the number of the electrons contributing in the collector current per unit time, or I_C/q, to the number of striking photons per unit time, $N_{ph} = PA/h\nu$. The formula for G_{opt} is

$$G_{opt} = \frac{I_C}{qN_{ph}} = \eta\beta \tag{1.19}$$

where β is the current gain of the bipolar transistor [1].

The depletion layer of base-emitter junction introduces a large capacitance, and limits the operation speed of the phototransistor. To address this and enhance the gain of the transistor, hetero-junction bipolar transistors (HBT) have been suggested [58]. Emitter in such transistors is usually made from a material with a wider bandgap to provide a higher barrier for the majority carriers of the base. The result is that fewer carriers can diffuse into the emitter region and therefore the emitter efficiency, γ, of the device is increased. In homo-junction transistors it is essential to choose a lower doping density for the base region in comparison with the emitter, to improve the emitter efficiency. However, low doping concentration increases the base resistance and degrades the frequency response of the device. Moreover, the depletion width inside the base region extends more in the case of lower doping, which in turn enhances the base width modulation or *Early effect*, especially in narrow base transistors. In HBT transistors however, the base can be heavily doped and at the same time kept narrow with no concern about the aforementioned drawbacks [1, 40]. In addition, in hetero-junctions the emitter can be doped lightly to decrease the capacitance of the emitter-base junction [59]. The wider bandgap of emitter would also be transparent to some wavelengths, and therefore most of the photons are absorbed in the base region, leading to increase in the quantum efficiency of the transistor [59, 60].

Si, Si-SiGe, InP-InGaAs, GaAlAs-GaAs, InGaAsP-InP, and AlGaAsSb-InGaAsSb are examples of the materials used in phototransistors [58, 59, 61–63]. High sensitivity phototransistors are fabricated with responsivities of 1000 and 1500 A/W for wavelengths of 650 and 400 nm, respectively [64, 65]. For wavelengths between 1.8-3 μm, suitable for applications like laser radar systems, molecular spectroscopy and remote gas sensing, AlGaAsSb-InGaAsSb Heterojunction Phototransistors (HPTs) are fabricated with very high responsivity, almost 3000A/W, and NEP of lower than commercially available InGaAs *pin* photodiodes [63, 66].

Phototransistors are rather slow devices because they rely on carrier diffusion. For high frequency applications, it is shown that applying a DC voltage to the base would help [67, 68]. Cut-off frequencies of up to 28 GHz are reported as a result of this technique [68]; however, the drawback is the degradation of signal to noise ratio (SNR) as a result of the extra shot noise that is introduced to the structure [67]. Another approach to reach higher speeds, while keeping the noise level low enough, is using punch-through phototransistors [67, 69, 70]. Gain-bandwidth product of >50 GHz is obtained with a hetero-junction, punch-through phototransistor [67]; while the optical gain and -3 dB bandwidth of larger than 15×10^3 and 300 MHz are reported for a similar Si based device [69]. Punch-through phototransistors are capable of detecting very low level optical intensities, as well. Optical gains as high as 10^7 are reported under the incident power of 7×10^{-15}W at the wavelength of 650 nm [70].

1.8 Nanowire based Photodetectors

Incorporation of nanowires in device structures is being actively investigated due to several reasons. The miniaturized size of one-dimensional devices provides low power consumption and more importantly the opportunity of integrating massive arrays of devices in a system. Parallel working devices are attractive in sensor applications as their ability to work independently provides the opportunity of real time detection. Moreover, for those nanowire devices that are fabricated using top-down approaches [4], the fabrication process could be compatible with mainstream complementary metal oxide semiconductor (CMOS) technology.

Reducing the size of the wire towards few nano-meter scales leads to some unique phenomena that no longer follow the well-known classical rules. Visible photo-luminescence [71,72], indirect to direct bandgap transition [73,74], ballistic transport [75], and Coulomb blockade (single electron tunneling) [76] are some of the properties that are proved to originate from carrier confinement by potential wells inside nano-scale structures. These quantum mechanical effects are not dominant in nanowire diameters of above 10nm; however, even at large diameters the surface to volume ratio of one-dimensional structures is higher than that of the two, and three dimensional structures made out of the same materials. As a result, the electrical properties of a one dimensional device can change easily in response to the adjacent charges that bind to the surface of the wire, and even the electric field of a gate contact. This property has proved useful in sensor applications; in some cases, the change in the electrical properties has provided single molecule detection [77–80]. In addition, large surfaces are more prone to surface states. The surface states can trap one type of carriers and therefore increase the recombination time. This is proved to be useful in boosting the photodetector's optical gain [81,82].

The small cross section of nanowires puts a limitation on the ability of such structures in optical absorption [83]; however the small diameter leads to properties such as polarization anisotropy of absorption in nanowire based photodetectors. In fact experiments on indium phosphide (InP), zinc oxide (ZnO) and gallium nitride (GaN) nanowire- and carbon nanotube (CNT) photodetectors have revealed that photo-detection is maximum when the incident light is polarized along the wire (tube) length; while it is minimum when light is polarized perpendicular to the wire [84–87]. Another property of these nanostructures is the dependency of the absorption spectrum on crystal orientation and doping. For example, experimental observations of silicon nanowires (diameter < 10 nm) with crystal orientations of <100> and <110> have shown that at photon energies of ≈4.7 eV, the absorption of <100> wires is higher. While at energies of ≈3.5 eV, <110> nanowires

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[4]Top-down methods aim to fabricate 1D-structures using conventional micro-fabrication techniques like lithography, oxidation, and etching.

absorb more effectively than those with <100> orientation [72]. In another report involving undoped and doped thermally grown silicon nanowires, the undoped wires generated larger photocurrent at the excitation wavelength of 633 nm; while doped nanowires did not respond to this wavelength at all [88].

The weak absorption in one-dimensional nanowires is usually compensated in two ways. The first approach tries to use arrays of nanowires that are fabricated either by lithography and etching [82], or by growing them using bottom-up techniques [89]. This increases the fill factor of the structure. In addition, nanowires diameter and pitch can be engineered to cause waveguiding effect and increase the external quantum efficiency [82].

The second approach incorporates nanowires into photodetector geometries with internal gain, such as avalanche photodiodes, photoconductors, and phototransistors. Avalanche photodiodes offer very high optical gain with good sensitivity. One example is an APD made of crossed silicon - cadmium sulphide (Si-CdS) nanowires with detection sensitivity of less than 100 photons at λ=400 nm; where the CdS nanowire is used as the detection element [90]. However, APDs have a major drawback; which is their high operating voltage. The second group of gain producing photodetectors, the photoconductors, also suffer from high dark current. This leads to a poor sensitivity for such detectors, as the high gain together with the large dark current would cause a large level of shot noise. However, the dark current can be reduced with the aid of a third terminal, e.g. gate, that turns the photoconductor into a junction-less phototransistor. This approach is very favorable as the device structure is simple. Having access to Silicon on Insulator (SOI) wafers also eases the creation of the third terminal using the buried oxide as the gate dielectric and the bottom silicon substrate as the gate contact [86, 88]. It is also possible to pattern and create the third terminal on top of the channel [91]. One can also dope the source/ drain areas to create junction phototransistors [92, 93], with responsivities of about $100A/W$ [93]. Besides the impact of physical gates, surface states can also contribute in device performance by separating the carriers and increasing the recombination time. Optical gains of about 35×10^3 and 10^{10} are reported in silicon and zinc-oxide based junction-less phototransistors, respectively [81, 82].

1.9   Research Objectives

Motivated by the unique properties of nanowires, we set our goal to investigate the pros and cons of using nanowires in photodetector geometries, to design devices with superior performance in terms of optical gain and sensitivity as compared with wide channel, non-nanowire based photodetectors. The material of choice in this study is silicon, but the concepts presented here

can be extended to other semiconductor materials as well.

Photodetectors with single nanowires usually suffer from lack of good interaction with light, and that is why nanowire arrays are often used. In our design, we address this by allocating a specific bulk area for absorption, and using the nanowires mainly for electrostatic purposes. The bulk absorption area should also help in mitigating the polarization dependent absorption in photodetectors with lateral nanowires. In addition, among the different device geometries, we focus on junction and junction-less phototransistors, as they are compatible with mainstream CMOS technology, and more importantly, the design benefits from the internal gain of photo-transistor geometries. We also remark that a large optical gain does not necessarily make such phototransistors capable of detecting low level intensities in a superior manner, compared to the photodetectors made out of bulk semiconductors. In a sensitive phototransistor the dark current needs to be small so that the associated noise level is low. In our design we consider ways to fulfill this requirement.

Overall, at the start of this study we aimed to find answers to the following questions:

1. What are the advantages and disadvantages of using nanowires in the channel of photode-tectors, in comparison to similar geometries without nanowires?

2. How does the photodetector response depend on the nanowire parameters such as width, depth, or doping?

3. Are there ways to incorporate nanowires in photodetectors in order to enhance their perfor-mance? What we are specifically looking for is increasing the ability of the device to detect low level intensities.

4. Would the fabricated structures verify the results obtained by modeling?

1.10 Organization of the Thesis

In chapters 2 and 3 we investigate the first three questions in junction and junction-less geometries, respectively. Since the diameter of the nanowires we study are large enough that quantum effects are unimportant, we calculate the device properties and physical quantities of interest by solving Poisson's equation and the electron and hole carrier continuity equations using the drift-diffusion framework [94]. We compare photodetectors in terms of their photocurrent, dark current, and the well known figures of merit such as responsivity, noise equivalent power, optical gain and signal to noise ratio. We also briefly discuss a few non-ideal cases such as surface recombination,

as well as the speed of devices in responding to light stimulation for the junction-less devices in chapter 3. Next, we propose ways to improve the performance of photodetectors, mostly in terms of optical gain and sensitivity, by modifying the channel geometry, composition, and energy band engineering using multiple gates.

Chapters 4 and 6 are devoted to the pathway we have followed in order to fabricate the photodetectors, and the measurement results obtained from the fabricated structures. Devices are made based on top-down approaches, due to more compatibility to CMOS technology. In addition, the smallest feature size of tens of nanometers, required for nanowires, was not out of the scope of the top-down approach. It should be noted that during device fabrication, our priority was the availability of a process, and not its optimization, as our main goal was to verify the concepts presented in the previous chapters. Later in chapter 7 we explain the future outlook and shortcoming of this study both in terms of modeling and fabrication.

As a part of investigating the effect of surface states on the performance of the devices, we studied Metal-Oxide-Semiconductor capacitor (MOS cap), which is an essential part of a MOS transistor. Since the three important biasing modes of the MOS transistors (accumulation, depletion and inversion) occur in the capacitor section of the transistor, study of the MOS capacitor gives precious information about the transistor, such as the channel doping type, gate dielectric thickness, and non-ideal conditions e.g. interface state properties.

While investigating the silicon - dielectric interface properties, we observed the very interesting light induced negative capacitance in fabricated capacitors. Device modeling revealed that such behavior has roots in the surface properties. In chapter 5, we discuss the modeling and fabrication of MOS capacitors and study their capacitance - voltage response under dark and illumination conditions.

For the measurement results that are presented in chapters 5 and 6, we used facilities at the Giga-to-Nanoelectronics Centre (G2N) of the University of Waterloo, and also the facilities at the University of Washington. At G2N Centre, my colleague Iman Khodadad set up and tuned the light source during the current-voltage and capacitance voltage measurements. The current-voltage measurements on the single gate structures (presented in chapter 6) are performed by my colleague Jenny Wan at the University of Washington.

Chapter 2

Nanowire based Junction Phototransistors

In this chapter we aim to explore the role of nanowires in junction phototransistors. Starting from a simple single gate phototransistor, we investigate how the structural properties such as channel width, doping and thickness impact the detector's dark and photo responses. Next, we introduce a new geometry, which was published by us in references [95–97], in which the use of nanowires leads to improved photo-response, and discuss ways of optimizing the structure.

2.1 Photodetector Structure and Modeling

Figure 2.1(a) shows the Silicon On Insulator Metal Oxide Semiconductor (SOI MOS) photodetector used in this study. The thickness of the buried oxide (BOX) layer is $200nm$. The active region is composed of source and drain areas that are separated by a $1\mu m$ channel. The source and drain are highly doped with n-type dopants (doping concentration: $10^{20}cm^{-3}$), while the channel is p-type. The gate oxide layer is $20nm$ thick and the gate has a work function of $4.17eV$. Other variables will be specified in the coming sections.

The SOI MOS device of figure 2.1(a) is biased under a positive drain voltage, while the source is connected to the ground. A typical drain current versus gate voltage of such structure is plotted in figure 2.1(b), under dark and illumination conditions. As a photodetector, we are interested to bias the gate in accumulation or depletion modes, although the actual drain current is larger in the inversion mode. The key reason for this choice is the low level of drain current under dark, which would enable the device to detect lower light intensities, and will be discussed later in this
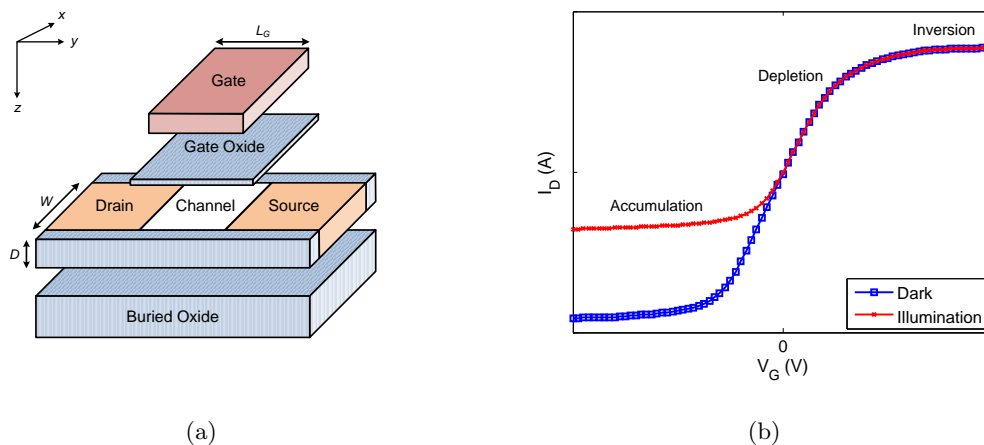
Figure 2.1: (a) Block diagram of a SOI MOS phototransistor. The device is $200nm$ thick, and source, channel and drain regions are $1\mu m$ long. Source and drain are n-type, with doping level of $10^{20}cm^{-3}$. The channel is p-type. (b) An example of drain current as a function of gate voltage, under dark and illumination conditions.

chapter.

When the gate is biased in accumulation or depletion modes, the device works under lateral bipolar action [98]. The negatively biased gate prevents the creation of the inversion layer in the p-type channel. This way, as plotted in figure 2.2, the energy band profile of the device from drain to source resembles the profile of a bipolar npn transistor whose collector and emitter contacts are actually the drain and source contacts of the MOS device. The negative gate keeps the junctions on both drain and source sides reverse biased and keeps the dark current low. Illumination generates electron-hole pairs within the channel. The electrons drift towards the drain in response to the high electric field (created by the positive voltage) as shown in figure 2.2(a). The holes on the other hand cannot pass the potential barrier and get trapped inside the channel. The accumulation of holes in the channel lowers the potential barrier, and as a result, the gate-source (or base-emitter) junction is forward biased as shown in figure 2.2(b); the lateral bipolar transistor is now in ON state; and a large current flows through the source-drain (emitter-collector) contacts of the transistor [98].

The electrical characteristics of this device can be calculated by solving Poisson's equation and the electron and hole carrier continuity equations in three dimensions, as formulated in equations 2.1, 2.2, and 2.3. We note that as long as the diameter of nanowires is larger than the quantum mechanical limit of about $10nm$, the impact of the quantum mechanical effect is minimal and the

24
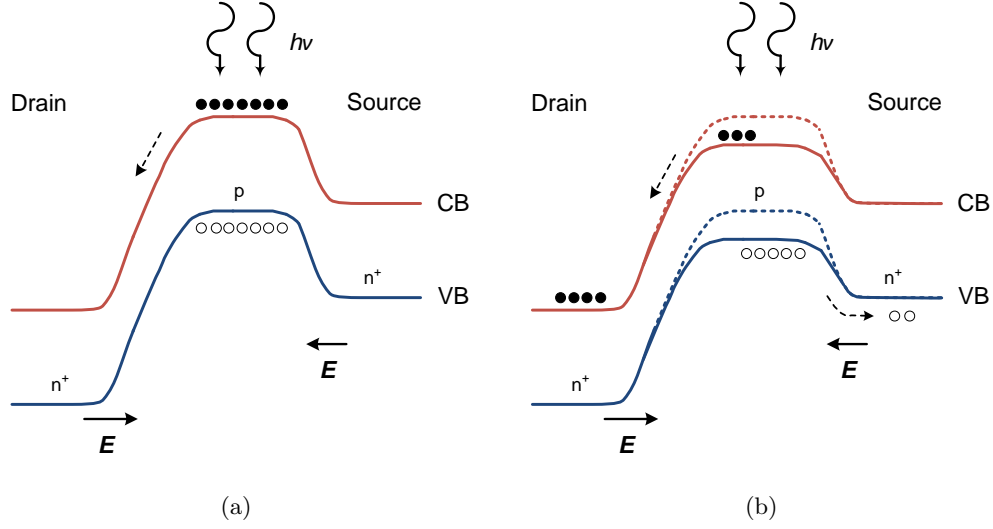
Figure 2.2: Lateral bipolar action in SOI MOS phototransistors. Energy band diagram of the phototransistor in figure 2.1(a), at a cutline along y direction. (a) Electron-hole generation after illumination. (b) Barrier lowering due to accumulation of holes in the channel. $V_G < 0$ and $V_D > 0$.

Drift-Diffusion equations are sufficient.

$$\nabla.\vec{D}(x,y,z) = \rho(x,y,z) \tag{2.1}$$

$$\frac{\partial n(x,y,z)}{\partial t} = \frac{1}{q}\nabla.\vec{J}_n(x,y,z) + \frac{\partial n(x,y,z)}{\partial t}\Big|_{thermalR-G} + \frac{\partial n(x,y,z)}{\partial t}\Big|_{others} \tag{2.2}$$

$$\frac{\partial p(x,y,z)}{\partial t} = -\frac{1}{q}\nabla.\vec{J}_p(x,y,z) + \frac{\partial p(x,y,z)}{\partial t}\Big|_{thermalR-G} + \frac{\partial p(x,y,z)}{\partial t}\Big|_{others} \tag{2.3}$$

$\vec{D}$ and ρ in equation 2.1 are the electric displacement field and the charge density, respectively. $\vec{J}_n$ and $\vec{J}_p$ in equations 2.2 and 2.3 represent the electron and hole current density vectors; each composed of drift and diffusion current density components [40].

$$\vec{J}_n(x,y,z) = \vec{J}_{n|drift} + \vec{J}_{n|diff} = q\mu_n n(x,y,z)\vec{E}(x,y,z) + qD_n\nabla n(x,y,z) \tag{2.4}$$

$$\vec{J}_p(x,y,z) = \vec{J}_{p|drift} + \vec{J}_{p|diff} = q\mu_p p(x,y,z)\vec{E}(x,y,z) - qD_p\nabla p(x,y,z) \tag{2.5}$$

where μ_n and μ_p represent the electron and hole mobility, and $\vec{E}$ is the electric filed. n (p), ∇n (∇p), and D_n (D_p) are the electron (hole) concentration, electron (hole) concentration gradient and electron (hole) diffusion coefficient, respectively.

$\frac{\partial n(x,y,z)}{\partial t}|_{thermalR-G}$ and $\frac{\partial p(x,y,z)}{\partial t}|_{thermalR-G}$ are the thermal generation and recombination rates of carriers that depend on recombination-generation or R-G centers (lattice defects and special impurity atoms).

$$\frac{\partial n(x,y,z)}{\partial t}|_{thermalR-G} = -\frac{\Delta n(x,y,z)}{\tau_n} \tag{2.6}$$

$$\frac{\partial p(x,y,z)}{\partial t}|_{thermalR-G} = -\frac{\Delta p(x,y,z)}{\tau_p} \tag{2.7}$$

Finally, the last two terms in equations 2.2 and 2.3, $\frac{\partial n(x,y,z)}{\partial t}|_{others}$ and $\frac{\partial p(x,y,z)}{\partial t}|_{others}$, represent all other processes that change the carrier concentration rate. For simplicity, it is assumed that the only 'other' process which takes place within the system is photo-generation. Assuming G_L represents the photo-generation rate [40],

$$\frac{\partial n(x,y,z)}{\partial t}|_{others} = \frac{\partial n(x,y,z)}{\partial t}|_{light} = G_L(x,y,z,\lambda) \tag{2.8}$$

$$\frac{\partial p(x,y,z)}{\partial t}|_{others} = \frac{\partial p(x,y,z)}{\partial t}|_{light} = G_L(x,y,z,\lambda) \tag{2.9}$$

We have used ATLAS commercial simulator [94] in order to solve Poisson's and carrier continuity equations and obtain the electrical characteristics of the devices. As for mobility models, in most of the simulations, we have used the default model, or Constant low-field mobility model, in which the mobility μ_x is obtained [1] by including the effect of the lattice scattering as a function of the lattice temperature T_L, as shown in equation 2.10. The parameters Mu_x and TMu_x are summarized in table 2.1 [94].

$$\mu_x = Mu_x(\frac{T_L}{300})^{-TMu_x} \tag{2.10}$$

Table 2.1: Parameters for the constant low-field mobility model

	Parameter	Value
1	Mu_n $(cm^2/(V.s))$	1000
2	Mu_p $(cm^2/(V.s))$	500
3	TMu_n	1.5
4	TMu_p	1.5

[1]$_x$ is replaced with $_n$ and $_p$ to represent data for electrons and holes, respectively.

In addition, unless otherwise specified, we assumed an infinite recombination-generation lifetime for minority carriers. This assumption does not impose much inaccuracy in the results as long as the diffusion length in each region (source, drain, or channel) is larger than the length of that region itself. As an example, for a doping of $10^{20} cm^{-3}$ and the recombination time of 10^{-5}sec, the diffusion length is almost $36\mu m$. This is quite longer than the $1\mu m$ length of the source and drain.

As the light source, we choose a monochromatic source with wavelength of $633nm$ that is incident on the channel through a window whose dimensions determine the striking photon rate. In order to include the illumination in the modeling, it is required to obtain the optical intensity profiles and convert them into photo-generation rates. ATLAS uses a general purpose ray tracing program, called LUMINOUS, for this purpose [94]. The photo-generation rate, $\bar{G}_L$ (the average number of photogenerated carriers per unit volume of the semiconductor, per unit time), is mathematically described by (same as equation 1.3)

$$\bar{G}_L = (1 - R)(1 - e^{-\alpha D})\frac{P_{in}}{AD}\frac{1}{h\nu} \tag{2.11}$$

where R is the reflection of light from the surface and P_{in}/A is the optical intensity of light (unit: W/cm^2, P_{in}: total incident power, A: the area that light is shining through). D is the semiconductor thickness; and h, α and ν are Planck's constant, absorption coefficient of the material and the frequency of the light, respectively. The absorption coefficient is:

$$\alpha = \frac{4\pi}{\lambda}k_{imag} \tag{2.12}$$

λ is the light wavelength and k_{imag} is the imaginary part of the refractive index. We note that equation 2.12 gives the absorption coefficient for bulk, and not for confined structures such as nanowires whose widths can be smaller than the wavelength of the incident light. Therefore, the simulation results will purely show the role of electrostatics in the response of photodetectors with different widths.

When simulating the device under dark conditions and at room temperature, the device current is usually in the same order as the machine precision ($< 10^{-16}$A), and therefore the simulation results are not accurate. To surpass this problem, we simulate the dark current at multiple higher temperatures, while keeping the semiconductor mobility and bandgap fixed. Afterwards, we estimate the room temperature current by extrapolation.

2.2 Role of Channel Width and Doping

In this section the thickness of the active region is $200nm$. The gate, drain and source contacts are biased at $-2V$, $0.5V$ and $0V$, respectively.

If the front and back oxide layers in figure 2.1 are removed, then the whole structure would be two dimensional. In fact, one can assume that the device is composed of n perfectly similar transistors, each with channel width of δw ($n \times \delta w = W$, W: channel width of the original device), that are connected together along the x axis. In such two dimensional structures, the drain current directly scales with the channel width, and the gate impact on the potential barrier does not depend on the channel width. This is illustrated in figure 2.3(a), where the conduction band energy of two structures with different channel widths is compared. In the first structure the channel is $1\mu m$ wide, and in the second structure the channel width is $100nm$. The energy band is obtained along the z axis at the middle of the channel (figure 2.1), and simply shows that the barriers are identical. Therefore, one expects the dark current to change linearly with the channel width. In figure 2.3(b), we have plotted the drain current of the two aforementioned structures, under dark condition and at different temperatures [2]. As shown in the graphs, at all temperatures the drain current of the device with $1\mu m$ channel is indeed 10 times larger than that of the device with $100nm$ channel.

Now, let us consider N photons per second strike both structures through equal size windows (equal light intensity). Assuming each photon generates one electron-hole pair, this results in an equal number of photo-generated carriers in the two detectors. The barrier height [3] is logarithmically proportional to the number of photo-generated holes per unit volume, or $N/(WLD)$, where L and D represent the channel length and thickness, respectively [4]. As a result, firstly, the barrier change (decrease) as a function of photon rate is logarithmic, as plotted in figure 2.3(c). Secondly, since the number of photo-generated carriers per unit volume is larger for the device with narrow channel (small W), the potential barrier of the narrow device would be lower than that of the wide device (figure 2.3(c)).

On the other hand, in a bipolar transistor the total current is proportional to the channel width W. In addition, the current has an exponential dependence on the barrier height. As a result, the photocurrent in two dimensional structures is proportional to N, but independent of

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[2]As explained earlier, due to machine precision issues, we obtained the dark current at higher temperatures.

[3]The barrier height is considered as the difference between the conduction band level at the channel, and the conduction band level at the source (that is grounded). The barrier height is obtained at the top silicon-silicon dioxide interface.

[4]L and D are equal in the two devices and therefore can be ignored.

W. This is plotted in figure 2.3(d). The graphs show the drain current of the two aforementioned structures as a function of light intensity. Regardless of the intensity, both structures show equal currents.

(a)

(b)

(c)

(d)
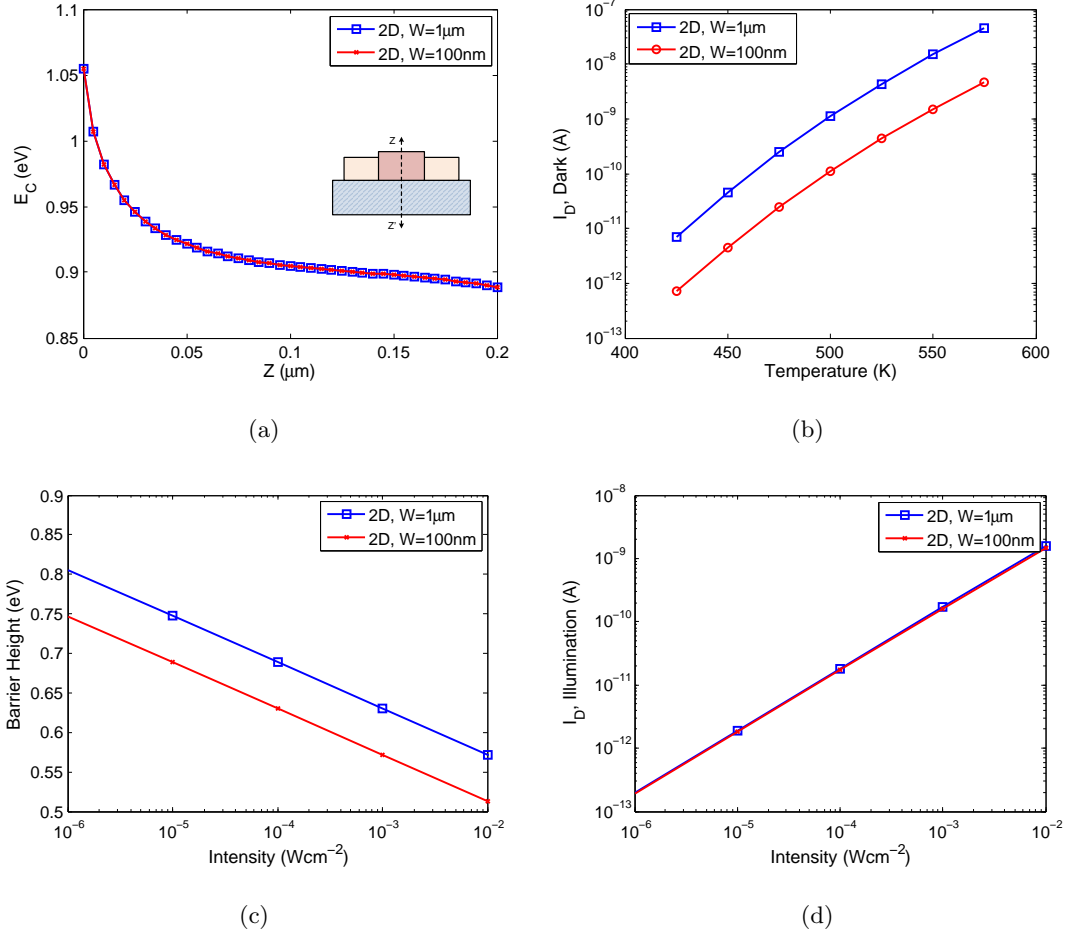
Figure 2.3: Two dimensional structures with channel widths of $1\mu m$ and $100nm$ are compared in terms of (a) Conduction band at dark (along cutline ZZ') (b) dark current versus temperature, (c) barrier height and (d) photocurrent as a function of intensity. Device thickness: $200nm$. Channel doping: $10^{16}cm^{-3}$, $V_G = -2V$, $V_D = 0.5V$.

Adding the front and back oxide layers (figure 2.1) changes the gate's impact on the potential barrier, and affects the drain current. Under this circumstance, the drain current does not necessarily scale with the channel width. In figure 2.4(a) we have plotted the dark current of such *three dimensional* structures, as a function of the channel width. The dark current is obtained at room temperature, for different doping concentrations of the channel. Similarly, figure 2.4(b) shows the drain current versus the channel width when the device is illuminated.

(a)   (b)
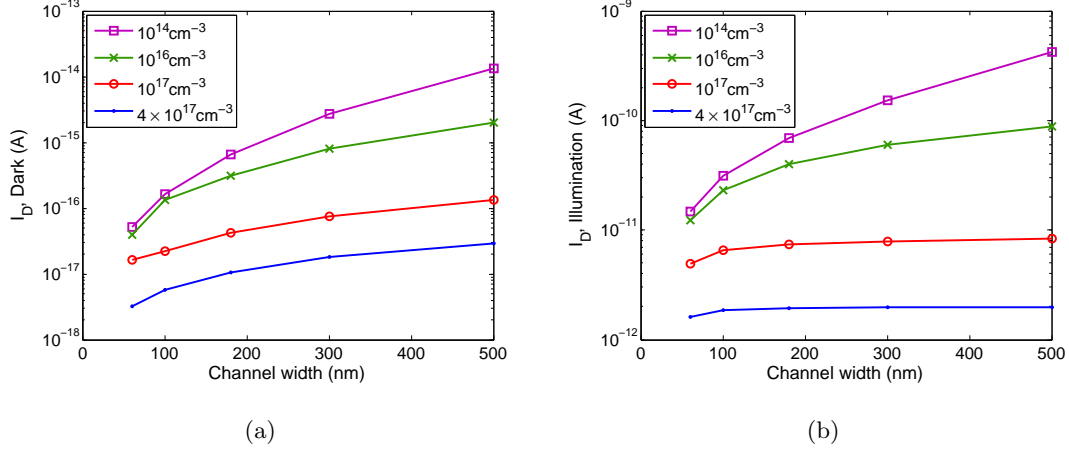
Figure 2.4: Room temperature drain current of the phototransistor in figure 2.1(a), as a function of channel width and doping, under (a) Dark, and (b) illumination conditions. $V_G = -2V$, $V_S = 0V$, $V_D = 0.5V$. Light intensity and photon rate are $10^{-4}W/cm^2$ and $1.9 \times 10^5 s^{-1}$, respectively.

As shown in figure 2.4, the three dimensional effects indeed change the impact of the channel width on the drain current. This however seems to strongly depend upon the doping level of the channel. Under dark condition (figure 2.4(a)), and at the doping concentration of $4 \times 10^{17} cm^{-3}$, when the channel is $500nm$ wide, the dark current is 9 times larger than the current of a device with a $60nm$ wide channel. This is very close to the ratio of the channel widths, or $500/60$. However, at the doping level of $10^{14} cm^{-3}$ the ratio is about 130, which is much larger than the channel width ratio. This behaviour can also be observed under illumination, in figure 2.4(b). In the accumulation mode ($V_G = -2V$), for wide channels and at high doping levels, the photocurrent is almost independent of the channel width (blue and red curves in figure 2.4(b)). As the channel gets narrower, and at lower channel doping concentrations, the drain current gets smaller for structures with narrow channels.

Regardless of being illuminated or not, when the channel is surrounded by oxide, the gate electric field is transferred to the silicon-silicon dioxide interface at the top, the two sides, as well as the bottom of the channel. In the accumulation mode, the majority carriers concentrate at all four interface areas and pull up the potential barrier. The conduction band contours of two devices at dark condition are pictured in figure 2.5(a). One of the devices has a $60nm$ wide channel; while the channel width of the other device is $500nm$. The contours are obtained across the channel of each device (xz plane). Both devices show the accumulation of holes at interfaces; however, the gate capacitance coupling is stronger in the narrow channel. The barrier height at

the interfaces is therefore higher than the case of a two dimensional structure. A similar gate effect can also be observed when the device is illuminated, as presented in figure 2.5(b).

(a) Dark
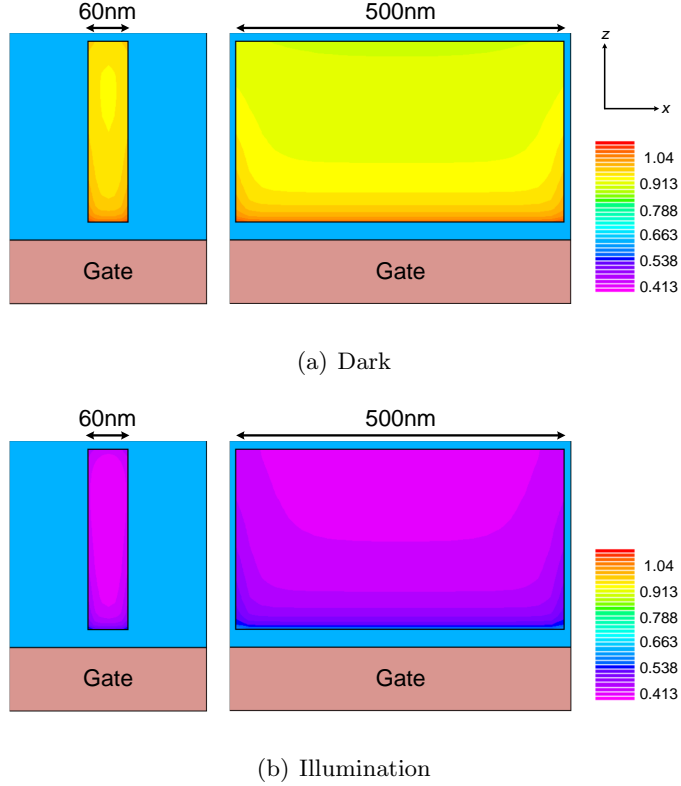
(b) Illumination

Figure 2.5: Conduction band energy contours of two 3D SOI MOS structures (figure 2.1(a)) at (a) dark, and (b) illumination conditions. The channel width is $60nm$ for the structure on the left, and $500nm$ for the structure on the right. The contours are obtained across the channel, xz plane. The channel doping is $10^{16}cm^{-3}$; $V_G = -2V$, $V_S = 0V$, $V_D = 0.5V$.

As plotted in figure 2.5, when the channel gets narrower, the barrier at the interfaces changes the total current more effectively. As a result, the drain current does not scale with the channel width under dark condition. Due to the same reason, under illumination the drain current is smaller in devices with narrower channels. We also remark that the doping concentration of the channel determines the accumulation width. At doping level of $10^{17}cm^{-3}$ and higher, accumulation is quite localized to the areas close to the silicon and dielectric interface. As a result, the overall three dimensional effect is less pronounced, except in narrow channels as shown in figure 2.4.

The capacitance coupling of the gate occurs in depletion mode as well. Here, one expects the gate to lower the potential barrier of a narrow channel more than the barrier of a wide
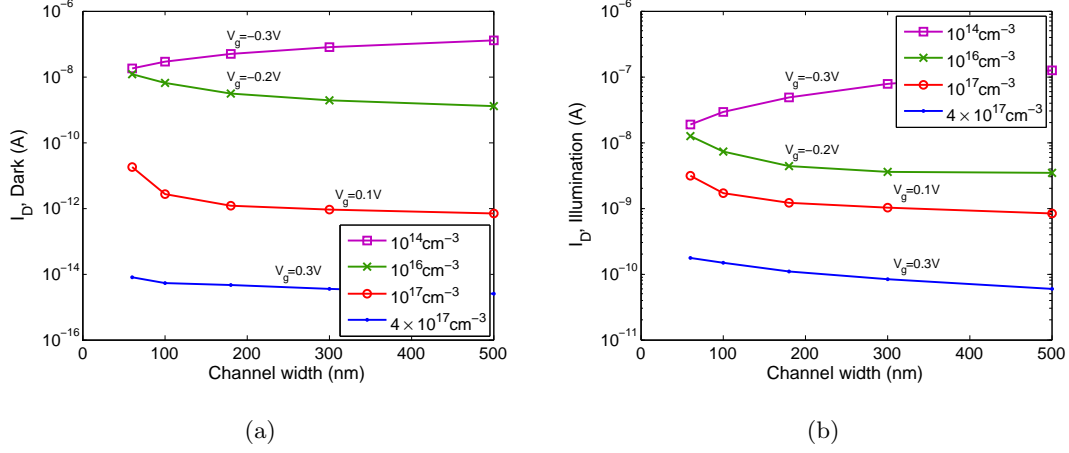
Figure 2.6: Room temperature drain current of the phototransistor in figure 2.1(a), as a function of channel width and doping in depletion mode. (a) Dark, and (b) illumination conditions. $V_S = 0V$, $V_D = 0.5V$. Light intensity and photon rate are $10^{-4}W/cm^2$ and $1.9 \times 10^5 s^{-1}$, respectively.

channel. This should potentially increase the drain current of narrow structures. For structures with channel doping of $10^{16}cm^{-3}$ and higher, this hypothesis is correct, as plotted in figure 2.6(a), and (b). The drain current under both dark and illumination has increased when the channel is narrowed down. For doping level of $10^{14}cm^{-3}$ however, the drain current has decreased in devices with narrower channels, contrary to the expectations.

In order to explain this, we note that when the device is biased in the depletion mode, the total gate capacitance is determined by the series combination of the gate oxide capacitance (C_{ox}) and the depletion layer capacitance (C_s). The contribution level of C_s depends on the doping concentration and the thickness of the channel. When the channel is highly doped, the depletion width is shorter than the channel thickness ($200nm$). However, (under the same doping condition) if the channel becomes narrow, the gate coupling to the side interfaces can contribute to the depletion and therefore increase of the depletion width. We have plotted the contours of the conduction band energy of two devices in figure 2.7(a) for the channel doping of $10^{17}cm^{-3}$. For the device with $500nm$ wide channel, the width of the depletion layer is about one third of the channel thickness. However, for the $60nm$ wide device, the depletion width is extended due to the strong gate coupling. This results in a smaller depletion capacitance C_s for the narrow device and impacts the device characteristics, such as the sub-threshold slope and the threshold voltage. A smaller depletion capacitor will have a stronger contribution in the series combination of the total gate capacitance; as a larger percentage of the gate voltage is transferred to C_s. Therefore, the narrow channel is depleted at a smaller gate bias, in comparison with a wider

channel. When the gate voltage is increased, the current in the narrow device starts to increase faster in the sub-threshold region and enter the strong inversion sooner. As a result, at some point, the current of the device with the narrower channel is larger than the current of the wide structure, as indicated in figure 2.7(b).

(a)

(b)

(c)

(d)
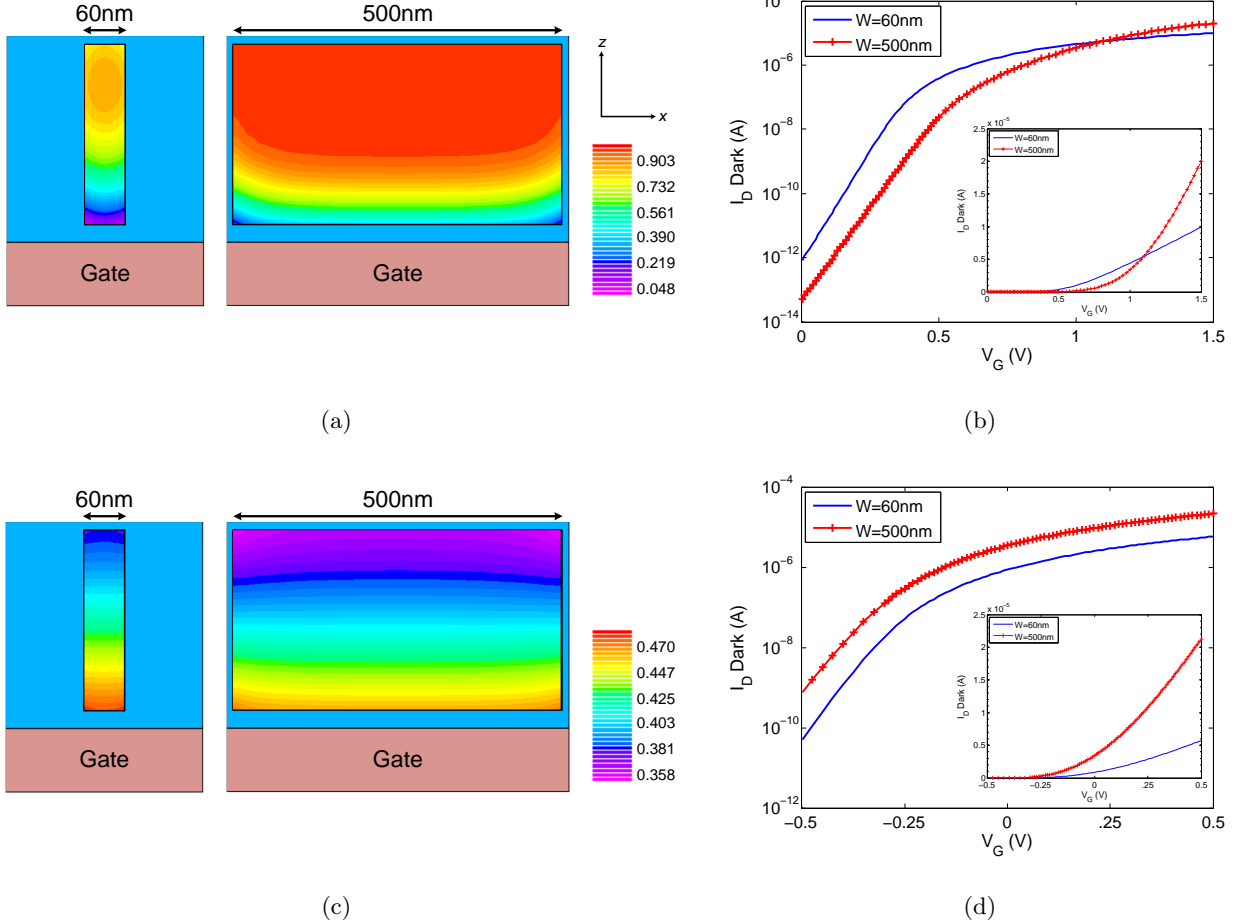
Figure 2.7: (a) Conduction band energy contours of two SOI MOS structures (figure 2.1(a)), with channel doping of $10^{17}cm^{-3}$. The gate is biased in depletion mode, at $0.4V$. (b) Drain current of the structures in (a) as a function of the gate voltage. Inset shows the current in linear scale. (c) Conduction band energy contours of two SOI MOS structures, with channel doping of $10^{14}cm^{-3}$. The gate is biased in depletion mode, at $-0.5V$. (d) Drain current of the structures in (c) as a function of the gate voltage. Inset shows the current in linear scale. The contours are obtained across the channel, xz plane.

At low doping levels of the channel, the depletion width is much longer than both the device

thickness and channel width. Under this circumstance, the gate coupling to the narrow channels does not dramatically change the potential barrier. This is shown in the conduction band contours of figure 2.7(c). Here the channel doping is $10^{14} cm^{-3}$, and the gate is biased at $-0.5V$. Both channels are depleted similarly; the narrow device is just slightly more depleted. We note that the scale bar in this figure shows a total energy change of less than $0.15eV$ within the device. The threshold voltage and the sub-threshold slope of the two devices are therefore very close together, as shown in figure 2.7(d), and the drain currents of the structures do not cross. As a result, in devices with lightly doped channels, the narrow channel cannot help to increase the drain current in depletion mode.

2.2.1 Devices with Nanowire Arrays

Nanowire arrays are widely used in designing optical devices like solar cells and photo-detectors. The array provides the opportunity of a more efficient light capture, as well as a high density of parallel working nanowire devices [82, 99, 100]. In this section we study the drain current of a photo-detector array, shown in figure 2.8(a), where the device is composed of 5 horizontal *npn* nanowires underneath the gate. Each nanowire is $60nm$ wide. The wires are separated from each other by $40nm$ of silicon dioxide. Each wire is an *npn* junction transistor, with highly doped n^+ regions (doping concentration:$10^{20} cm^{-3}$). The channel is *p*-type, with doping level of $10^{16} cm^{-3}$. Other specifications of the array device are similar to the case of figure 2.1.

We obtained the drain current of the array photodetector and compared it with two other devices. The first device is a single channel photodetector with channel width of $60nm$, and we multiply its current by a factor of 5. The second device is a single channel device whose channel is $500nm$ wide. The drain current versus the gate voltage of each device is shown in figures 2.8(b) and (c) for room temperature dark and illumination conditions, respectively. For the case of illumination, the intensity of light and the photon rate are kept the same for all three cases.

The current of the photodetector array falls somewhere in between those of the other two structures (figures 2.8(b) and (c)). The conduction band contours of the three structures, plotted in figure 2.8(d) at $V_G = -2.0V$, also confirm this. Firstly, we note that the conduction band of the two nanowires on the left and right end of the array is higher in comparison with the conduction band energy of the other three nanowires located in the middle. This is due to having a thicker layer of oxide at the two ends (not shown in the figure), in comparison with the $40nm$ thick oxide that have separated the inner nanowires. Since the nanowires in the array are packed, the effective capacitance for each nanowire in the array is smaller than that of a single nanowire device. The weaker capacitive coupling leads to a weaker accumulation and a lower barrier height for each

individual nanowire in the array. As a result the drain current of the *array with 5 nanowires* is larger than the drain current of *5 single gate nanowire devices.*

On the other hand, each individual nanowire in the array experiences a stronger capacitive coupling when compared with the $500nm$ channel. As shown in figure 2.8(d), even the conduction band of the inner nanowires is slightly higher than that of the $500nm$ device at the middle areas. Besides that, the total width of the nanowires in the array is smaller than $500nm$, and as result one expects a smaller current for the array. Increasing the spacing between the nanowires [5] would result a smaller current than the studied case. Decreasing the space between the wires, or packing one more wire pushes the current closer to that of the $500nm$ device.

2.3 Role of Channel Thickness

In this section, we investigate the role of the active region thickness on the drain current of the photodetectors. Generally it is expected to observe an increase in the current as the semiconductor depth (therefore the device cross sectional area) is increased. Increasing the thickness can also improve the quantum efficiency and increase the photocurrent. However, the gate contact and also the three dimensionality of the structures (the fact that the active region is surrounded by oxide) cause the drain current to deviate from the values that one expects form a purely two dimensional structure. This will be discussed in more detail in this section, by comparing the results at dark and illumination conditions for structures with different channel depths. We begin by investigating how the response of a pure, lateral bipolar transistor (no gate contact) varies as the thickness of the active region changes. Afterwards, the impact of the gate bias (in accumulation) on a two dimensional structure is studied, and finally the effect of three dimensionality is included.

Regardless of the transistor geometry (with or without gate), in the devices we study here, the doping level of the channel (or base, p-type), source (or emitter, n-type), and drain (or collector, n-type) are 10^{16}, 10^{20}, and $10^{20}cm^{-3}$, respectively. The channel is $1\mu m$ long, and the gate oxide is $20nm$ thick. The gated structures are biased in accumulation mode, at $V_G = -2.0V$. The source and drain regions are biased at $0V$ and $0.5V$, respectively. The drain dark current is obtained at the temperature of $475K$.

Similar to conventional bipolar transistors, in a lateral bipolar transistor the drain current is proportional to the cross sectional area. As a result, one expects the dark current to linearly vary as a function of the channel thickness. This is demonstrated in figure 2.9(a), where we have plotted the drain current of a two dimensional lateral bipolar transistor versus the channel

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[5]One nanowire has to be removed to keep the whole array embedded within the same volume.

(a)

(b)

(c)

(d)
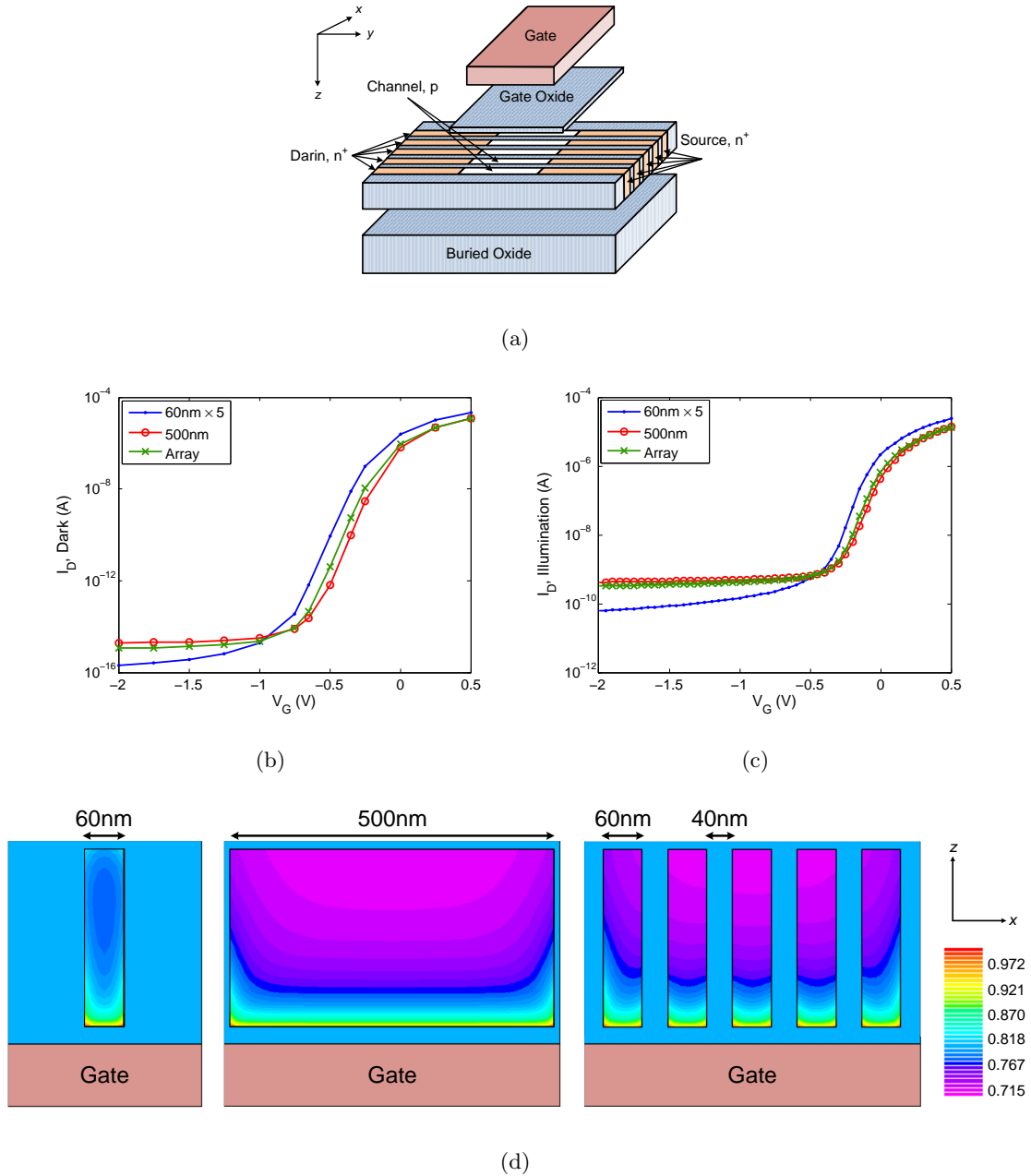
Figure 2.8: (a) Photodetector with array of nanowires. The nanowires are $60nm$ wide. The channel is p-type, with doping level of $10^{16}cm^{-3}$. Other specifications of the device are similar to figure 2.1. Drain current versus the gate voltage of the nanowire array device, under dark (b) and illumination (c). The results are compared with those of a single channel device with channel width of $60nm$, whose current is multiplied by 5, and also a single channel device whose channel is $500nm$ wide. $V_S = 0V$, $V_D = 0.5V$; the striking photon rate$= 9.6 \times 10^5 sec^{-1}$.(d) Conduction band energy contours of the structures at dark. $V_G = -2.0V$, $T = 475K$.

thickness. In this particular structure the channel width is $1\mu m$. Furthermore, no gate or base contact is present, and therefore the source and drain currents are equal. The dark current shows a linear change as the thickness of the channel is changed. To further analyze this, we have calculated the ratio of $\frac{I_{Drain}(D)}{D}$, and plotted the normalized value in figure 2.9(b). D denotes the device thickness. The normalized value of 1 at all depths confirms the linear dependency of the dark current to the semiconductor thickness.
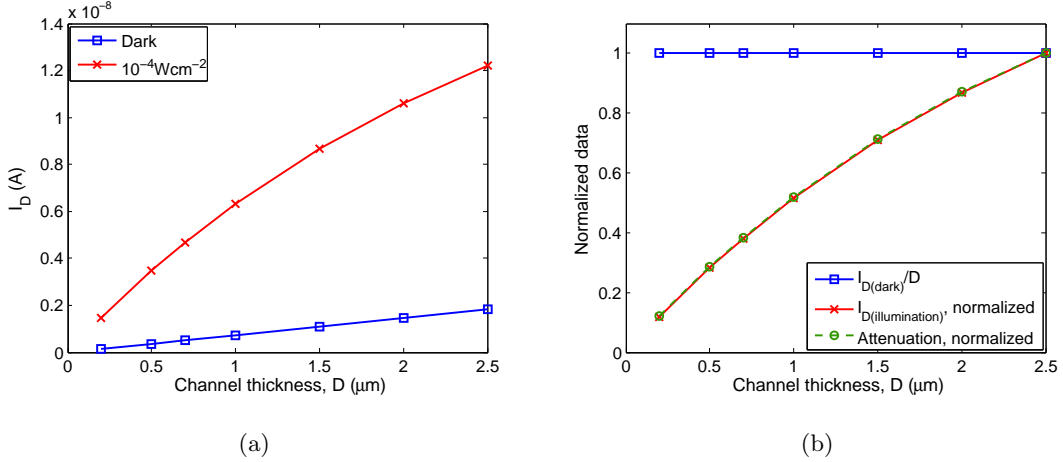
Figure 2.9: Dependence of the drain current on the semiconductor thickness in a two dimensional lateral bipolar transistor (n^+pn^+), with channel width, length and doping of $1\mu m$, $1\mu m$, and $10^{16}cm^{-3}$, respectively. (a) Drain current versus thickness under dark $(T = 475K)$ and illumination. (b) Blue: $\frac{I_{Drain}(D)}{D}$, (D: semiconductor thickness) under dark. Red: the drain current under illumination, normalized to its maximum value at $D = 2.5\mu m$. Green: attenuation curve, normalized to its value at $D = 2.5\mu m$. $V_S = 0V$ and $V_D = 0.5V$.

Under illumination, the drain current is also proportional to the photo-generation rate, $\bar{G}_L$, described in equation 2.11. The total illumination current, plotted in figure 2.9(a), is therefore a function of attenuation $1 - e^{-\alpha D}$. To clarify this, we normalized the drain current under illumination to its maximum value, e.g. the current at $D = 2.5\mu m$. We also normalized the attenuation to its value at $D = 2.5\mu m$. Both normalized curves are plotted in figure 2.9(b). Agreement of the two curves confirms the dependency of the current under illumination, to the attenuation.

Adding the gate to the structure of a two dimensional device would cause the drain current to deviate from the pure bipolar case. This is caused by the creation of the accumulation layer as a result of the gate negative bias. The change would be even more pronounced if the structure is surrounded by oxide (three dimensional case). The structures with doping levels of about

$10^{16}cm^{-3}$ and below are also more influenced by the gate and the three dimensionality of the channel.

The width of the channel would also play a role on how much the drain current is changed with the device thickness. Here, we investigate devices with channel width of $500nm$ and $60nm$. In both groups, the gate covers the top, as well as the front and back sides of the channel; while the gate oxide is $20nm$ thick on all three sides [6].

For the three dimensional gated structures, the change in the drain current as a function of the channel depth is plotted in figures 2.10(a), and (b) under dark and illumination conditions, respectively. Each graph contains a plot for structures with channel width of $500(60)nm$, as well as a plot for a pure, two dimensional bipolar structure (no gate) with the same channel width. The gate in the three dimensional structures pulls up the barrier at the interface areas. As a result, regardless of the thickness, in both figures the drain current of the gated structure is smaller than the drain current of the two dimensional case with the same width and thickness. The exponential relation of the drain current under illumination to the semiconductor thickness results in more deviation in the drain current, when the device is illuminated (figure 2.10(b)). In addition, the thinner structures with narrower channels are more influenced, as the portion of channel that is accumulated becomes more comparable to the total channel. Therefore, the drain current is decreased the most when the channel size moves towards the nano-scale range.

2.4 Ideas to Increase the Photocurrent

Based on extensive investigation in sections 2.2 and 2.3, where we studied the role of width, doping and thickness, we conclude that including nanowires can not increase the photocurrent of a junction phototransistor in an appreciable manner. In this section, we illustrate how one can incorporate nanowires in a SOI MOS phototransistor in order to increases the device photocurrent. In contrast to other designs in which nanowires serve as the absorption medium and also a part of the device, in our proposed geometry, the nanowires are mostly used for gain purpose. In our design, the device channel is partly wide for efficient light absorption, and partly narrow (nanowires) for band engineering. The charge transport within the nanowires is electro-statically controlled by a set of two gates. This increases the photocurrent; and leads to a large optical gain and photo-responsivity.

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[6]It is important to note that the gate geometry plays a significant role in the results presented here. Due to the oxides that cover the left and right sides of the channel, both source and drain contacts can couple to the channel, and change its barrier height. Especially, the positively biased drain tends to pull down the potential barrier. This can change the drain current significantly in thick structures, if the gate is placed only on top of the channel.

(a)   (b)
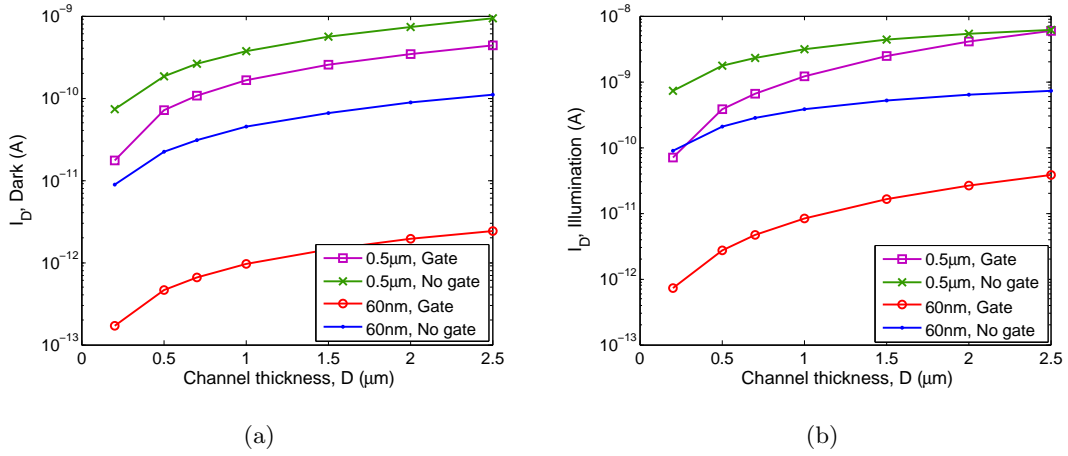
Figure 2.10: Dependence of the drain current on the semiconductor thickness in three dimensional, gated transistors, with channel widths of 60, and $500nm$. The drain currents of pure, two dimensional bipolar structures (no gate) with similar channel widths are also plotted for comparison. (a) Drain current versus thickness under dark ($T = 475K$). (b) Drain current versus thickness under illumination. The channel length and doping are $1\mu m$, and $10^{16}cm^{-3}$, respectively. The gated structures are biased at $V_G = -2.0V$. $V_S = 0V$ and $V_D = 0.5V$.

The key to an optimized design is understanding the parameters that affect the current in a bipolar phototransistor (section 2.1) more dominantly. When the device is illuminated, the lateral bipolar transistor (figure 2.2(b)) is in its ON state. The current therefore linearly depends on the width [7]; and exponentially depends on the barrier height on the source side. When a nanowire is used, the width is decreased and this can potentially decrease the photocurrent. As a result, the design should be such that incorporation of the nanowire leads to more change (lowering) in the barrier height; so that the exponential increase in the current compensates the linear decrease of the width.

At dark, the bipolar transistor is OFF; and this results in a negligible dependence of the current on the barrier height, and carrier diffusion. The dark current depends on the minority carrier drift from the channel [8], mostly on the drain side due to the larger electric field (drain is biased positively). As a result, as long as the barrier is high enough to consider the device in OFF state, the dark current depends on the width in a linear manner, and a narrower channel on the drain can help decrease the dark current.

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[7]To be more precise, the current depends on the cross sectional area; however here we do not change the thickness of the structure.

[8]Since the doping concentration of the channel is much smaller than source and drain.

Our proposed device, shown in figure 2.11(a) is a SOI MOS detector with multiple gates. For illustration purposes, the active region is $200nm$ thick, and is located on top of a $200nm$ buried oxide. The active region includes n^+ source and drain areas (doping: $10^{20}cm^{-3}$) and a p-type channel (doping: $10^{16}cm^{-3}$). The channel is composed of three regions. The middle part, W_m, is under the primary gate G_1 and is $500nm$ wide. G_1 is referred to as the primary gate, as its role is similar to the role of the gate in the single gate structures introduced previously in figure 2.1. On the two sides, the channel is made of nanowires whose widths on the source and drain sides, W_s and W_d, are less than $60nm$ ($W_s = W_d \equiv W_{NW}$). The nanowire on the drain side is $200nm$ long and is covered by G_1. The nanowire on the source side is $300nm$ long and is covered by the secondary gate G_2. G_2 covers the front and back of the nanowire too. The work-function of both gates is $4.17eV$. The two gates are separated from the active region underneath by a layer of $20nm$ thick gate oxide. The separation between the gates is $50nm$. Throughout this section this device is referred to as 'Narrow-Wide-Narrow' (NWN or NWN_x), where 'x' represents the nanowire width W_{NW}.

The wide middle part of the channel is the main region of absorption. Nanowires absorb light too, but their primary role is to enhance the photocurrent and lower the dark current as we will explain later. The photo-response of NWN will be compared with that of a SOI MOS phototransistor with a single gate (figure 2.1), whose channel is $500nm$ wide. Other dimensions and doping profiles of SOI MOS are similar to those of NWN. The main reason for choosing SOI MOS as the control is that it generates the largest amount of photocurrent, among the family of single-gate phototransistors with the same channel length, and channel width of less than $500nm$ (figure 2.4).

The solid blue line in figure 2.12(a) represents the drain current versus the 'primary' gate voltage of a NWN$_{60}$ ($W_{NW} = 60nm$). The result for SOI MOS is plotted by the red line. At $V_{G1} = -2V$, the photocurrent of NWN$_{60}$ is more than 7 times larger than that of SOI MOS. This leads to a photo-responsivity of $1.04 \times 10^4 A/W$ at the intensity of $0.01mWcm^{-2}$ for NWN$_{60}$; while the responsivity of the SOI MOS is $1.2 \times 10^3 A/W$ at the same intensity. The dark current versus temperature graphs for the two aforementioned structures are plotted in figure 2.12(b) (Inset: Drain current versus V_{G1} at $T = 475K$). At $V_{G1} = -2V$, the dark current of NWN$_{60}$ is just slightly larger than that of the SOI MOS.

The improved performance of the NWN is attributed to the better control of the gates over the nanowires energy band when compared to wider channels. As plotted in figure 2.13(a), the potential barrier of NWN$_{60}$ is lower than that of the SOI MOS. The current increases exponentially with reducing the barrier height. It also linearly depends on the nanowire width, W_{NW}.

(a)

(b)
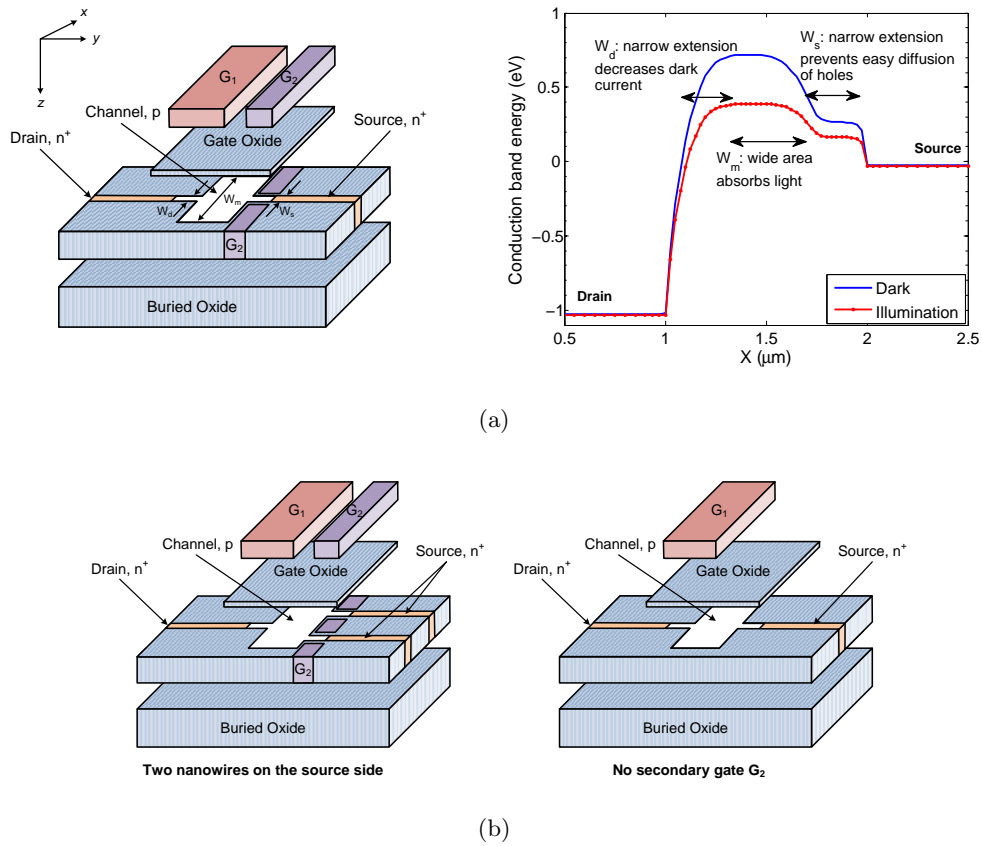
Figure 2.11: (a) Multiple gate NWN phototransistor, along with its energy band diagram. The widths of the nanowires on the source and drain sides, W_s and W_d, are both $60nm$. $W_m = 500nm$, and the total channel length is $1\mu m$. Active region thickness: $200nm$. Channel doping: $10^{16}cm^{-3}$. (b) Left: NWN photodetector with two nanowires on the source side. Right: NWN photodetector without the secondary gate G_2. Light is shined through a $0.5 \times 0.5\mu m^2$ window over the channel.

As a result, the lower barrier of NWN$_{60}$ overcomes the smaller channel width and results in a larger photocurrent.

The low potential barrier in NWN$_{60}$ is created by the small nanowire on the source side. The nanowire acts like a *'funnel'*; its small cross sectional area prevents the holes from diffusing into the source as easily as those in SOI MOS. The lateral bipolar action is then enhanced, causing more change (lowering) in the barrier height (figure 2.13(a)) and therefore a larger photocurrent.

In order to further explain the concept of funneling effect, we added a second $60nm$ nanowire to the source side, and covered it by the secondary gate on top and two sides, exactly the same way as the first nanowire (figure 2.11(b), left). We obtained the photocurrent while keeping all

(a)   (b)
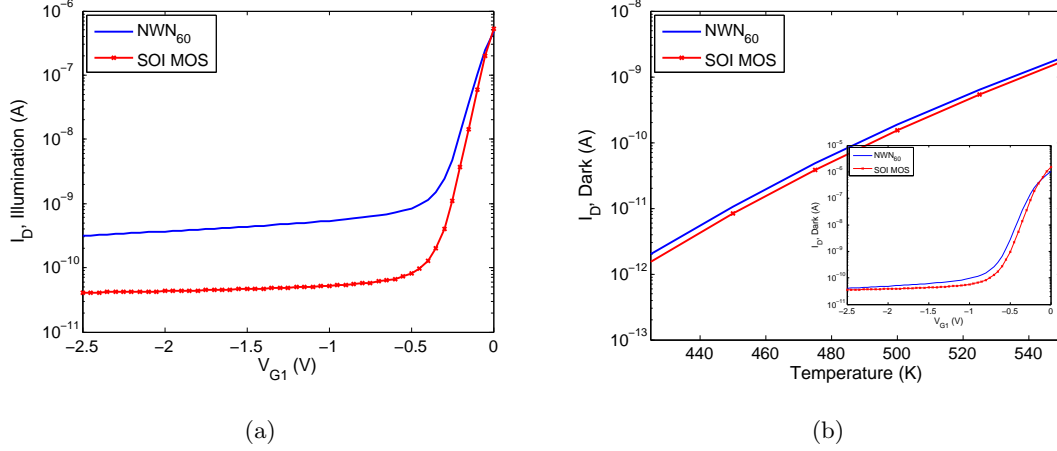
Figure 2.12: (a) Drain current versus gate voltage of NWN_{60} (figure 2.11(a)) and SOI MOS (figure 2.1(a)), under illumination. Light intensity is $0.01mW/cm^{-2}$ and light is illuminated through a $0.25\mu m^2$ window. (b) Dark current versus temperature for NWN_{60} and SOI MOS; inset: Drain current versus V_{G1} at $T = 475K$. Channel doping: $10^{16}cm^{-3}$. $V_S = 0V$, $V_D = 1V$, and $V_{G2} = 0V$ (where applicable).

of the other parameters the same. The photocurrent, plotted in figure 2.13(b), is decreased by a factor of 1.9 in comparison with the photocurrent of NWN_{60} (that is also added in the figure). In the device with two nanowires on the source side, the extra diffusion pathway that is provided for the holes weakens their impact on pulling down the barrier, as plotted in figure 2.13(a). As a result the photocurrent is dropped in comparison with the photocurrent of NWN_{60}.

The zero biased secondary gate (G_2) also plays an important role in the photocurrent. Biasing the secondary gate in depletion mode pulls down the barrier under G_2. As a result, the base effective length in the lateral bipolar transistor is reduced, and this can potentially impact the current. In fact as shown in figure 2.11(b), if G_2 in NWN is removed, the barrier height will not change significantly in comparison with NWN_{60} (figure 2.13(a)). However, due to the removal of G_2, the longer base causes the photocurrent to decrease, as plotted in figure 2.13(b).

We remark that the barrier change by G_2 (shorter channel) can come at the price of a high dark current. We have suppressed this by the aid of the primary gate G_1 and also the channel geometry by adding a nanowire on the drain side. As shown in figure 2.13(c), the barrier of the nanowire underneath G_1 (figure 2.11(a)) is controlled more effectively by the negative gate in comparison with SOI MOS channel. In fact, despite the fact that the position of G_1 relative to drain is the same in both NWN_{60} and SOI MOS structures, the barrier of NWN_{60} is shifted towards the drain side due to the stronger gate control on the nanowire. In addition, the small
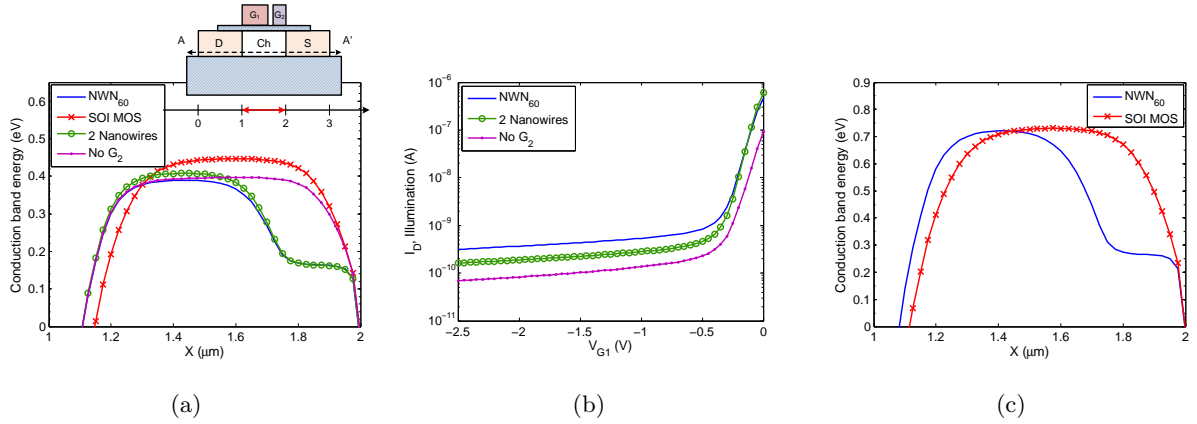
Figure 2.13: Energy band diagrams of NWN_{60} (figure 2.11(a)), SOI MOS (figure 2.1(a)) and two modified NWN structures (figure 2.11(b)) under illumination. (b) Drain current versus primary gate voltage of the modified NWN structures under illumination. Intensity: $0.01mW/cm^2$. (c) Energy bands of NWN_{60} and SOI MOS along the channel, under dark, at $T = 475K$. $V_S = 0V$, $V_D = 1V$, $V_{G1} = -2V$, and $V_{G2} = 0V$ (where applicable).

cross sectional area of the nanowire on the drain side keeps the dark current low in NWN_{60}, as the dark current is mainly due to the drift of the minority carriers in the channel towards the drain.

2.4.1 Role of Nanowire Width and Length

In the previous section, the nanowires of the NWN structure were $60nm$ wide and a few hundreds of nano-meters long. In this section we aim to better understand the role of nanowires on the device performance. Therefore, we model the drain current as a function of nanowires width and length.

Figure 2.14 illustrates how the width of the nanowire on the source side (W_s) affects the drain current. We note that the nanowire width on the drain side is kept fixed at $60nm$. The red curve in the figure represents the impact of nanowire width on the photocurrent. The blue curve shows the effect of nanowire width on the dark current. Dark currents are obtained at $T = 475K$.

The nanowire width on the source side plays an important role in the photocurrent. As W_s is decreased, the photocurrent is increased as plotted in figure 2.14(a). A narrower W_s increases the dark current as well, but in a more gentle way compared to the photocurrent. This behavior becomes more clear by studying the conduction band energy of the structures with different values

of W_s. The energy bands for two cases of $40nm$ and $0.5\mu m$ are shown in figure 2.14(b). The impact of the secondary gate on the barrier (at $1.8\mu m \leq X \leq 2\mu m$) becomes more pronounced as the nanowire width is reduced. At dark, change of W_s has not changed the overall barrier height tangibly. Besides that, at dark the source - channel junction is reverse biased, and therefore the exponential dependency of the current on the barrier height is negligible. The current change is therefore a result of changing the effective width of the channel (base) region, with almost no dependency on the barrier height. The current increases as the source region gets narrower, but not in an exponential manner. Under illumination, on the other hand, the funneling effect causes the barrier height of the structure with narrower W_s to drop more (figure 2.14(b)). The channel - source junction is also forward biased and the dependency of the current on the barrier height is exponential. As a result, under illumination, the increase in the photocurrent is more in comparison with the case of dark.

(a)	(b)
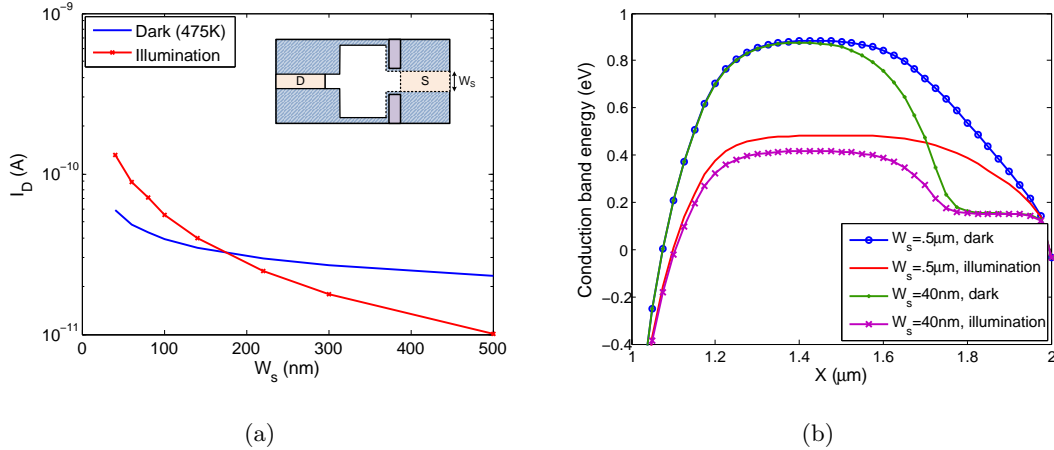
Figure 2.14: (a) Drain current versus nanowire width on the source side (W_s), while the nanowire width on the drain side is $60nm$ (NWN structure in figure 2.11(a)). (b) Conduction band energy of two structures with W_s of $40nm$ and $0.5\mu m$, under dark and illumination. The energy bands are obtained along the channel, at $5nm$ above the bottom oxide-semiconductor interface. Light intensity=$2.4\mu W/cm^2$ and the number of photons striking the channel per second is kept the same. $T = 475K$ for dark.

Figure 2.15 illustrates how changing the width of the nanowire on the drain side, W_d, impacts the current. Similar to the previous case, here the nanowire width on the source side is kept fixed at $60nm$. As plotted in figure 2.15(a), W_d has a stronger impact on the dark current, and a weaker impact on the photocurrent. Studying the conduction band energy of two structure with $W_d = 40nm$, and $0.5\mu m$ (figure 2.15(b)) shows that W_d is effective in changing the effective

length of the channel (base), and not the barrier height [9]. Besides that, on the source - channel side, where the hole diffusion takes place, the energy band is independent of W_d.

At dark, both junctions are reverse biased and therefore the current is mainly determined by the minority carriers in the channel that drift towards the drain [10]. As a result, the dark current is expected to linearly depend on W_d, as illustrated in figure 2.15(a). The small deviation from linearity is due to the variation in the effective channel length, as well as the change in the electric field on the drain-channel side (figure 2.15(b)).

Under illumination, the source-channel junction is forward biased and the photocurrent depends on the barrier height, which has not changed as a function of W_d, as shown in figure 2.15(b). As a result, the photocurrent does not change as much as the dark current. The small increase in the photocurrent (figure 2.15(a)) is a result of decrease in the channel effective length as W_d becomes wider.

| (a) | (b) |
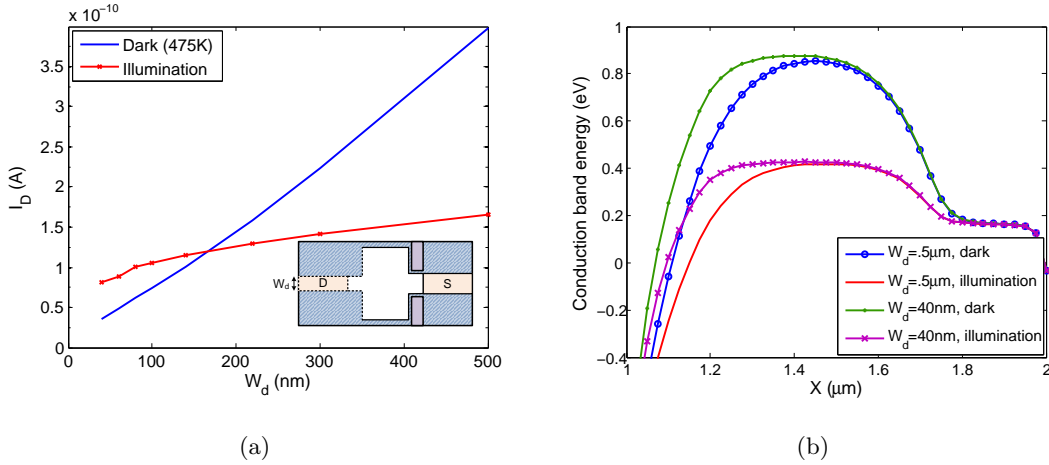
Figure 2.15: (a) Drain current versus nanowire width on the drain side (W_d), while the nanowire width on the source side is $60nm$ (NWN structure in figure 2.11(a)). (b) Conduction band energy of two structures with W_d of $40nm$ and $0.5\mu m$, under dark and illumination. The energy bands are obtained along the channel, at $5nm$ above the bottom oxide-semiconductor interface. Light intensity=$2.4\mu W/cm^2$ and the number of photons striking the channel per second is kept the same. $T = 475K$ for dark.

Overall, a large photocurrent is achievable with either a narrow nanowire on the source side

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[9]Unless the length of the nanowire on the drain side is increased. This is discussed later when we investigate the impact of the nanowire lengths.

[10]This is because the doping of the channel is smaller than that of the drain. Moreover, the electric field of the drain-channel junction is stronger than that of the source-channel junction.

(figure 2.14(a)), or with a wide nanowire on drain side (figure 2.15(a)). However, wide wires on the drain side increase the dark current. Therefore, in order to obtain a large photocurrent, as well as a small dark current, the nanowire widths on both sides must be small.

The effect of the nanowire lengths on the drain current is plotted in figure 2.16. Here, the nanowires on both sides are $60nm$ wide. In addition, the total length of the channel is fixed; as a result, when the length of the wire on one side is changed, it causes the length of the wide middle area to change as well. We also remark that for the results presented, the window opening for light is equal to the area of the narrow and wide regions. Therefore, the size of the window changes as the nanowire length is changed.

In figure 2.16(a) the effect of the nanowire length on the source side (L_s) is investigated. Here the nanowire on the drain side is $200nm$ long. Increasing the length of the nanowire on the source side strengthens the effect of G_2 on lowering the potential barrier; which leads to an increase in the photocurrent. However, this will increase the dark current at the same time. This is due to the fact that increasing L_s will eventually cause G_1 to become less and less effective on the barrier height. In fact after around $300nm$ the increase in the dark current is more rapid than the increase in photocurrent, which is not desirable. In addition, by making the nanowire long, we decrease the length of the middle wide area (L_{wm}); this in turn decreases the area of light absorption. As a result, the nanowire length on the source side should not exceed a limit.

The change in the drain current as a function of the nanowire length on the drain side, L_d, is investigated in figure 2.16(b). This time, the length of the nanowire on the source side is kept fixed at $300nm$. Increasing the nanowire length on the drain end will strengthen the impact of G_1 over the potential barrier. This would decrease the current at both dark and illumination conditions. In addition, increasing L_d causes the area of the wide region at the middle of the channel (L_{wm}) to decrease, and this is another cause that degrades the photocurrent.

2.5   Discussion

The figures of merit of the photodetectors introduced in this chapter are compared in table 2.2. The channel doping for these devices ranges from $10^{14} cm^{-3}$ to $4 \times 10^{17} cm^{-3}$. More information about the details of calculating the figures of merit is available in chapter 1 and also in appendix B.

The data in the table is obtained under ideal circumstances, and shows that junction transistors are potentially able to generate large optical gains, and detect low levels of light intensity.
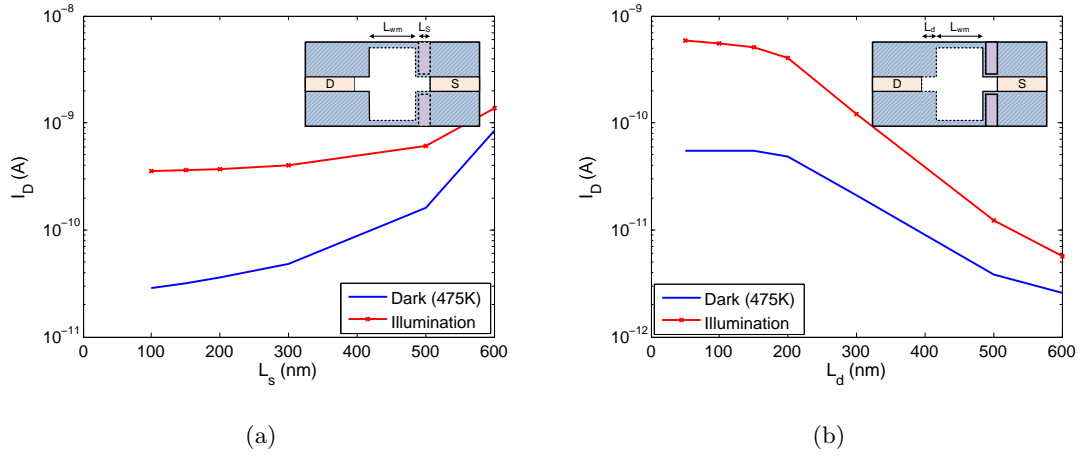
Figure 2.16: (a) Drain current versus nanowire length on the source side (L_s). The nanowire length on the drain side is $200nm$ (NWN structure in figure 2.11(a)). (b) Drain current versus nanowire length on the drain side (L_d). The nanowire on the source side is $300nm$ long. The total channel length is $1\mu m$, and hence L_{wm} is varied in each experiment. $T = 475K$ for dark.

The table shows that the lowest dark currents belong to the single gate MOS devices [11], with the channel width of $60nm$. As discussed earlier in this chapter, the small cross sectional area of the channel helps to have a strong gate coupling and a high potential barrier that lead to a small dark current. The dark current is smaller when the doping level of the channel is higher, as it helps to keep the bulk potential barrier at a higher level. Despite the mediocre optical gain of the single gate MOS_{60} structures, their very low level of dark current is responsible for the small NEP, and the ability of such devices to detect a very low photon rate.

However, we remark that for the data presented in table 2.2, 'ray tracing' method is used to model the illumination case. In reality for the devices with narrow nanowires, a smaller percentage of absorption is expected; which can lead to a smaller level of photocurrent. The NWN structures (NWN_{60} and NWN_{30}) are less vulnerable to such problem, as the wide region of the channel can absorb light more efficiently. Although the dark current in NWN is larger, the geometry of the structure and the use of multiple gates result in a device with the highest optical gain among the other devices, which in turn can compensate the slightly larger level of dark current and give the device the advantage of a low NEP as well.

We should however note that under non-ideal conditions, the large surface to volume ratio of nanowires makes them more vulnerable to the surface recombination issues, in comparison

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[11]In table 2.2, single gate SOI MOS devices are presented as MOS_x, where x represents the channel width.

Table 2.2: Comparison of junction phototransistors

Device	Ch doping (cm^{-3})	I_{Dark} (A)	Optical gain	Responsivity (AW^{-1})	NEP (WHz$^{-0.5}$)	Photon rate (s^{-1})
MOS$_{500}$	4×10^{17}	2.9×10^{-17}	8.7×10^2	23.6	5.4×10^{-18}	18
	10^{16}	2.0×10^{-15}	3.9×10^4	1051.1	6.7×10^{-18}	22
	10^{14}	1.3×10^{-14}	1.8×10^5	5029.9	7.9×10^{-18}	25
MOS$_{60}$	4×10^{17}	3.2×10^{-18}	7.1×10^2	19.2	1.9×10^{-18}	7
	10^{16}	3.9×10^{-17}	5.4×10^3	147.9	2.5×10^{-18}	8
	10^{14}	5.1×10^{-17}	6.4×10^3	175.2	2.6×10^{-18}	9
Array$_{6 \times 60}$	10^{16}	1.1×10^{-15}	2.8×10^4	765.8	5.9×10^{-18}	19
NWN$_{60}$	10^{16}	3.6×10^{-15}	3.85×10^5	10485.5	2.8×10^{-18}	10
NWN$_{30}$	10^{16}	2.9×10^{-15}	8.2×10^5	22443.2	1.7×10^{-18}	6

Single gate SOI MOS devices are presented as MOS$_x$, where x represents the channel width.

The doping level at the source and drain regions is $10^{20} cm^{-3}$. The semiconductor thickness is $200 nm$.

A surface reflection of 30% is considered. The photocurrent presented here is multiplied to transmission.

The noise sources considered in calculating the NEP are input and source shot noise, and also the thermal noise of the channel. We did not calculate the Flicker noise, as it strongly depends on how the device is fabricated. The load is considered to be infinitely large; otherwise the thermal noise of the load at room temperature dominates.

to wide channels. A device with a poorly passivated surface can exhibit a higher level of dark current, due to the weaker gate control over the channel. The photocurrent can also be lower than ideal, due to the recombination of the photo-generated carriers at the surface states. Surface recombination is strongly dependent on the fabrication process, and we will investigate it later in the coming chapters.

2.6 Chapter Summary

In summary, in this chapter we investigated the role of nanowires incorporated in junction phototransistors. Starting with simple, single gate structures, we found that nanowires are more effective in decreasing the level of dark current, due to the better control of the gate over their potential barrier. However, we did not find any improvement in the photocurrent of single gate nanowire devices (in accumulation), when compared with wide channel photodetectors.

The ability to effectively engineer the energy band of nanowires encouraged us to propose a new device geometry. The new device is composed of two nanowire/gate regions for electrostatic control, and a wide channel for efficient light absorption. With this geometry, the photocurrent of

the device in the accumulation is increased. We further studied the physics behind the improved operation of the structure, by investigating the role of nanowire width and length in order to optimize the current. Selecting narrower nanowires improves the detector response in terms of both photo- and dark current. The new *narrow-wide-narrow* geometry potentially exhibits a large optical gain, as well as a small NEP.

Chapter 3

Nanowire based Junction-less Phototransistors

The main theme of this chapter is on incorporating nanowires in junction-less phototransistors. Junction-less structures are of interest due to two main reasons. The first is the native gain of the phototransistor that can compensate the poor absorption in nanowires. The second reason is the advantage of a simpler fabrication, as all the extra steps required for doping the source and the drain regions in a top-down approach are eliminated. Using Silicon on Insulator (SOI) substrates in top-down methods would also ease the fabrication of the nanowires. In addition, regardless of the fabrication approach, SOI substrates facilitate the creation of the gate terminal by providing the buried oxide as the gate dielectric and the bottom silicon substrate as the gate [86, 88, 101], although it is possible to pattern and create the third terminal on top of the channel [91].

Examples of prior works on junction-less transistor geometries include n- and p- type Si nanowire based photodetectors [88], Si, and ZnO nanowire detectors with interface states that separate the carriers and increase the recombination lifetime [81, 82, 102], and Ge, ZnO, Si, and GaN nanowire based photodetectors with back gates [86, 101, 103, 104]. The gate in a junction-less transistor is able to switch OFF the charge flow within the nanowire channel, by depleting the nanowire out of majority carriers and creating a potential barrier. The amount of charge flow and the device ON-OFF states are controlled by the height of the potential barrier [105]. Although as a photodetector the device can be biased in either ON or OFF states, the focus of this chapter is the OFF state. Under this circumstance the dark current, and therefore the dark current shot noise are both low. When biased in OFF state, the operating principle of the device is very similar to the lateral bipolar action [98] that was explained in chapter 2, and will be discussed very briefly.

A low level of dark current is a great advantage of junction-less phototransistors over photoconductors. However, lack of junction can lead to a low optical gain. The quantum efficiency of a small size nanowire would also be low. Both of these issues could lead to a poor noise equivalent power (NEP) for the phototransistor. To address these issues, in this chapter we focus on junction-less transistors that are thicker in comparison with the devices in chapter 2, as this will increase the quantum efficiency of the device. After a brief investigation on the role of channel width on the output current, we propose ways to improve the performance of the junction-less phototransistor in terms of optical gain and sensitivity, by modifying the channel geometry, incorporating nanowires and band-gap engineering by using multiple gates.

3.1 Junction-less Phototransistors: Principle of Operation

Junction-less transistors operate rather differently compared to junction, MOS transistors [105]. Figure 3.1 (a) shows a SOI junction-less transistor, made out of lightly doped p-type silicon. The gate is located over a thin layer of dielectric at the center of the channel. The drain and the source contacts are biased at $0V$ and $0.5V$, respectively.

During the OFF state, a positively biased gate depletes the channel out of the majority carriers. As a result, a potential barrier is built up which prevents the charge flow. The energy band diagram of the device, plotted in figure 3.1(b) in solid blue, clearly shows the gate effect in creating the potential barrier. This causes the source current to drop, as shown in figure 3.1 (c) in blue ($V_G > 0$) [1]. When the gate voltage is swept towards negative values, the majority carrier concentration in the channel is increased. This consequently reduces the barrier height (red curve in figure 3.1(b)); the source current increases and the device is considered to be in ON state, as plotted in figure 3.1(c) (blue curve, $V_G < 0$).

The red curve in figure 3.1(c) shows the change of source current versus the gate voltage, when the junction-less transistor is illuminated. The light source is monochromatic, with the wavelength of $630nm$. The graph shows that illumination changes the source current by orders of magnitude when the phototransistor is OFF ($V_G > 0$). As mentioned earlier, we are specifically interested in biasing the gate in this region, although the drain current is much larger when the transistor is ON. This gives us the opportunity to detect low level intensities. Here, the operating principle is very similar to the lateral bipolar action [98].

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[1]Since the channel is depleted from holes, the structure looks like a *pnp* transistor. As a result, here we bias the source contact and measure the source current.
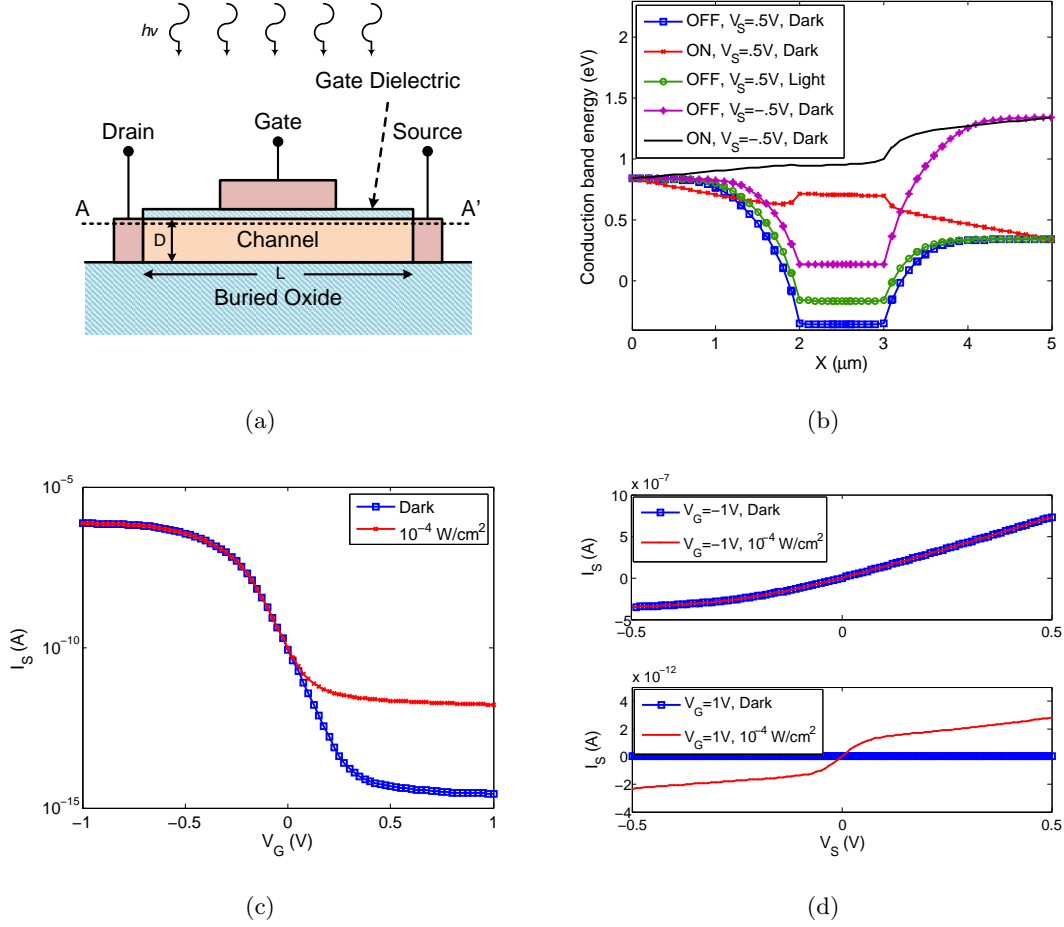
Figure 3.1: (a) Single gate junction-less phototransistor. The semiconductor is p-type silicon with doping level of $10^{15}cm^{-3}$ and thickness (D) of $350nm$. The width (W) and the length (L) of the channel are $2\mu m$ and $5\mu m$, respectively. The gate covers the central $1\mu m$ of the channel length, and is located over $20nm$ silicon dioxide. Light is shined through a window with the area of $3.6\mu m^2$. (b) Energy band diagram of the phototransistor, along the channel (cutline AA'). The blue and green curves represent the energy band under positive gate bias and the red curve shows the energy band under negative gate bias ($V_S = +0.5V$). The purple and the black curves show the energy band when $V_S = -0.5V$. (c) Source current versus gate voltage, under dark and illumination conditions. (d) Source current versus source voltage at gate voltage of $-1V$ (top), and $1V$ (bottom).

When the channel is illuminated, most of the photo-generated majority carriers (here, the holes) easily travel towards the contacts in response to the high electric field. The minority carriers (here, the electrons) trap inside the potential barrier created by the gate (OFF state).

To satisfy the charge neutrality the barrier height is reduced, as shown with green in figure 3.1(b). A lower potential barrier creates a pathway for the trapped minority carriers to diffuse; but more importantly it eases the overall carrier flow and pushes the transistor towards ON state. The overall photocurrent therefore increases, as plotted in red in figure 3.1(c).

The change of the source current versus the source voltage is plotted in figure 3.1(d). Unlike photoconductors, here the current does not necessarily have a symmetrical behavior with respect to the source bias. Although asymmetry in the current-voltage curve can occur as a result of different metal work-functions at source and drain [106], in this example it is because of the asymmetric shape of the potential barrier due to the gate bias. This is better clarified by comparing the energy band of the structure at source voltages of $-0.5V$ and $+0.5V$ in figure 3.1(b). At $V_G = 1V$, the energy band has very symmetrically flipped as the drain voltage is changed from $0.5V$ (blue) to $-0.5V$ (purple). The current is therefore symmetric (figure 3.1(d), bottom). On the other hand, when $V_G = -1V$, the energy bands at $V_S = 0.5V$ and $V_S = -0.5V$ look different (red and black). This results in an asymmetric source current, as plotted in figure 3.1(d), top.

3.1.1 Role of Channel Width and Doping

For discussion and demonstration purposes, we use the wavelength of $630nm$ in this section. In junction-less transistors, the channel is normally very thin [105] to ensure the gate is able to fully deplete it. Considering the relatively small absorption coefficient of silicon at the wavelength of interest ($\approx 3.9 \times 10^3 cm^{-1}$), the drawback of the thin absorption region is low quantum efficiency. Although the quantum efficiency can be improved by use of anti-reflection layers and mirrors, we choose a silicon thickness of $0.85\mu m$ for this work to increase the quantum efficiency of the phototransistor.

When the channel is thick, depleting the channel can be challenging, especially at high doping concentrations. In order to safely increase the thickness of the semiconductor layer, we use the same concept that is used in junction-less transistors [105], and replace the channel underneath the gate with a narrow layer, as marked with NW_1 in figure 3.2. This allows for introducing the gate in three dimensions, which helps to complete the depletion of the channel. We name the gate as 'primary gate', since later we will add another gate to the design. The semiconductor is considered to be p-type, and therefore the primary gate has to be biased positively to keep the phototransistor in OFF state. In this section we investigate how the channel width and doping level would affect the device output current.
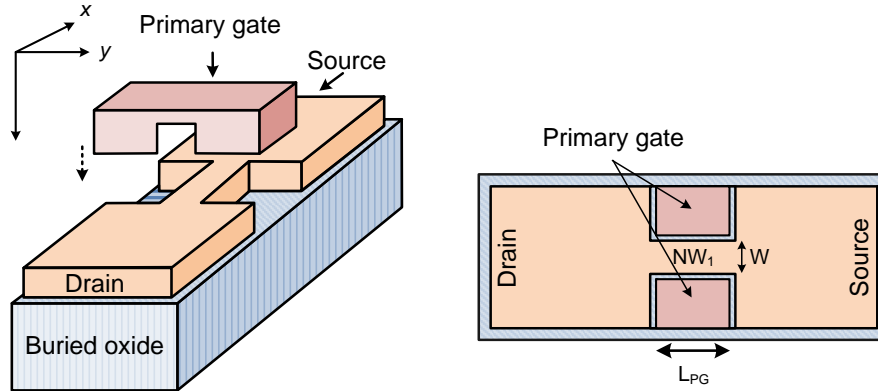
Figure 3.2: Single gate, junction-less phototransistor with nanowire channel. The semiconductor is p-type silicon with doping level of $10^{15} cm^{-3}$ and thickness of $0.85 \mu m$. The length of the channel is $5 \mu m$. The channel is $2 \mu m$ wide everywhere except the NW_1 region. The gate covers the central $1 \mu m$ of the channel length, and is located over $20 nm$ silicon dioxide.

Figure 3.3 shows how the source current changes as a function of the width of NW_1. The length of the detector is $5 \mu m$, and data is obtained for both dark and illumination conditions, while the gate and source contacts are biased at $+1V$ and $+0.5V$, respectively. The semiconductor doping is $10^{15} cm^{-3}$ in figure 3.3(a) and $10^{16} cm^{-3}$ in figure 3.3(b). For both cases, as the width of NW_1 is decreased, the current drops almost exponentially. At the same time, the ratio of the photocurrent to dark current increases, until the channel width is about $1 \mu m$ in figure 3.3(a) and less than about $0.4 \mu m$ in figure 3.3(b). For narrower channels, the current to width dependency becomes less exponential; until the current becomes almost flat for both dark and illumination conditions.

Since the current trend is very similar for the two doping levels, we focus on the structure with semiconductor doping of $10^{15} cm^{-3}$. When the channel is wide, the gate control is not strong enough to deplete the whole depth (thickness) of the channel. The barrier height of the junction, shown in blue in figure 3.4(a), is obtained along the channel, at cutline AA' close to the bottom of the structure (far from the top gate), at the middle of the channel. It clearly shows that the barrier height is low. In addition, the electron and hole concentrations along cutline BB' (figure 3.4(d)) across the channel, shown in figure 3.4(b), both confirm that the depletion is local. As a result, except for some areas that are close to the gate, the carriers do not see a large potential barrier. The lateral bipolar transistor is in ON state, and the current dependence on the barrier height is exponential. Under this circumstance, when the channel width is decreased, as long as the device is not OFF, the increase in the potential barrier (due to the decrease in channel
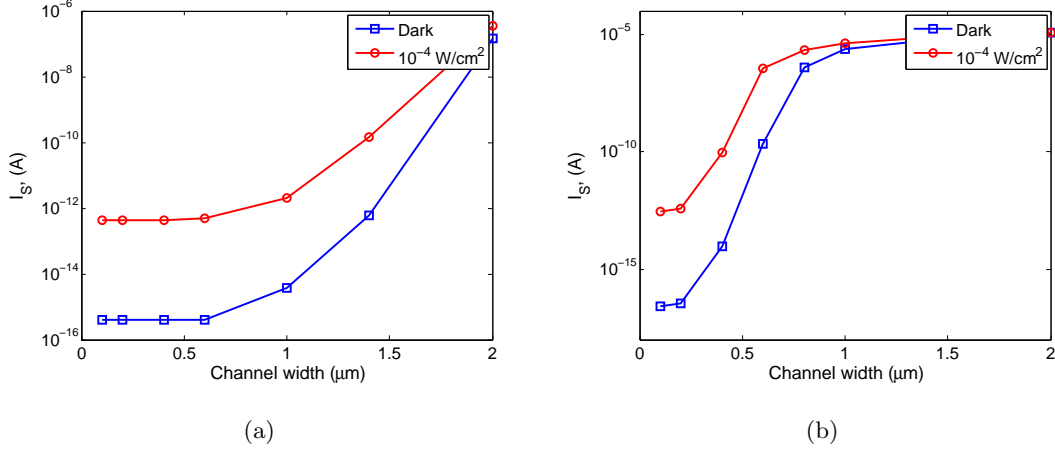
Figure 3.3: Source current versus channel width in a single gate, junction-less phototransistor with nanowire channel (figure 3.2) when the semiconductor doping is (a) $10^{15}cm^{-3}$, and (b) $10^{16}cm^{-3}$. $V_G = 1.0V$, $V_S = 0.5V$, $V_D = 0V$.

width) causes the source current to drop exponentially. This is true for channels wider than about $600nm$ under both dark and illumination conditions, as the photo-generation would just reduce the barrier height of an already ON transistor.

Below $600nm$ the channel is already depleted as confirmed by the energy band diagram in figure 3.4(a). In addition, the electron concentration for $400nm$ and $100nm$ wide channels in figures 3.4(c) and (d) is larger than the doping level of the silicon layer ($10^{15}cm^{-3}$). Here, the barrier is high enough to consider the bipolar transistor in OFF state under dark condition. As a result, there is no exponential dependency of the current on barrier height at dark. The resulting leakage current originates from the minority carriers (electrons) at the source and drain, that drift towards the channel; and also from the minority carriers (holes) in the channel, that drift towards source and drain. Since the doping level of the source and drain ($10^{15}cm^{-3}$) is lower than the concentration of the electrons in the channel (figure 3.4 (c) and (d)), the contribution of the channel becomes negligible. As a result, for devices with channel width of smaller than $600nm$, the overall dark current becomes independent of the channel width.

Under illumination, the barrier height decreases and the device is considered ON. Therefore, the current depends on the carrier diffusion in the channel-source region, as well as the cross sectional area. Since the electron concentration in the channel (figure 3.4(c) and (d)) is more than the hole concentration in the source, we expect the electron diffusion to be dominant. As for the cross sectional area, we should emphasize that the junction is artificially created by applying a gate voltage and not by directly doping the channel area. As a result, the carrier concentration

is not uniform all over the channel (figure 3.4(c) and (d)). The electrons that are located at the center of the channel have very small contributions in the diffusion current, as the concentration of these carriers is low. The highly concentrated electrons at the inverted regions of the channel are those that play the major contribution to the current. Such electrons are concentrated at very narrow regions close to the interface, regardless of the channel width. As a result, the drain photocurrent remains almost constant for channel widths of below $600nm$.

(a)

(b)

(c)

(d)
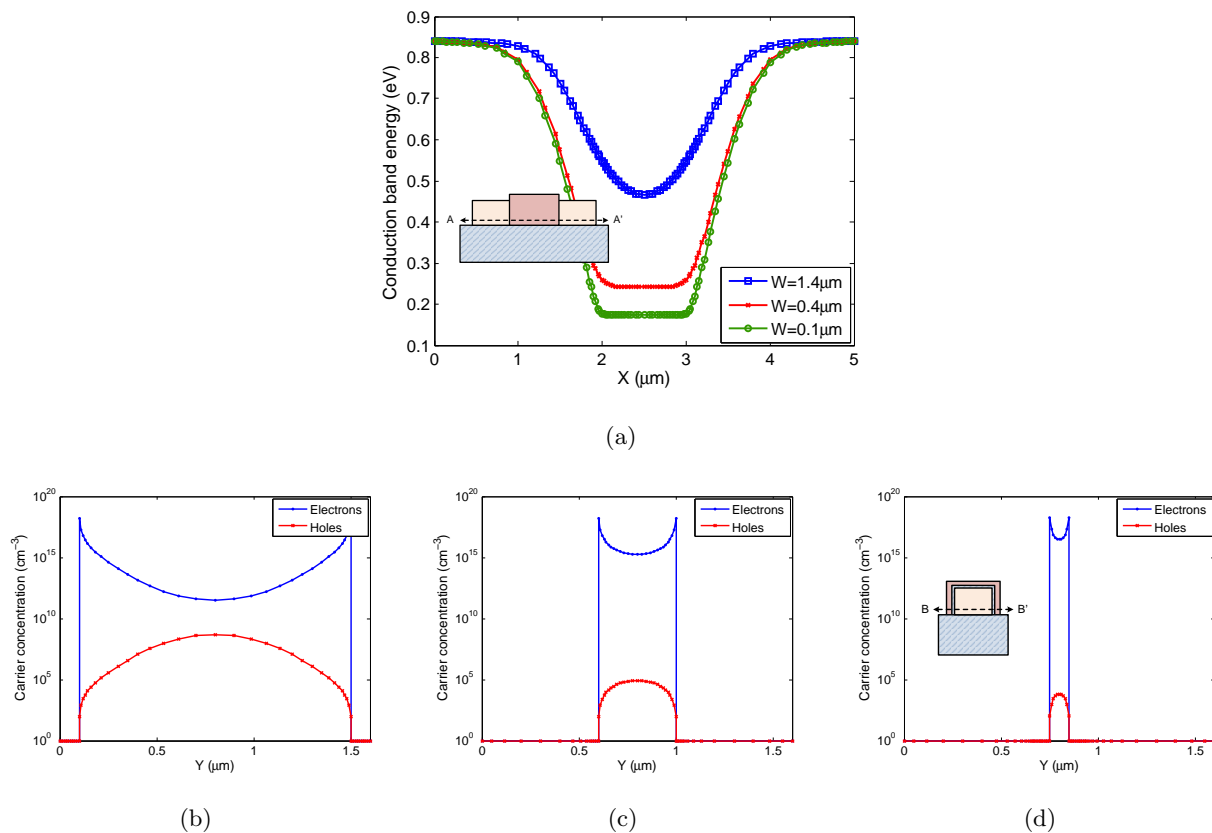
Figure 3.4: (a) Energy band diagram of three single gate nanowire phototransistors (figure 3.2) with widths of $600nm$, $400nm$ and $100nm$, along the channel (cutline AA'). $V_G = 1.0V$, $V_S = 0V$, $V_D = 0V$. (b)-(d) Electron and hole concentration of the aforementioned structures at cutline BB' across the channel.

Figure 3.5 shows how the figures of merit of the device (optical gain, responsivity, normalized dark noise, and minimum detectable photon rate) change as a function of the channel width. Details of calculating the noise and figures of merit are described in Appendix B. Decreasing the channel width causes the illumination current to drop (figure 3.3(a)); as a result, the optical gain (blue) and similarly the responsivity (red) decrease proportional to the photocurrent. The

dark current noise (green, normalized value is plotted) also decreases; however, we remark that such noise is proportional to the dark and not the photocurrent. As a result, the minimum detectable photon rate (purple), or similarly the NEP, is large at wider channels where the noise to responsivity ratio is high; and small for narrow channels since the noise level drops. At channel widths narrower than $600nm$, the minimum photon rate does not change much, as the photocurrent (and as a result the responsivity) and the dark current (therefore noise) do not change drastically.
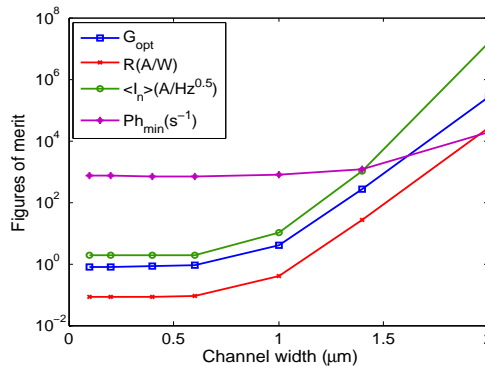
Figure 3.5: Figures of merit versus channel width. Similar to figure 3.3(a), the channel thickness is $0.85\mu m$, and $V_G = 1.0V$, $V_S = 0.5V$, $V_D = 0V$.

3.1.2 Role of Gate Length

Analysis of the channel width has shown that below a certain width the current does not change and therefore there is no benefit in reducing the channel width any further. However, studying the role of the length of the narrow region, NW_1, gives us more insight about this [2]. We note that it is desirable for a photodetector to have a wide surface area, in order to absorb photons more efficiently. As a result, the length of NW_1 is best reduced. The risk of reducing the length of NW_1 is the incomplete depletion of the channel, due to short channel effects, unless the width of the nanowire is reduced. The graphs for the sub-threshold slope versus the gate length of two structures are plotted in figure 3.6(a). The width of NW_1 in the first structure is $600nm$ and in the second structure is $100nm$. In addition to the gate length, in the results presented here the length of the channel has also changed. The importance of having a narrower channel width is verified when the graphs for the two structures are compared. While the sub-threshold slope shows a similar trend for both structures, the slope has increased at a higher rate for the $600nm$

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[2]We remark that when we increase or decrease the length of the channel, we change the length of the gate contact accordingly. As a result, unless otherwise stated, we use the term *gate length* to express the same concept.

(a)   (b)
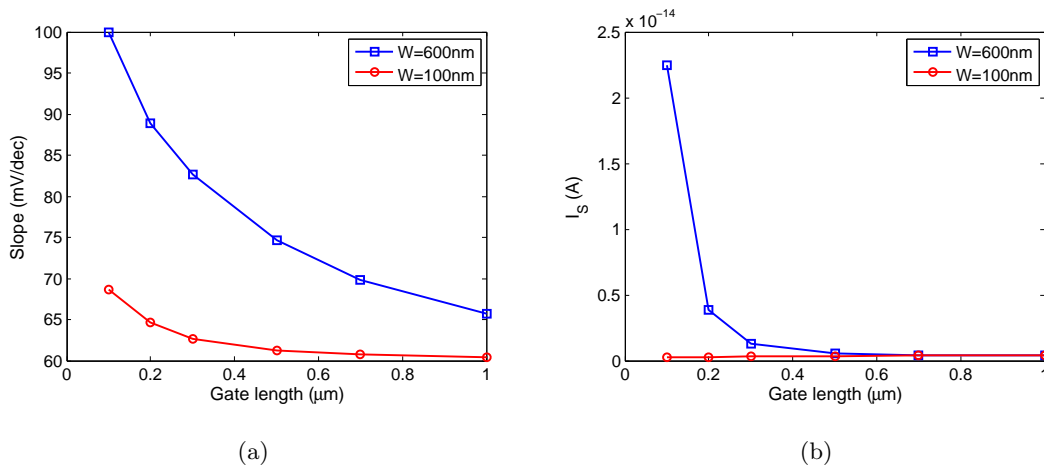
Figure 3.6: Single gate phototransistors with nanowire widths of $100nm$ and $600nm$, role of gate length L_{PG} (figure 3.2). (a) Sub-threshold slope versus gate length. (b) Dark current as a function of gate length. Data is obtained for semiconductor doping of $10^{15}cm^{-3}$. Dark current data for $100nm$ wide channel is obtained by simulating the device at high temperatures and estimating the room temperature current.

wide channel as the channel length is decreased. For the same structure, the dark current has also increased about 50 times when the gate length is decreased from $1\mu m$ to $0.1\mu m$, as shown in figure 3.6(b), while the dark current of the $100nm$ wide channel does not show much of increase.

3.2 Ideas to Increase the Optical Gain: Use of Multiple Gates

According to figure 3.5, junction-less photodetectors are potentially able to detect low level intensities. However, this is obtained at the cost of losing the optical gain, especially in devices with narrow channels. In this section, we propose a number of modifications to increase the optical gain. Combining with a low level of dark current, this would further improve the noise equivalent power. The key modifications come from the concept of bipolar transistors. In a well-designed bipolar transistor, the base length is short to guarantee that almost all of the majority carriers which have diffused from the emitter into the base can pass through the base length and enter the base-collector depletion region. In addition, to push the emitter efficiency toward unity, the structure doping must satisfy $N_{emitter} \gg N_{base} > N_{collector}$ [40]. In section 3.1.2 we discussed about ways to shorten the channel (base) length. The doping criterion however has not been considered yet. In the structure of figure 3.2, for narrow channels, the channel electron (majority carrier) concentration at positive bias can be orders of magnitude larger than the doping

concentration at the source (emitter), as shown in figures 3.4(c) and (d). This results in very poor emitter efficiency, and therefore a low optical gain. In this section, first we illustrate the role of doping the source region on the photocurrent of the device. Next we propose ways to implement a similar behavior in a junction-less geometry. The proposed device is published by us in reference [107].

Figure 3.7 illustrates how the source current varies as a function of the doping level on the source side. To obtain the data, we kept the device geometry similar to figure 3.2, as shown in figure 3.7(a). The gate is $1\mu m$ long and covers a $200nm$ wide nanowire. The semiconductor doping level is $10^{15}cm^{-3}$ on the drain side, as well as the area underneath the gate. The doping level on the source side is modified at $500nm$ after the edge of the gate contact, and is varied according to the graph in figure 3.7(b).

(a)   (b)
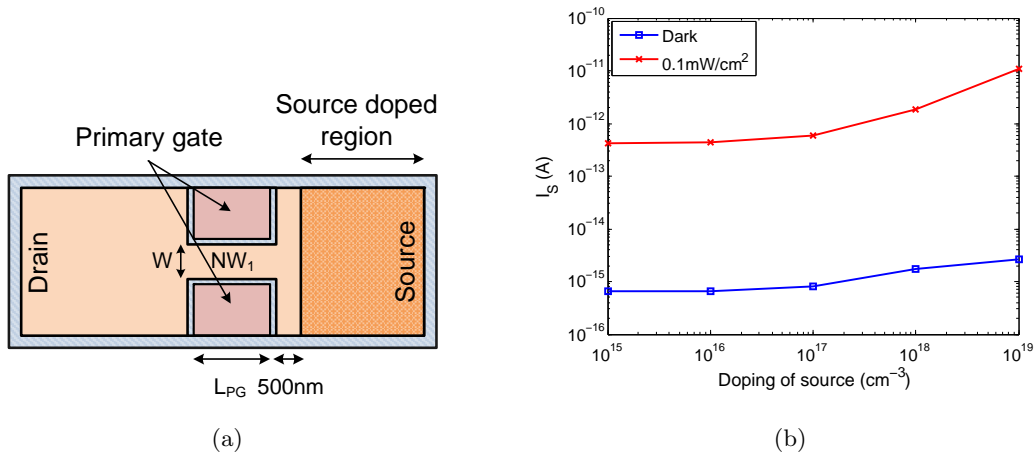
Figure 3.7: (a) Top view of the nanowire phototransistor with a higher doping concentration on the source side. (b) Source current versus doping level on the source side. The semiconductor doping is $10^{15}cm^{-3}$ elsewhere (p-type). Semiconductor thickness is $0.85\mu m$. NW_1 is $200nm$ wide. $L_{PG} = 1\mu m$, $V_G = 1.0V$, $V_S = 0.5V$, $V_D = 0V$.

Under both dark and illumination conditions the current increases as the source doping level is varied from 10^{15} (junction-less) to $10^{19}cm^{-3}$. This can be explained by studying the emitter efficiency of a one dimensional, pnp junction transistor, defined as [40]:

$$\gamma = \frac{I_{Ep}}{I_{Ep} + I_{En}} \tag{3.1}$$

where I_{Ep} denotes the current of the holes, diffusing from emitter (source) into the base (channel); and I_{En} is the current of the electrons that are injected into the emitter (source) form

the base (channel). By increasing the doping level at the source region, the hole diffusion current (from source into the channel) starts to dominate the electron diffusion current (from channel into the source). The ratio of I_{Ep}/I_{En}, and therefore the emitter efficiency both increase. As a result, one expects a larger source current.

We note that although dark and illumination currents have both increased (figure 3.7(b)), it looks like the highest to lowest current ratio is not the same for dark, and illumination conditions. In fact, one can see that while the source current under illumination has changed by more than 25 times, the dark current has only increased by about 4 times. The reason is that the emitter efficiency of a bipolar transistor does not remain constant when the transistor ON/ OFF status is changed. We will discuss about this further in this section.

There is an alternative way to satisfy the doping criteria. As plotted in figure 3.8, instead of actually doping the source region with acceptors, we use a 'secondary' gate to control the carrier concentration of the source, the same way we have used the 'primary' gate to control the carrier concentration over the channel in figure 3.2. The semiconductor doping is uniform throughout the whole device. The secondary gate is located in an area between the primary gate and the source contact. For a *p*-type semiconductor the secondary gate is biased negatively in order to increase the concentration level of holes in the source region. In addition to the secondary gate, more modifications are made in the structure of figure 3.8 that are summarized below:

- Since the impact of the gate in carrier accumulation is local, in order to make the gate effect more pronounced, the area underneath the secondary gate is also narrowed down, as shown by NW_2 in the top view of figure 3.8.

- The position of the primary gate is changed from the center of the device towards areas closer to the source. Here the goal is to increase the surface area for photon absorption between gate and drain, similar to the base and collector junction in a bipolar phototransistor [40].

- The channel underneath the primary gate is made of a nanowire NW_1. This helps us to reduce the primary gate length, without sacrificing the channel depletion [3].

When compared to the *NWN* structure in chapter 2, the device introduced here looks similar in terms of the overall geometry. Besides that, both detectors are biased in OFF state to operate under lateral bipolar action. However, we note that the lateral bipolar action in each device is

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[3]The narrow regions of NW_1 and NW_2 are more like narrow slabs and not nanowires in thick devices. However, the ultimate goal is to replace them with nanowires that bridge the thick, wide areas of channel and source.
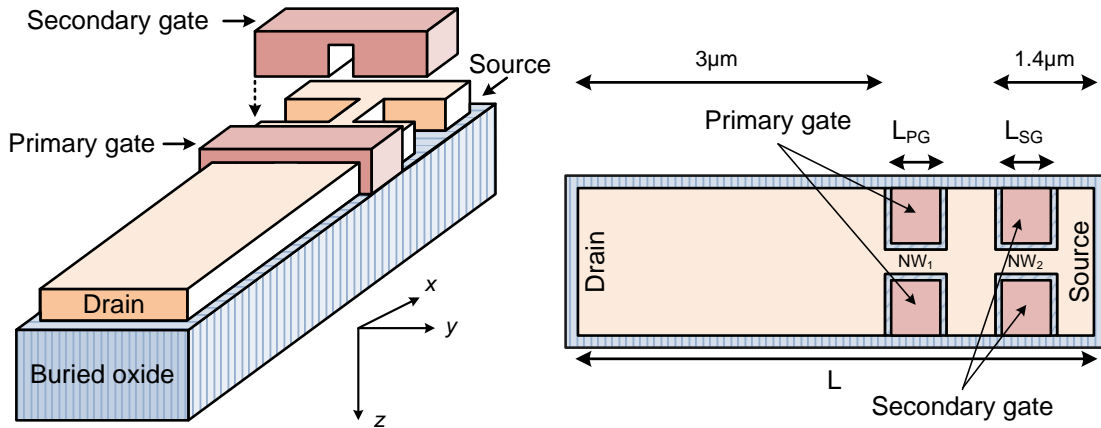
Figure 3.8: Junction-less phototransistor with multiple gates. Semiconductor is entirely *p*-type (doping: $10^{15}cm^{-3}$), with the thickness of $0.85\mu m$. The total channel length is $5\mu m$. The channel is $2\mu m$ wide everywhere except the narrow regions. The gate oxide is $20nm$ (not shown in figure). The secondary gate is lifted up to show the narrow region NW_2. A similar geometry is present underneath the primary gate that is shown in the top view, where the gates' top layer is removed. Light is shined through a window with the area of $5.6\mu m^2$.

maintained differently, due to the fact that the operating principles of the junction and junction-less transistors are different. In chapter 2, the OFF state was obtained via the reverse biased drain-channel *p-n* junction and the primary gate that accumulated the carriers within the channel. Whereas here, the potential barrier during the OFF state is created only by the primary gate that pushes the channel towards depletion and inversion. In both structures the nanowire/ secondary gate combination is used to benefit the electrostatic role of nanowires in increasing the optical gain; but here too, the implementation is different. The secondary gate in chapter 2 was added over the channel for the purpose of lowering the barrier by depleting the carriers. Here the role of the secondary gate is to *artificially* create a junction. This eliminates the need for having a doped *p-n* junction, and simplifies the design of the junction-less phototransistor.

3.2.1 Role of Bias and Nanowire Geometry

Figure 3.9(a) shows how the source current is influenced by the voltage of the secondary gate. Figure 3.9(b) shows the conduction band energy of the structure, along the channel, for different voltages of the secondary gate. The primary gate is biased at $1.0V$ to create the OFF state potential barrier. As the secondary gate is biased towards more negative values, it increases the carrier concentration at the source region, as if the channel is doped with a higher concentration

(a) (b)
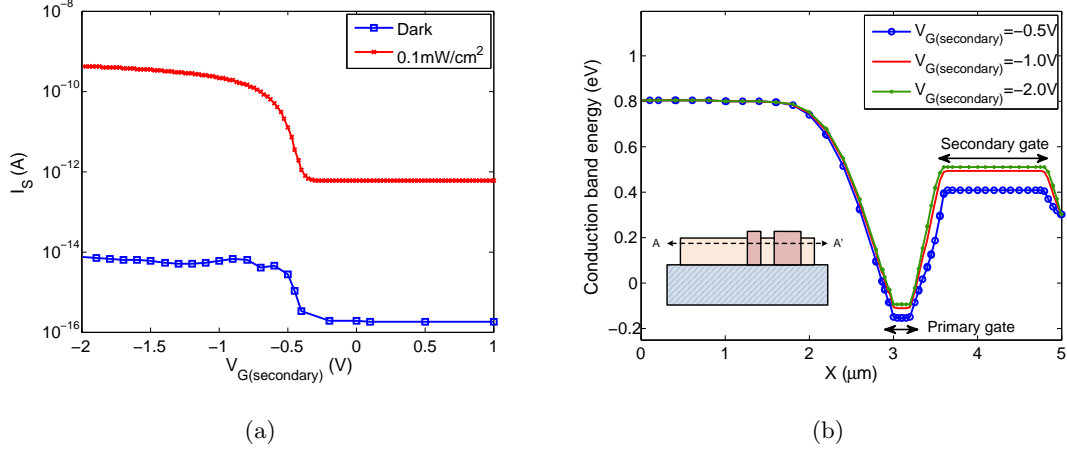
Figure 3.9: (a) Source current versus the secondary gate bias in the multiple gate, junction-less phototransistor (figure 3.8). The primary gate is $200nm$ long and covers a $200nm$ wide channel (NW_1). The secondary gate is $1.2\mu m$ long, and covers a $20nm$ wide region (NW_2). (b) Impact of the secondary gate bias on conduction band energy of the structure along the channel (cutline AA'). Device thickness is $0.85\mu m$, $V_{G(primary)} = 1.0V$, $V_S = 0.5V$, $V_D = 0V$.

of acceptors (figure 3.9(b)). This directly impacts the emitter efficiency of the structure, that is rephrased below, based on the definition of the emitter efficiency in a one dimensional, *pnp* junction transistor (equation 3.1):

$$\gamma = \frac{I_p}{I_p + I_n} \tag{3.2}$$

Reinterpreting the definition of the emitter efficiency to suit the junction-less transistor case, I_p denotes the current of the holes, diffusing from source into the channel; and I_n is the current of the electrons that are injected into the source from the channel. When the concentration of holes in the source is increased, the holes that diffuse into the channel outnumber the channel electrons that diffuse into the source. The ratio of I_p/I_n would therefore increase, and the emitter efficiency approaches the limit of 1. As a result, one expects a larger source current.

Narrowing the size of NW_2 can similarly lead to an increase in the source current. This is verified in figure 3.10(a), where the source current versus the width of NW_2 is plotted. The current change is attributed to fact that accumulation of holes under the secondary gate is a local effect. We have plotted the conduction band energy for two source widths of $100nm$, and $20nm$ in figure 3.10(b). The energy band is obtained along a cutline across the source. When the source is wide, only the areas that are very close to the interface are in accumulation. As the source

(a)   (b)
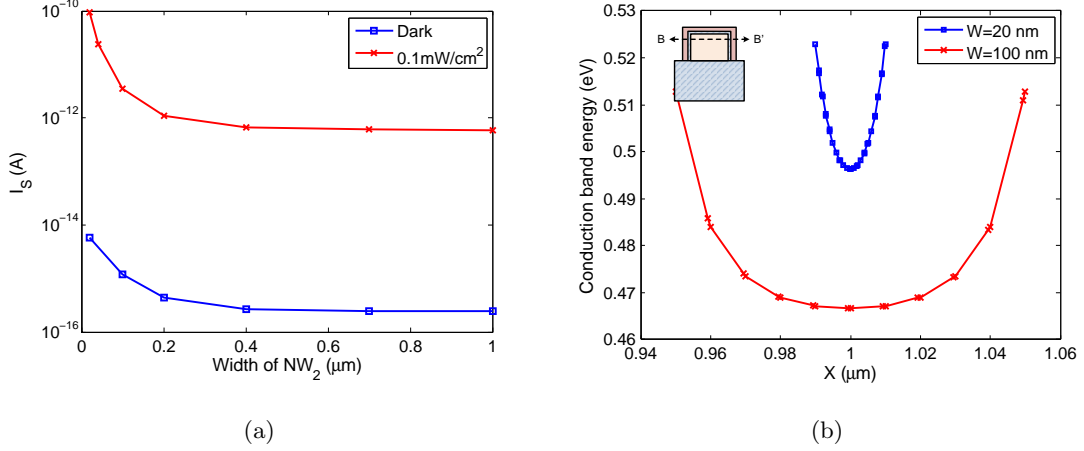
Figure 3.10: (a) Source current versus width of NW_2, in the multiple gate junction-less photo-transistor of figure 3.8. The primary gate is $200nm$ long and covers a $200nm$ wide nanowire (NW_1). The secondary gate is $400nm$ long. $V_{G(primary)} = 1.0V$, $V_S = 0.5V$, $V_D = 0V$, $V_{G(secondary)} = -1.0V$. (b) Conduction band energy, across the source area (cutline BB').

width is narrowed down, a larger percentage of the channel is influenced by the secondary gate, and the net concentration of holes is increased. The emitter efficiency, and therefore the source current will both increase.

Although the secondary gate bias and the width of NW_2 influence both dark and photo-currents (figures 3.9 and 3.10), the change in the current is less pronounced at dark. For example, in figure 3.10(a), the source current changes by more than two orders of magnitude when the device is illuminated; while the dark current varies by about 25 times. A similar behavior was also observed in figure 3.7, where we had changed the doping concentration of the source. To clarify this, we study the emitter efficiency when the transistor is in dark (OFF state), or under illumination (ON state). Formulas for I_p and I_n in equation 3.2 are available in text books such as [40]. By making some simplifications at ON and OFF states, and also fitting the equation to the junction-less phototransistor, the emitter efficiency is simplified as below:

$$\gamma = \begin{cases} \dfrac{1}{1+(K\frac{N_2}{N_1})\frac{sinh(X)}{cosh(x)}} & ON, illumination \\[3mm] \dfrac{1}{1+(K\frac{N_2}{N_1})\frac{sinh(X)}{cosh(x)-1}} & OFF, dark \end{cases} \qquad (3.3)$$

In this equation, K is a parameter that depends upon the diffusion coefficient and the minority carrier diffusion length in the source and the channel. Parameter X depends on the portion of the channel length that is not influenced by the source or drain biasing, as well as minority carrier

(a)

(b)
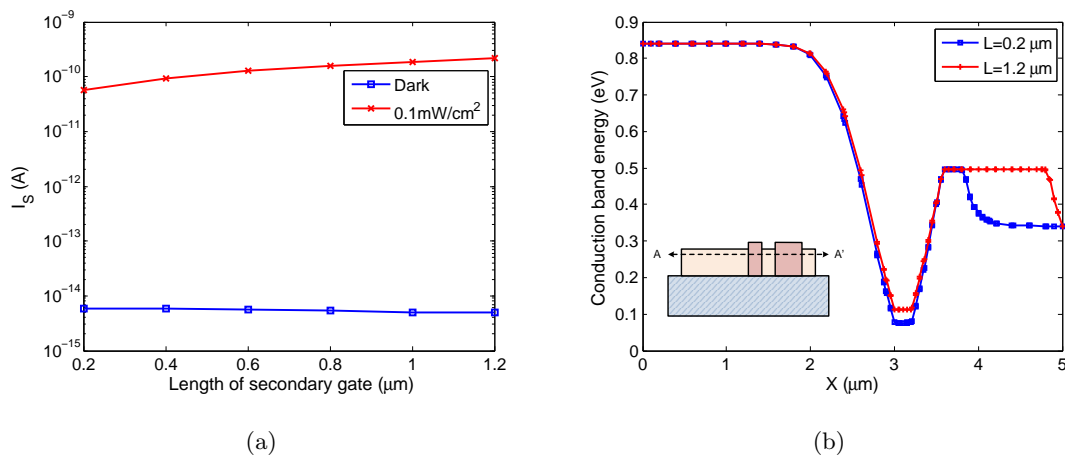
Figure 3.11: (a) Source current versus nanowire length underneath the secondary gate (figure 3.8). (b) Conduction band energy, along the channel for different lengths of the secondary gate and NW_2. For both cases the primary gate is $200nm$ long and covers a $200nm$ wide nanowire (NW_1), and the secondary gate covers a $20nm$ wide channel (NW_2). $V_{G(primary)} = 1.0V$, $V_{G(secondary)} = -1V$, $V_S = 0.5V$, $V_D = 0V$.

diffusion length at the channel [40]. N_1 and N_2 represent the concentration of electrons and holes underneath the secondary gate (source) and the primary gate (channel), respectively. As discussed before, increasing N_1 in the denominator causes the emitter efficiency to get closer to unity. However, regardless of the value of N_1, the emitter efficiency of the OFF state is always smaller than that of the ON state. As a result, the dark current is not increased as much as the illumination current, as plotted in figures 3.9(a) and 3.10(a).

Investigation on the role of the length of NW_2 is plotted in figure 3.11(a). We note that the total length of the detector is kept fixed. A longer NW_2 causes the source current to increase; however, it does not change the barrier height under the secondary gate (figure 3.11(b)). The change in the current is due to the funneling effect, that was discussed in chapter 2. The long, narrow diffusion pathway creates a physical barrier for electrons and slows down the diffusion process. This forces the potential barrier under the primary gate to decrease; which in turn causes the photocurrent to increase.

By combining the three parameters discussed in this section, the secondary gate bias, the width, and the length of NW_2, it is possible to improve the performance of the junction-less phototransistor in terms of photocurrent and noise equivalent power. We have tabulated a few cases in table 3.1. The data ranges from different biases of the secondary gate, to different widths and lengths of NW_2. The most dramatic increase in the optical gain takes place when the width

of the nanowire (NW_2) is reduced from $400nm$ (first row) to $20nm$ (second row). This verifies the importance of having a narrow region under the secondary gate. Decreasing the voltage and increasing the length of the secondary gate in rows 3 and 4 are both effective, but the improvement is not as much as the change due to the width of NW_2. Please note that for the data presented in the table, the secondary gate is biased in accumulation, which is the best possible bias as verified in Figure 3.9(a).

We have also included a case in which the thickness of NW_2 is reduced (fifth row), as if a nanowire bridges the channel and the source regions. The effect of decreasing the thickness of NW_2 is very similar to the effect of decreasing its width. It strengthens the control of the secondary gate over NW_2 and increases the concentration of majority carriers. As a result, one expects a better emitter efficiency and photocurrent. Although the case of the narrow, thin NW_2 seems to be challenging in terms of fabrication, it exhibits the best photocurrent and NEP among the other devices in the table.

We remark that for the results presented in table 3.1 the effect of the surface states is not included, while the large surface to volume ratio in nanowires can lead to carrier recombination, and therefore degradation of the photodetector response. To study this, we chose the devices on rows 2 and 5 of table 3.1, and investigated their response with the effect of surface states included. The surface recombination velocity of passivated silicon nanowires ranges from less than $13cms^{-1}$ to about $61cms^{-1}$ in the state of the art structures reported in literature [108–110]. In our simulations, the surface recombination velocities of electrons and holes are both assumed to be $13cms^{-1}$[4].

As a result of surface recombination, the photocurrent of the device on the second row of table 3.1 has dropped to $3.6 \times 10^{-11}A$. The device in the fifth row of the table has a thinner NW_2, which translates into a higher surface to volume ratio. The photocurrent of this device is decreased to $1.45 \times 10^{-10}A$. The decrease in the photocurrent is due to the recombination of carriers within both NW_1 and NW_2 regions. In NW_1, carrier recombination leads to losing some of the photo-generated carriers. As a result, the barrier would not decrease as much as in the ideal case, leading to degradation in the overall current flow. Recombination of carriers as they pass through NW_2 is also responsible for further decrease in the current. Work to decrease the surface recombination velocity and bulk recombination times will be helpful in increasing the optical gain, but as expected they will lead to an increase in the time scales associated with the transient response.

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[4]Shockley-Read-Hall (SRH) model is also activated. Bulk recombination lifetime is $10^{-5}s$.

Table 3.1: Comparison of multiple gate junction-less phototransistors

Device specifications			Dark current (A)	Photocurrent (A)	Optical gain	Responsivity (A/W)	NEP (W/Hz$^{0.5}$)	Photon rate (s^{-1})
1	NW_2	Width (nm) 400 Thickness (μm) 0.85	2.7×10^{-16}	4.7×10^{-13}	0.8	0.08	1.8×10^{-16}	588
	$G_{secondary}$	Length (μm) 0.4 Bias (V) -1						
2	NW_2	Width (nm) 20 Thickness (μm) 0.85	5.9×10^{-15}	6.6×10^{-11}	114.8	11.7	5.6×10^{-17}	180
	$G_{secondary}$	Length (μm) 0.4 Bias (V) -1						
3	NW_2	Width (nm) 20 Thickness (μm) 0.85	5.9×10^{-15}	1.5×10^{-10}	264.3	27.0	3.7×10^{-17}	118
	$G_{secondary}$	Length (μm) 1.2 Bias (V) -1						
4	NW_2	Width (nm) 20 Thickness (μm) 0.85	7.2×10^{-15}	2.9×10^{-10}	512.7	52.4	2.9×10^{-17}	94
	$G_{secondary}$	Length (μm) 1.2 Bias (V) -2						
5	NW_2	Width (nm) 20 Thickness (μm) 0.05	4.0×10^{-15}	1.2×10^{-09}	2053.1	209.7	1.1×10^{-17}	35
	$G_{secondary}$	Length (μm) 1.2 Bias (V) -2						

Width of $NW_1 = 200nm$, Length of primary gate=$200nm$, Semiconductor thickness=$0.85\mu m$, $V_{G(primary)} = 1.0V$.

A surface reflection of 30% is considered. The photocurrent presented here is multiplied to transmission.

The noise sources considered in calculating the NEP are input and source shot noise, and also the thermal noise of the channel. We did not calculate the Flicker noise, as it strongly depends on how the device is fabricated. The load is considered to be infinitely large; otherwise the thermal noise of the load at room temperature dominates.

3.2.2   Linearity

Figure 3.12 investigates the linearity of the output current, versus the input light intensity. The graphs are obtained for two multiple gate structures whose information is summarized in rows 1 and 5 of table 3.1. Both structures are similar in terms of the doping level ($10^{15} cm^{-3}$), and the geometry of the primary gate. NW_1 in both structures is $200nm$ wide and is covered by a 200nm long primary gate. The secondary gate in the first structure, the blue curve, is biased at $-1V$; the gate is $400nm$ long and covers a $400nm$ wide NW_2. In the second structure shown by red curve, the secondary gate is $1.2\mu m$ long and is biased at $-2V$. In this device, the width and thickness of NW_2 are $20nm$ and $50nm$, respectively.

The source current versus intensity graph for the first structure shows a more linear response in comparison with the second structure. This is consistent with the behavior of the bipolar transistors in response to the base-emitter biasing [40]. When the forward bias level approaches the built in voltage, due to high level injection, the current is exponentially proportional to $(q/2kT)$. For the second device, that has a higher optical gain, the barrier height (or similarly the channel-source bias) drops faster leading to high level injection, and non-linearity of the output current versus intensity.
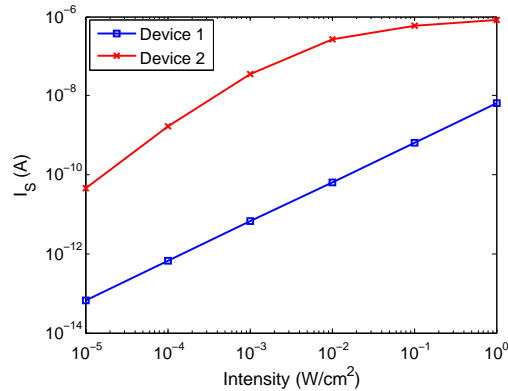
Figure 3.12: Source current versus light intensity in two multiple gate structures (rows 1 and 5 of table 3.1). In both structures, NW_1 is $200nm$ wide and is covered by a 200nm long primary gate. In Device 1, the secondary gate is biased at $-1V$; the secondary gate is $400nm$ long and covers a $400nm$ wide NW_2. In Device 2, the secondary gate is $1.2\mu m$ long and is biased at $-2V$. The width and thickness of NW_2 are $20nm$ and $50nm$, respectively. Semiconductor thickness is $0.85\mu m$, except for NW_2 in Device 2.

3.2.3 Phototransistor Speed

The speed of the phototransistor depends on a different set of physical processes during the rise and fall of the photocurrent. When the light source is turned ON, the rise time (speed) is limited by the RC time constant. The capacitance (C) is determined by the two gates, and the resistance (R) is determined by the narrow NW regions. Since in most of the devices presented, NW_2 is longer and narrower than NW_1, we expect the time constant of this region to dominate. Once the light source is switched OFF, the extra carriers in the NW_1 region recombine and increase the potential barrier (under the primary gate) to its original value. In this case, the size of NW_2 does not cause much variation in the fall time, as the dominant process is the carrier recombination in NW_1.

The transient response of a structure with NW_1: $200nm$ wide, and NW_2: $20nm$ wide (second row in table 3.1) is plotted in figure 3.13. The logarithmic scale in the inset shows that when the light is switched OFF, the current drops by about 3 orders of magnitude in the first few milliseconds. Normally external circuits in a pixel apply a reset signal to the photodetector to decrease the fall time. We have also summarized the rise time and fall time of two more structures in table 3.2. The data shows a small difference in values as the size of NW_2 is changed.
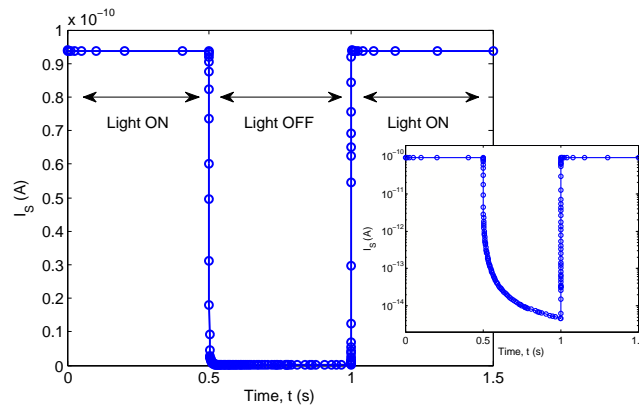
Figure 3.13: Transient response of a junction-less, multiple gate phototransistor, that corresponds to the second row of table 3.2. The width of NW_1 and NW_2 is $200nm$ and $20nm$, respectively. The inset shows the same data in logarithmic scale. $V_{G(primary)} = 1.0V$, $V_{G(secondary)} = -1.0V$, $V_S = 0.5V$, $V_D = 0V$, Intensity=$10^{-4}W/cm^2$.

Table 3.2: Rise time and fall time of multiple gate junction-less phototransistors

Width/Length/Thickness of NW$_2$ (nm/μm/μm)	Rise Time (s)	Fall Time (s)
1000/0.4/0.85	0.8	1
20/0.4/0.85	0.7	1.1
20/1.2/0.05	1	0.95

Rise time: the time during which the current changes from 10% to 90% of the peak value.

Fall time: the time during which the current drops from 90% to 10% of the peak value.

Width of $NW_1 = 200nm$, Length of primary gate=200nm.

$V_{G(primary)} = 1.0V$, $V_S = 0.5V$, $V_D = 0$V, Intensity=$10^{-4}W/cm^2$.

First two rows: $V_{G(secondary)} = -1.0V$; third row: $V_{G(secondary)} = -2.0V$.

3.3 Chapter Summary

In this chapter we investigated the possibility of using junction-less transistors as photo-detectors. The motivation of using junction-less structures comes from the advantage of a simpler fabrication. We proposed ways to surpass the low optical gain of such structures, by incorporating nanowires within the device channel, and using multiple gates.

In our design, instead of having an entirely narrow channel, we keep the channel partly narrow and partly wide for electrostatic and optical reasons, respectively. The wide area of the channel provides a surface for light absorption. The narrow region is covered by a (primary) gate that creates the potential barrier required for phototransistor operation. Further boost of the optical gain is achieved by increasing the emitter efficiency of the device by adding a secondary gate and narrowing down the source region. This artificially increases the majority carrier concentration at this region and causes the optical gain to increase and the NEP to improve. We demonstrated multiple gate photodetectors showing NEP of $1.1 \times 10^{-17} W/Hz^{0.5}$, which corresponds to a photon rate of about $35s^{-1}$.

Chapter 4

Device Fabrication

This chapter is devoted to the step by step methods developed to fabricate the devices introduced in the previous chapters. Easier access to the top-down facilities encouraged us to follow this approach for fabrication of photodetector structures. Although bottom-up methods [1] are able to grow nanowires with diameters as small as a few nanometers, [111–113], and out of a wide variety of materials in a high-yield and reproducible manner [83, 114–116], they suffer from difficulties during the assembly of the nano-structures. Top-down methods are able to create nanowires at the desired locations [117]. The ability of placing an individual nano-component onto a precise location is an important fabrication step for our device, and therefore top-down methods are preferred. The main issue of top-down created nanowires could be surface recombination states as a result of defects and incomplete atomic bonds, which would be discussed later.

As shown in figure 4.1, the device fabrication is divided into four major steps: (1) fabricating the junction (doping), (2) active region, (3) gate dielectric layer, and (4) source, drain and gate contacts. The only difference in the fabrication of the junction and junction-less structures (chapters 2 and 3) is the doping step in junction devices. We also remark that the fabrication steps in this chapter will focus on single gate devices, as the fabrication of multiple gate structures is similar.

We used two types of Silicon on Insulator (SOI) wafers from Soitec® [118], with different specifications. The thickness of the top silicon layer was $340nm \pm 40nm$ in the first set of wafers; and $35nm \pm 5nm$ in the second set of wafers. Both wafer types were lightly boron doped, with the crystal orientation of $< 100 >$. Other specifications of each wafer, e.g. doping density and

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[1]There are two general categories of fabricating nanowires: Bottom-up and Top-down. Bottom-up methods synthesize the nanowires by growing them. Top-down methods aim to fabricate one dimensional (1D) structures using conventional micro-fabrication techniques like lithography, oxidation, and etching.

thickness of the buried oxide layer are discussed along with the experimental results in chapters 5 and 6.

1. Junction

i. Alignment marks
Patterning
- Lithography steps

Etching
- Silicon dry etch
- Etch mask removal

ii. Ion implantation (II) steps
Mask
- Cleaning
- II mask material deposition
- Lithography steps
- Dry etching the II mask material
- Resist removal

Ion implantation
- Implantation
- Annealing
- Mask removal

3. Gate Dielectric

i. Cleaning
- Organic and metallic contamination removal
- Native oxide removal

ii. Dielectric deposition
iii. Annealing

4. Contacts

i. Patterning
- Surface treatment
- Bilayer lithography steps

ii. Dielectric removal (source/ drain only)
- Dielectric wet etch

iii. Contacts
- Metal deposition
- Lift off

2. Active Region

i. Patterning
- Cleaning, *sacrificial layer deposition*
- Lithography steps
- *hard mask deposition, lift off*

ii. Etching
- *Sacrificial layer dry etch*
- Silicon dry etch
- Etch mask (*hard mask, sacrificial layer*, resist) removal

Figure 4.1: Four major steps of device fabrication. In the second block (Active Region), two fabrication approaches are followed; and that is why some of the steps are written in *italic*.

4.1 Junctions

Fabricating the n^+pn^+ junctions was the first step performed on the wafers (for the junction devices). Although the 'self-aligned gate' method is a very common and straightforward way in

fabricating junction transistors [119], some concerns prevented us from following that approach. The main, most important reason was the concern about gold contamination, due to the fact that our cleanroom was not a gold-free facility. The high temperature annealing process required to activate the dopant atoms could potentially create trap states in the contaminated samples. As a result, we decided to create the junctions on the whole wafer, before introducing the wafer to the contaminated systems of the cleanroom.

The most popular method of doping the active region of a transistor is ion implantation [120]. The advantages of ion implantation are localized and precise doping. For improved localization which is critical in nano-scale devices, we selected ion implantation as well. Since the wafer was p-type, the goal was to create abrupt n^+p junctions. And although the length of the channel in our simulation (chapter 2) was $1\mu m$, we planned to pattern junctions with a variety of lengths, up to $5\mu m$.

We chose phosphorous (P) as the doping material, and ran a series of simulations in order to find out the number of implantation runs, the required dose and energy, and also the thickness of the implantation mask. For this purpose we used 'MicroTec' simulator which is designed for two dimensional process and device simulation [121]. An optimized process was developed with five implantation runs. The dose and energy for each run, together with the average projected range (R_P) and the standard deviation (ΔR_P) at each energy is summarized in table 4.1. Figure 4.2 shows the profile before and after the (high temperature) rapid thermal annealing (RTA) process. As shown in the figure, a uniform doping profile was obtained after annealing.

Table 4.1: Properties of the phosphorous ions that result the profile of figure 4.2

	Energy (keV)	Dose (cm^{-2})	Projected range, R_p (nm)	Standard deviation, ΔR_p (nm)
1	10	2.3×10^{14}	16.9	8.3
2	27	1.6×10^{14}	39.6	17.3
3	50	4.2×10^{14}	69.0	27.7
4	90	7.3×10^{14}	121.3	43.5
5	175	1.95×10^{14}	229.6	69.6

Note: The data is obtained using 'SRIM' simulator [122].

The ion implantation process needed a mask to protect some areas from phosphorous ions. To fabricate the mask, we chose conventional photo-lithography, as the critical dimension was $1\mu m$. The material for implantation mask was silicon dioxide. Other alternatives such as metals and silicon nitride were also available; however we preferred silicon dioxide over metals to avoid any
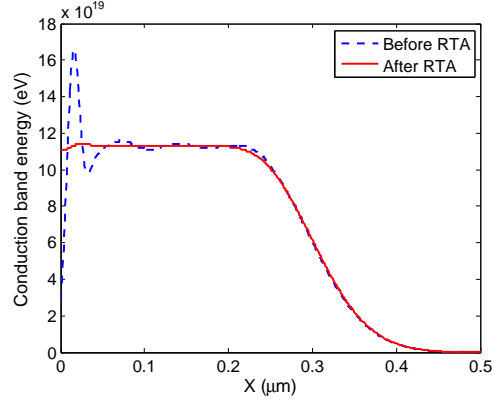
Figure 4.2: Modeling results of the ion implantation profile. The target material is p-type silicon, with background doping level of $10^{15} cm^{-3}$. The implants are phosphorous ions, whose dose and energy are listed in table 4.1.

metal contamination, especially during the post implantation annealing process. In addition, the etch rate of silicon dioxide in solutions containing hydrofluoric acid is faster than the etch rate of silicon nitride [123]. We therefore chose silicon dioxide over silicon nitride to avoid prolonged soaking in such etchants that can dissolve the buried oxide layer as well.

The thickness of the mask was determined through a series of simple calculations based on approximating the distribution of the ions with a symmetric Gaussian distribution [120]:

$$C(x) = C_p exp(-\frac{(x - R_p)^2}{2\Delta R_p^2}) \qquad (unit : cm^{-3}) \qquad (4.1)$$

In equation 4.1, $C(x)$ represents the ion distribution at depth x, and C_p is the peak concentration of the ions. R_P is the average projected range; and ΔR_P is the standard deviation, also known as straggle. Both of these parameters depend on the target material, as well as the implantation energy. The implantation dose, Q, is:

$$Q = \sqrt{2\pi}\Delta R_p C_p \qquad (unit : cm^{-2}) \qquad (4.2)$$

The minimum thickness of the mask, x_m, is determined based on the assumption that the concentration of ions that can pass the mask layer has to be below the background doping level (C_B) of silicon, or $C(x_m) \leq C_B$ [120], where C_B is $10^{15} cm^{-3}$.

We considered the maximum implantation energy of $175 keV$, and the dose of $1.95 \times 10^{14} cm^{-2}$ (table 4.1) to obtain the minimum thickness. For silicon dioxide, at this energy, the projected

range and the straggle are about $236nm$ and $63nm$, respectively [122]. Using equations 4.1 and 4.2, a minimum thickness of about $550nm$ was calculated for the mask layer.

The steps we followed to fabricate the junctions are summarized in table 4.2. Fabrication of the junctions started with patterning the wafer with a set of alignment marks, shown in figure 4.3, which were later used to find the position of the junction. We designed a set of large alignment marks for optical lithography, and a set of small alignment marks for electron beam lithography. Both marks were in the form of cross shape ridges of silicon, and were created by electron beam lithography with *ZEP520A* as the resist [124]. ZEP was also used as the etching mask, during silicon dry etch. Figure 4.3 shows the SEM picture of the alignment marks after etching (silicon) and removing the resist.
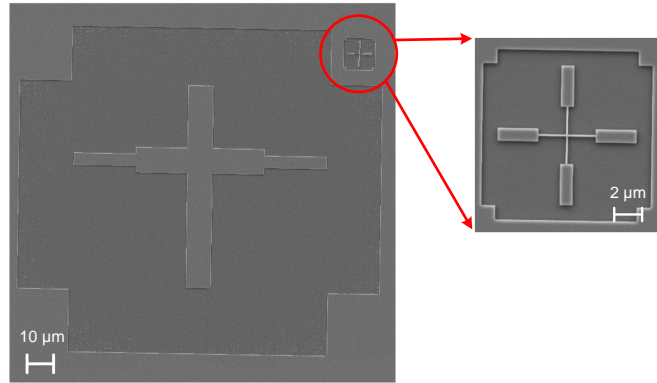
Figure 4.3: Alignment marks, in the form of ridges fabricated on the wafer by electron beam lithography and dry etching the silicon. The large alignment marks are used for optical lithography, while the small ones (magnified in the inset) are used for electron beam lithography.

The wafer surface was cleaned after removing the ZEP resist and then a layer of silicon dioxide (ion implantation mask material) was deposited. Next, after treating the surface of the wafer in an HMDS oven (for improved adhesion [125]), the wafer was coated with photoresist and baked. The photoresist was then patterned by photo-lithography, using Karl Suss MA6® mask aligner [126]. During the lithography we tried to perform an accurate alignment by trying to align the large alignment marks (figure 4.3) on the wafer with those located on the mask itself. The lithography was performed in hard contact mode to achieve the critical dimension of $1\mu m$.

After development, we used Oxford Instruments® Inductively Coupled Plasma Reactive Ion Etcher (ICPRIE) [127] to etch the silicon dioxide layer. The C_4F_8 gas was used to etch the oxide layer, while the photoresist acted as the etching mask. The photoresist was then stripped by soaking the wafer in acetone, followed by the oxygen plasma process to de-scum any residues.

Table 4.2: Summary of the n^+pn^+ junction fabrication

	Task	Process	Comments
1	Wafer cleaning	Acetone, IPA sonic bath	5 minutes each
2	Alignment mark pattern	Sample dehydration	$180°C$, 2 minutes
3		ZEP spin coating	6000 rpm, baked at $180°C$ for 3 minutes
4		Electron beam lithography (EBL)	Voltage = $100kV$
5		Development	ZED-N50 [124], followed by MIBK + IPA (9:1)
6	Alignment mark etch	Si dry etch	$SF_6 + C_4F_8$
7		Resist removal	Oxygen plasma
8	Wafer cleaning	Standard Clean 1 (SC-1)	H_2O : NH_4OH : H_2O_2 (5:0.2:1), $70°C$ for 10 minutes
9	Oxide removal	2% HF dip	30 seconds
10	Ion implantation mask	Silicon dioxide deposition	PECVD, at $330°C$
11		HMDS mono-layer coating	$150°C$ for 5 minutes
12		Shipley 1811 [128] spin	6000 rpm, baked at $120°C$ for 1 minute
13		Photo-lithography	MA6 mask aligner, hard contact mode
14		Development	MF319
15		SiO$_2$ dry etch	C_4F_8
15		Photoresist removal	Acetone, oxygen plasma
16	Ion Implantation	Phosphorous ions	Table 4.1
17	Ion activation	Rapid thermal annealing	$1000°C$, 12 sec
18	Mask removal	SiO$_2$ wet etch	BHF wet etch

Figure 4.4(a) shows the etch profile of a sample, after the photoresist removal. We remark that the sidewalls could be more vertical and smooth if a hard metal mask was used instead of photoresist, as shown in figure 4.4(b) for a sample with aluminum mask. However, due to metal contamination concerns (during high temperature RTA process) we chose the photoresist mask.

(a)   (b)
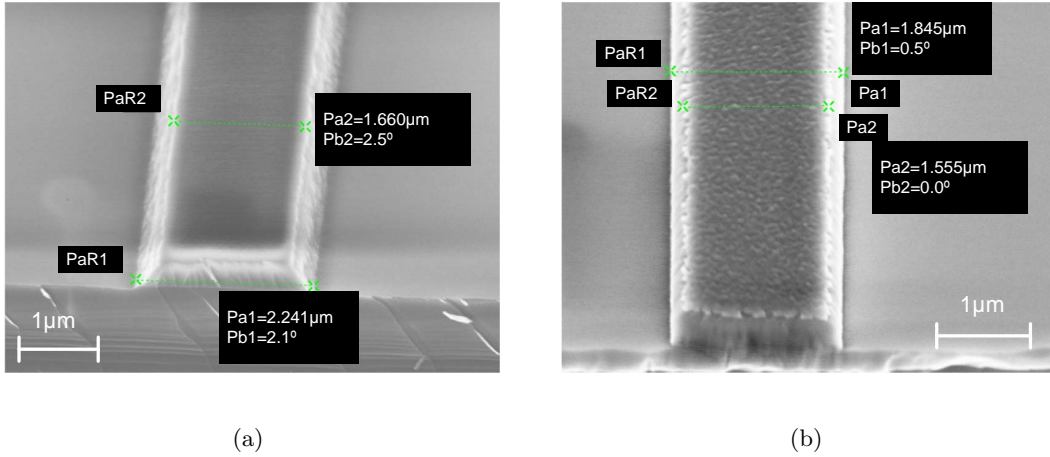
Figure 4.4: Profile of the SiO$_2$ layer after dry etching, (a) when the etch mask is photoresist, and (b) when the etch mask is aluminum.

The wafer was then sent to other facilities for ion implantation and activation [129, 130][2].

4.2 Active Region

Figure 4.5(a) illustrates the details of fabricating the active region. The active region is almost 'H' shaped, as sketched in figure 4.5(b). The middle narrow part is where the source, drain and the channel will later be defined. The large pads at the two ends are included in order to facilitate the connection of the metal contacts to the source and drain regions.

Different approaches have been used to define the active region of a transistor with a nano-scale channel. A combination of conventional photolithography and etching, electron beam lithography, thinning the channel region by thermal oxidation and anisotropic wet etching are some examples [92,93,131–133]. We used electron beam lithography to pattern the structures due to its reliability, repeatability and also availability. Later we etched the active region by means of dry etching.

Fabrication of the active region is summarized in table 4.3. The patterns were written on a positive resist named Poly(methyl methacrylate), or PMMA [134]. PMMA is an excellent resist in terms of resolution and ease of handling. However, it is not a strong dry etching mask [135]. As a result, we chose to make a hard, metallic mask for etching the active region. The two available metal choices for us were chromium (Cr), and aluminum (Al). We first tried chromium as the

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[2]**Note:** Even though we spent a substantial amount of time with ion implantation, the devices fabricated finally were junction-less. The section on ion implantation above is included for completeness.
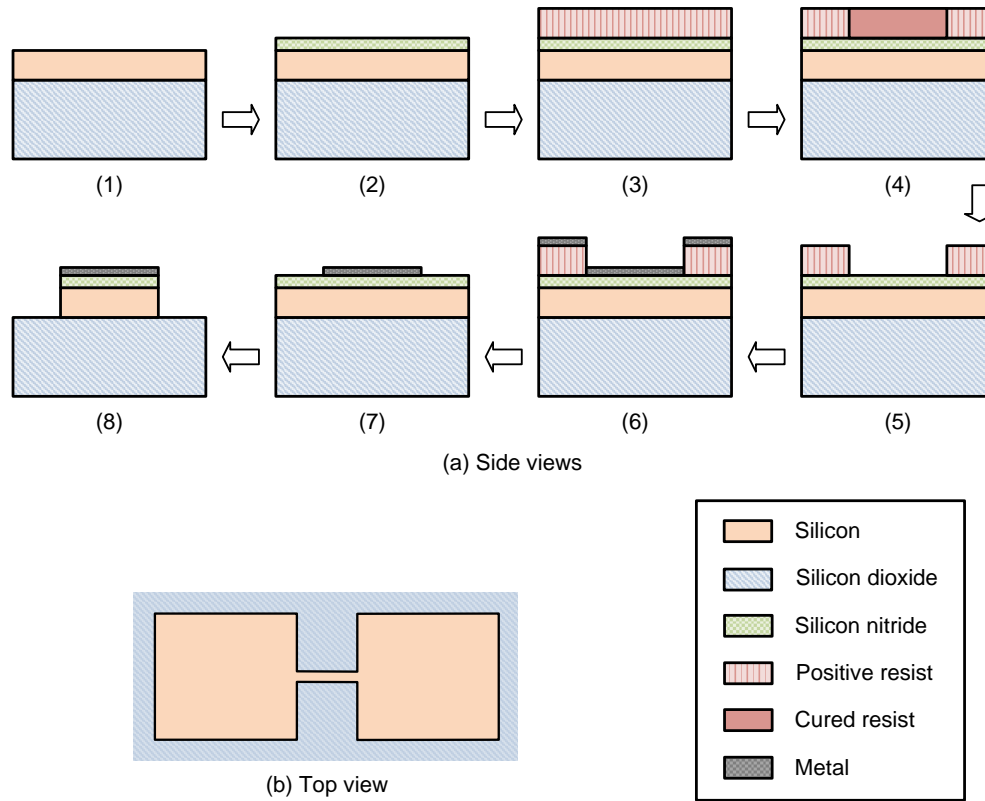
Figure 4.5: (a) Fabrication of the active region. (1) Side view of the sample (the top silicon and the buried oxide layers are shown). (2) Silicon nitride is deposited. (3) Resist is spun. (4) Resist is exposed to the electron beam. (5) Side view after development. (6) Metal is deposited. (7) Side view after lift-off. (8) Side view after etching. (b) Top view of the active region after the metal mask and the silicon nitride layer are removed.

etching mask; however due to concerns about Cr contamination, we switched to aluminum. In order to avoid any metal diffusion into silicon, we decided not to deposit the metal right on top of the silicon layer. For this reason, we started to form the active region by depositing a thin layer of silicon nitride (SiN_x) over the silicon surface (figure 4.5(a)). This layer acts as a sacrificial layer and separates the silicon and aluminum layers. We deposited the silicon nitride layer in a Plasma Enhanced Chemical Vapor Deposition (PECVD) chamber, at 330°C.

After depositing the silicon nitride layer, we coated the sample surface by a layer of 950K PMMA A3 [134] (spun at the speed of 3000 rpm and baked in an oven at 180°C for 20 minutes). The patterns were then written by electron beam lithography. The aperture size and voltage were $20\mu m$ and $20kV$, respectively. The patterns were then developed in a mixture of Methyl isobutyl

ketone (MIBK) and Isopropyl alcohol (IPA) 3:1 [134], followed by dipping the sample in IPA to terminate the development process. Next we deposited a thin layer of aluminum (about 30nm) in an Intlvac electron beam evaporator. The excess aluminum was then removed by lift-off process. For this purpose the sample was soaked in Remover PG [136] for several hours (overnight). The solution was then heated to about $60^\circ C$ for at least 30 minutes. The sample was then rinsed by IPA and blow dried [136].

Table 4.3: Fabrication of the active region, using a hard metallic mask

	Task	Process	Comments
1	Sample cleaning	Acetone, IPA sonic bath	5 minutes each
2	Sacrificial layer	SiN$_x$ deposition	$40nm$, PECVD, $SiH_4 + N_2$, at $330^\circ C$
3	Device patterning	Sample dehydration	$180^\circ C$, 2 minutes
4		PMMA spin coating	3000 rpm, baked at $180^\circ C$ for 20 minutes
5		Electron beam lithography (EBL)	Aperture size $= 20\mu m$, voltage $= 20kV$
6		Development	MIBK + IPA (3:1), IPA
7	Hard mask	Al deposition	$30nm$, Electron beam evaporation
8		Lift-off	Remover PG
9	Active region etch	SiN$_x$ dry etch	$SF_6 + O_2$ (10:20 sccm) at $5^\circ C$
10		Si dry etch	$SF_6 + C_4F_8$ [137]
11	Polymer removal	Oxygen plasma	O_2 at $180^\circ C$
12	Hard mask removal	Al wet etch	Aluminum etchant type A at $50^\circ C$
13	Sacrificial layer removal	SiN$_x$ wet etch	Phosphoric acid at $140^\circ C$

We etched the silicon nitride and silicon layers in two separate steps. To etch the silicon nitride, usually fluorine based gas chemistries such as Tetrafluoromethane (CF_4) and Sulfur hexafluoride (SF_6) are used [120,138,139]. To increase the etch selectivity over silicon, and also achieve a more anisotropic etch profile, it is common to add gases like Oxygen (O_2) and Hydrogen (H_2) that react with the free fluorine radicals. Adding such gases also causes the formation of polymer that

acts like an inhibitor and prevents lateral etching [120]. We used the ICPRIE Oxford® plasma etch system to etch the silicon nitride layer. The available gas chemistry was a mixture of SF_6 and O_2 gases, and the ratio was chosen to minimize the undercutting.

Etching the silicon layer was performed in another Oxford system, using a mixture of Octafluorocyclobutane (C_4F_8) and SF_6 gases. The etch process was a *pseudo Bosch* etch process, suitable for etching nano-scale patterns. In a pure Bosch process, two different plasmas are created in an alternating sequence. The first plasma is an etch plasma, that uses the SF_6 gas. The fluorine radicals react with silicon and create the volatile Silicon tetrafluoride (SiF_4) gas in an isotropic way. Afterwards, the second plasma that uses the C_4F_8 gas is activated. During this plasma a Teflon-like polymer is created; which covers the surface of the sample. During the next etch, the fluorine radicals do not react with the polymer. However, the ions in the plasma that are accelerated by the electric field, sputter the polymer away from the silicon surface but not the sidewalls, as the ions are very directional. As a result, the sidewalls are protected by the polymer during the etch cycle, and the etch process continues in an anisotropic way [140].

In the pseudo Bosch process, which is essentially a mixed mode etching, the passivation gas is introduced at the same time as etching. As a result, the polymer deposition takes place while the etching is still running. The ions remove the polymer on the horizontal surfaces faster than it can deposit, and as a result the horizontal surfaces are exposed (and can be etched), while the sidewalls are still protected. The smooth etched sidewalls, and the slow etching rate makes the pseudo Bosch process ideal for nano-scale etching [141, 142].

After the silicon layer was etched using a recipe optimized for high aspect ratio structures [137], the next step was to remove the Al mask and the silicon nitride sacrificial layer (not shown in figure 4.5(a)). Before running any process at this stage, oxygen plasma was introduced in order to remove the polymer layer that was created during the previous etching steps, in order to make the sample ready for consequent mask removal [143]. Figure 4.6 shows the etch profile after the oxygen plasma.

We removed the Al mask by means of wet etching; mainly due to selectivity concerns. The Chlorine (Cl_2) gas that is used for Al dry etching can also etch silicon [120]. As for wet etching, Al can be removed in a mixture of phosphoric acid, nitric acid and acetic acid, commercially available under the name aluminum etchant type A [123, 144].

We also chose wet etching to remove the silicon nitride layer [3], but our etchant choice was limited again. The first available wet etch option is 49% HydroFluoric acid (HF) [120, 145], or

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[3]Removing the silicon nitride layer was very critical, as the silicon surface had to be free of the residual silicon nitride, so that the surface could be passivated by the dielectric layer.
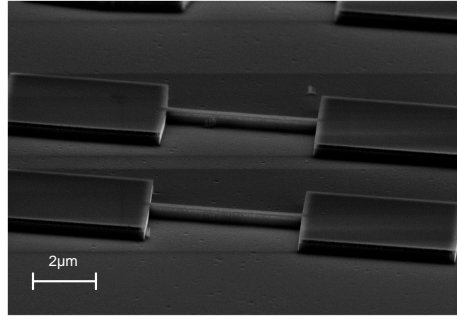
Figure 4.6: Etch profile of a sample, after the SiN_x and Si layers are etched. The Al mask is still on top of the SiN_x layer. The thickness of silicon layer is $350nm$.

the buffered mixture (BHF) that contains ammonium fluoride [123]. Both can remove the silicon nitride layer in a rather fast rate. However, we could not use this option due to the poor selectivity over silicon dioxide [120, 123]. The second popular option is phosphoric acid. Hot phosphoric acid (typically $150 - 180°C$) is often used to remove the silicon nitride layer when selectivity over silicon dioxide is required [120, 146]. The temperature of the solution, as well as the water content play important roles in the etch rate, and selectivity over silicon dioxide [146]. In fact water is usually added to the solution in order to adjust the concentration and the boiling point of the solution [147]. For our process we used hot phosphoric acid; and obtained an etch rate of about $0.12nm/s$ at $140°C$. The top view of the active region before and after mask and sacrificial layer removal is shown in Figure 4.7.

(a)　　　　　　　　　　　　　　　(b)
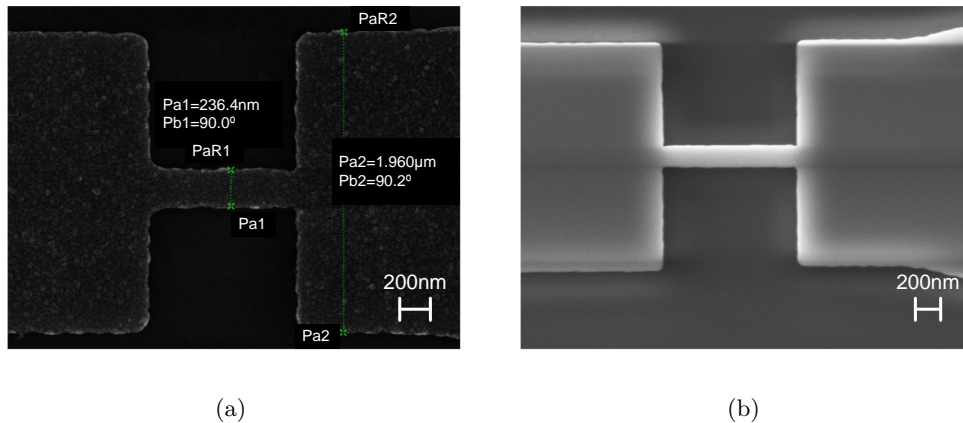
Figure 4.7: Top view of (parts of) the active region, (a) before, and (b) after Al mask and SiN_x removal.

Overall 13 steps are involved in creating the active region (table 4.3). Out of these, 6 are used to create a hard mask for dry etching (steps 2,7-9,12,13 in table 4.3). This has increased the length of the fabrication process and the risk for introducing defects and contamination on the silicon surface by deposition of silicon nitride and aluminum layers. As shown in figure 4.8, using a resist as an etch mask can simplify the process, and eliminate the need for metallic masks. While PMMA is not a good candidate for dry etching, other resists can be used as dry etching masks. An example is the Ma-N 2400 series, a negative tone resist that is not good as PMMA in terms of resolution, but it is a good etch mask for fluorine based plasmas [148]. The resist thickness for the commercially available Ma-N 2403 is about 300nm when spun at 3000 rpm [148]. This resist can be diluted by addition of Mr-T 1090, to obtain thinner layers that provide more resolution during writing [149].
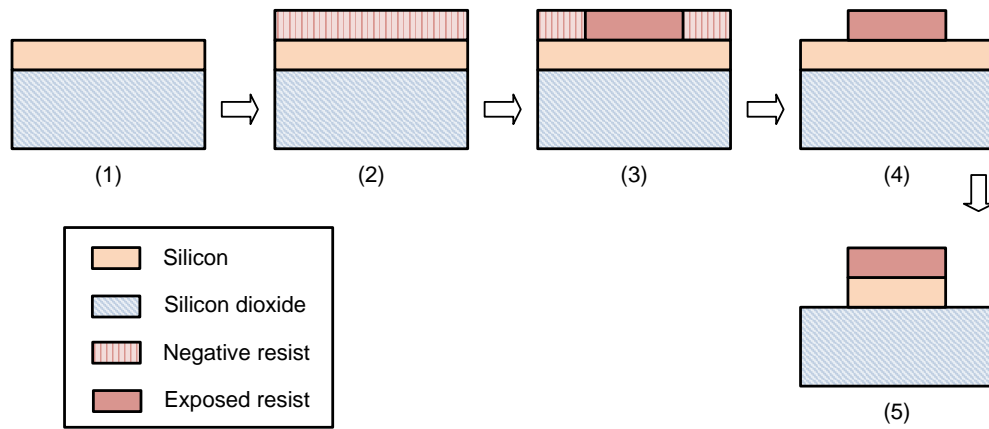
Figure 4.8: Fabrication of the active region, when the electron beam resist is used as a mask for dry etching. (1) Side view of the sample (the top silicon and the buried oxide layers are shown). (2) Resist is spun. (3) Resist is exposed to the electron beam. (4) Side view after development. (5) Side view after etching.

Selecting the Ma-N resist for both patterning and dry etching simplifies the process of fabricating the active region, as summarized in table 4.4. The surface of the sample has to be very clean and moisture free, as the adhesion of the Ma-N resist to the silicon surface is very poor in comparison with PMMA. As a result, it is sometimes recommended to use an oxygen plasma after the usual cleaning procedures [149]. The dose required to expose the Ma-N resist is smaller than the dose that is required for PMMA. As for MaN development, aqueous-alkaline developers such as MF319 can be used [148,149]. The exposed silicon layer was then etched using the pseudo Bosch process explained earlier. After dry etching, the resist was removed in remover PG [136], followed by oxygen plasma process.

Table 4.4: Fabrication of the active region, using a negative resist for patterning and etching

	Task	Process	Comments
1	Sample cleaning	Acetone, IPA sonic bath	5 minutes each
2	Device patterning	Sample dehydration	$180°C$, 10 minutes
3		Oxygen plasma	O_2 at $180°C$
4		MaN spin coating	5000 rpm, baked at $90°C$ for 1 minute
5		Electron beam lithography (EBL)	Aperture size $= 30\mu m$, voltage $= 20kV$
6		Development	MF319, DI water
7	Active region etch	Si dry etch	$SF_6 + C_4F_8$ [137]
8	Mask removal	MaN removal	Remover PG at $60°C$, followed by oxygen plasma

4.3 Fabrication of the Gate Dielectric

Gate dielectric is perhaps the most critical insulator of a transistor in modern CMOS fabrication. It is a very thin layer (less than $10nm$) in current state-of-the-art technology [120]. The gate dielectric has to be defect free in order to avoid high leakage currents. In addition, it should act as a passivation layer at the silicon-dielectric interface to minimize the unwanted recombination of carriers at the surface states [150].

Since the minimum thickness of the gate dielectric in the photodetector device is about $20nm$ (chapters 2 and 3), thermally grown silicon dioxide seems like a good choice. However, three reasons encouraged us not to follow this option. The first reason was the need for a post oxidization, high temperature thermal annealing. In case of junction transistors the samples were already doped, and a high temperature process could make the dopant atoms to diffuse further into the semiconductor. Besides that, we were fabricating the devices in a facility which was not gold-free, and this could result in gold migration and creation of trap states. The third reason was the need to ship the samples to facilities outside of University of Waterloo for thermal oxidation.

We chose the high-κ aluminum oxide (Al_2O_3) as the alternative for the thermally grown oxide. Al_2O_3 is a wide band-gap [151–153] insulator with a large dielectric constant and excellent thermal and chemical stability [150,154]. Al_2O_3 is used as the gate dielectric layer in Metal Insulator Semiconductor (MIS) transistors, and also as the passivation layer in solar cells [155–159].

Furthermore, conformal layers of Al_2O_3 can be deposited by means of atomic layer deposition (ALD) [160], which is especially important for non-planar devices.

The steps of fabricating the gate dielectric layer are listed in table 4.5. Prior to dielectric deposition, we cleaned the samples by means of Standard Clean 1 (SC-1) and 2 (SC-2), and dilute 2% HF dip [161], to remove the organic and metallic contaminations of the sample surface, as well as the thin native oxide layer. In order to avoid micro-roughening of the silicon surface, we used a decreased ratio of ammonium hydroxide (NH_4OH) in SC-1 mixture [120, 162]. For samples that were prepared using the negative resist as the dry etching mask (figure 4.8, table 4.4), we replaced steps 1 to 4 (in table 4.5) with Piranha clean [120], as the samples were not exposed to any metal. A $35nm$ layer of Al_2O_3 was then deposited in an Oxford PlasmaLab 100 FlexAL® Atomic Layer Deposition system, using a plasma process at $300°C$. Samples were then annealed at $425°C$ in forming gas (N_2:H_2, 90:10) for 30 minutes in order to passivate the silicon surface [40, 153, 163].

Table 4.5: Fabrication of the Gate Dielectric

	Task	Process	Comments
1	Native oxide removal	2% HF dip	30 seconds
2	Organic/light metal cleaning	Standard Clean 1 (SC-1)	H_2O : NH_4OH : H_2O_2 (5:0.2:1), $70°C$ for 10 minutes
3	Oxide removal	2% HF dip	30 seconds
4	Metal contamination removal	Standard Clean 2 (SC-2)	H_2O : HCl : H_2O_2 (6:1:1), $65°C$ for 10 minutes
5	Oxide removal	2% HF dip	90 seconds
6	Dielectric deposition	Al_2O_3 deposition	$35nm$, Atomic Layer Deposition (ALD), $300°C$, plasma process
7	Surface passivation	Annealing	$425°C$ in N_2 : $H_2(90:10)$, 30 minutes

For samples whose active region was prepared using the MaN resist as the etch mask (as summarized in table 4.4), steps 1 to 4 were replaced by Piranha clean process (H_2SO_4 : H_2O_2 for 12 minutes).

4.4 Source, Drain and Gate Contacts

The final fabrication step is making contacts to the device. The material of choice is aluminum (Al) and the steps for creating the source and drain contacts are shown in figure 4.9.

Although the gate material was also aluminum, fabricating the gate had to be done separately from fabricating the source and drain contacts. This was a necessary step, as the dielectric layer at the position of source and drain (but not the gate) had to be removed prior to metal deposition. Otherwise, fabricating the gate contact is very similar to the fabrication of the source and drain contacts, except that we skipped step (6) in figure 4.9, which is the removal of the gate dielectric.
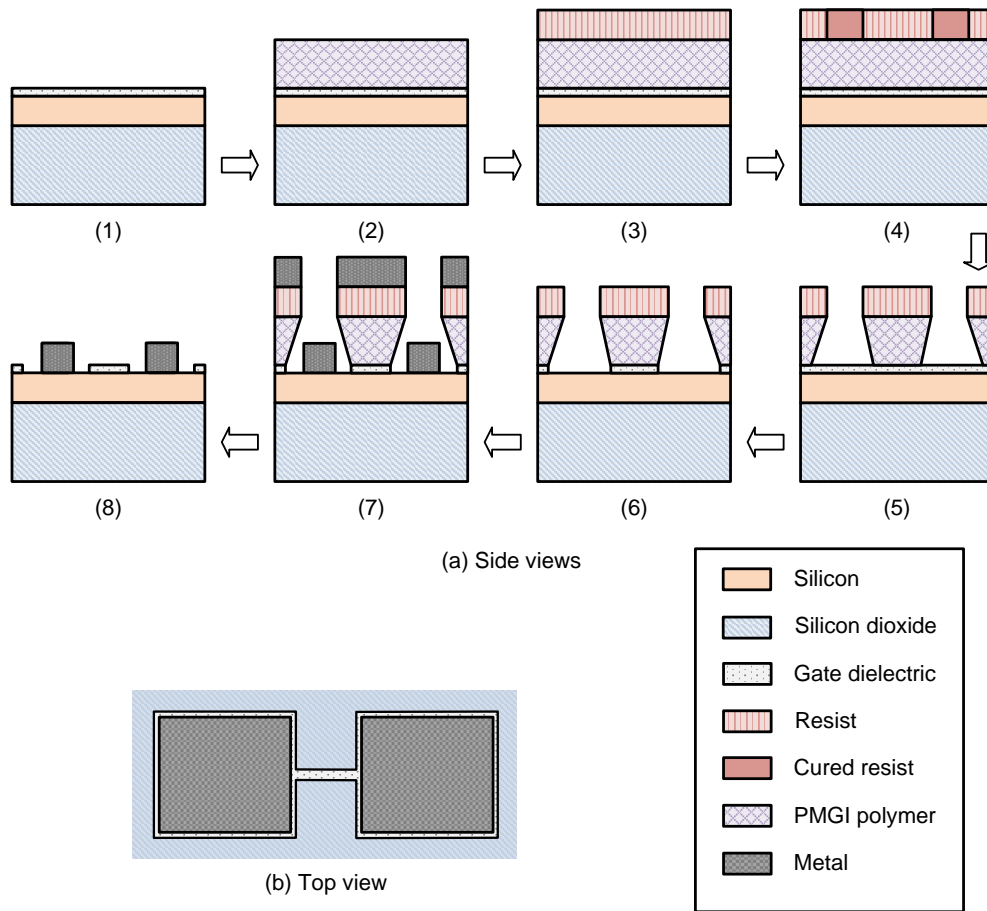
Figure 4.9: (a) Steps of creating the source and drain contacts. (1) Side view of the sample. (2) PMGI polymer is spun. (3) PMMA resist is spun. (4) PMMA is cured by electron beam lithography. (5) Side view after development. (6) Dielectric is etched. (7) Metal is deposited. (8) Side view after lift-off. (b) Top view after lift-off. Creating the gate involves similar steps, except step 6 which is skipped.

We created the contacts by means of lithography, deposition, and lift-off, as summarized in table 4.6. The area of each contact was chosen to be at least $100\mu m \times 100\mu m$, for easy access during measurements. The thickness of the source and drain contacts was $250nm$. The gate material had to be thicker to cover all three sides of the channel in samples with $350nm$ silicon layer. Therefore, we deposited $400nm$ of aluminum as gate material for a number of samples. For other samples, during metal deposition for the gate, we placed the sample on a 45° mount, as shown in figure 4.10 [164]. With this strategy a thinner layer of metal was required to cover the channel area. The drawback was that with our mount/chuck equipment, one side of the channel was not covered by metal (figure 4.10).

(a) (b)
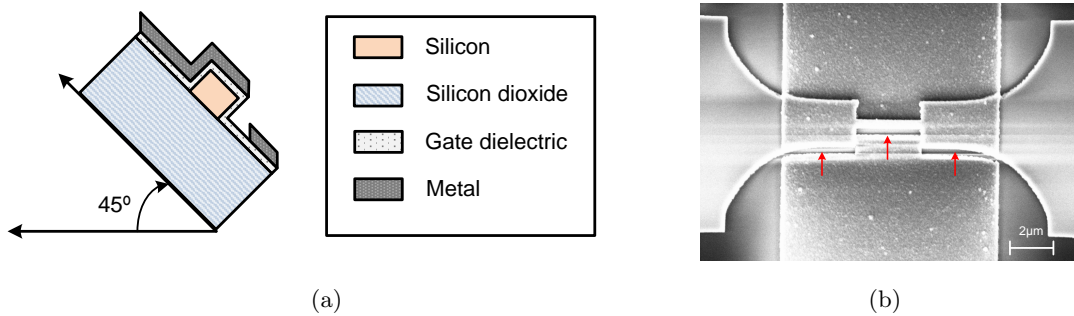
Figure 4.10: (a) Mounting the sample on a 45° angle during metal deposition for gate. The bilayer resist is not shown. (b) SEM image of a gate contact that is deposited using the 45° mount. The arrows show the areas that are not covered with metal.

Since the minimum thickness of the Al layer was $250nm$, in order to have a successful lift-off, we needed to either use a thick electron beam resist such as PMMA A8-A11 [134], or a bi-layer configuration [165]. We chose the second option (figure 4.9), due to access to Polymethylglutarimide (PMGI) Resists. Since the thickness of the available resist, PMGI-SF7, was about $400nm$ [165], we spun two layers of PMGI to achieve the required thickness (for lift off). As summarized in table 4.6, prior to PMGI spin coating, the sample surface was treated with vapor-phase hexamethyldisilazane (HMDS), to increase the adhesion of the resist to the surface [125]. The e-beam resist was PMMA A3, the same resist used to pattern the active region. After electron beam lithography, the PMMA resist was developed first, followed by developing the PMGI layer using Microposit Developer [166]. For source and drain contacts, the sample was then dipped in BHF mixture to wet etch the dielectric. Next, aluminum was deposited on the sample in an Intlvac electron beam deposition system. The residual aluminum was then removed by dipping the sample in Remover PG for lift-off. Figure 4.11 shows a Scanning Electron Micro-graph (SEM) of two of the fabricated devices, with nanowire channels and single and multiple gates.

Table 4.6: Fabrication of the Contacts

	Task	Process	Comments
1	Sample surface treatment	HMDS mono-layer coating	$150°C$ for 5 minutes
2	Source/Drain patterning	1st PMGI spin coating	2800 rpm, baked at $220°C$ for 20 minutes
3		2nd PMGI spin coating	2800 rpm, baked at $220°C$ for 20 minutes
4		PMMA spin coating	3000 rpm, baked at $180°C$ for 20 minutes
5		Electron beam lithography (EBL)	Aperture size = 30 μm, voltage = $20kV$
6		Development	MIBK+IPA (3:1), IPA
7		PMGI wet etch	Microposit Developer, Deionized water, IPA
8	Dielectric removal	BHF wet etch	
9	Source/Drain metal	Al deposition	$250nm$, Electron beam evaporation
10		Lift-off	Remover PG
11	Gate patterning	1st PMGI spin coating	2800 rpm, baked at $220°C$ for 20 minutes
12		2nd PMGI spin coating	2800 rpm, baked at $220°C$ for 20 minutes
13		PMMA spin coating	3000 rpm, baked at $180°C$ for 20 minutes
14		Electron beam lithography (EBL)	Aperture size = 10, 30 μm, voltage = $20kV$
15		Development	MIBK+IPA (3:1), IPA
16		PMGI wet etch	Micro Dev, Deionized water, IPA
17	Gate metal	Al deposition	$350nm$, Electron beam evaporation
18		Lift-off	Remover PG

(a)

(b)
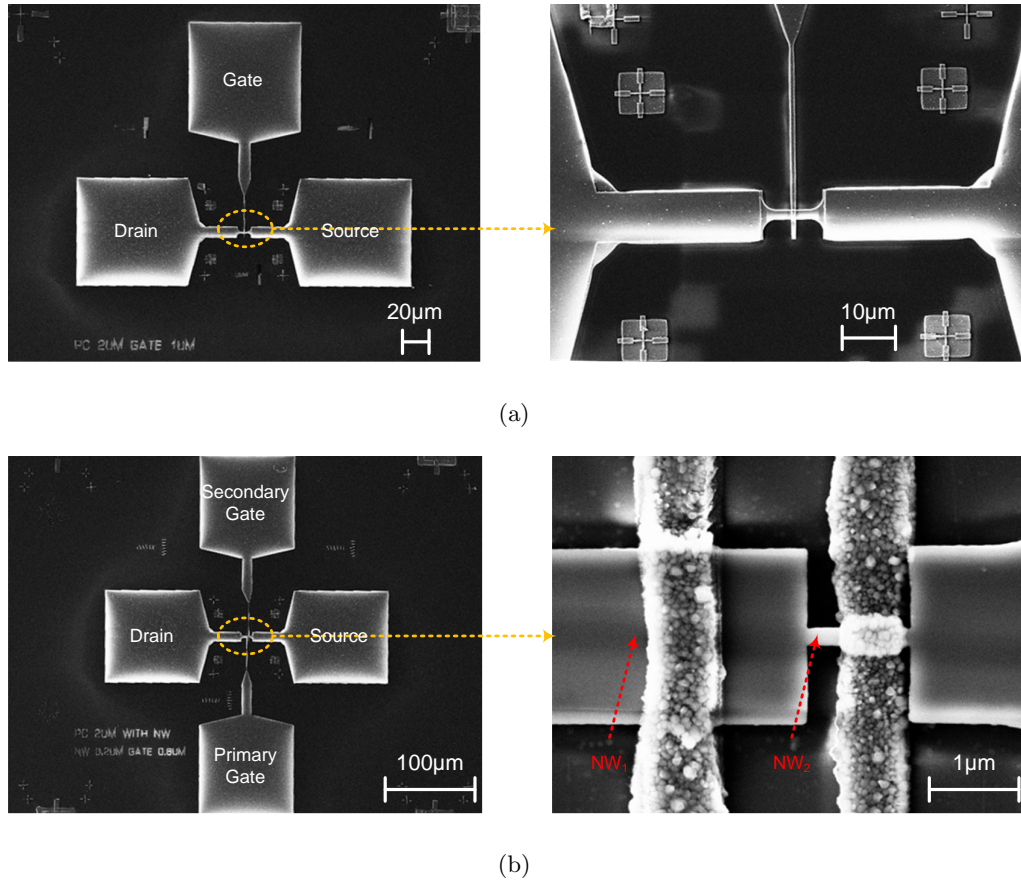
Figure 4.11: SEM graph of a fabricated (a) single gate and (b) multiple gate device (corresponding to figure 3.8).

4.5 Chapter Summary

We described the details of fabricating the photodetector devices in this chapter. We used SOI wafers with silicon layers of $35nm$ and $350nm$ thick, and fabricated both single gate and multiple gate structures, with channel widths ranging from $200nm$ to $10\mu m$. The fabricated devices were all junction-less; since in order to verify the concept of *electrostatic charge control in nanowire devices*, fabrication and measurement of junction-less devices was satisfactory. While fabricating the devices, our primary goal was to proof the design principle ideas. We were not focused on developing technology for industrial purposes, and the facilities we had accessed to, did not provide the required systems either.

We also note that some processes required for our work were not available in our cleanroom, and we sent the samples to other facilities outside the University of Waterloo. The Electron

beam lithography step for creating the alignment marks was done at the 'Toronto Nanofabrication Centre (TNFC)', University of Toronto [167]. For ion implantation, the samples were sent to the 'Core System Inc.' [129]. High temperature annealing for activating the dopants was done in the 'Microfabrication Facility and Molecular & NanoTech User Facility/Center for Nanotechnology' at the University of Washington [130]. For low temperature and forming gas annealing we used the facilities at TNFC at the University of Toronto and also the 'Centre for Advanced Photovoltaic Devices and Systems (CAPDS)' at the University of Waterloo [167, 168].

Chapter 5

Negative Capacitance; Experiment and Theory

The Metal-Oxide-Semiconductor capacitor (MOS cap) is an essential part of a MOS transistor, as the three important biasing modes of the transistor (accumulation, depletion and inversion) occur in the capacitor section. Study of the MOS capacitor gives precious information about the transistor properties, such as the channel doping type, gate dielectric thickness, and non-ideal conditions e.g. interface state properties.

This chapter is devoted to the modeling and fabrication of MOS capacitors. Initially, we fabricated the capacitors to investigate the interface properties of the silicon and the gate dielectric. The very interesting negative capacitance phenomenon emerged later, when we introduced light to the fabricated capacitors. Device modeling revealed that such behavior originates from the surface properties. To our knowledge, this is the first time that a *light induced, negative capacitance* is reported in MOS geometry. The simple fabrication of the capacitor, and also the fact that the dielectric material is non-ferroelectric, are two other features that make this work unique. In this chapter, we start with the case of an ideal MOS capacitor, and study the capacitance-voltage response under dark and illumination conditions. Next we introduce the interface states in the model and investigate the capacitor behavior.

5.1 Ideal MOS Capacitor

Figure 5.1 shows the MOS capacitor of this study. It consists of a p-type silicon layer with thickness of $350nm$, and doping concentration of $10^{15}cm^{-3}$. The thickness and permittivity of
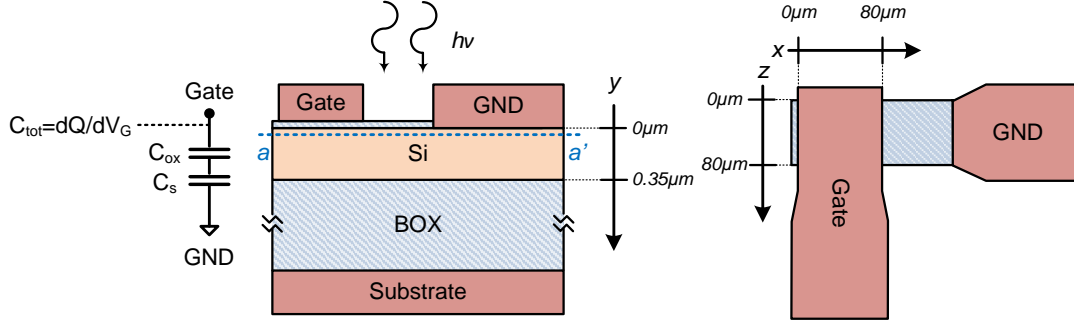
Figure 5.1: Side and top views of the MOS capacitor. The silicon layer is p-type, with doping concentration of $10^{15} cm^{-3}$.

the gate dielectric are $25nm$ and 7, respectively. The buried oxide (BOX) layer is $10\mu m$. The gate covers a dielectric area of $80\mu m \times 80\mu m$ [1]. In this section, the gate, substrate and ground (GND) contacts are all considered Ohmic. In addition, the silicon and dielectric interface is assumed to be defect free.

The Quasi-Static Capacitance-Voltage (QSCV) curve of the MOS capacitor is plotted in figure 5.2(a). We also obtained the electron and hole concentration as a function of the gate voltage at $(x, y) = (40\mu m, 1\mathring{A})$, and plotted the corresponding data in figure 5.2(b). Both dark and illumination data are presented in the figures. During light exposure, a monochromatic light source with wavelength of $633nm$ is used. The device is illuminated over the top, through a window between the gate and GND contacts, as shown in figure 5.1.

Under dark condition, when the gate is biased negatively, the majority carriers (here holes) are accumulated at the interface of the p-type silicon and the dielectric (figure 5.2(b)). The accumulated positive charge acts as the second plate of the capacitor (the first plate is the negatively charged gate contact), and the total capacitance C_{tot} is equal to the geometrical dielectric capacitance that can be easily calculated using the classic capacitance equation.

$$C_{tot}|_{acc} = C_{ox} = \epsilon_0 K_{ox} \frac{A}{t_{ox}} \tag{5.1}$$

where ϵ_0, K_{ox}, A and t_{ox} are the vacuum and dielectric permittivity, the capacitor area and dielectric thickness, respectively [40]. Substituting the capacitor data in equation 5.1 gives a

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[1]Two dimensional framework is used, where the device depth along the z direction is $1\mu m$. For the results presented here, we have multiplied the output data by 80, to include the capacitor depth along the z direction. Since the capacitor dimensions are large, such assumption does not impose inaccuracy to the results.

value of $1.6 \times 10^{-11} F$ as the capacitance in the accumulation mode, which is in a good agreement with that of figure 5.2(a), when $V_G < -1V$.

(a)   (b)   (c)
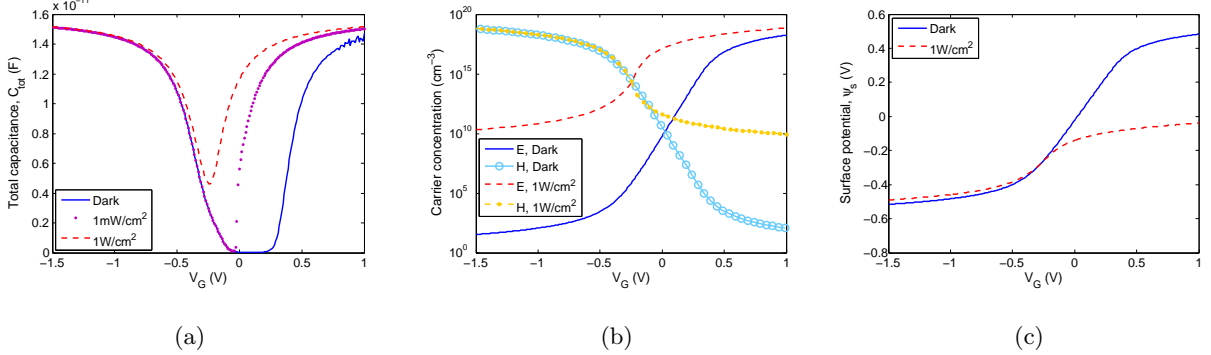
Figure 5.2: (a) Quasi-static capacitance-voltage (QSCV) curves of the MOS capacitor in figure 5.1, under dark and illumination conditions. (b) Electron (E) and hole (H) concentration versus gate voltage at $(x, y) = (40\mu m, 1\mathring{A})$. (c) Surface potential as a function of gate bias, at $(x, y) = (40\mu m, 0)$.

Increasing the gate voltage will push the capacitor towards depletion. Under this circumstance, the majority carriers start to migrate towards the semiconductor bulk, leaving the negatively charged (doping) acceptor states behind. As shown in figure 5.2(b), when the gate voltage increases, the hole (electron) concentration starts to decline (increase). Since the charge that compensates the opposite charge at the gate plate is now spread through the semiconductor layer, the total capacitance is a series combination of the dielectric capacitance C_{ox}, and the semiconductor capacitance C_s [40]. This causes the total capacitance to decrease in depletion mode, as illustrated in figure 5.2(a).

$$C_{tot}|_{depl} = \frac{C_{ox}C_s}{C_{ox} + C_s} \tag{5.2}$$

After the channel is fully depleted, if the gate voltage is increased further, the minority carriers (here electrons) move towards the surface in response to the change of the positive charge at the gate contact. Under quasi-static measurements, the electrons have enough time to concentrate right at the silicon and dielectric interface. As a result, once again the total capacitance is equal to the dielectric capacitance [40].

Figure 5.2(c) illustrates how the surface potential varies as a function of the gate bias. The surface potential is obtained at the silicon and dielectric interface, at $(x, y) = (40\mu m, 0)$. The relationship between the surface potential and the gate bias can be easily derived, by considering

the classic dependence of C_{tot} and C_{ox} to the charge and voltage. Assuming that charge 'Q' is present at the gate plate, while voltage 'V_G' is applied,

$$C_{tot} = \frac{dQ}{dV_G} \tag{5.3}$$

$$C_{ox} = \frac{dQ}{d(V_G - \psi_s)} \tag{5.4}$$

where ψ_s is the surface potential. One can eliminate dQ by combining the two equations, to obtain the relationship between surface potential and the gate voltage.

$$C_{tot} = C_{ox}(1 - \frac{d\psi_s}{dV_G}) \tag{5.5}$$

Equation 5.5 clearly demonstrates that in an ideal MOS capacitor, where $C_{tot} \leq C_{ox}$, the surface potential increases monotonically in response to an increase in the gate voltage. Moreover, the ratio of $d\psi_s/dV_G$ depends on the biasing mode of the capacitor. As illustrated in figure 5.2(c), the ratio is small in accumulation and inversion modes, where the total capacitance C_{tot} is very close to the oxide capacitance C_{ox}. In other words, since in these two modes the charge variation at the gate is compensated by opposite charges at the silicon-dielectric interface, the surface potential does not need to vary in response to the change of the gate voltage. In depletion region however, $d\psi_s/dV_G$ can be large; as C_{tot} may become much smaller than C_{ox}.

Once the MOS capacitor is exposed to light, electron and holes pairs are generated within its semiconductor region. Depending on the gate bias, the extra carriers may impact the capacitance. In accumulation, as shown in figure 5.2(b), the concentration of the electrons at the interface increases by orders of magnitude. However, hole concentration is still orders of magnitude higher; and as a result, the change in the device capacitance and also the change in the surface potential are both very small (figures 5.2(a) and (c)).

In depletion mode, the gate electric field is such that the photo-generated electrons are attracted towards the interface. As a result of these extra available electrons, the semiconductor does not need to be depleted as much in comparison with the dark case. Since the depletion width becomes smaller, the semiconductor capacitor C_s becomes larger, leading to a larger total capacitance, as illustrated in figure 5.2(a). The surface potential also experiences a smaller variation in response to the gate bias, as plotted in figure 5.2(c).

At larger gate biases, the electron concentration at the surface becomes so large that the total capacitance moves towards the inversion. As plotted in figure 5.2(a), at $V_G = 0.25V$, $C_{tot} \approx C_{ox}$.

Note that in the presence of light there is also a lager number of holes close to the interface, as shown in figure 5.2(b). The potential also starts to saturate at a smaller gate bias, due to the early inversion, as shown in figure 5.2(c).

5.2 Negative MOS Capacitor

The negative capacitance phenomena in devices have been reported over the last twenty years. Such phenomena have so far been observed in three classes of devices: forward biased rectifying devices, two dimensional electron/hole gases where exchange-correlation determines the physics, and the ubiquitous metal-oxide-semiconductor devices with ferroelectric gate dielectrics. Reports of the observation of negative capacitance in a broad family of rectifying devices include metal-semiconductor junctions [169], organic light emitting diodes [170–172], solar cells [173], and quantum well infrared photo-detectors [174]. These capacitors have a large leakage current and hence do not have a purely complex impedance, which makes them highly dissipative and unsuitable for low power device applications.

In the second group, the two dimensional electron or hole gas based devices, the total capacitance of a parallel plate capacitor in the quantum limit is a series combination of the geometric capacitance and four other capacitances, which originate from the electrons kinetic energy, exchange energy, correlation energy and from the coupling energy of electrons and phonons [175,176]. Since the exchange and the correlation capacitances can be negative, the total capacitance can take values larger than the geometrical capacitance. Experimentally, a large capacitance has been observed in two-dimensional hole [177] and electron [178] gases, carbon nanotubes [179], and in graphene in the presence of magnetic fields [180, 181], due to negative compressibility arising from the quantum mechanical (exchange-correlation) interaction energy. Negative capacitance corrections have also been proposed in recent experiments involving single layer graphene. Reference [182] proposed that the negative capacitance in Ag-adsorbed single-layer graphene capacitors is due to an interplay between kinetic energy quenching and Coulomb energy variation. While [178] and [182] measure the quantum mechanically induced negative capacitance at liquid helium temperatures, [177] reports it at room temperature.

The third class of devices where negative capacitances have been proposed and observed are conventional metal-oxide-semiconductor (MOS) structures with a novel modification to include a ferroelectric gate dielectric [183]. The polarization versus electric field in ferroelectric materials exhibits a negative slope. This translates into a negative charge versus voltage curve and hence a negative capacitance. As a result, it is possible to design low power devices because sub-threshold

slopes smaller than $60mV/dec$ are feasible in negative capacitance based MOS transistors [183, 184].

Negative capacitances can also be engineered in MOS capacitors with conventional gate dielectrics using alternate methods. According to equation 5.2, when a MOS capacitor is biased in depletion, the total capacitance C_{tot} consists of the geometrical oxide capacitances C_{ox}, in a series combination with the semiconductor capacitance C_s (this neglects quantum effects). While C_{ox} depends on the permittivity and thickness of the oxide, the value of C_s depends on the properties of the semiconductor (bandgap and density of states, doping) and gate bias. In the presence of the trap states at the oxide-semiconductor interface, C_s can also depend on the contribution of filled/empty trap states. Later we will show that the interface states can force C_s to become negative, causing C_{tot} to be larger than C_{ox}.

On the other hand, equation 5.5 shows that C_{tot} can be greater than C_{ox} only when the surface potential of the semiconductor decreases with increase in gate bias (that is, $d\psi_s/dV_G < 0$). While in an ideal MOS cap $d\psi_s/dV_G$ is positive and smaller than unity, in a non-ideal MOS capacitor the interface traps can make $d\psi_s/dV_G$ negative.

In this section, we ask the basic question if capacitances larger than C_{ox} can be induced by photons in a MOS capacitor by making $d\psi_s/dV_G < 0$. The basic idea, which is proposed by us in [185], is the theoretical possibility to fill the traps at the oxide-semiconductor interface by photo-excitation of electrons from the valence band. This filling of trap states by electrons can potentially lead to a large enough *decrease* of the surface potential ψ_s at the oxide-semiconductor interface, leading to the total capacitance larger than C_{ox}.

To keep the discussion of the concept straightforward, we consider p-type silicon with acceptor type interface traps, which are neutral when empty, and negatively charged when filled. These states do not influence the surface potential in accumulation mode, as they are empty and neutral. Sweeping the gate voltage towards depletion leads to the migration of the majority carriers (holes) away from the oxide-semiconductor interface, and attraction of electrons towards the interface, which is accompanied by the lowering of the conduction and valence bands at the interface. With increase in gate voltage, the interface traps start to fall below the Fermi level and fill up. The channel therefore needs to be less depleted in response to the gate voltage increase, as the filled trap states provide a negative charge. This drops the rate at which the surface potential increases with gate bias, when compared to a capacitor without interface traps. Under this circumstance, if a large number of electrons fill the interface trap states, one may be able force the surface potential to decrease (instead of increasing) in response to an increase in the gate voltage. We show that this large number of electrons can be provided by photo-excitation of electrons from
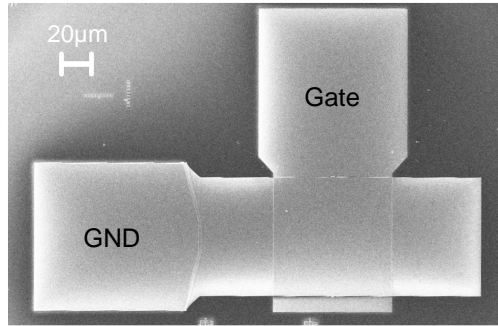
Figure 5.3: SEM image of the fabricated MOS capacitor

the valence band. The resulting capacitance is larger than the geometrical oxide capacitance, and the accompanying C_s is negative.

5.2.1 Device Fabrication and Measurements

We fabricated the MOS capacitors on (100) Silicon on Insulator (SOI) wafers, with the top silicon and buried oxide layers of $340nm$ and $1\mu m$, respectively. The silicon layer is p-type with doping density of about 6×10^{14} to $9.5 \times 10^{14} cm^{-3}$. The fabrication process is based on chapter 4, and is described very briefly here. The active region was created by dry etching the top silicon layer into mesas, using a negative resist (Ma-N 2400) for patterning and also as the etch mask. After dry etching, the resist was removed and the samples were cleaned by Piranha cleaning process (H_2SO_4: H_2O_2, 4:1). Next the native oxide layer was etched away in a buffered Hydro Fluoric acid mixture (BHF, 10:1), and $25nm$ of Aluminum Oxide (Al_2O_3) was deposited over the exposed silicon surface by means of plasma assisted Atomic Deposition Layer (ALD), at $300°C$.

To fabricate the ground (GND) contact, we created appropriate windows in the Al_2O_3 layer using electron beam lithography and then etched the Al_2O_3 layer in a BHF mixture. Next we deposited $250nm$ of Al, followed by the lift-off process. The process of fabricating the gate contact was similar, with the exception of wet etching the dielectric layer. We annealed the samples in forming gas at a temperature of $425°C$ for 30 minutes. Figure 5.3 shows the Scanning Electron Microscope (SEM) image of the MOS capacitor.

The quasi-static capacitance-voltage (QSCV) characteristic of the MOS capacitor is obtained using an Agilent 4155C semiconductor parameter analyzer. During the measurements, the device was illuminated by a laser diode with wavelength of $405nm$ at various intensities. The representative results are shown in figure 5.4(a). Under dark, we do not observe a peak in the CV curve. As the intensity of light from the laser diode increases, we see the emergence of a capacitance peak in

depletion region that grows by increasing the light intensity. At the intensity of $7.2mW/cm^2$, the capacitance peak is larger than the capacitance in accumulation region, which shows the negative capacitance mechanism at work.

We also made capacitance-voltage measurements using the microscope light for illumination, as shown in figures 5.4(b) and (c). The peak in the capacitance is observed here as well. Moreover, contrary to the case of figure 5.4(a), the overall QSCV curve is less noisy.

(a)

(b)

(c)

(d)
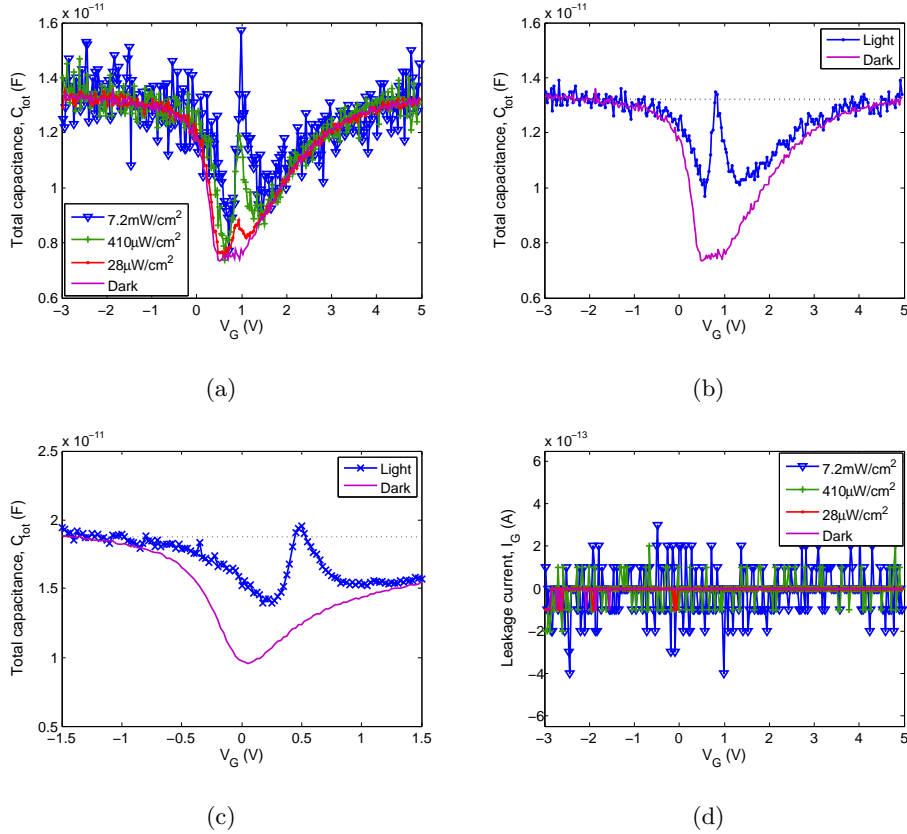
Figure 5.4: (a) Quasi-static capacitance versus voltage (QSCV) curves of a *fabricated* MOS capacitor (*with a non-leaky gate dielectric*) at various light intensities. $t_{ox} = 25nm$ and $\lambda = 405nm$. (b) QSCV curve of the MOS capacitor in (a) when illuminated with microscope light (intensity not recorded). (c) Capacitance versus voltage curves of a MOS capacitor with $t_{ox} = 20nm$, when the microscope light is used for illumination, the light intensity is not recorded. (d) Gate leakage current versus gate voltage for the device in (a).

We also ensured that the leakage current through the gate oxide is negligible, as shown in figure 5.4(d). The phenomena observed in figures 5.4(a)-(c) is different from the large capacitance seen in leaky capacitors. The CV curve, and the corresponding gate current of a *leaky* MOS capacitor

are plotted in figure 5.5. The gate leaks as its voltage is increased to values of more than about $3V$ (inversion mode, figure 5.5(b)). The parameter analyzer calculates the capacitance by applying a small voltage ΔV_G to the gate, and reading the small signal current i during an integration time Δt. The capacitance is then calculated by

$$C = \frac{\Delta Q}{\Delta V_G} = \frac{i \Delta t}{\Delta V_G} \tag{5.6}$$

As a result, (due to the leakage current) the measured capacitance increases, showing a value which is much larger than the dielectric capacitance.

<div align="center">(a)   (b)</div>
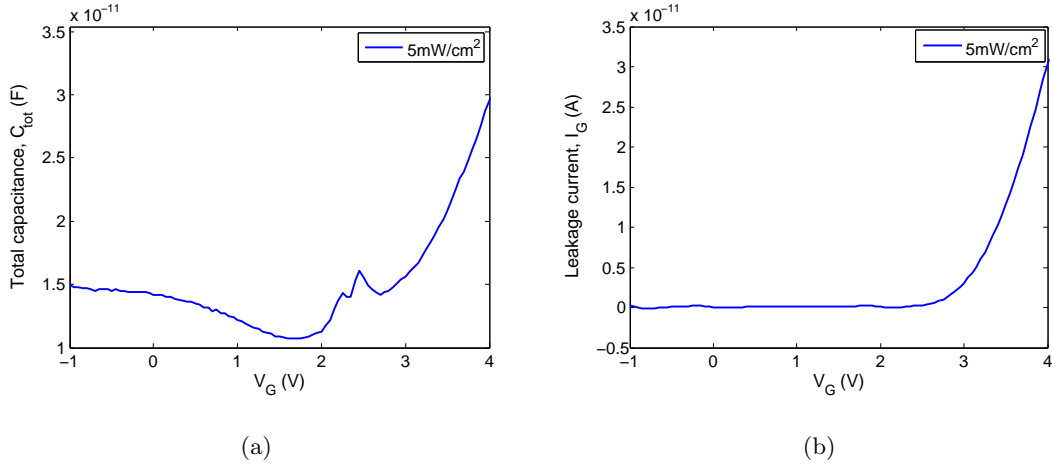
Figure 5.5: (a) Quasi-static capacitance versus voltage (QSCV) curve of a *fabricated* MOS capacitor with *leaky* gate dielectric. $t_{ox} = 25nm$ and $\lambda = 532nm$. (b) Gate leakage current versus gate voltage.

5.2.2 Device Modeling

We construct a model to explain the peak in capacitance observed in the experiments. The device is shown in figure 5.1, and its dimensions are comparable to the experimental device. We consider p-type silicon that is $350nm$ thick with a doping concentration of $10^{15}cm^{-3}$. The thickness and permittivity of the top dielectric (Al_2O_3) are $25nm$ and 7, respectively [2]. The buried oxide (BOX) layer is $10\mu m$ thick. A work-function of $5.5eV$ is assigned to the gate that covers a dielectric area of $80\mu m \times 80\mu m$. The substrate and GND contacts are considered Ohmic.

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[2]Later and after obtaining the total capacitance, we use a scaling factor of 0.86 for fitting purposes. The goal is to fit the simulated and measured values of the capacitance in the accumulation mode (e.g. C_{ox}).

The numerical calculations are performed using the drift-diffusion framework at room temperature [94]. The *bulk* minority carrier lifetime is assumed to be $10^{-5}s$. The trap states at the silicon-dielectric interface are modeled using the bandgap interface defect model [94] that approximates the density of the acceptor- and donor-like states by a Gaussian and an exponential distribution. The numerical values for distributions are summarized in table 5.1. These values are determined so as to match the CV under dark condition in our experiments and are close to the values reported in literature for a silicon-alumina interface [186].

Table 5.1: Parameters of the bandgap interface defect model

Defect type	Gaussian distribution			Exponential distribution	
	Energy that corresponds to the peak (eV)	Total density of states $(cm^{-2}eV^{-1})$	The characteristic decay energy (eV)	Density of trap states at the band edge $(cm^{-2}eV^{-1})$	The characteristic decay energy (eV)
Acceptor	0.35	10^{12}	0.4	2×10^{13}	0.12
Donor	0.6	10^{6}	0.3	2×10^{12}	0.2

The density of the filled traps depends on the overall trap density, and also on the trap ionization probability. The probability of an acceptor type interface trap to be occupied at energy E_t is [187]

$$F_{tA} = \frac{v_n \sigma_{An} n + e_{Ap}}{v_n \sigma_{An} n + v_p \sigma_{Ap} p + e_{An} + e_{Ap}} \tag{5.7}$$

In equation 5.7, n, p, v_n and v_p denote the electron and hole concentration, and the electron and hole thermal velocity, respectively. σ_{An} and σ_{Ap} are the electron and hole capture cross sections, with values of 10^{-16} and $10^{-14} cm^2$, respectively. e_{An} and e_{Ap} are the electron and hole emission rates, described by:

$$e_{An} = v_n \sigma_{An} n_i e^{(\frac{E_t - E_i}{kT})} \tag{5.8}$$

$$e_{Ap} = v_p \sigma_{Ap} n_i e^{(\frac{E_i - E_t}{kT})} \tag{5.9}$$

where n_i and E_i are the intrinsic charge concentration and the intrinsic Fermi level, respectively. The probability of a donor type interface trap being filled is [187]

$$F_{tD} = \frac{v_p \sigma_{Dp} p + e_{Dn}}{v_n \sigma_{Dn} n + v_p \sigma_{Dp} p + e_{Dn} + e_{Dp}} \tag{5.10}$$

where σ_{Dn} and σ_{Dp} are the electron and hole capture cross sections, with values of 10^{-14} and $10^{-16} cm^2$, respectively. e_{Dn} and e_{Dp} represent the electron and hole emission rates for donor type interface traps, described by:

$$e_{Dn} = v_n \sigma_{Dn} n_i e^{(\frac{E_t - E_i}{kT})} \tag{5.11}$$

$$e_{Dp} = v_p \sigma_{Dp} n_i e^{(\frac{E_i - E_t}{kT})} \tag{5.12}$$

The simulated quasi-static capacitance at dark and various light intensities is shown in figure 5.6(a). The light (wavelength=405nm) is illuminated over the MOS capacitor as shown in figure 5.1. We find that a peak in the capacitance emerges in depletion in the presence of photons, which is in qualitative agreement with the experimental results in Figure 5.4. As the intensity of light increases, the capacitance peak increases in magnitude and exceeds the value of the oxide capacitance. Using the simulated value of the capacitor and the oxide capacitance in figure 5.6(b), the semiconductor capacitance (C_s in equation 5.2) is calculated and plotted in Figure 5.6(c). The value of C_s is negative between gate voltages of $0.85V$ and $1.05V$.

The surface potential versus gate voltage from the model at three different cross sections is plotted in figure 5.6(d), where we observe a negative slope. That is, the surface potential of the semiconductor decreases with increasing gate voltage. The surface potentials are obtained at three different interface points, $x = 15, 40$ and $65\mu m$ (figure 5.1). The difference in the curves comes from the fact that each point receives a different amount of photo-generated carriers. Under such a condition, equation 5.5 is still valid if it is slightly modified. To take the non-uniformity of the surface potential into the account, one can break the total MOS capacitor into a parallel combination of n smaller capacitors along the x direction, where each capacitor has a length of Δx, ($n \times \Delta x = L$, L: gate length). The total capacitance would therefore be:

$$C_{tot} = \frac{C_{ox}}{n} \sum_{k=1}^{n} (1 - \frac{d\psi_{sk}}{dV_G}) \tag{5.13}$$

where ψ_{sk} represents the surface potential of the k-th capacitor. The dashed curve in figure 5.6(b) is obtained using equation 5.13 with $n = 8$, which agrees well with the simulated capacitance.
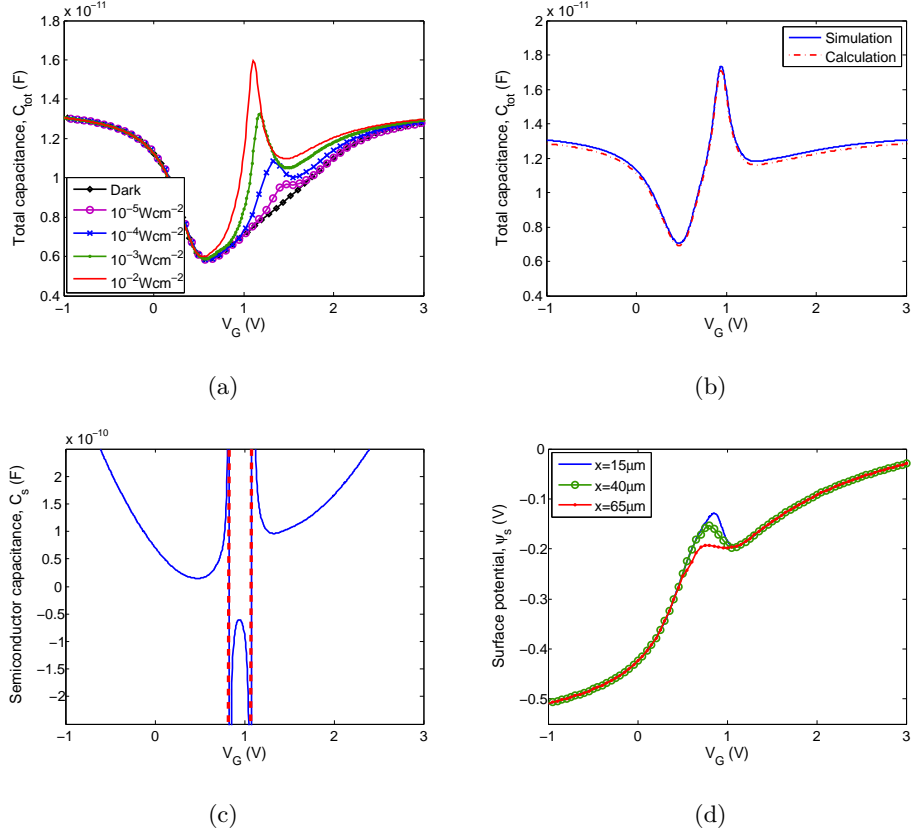
Figure 5.6: Results from modeling and calculations (capacitor dimensions are presented in figure 5.1). (a) The capacitance versus voltage for different light intensities calculated using the drift-diffusion framework. (b) The solid line is the capacitance corresponding to the intensity of $1Wcm^{-2}$; the dashed line is obtained from the surface potential data using equation 5.13. (c) Semiconductor capacitance, C_s. (d) Surface potential at different points underneath the gate.

The gate voltage determines the location of the capacitance peak, by controlling the way the interface traps are filled. As shown in figure 5.7(a), there exists a lateral potential along the channel (cutline aa' in figure 5.1), whose height is controlled by the gate. At gate voltages below $0.5V$, the barrier height is very high. Therefore, only few photo-generated electrons can diffuse towards the areas under the gate. As a result, the number of filled interface states does not change in comparison with the dark case. This is illustrated in figure 5.7(b), that shows the density of the occupied traps as a function of gate bias, under dark and illumination.

For gate voltages larger than $0.5V$, the photo-generated electrons see a potential profile in the channel where transport is feasible. A large stream of electrons diffuse underneath the gate and fill the interface traps, causing a sharp change in the density of the ionized traps, as marked

with an arrow in figure 5.7(b). Such variation in the charge density at the interface states is more than what is required to compensate the slight voltage change at the gate, ΔV_G. As a result, the depletion width has to be reduced to decrease the overall available negative charge; in other words the surface potential has to decrease.

(a)

(b)
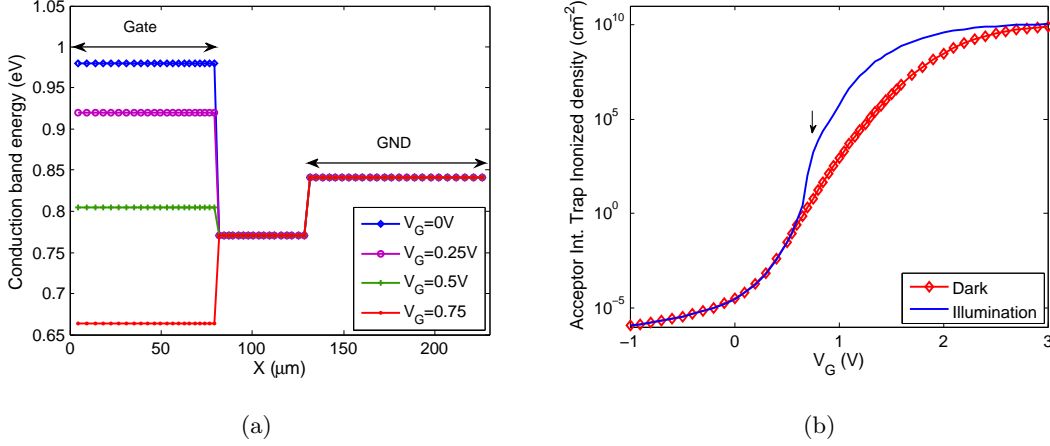
Figure 5.7: (a) Conduction band energy, along the channel below the gate dielectric. (b) Density of the occupied trap states. Capacitor dimensions are presented in figure 5.1. The plots are obtained at $(x, y) = (30 \mu m, 0.1 \overset{\circ}{A})$.

Figure 5.8 illustrates the impact of the interface trap density over the quasi-static CV curve. In order to obtain the data we multiplied the original trap density (D, table 5.1) by a factor ranging from 0.02 to 20. The change of the CV curve is quite dramatic when the density of the trap states is varied. If the trap density is small, the number of the filled states is not sufficient to force the potential to decrease. In this case, as shown for factors of 0.02D and 0.05D in figure 5.8(a), there is very little or no peak in the CV curve. The impact of the interface traps becomes more tangible at higher trap densities and the peak in the CV curve grows. However, at higher densities the peak starts to decrease and broaden as the trap density changes from D to 10D (figure 5.8(b)), up to a point that it seems to disappear (figure 5.8(b), 20D). The reason is that when the interface trap density is high, more traps can be filled by a small change in the surface potential. As a result, $d\psi_s/dV_G$ and therefore the peak in capacitance decrease. In addition, when the gate voltage is changed by ΔV_G, a major part of the charge is compensated by the filled traps. The channel is therefore less depleted for the same bias, and therefore the peak in the CV curve is moved towards higher gate biases. An increase in acceptor trap density to much larger values significantly changes the shape of the CV curve; since the inversion of the channel cannot occur, and the capacitance remains fixed at the value of the geometrical capacitance. Under this

circumstance a peak in the capacitance is again not seen in the simulations.

(a)

(b)
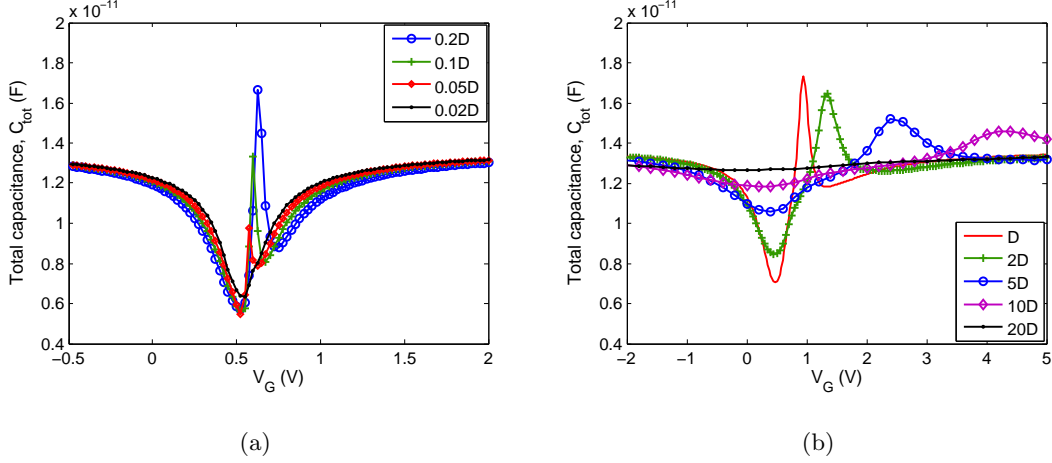
Figure 5.8: Impact of interface trap density on the photon induced capacitance peak. CV curve versus gate bias, when the trap densities are (a) smaller and (b) larger than the original trap density shown in table 5.1. Capacitor dimensions are presented in figure 5.1.

5.2.3 Design Considerations: Role of Thickness and Width

As discussed earlier, the negative capacitance is due to the filling of the trap states at the semiconductor-oxide interface. Therefore, it is very important for the injected electrons to reach the interface. If a large number of electrons remains at the bulk section of silicon, the resulting negative charge contributes in compensation of the positive charge variation at the gate. Study of the surface potential in figure 5.6(d) shows that the negative slope of the surface potential varies at different points of the interface. The slope becomes more pronounced a interface points that are located farther from $x = 80\mu m$ and closer to $x = 0$ (figure 5.1). The reason is that the photo-generated electrons are injected laterally into the area underneath the gate. As a result, there is a larger concentration of electrons at areas close to $x = 80\mu m$.

Both diffusion and drift mechanisms affect the movement of the photo-generated electrons. Underneath the gate contact ($x = 0$ to $80\mu m$), there exists a strong electric field along y-axis. Along the x- axis however, the electric field component is more local around $x = 80\mu m$, and very small at other regions. The photo-generated electrons that enter the area under the gate move to the left due to diffusion, and drift towards the surface due to the vertical component of electric field. The net movement would be somewhat diagonal. As a result, those electrons that are located farther from the interface (deeper in the silicon layer) take a longer path to reach the

surface.

Based on this conclusion, if the thickness of the silicon layer is reduced, the injected electrons will reach the interface after passing a shorter pathway. Therefore, one expects a stronger contribution of the interface states, and hence a stronger negative capacitance. Figure 5.9(a) demonstrates how the silicon thickness impacts the QSCV curves of MOS capacitors. When the silicon thickness is $20nm$, the capacitance shows a peak that is more than 3 times larger than the geometrical capacitance, C_{ox}. The peak decreases as the silicon layer thickness increases.
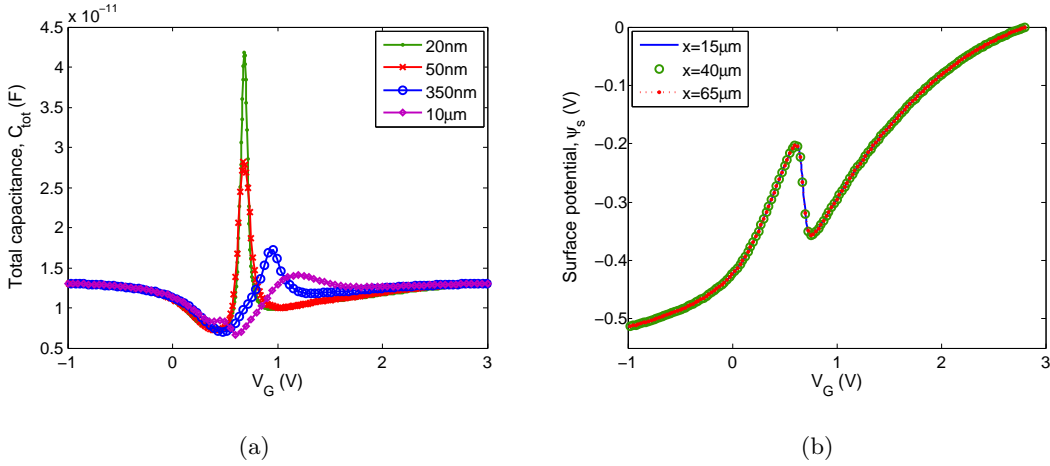
Figure 5.9: (a) Impact of the thickness of the silicon layer on the capacitance peak. (b) Surface potential at different points underneath the gate, for a MOS capacitor with silicon thickness of $20nm$.

Due to the same reason, in a thin MOS capacitor one expects less variation in the surface potential along the x direction, as plotted in figure 5.9(b) (compare to figure 5.6(b), which is for silicon thickness of $350nm$). The contribution of the photo-generated electrons in the bulk is more localized to the areas closer to $x = 80\mu m$, causing the surface potential at other regions to be entirely determined by the interface states.

The length of the gate can also affect the capacitance peak in the CV curve. For a fixed silicon thickness, decreasing the gate length leads to a stronger contribution of the bulk electrons. As a result, the peak in the total capacitance would drop in devices with shortened gates. This is verified in figure 5.10, where we have plotted the QSCV curve of two MOS capacitors, with silicon thickness of $350nm$, and gate length of $80\mu m$ and $40\mu m$. For ease of comparison we have assumed the width of the gate in the shorter capacitor is twice the width of gate in the longer capacitor, so that both capacitors have the same area. As demonstrated in the figure, the capacitance peak is smaller in the shorter capacitor.
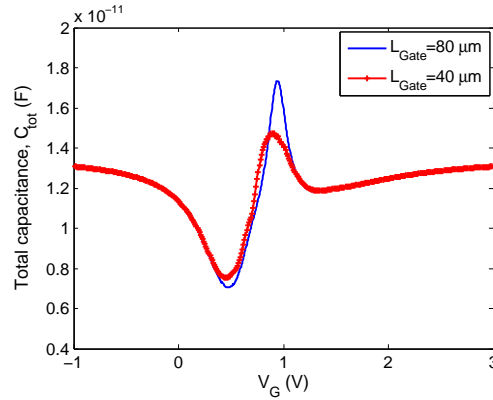
Figure 5.10: Impact of the gate length on the capacitance peak. In both capacitors the area is $6.4 \times 10^3 \mu m^2$. Silicon thickness is $350 nm$.

5.3   Chapter Summary

We report the experimental observation of negative capacitance in a conventional MOS capacitor in the presence of photons. The physics behind the phenomena is the filling of the trap states at the semiconductor-oxide interface, which in turn leads to a decrease in surface potential with increase in gate voltage.

Design and implementation of this phenomenon is presented in a capacitor where a non-ferroelectric aluminum oxide layer serves as the gate dielectric, and the capacitor is in depletion mode. Through extensive modeling, we establish that trap states at the semiconductor-oxide interface, coupled with the injection of photo-generated electrons are responsible for the negative capacitance. We find that varying the trap density and/or light intensity can tune the value of the negative capacitance. We show that in the presence of photons, the experimentally measured quasi-static capacitance in depletion is almost twice the value without photons. Further, the measured capacitance is larger than the values in accumulation and inversion.

To our knowledge, this is the first time that a light induced, negative capacitance is reported in MOS geometry. The simple fabrication of the capacitor, and also the fact that the dielectric material is non-ferroelectric, are two other features that make this work unique.

Chapter 6

Measurement Results

In this chapter we present the current-voltage measurement results of the fabricated junction-less phototransistors. First, the measurement setup is described briefly and next, the details of each device, together with their measurement plots are discussed.

6.1 Measurement Setup

Figure 6.1 illustrates the setup we used for our measurements. The Device Under Test (DUT) is placed on the stage of a probing station, and stabilized by vacuum. Access to each device contact is provided through a micro-positioner and coaxial/triaxial cables that connect the contact pad to a Source Monitor Unit (SMU) of a parameter analyzer. Each SMU is used for applying a voltage or a current to the contact, and reading the voltage or current at each contact.

For illumination measurements a light source is mounted over the probe station unit. For our measurements we used a laser diode with $\lambda = 405nm$, whose power can be controlled by a controller unit. Other light sources with fixed intensity are also used, as will be described later in the chapter.

6.2 Decision about Device Thickness

We fabricated the first device generation on SOI wafers with top silicon layer of $340nm$. The overall fabrication procedure is similar to the description in chapter 4. Some differences and highlights are summarized below.
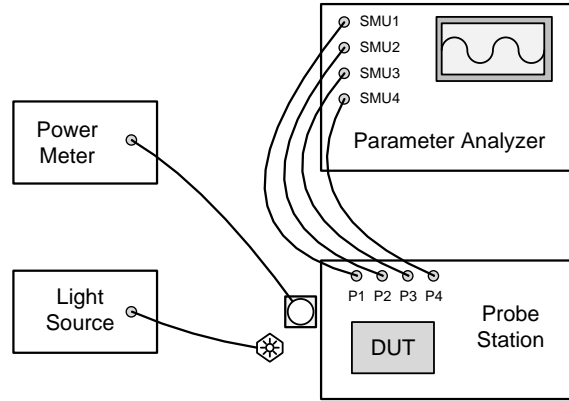
Figure 6.1: The measurement setup for current-voltage measurements.

- The SOI wafer was p-type with doping density of about 6×10^{14} to $9.5 \times 10^{14} cm^{-3}$. The thickness of the buried oxide layer was about $1\mu m \pm 22.5 nm$.

- Devices with channel widths of $200 nm$ were fabricated. The total channel length, and the nanowire length are $17\mu m$, and $1.2\mu m$, respectively. Figure 6.2(a) shows a fabricated structure.

- The gate dielectric layer (Al_2O_3) is $35 nm$ thick, and the length of the gate region is $1\mu m$.

- The samples were placed on a $45°$ mount during gate material deposition, as discussed in chapter 4, section 4.4.

- Each sample was annealed in forming gas at $425°C$ 30 minutes, after deposition of source and drain metal.

Figure 6.2(b) presents the drain current of a structure, as a function of the gate voltage. The current shows a very weak dependence on the voltage. The current variation is less than two orders of magnitude as the gate is swept by $20V$. It is as if the channel is just partially depleted in response to the positive bias of the gate. One possible reason for the incomplete depletion of the channel can be the trap states that are present at the interface of the silicon and the Al_2O_3 layer. Lack of gate coverage on all three sides of the channel (due to placing of samples at 45 degree during deposition of the gate metal) can also contribute to the incomplete depletion of the channel.

In order to have a deeper insight on the impact of the surface states, we also studied the measured Quasi-Static Current Voltage (QSCV) curves of MOS capacitors. The specification of

(a)   (b)
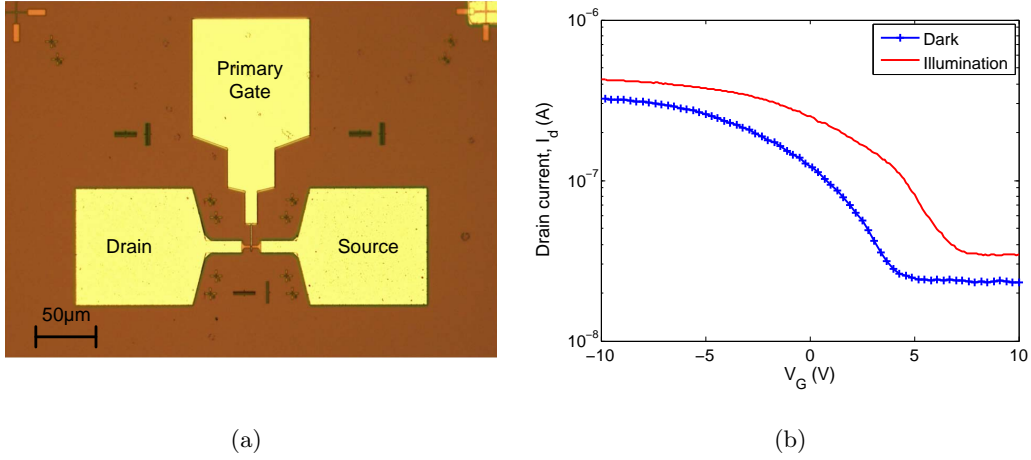
Figure 6.2: A fabricated single gate, junction-less photodetector with a nanowire channel. (b) Drain current as a function of gate bias, under dark and illumination. Channel width: $200nm$. Total channel length: $17\mu m$. Nanowire length: $1.2\mu m$. Semiconductor thickness: $350nm$. $V_S = 0V$, $V_D = 1V$. Light intensity is not recorded.

these capacitors and their fabrication process is discussed in chapter 5. The graphs in figure 6.3 belong to four MOS capacitors. All capacitors are identical in terms of surface area ($80\mu m \times 80\mu m$) and dielectric material (Al_2O_3). In figures 6.3(a) and (c), the active region of the capacitors is fabricated based on table 4.4 in chapter 4, where a negative resist (Ma-N 2400 series) is used for patterning. The same resist is also used as the etching mask. For the results presented in figures 6.3(b) and (d), the active region is fabricated by following the steps described in table 4.3, where we used a hard metallic mask (Al) for etching. The dielectric thickness for all capacitors is $25nm$, except for the device in figure 6.3(c), where it is $20nm$. Due to the difference of dielectric thickness, we have plotted the value of C_{tot}/C_{ox} [1] for easier comparison. Regardless of the approach for the fabrication of the active region, the minimum ratio of C_{tot}/C_{ox} is mostly around 0.5 and smaller (figure 6.3(a) and (b)), with the minimum measured ratio of about 0.2 (figure 6.3(c) and (d)).

When a MOS capacitor is biased in depletion, the total capacitance C_{tot} is a series combination of the geometrical capacitance C_{ox} and the semiconductor capacitance C_s (equation 5.2). Considering the relationship of a parallel plate capacitor to the area (A), thickness (t) and permittivity (ϵ) or $C = \epsilon A/t$, one can simplify the ratio of C_{tot}/C_{ox}.

$$\frac{C_{tot}}{C_{ox}}\big|_{depl} = \frac{\epsilon_s t_{ox}}{\epsilon_s t_{ox} + \epsilon_{ox} t_s} \tag{6.1}$$

---

[1]C_{tot}: total capacitance, C_{ox}: dielectric capacitance.

Subscripts s and ox in equation 6.1 represent the semiconductor and dielectric, respectively. The minimum ratio of C_{tot}/C_{ox} is achieved when the channel is at its maximum depletion. Therefore, the equation can be used to determine the maximum channel depth (t_s) that is fully depleted. We have calculated t_s for different ratios of C_{tot}/C_{ox}, and summarized the data in table 6.1.
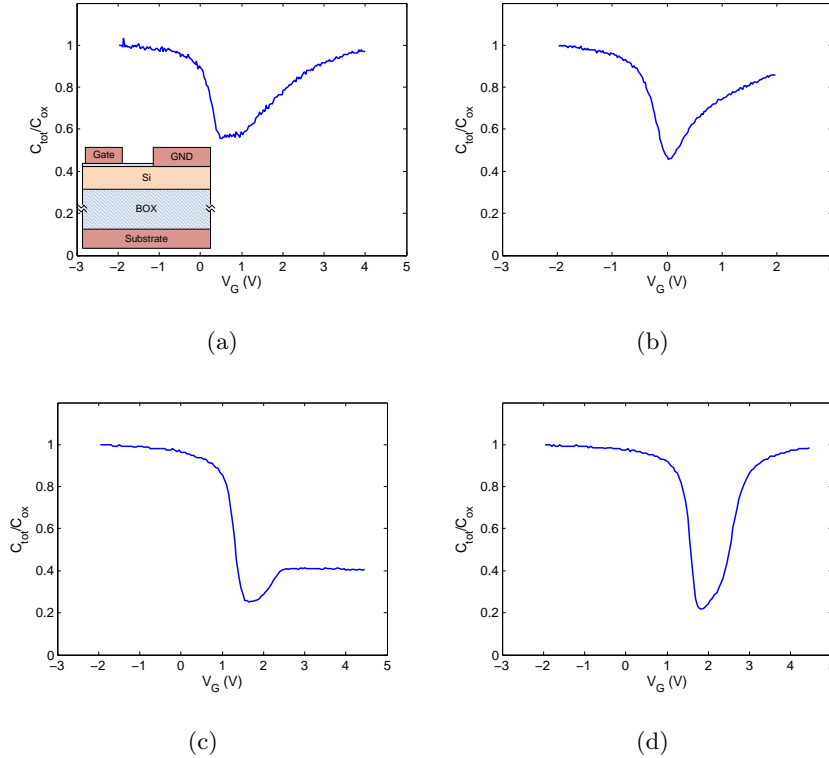
Figure 6.3: The ratio of C_{tot}/C_{ox} in four different MOS capacitors (figure 5.3). The active region is $350nm$ thick. The gate covers a dielectric area of $80\mu m \times 80\mu m$. The dielectric thickness is $25nm$ for capacitors in (a), (b) and (d); and $20nm$ for the capacitor in (c).

According to table 6.1, in order to deplete the total thickness of $340nm$, the minimum ratio of C_{tot}/C_{ox} must be around 0.1. However, as plotted in figure 6.3, the best ratio that we achieved was about 0.2, that corresponds to a depletion width of about $170nm$.

We remark that due to the three dimensional characteristic of the fabricated MOS capacitors, and also the position of the 'ground' (GND) with respect to the 'gate' contact (inset of figure 6.3(a)), the numbers can differ from table 6.1. However, the table gives us a good approximation of the thickness of the active region that can be fully depleted by the gate. In order to ensure that our devices will be depleted even under the worst case of measured C_{tot}/C_{ox} (figures 6.3(a),

Table 6.1: Maximum possible depletion width (t_s), as a function of C_{tot}/C_{ox}

$C_{tot}/C_{ox}\|_{min}$	0.1	0.2	0.3	0.4	0.5
$t_s(nm)$	379.3	168.6	98.3	63.2	42.1

Device area: $80\mu m \times 80\mu m$.
Semiconductor permittivity: $k_s = 11.8$
Dielectric permittivity: $k_{ox} = 7$
Dielectric thickness: $t_{ox} = 25nm$

(b)), we chose a SOI wafer with top layer thickness of less than $40nm$ [2]. First we fabricated junction-less single gate structures on thin SOI wafers to ensure the practicality of this strategy. The device specifications are summarized below.

- Devices are fabricated on SOI wafers, with top silicon layer of $35nm$ thick. The resistivity of the silicon layer is in the range of $8.5 - 22\Omega.cm$. The doping concentration is therefore estimated between 5.9×10^{14} and $1.6 \times 10^{15}cm^{-3}$ [40]. The thickness of the buried oxide layer is about $145nm \pm 5nm$.

- The channel length is $70\mu m$. The channel width is $10\mu m$ at the contacts and narrows down in areas under the gate, as illustrated in figure 6.4(a).

- The gate dielectric layer (Al_2O_3) is $25nm$ thick. Dielectric material is deposited at the *nanoFAB Fabrication & Characterization Facility* of University of Alberta [188].

- Since the thickness of the active region is $35nm$ only, there is no need to place the samples on a $45°$ mount during gate material deposition (chapter 4). The samples are placed on a flat mount, and the gate material (aluminum) covers all three exposed sides of the channel.

- Each sample is annealed in forming gas once after deposition of dielectric, and a second time after deposition of source and drain metal. The first annealing process takes about 30 minutes at $425°C$, while the second process is 10 minutes at $400°C$.

The current-voltage measurements on these structures are performed by my colleague Jenny Wan at the University of Washington. The voltage is supplied by a *Keithley 2612B SYSTEM Source Meter*®, and the current is read by the same system. The electrical connections to the device are provided by two coaxial cables that connect the drain and gate contacts to two SMUs

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[2]The most important drawback of the thin substrate is that it leads to a small absorption, that will be discussed later.

<table>
<tr><td>(a)</td><td>(b)</td></tr>
</table>
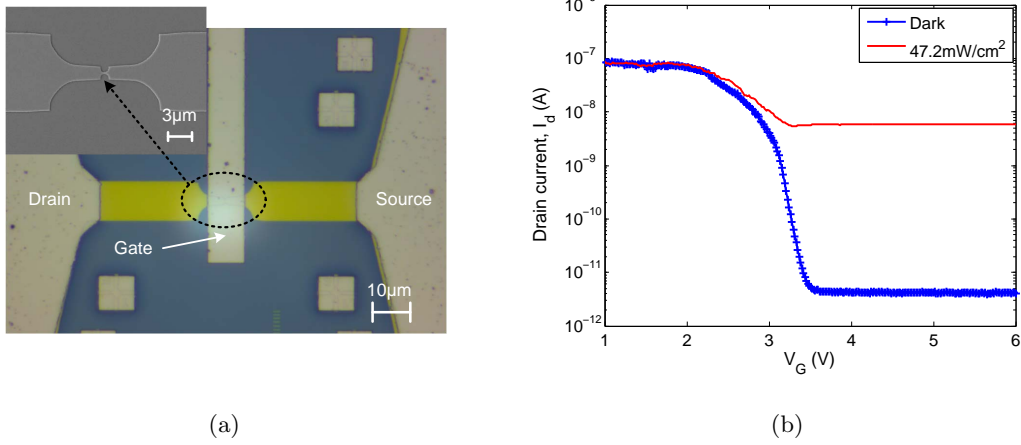
Figure 6.4: (a) Single gate, junction-less photodetector with a nanowire channel. The gate is $10\mu m$ long in the picture (picture is taken by Jenny Wan at the University of Washington). Inset shows the SEM image of the active region. (b) Drain current as a function of gate bias, under dark and illumination. Channel width: $200nm$. Device thickness: $35nm$. Gate length: $40\mu m$. Total channel length: $70\mu m$. $V_S = 0V$, $V_D = 1V$, and $\lambda = 405nm$.

of the source meter. The source contact is connected to the ground. An LED laser pointer with wavelength of $405nm$ is used for illumination. The light source is directly placed over the samples with no coupling through fiber optics. Figure 6.4(b) illustrates the change of the drain current as a function of the gate bias, for a device whose channel is $200nm$ wide at its narrowest region.

Under dark condition, the device shows an ON/OFF ratio of more than 4 orders of magnitude, which is quite an improvement in comparison with the earlier results presented in figure 6.2. Also when illuminated, at gate voltages of larger than about $3V$, the current changes dramatically, indicating the lateral bipolar action at work.

6.3 Multiple Gate Structures

Motivated by the improved measurement results, we fabricated junction-less, multiple gate devices by following an approach similar to that used for the device in figure 6.4. The specifications of these structures are summarized below.

- Devices are fabricated on SOI wafers, with top silicon layer of $35nm$ thick. The silicon layer is p-type, and its resistivity is in the range of $8.5 - 22\Omega.cm$.

- Multiple gate devices with different combinations of NW_1, and NW_2 are fabricated. The width of (NW_1, NW_2) include $(10\mu m, 2\mu m)$, $(10\mu m, 0.2\mu m)$, $(2\mu m, 2\mu m)$, and $(2\mu m, 0.2\mu m)$.

- The total channel length, the distance between source and drain contacts, in all of the devices is $70\mu m$. For devices with channels narrower than $10\mu m$ the channel width starts with $10\mu m$ at the contacts and narrows down close to the gate. Moreover, the two gates are positioned symmetrically with respect to the source and drain, and the reason for this strategy will be discussed later.

- The gate dielectric is $25nm$ of Al_2O_3 (deposited in our cleanroom). The length of the gate region is $10\mu m$ for both primary and secondary gates. The spacing between the two gates is $10\mu m$.

Figure 6.5 shows an optical image of a multiple gate structure, as well as two Scanning Electron Micrograph (SEM) images of the NW_1 and NW_2 regions (located inside the black oval in figure 6.5(a)).

(a) (b) (c)
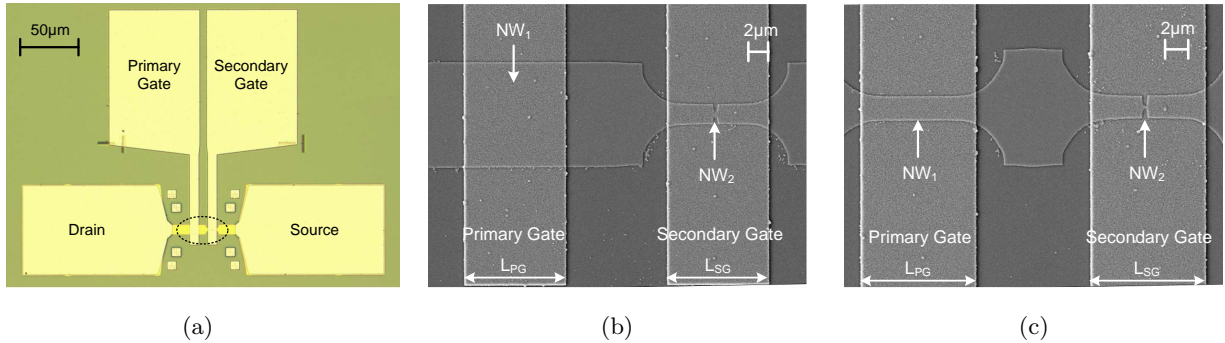
Figure 6.5: (a) Junction-less phototransistor with multiple gates. (b) SEM image of the device channel (inside the black oval in (a)), showing NW_1 ($10\mu m$ wide) and NW_2 ($200nm$ wide). (c) SEM image of the channel, showing NW_1 ($2\mu m$ wide) and NW_2 ($200nm$ wide). Device thickness is $35nm$. The gate lengths L_{PG} and L_{SG} are both $10\mu m$.

Cascade® probe station and triaxial cables are used to electrically connect each photodetector to an Agilent 4155C® parameter analyzer for current-voltage measurements. The light source is a laser diode with the wavelength of $405nm$ and tunable optical power. Figure 6.6(a) shows the current as a function of the primary gate bias, for a device whose NW_1 and NW_2 are $2\mu m$ and $200nm$ wide, respectively. The device OFF state starts at about $V_{G(primary)} > 3V$; and the device shows an ON/ OFF ratio of more than four orders of magnitude under dark condition. The current under illumination, also plotted in the is same figure, clearly shows the lateral bipolar

effect. The current during illumination varies as a function of light intensity in an almost linear trend over $50mW/cm^2$ change of intensity, as shown in figure 6.6(b). The data for this graph is obtained by averaging the current at each intensity over $3.5V < V_{G(primary)} < 5V$.

As discussed in chapter 3 (section 3.2.1), the secondary gate is designed to bias NW_2 in accumulation. It pulls up the potential barrier and increases the carrier concentration in NW_2. This in turn causes the emitter efficiency of the device to increase, resulting in an increased photocurrent. Figure 6.6(c) shows the current as a function of the secondary gate, when the primary gate is biased at $3V$ (OFF state). When the secondary gate is greater than about $2.7V$, it essentially acts as an extension of the primary gate. Below this voltage however, the secondary gate increases the carrier concentration in the source region, and the photocurrent as a result (figure 6.6(c)).

(a)   (b)   (c)
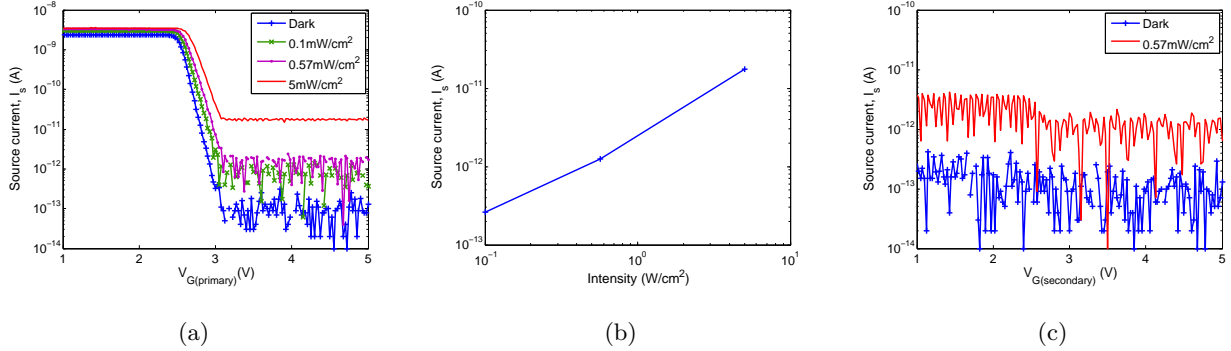
Figure 6.6: (a) Current versus the primary gate bias, under dark and different illumination intensities. The secondary gate is biased at $V_{G(secondary)} = -3V$. (b) Current as a function of light intensity in (a). (c) Current versus the bias of the secondary gate, when the primary gate is biased at $V_{G(primary)} = 3V$. The width of NW_1 and NW_2 is $2\mu m$ and $200nm$, respectively. Other dimensions are similar to figure 6.5. $V_S = 1V$, and $V_D = 0V$.

In addition, according to chapter 3 (sections 3.1.2 and 3.2), in order for the gates to be able to effectively control the channels, the width of NW_1 and NW_2 regions has to be carefully selected. Among the two regions, for the devices presented here, NW_1 is less critical. This is due to the fact that the $35nm$ layer of silicon in the fabricated structures is thin enough to be fully depleted by the primary gate. However, biasing in accumulation by the secondary gate is a more localized effect that mostly influences the charges that are close to the interface of the semiconductor and dielectric. As a result, a larger volume of NW_2 can be influenced by the secondary gate as it gets narrower; and one expects a larger photocurrent in the device with a narrower NW_2.

In order to verify the role of NW_2/ secondary gate combination, the current of two devices is compared in figures 6.7(a) and (b). Each figure represents the current as a function of the primary gate bias, under dark and also for two illumination intensities. The two devices have similar geomrties; the only difference is the size of NW_2 region. At $V_{G(primary)}$ of greater than about $3.25V$, where the photodetectors operate under lateral bipolar action, both devices show an equal level of dark current. However, for both intensities, despite being about 10 times narrower, the photocurrent of the structure with NW_2 : $200nm$ wide (figure 6.7(b)) is more than 4.5 times larger than that of the device with NW_2 : $2\mu m$ wide (figure 6.7(a)).

This result clearly verifies the role of narrower NW_2 regions in improvement of the photocurrent. We should also note that although the dark level of the two detectors seems to be the same, this amount of current is very close to the minimum level of current that is detectable by the parameter analyzer, and as a result we can not consider it as an accurate measure of dark current.

(a)   (b)
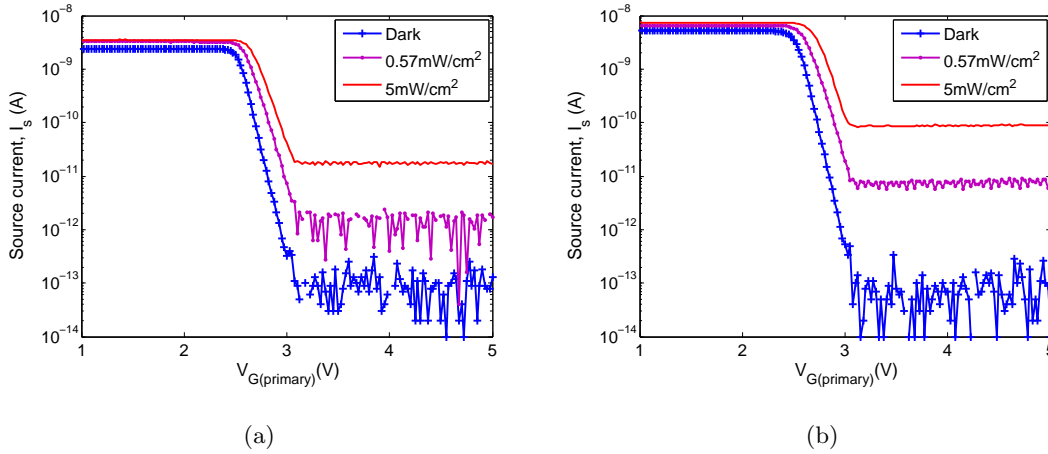
Figure 6.7: Current versus the primary gate bias for devices with (a) NW_1: $10\mu m$ wide and NW_2: $2\mu m$ wide, and (b) NW_1: $10\mu m$ wide and NW_2: $200nm$ wide. Other dimensions are similar to figure 6.5. $V_D = 0V$, $V_S = 1V$, $V_{G(secondary)} = -3V$, and $\lambda = 405nm$.

6.3.1 Normal and Mirrored Measurements

As we measured different devices on different samples, we found some inconsistencies in the results. Devices with similar 'nominal' size and geometry generated different amount of current. Some examples are plotted in figure 6.8. For the three devices in figure 6.8(a), NW_1 and NW_2 are $2\mu m$ and $200nm$ wide, respectively. The devices show different threshold levels, as well

as different levels of current during illumination. Several parameters can impact the threshold voltage of a transistor. Variation in semiconductor doping and dielectric thickness, fixed trap charge in the dielectric and also the interface trap charge can all change the threshold voltage of a transistor [40].

Variation of the semiconductor thickness, especially when the device is only $35nm$ thick, and also variation in the channel size can both impact the current. Position of the light source over the device plays a very important role, as well. Misplacement of the light source can change the photo-current drastically. The data in figure 6.8(b) belong to two measurements of a single device. While the dark currents look very similar, the current under illumination has changed. To minimize the measurement errors during illumination, we used alignment marks to ensure the light source is correctly positioned.

(a)   (b)
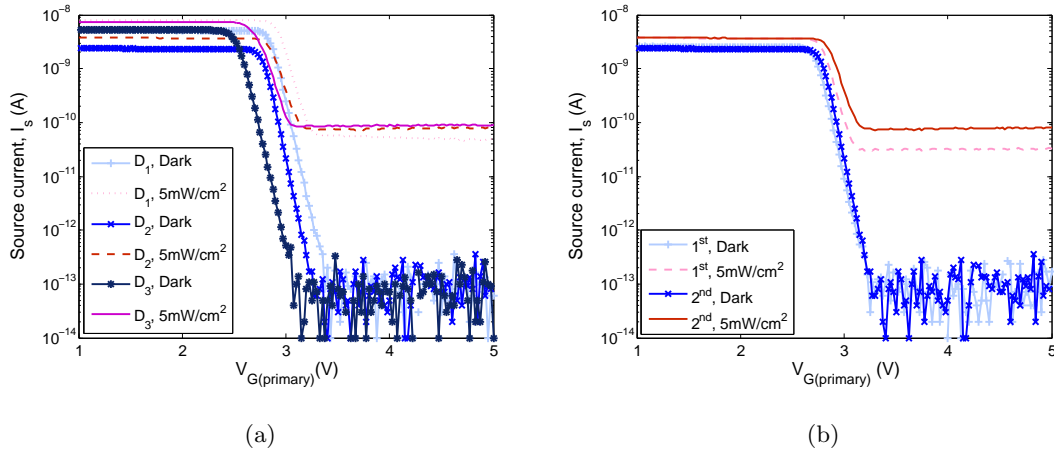
Figure 6.8: (a) Current versus the primary gate bias for three devices (labeled D_1, D_2 and D_3) with similar size and geometry. (b) Two measurements of a single device (D_2). The width of NW_1 and NW_2 is $10\mu m$ and $200nm$, respectively. Other dimensions are similar to figure 6.5. $V_D = 0V$, $V_S = 1V$, and $V_{G(secondary)} = -3V$. $\lambda = 405nm$.

In addition to the alignment considerations, we perform another experiment to ensure that the observed results are not due to measurement setup errors such as misplacement of the light source. This time, during the whole experiment, the light source and also the device are kept at fixed positions. First, the dark and illumination currents are measured while $V_D = 0V$, $V_S = 1V$, and $V_{G(secondary)} = -3V$; and the primary gate voltage is varied between 1 and $5V$. We name this experiment as the 'normal' measurement.

We compare the above 'normal' measurements to 'mirrored' measurements. 'Mirrored' measurements refer to the condition where the roles of source and drain are flipped compared to

'normal' measurements, and the roles of the primary and secondary gates are also flipped. That is, now, $V_D = 1V$, $V_S = 0V$, $V_{G(primary)} = -3V$ and $V_{G(secondary)}$ is varied between 1 and 5V. The nomenclature of 'primary' and 'secondary' gates is the same as figure 6.5. This experiment is important as it can show the impact of the nanowire size more clearly. The effect of unwanted, external factors such as variation in the silicon thickness and the size of (nominally equal) channels in different devices, and also alignment errors during placement of the light source are minimized here. Furthermore, the symmetric position of the gates with respect to the source and drain regions allows for the specific comparison of the nanowires.

The normal/ mirrored measurement results for three devices are presented in figure 6.9. In agreement with our previous observations shown in figure 6.7, in each device, the illumination current is larger when the channel underneath the *negatively biased* gate is narrower.

(a)   (b)   (c)
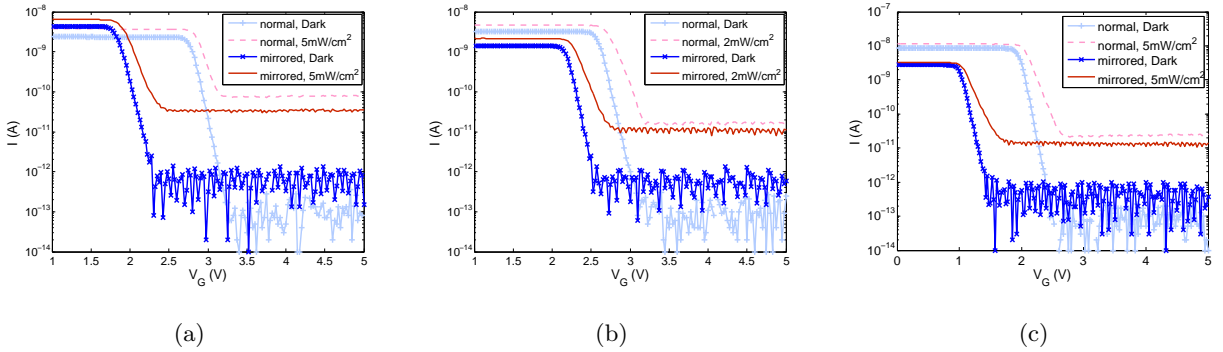
Figure 6.9: Normal measurement: change of the current (at source contact) as a function of primary gate bias, under dark and illumination. $V_D = 0V$, $V_S = 1V$, and $V_{G(secondary)} = -3V$. Mirrored measurement: change of the current (at drain contact) as a function of secondary gate bias (acting as primary gate), under dark and illumination. $V_D = 1V$, $V_S = 0V$, and $V_{G(primary)} = -3V$. (a) NW_1 width=10μm, NW_2 width=200nm. (b) NW_1 width=10μm, NW_2 width=2μm. (c) NW_1 width=2μm, NW_2 width=200nm. Other dimensions are similar to figure 6.5. $\lambda = 405nm$.

We present modeling results to further discuss the device response under normal and mirrored measurements using two dimensional simulations. The conduction band energy of a multiple gate structure under normal and mirrored biasing is plotted in figures 6.10(b) and (c). The device itself, shown in figure 6.10(a), has the same channel and primary/ secondary gate length as the fabricated devices. NW_1 in this structure is 500nm wide; while NW_2 is 40nm. The energy bands are obtained along the channel, shown by AA' in figure 6.10(a).

The energy bands show the importance of the nanowire width under the negatively biased
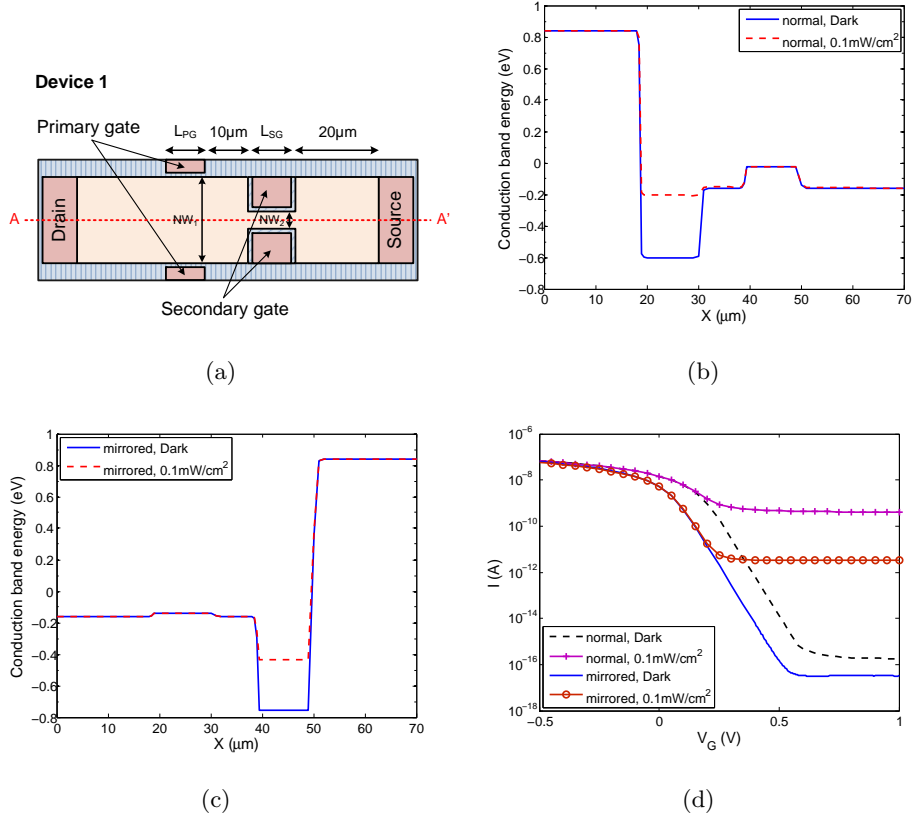
Figure 6.10: (a) Two dimensional, multiple gate junction-less structure with NW_1 width=$0.5\mu m$, NW_2 width=$40nm$. (b) Conduction band energy (cutline AA'), normal biasing ($V_D = 0V$, $V_S = 1V$, and $V_{G(secondary)} = -2V$). (c) Conduction band energy (cutline AA'), mirrored biasing ($V_D = 1V$, $V_S = 0V$, and $V_{G(primary)} = -2V$). (d) Current as a function of gate bias. $\lambda = 405nm$.

gate. Under 'normal' biasing, the secondary gate *strongly* controls the barrier height of NW_2 ($40\mu m < x < 50\mu m$) as shown in figure 6.10(b). In comparison, under 'mirrored' biasing, the primary gate is not as effective in controlling the barrier height on NW_1 ($20\mu m < x < 30\mu m$) as shown in figure 6.10(c). Therefore, under illumination, the change in barrier height for 'normal' biasing ($20\mu m < x < 30\mu m$ of figure 6.10(b)) is larger than the change in barrier height for 'mirrored' biasing ($40\mu m < x < 50\mu m$ of figure 6.10(c)). This causes the photocurrent under normal biasing to be larger, as illustrated in figure 6.10(d).

We also notice from figures 6.10(b) and (c) that under dark, the overall barrier height (for the charge flow) is larger when the biasing is mirrored. The reason is the stronger effect of the positively biased secondary gate in depleting the $40nm$ wide NW_2 (figure 6.10(c), $40\mu m < x < 50\mu m$), compared to the case of $500nm$ channel when the device is biased normally (figure 6.10(b),

$20\mu m < x < 30\mu m$). As a result, as plotted in figure 6.10(d), we expect the level of dark current under mirrored biasing to be smaller than that of the normal case.

However, when we studied the measured dark currents in figure 6.9, we noticed that contrary to the simulation results, the dark current level was higher during mirrored measurements. Initially this seemed puzzling, as the channel NW_2 was narrow and thin enough to be fully depleted, and therefore we expected the observed dark current to be at least as low as the normal case (limited to the machine accuracy). Later we learned that the higher dark current during the mirrored measurement was due to the poor protection of the device from the background light. For the next experiments we covered the device correctly, and the dark level during mirrored measurements reduced, as shown in figure 6.11.

(a)   (b)
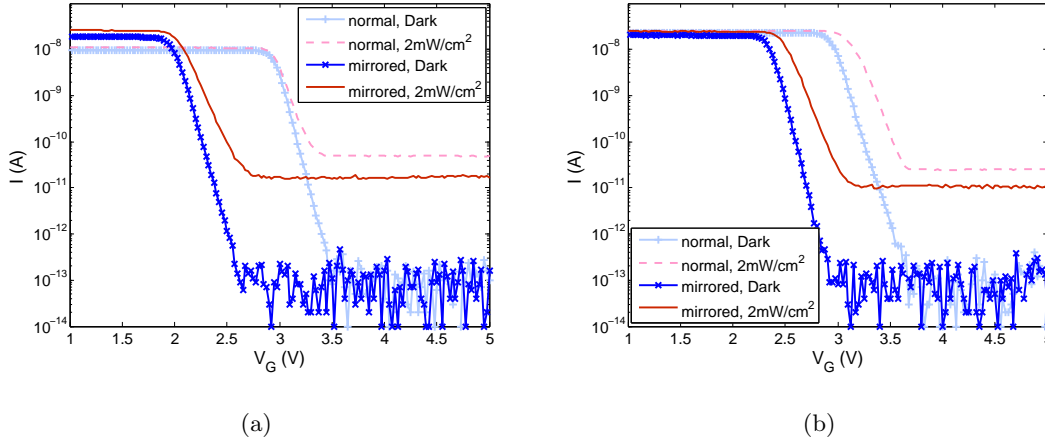
Figure 6.11: Normal measurement: change of the current (at source contact) as a function of primary gate bias, under dark and illumination. $V_D = 0V$, $V_S = 1V$, and $V_{G(secondary)} = -3V$. Mirrored measurement: change of the current (at drain contact) as a function of secondary gate bias (acting as primary gate), under dark and illumination. $V_D = 1V$, $V_S = 0V$, and $V_{G(primary)} = -3V$. (a) NW_1 width=$10\mu m$, NW_2 width=$200nm$. (b) NW_1 width=$10\mu m$, NW_2 width=$2\mu m$. Other dimensions are similar to figure 6.5. $\lambda = 632nm$.

Using the experimentally obtained dark and photo- currents, we calculated the optical gain of the photodetectors [3]. We found that the devices were not able to generate a large optical gain. For example, the optical gain of the photodetector shown in figure 6.7(b) is about 0.08 when the light intensity is $5mW/cm^2$. Although this looks contrary to the results obtained in chapter 3, we think three reasons are responsible for the structures small optical gain.

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[3]For information about calculating the optical gain, please see Appendix B.

Firstly, the thin active region leads to a small attenuation. The absorption coefficient of silicon is about $10^5 cm^{-1}$ at $\lambda = 405nm$. Considering the $35nm$ thick active region, the attenuation ($1 - e^{-\alpha D}$, α: absorption coefficient, D: thickness) is about 0.3.

Secondly, the fabricated devices are not optimized to generate a large gain. There are a number of parameters (discussed in chapter 3) that can be modified in order to improve the device in figure 6.5. For example, in the fabricated structures the two gates are placed symmetrically, as it was necessary for us to be able to try normal and mirrored measurements. However, as discussed in section 3.2, the asymmetrical placement of the gates causes more photo-generated carriers to contribute to the lateral bipolar action. Furthermore, the $250nm$ thick aluminum that is used as the gate material reflects the incident light. To provide a wider area for light absorption, the length of the primary gate (L_{PG} in figure 6.5) can be reduced.

Figure 6.12 illustrates how such modifications can improve the photocurrent. In comparison with the *Device 1* shown in figure 6.10(a), two major changes are made in *Device 2*. The gates are located closer to the source, and the width of the primary gate is reduced to $1\mu m$. As a result, the photocurrent increases by more than 45 times, as shown in figure 6.12(b). The dark current, photocurrent, and also the optical gain of the two devices are summarized in table 6.2. The data shows the importance of such modifications in improving the optical gain.

|(a)| |(b)|
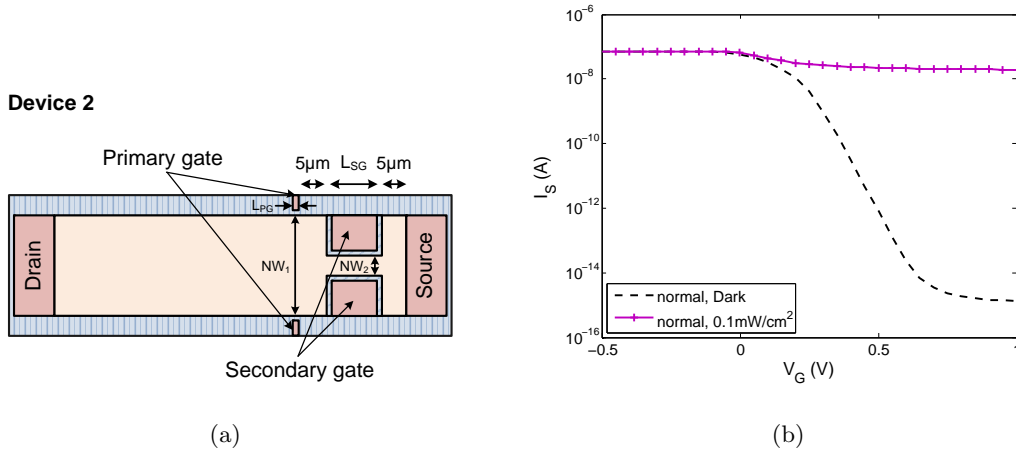
Figure 6.12: Strategies for performance improvement. (a) Two dimensional view of the modified structure. (b) Source current as a function of primary gate bias. NW_1 width=$0.5\mu m$, NW_2 width=$40nm$, $V_D = 0V$, $V_S = 1V$, $V_{G(secondary)} = -2V$, and $\lambda = 405nm$.

Surface recombination is the third and perhaps the most important reason that causes the optical gain of the fabricated structures to be small. In chapter 3, we used the state of the art surface recombination velocity of $13cm/s$ for discussing the role of surface recombination.

However, study of the MOS capacitors (section 6.2) shows that the surface recombination velocity of the fabricated structures can be orders of magnitude larger. This degrades the device response dramatically; e.g. it increases the level of dark current, and decreases the photocurrent.

To clarify this, we modeled Device 1 and Device 2, assuming a surface recombination velocity of $10^3 cm/s$. The results are listed in table 6.2. In comparison with the ideal case, the dark current in Device 1 increases by two orders of magnitude as a result of surface recombination. The change of the photocurrent is slightly larger than 100 times. Surface recombination causes the optical gain of this device to drop by more than 120 times.

The dark current in Device 2 is less vulnerable to the surface recombination. At similar conditions, the dark current increases by about 13 times. The reason is that the potential barrier at NW_1 mainly determines the dark current level, and the shorter length of the primary gate in Device 2 results in a weaker recombination at dark.

Table 6.2: Effect of surface recombination on phototransistors

	Ideal			Surface recombination		
	I_{dark} (A)	I_{photo} (A)	G_{opt}	I_{dark} (A)	I_{photo} (A)	G_{opt}
Device 1	1.8×10^{-16}	4.1×10^{-10}	50.9	1.8×10^{-14}	3.4×10^{-12}	0.42
Device 2	1.3×10^{-15}	1.9×10^{-8}	2070.9	1.8×10^{-14}	1.4×10^{-11}	1.5

G_{opt} : Optical gain.
$NW_1 = 500nm$, $NW_2 = 40nm$.
$V_{G(primary)} = 1.0V$, $V_{G(secondary)} = -2.0V$.
A surface reflection of 50% is considered. The photocurrent presented here is multiplied to transmission.
Minority carrier lifetime $= 10^{-5}$s.
For data in columns 4-6, surface recombination velocity $= 10^3$ cm/s.

However, the photocurrent of Device 2 drops by more than 3 orders of magnitude due to surface recombination. To clarify this, we remark that the 'ideal' optical gain of Device 2 is about 50 times larger than that of Device 1 (third column in table 6.2), meaning that the variation of barrier height at NW_1 in Device 2 is more sensitive to the number of trapped electrons. As a result, recombination of the photo-generated electrons due to surface traps leads to a larger degradation in the photocurrent of Device 2.

6.4 Chapter Summary

In summary, we presented the measurement results of the fabricated structures in this chapter. The thickness of the active region was $340nm$ in the first generation of our devices. The measurements showed a weak dependence of the device current to the gate voltage. The current variation was less than two orders of magnitude during the ON/ OFF state of the device. One possible reason for the low ON/OFF ratio is the incomplete depletion of the channel due to recombination at the interface of silicon and the dielectric layer. Our studies on the fabricated MOS capacitors revealed that the surface states can decrease the depletion width to less than $45nm$. The second reason for the poor response of the devices to the gate voltage is the lack of gate coverage on all three sides of the channel.

To address both of these issues, we fabricated the second generation of devices on a SOI wafer with a thin silicon layer having a thickness of $35nm$. This allowed for full depletion of the channel, as well as complete metal gate coverage on three sides of the dielectric surrounding the channel. The new devices showed an ON/ OFF ratio of more than 4 orders of magnitude.

In addition, we discussed possible reasons for the low optical gain in our fabricated devices. Fabricating devices with a thicker active region to enhance the fraction of photons absorbed, and more importantly, future work to improve the surface passivation will increase the optical gain and lead to phototransistors with high optical gain.

The measurement results verified our design considerations proposed in chapters 2 and 3, that **band engineering through smart use of nanowire/ gate geometries** can improve the photocurrent in phototransistors. We demonstrated that the photocurrent in a junction-less, multiple gate photodetector is enhanced if the width of the nanowire under the secondary gate is reduced.

Chapter 7

Conclusion and Future Work

At the beginning of this dissertation and in chapter 1, we set our goal to model the electrostatic behavior of nanowire based junction and junction-less phototransistors, to find answers to the following questions:

1. What are the advantages and disadvantages of using nanowires in the channel of photodetectors, in comparison to similar geometries without nanowires?

2. How does the photodetector respond as the nanowire parameters such as width, depth, or doping is varied?

3. Are there ways to incorporate nanowires in photodetectors in order to enhance their performance? What we are specifically looking for is increasing the ability of the device to detect low level intensities.

4. Would the fabricated structures verify the results obtained by modeling?

As the platform of our study, we selected junction and junction-less phototransistors with nanowires incorporated within their channels. Lateral bipolar action is the principle behind the operation of both type of phototransistors, although it is achieved differently in each device. Our work and accomplishments are summarized below:

1. **Modeling Nanowire Based Junction Phototransistors:** Our investigations on single gate junction phototransistors with nanowire channels revealed that reducing the channel width can decrease the level of dark current, especially if the channel doping level is low.

However, our results did not show photocurrent improvement as a result of using a nanowire channel. At the same rate of striking photons, the photocurrent of devices with narrower channels showed degradation when compared with the results of devices with wide channels. We expected the results to be even poorer considering the limitation of single nano-scale channels in absorbing light.

2. **Modeling Nanowire Based Junction-less Phototransistors:** We also investigated the role of nanowire channels in junction-less phototransistors. The change in the dark current as a function of the channel width was exponential and non-linear in junction-less nanowire devices. This proved to be due to the fact that creation of the lateral bipolar action in junction-less transistors strongly depends on the strength of the gate in controlling the channel and creating the potential barrier. As a result, the lateral bipolar action is feasible when the channel width moves towards the nano-scale range. However, similar to the case of junction phototransistors, decreasing the nanowire width did not improve the device photocurrent.

3. **Proposing New Nanowire Based Devices:** In the quest to find a solution for photodetector performance improvement, we made modifications in the phototransistor channels and allocated a **wide region** for light absorption purpose. In addition, we found the key element for an improved photocurrent to be the superior ability of band engineering in nanowires incorporated in Metal Oxide Semiconductor (MOS) geometries. The charge flow in the narrow nanowires can be strongly controlled by biasing the gate.

   In both **junction** and **junction-less** geometries we incorporated nanowires within the channel for electrostatic purposes. We used a **nanowire/primary gate** combination to bias the device in lateral bipolar action, and keep the dark current low. The lateral bipolar action in junction and junction-less devices was maintained differently, due to the fact that the operating principles of the two structures are different.

   We also incorporated a **nanowire/secondary gate** combination in the device channel to increase the photocurrent. In junction phototransistors, the secondary gate was added over the nanowire channel for the purpose of lowering the barrier by depleting the carriers. Whereas in junction-less transistors the role of the secondary gate was to artificially create a junction. The design allowed for increased photocurrent, and optical gain. Combined with the low dark current, both designs showed improved Noise Equivalent Powers (NEP).

4. **Developing Fabrication Process:** We developed the required processes for fabricating the nanowire based (junction or junction-less, single or multiple gate) devices. Fabrication

of junction-less transistors involved more than 30 steps of of cleaning, electron beam lithography, dry and wet etching, dielectric deposition, dielectric removal, metal deposition and annealing. We used pre-developed recipes when available. We also developed new recipes to better suit the specific needs of our design.

5. **Experimental Validation of Proposed Devices:** The measurement results obtained on the fabricated junction-less phototransistors verified our design considerations proposed in chapters 2 and 3, that band engineering through smart use of nanowire/ gate geometries can improve the photocurrent in phototransistors. We demonstrated that the photocurrent in a junction-less, multiple gate photodetector is enhanced if the width of the nanowire under the secondary gate is reduced. The gain was however small and we believe that this is due to surface recombination.

6. **Modeling and Fabrication of Negative Capacitance:** We showed that light can induce negative capacitance in MOS geometries. During QSCV measurements of MOS capacitors, we observed that the total capacitance is larger than the geometrical capacitance in depletion region in the presence of light. Through extensive modeling, we established that trap states at the semiconductor-oxide interface, coupled with the injection of photo-generated electrons are responsible for the negative capacitance.

7.1   Ideas for Future Work

During the design and modeling of the photodetector devices, we used the minimum required models to avoid shadowing the core design idea by unnecessary complications. Besides that and while fabricating the devices, our main goal was to proof the design principle ideas. We were not focused on developing technology for industrial purposes, and our cleanroom facility did not provide the required systems either. In this section we discuss ideas that give a broader perspective about this work, and improve the performance of the devices.

1. **Modeling the Surface Effects:** We briefly discussed the effect of surface states in chapters 3 and 6. This non-ideal effect strongly depends on the fabrication process. However, modeling and analyzing the effect of surface states would give us more insight to modify the design and minimize the impact of the surface states. Improving the fabrication process to reduce the interface effects is also an important step towards optimal devices.

2. **Investigating the Design for other Materials:** Our proposed concepts of channel modification and the use of multiple gates can be applied to photodetectors made of other

materials as well. For example, there has been intense research activity in the area of two dimensional materials such as graphene and MoS_2. These materials are promising for electronics and optoelectronics applications because they are flexible and come in a variety of bandgaps [189–191]. Even though photodetectors have been demonstrated using these materials, their optical absorption is small because they are just one atomic layer thin. We believe that integrating these materials into multiple gate structures proposed in chapter 3 will result in gain producing geometries that can improve the photo-response.

3. **Use of sub 5nm Nanowires:** This thesis considered large cross sectional area nanowires. In chapter 2 we concluded that even nanowire arrays (without multiple gates) are not of much advantage when compared to bulk SOI devices. However, studies have shown that nanowires with diameters smaller than $5nm$ provide an increased optical absorption due to a fundamental change in the electronic band-structure [192]. Arrays of such nanowires might provide an opportunity to go beyond the advances proposed in this thesis in designing optoelectronic devices including photodetectors.

4. **Photodetector with Nanowire Bridges:** In chapter 3, section 3.2.1, we discussed about the superior performance of junction-less photodetectors with nanowires that connect the thicker sections of active region. Similar structures have been fabricated by a combination of top-down and bottom-up techniques [193–195]. Here we suggest a method to fabricate the structure by top-down approach only. Shown in figure 7.1 is the three dimensional view of the structure. The two nanowires, NW_1 and NW_2 are not suspended. They are located over the buried oxide layer, connecting the thick parts of the active region together.

The fabrication process of this device is very similar to what discussed in chapter 4, except for the fabrication of the active region. One can fabricate the active region in two steps. In the first step the thick areas can be patterned and partly etched. The etching process should stop at a thickness equal to the thickness (height) of nanowires. The rest of the active region (including the nanowires) will be patterned and etched in an electron beam lithography and etch step. Since the second patterning step is over a non-planar surface, techniques that use evaporated resists are recommended in order to achieve small feature sizes [196].

This strategy allows for using SOI wafers with a thick top silicon layer which would increase the quantum efficiency of the phototransistor. At the same time, the device is expected to have a good ON/OFF ratio, as the thin wires allow for total depletion of the channel.
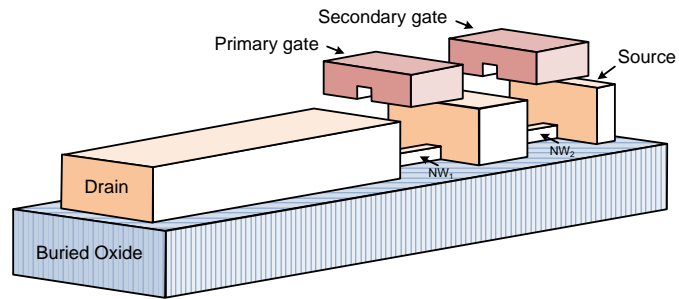
Figure 7.1: Junction-less phototransistor with multiple gates, and nanowires that bridge the thick sections of active region. The gates are lifted up to show NW_1 and NW_2.

APPENDICES

Appendix A

Analytical Approach for Lateral Bipolar Action in Phototransistors

Even in a simple two-dimensional MOS photodetector, including the effect of the gate electric field requires solving two dimensional Poisson's and carrier continuity equations. Since the goal of this section is to give an insight on the behaviour of the device, the current in a simpler one-dimensional structure is derived. For more complicated structures, the commercially available simulators can always obtain more accurate numerical results. The closest simple one-dimensional structure to an n-channel SOI MOS detector, biased in lateral bipolar mode, is of course an npn bipolar transistor, shown in figure A.1. Since in an ideal MOS transistor the gate current is zero, the same condition will be assumed for the bipolar transistor; e.g. the transistor base is considered as a float contact. The base is then illuminated by a uniform light source, through a window that covers the emitter and collector sections from illumination, and generates G_L electron-hole pairs per unit volume, per unit time in the base region only. The emitter and the collector are connected to DC voltages of V_C and V_E. In order to obtain the current, the carrier continuity equations must be solved for collector-base (CB) and emitter-base (EB) junctions. A series of basic assumptions are usually made to simplify the equations. The assumptions are [40]:

- The device regions are non-degenerate, and uniformly doped. The junctions are then abrupt.

- Low level injection is assumed in the quasi-neutral regions.

- No process other than drift, diffusion, and thermal generation-recombination takes place inside the transistor. Moreover, $G_L = 0$ for emitter and collector regions, but not for the base region.
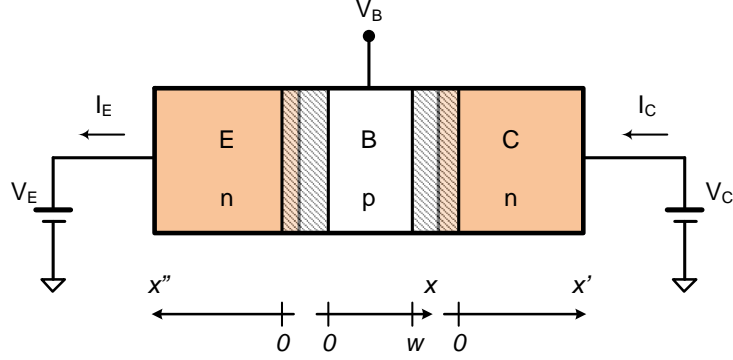
Figure A.1: An *npn* bipolar transistor with a floating base.

- The thermal generation-recombination is negligible throughout the CB and EB depletion regions.

- The contacts are considered Ohmic.

The assumptions lead to a simplified version of the continuity equation that holds for the minority carrier concentration of each region. For emitter quasi-neutral region, under steady state conditions the equation is as follows:

$$\frac{\partial \Delta p_E}{\partial t} = D_E \frac{d^2 \Delta p_E}{dx"^2} - \frac{\Delta p_E}{\tau_E} = 0 \tag{A.1}$$

ΔP_E in equation A.1 is the difference between the initial and the steady state minority carrier concentration (holes) in emitter quasi neutral region. D_E and τ_E are the diffusion coefficient and the minority carrier life time, respectively. Two boundary conditions are required to obtain a unique solution. The first boundary condition is:

$$\Delta p_E(x" = 0) = \frac{n_i^2}{N_E} \left(e^{\frac{qV_{BE}}{k_B T}} - 1 \right) \equiv p_{E0} \left(e^{\frac{qV_{BE}}{k_B T}} - 1 \right) \tag{A.2}$$

V_{BE} is the potential difference between the base and the emitter; N_E is the doping concentration in the emitter, and n_i is the intrinsic carrier concentration. Finally T is the operating temperature and k_B is the Boltzmann constant. The second boundary condition is:

$$\Delta p_E \left(x" = w_E \right) = 0 \tag{A.3}$$

where w_E is the length of emitter quasi neutral region. This condition is a result of the fifth assumption; at an ohmic contact, the minority carrier concentration is maintained near its equilibrium value due to the high recombination rate [40]. The solution of the differential equation A.1 would then be

$$\Delta p_E(x") = p_{E0} \left(e^{\frac{qV_{BE}}{k_BT}} - 1 \right) \left[\left(\frac{-e^{\frac{2w_E}{L_E}}}{1 - e^{\frac{2w_E}{L_E}}} \right) e^{\frac{-x"}{L_E}} + \left(\frac{1}{1 - e^{\frac{2w_E}{L_E}}} \right) e^{\frac{x"}{L_E}} \right] \tag{A.4}$$

In equation A.4, $L_E = \sqrt{D_E\tau_E}$ is the diffusion length in the emitter quasi-neutral region. The same approach can be followed to calculate the minority carrier concentration in the collector region. Assuming that w_C is the length of collector quasi-neutral region, $L_C = \sqrt{D_C\tau_C}$ is the diffusion length, V_{BC} is the base-collector voltage, and $p_{C0} = \frac{n_i^2}{N_C}$ (N_C is the collector doping), one will find:

$$\Delta p_C(x') = p_{C0} \left(e^{\frac{qV_{BC}}{k_BT}} - 1 \right) \left[\left(\frac{-e^{\frac{2w_C}{L_C}}}{1 - e^{\frac{2w_C}{L_C}}} \right) e^{\frac{-x'}{L_C}} + \left(\frac{1}{1 - e^{\frac{2w_C}{L_C}}} \right) e^{\frac{x'}{L_C}} \right] \tag{A.5}$$

Calculating the minority carrier concentration for the base region requires including the carrier generation due to light. The boundary conditions would also be slightly different from those of emitter and collector regions. Assuming that the base doping is P_B, and the quasi-neutral length for the base is represented by w, the steady state minority carrier equation and the boundary conditions can be written as:

$$\frac{\partial \Delta n_B}{\partial t} = D_B \frac{d^2\Delta n_B}{dx^2} - \frac{\Delta n_B}{\tau_B} + G_L = 0 \tag{A.6}$$

$$\Delta n_B(x = 0) = \frac{n_i^2}{P_B} \left(e^{\frac{qV_{BE}}{k_BT}} - 1 \right) + G_L\tau_B \equiv n_{B0} \left(e^{\frac{qV_{BE}}{k_BT}} - 1 \right) + G_L\tau_B \tag{A.7}$$

$$\Delta n_B(x = w) = \frac{n_i^2}{P_B} \left(e^{\frac{qV_{BC}}{k_BT}} - 1 \right) + G_L\tau_B \equiv n_{B0} \left(e^{\frac{qV_{BC}}{k_BT}} - 1 \right) + G_L\tau_B \tag{A.8}$$

Equation A.6 has a solution in the form of $y(x) = A exp(\frac{-x}{L_B}) + B exp(\frac{x}{L_B}) + G_L\tau_B$, where $L_B = \sqrt{D_B\tau_B}$ is the diffusion length at the base region. Applying the boundary conditions would result in an analytical equation for base.

$$\Delta n_B(x) = \left[n_{B0} \left(e^{\frac{qV_{BE}}{k_B T}} - 1 \right) - G_L \tau_B \right] \frac{sinh\left(\frac{w-x}{L_B} \right)}{sinh\left(\frac{w}{L_B} \right)}$$

$$+ \left[n_{B0} \left(e^{\frac{qV_{BC}}{k_B T}} - 1 \right) - G_L \tau_B \right] \frac{sinh\left(\frac{x}{L_B} \right)}{sinh\left(\frac{w}{L_B} \right)} \tag{A.9}$$

$$+ G_L \tau_B$$

Once $\Delta p_{C(E)}$ and Δn_B are obtained, the electron and hole current components flowing across the EB and CB junctions can be readily derived. The current is composed of two components, due to electron and hole movements that are either the minority or majority carrier currents depending on the doping type of each region. The majority carrier current component in each region cannot be calculated directly. However there is a shortcut to find the majority carrier concentration right at the junction edge. Since the depletion region is assumed to have no generation or recombination, the current that passes through is constant. As a result, if the minority carrier current is known at the edges of the depletion region, it is known throughout the depletion region and at the contacts. Therefore the total current through each junction is the sum of the two minority current densities at edge of depletion region, multiplied by the cross sectional area of the junction. The current density for each carrier is due to both carrier drift and diffusion taking place inside the semiconductor. For the minority carriers however the electric field at the quasi neutral regions is negligible; and thus the minority carrier current density would have a diffusion component only. The emitter and the collector currents would then be:

$$I_C = I_{Cp} + I_{Cn}$$

$$= qA \left[-D_C \frac{d\Delta p_C}{dx'} |_{x'=0} + D_B \frac{d\Delta n_B}{dx} |_{x=w} \right]$$

$$= qA \left[\frac{D_C}{L_C} p_{C0} \left(e^{\frac{qV_{BC}}{k_B T}} - 1 \right) coth \left(\frac{2w_C}{L_C} \right) \right.$$

$$- \frac{D_B}{L_B} \left[n_{B0} \left(e^{\frac{qV_{BE}}{k_B T}} - 1 \right) - G_L \tau_B \right] \frac{1}{sinh\left(\frac{w}{L_B} \right)} \tag{A.10}$$

$$+ \left. \frac{D_B}{L_B} \left[n_{B0} \left(e^{\frac{qV_{BC}}{k_B T}} - 1 \right) - G_L \tau_B \right] \frac{cosh\left(\frac{w}{L_B} \right)}{sinh\left(\frac{w}{L_B} \right)} \right]$$

$$I_E = I_{Ep} + I_{En}$$

$$= qA \left[D_E \frac{d\Delta p_E}{dx"} \big|_{x"=0} + D_B \frac{d\Delta n_B}{dx} \big|_{x=0} \right]$$

$$= qA \left[-\frac{D_E}{L_E} p_{E0} \left(e^{\frac{qV_{BE}}{k_B T}} - 1 \right) \coth \left(\frac{2w_E}{L_E} \right) \right.$$

$$- \frac{D_B}{L_B} \left[n_{B0} \left(e^{\frac{qV_{BE}}{k_B T}} - 1 \right) - G_L \tau_B \right] \frac{\cosh \left(\frac{w}{L_B} \right)}{\sinh \left(\frac{w}{L_B} \right)}$$

$$\left. + \frac{D_B}{L_B} \left[n_{B0} \left(e^{\frac{qV_{BC}}{k_B T}} - 1 \right) - G_L \tau_B \right] \frac{1}{\sinh \left(\frac{w}{L_B} \right)} \right] \quad \text{(A.11)}$$

All of the parameters in equations A.10 and A.11 are known except the base voltage, since it is left float. The floating base leads to a zero base current; therefore $I_C = I_E$. Incorporating this assumption with equations A.10 and A.11 will easily result in a formula for V_B (note: $V_{BC} = V_B - V_C, V_{BE} = V_B - V_E$ and let $V_E = 0$).

$$V_B = \frac{k_B T}{q} \ln \left[\frac{\frac{D_E}{L_E} p_{E0} \coth \left(\frac{2w_E}{L_E} \right) + \frac{D_C}{L_C} p_{C0} \coth \left(\frac{2w_C}{L_C} \right) + 2 \frac{D_B}{L_B} \left(n_{B0} + G_L \tau_B \right) \frac{\cosh \left(\frac{w}{L_B} \right) - 1}{\sinh \left(\frac{w}{L_B} \right)}}{\frac{D_E}{L_E} p_{E0} \coth \left(\frac{2w_E}{L_E} \right) + \frac{D_C}{L_C} p_{C0} e^{\frac{-qV_C}{k_B T}} \coth \left(\frac{2w_C}{L_C} \right) + \frac{D_B}{L_B} n_{B0} \left(1 + e^{\frac{-qV_C}{k_B T}} \right) \frac{\cosh \left(\frac{w}{L_B} \right) - 1}{\sinh \left(\frac{w}{L_B} \right)}} \right]$$

$$\text{(A.12)}$$

Appendix B

Noise Calculation

The sources of noise and figures of merit of photo-detectors were introduced in chapter 1. What is explained here is how to calculate each source of noise for the special case of a phototransistor. We have considered three sources of noise, in calculating the total noise. The first noise source is the shot noise due to the fluctuations of the carriers in the channel, as well the fluctuations of the incoming photons. The next source of the noise is the shot noise at the output, due to the fluctuations in the current at the output. Finally, the third source of noise is the thermal noise generated in the device as the current passes through. We have not included the Flicker noise, as some of the required parameters are experimental. Thermal noise due to the load resistance R_L is not included either. Such noise would be dominant at room temperature when the illumination intensity is low (unless R_L is infinitely large), and under such circumstance it would not be possible to study and compare the performance of the phototransistors.

The spectral density of the shot noise at the input of the phototransistor, due to the fluctuations of the carriers in the channel and also due to the incoming photons, is:

$$\frac{< I^2_{sh_{in}} >}{\Delta f} = 2[2q(I_\phi + I_{elec})] \tag{B.1}$$

Here q is the electron charge, and I_ϕ and I_{elec} are the primary photocurrent, and the electrical bias current, respectively. Since the base-emitter junction and the base-collector junction are correlated, the pre-factor 2 is added to equation [197]. The primary photocurrent I_ϕ is determined by finding out how many of the striking photons have generated electron-hole pairs after all. Out of N_{ph} striking photons per unit time, some will reflect back at the surface. As a result, assuming R is the surface reflection, the ratio of photons that will be transmitted through the semiconductor is $T = 1 - R$. In addition, depending on the thickness of the semiconductor, some photons may

not be absorbed at all. The attenuation due to semiconductor thickness is $1 - e^{-\alpha D}$; where D is the semiconductor thickness, and α is the absorption coefficient at the wavelength of interest. The last parameter that we should consider is the conversion efficiency of the semiconductor, or the percentage of conversion of the absorbed photons to carriers (η_{conv}). The primary photocurrent I_ϕ is then:

$$I_\phi = q(1 - R)(1 - e^{-\alpha D})\eta_{cov}N_{ph} \qquad (B.2)$$

For simplicity we assume that the conversion efficiency η_{conv} is 1. We also simplify the photon rate in terms of optical power P_{opt} and photon energy $h\nu$ (h: Planck constant, ν: photon frequency).

$$I_\phi = q(1 - R)(1 - e^{-\alpha D})\frac{P_{opt}}{h\nu} \qquad (B.3)$$

The electrical bias current, I_{elec}, in a bipolar transistor is a combination of bulk and surface leakage currents, that result in the dark current at the output [197]. In addition, we should include the gate leakage current in I_{elec} since the structure in our study is a MOS transistor. However, for simplicity we assume that the surface leakage current and the gate leakage current are both negligible. Since we access the dark current at the output, we calculate I_{elec} as:

$$I_{elec} = \frac{I_{out(dark)}}{g_{opt}} \qquad (B.4)$$

g_{opt} is the dynamic optical gain [197]; but we have replaced it with the static optical gain (optical gain at DC) to further simplify the equation.

$$g_{opt} = \frac{I_{out(optical)}}{I_\phi} = \frac{I_{out(illumination)} - I_{out(dark)}}{I_\phi} \qquad (B.5)$$

The next source of the noise is the shot noise at the output. The spectral density of this noise is:

$$\frac{< I^2_{sh_{out}} >}{\Delta f} = 2q(I_{out}) \qquad (B.6)$$

In equation B.6 I_{out} is the current at the output of the structure, which is composed of both dark current and photocurrent.

The last source of noise that we considered is the thermal noise generated in the device as the current passes through.

$$\frac{< I_{th}^2 >}{\Delta f} = \frac{4k_B T}{R} \tag{B.7}$$

Here k_B is the Boltzmann constant, T is the operating temperature, and R is the dynamic resistance the current sees as it is passing through the device, when the voltage or current fluctuates by a small value. For junction-less transistors, since the drain current versus drain voltage is somewhat linear, for simplicity we have assumed that the dynamic resistance is equal to the static resistance. The static resistance is obtained by dividing the bias voltage to the current, or $\frac{V}{I}$. We applied the current-voltage linearity assumption for the case of junction transistors as well. However, since over here there are two distinct doped areas for source and drain, we subtracted the resistance of these two regions out of the total resistance obtained from $\frac{V}{I}$. We calculated the resistance of the highly doped source and drain regions by the static formula of $\rho \frac{l}{A}$, where ρ, l and A are the resistivity, length and area of the source or drain regions, respectively.

Assuming that the noise sources are not correlated, the total noise at the output can be simply obtained by summing up the three noises. Since it is intended to obtain the noise at the output, the term $|g_{opt}|^2$ should be multiplied to the input shot noise in order to link it to the output [197].

$$< I_n^2 >= |g_{opt}|^2 < I_{sh_{in}}^2 > + < I_{sh_{out}}^2 > + < I_{th}^2 > \tag{B.8}$$

Bibliography

[1] J. Singh, *Semiconductor Optoelectronics: Physics and technology.* New York: McGraw-Hill, Inc., 1995. 1, 2, 3, 5, 6, 9, 10, 11, 12, 13, 14, 15, 17, 18

[2] P.-Y. Chan and J. Enderle, "Automatic door opener," in *Bioengineering Conference, 2000. Proceedings of the IEEE 26th Annual Northeast*, pp. 139–140, 2000. 1

[3] R. G. Beals, "Fully automatic garage door opener," June 1989. U.S. Patent 4843639. 1

[4] D. J. Carlson, "Television remote control system for selectively controlling a plurality of external apparatus," July 1983. U.S. Patent 4392022. 1

[5] K. Kato, S. Hata, K. Kawano, J. Yoshida, and A. Kozen, "A high efficiency 50GHz In-GaAs multimode waveguide photodetector," *IEEE Journal of Quantum Electronics*, vol. 28, pp. 2728–2735, December 1992. 1, 14

[6] K. Kato, A. Kozen, Y. Muramoto, Y. Itaya, T. Nagatsuma, and M. Yaita, "110GHz, 50%-efficiency mushroom-mesa waveguide p-i-n photodiode for a 1.55μm waveguide," *IEEE Photonics Technology Letters*, vol. 6, pp. 719–721, June 1994. 1

[7] A. Beling and J. C. Campbell, "InP-based high-speed photodetectors," *Journal of Lightwave Technology*, vol. 27, pp. 343–355, February 2009. 1

[8] S. Fedderwitz, A. Sthr, S. F. Yoon, K. H. Tan, M. Wei, W. K. Loke, A. Poloczek, S. Wicaksono, and D. Jger, "Multigigabit 1.3μm GaNAsSb/GaAs photodetectors," *Applied Physics Letters*, vol. 93, no. 3, 2008. 1

[9] F. Paresce, "Towards the ideal detector," *Nature*, vol. 381, pp. 115–115, May 1996. 1

[10] G. Rieke, "Infrared detector arrays for astronomy," *Annual Review of Astronomy and Astrophysics*, vol. 45, pp. 77–115, 2007. 1

[11] C. Stahle, B. Parker, A. Parsons, L. Barbier, S. Barthelmy, N. Gehrels, D. Palmer, S. Snodgrass, and J. Tueller, "CdZnTe and CdTe detector arrays for hard X-ray and gamma-ray astronomy," *Nuclear Instruments and Methods in Physics Research A*, vol. 436, pp. 138–145, October 1999. 1

[12] C. Barbieri, G. Naletto, T. Occhipinti, C. Facchinetti, E. Verroi, E. Giro, A. Di Paola, S. Billotta, P. Zoccarato, P. Bolli, *et al.*, "AquEYE, a single photon counting photometer for astronomy," *Journal of Modern Optics*, vol. 56, no. 2-3, pp. 261–272, 2009. 1

[13] E. J. Lerner, "Introduction to photodetectors and applications," *Laser Focus World*, December 2000. 1

[14] D. Litwiller, "CMOS vs. CCD: Maturing technologies, maturing markets," *Photonics Spectra*, pp. 54–59, August 2005. xii, 1, 6, 7

[15] A. D. Guerra, N. Belcari, M. G. Bisogni, G. L. S. Marcatili, and S. Moehrs, "Advances in position-sensitive photodetectors for PET applications," *Nuclear Instruments and Methods in Physics Research A*, vol. 604, pp. 319– 322, June 2009. 1

[16] J. Wilson and J. F. B. Hawkes, *Optoelectronics, an Introduction.* UK: Prentice Hall International, 2nd ed., 1989. xii, 1, 2, 4, 5, 7, 8, 9, 10, 11, 12

[17] N. Faramarzpour, M. El-Desouki, M. J. Deen, Q. Fang, S. Shirani, and L. Liu, "CMOS imaging for biomedical applications," *Potentials, IEEE*, vol. 27, no. 3, pp. 31–36, 2008. 2, 8

[18] K. Watase, "Photomultiplier tubes: μPMT is key to high-performance portable devices," *LaserFocusWorld*, May 2013. 2

[19] `http://park.chem.cornell.edu/research.htm`. [Online; accessed 02-June-2014]. 2

[20] `http://nanowires.berkeley.edu/`. [Online; accessed 02-June-2014]. 2

[21] `http://cml.harvard.edu/publicationposts/2014//`. [Online; accessed 02-June-2014]. 2

[22] B. P. Lathi, *Communication Systems.* New York: John Wiley and Sons, Inc., 1968. 3, 5

[23] E. Uiga, *Optoelectronics.* New Jersey: Prentice Hall, Inc., 1995. 5, 6

[24] D. Litwiller, "CCD vs. CMOS: Facts and fiction," *Photonics Spectra*, pp. 154– 158, January 2001. 6, 7, 8, 9

[25] E. R. Fossum, "CMOS image sensors: Electronic Camera-On-A-Chip," *IEEE Transactions on Electron Devices*, vol. 44, pp. 1689–1698, October 1997. 7

[26] M. Bigas, E. Cabruja, J. Forest, and J. Salvi, "Review of CMOS image sensors," *Microelectronics Journal*, vol. 37, pp. 433– 451, May 2006. 8

[27] P. Magnan, "Detection of visible photons in CCD and CMOS: A comparative view," *Nuclear Instruments and Methods in Physics Research Section A*, vol. 504, pp. 199– 212, May 2003. 8, 9

[28] P. A. Levine, "Blooming control for charge coupled imager," January 1976. U. S. Patent 3931465. 9

[29] J. S. Jie, W. J. Zhang, Y. Jiang, X. M. Meng, Y. Q. Li, and S. T. Lee, "Photoconductive characteristics of single-crystal CdS nanoribbons," *Nano Letters*, vol. 6, pp. 1887–1892, September 2006. 10

[30] N. E. Coates, H. Zhou, S. Krmer, L. Li, and D. Moses, "Solution-based in situ synthesis and fabrication of ultrasensitive CdSe photoconductors," *Advanced Materials*, vol. 22, p. 53665369, December 2010. 10

[31] T. S. Moss, "Lead salt photoconductors," in *Proc. IRE*, vol. 43, (Farnborough, England), pp. 1869–1881, December 1955. 10

[32] E. H. Putley, "Indium antimonide submillimeter photoconductive detectors," *Applied Optics*, vol. 4, pp. 649–657, June 1965. 11

[33] E. T. Young, "Review of low-background Ge photoconductors," in *Proc. SPIE 1874, Infrared and Millimeter-Wave Engineering*, vol. 1874, pp. 268–282, July 1993. 11

[34] C. Xu, C. Shen, W. Wu, and M. Chan, "Backside-illuminated lateral PIN photodiode for CMOS image sensor on SOS substrate," *IEEE Transactions on Electron Devices*, vol. 52, pp. 1110– 1115, June 2005. 13

[35] G. J. Gruber, W. S. Choong, W. W. Moses, S. E. Derenzo, S. E. Holland, M. Pedrali-Noy, B. Krieger, E. Mandelli, G. Meddeler, and N. W. Wang, "A compact 64-pixel CsI(Tl)/Si PIN photodiode imaging module with IC readout," *IEEE Transactions on Nuclear Science*, vol. 49, pp. 147–152, February 2002. 13

[36] B. E. Patt, J. S. Iwanczyk, C. R. Tull, N. W. Wang, M. P. Torani, and E. J. Hoffman, "High resolution CsI(TI)/ Si-PIN detector development for breast imaging," *IEEE Transactions on Nuclear Science*, vol. 45, pp. 2126– 2131, August 1998. 13

[37] V. P. Semynozhenko, B. Grinyov, V. V. Nekrasov, and Y. A. Borodenko, "Recent progress in the development of CsI(Tl) crystal-Si-photodiode spectrometric detection assemblies," *Nuclear Instruments and Methods in Physics Research A*, vol. 537, pp. 383– 388, January 2005. 13

[38] J. E. Bowers and C. Burrus, "High-speed zero-bias waveguide photodetectors," *Electronics Letters*, vol. 22, pp. 905– 906, August 1986. 14

[39] E. Bowers and C. A. B. Jr., "Ultrawide-band long-wavelength p-i-n photodetectors," *Journal of Lightwave Technology*, vol. LT-5, pp. 1339–1350, October 1987. 14

[40] R. F. Pierret, *Semiconductor Device Fundamentals*. Massachusetts: Addison-Wesley, 2nd ed., 1996. 14, 15, 17, 18, 25, 26, 58, 59, 60, 63, 64, 67, 83, 90, 91, 109, 114, 127, 129

[41] B. F. Aull, A. H. Loomis, D. J. Young, R. M. Heinrichs, B. J. Felton, P. J. Daniels, and D. J. Landers, "Geiger-mode avalanche photodiodes for three-dimensional imaging," *Lincoln Laboratory Journal*, vol. 13, no. 2, pp. 335–350, 2002. 14, 15

[42] P. Brard, C. M. Pepin, D. Rouleau, J. Cadorette, and R. Lecomte, "CT acquisition using PET detectors and electronics," *IEEE Transactions on Nuclear Science*, vol. 52, no. 3, pp. 634– 637, 2005. 15

[43] R. Grazioso, N. Zhang, J. Corbeil, M. Schmand, R. Ladebeck, M. Vester, G. Schnur, W. Renz, and H. Fischer, "APD-based PET detector for simultaneous PET/MR imaging," *Nuclear Instruments and Methods in Physics Research A*, vol. 569, pp. 301– 305, December 2006. 15

[44] B. J. Pichler, M. S. Judenhofer, C. Catana, J. H. Walton, M. Kneilling, R. E. Nutt, S. B. Siegel, C. D. Claussen, and S. R. Cherry, "Performance test of an LSO-APD detector in a 7-T MRI scanner for simultaneous PET/MRI," *The Journal of Nuclear Medicine*, vol. 47, pp. 639– 647, April 2006. 15

[45] M. Azadeh, *Fiber Optics Engineering*. Springer Verlag, 2nd ed., 2009. 15

[46] R. McIntyre, "Multiplication noise in uniform avalanche diodes," *IEEE Transactions on Electron Devices*, vol. 13, no. 1, pp. 164–168, 1966. 16

[47] B. K. Ng, J. P. R. David, R. C. Tozer, M. Hopkinson, G. Hill, and G. J. Rees, "Excess noise characteristics of $Al_{0.8}Ga_{0.2}As$ avalanche photodiodes," *IEEE Photonics Technology Letters*, vol. 14, pp. 522–524, April 2002. 16

[48] X. G. Zheng, X. Sun, S. Wang, P. Yuan, G. S. Kinsey, A. L. Holmes, B. G. Streetman, and J. C. Campbell, "Multiplication noise of $Al_xGa_{1-x}As$ avalanche photodiodes with high Al concentration and thin multiplication region," *Applied Physics Letters*, vol. 78, pp. 3833–3835, June 2001. 16

[49] J. Katz, "Detectors for optical communications: A review," *Telecommunications and Data Acquisition Progress Report*, pp. 21–38, July-September 1983. 16

[50] J. D. Beck, C. F. Wan, M. A. Kinch, and J. E. Robinson, "MWIR HgCdTe avalanche photodiodes," in *Proc. SPIE, Materials for Infrared Detectors*, p. 188197, 2001. 16

[51] C. H. Tan, J. C. Clark, J. P. R. David, G. J. Rees, S. A. Plimmer, R. C. Tozer, D. C. Herbert, D. J. Robbins, W. Y. Leong, and J. Newey, "Avalanche noise measurement in thin Si p^+-in^+ diodes," *Applied Physics Letters*, vol. 76, pp. 3926–3928, June 2000. 16

[52] P. Yuan, C. C. Hansing, K. A. Anselm, C. V. Lenox, H. Nie, A. L. Holmes, B. G. Streetman, and J. C. Campbell, "Impact ionization characteristics of III-V semiconductors for a wide range of multiplication region thicknesses," *IEEE Journal of Quantum Electronics*, vol. 36, pp. 198–204, February 2000. 16

[53] J. C. Campbell, "Recent advances in telecommunications avalanche photodiodes," *Journal of Lightwave Technology*, vol. 25, pp. 109–121, January 2007. 16

[54] M. M. Hayat, B. E. A. Saleh, and M. C. Teich, "Effect of dead space on gain and noise in Si and GaAs avalanche photodiodes," *IEEE Journal of Quantum Electronics*, vol. 28, p. 13601365, May 1992. 16

[55] J. C. Campbell, S. Demiguel, F. Ma, A. Beck, X. Guo, S. Wang, X. Zheng, X. Li, J. D. Beck, M. A. Kinch, A. Huntington, L. A. Coldren, J. Decobert, and N. Tscherptner, "Recent advances in avalanche photodiodes," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 10, pp. 777–787, July-August 2004. 16

[56] P. Yuan, S. Wang, X. Sun, X. G. Zheng, A. L. Holmes, and J. C. Campbell, "Avalanche photodiodes with an impact-ionization-engineered multiplication region," *IEEE Photonics Technology Letters*, vol. 12, pp. 1370–1372, October 2000. 16

[57] S. Wang, F. Ma, X. Li, R. Sidhu, X. Zheng, X. Sun, A. L. Holmes, and J. C. Campbell, "Ultra-low noise avalanche photodiodes with a centered-well multiplication region," *IEEE Journal of Quantum Electronics*, vol. 39, pp. 375–378, February 2003. 16

[58] W. P. Dumke, J. M. Woodall, and V. L. Rideout, "GaAs-GaAlAs heterojunction transistor for high frequency operation," *Solid-state Electronics*, vol. 15, pp. 1339– 1343, 1972. 18

[59] J. C. Campbell, A. G. Dentai, C. A. Burrus, and J. F. Ferguson, "High sensitivity InP/InGaAs heterojunction phototransistor," *Electronics Letters*, vol. 16, pp. 713– 714, August 1980. 18

[60] J. C. Campbell, A. G. Dentai, C. A. Burrus Jr, and J. Ferguson, "InP/InGaAs heterojunction phototransistors," *Quantum Electronics, IEEE Journal of*, vol. 17, no. 2, pp. 264–269, 1981. 18

[61] Z. Pei, C. Liang, L. Lai, Y. Tseng, Y. Hsu, P. Chen, S. Lu, C. Liu, M.-J. Tsai, and C. Liu, "High efficient 850nm and 1310nm multiple quantum well SiGe/Si heterojunction phototransistors with 1.25 plus GHz bandwidth (850nm)," in *Electron Devices Meeting, 2002. IEDM'02. International*, pp. 297–300, IEEE, 2002. 18

[62] P. D. Wright, R. J. Nelson, and T. Cella, "High-gain InGaAsP-InP heterojunction phototransistors," *Applied Physics Letters*, vol. 37, pp. 192–194, July 1980. 18

[63] M. N. Abedin, T. F. Refaat, O. V. Sulima, and U. N. Singh, "AlGaAsSb-InGaAsSb HPTs with high optical gain and wide dynamic range," *IEEE Transactions on Electron Devices*, vol. 51, pp. 2013– 2018, December 2004. 18

[64] Y. W. Chang, Y. T. Tai, Y. T. Huang, and Y. S. Yang, "A CMOS- based phototransistor for high- sensitivity biochemical detection using absorption photometry," in *3rd International Conference on Sensing Technology*, pp. 82–85, 2008. 18

[65] Y. W. Chang and Y. T. Huang, "The ring-shaped CMOS-based phototransistor with high responsivity for the UV/blue spectral range," *IEEE Photonics Technology Letters*, vol. 21, pp. 899– 901, July 2009. 18

[66] H. Shao, W. Li, A. Torfi, D. Moscicka, and W. I. Wang, "Room-temperature p-n-p AlGaAsSb-InGaAsSb heterojunction phototransistors with cut-off wavelength at $2.5\mu m$," *IEEE Photonics Technology Letters*, vol. 18, pp. 2326– 2328, November 2006. 18

[67] Y. Wang, E. S. Yang, and W. I. Wang, "High gain and wide dynamic range punchthrough heterojunction phototransistors," *Journal of Applied Physics*, vol. 74, p. 69786981, December 1993. 18

[68] R. Sridhara, S. M. Frimel, K. P. Roenker, N. Pan, and J. Elliott, "Performance enhancement of GaInP/GaAs heterojunction bipolar phototransistors using DC base bias," *Journal of Lightwave Technology*, vol. 16, pp. 1101– 1106, June 1998. 18

[69] H. Luo, Y. Chang, K. S. Wang, and Y. Wang, "Ultrasensitive Si phototransistors with a punchthrough base," *Applied Physics Letters*, vol. 79, p. 773775, August 2001. 18

[70] X. Liu, S. Guo, C. Zou, G. Du, Y. Wang, and Y. Chang, "Punchthrough enhanced phototransistor fabricated in standard CMOS process," *IEEE Electron Device Letters*, vol. 30, pp. 272– 274, March 2009. 18

[71] L. T. Canham, "Silicon quantum wire array fabrication by electrochemical and chemical dissolution of wafers," *Applied Physics Letters*, vol. 57, pp. 1046– 1048, September 1990. 19

[72] J. D. Holmes, K. P. Johnston, R. C. Doty, and B. A. Korgel, "Control of thickness and orientation of solution-grown silicon nanowires," *Science*, vol. 287, pp. 1471– 1473, February 2000. 19, 20

[73] D. Shiri, Y. Kong, A. Buin, and M. P. Anantram, "Strain induced change of bandgap and effective mass in silicon nanowires," *Applied Physics Letters*, vol. 93, p. 073114, August 2008. 19

[74] X. B. Yang and R. Q. Zhang, "Indirect-to-direct bandgap transitions in phosphorus adsorbed <112> silicon nanowires," *Applied Physics Letters*, vol. 93, p. 173108, October 2008. 19

[75] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, "Ballistic carbon nanotube field-effect transistors," *Nature*, vol. 424, pp. 654– 657, August 2003. 19

[76] H. Ishikuro, T. Fujii, T. Saraya, G. Hashiguchi, T. Hiramoto, and T. Ikoma, "Coulomb blockade oscillations at room temperature in a Si quantum wire metal-oxide-semiconductor field-effect transistor fabricated by anisotropic etching on a silicon-on-insulator substrate," *Applied Physics Letters*, vol. 68, pp. 3585– 3587, June 1996. 19

[77] Z. Li, Y. Chen, X. Li, T. I. Kamins, K. Nauka, and R. S. Williams, "Sequence-specific label-free DNA sensors based on silicon nanowires," *Nano Letters*, vol. 4, pp. 245– 247, February 2004. 19

[78] S. M. Koo, Q. Li, M. D. Edelstein, C. A. Richter, and E. M. Vogel, "Enhanced channel modulation in dual-gated silicon nanowire transistors," *Nano Letters*, vol. 5, pp. 2519– 2523, December 2005. 19

[79] A. Agarwal, K. Buddharaju, I. Lao, N. Singh, N. Balasubramanian, and D. Kwong, "Silicon nanowire sensor array using top-down CMOS technology," *Sensors and Actuators A*, vol. 145-146, pp. 207– 213, July-August 2008. 19

[80] J. Wan, S. R. Deng, R. Yang, Z. Shu, B. R. Lu, S. Q. Xie, Y. Chen, E. Huq, R. Liu, and X. P. Qu, "Silicon nanowire sensor for gas detection fabricated by nanoimprint on SU8/SiO2/PMMA trilayer," *Microelectronic Engineering*, vol. 86, pp. 1238– 1242, April 2009. 19

[81] A. Zhang, C. Soci, B. Xiang, J. Park, D. Wang, and Y. H. Lo, "High gain ZnO nanowire phototransistor," in *Conference on Lasers and Electro-Optics/Quantum Electronics and Laser Science Conference and Photonic Applications Systems Technologies*, 2007. paper CMY2. 19, 20, 50

[82] A. Zhang, S. You, C. Soci, Y. Liu, D. Wang, and Y. H. Lo, "Silicon nanowire detectors showing phototransistive gain," *Applied Physics Letters*, vol. 93, p. 121110, September 2008. 19, 20, 34, 50

[83] R. Agarwal and C. M. Lieber, "Semiconductor nanowires: Optics and optoelectronics," *Applied Physics A, Material Science and Processing*, vol. 85, pp. 209–215, November 2006. 19, 70

[84] J. Wang, M. S. Gudiksen, X. Duan, Y. Cui, and C. M. Lieber, "Highly polarized photoluminescence and photodetection from single indium phosphide nanowires," *Science*, vol. 293, pp. 1455–1457, August 2001. 19

[85] Z. Fan, P. Chang, J. G. Lu, E. C. Walter, R. M. P. C. Lin, and H. P. Lee, "Photoluminescence and polarized photodetection of single ZnO nanowires," *Applied Physics Letters*, vol. 85, pp. 6128– 6130, December 2004. 19

[86] S. Han, W. Jin, D. Zhang, T. Tang, C. Li, X. Liu, Z. Liu, B. Lei, and C. Zhou, "Photoconduction studies on GaN nanowire transistors under UV and polarized UV illumination," *Chemical Physics Letters*, vol. 389, pp. 176– 180, May 2004. 19, 20, 50

[87] M. Freitag, Y. Martin, J. A. Misewich, R. Martel, and P. Avouris, "Photoconductivity of single carbon nanotubes," *Nano Letters*, vol. 3, pp. 1067– 1071, August 2003. 19

[88] K. H. Kim, K. Keem, D. Y. Jeong, B. Min, K. Cho, H. Kim, B. M. Moon, T. Noh, J. Park, M. Suh, and S. Kim, "Photocurrent of undoped, n- and p-type Si nanowires synthesized by thermal chemical vapor deposition," *Japanese Journal of Applied Physics*, vol. 45, pp. 4265–4269, May 2006. 20, 50

[89] Z. Guo, D. Zhao, Y. Liu, D. Shen, J. Zhang, and B. Li, "Visible and ultraviolet light alternative photodetector based on ZnO nanowire/n-Si heterojunction," *Applied Physics Letters*, vol. 93, p. 163501, 2008. 20

[90] O. Hayden, R. Agarwal, and C. M. Lieber, "Nanoscale avalanche photodiodes for highly sensitive and spatially resolved photon detection," *Nature Materials*, vol. 5, pp. 352– 356, May 2006. 20

[91] E. Lee, D. I. Moon, J. Yang, K. S. Lim, and Y. K. Choi, "Transparent zinc oxide gate metal-oxide-semiconductor field-effect transistor for high-responsivity photodetector," *IEEE Electron Device Letters*, vol. 30, pp. 493–495, May 2009. 20, 50

[92] H. G. Choi, Y. S. Choi, Y. C. Jo, , and H. Kim, "A low-power silicon-on-insulator photodetector with a nanometer-scale wire for highly integrated circuit," *Japanese Journal of Applied Physics*, vol. 43, pp. 3916–3918, June 2004. 20, 76

[93] J. H. Park, S. H. Seo, I. S. Wang, H. J. Yoon, J. K. Shin, P. Choi, Y. C. Jo, and H. Kim, "Active pixel sensor using a 1×16 nano-wire photodetector array for complementary metal oxide semiconductor imagers," *Japanese Journal of Applied Physics*, vol. 43, pp. 2050–2053, April 2004. 20, 76

[94] "Atlas Device Simulation Framework." `http://www.silvaco.com/products/tcad/device_simulation/atlas/atlas.html`. [Online; accessed 14-January-2014]. 21, 26, 27, 98

[95] A. Fadavi Roudsari, S. S. Saini, O. Nixon, and M. Anantram, "High-gain multiple-gate photodetector with nanowires in the channel," *IEEE Electron Device Letters*, vol. 32, no. 3, pp. 357–359, 2011. 23

[96] A. Fadavi Roudsari, G. Li, S. Saini, N. O, and M. P. Anantram, "Highly sensitive, silicon-on-insulator nanowire based photodetector: Device optimization and analysis," in *Nanotechnology (IEEE-NANO), 2011 11th IEEE Conference on*, pp. 873–876, Aug 2011. 23

[97] A. Fadavi Roudsari, , S. S. Saini, N. O, and M. P. Anantram, "High gain, silicon-on-insulator photodetector with multiple gates and a nanowire based narrow-wide-narrow channel," in

Symposium AA Group IV Semiconductor Nanostructures and Applications, vol. 1305 of *MRS Proceedings*, 1 2011. 23

[98] H. Yamamoto, K. Taniguchi, and C. Hamaguchi, "High-sensitivity SOI MOS photodetector with self-amplification," *Japanese Journal of Applied Physics*, vol. 35, no. 2B, pp. 1382–1386, 1996. 24, 50, 51

[99] J. Bae, a. X. M. Z. H. Kim, C. H. Dang, Y. Zhang, Y. J. Choi, A. Nurmikko, and Z. L. Wang, "Si nanowire metal-insulator-semiconductor photodetectors as efficient light harvesters," *Nanotechnology*, vol. 21, p. 095502, 2010. 34

[100] J. Wallentin, N. Anttu, D. Asoli, M. Huffman, I. Åberg, M. H. Magnusson, G. Siefer, P. Fuss-Kailuweit, F. Dimroth, B. Witzigmann, *et al.*, "InP nanowire array solar cells achieving 13.8% efficiency by exceeding the ray optics limit," *Science*, vol. 339, no. 6123, pp. 1057–1060, 2013. 34

[101] W. Kim and K. S. Chu, "ZnO nanowire field-effect transistor as a UV photodetector; optimization for maximum sensitivity," *Physica Status Solidi A*, vol. 206, no. 1, pp. 179–182, 2009. 50

[102] G. Cheng, X. Wu, B. Liu, B. Li, X. Zhang, and Z. Du, "ZnO nanowire Schottky barrier ultraviolet photodetector with high sensitivity and fast recovery speed," *Applied Physics Letters*, vol. 99, p. 203105, 2011. 50

[103] G. Cheng, X. Wu, B. Liu, B. Li, X. Zhang, and Z. Du, "Efficient visible light detection using individual germanium nanowire field effect transistors," *Applied Physics Letters*, vol. 91, p. 162102, 2007. 50

[104] K. S. Shin, A. Pan, and C. O. Chui, "Channel length dependent sensitivity of schottky contacted silicon nanowire field-effect transistor sensors," *Applied Physics Letters*, vol. 100, p. 123504, 2012. 50

[105] A. Kranti, R. Yan, C.-W. Lee, I. Ferain, R. Yu, N. D. Akhavan, P. Razavi, and J. P. Colinge, "Junctionless nanowire transistor (JNT): Properties and design guidelines," in *Solid-State Device Research Conference (ESSDERC), 2010 Proceedings of the European*, pp. 357–360, 2010. 50, 51, 53

[106] P. Servati, A. Colli, S. Hofmann, Y. Q. Fu, P. Beecher, Z. A. K. Durrani, A. C. Ferrari, A. J. Flewitt, J. Robertson, and W. I. Milne, "Scalable silicon nanowire photodetectors," *Physica. E, Low-Dimensional Systems & Nanostructures*, vol. 38, pp. 64–66, 4 2007. 53

[107] A. Fadavi Roudsari, S. S. Saini, N. O, and M. P. Anantram, "Junction-less phototransistor with nanowire channels, a modeling study," *Optics Express*, vol. 22, pp. 12573–12582, May 2014. 59

[108] M. Otto, M. Kroll, T. Käsebier, R. Salzer, A. Tünnermann, and R. B. Wehrspohn, "Extremely low surface recombination velocities in black silicon passivated by atomic layer deposition," *Applied Physics Letters*, vol. 100, no. 19, p. 191603, 2012. 65

[109] O. Demichel, V. Calvo, A. Besson, P. Noé, B. Salem, N. Pauc, F. Oehler, P. Gentile, and N. Magnea, "Surface recombination velocity measurements of efficiently passivated gold-catalyzed silicon nanowires by a new optical method," *Nano letters*, vol. 10, no. 7, pp. 2323–2329, 2010. 65

[110] R. Coustel, Q. Benoit a la Guillaume, V. Calvo, O. Renault, L. Dubois, F. Duclairoir, and N. Pauc, "Measurement of the surface recombination velocity in organically functionalized silicon nanostructures: The case of silicon on insulator," *The Journal of Physical Chemistry C*, vol. 115, no. 45, pp. 22265–22270, 2011. 65

[111] Y. Cui, L. J. Lauhon, M. S. Gudiksen, J. Wang, and C. M. Lieber, "Diameter-controlled synthesis of single-crystal silicon nanowires," *Applied Physics Letters*, vol. 78, pp. 2214–2216, April 2001. 70

[112] A. M. Morales and C. M. Lieber, "A laser ablation method for the synthesis of crystalline semiconductor nanowires," *Science*, vol. 279, pp. 208–211, January 1998. 70

[113] P. Gentile, T. David, F. Dhalluin, D. Buttard, N. Pauc, M. D. Hertog, P. Ferret, and T. Baron, "The growth of small diameter silicon nanowires to nanotrees," *Nanotechnology*, vol. 19, p. 125608, January 2008. 70

[114] O. Hayden, R. Agarwal, and W. Lu, "Semiconductor nanowire devices," *Nano Today*, vol. 3, pp. 12–22, October 2008. 70

[115] Y. Li, F. Qian, J. Xiang, and C. M. Lieber, "Nanowire electronic and optoelectronic devices," *Materials Today*, vol. 9, pp. 18–27, October 2006. 70

[116] W. Lu, P. Xie, and C. M. Lieber, "Nanowire transistor performance limits and applications," *IEEE Transactions on Electron Devices*, vol. 55, pp. 2859–2876, November 2008. 70

[117] Y. T. Cheng, Y. H. Cho, N. Takama, P. Lw, C. Bergaud, and B. J. Kim, "Simple fabrication of Si nanowire and its biological application," *Journal of Physics: Conference Series*, vol. 152, no. 1, p. 012048, 2009. 70

[118] "Soitec." `http://www.soitec.com/en/index.php`. [Online; accessed 19-April-2013]. 70

[119] R. Bower and R. Dill, "Insulated gate field effect transistors fabricated using the gate as source-drain mask," in *Electron Devices Meeting, 1966 International*, vol. 12, pp. 102–104, 1966. 72

[120] J. D. Plummer, M. D. Deal, and P. B. Griffin, *Silicon VLSI Technology: Fundamentals, Practice and Modeling.* New Jersey: Prentice Hall, Inc., 2000. 72, 73, 78, 79, 80, 82, 83

[121] "Microtec semiconductor process and device simulator." `http://www.siborg.ca/demos.html`. [Online; accessed 26-November-2013]. 72

[122] "Particle interactions with matter." `http://www.srim.org/`. [Online; accessed 26-November-2013]. 72, 74

[123] K. Williams, K. Gupta, and M. Wasilik, "Etch rates for micromachining processing-part II," *Microelectromechanical Systems, Journal of*, vol. 12, no. 6, pp. 761–778, 2003. 73, 79, 80

[124] "ZEP520A technical report." `http://www.zeonchemicals.com/pdfs/ZEP520A.pdf`. [Online; accessed 26-November-2013]. 74, 75

[125] "Photoresist adhesion." `http://www.yieldengineering.com/applications/photoresist-treatment/resist-adhesion`. [Online; accessed 26-April-2013]. 74, 85

[126] "MA/BA6 manual high precision mask & bond aligner." `http://www.suss.com/en/products-solutions/products/mask-aligner/maba6/overview.html`. [Online; accessed 26-November-2013]. 74

[127] "Inductively Coupled Plasma (ICP) etching." `http://www.oxford-instruments.com/products/etching-deposition-and-growth/plasma-etch-deposition/icp-etch`. [Online; accessed 26-November-2013]. 74

[128] "Microposit S1800$^{\circledR}$ series photo resists." `http://www.microchem.com/PDFs_Dow/S1800.pdf`. [Online; accessed 26-November-2013]. 75

[129] `http://www.coresystems.com/HOME.asp`. [Online; accessed 26-November-2013]. 76, 88

[130] "University of Washington - Washington Nanofabrication Facility." `https://www.wnf.washington.edu/`. [Online; accessed 27-November-2013]. 76, 88

[131] I. Wang, J. Park, S. Seo, Y. Shin, J. Shin, and M. Lee, "Quantum wire SOI MOSFET with sub-band effects using conventional photolithography and its application to photodetector," *The Journal of the Korean Physical Society*, vol. 45, no. 5, pp. 1347–1351, 2004. 76

[132] J. H. Park, H. Kim, I. S. Wang, and J. K. Shin, "Quantum-wired MOSFET photodetector fabricated by conventional photolithography on SOI substrate," in *4th IEEE Conference on Nanotechnology*, p. 425 427, 2004. 76

[133] H. Heidemeyer, C. Single, F. Zhou, F. Prins, D. Kern, and E. Plies, "Self limiting and pattern dependent oxidation of silicon dots fabricated on silicon on insulator material," *Journal of Applied Physics*, vol. 87, no. 9, pp. 4580–4585, 2000. 76

[134] "NANO^{TM} PMMA and Copolymer." `http://microchem.com/pdf/PMMA_Data_Sheet.pdf`. [Online; accessed 19-April-2013]. 76, 77, 78, 85

[135] K. Wilder, C. F. Quate, B. Singh, and D. F. Kyser, "Electron beam and scanning probe lithography: A comparison," *Journal of Vacuum Science & Technology B*, vol. 16, p. 3864, 1998. 76

[136] "NANO^{TM} Remover PG." `http://microchem.com/pdf/removerpg.pdf`. [Online; accessed 19-April-2013]. 78, 81

[137] M. Khorasaninejad, N. Abedzadeh, A. S. Jawanda, M. P. Anantram, and S. S. Saini, "Bunching characteristics of silicon nanowire arrays," *Journal of Applied Physics*, vol. 111, no. 4, pp. 044328–044328, 2012. 78, 79, 82

[138] P. E. Clarke, D. Field, A. J. Hydes, D. F. Klemperer, and M. J. Seakins, "Mass spectrometric studies of plasma etching of silicon nitride," *Journal of Vacuum Science & Technology B*, vol. 3, p. 1614, 1985. 78

[139] L. M. Loewenstein, "Selective etching of silicon nitride using remote plasmas of CF_4 and SF_6," *Journal of Vacuum Science & Technology A*, vol. 7, p. 686, 1989. 78

[140] C. J. D. Craigie, T. Sheehan, V. N. Johnson, S. L. Burkett, A. J. Moll, and W. B. Knowlton, "Polymer thickness effects on Bosch etch profiles," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 20, no. 6, pp. 2229–2232, 2002. 79

[141] M. D. Henry, S. Walavalkar, A. Homyk, and A. Scherer, "Alumina etch masks for fabrication of high-aspect-ratio silicon micropillars and nanopillars," *Nanotechnology*, vol. 20, no. 25, p. 255305, 2009. 79

[142] A. B. Kaul, *Microelectronics to Nanoelectronics: Materials, Devices & Manufacturability.* Taylor & Francis Group, 2012. 79

[143] G. N. Taylor and T. M. Wolf, "Oxygen plasma removal of thin polymer films," *Polymer Engineering & Science*, vol. 20, no. 16, pp. 1087–1092, 1980. 79

[144] "Aluminum Etchants." `http://www.transene.com/aluminum.html`. [Online; accessed 24-April-2013]. 79

[145] D. M. Knotter and T. D. Denteneer, "Etching mechanism of silicon nitride in HF-based solutions," *Journal of The Electrochemical Society*, vol. 148, no. 3, pp. F43–F46, 2001. 79

[146] W. Van Gelder and V. E. Hauser, "The etching of silicon nitride in phosphoric acid with silicon dioxide as a mask," *Journal of the Electrochemical Society*, vol. 114, no. 8, pp. 869–872, 1967. 80

[147] "Phosphoric acid nitride removal." `http://www.microtechprocess.com/pdf/MTS_Nitride.pdf`. [Online; accessed 24-April-2013]. 80

[148] "Ma-N 2400 - negative tone photoresist series." `http://www.microchem.com/PDFs_MRT/ma-N%202400%20overview.pdf`. [Online; accessed 27-November-2013]. 81

[149] N. Nelson-Fitzpatrick, "MaN 2400 electron beam lithography process." `https://qncfab.uwaterloo.ca/equipment/all/gen-resources/process-library/PROC_EB_Litho_MaN2403_rev1.pdf/view`. [Online; accessed 27-November-2013]. 81

[150] J. Robertson, "High dielectric constant oxides," *The European Physical Journal Applied Physics*, vol. 28, no. 03, pp. 265–291, 2004. 82

[151] V. Afanasev and A. Stesmans, "Hole trapping in ultrathin Al_2O_3 and ZrO_2 insulators on silicon," *Applied Physics Letters*, vol. 80, no. 7, pp. 1261–1263, 2002. 82

[152] P. Katiyar, C. Jin, and R. Narayan, "Electrical properties of amorphous aluminum oxide thin films," *Acta Materialia*, vol. 53, no. 9, pp. 2617–2622, 2005. 82

[153] W. M. M. Kessels, J. A. van Delft, G. Dingemans, and M. M. Mandoc, "Review on the prospects for the use of Al_2O_3 for high-efficiency solar cells." `http://www.tue.nl/fileadmin/content/faculteiten/tn/PMP/SolarLab_documents/C-Si_Workshop_Kessels.pdf`. [Online; accessed 4-May-2013]. 82, 83

[154] M. Groner, J. Elam, F. Fabreguette, and S. George, "Electrical characterization of thin Al$_2$O$_3$ films grown by atomic layer deposition on silicon and various metal substrates," *Thin Solid Films*, vol. 413, no. 1-2, pp. 186–197, 2002. 82

[155] S. Abermann, C. Henkel, O. Bethge, and E. Bertagnolli, "Electrical characteristics of atomic layer deposited aluminium oxide and lanthanum-zirconium oxide high-k dielectric stacks," in *Ultimate Integration of Silicon, 2009. ULIS 2009. 10th International Conference on*, pp. 209–212, March 2009. 82

[156] E. P. Gusev, M. Copel, E. Cartier, I. J. R. Baumvol, C. Krug, and M. A. Gribelyuk, "High-resolution depth profiling in ultrathin Al$_2$O$_3$ films on Si," *Applied Physics Letters*, vol. 76, no. 2, pp. 176–178, 2000. 82

[157] J. Kolodzey, E. Chowdhury, T. Adam, G. Qui, I. Rau, J. Olowolafe, J. Suehle, and Y. Chen, "Electrical conduction and dielectric breakdown in aluminum oxide insulators on silicon," *IEEE Transactions on Electron Devices*, vol. 47, pp. 121–128, 1 2000. 82

[158] X.-H. Zhang, B. Domercq, X. Wang, S. Yoo, T. Kondo, Z. L. Wang, and B. Kippelen, "High-performance pentacene field-effect transistors using Al$_2$O$_3$ gate dielectrics prepared by atomic layer deposition (ALD)," *Organic Electronics*, vol. 8, no. 6, pp. 718–726, 2007. 82

[159] J. Schmidt, A. Merkle, R. Brendel, B. Hoex, M. C. M. van de Sanden, and W. M. M. Kessels, "Surface passivation of high-efficiency silicon solar cells by atomic-layer-deposited Al$_2$O$_3$," *Progress in Photovoltaics: Research and Applications*, vol. 16, pp. 461–466, 9 2008. 82

[160] S. M. George, A. W. Ott, and J. W. Klaus, "Surface chemistry for atomic layer growth," *Journal of Physical Chemistry*, vol. 100, pp. 13121–13131, 8 1996. 83

[161] K. Reinhardt and W. Kern, *Handbook of Silicon Wafer Cleaning Technology, 2nd Edition*. Elsevier Science, William Andrew, 2008. 83

[162] M. Meuris, S. Verhaverbeke, P. W. Mertens, M. M. Heyns, L. Hellemans, Y. Bruynseraede, and A. Philipossian, "The relationship of the silicon surface roughness and gate oxide integrity in NH$_4$OH/H$_2$O$_2$ mixtures," *Japanese Journal of Applied Physics*, vol. 31, no. Part 2, No. 11A, pp. L1514–L1517, 1992. 83

[163] B. Hoex, S. B. Heil, E. Langereis, M. C. van de Sanden, and W. M. Kessels, "Ultralow surface recombination of c-Si substrates passivated by plasma assisted atomic layer deposited Al_2O_3," *Applied Physics Letters*, vol. 89, no. 042112, 2006. 83

[164] K. Robbie, J. Sit, and M. Brett, "Advanced techniques for glancing angle deposition," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 16, no. 3, pp. 1115–1122, 1998. 85

[165] "LOR and PMGI resists." `http://www.microchem.com/pdf/PMGI-Resists-data-sheetV-rhcedit-102206.pdf`. [Online; accessed 24-April-2013]. 85

[166] "PMGI and LOR resists: FAQs." `http://microchem.com/pmgi-lor_faq.htm`. [Online; accessed 26-April-2013]. 85

[167] "Toronto Nanofabrication Centre (TNFC)." `http://tnfc.utoronto.ca/`. [Online; accessed 06-March-2014]. 88

[168] "The Centre for Advanced Photovoltaic Devices and Systems (CAPDS)." `http://www.capds.uwaterloo.ca/`. [Online; accessed 06-March-2014]. 88

[169] X. Wu, E. S. Yang, and H. L. Evans, "Negative capacitance at metal-semiconductor interfaces," *Journal of Applied Physics*, vol. 68, p. 2845, 1990. 93

[170] B. Jones, J. Santana, and M. McPherson, "Negative capacitance effects in semiconductor diodes," *Solid State Communications*, vol. 107, no. 2, pp. 47–50, 1998. 93

[171] C. Zhu, L. Feng, C. Wang, H. Cong, G. Zhang, Z. Yang, and Z. Chen, "Negative capacitance in light-emitting devices," *Solid-State Electronics*, vol. 53, no. 3, pp. 324–328, 2009. 93

[172] J. Bisquert, G. Garcia-Belmonte, . Pitarch, and H. J. Bolink, "Negative capacitance caused by electron injection through interfacial states in organic light-emitting diodes," *Chemical Physics Letters*, vol. 422, no. 1-3, pp. 184–191, 2006. 93

[173] I. Mora-Sero, J. Bisquert, F. Fabregat-Santiago, G. Garcia-Belmonte, G. Zoppi, K. Durose, Y. Proskuryakov, I. Oja, A. Belaidi, T. Dittrich, R. Tena-Zaera, A. Katty, C. Lvy-Clment, V. Barrioz, and S. J. C. Irvine, "Implications of the negative capacitance observed at forward bias in nanocomposite and polycrystalline solar cells," *Nano Letters*, vol. 6, no. 4, pp. 640–650, 2006. 93

[174] M. Ershov, H. Liu, L. Li, M. Buchanan, Z. Wasilewski, and V. Ryzhii, "Unusual capacitance behavior of quantum well infrared photodetectors," *Applied Physics Letters*, vol. 70, no. 14, pp. 1828–1830, 1997. 93

[175] L. Latessa, A. Pecchia, A. Di Carlo, and P. Lugli, "Negative quantum capacitance of gated carbon nanotubes," *Physical Review B*, vol. 72, p. 035455, Jul 2005. 93

[176] T. Kopp and J. Mannhart, "Calculation of the capacitances of conductors: Perspectives for the optimization of electronic devices," *Journal of Applied Physics*, vol. 106, p. 064504, 2009. 93

[177] P. Dianat, R. W. Prusak, A. Persano, F. Quaranta, A. Cola, and B. Nabet, "Giant light-induced capacitance enhancements in an unconventional capacitor with two-dimensional hole gas," in *Photonics Conference (IPC), 2012 IEEE*, pp. 792–793, IEEE, 2012. 93

[178] L. Li, C. Richter, S. Paetel, T. Kopp, J. Mannhart, and R. C. Ashoori, "Very large capacitance enhancement in a two-dimensional electron system," *Science*, vol. 332, no. 6031, pp. 825–828, 2011. 93

[179] S. Ilani, L. A. Donev, M. Kindermann, and P. L. McEuen, "Measurement of the quantum capacitance of interacting electrons in carbon nanotubes," *Nature Physics*, vol. 2, no. 10, pp. 687–691, 2006. 93

[180] B. Skinner, G. Yu, A. Kretinin, A. Geim, K. Novoselov, and B. Shklovskii, "Effect of dielectric response on the quantum capacitance of graphene in a strong magnetic field," *Physical Review B*, vol. 88, no. 15, p. 155417, 2013. 93

[181] G. Yu, R. Jalil, B. Belle, A. S. Mayorov, P. Blake, F. Schedin, S. V. Morozov, L. A. Ponomarenko, F. Chiappini, S. Wiedmann, *et al.*, "Interaction phenomena in graphene seen through quantum capacitance," *Proceedings of the National Academy of Sciences*, vol. 110, no. 9, pp. 3282–3286, 2013. 93

[182] L. Wang, Y. Wang, X. Chen, W. Zhu, C. Zhu, Z. Wu, Y. Han, M. Zhang, W. Li, Y. He, *et al.*, "Negative quantum capacitance induced by midgap states in single-layer graphene," *Scientific reports*, vol. 3, 2013. 93

[183] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Letters*, vol. 8, no. 2, pp. 405–410, 2008. 93, 94

[184] G. Salvatore, D. Bouvet, and A.-M. Ionescu, "Demonstration of subthreshold swing smaller than 60mv/decade in Fe-FET with P(VDF-TrFE)/SiO$_2$ gate stack," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, pp. 1–4, Dec 2008. 94

[185] A. Fadavi Roudsari, I. Khodadadzadeh, S. S. Saini, and M. P. Anantram, "Photon induced negative capacitance in metal oxide semiconductor structures," submitted for publication. 94

[186] F. Werner, B. Veith, D. Zielke, L. Kühnemund, C. Tegenkamp, M. Seibt, R. Brendel, and J. Schmidt, "Electronic and chemical properties of the c-Si/Al_2O_3 interface," *Journal of Applied Physics*, vol. 109, no. 11, p. 113701, 2011. 98

[187] J. Simmons and G. Taylor, "Nonequilibrium steady-state statistics and associated effects for insulators and semiconductors containing an arbitrary distribution of traps," *Physical Review B*, vol. 4, no. 2, p. 502, 1971. 98

[188] "University of Alberta nanoFAB fabrication & characterization facility." `http://www.nanofab.ualberta.ca/`. [Online; accessed 11-April-2014]. 109

[189] T. Palacios, A. Hsu, and H. Wang, "Applications of graphene devices in RF communications," *IEEE Communications Magazine*, vol. 48, no. 6, pp. 122–128, 2010. 124

[190] H. Wang, T. Taychatanapat, A. Hsu, K. Watanabe, T. Taniguchi, P. Jarillo-Herrero, and T. Palacios, "BN/graphene/BN transistors for RF applications," *arXiv preprint arXiv:1108.2021*, 2011. 124

[191] H. Wang, L. Yu, Y.-H. Lee, Y. Shi, A. Hsu, M. L. Chin, L.-J. Li, M. Dubey, J. Kong, and T. Palacios, "Integrated circuits based on bilayer MoS_2 transistors," *Nano letters*, vol. 12, no. 9, pp. 4674–4680, 2012. 124

[192] D. Shiri, A. Verma, C. Selvakumar, and M. Anantram, "Reversible modulation of spontaneous emission by strain in silicon nanowires," *Scientific reports*, vol. 2, 2012. 124

[193] R. He, D. Gao, R. Fan, A. I. Hochbaum, C. Carraro, R. Maboudian, and P. Yang, "Si nanowire bridges in microtrenches: Integration of growth into device fabrication," *Advanced Materials*, vol. 17, no. 17, pp. 2098–2102, 2005. 124

[194] J. Y. Oh and M. S. Islam, "Silicon nanowire bridge arrays with dramatically improved yields enabled by gold colloids functionalized with HF acid and poly-L-Lysine," *IEEE Transactions on Nanotechnology*, vol. 12, pp. 1173– 1177, November 2013. 124

[195] J. Y. Oh and M. S. Islam, "Nanobridge gate-all-around phototransistors for electro-optical or gate circuit and frequency doubler applications," *Applied Physics Letters*, vol. 104, no. 2, p. 022110, 2014. 124

[196] J. Zhang, C. Con, and B. Cui, "Electron beam lithography on irregular surfaces using an evaporated resist," *ACS Nano*, vol. 8, no. 4, pp. 3483–3489, 2014. 124

[197] D. Decoster and J. Harari, *Optoelectronic Sensors*. John Wiley & Sons, Inc., 2009. 132, 133, 134