Mixed-Signal Multimode Radio Software/Hardware Development Platform

by

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A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Master of Applied Science
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2012

Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Radio frequency power amplifiers (PAs) are the most challenging part of the design of radio systems since they dictate the overall system's performance in terms of power efficiency and distortion generation. The performance is further challenged by modern modulation schemes which are characterized by highly varying signal envelopes. In order to meet the spectrum mask requirements, PAs are usually operated at high power back-off to ensure linearity, at the cost of efficiency. To tackle this issue, many efficiency enhancement techniques have been presented in the literature. In fact, these techniques do increase the PA power efficiency at back-off, however, efficiency enhancement techniques do not ensure the linearity of the PA. Furthermore, these techniques may lead to additional distortion. On the other hand, several linearization techniques have been developed to mitigate the PA nonlinearity problem and allow the PA to operate at less back-off. Digital Pre-Distortion (DPD) technique is gaining more attention, as compared to other linearization techniques, thanks to its simple concept and advancements in digital signal processors (DSP) and signal converters. DPD technique consists of introducing a nonlinear function before the PA so that the overall cascaded system behaves linearly. It was clear from the literature that this technique showed good performance. Yet, it has primarily been validated using commercial test equipment, which has good capabilities, and far from the real world environment in which this technique would be implemented. Indeed, DPDs would need to be implemented in signal processors characterised by limited resources and computational accuracy. This thesis presents an implementation of several DPD models, namely look-up table (LUT), memoryless polynomial and memory polynomial (MP), on a field programmable gate array (FPGA). A novel model reformulation made this implementation possible in fixed-point arithmetic. Measurements were collected to validate the DPD models' implementation and an improvement of the signal quality was recorded in terms of error vector magnitude (EVM) and adjacent channel leakage ratio (ACLR).

As many wireless access technologies must continue to coexist, multi-standard radio systems are required to reduce the cost while maintaining the interoperability. This thesis presents a development platform for multimode radio which comprises mixed-signal modules. The platform provides the capacity for hardware and software development. In fact, the FPGA under investigation allowed for the implementation of a baseband transceiver and DPD schemes. In addition, a software tool was developed as a dashboard to control and monitor the system. The radio system in the platform was optimized through the equalization of the feedback receiver frequency response performed through a simultaneous measurement of the amplitude ripple of the transmitter and receiver. Furthermore, a phase-coherent frequency synthesizer was designed to bring more flexibility by allowing the transmitter's carrier frequency to be different from the receiver's frequency.

Acknowledgements

I would like to express my sincere gratitude to all of those who helped me during the period of my Master of Applied Sciences at the University of Waterloo.

By this occasion, I wish to express my deepest thanks and gratitude to my supervisor, Dr. Slim Boumaiza, for his valuable guidance, encouragement and support throughout my graduate studies. His expertise, understanding, and patience added considerably to my graduate experience.

I would like to thank Dr. Sebastian Fischmeister and Dr. Mohamed Oussama Damen for reading my thesis.

I am indebted to Farouk Mkadem, PhD Student; Imaddudin Mohammad and Oleg Petelin, Co-op Students; and Houssem Medini, Internship Student; and I would like to acknowledge their collaboration in this work.

Special thanks go to my colleagues in Emerging Radio System Group (EmRG).

Last but not least, I would like to express my thanks, love and respect to my family for their support throughout my life.

Table of Contents

List of Tables

List of Figures

Nomenclature

3GPP	3rd Generation Partnership Project
ACLR	Adjacent Channel Leakage Ratio
ADC	Analog to Digital Converter
AM/AM	Amplitude-to-Amplitude distortion
AM/PM	Amplitude-to-Phase distortion
CDMA	Code Division Multiple Access
DAC	Digital-to-Analog Converter
dB	Decibel
DC	Direct Current
DDR	Double Data-Rate
DDS	Direct Digital Synthesizer
DPD	Digital Pre-Distortion
DUT	Device Under Test
EER	Envelope Elimination and Restoration
ET	Envelope Tracking
EVM	Error Vector Magnitude
FIR	Finite Response Filter

FPGA	Field-Programmable Gate Array
GSM	Global System for Mobile communications
GUI	Graphical User Interface
HSMC	High-Speed Mezzanine Connector
I and Q	In-phase and Quadrature
IF	Intermediate Frequency
LSE	Least Square Error
LTE	Long Term Evolution
LUT	Look-Up Table
MiMAX	Worldwide interoperability for Microwave Access
MP	Memory Polynomial
MSB	Most Significant Bit
MSDPD	Mixed-Signal Digital Pre-Distortion
MSR	Muli-Standard Radio
NMSE	Normalized Mean Square Error
PA	Power Amplifier
PAPR	Peak to Average Power Ratio
PEP	Peak Power
PLL	Phase-Locked Loop
RAT	Radio Access Technology
RF	Radio Frequency
VCO	Voltage-Controlled Oscillator
VGA	Variable Gain Amplifier
WCDMA	Wideband Code Division Multiple Access

Chapter 1

Introduction

In the last three decades, the explosive growth of mobile and wireless communication systems has changed people's lives. Wireless services have migrated from conventional voice-based services to data-based services. Wireless access technologies have also evolved; from first-generation (1G) analog systems which satisfied the need for basic mobile voice service; to second-generation (2G) systems which introduced great user' capacity and wider coverage; to third-generation (3G) systems which offered higher speed data; to fourth-generation (4G) systems now under development, which should enhance mobile system performance. Throughout this evolution, standards and technologies were being deployed; global system for mobile communications (GSM) and IS-95 code division multiple access (CDMA) technologies follow the 2G standards; CDMA2000, wideband CDMA (WCDMA) and worldwide interoperability for microwave access (WiMAX) are considered 3G technologies; and long term evolution (LTE) Advanced is being designed to meet the 4G requirements.

Furthermore, these heterogeneous wireless networks, where diverse types of communication standards are expected to coexist, call for flexible multi-standard radio (MSR) systems to replace traditional single-standard ones. For example, according to the 3rd Generation Partnership Project (3GPP), an MSR base station is a base station characterized by the ability of its receiver and transmitter to process two or more carriers in common active radio frequency (RF) components simultaneously in a declared RF bandwidth, where at least one carrier is of a different radio access technology (RAT) than the other carrier(s). Multimode radio provides mobile communication operators with a low cost solution which tolerates the inter-operability of the different technologies.

The design of radio systems has become more challenging as where the new modulation schemes are characterized by their high spectral efficiency as well as high peak to average

power ratio (PAPR). Radio frequency power amplifiers (RF PAs) are fundamental components in wireless communication systems. They must amplify the transmitted RF signal to allow it to reach the required distant receiver. Moreover, the performance of the PA dictates the overall performance of the radio chain in terms of linearity and efficiency. On one hand, nonlinearity can appear as in-band distortion, degrading the signal quality, or as out-of-band distortion, in the form of spectral regrowth both of which interfere with adjacent channels and result in a violation of the emission requirements assigned by regulatory bodies. On the other hand, higher power efficiency translates into longer lifetime and also reduces the size and cost of the necessary cooling system.

High linearity and high power efficiency are two antagonistic requirements. The PA can be biased in a linear class of operation such as class A or B. However, these classes of operation are characterized by very poor efficiency at high power back-off. Two axes of PA performance improvement can be distinguished; the first focuses on designing PAs with improved efficiency in the back-off region by means of efficiency enhancement techniques, such as Doherty PAs[1], envelope-elimination and restoration[2] and envelope-tracking[3] techniques; the second axis being the implementation of one of the linearization techniques, such as feedforward, feedback and predistortion techniques, to extend the linear range of the PA and allow the PA to work in its high efficiency region. Among the existing linearization techniques, the digital pre-distortion (DPD) is currently the most cost-effective solution and its linearization capability is improving thanks to the advancements in digital signal processing and signal converters. The principle of DPD consists of building an inverse nonlinear function based on the PA behavior, which is then used to introduce distortion to the transmitted signal in such way that the cascade (predistorter-PA) is linear.

Several behavioral modeling schemes have been presented in the literature. These schemes can be divided into two general groups based on their memory effects handling capability. The first group includes modeling schemes dealing with static nonlinearity, namely memoryless polynomial[4] and look-up table (LUT)[5, 6]. The second one includes modeling schemes dealing with dynamic nonlinearity such as Volterra series[7, 8] and memory polynomial[9]. When examining a DPD's capacity to act as linearizer, the test setup should ensure good performance to reduce negative effects on the device under test (DUT) thus increasing accuracy. The test system also has to reproduce a realistic environment as much as possible. Moreover, processing time needs to be taken into account; otherwise, instead of improving the system, it would be slowed down. For this reason, real-time systems are more suitable to satisfy the required timing performance of this application. Indeed, many of the test beds[10, 11] used to validate a given DPD as a linearizer make use of standard test equipment, such as signal generator and vector analyzer, to feed and capture the signal to and from the PA, respectively. Such advantageous measurement set-ups do

not reflect the practical implications of implementing DPD in a real world environment (e.g., when the PA is used in a base station and not in a laboratory), such as restricted accuracy due to the lack of floating-point arithmetic and limited resources.

The objective of this work is the realization of a development platform for multimode radio where both analog and digital parts are involved. Unlike previous work, the proposed platform is very close to the industrial design.

This thesis comprises four main chapters organized as follows:

- **Chapter 2**, the PA behavior and its characterization are discussed and problematic memory effects are presented.
- **Chapter 3** presents an overview of PA efficiency enhancement and linearization techniques focusing on DPD.
- **Chapter 4**, the mixed-signal multimode hardware/software development platform is presented along with component implementation, hardware calibration, the software tool, and measurement results.
- **Chapter 5**, a summary of the work is presented accompanied by a discussion of the major implications and results.

Chapter 2

Radio-Frequency Power Amplifiers

2.1 Introduction

A power amplifier (PA) is an electronic circuit that produces a large amount of power as its output by means of direct current(DC) input power. The output of the PA is at radio frequency (RF)/microwave and its level is greater than 1 Watt. A PA is usually operating in a nonlinear mode where diverse techniques have to be deployed such as linearization techniques, detailed in chapter 3, also requiring nonlinear modeling and characterization, discussed below. PAs are used in mqny applications; communication base stations, radar and RF heating, for example. In fact, the PA is benefiting from many improvements thanks to the advances taking place in the signal processing field.

The development cycle of RF power amplifiers can be divided into four eras. In the beginning of the 19th century, RF power amplifiers were implemented through several techniques namely spark, arc and alternator techniques. Next followed the era of vacuum-tube PAs, when the thermo-ionic vacuum tube made the generation and control of the RF signal possible. Then came the solid state RF power devices, coinciding with the start of silicon bipolar transistor manufacturing. During the last era, there has been a proliferation of the PA with a variety of solid state devices (eg., HEMT, FET, MOS) being made available, constructed from a variety of materials (eg., SiC, GAs, GaN), which are suitable for monolithic microwave integrated circuit (MMIC) due to their reduced scale.

In this chapter, PA related quantities such as gain and efficiency are defined, linear and nonlinear PAs are presented, nonlinear PA characterization is outlined using distortion and behavioral modeling and finally, problematic memory effects are discussed.

2.2 Power Amplifier Gain and Efficiency

In this section, definitions of key quantities are presented. First, the output and input power are defined, then, the power amplifier gain, DC power and the efficiency.

The output power is the power delivered to the load in a specified frequency band as shown in the following Equation 2.1.

$$P_{out} = P_{out}(f), \qquad f_l \leq f \leq f_u \tag{2.1}$$

Where f_l and f_u are the lower and upper frequency range, respectively.

The input power is the power available to the PA in a specified frequency band as shown in Equation 2.2.

$$P_{in} = P_{in,av}(f), \qquad f_l \leq f \leq f_u \tag{2.2}$$

The power gain is the ratio between the two previous quantities in the form:

$$G(f) = \frac{P_{out}}{P_{in}}, \qquad f_l \leq f \leq f_u \tag{2.3}$$

The DC power is the power delivered by the power supply to the PA. Since the PA is biased at constant voltage, the DC power is expressed by:

$$P_{DC} = V_{bias}(t) \cdot \frac{1}{T} \int_0^T I_{bias} \cdot dt \tag{2.4}$$

In the general case, the DC power is not all converted to an output power; there is a portion of it converted into harmonic frequency and another portion dissipated inside the amplifier. Hence, the power balance can be expressed as:

$$P_{DC} + P_{in}(f) = P_{out}(f) + P_{out}(\tilde{f}) + P_{diss}, \qquad f_l \leq f \leq f_u \, and \, \tilde{f} \leq f_l \, or \, \tilde{f} \geq f_u \tag{2.5}$$

The previous equation can be modeled as shown in Figure 2.1.

The PA efficiency represents the quality factor for DC power consumption. A general expression of the efficiency is computed as shown in Equation 2.6.

$$\eta = \frac{P_{out}}{P_{in,tot}} = \frac{P_{out}(f)}{P_{in}(f) + P_{DC}} \tag{2.6}$$

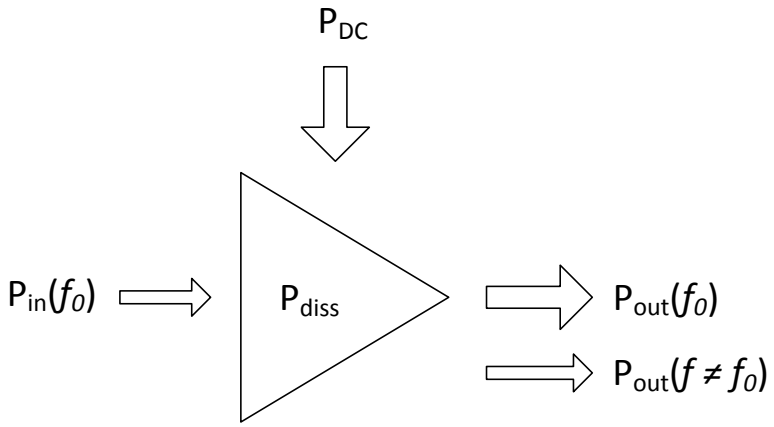


Figure 2.1: Power Budget in Power Amplifier.

When the gain is large, that quantity is reduced to the drain/collector efficiency and expressed as:

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.7}$$

Another definition of the efficiency is the power added efficiency which is the ratio between the RF power added by the amplifier and the DC power required. It is expressed in the Equation 2.8.

$$\eta_{poweradded} = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}}{P_{DC}}\left(1 - \frac{1}{G}\right) \tag{2.8}$$

The PA efficiency is usually expressed as a percentage as in:

$$\eta(\%) = \eta \cdot 100 \tag{2.9}$$

Typical output power, gain and efficiency are presented in Figure 2.2 below. As can be seen, for a certain level of input power (usually referred to as the input power compression point), when the output power is no longer in linear relation with the input power, the gain decreases. Furthermore, the efficiency is higher when the PA is nonlinear, however, it decrease after saturation. PA nonlinearity is addressed in more detail in the next section.

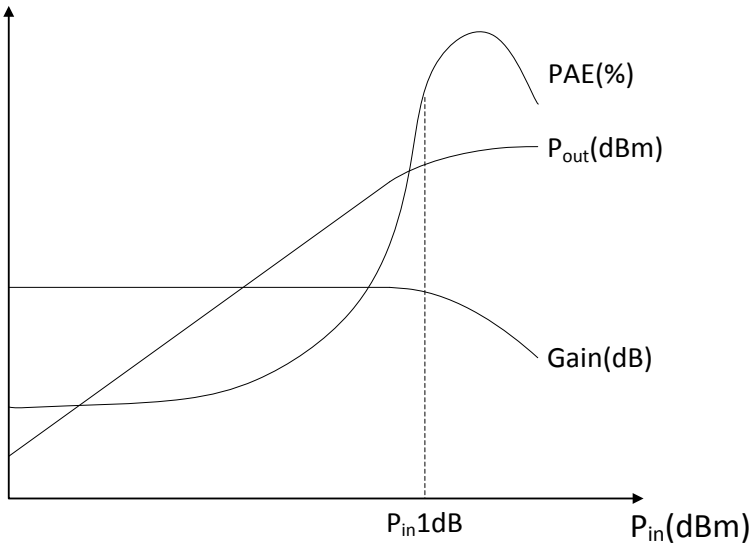


Figure 2.2: Output Power, Power Gain and Power-Added Efficiency.

2.3 Linear and Nonlinear Power Amplifier

RF power amplifiers are categorized into different classes, namely A, B, C, D, E and F, depending on their mode of operation. They can also be classified by their linearity; class A and B are considered linear amplifiers and class C, D, E and F are considered nonlinear amplifiers. In this section, an overview of these conventional PAs is presented.

In class A, the transistor remains active all the time due to the large quiescent current. It behaves as a voltage controlled current source. Hence, the drain voltage and current waveforms perfectly match as shown in Figure 2.3. In fact, the amplification process is inherently linear. The DC power is constant and the efficiency of an ideal class A PA is 50 percent at peak power (PEP).

In class B, the transistor is only active half of the time since the quiescent drain current is zero. Consequently, the drain current is half sinusoid unlike class A (Figure 2.3). However, a class B PA is linear since the amplitude of the drain current is proportional to the drive amplitude and the sinusoidal shape of the drain current could recovered by shorting the harmonics. The instantaneous efficiency of an ideal class B PA is $\frac{\pi}{4}$ (78.5 percent) at PEP. Even at a lower power level, a class B PA is more efficient than a class A.

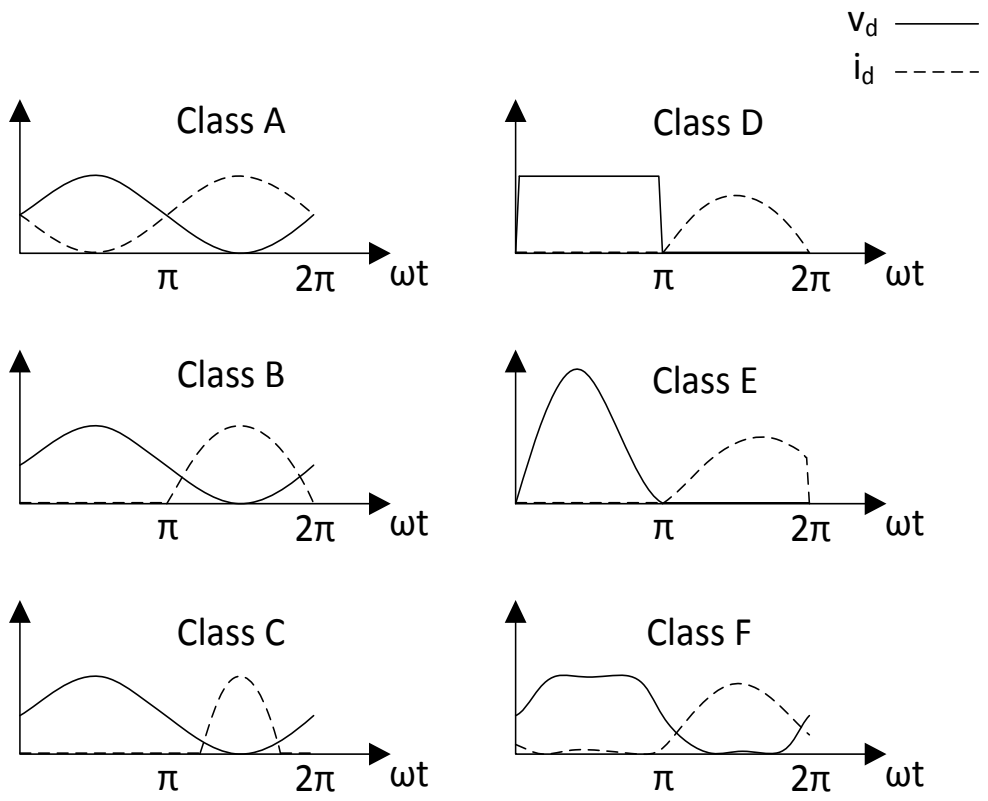


Figure 2.3: Ideal Power Amplifier Classes Waveforms.

In a classical class C PA, the transistor is active for less than half of the time because the quiescent drain current is negative and the gate is biased below the threshold. A class C PA is nonlinear but more efficient than a class A or B PA. Theoretically; the efficiency can be increased to 100 percent by reducing the conduction angle to 0 which will cause the output power to fall toward zero. However, at a typical conduction angle of 150 °, an ideal efficiency for a class C PA is 85 percent.

In a class D PA, a square drain-voltage waveform is generated using two or more transistors working as switches. The fundamental frequency component is passed to the load through a filter. The efficiency of an ideal class D PA is 100 percent since the current is drawn only while the transistor is ON. Practical class D PAs suffer from losses due to saturation, switching speed, and drain capacitance.

In class E, the drain voltage is the sum of the DC and RF currents charging the drain shunt capacitance. For this class of operation only a single transistor is used and it is operated as a switch. In an optimum class E PA, the drain voltage and current waveforms do not overlap, hence, the efficiency of an ideal class E PA is 100 percent. Finally, In class F, the drain waveforms are shaped using harmonic terminations. In fact, the voltage waveform includes odd harmonics and approximates a square wave, although the current waveform includes even harmonics and approximates a half sine wave. The efficiency of an ideal class F PA depends on the number of harmonic terminations. For example the efficiency is 83.3 percent for second and fourth current harmonic terminations and third and fifth voltage harmonic terminations.

2.4 Nonlinear Power Amplifier Characterization

2.4.1 Harmonic Distortion

One of the properties of nonlinear circuits is the creation of new frequency components at their output which are different from the input frequencies. To demonstrate how these new frequencies are generated in nonlinear circuits, the output is described by the power series of the input as shown in Equation 2.10 (in this case the order is limited to 3 for the ease of computation)

$$V_{out}(t) = a_1 V_{in}(t) + a_2 V_{in}^2(t) + a_3 V_{in}^3(t) \tag{2.10}$$

Where a_1, a_2 and a_3 are constant coefficients.

We assume that V_{in} is a single-tone input excitation of the form:

$$V_{in}(t) = A\cos(\omega t) \tag{2.11}$$

Substituting Equation 2.11 into Equation 2.10 and applying trigonometric identities, we obtain:

$$V_{out}(t) = \frac{a_2 A^2}{2} + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos(\omega t) + \frac{a_2 A^2}{2}\cos(2\omega t) + \frac{a_3 A^3}{4}\cos(3\omega t) \tag{2.12}$$

As can be seen, new components are generated at the output, and they are at frequencies of multiples of the input fundamental frequency. For that reason, these components are called harmonics.

2.4.2 Intermodulation Distortion

The same analysis could be applied to illustrate the generation of intermodulation components, however, the excitation signal is assumed to be a two-tone of the form

$$V_{in}(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \tag{2.13}$$

Substituting Equation 2.13 into Equation 2.10 and applying trigonometric identities, we obtain

$$\begin{aligned} V_{out}(t) \;=\; & \frac{a_2 A_1^2}{2} + \frac{a_2 A_2^2}{2} + \left(a_1 A_1 + \frac{3a_3 A_1^3}{4} + \frac{3a_3 A_1 A_2^2}{2} \right) \cos(\omega t) \\ & + \left(a_1 A_2 + \frac{3a_3 A_2^3}{4} + \frac{3a_3 A_1^2 A_2}{2} \right) \cos(\omega_2 t) \\ & + \frac{a_2 A_1^2}{2} \cos(2\omega_1 t) + \frac{a_2 A_2^2}{2} \cos(2\omega_2 t) \\ & + \frac{a_3 A_1^3}{4} \cos(3\omega_1 t) + \frac{a_3 A_2^3}{4} \cos(3\omega_2 t) \\ & + a_2 A_1 A_2 \left(\cos\Big((\omega_1 + \omega_2)t\Big) + \cos\Big((\omega_1 - \omega_2)t\Big) \right) \\ & + \frac{3a_3 A_1^2 A_2}{4} \left(\cos\Big((2\omega_1 + \omega_2)t\Big) + \cos\Big((2\omega_1 - \omega_2)t\Big) \right) \\ & + \frac{3a_3 A_2^2 A_2}{4} \left(\cos\Big((2\omega_2 + \omega_1)t\Big) + \cos\Big((2\omega_2 - \omega_1)t\Big) \right) \end{aligned} \tag{2.14}$$

As can be seen, on top of the harmonics, new frequency components are being added. These components are so-called intermodulation components. Furthermore, the generated frequencies for a nonlinear system occur at a linear combination of the two excitation frequencies

$$\omega_{n,m} = m\omega_1 + n\omega_2, \qquad m, n = -3, -2, -1, 0, 1, 2, 3 \tag{2.15}$$

Figure 2.4 illustrates the phenomena of frequency generation in nonlinear circuits

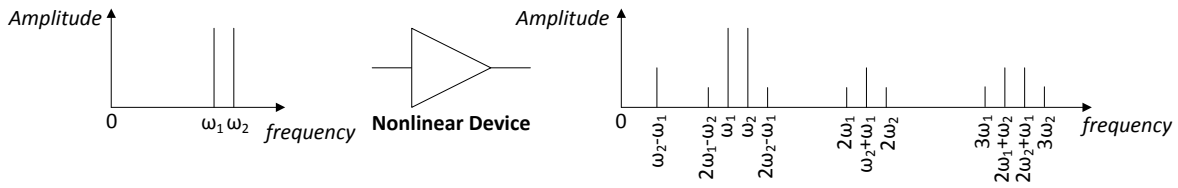


Figure 2.4: Frequency Components Generation in Nonlinear Devices.

2.4.3 Amplitude and Phase Distortion

The amplitude distortion is expressed by the change of the output amplitude power in comparison to the input amplitude power at the fundamental frequencies, as demonstrated in the previous section. It is usually referred to as the amplitude-to-amplitude distortion (AM/AM) characteristic and is expressed as follows:

$$A_{in}(t) = g(A_{out}(t)) \tag{2.16}$$

where A_{in} and A_{out} are the input and output amplitude power, respectively; and, $g(.)$ is a nonlinear function.

The amplitude distortion is usually accompanied by a phase distortion (phase shift), referred to as amplitude-to-phase distortion (AM/PM). The AM/PM characteristic represents the variation of the phase at a given amplitude level and it is expressed in the following equation:

$$\phi_{out} = \phi_{in} + f(A(t)) \tag{2.17}$$

where ϕ_{out} , ϕ_{in} and $A(t)$ are the input and the output phases and the input amplitude power, respectively, and $f(.)$ is a nonlinear function.

2.4.4 Quantities for Measuring the Nonlinearity

Adjacent Channel Leakage Ratio

The adjacent channel leakage ratio (ACLR), also named adjacent channel interference, is the power ratio of the neighboring channels and the intended channel. The ACLR describes

the amount of energy generated outside the appropriate channel, referred to as spectrum regrowth (Figure 2.5), and it occurs as result of intermodulation distortion of modulated signals. This sort of distortion is termed out-of-band distortion.

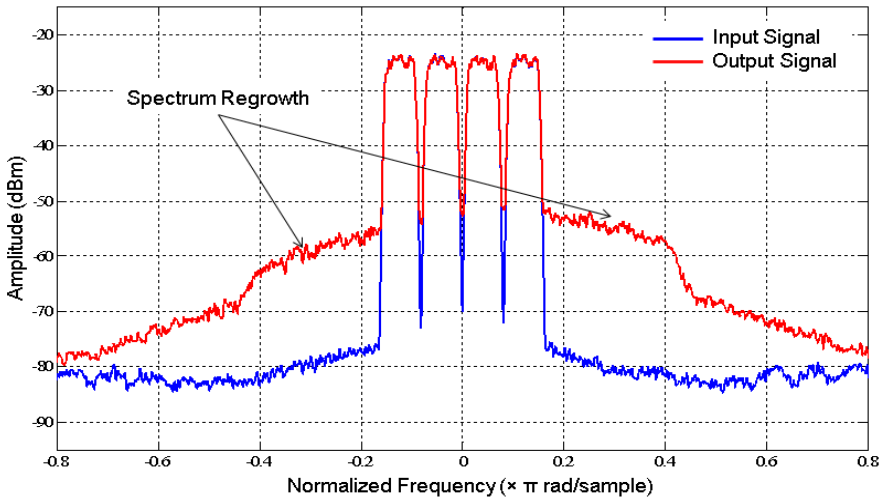


Figure 2.5: Spectrum Regrowth.

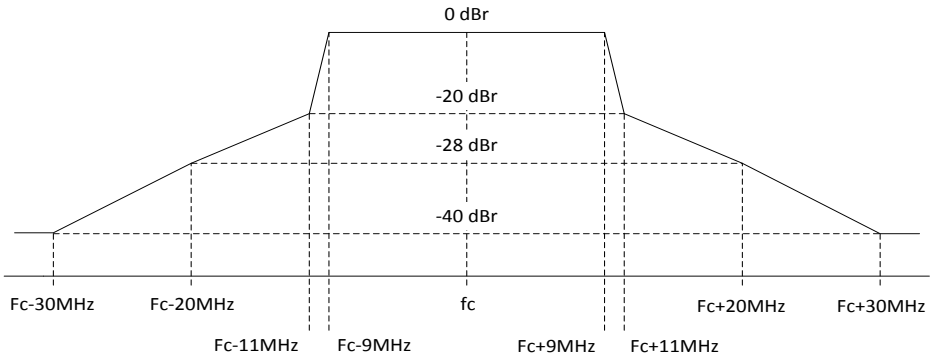


Figure 2.6: 802.11a Spectral Mask.

Regulatory agencies and standards bodies specify a spectral mask for each channel, an example is shown in Figure 2.6[12], which is a set of power levels associated with a frequency offset. The transmitted signal should fall within the specified mask unless it fails the regulation specifications.

Error Vector Magnitude

The error vector magnitude (EVM) is a quantity that measures the discrepancy between the received signal and the ideal (reference) signal and it is associated to the bit error rate in a digital modulation scheme. Usually, the received signal contains a phase error and a magnitude error due to the noise and imperfections occurring during the transmission of the signal. A large EVM can be translated to a large symbol error rate. The EVM describes the in-band distortion and the deformation of the constellation. An illustration is presented in Figure 2.7.

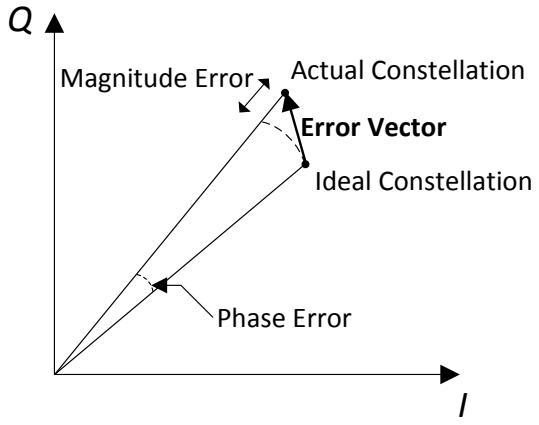


Figure 2.7: Error Vector Magnitude.

The EVM is calculated as follow:

$$EVM = \frac{\sum_{k=1}^{M} |Z(k) - R(k)|^2}{\sum_{k=1}^{M} |R(k)|^2} \tag{2.18}$$

where M is the measured sequence length, $Z(k)$ and $R(k)$ are the actual and the reference signal, respectively.

2.4.5 Power Amplifier Behavioral Modeling

PA modeling has many purposes; it can be used for circuit analysis, for simulation in computer-aided design (CAD) tools or for improving the PA performance through pre-distortion techniques (presented in the next chapter). A PA model should reproduce the performance of the PA, under given operating conditions, to a certain degree of accuracy.

Given the data extraction method, PA models can be classified into two sets: physical models and empirical models[13]. Physical models require knowledge of the equivalent circuit of the PA to develop equation relating terminal voltages and currents. However, empirical (behavioral) models do not require information on the internal structure of the PA. In fact, the data used for modeling the PA are collected through measuring its behavior. These data are usually in the form of AM/AM and AM/PM[14]. "The model only reproduces the measurements and acts as a compact description of the experimental data"[14], consequently, "the models are valid only in a neighborhood of the measuring conditions"[14].

PA behavioral models are classified in terms of memory effects handling: models without memory, with linear memory, and with nonlinear memory[15]. They are also classified into two categories: neural-network based models which consist of artificial neural-networks[16] and dynamic fuzzy neural networks[17], and Volterra series[7, 8] based models such as memory polynomial (MP)[9], Volterra with dynamic deviation reduction[18], generalized memory polynomial[19].

In this work, behavioral models were mainly used in the digital pre-distortion (DPD) analyses, detailed in the next chapter, where the behavior of the inverse of the PA is modeled to shape the input signal of the PA.

2.5 Memory Effects in Power Amplifier

Memory effects describe the dynamic behavior of the PA, unlike the other types of distortion that describe the static behavior of the PA. Memory effects are mainly caused by dynamic thermal effects, unintentional modulation on supply rails and the semiconductor trapping effects[20].

Time constants of the dynamic behavior of the PA can be divided into two classes: fast response, similar to the period of the RF signal frequency and so called short-term memory, and slow response, which is on the order of the signal envelope and termed long-term memory.

The phenomena of memory effects occur when the output of the PA is not only a function of its current input, but also a function of the previous input and output values. In fact, memory effects are more noticeable for wideband signals where the signal envelope has a shorter period.

2.6 Conclusion

This chapter has discussed several topics of relevance to PAs, with a focus on nonlinear PAs. The PA is a critical component in the transmission chain and its efficiency must be as high as possible. To achieve high efficiency, nonlinear PAs are deployed despite all of the problems associated with them. In order to clearly anticipate how they will function, PAs are characterized and modeled in the ways presented in this chapter. In the next chapter, an overview of PA efficiency enhancement and linearization techniques is presented.

Chapter 3

Power Efficiency and Linearity Enhancement for RF Power Amplifiers

3.1 Introduction

More recently developed modulation schemes tend to improve the spectral efficiency of PAs. However, they cause several problems for the PA. Conventional PAs are usually designed to deliver maximum efficiency at PEP. Hence, the average efficiency is low when the PA is derived by amplitude modulated signals. On the other hand, as discussed earlier in this thesis, the efficient region is characterized by its nonlinearity and using the PA in that region distorts the input signal. This chapter describes several techniques that can be used to enhance PA performance grouped into two categories: efficiency enhancement techniques and linearization techniques.

3.2 Efficiency Enhancement Techniques

As presented in Chapter 2, conventional RF PAs are characterized by poor efficiency at power back-off which reduces their overall efficiency when used with the new modulation schemes in which the PAPR is very high (about 9dB on average). Many techniques exist in the literature which enhance the PA efficiency at power backoff and include Doherty PA[1], envelope elimination and restoration[2], and envelope tracking[21].

3.2.1 Doherty Power Amplifier

The Doherty amplifier was first proposed by W. H. Doherty in 1936[1] who used high power tube amplifiers in a short wave amplitude modulated broadcast station. Different Doherty PA configurations exist in the literature but the most common configuration consists of a two-stage Doherty PA, shown in Figure 3.1, which includes two PAs. The first PA is called the main (or carrier) PA and the second is the auxiliary (or peaking) PA. The two amplifiers' outputs are combined through a quarter wavelength transmission line placed after the main amplifier (explained in more detail below). The quarter wavelength transmission line at the input of the auxiliary PA has the basic role of compensating for the 90 phase shift caused by the other transmission line. Usually, the main amplifier is biased in class B and the auxiliary is biased in class C.

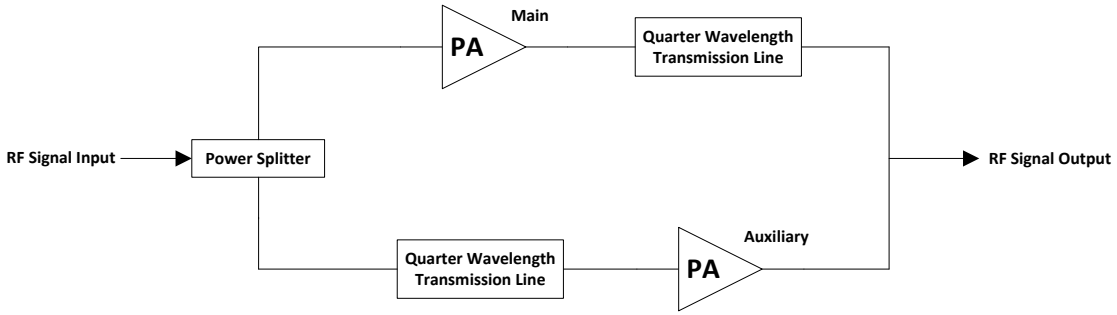


Figure 3.1: Doherty Power Amplifier Configuration.

To simplify the theory of operation of a Doherty PA, three operational conditions can be distinguished depending on the output power level[22]. In the low-power region, the drive to the peaking amplifier is insufficient to overcome its bias. Hence, the peaking amplifier remains cut-off and its output impedance is near infinite. However, the main amplifier operates in active region and is saturated due to the impedance present at its output. As a result, the efficiency at a back-off power level of 6dB is 78.5%, which is the PEP efficiency of a conventional class B amplifier. In the medium-power region, the main amplifier is saturated whereas the peaking amplifier is operating in its active region. The efficiency of the main amplifier is at its maximum value while the efficiency of the auxiliary amplifier reaches half of its maximum value. At output peak-power, both amplifiers are saturated and each delivers half of the system output power. The efficiency is equal to

the maximum achievable by class a B PA. The resulting instantaneous efficiency curve is shown in Figure 3.2.

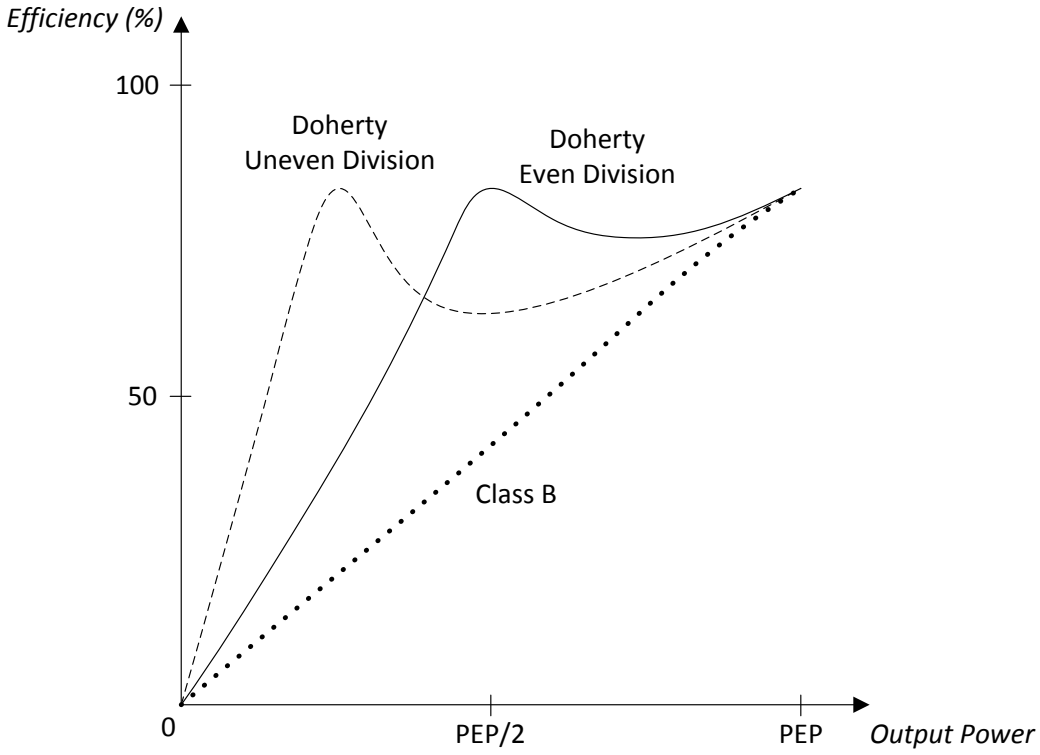


Figure 3.2: Typical Doherty Power Amplifier Efficiency.

In Doherty amplifier configuration, the auxiliary amplifier acts as a controlled current source that modulates the load seen at the output of the main PA (through the quarter wavelength transmission line) to deliver an adequate amount of power. The equal power division enables a high efficiency level to be maintained for a power back-off of 6 dB. However, when a higher back-off is required, uneven division could be used which will increase the high efficiency range of power back-off as shown in Figure 3.2.

3.2.2 Envelope Elimination and Restoration

The envelope elimination and restoration (EER) technique was proposed by Leonard R. Kahn in the 1950s[2] to improve the amplification efficiency of single side-band (SSB) transmitters. This technique aimed to create a high efficiency and linear PA by combining a highly efficient but nonlinear RF PA and a highly efficient envelope amplifier. The architecture of the EER transmitter is shown in Figure 3.3.

The principle of the classical approach to EER is a separation of the phase and envelope components of the signal by using a limiter and envelope detector, respectively. The phase component is amplified efficiently by a nonlinear PA since it is a constant-amplitude signal. The envelope is efficiently processed by an amplitude modulator. At the final stage, amplitude modulation of the phase component restores the original signal with an amplified amplitude.

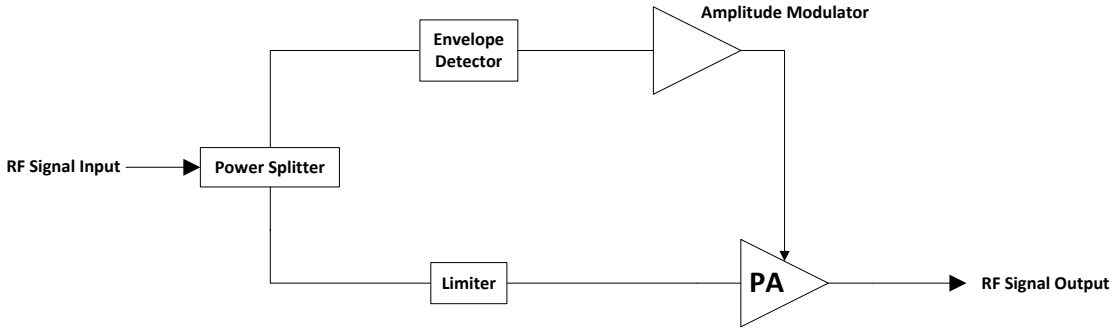


Figure 3.3: Envelope Elimination and Restoration Technique.

In a modern implementation, both the envelope and the phase components are generated by a DSP which directly feeds the amplifiers. EER transmitters are characterized by their high efficiency over a wide dynamic range. In fact, the average efficiency of a EER transmitter is three to five times of that of a linear amplifier[23, 24].

However, the practical implementation of Kahn EER technique has several limitations. The two greatest challenges are the linearity of the amplitude modulator and the alignment of the two paths since the envelope bandwidth must be at least twice the RF bandwidth and the misalignment must not exceed one tenth of the inverse of the RF bandwidth[25].

3.2.3 Envelope Tracking

Envelope tracking (ET) architecture (Figure 3.4) has similarities to that of the EER technique. However, the modulated signal is amplified linearly without subtracting the envelope component from it. The role of the envelope amplifier is to adjust the bias of the RF PA to improve its efficiency at back-off power[3].

The envelope of the RF input signal is detected, and then used to dynamically control the gate bias voltage which, in turn, forces the drain current to be proportional to the signal envelope. Hence, the DC power consumption is reduced at back-off power and consequently the efficiency become higher.

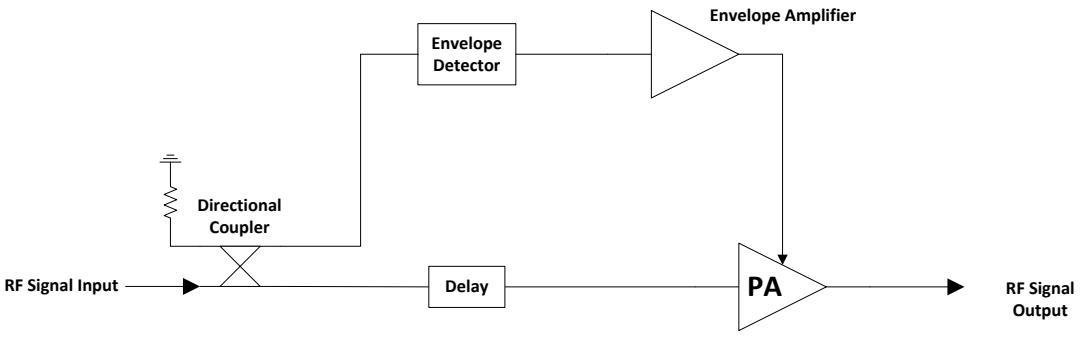


Figure 3.4: Envelop Tracking Technique.

The ET technique results in a greater efficiency than linear amplification, especially at back-off performance. It has been shown that at 10dB back-off, linear amplification efficiency was 10 percent compared to 41 percent while using ET technique[26].

Nevertheless, the ET technique is not free of problems. Since the gain and phase vary with the supply voltage, nonlinearity can be introduced to the RF PA[27]. Linearization techniques, discussed in the next section, are used to address this problem. Furthermore, the supply voltage ripple at the switching frequency can generate spurious outputs. Finally, while using the ET technique, the RF PA efficiency is improved but the overall efficiency may remain low since it depends on the efficiency of the envelope amplifier as shown in the Equation 3.1 below:

$$\eta_{overall} = \eta_{PA} \cdot \eta_{EA} \tag{3.1}$$

3.3 Linearization Techniques

As was demonstrated in the previous section, efficiency enhancement techniques attempt to improve the PA power efficiency without consideration of the impact on the linearity of the PA. However, linearization techniques can be used simultaneously with efficiency enhancement techniques to improve the overall performance of the PA. They do this in two ways; improving linearity and permitting the PA to operate at less back-off, and consequently with higher efficiency.

PA linearization has become a very broad research area due to its varied benefits such as improved battery lifetime and reduced heat emission. Linearization techniques tend to reduce PA nonlinearity and hence the problems related to this. This section provides an overview of the three main techniques that have been developed: feedforward, feedback, and predistortion.

3.3.1 Feedforward Technique

Feedforward technique makes use of two PAs, named main and error respectively, to obtain linear amplification. The feedforward architecture is shown in Figure 3.5. The signal in the main path is amplified by the main PA, generating nonlinearities at the output. Delayed PA input is subtracted from a sample of its output, and the resulting signal (error signal) is mostly formed by distortion only. This error signal is then linearly amplified by the error PA (EPA) to the required level and, when antiphase correction is coupled with the delayed output of the main PA, it removes the distortion. The delays in the loops are determined by the amplification time of the respective PAs. At the output, we obtain a linearly amplified replica of the input signal. With this kind of linearizer, the EPA is crucial as any nonlinearity in its performance would introduce additional distortion to the system. The EPA's gain should match the gain of the main PA so that the distortions cancel each other out. In addition, the delay lines should be tightly tuned to achieve good performance. In fact, a gain and phase mismatch limits the bandwidth of linearization and the value of distortion cancellation.

However, the error signal is characterized by a high PAPR, therefore the EPA is not very efficient. Consequently, the overall efficiency of the feedforward transmitter is low, typically 10 to 15 percent[28].

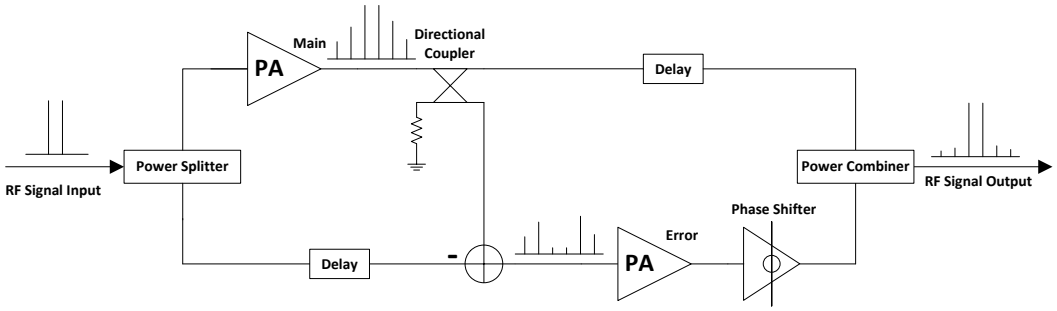


Figure 3.5: Typical Feedforward Linearizer System.

3.3.2 Feedback Technique

The feedback linearization concept relies on a comparison of the input and output of the RF PA and subsequent adjustment of the gain or phase of the input signal through a feedback loop to obtain linear output. Many feedback architecture variations are proposed in the literature such as envelope feedback[29], polar-loop feedback[30] and Cartesian feedback[31], which are discussed in more detail below.

In the envelope feedback architecture, the envelopes of the input and distorted output signals are extracted by envelope detectors and then compared. An error signal is then generated to control the gain of the amplifier and minimize its error signal. Envelope feedback architecture is shown in Figure 3.6. This type of feedback circuit is easy to implement but it has many limitations. The envelope feedback can correct only for amplitude distortion not for phase distortion, therefore, little improvement can be made in amplifiers with highly nonlinear phase distortion. Furthermore, the feedback components, such as the detectors, limit the linearization performance and bandwidth.

The polar-loop architecture is based on the phase-locked loop (PLL) concept as shown in Figure 3.7. The amplifier output is sampled and downconverted to an intermediate frequency, and then the envelope and the phase components of this signal are separated as is the case for the EER transmitter. The envelope component is then processed in a manner similar to that used in envelope feedback architecture. However, the phase component, after being filtered and amplified, is used to feed the voltage-controlled oscillator (VCO) to build a phase-locked loop architecture. Polar-loop architecture has the advantage of correcting for the phase distortion, nevertheless, it has many drawbacks. For example, the amplitude and phase distortions are not improved by the same proportion since the

bandwidth required for the envelope and phase paths are different and as a result, the overall performances is poor.

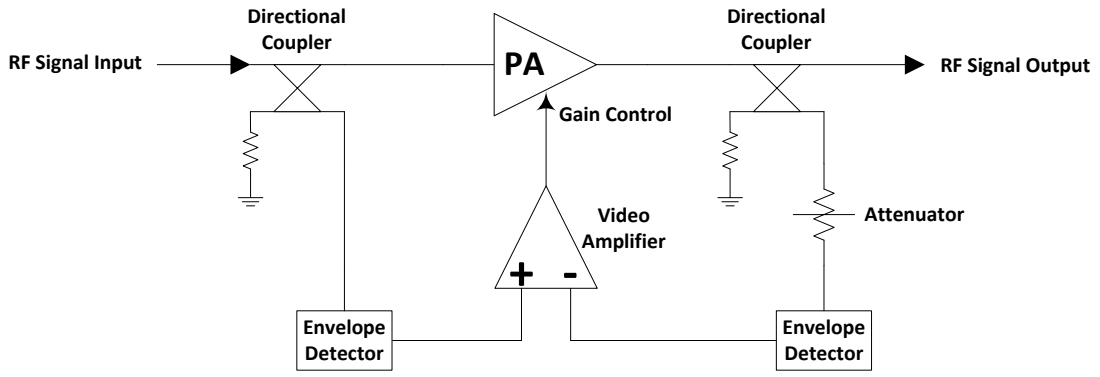


Figure 3.6: Typical Feedback Linearizer System.

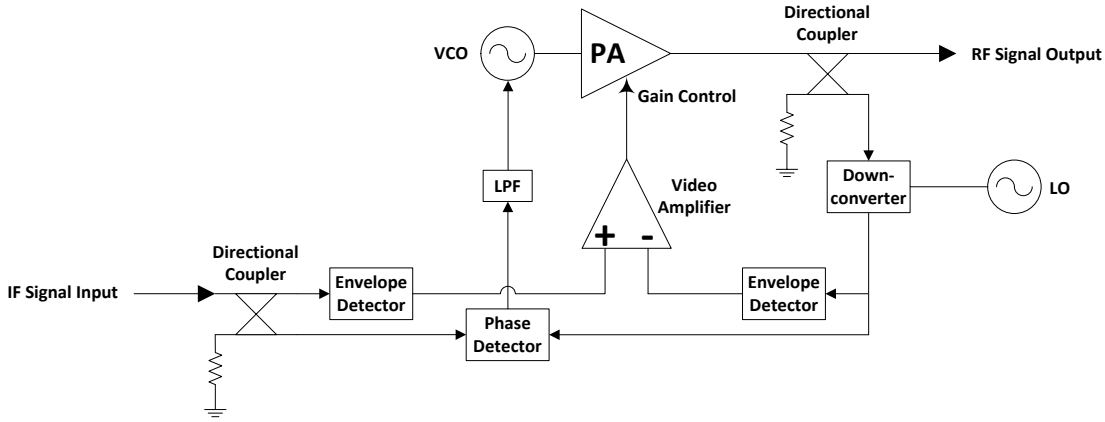


Figure 3.7: Polar-Loop Feedback System.

Cartesian feedback, shown in Figure 3.8, is another approach to feedback linearization technique. Since modern transmitters generate the baseband signal in the form of in-phase

and quadrature (I and Q) components, it is more suitable to use them in the feedback paths. The Cartesian feedback comprises two identical feedback loops working independently on the I and Q components. As the signals comparison occurs at baseband, this architecture contains quadrature modulator and demodulator to up-convert and down-convert the waveform components. Inherently, the Cartesian-feedback technique overcomes the problems associated with the bandwidth difference of the signal envelope and phase, unlike polar-loop feedback.

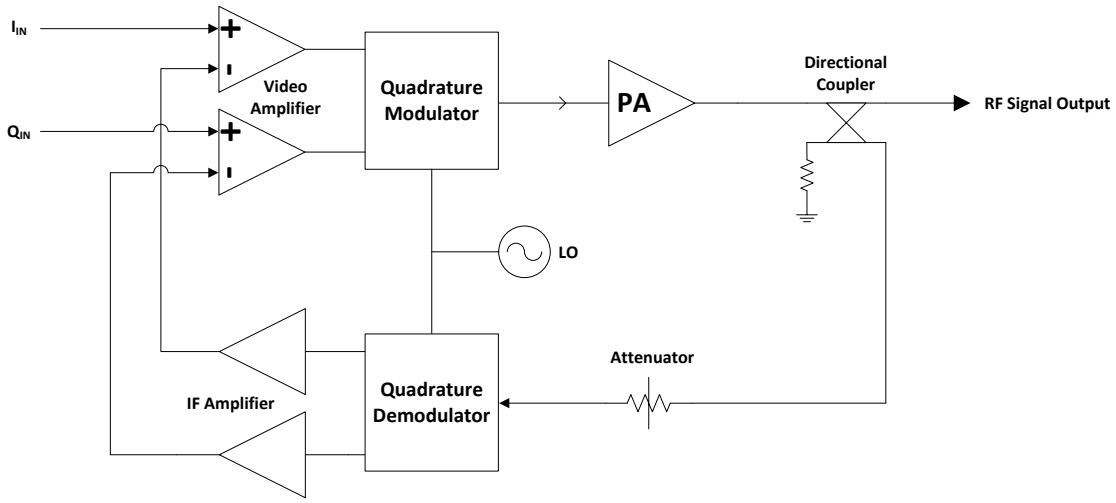


Figure 3.8: Cartesian-Loop Feedback System.

3.3.3 Predistortion Technique

The idea of predistortion technique is to shape the PA input signal in a way that when it is fed into the PA the output become linear. That modified signal is usually called a predistorted signal. The concept is illustrated further in Figure 3.9. Predistortion can be applied to the PA input signal either at RF, called the RF or analog predistortion, or at baseband, referred to as digital predistortion (DPD). In RF predistortion, the predistorted signal is created using nonlinear components such as diodes and then its gain and phase are modified to match those of the PA. However, in the DPD technique, the predistorted signal is created in two steps; the first step consists of modeling the PA, as explained in

the previous chapter, and the second step is to generate a signal which has an inverse characteristic of the PA.

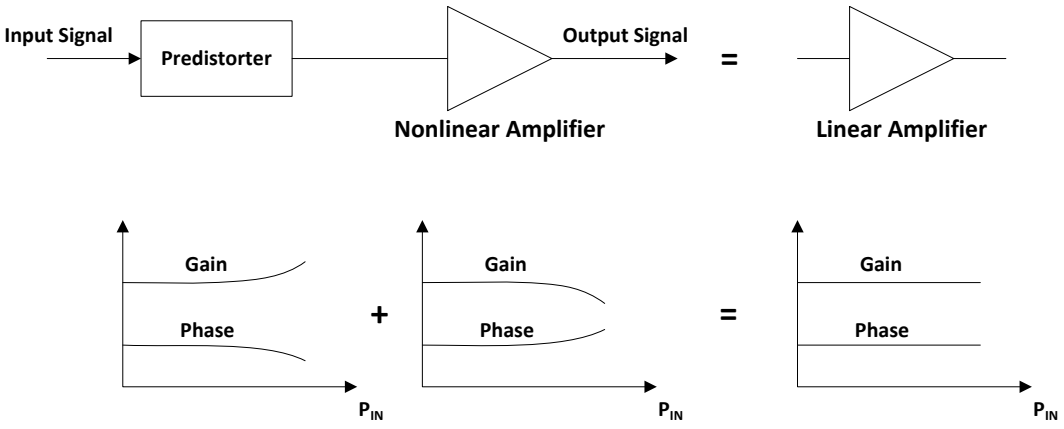


Figure 3.9: Predistortion Technique Principle.

Predistortion technique has several advantages. It is not conceptually complex. Predistortion technique does not have a stability issue as is seen with the feedback technique. Furthermore, the overall efficiency of the predistortion system is close to the PA efficiency since the power consumption of the predistortion circuit is insignificant, unlike the feedforward linearizer.

Predistortion technique has some drawbacks, however. Predistorters are optimized for predetermined PA conditions (e.g., power level, bandwidth, modulation type), and they are unlikely to continue performing well when these conditions change. Furthermore, DPD depends on a good modeling of the PA, which is not an easy task.

Due to the large number of predistortion technique variations presented in the literature, the discussion here will be limited to digital predistortion techniques only. These are most relevant to the work undertaken here.

3.4 Digital Predistortion Technique

DPD techniques are classified based on the PA behavioral model used to determine the predistortion function. Hence, two categories can be distinguished; DPD without memory effects, called memoryless DPD, and DPD that considers memory effects, or memory DPD. Both types are described in the sections that follow.

3.4.1 Memoryless Digital Predistortion

Look-Up Table Digital Predistortion

As its name indicates, the look-up table DPD (LUT DPD) consists of saving the inverse model values of the PA inside a memory and using these values to create the predistorted signal. The process is very simple: it consists of providing an output value for a corresponding input value.

The two main architectures of LUT DPD are mapping LUT[5] and gain-based LUT[6]. The mapping LUT process utilizes two separate look-up tables to map the input I and Q components onto predistorted ones. This method is simple to implement but it requires a significant storage capacity since many I and Q values should be addressed. The principle of the mapping LUT is illustrated in Figure 3.10.

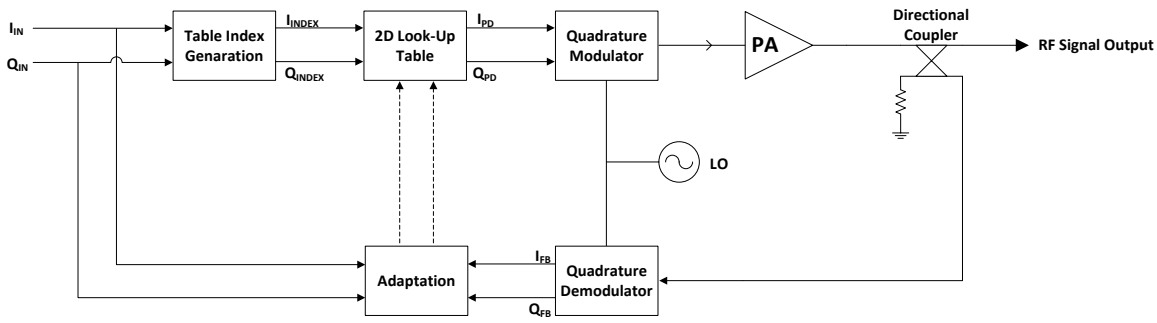


Figure 3.10: Mapping Look-Up Table.

The gain-based LUT combines the information required to distort the I and Q components into one table by using the signal envelope as an index. Therefore, the LUT contains

the complex gain based on the PA model. Inherently, this technique is simpler than the mapping LUT and requires less memory. The principle of the gain-based LUT is illustrated in Figure 3.11.

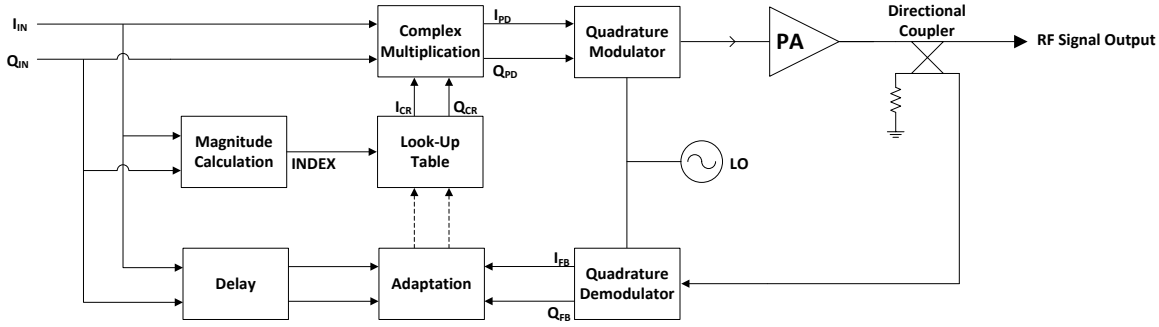


Figure 3.11: Gain-Based Look-Up Table.

Memoryless Polynomial Digital Predistortion

Polynomial functions are widely used to characterize nonlinear systems. The memoryless polynomial model is a polynomial formulation that relates the input and output signals of the PA. The following equation represents this relationship:

$$y(n) = \sum_{i=1}^{N} a_i x(n) |x(n)|^{i-1} \tag{3.2}$$

where $x(n)$ and $y(n)$ are the discretized input and output of the PA, respectively; a_i is the complex coefficient corresponding to the i^{th} power; and, N is the highest order of the memoryless polynomial model.

The identification of the memoryless model coefficients, a_i, is achieved using the least square estimate (LSE) algorithm, because the system can be written in a linear way. For a given signal sequence of length M, the preceding equation can be simplified to the following equation:

$$Y = X \cdot A \tag{3.3}$$

where

$$\begin{aligned} Y &= [y(n)\, y(n-1) \cdots y(n-(M-1))]^T \\ X &= \begin{bmatrix} x(n) & \cdots & x(n)|x(n)|^{N-1} \\ x(n-1) & \cdots & x(n-1)|x(n-1)|^{N-1} \\ \vdots & \ddots & \vdots \\ x(n-(M-1)) & \cdots & x(n-(M-1))|x(n-(M-1))|^{N-1} \end{bmatrix} \\ \textit{and} \qquad A &= [a_1\, a_2 \cdots a_N]^T \end{aligned}$$

The coefficients of the memoryless polynomial can then be calculated using pseudo-inversion, as shown in the following equation:

$$A = pinv(X) \cdot Y \tag{3.4}$$

with $pinv(.)$ is the pseudo-inverse of a matrix.

When implemented, the complex coefficients are usually split into two sets; amplitude and phase[32] or real and imaginary.

3.4.2 Digital Predistortion with Memory

Volterra Based Digital Predistortion

The Volterra series is considered one of the most complete nonlinear modeling schemes for the characterization of systems with dynamic nonlinearity such as a PA with memory effects. Indeed, they are generic models that can be used to model any random nonlinear system.

The formulation relating the input and output of the nonlinear system was proposed by the mathematician Vito Volterra early in the 20th century[7, 8], in the form:

$$\begin{aligned} y(t) &= \int_0^\infty h_1(\tau_1)x(t-\tau_1)d\tau_1 + \int_0^\infty \int_0^\infty h_2(\tau_1,\tau_2)x(t-\tau_1)x(t-\tau_2)d\tau_1 d\tau_1 + \cdots \\ &= \sum_{n=1}^{\infty} \left[\int_0^\infty \cdots \int_0^\infty h_n(\tau_1, \cdots \tau_n) \prod_{j=1}^{n} x(t-\tau_j) d\tau_j \right] \end{aligned} \tag{3.5}$$

Where $x(t)$ and $y(t)$ are the input and the output of the system, respectively, and h_n, $1 < n < \infty$ are the functions that generalize the transfer functions of the system, usually referred to as Volterra kernels.

The first term in the above formulation represents the linear term while subsequent terms represent the nonlinear ones. As can be seen in this formulation, the output consists of an infinite number of terms of increasing order; each term is the infinite sum of all contributions due to the input signal multiplied by itself n times, where n is the order of the term, in any possible combination of time instants in the past, weighted by the Volterra kernel.

For discrete signals, the formulation of Volterra series is in the form:

$$\begin{aligned} y(n) &= \sum_{q_1=0}^{\infty} h_1(q_1)x(n-q_1) + \sum_{q_1=0}^{\infty}\sum_{q_2=0}^{\infty} h_2(q_1,q_2)x(n-q_1)x(n-q_2) \\ &\quad + \sum_{q_1=0}^{\infty}\cdots\sum_{q_P=0}^{\infty} h_P(q_1,\cdots q_P)x(n-q_1)\cdots x(n-q_P) \end{aligned} \tag{3.6}$$

where P is the Volterra series order.

The extraction of kernels of high order is very complex. Therefore, many simplified models have been derived from this model, such as the memory polynomial model detailed in the next section.

Memory Polynomial Digital Predistortion

The memory polynomial (MP) model, proposed by Kim *et al*[9], is considered to be the standard for models with memory in the literature. The MP model is a derivation of the Volterra model that excludes the cross terms from the Volterra series. MP is expressed as follows:

$$y(n) = \sum_{j=0}^{M-1}\sum_{i=1}^{N} a_{i,j}x(n-j)\left|x(n-j)\right|^{i-1} \tag{3.7}$$

where $x(n)$ and $y(n)$ are the discretized input and output of the PA, respectively; $a_{i,j}$ is the complex coefficient corresponding to the i^{th} power and the j^{th} delayed sample; N is the highest order of the MP model; and, M is the memory depth.

A representation of the MP model is shown in Figure 3.12. The first branch resembles the memoryless polynomial model, since there is no delay introduced; the remaining branches symbolize the memory components.

As was done with the memoryless polynomial model, the MP model can be written in a linear system in order to be solved using the LSE algorithm.

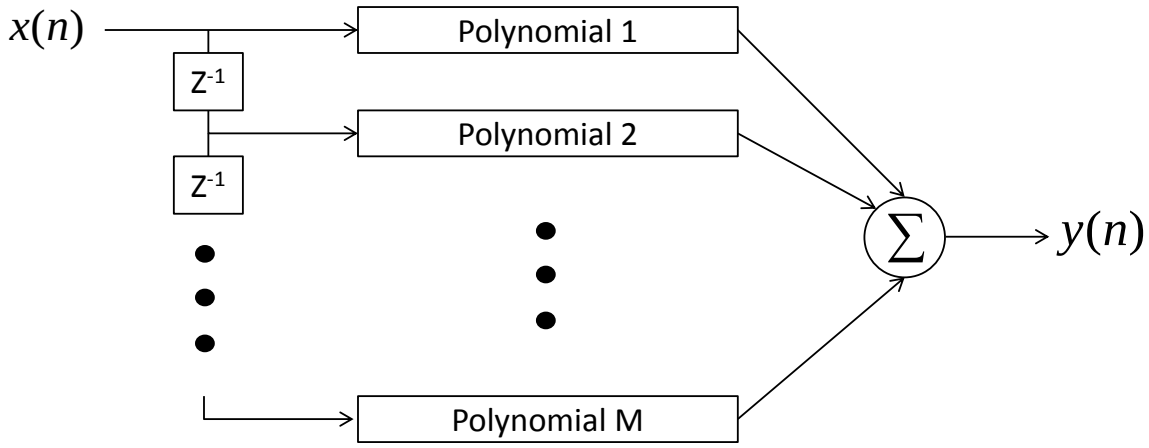


Figure 3.12: Memory Polynomial Structure.

If we consider a new quantity, $u_{i,j}(n)$, such as:

$$u_{i,j}(n) = x(n-j)\,|x(n-j)|^{i-1} \tag{3.8}$$

The MP equation (Equation 3.7) can be simplified to:

$$Y = U \cdot A \tag{3.9}$$

where

$$\begin{aligned} Y &= [y(n)\, y(n-1) \cdots y(n-(P-1))]^T \\ U &= [u_{1,0} \ \cdots \ u_{N,0} \ \cdots \ u_{1,M-1} \ \cdots \ u_{N,M-1}] \\ u_{i,j} &= [u_{i,j}(n)\, u_{i,j}(n-1) \ \cdots \ u_{i,j}(n-(P-1))]^T \end{aligned}$$

and

$$A = [a_{1,0} \ \cdots \ a_{N,0} \ \cdots \ a_{1,M-1} \ \cdots \ a_{N,M-1}]^T$$

where P is the identification sequence length.

Consequently, the solution of that system is provided in Equation 3.9:

$$A = pinv(U) \cdot Y \tag{3.10}$$

The MP model is, therefore, an extension of the memoryless polynomial model and with the addition of past components it is also considered a reduction of the Volterra series.

The relatively small number of coefficients and low complexity have made the MP model very attractive. Yet, the identification step is very demanding in terms of computation given the LSE algorithm is used.

3.5 Conclusion

This chapter considered many techniques for PA efficiency enhancement and linearization. These techniques are sometimes combined together for the goal of achieving the highest performance allowable by a PA. The choice of the appropriate technique to be implemented will depend on the application. For targeted applications, which include mobile communication infrastructure, Doherty PA combined with DPD is the best mixture. Doherty PA is suitable for RF frequency unlike other efficiency enhancement techniques and DPD can linearize wider bandwidth given the advances in signal converters and DSP.

Chapter 4

Multimode Radio Development Platform

4.1 Introduction

The multimode radio development platform presented in this chapter was developed to allow for i) the synthesis and generation of multimode signals, ii) the acquisition and analysis of the feedback signals, iii) the synthesis of two programmable and phase-coherent continuous waves, and iv) the application of advanced digital signal processing (DSP) algorithms, namely digital predistortion (DPD) techniques, to enhance the radio system's performance.

The literature on the topic of DPD has focused on innovating or improving the predistortion algorithms [10, 11, 33–38] rather than looking at the implementation of the DPD itself. The realisation of DPD in an environment where the testing, and measurements, are performed using commercial laboratory equipment and high precision computations, has been studied more. Traditionally, conventional linearization test bed, as shown in Figure 4.1, comprises a main component responsible for generating a test signal (stimulus), capturing the response of the PA and performing all of the signal processing schemes such as the PA model extraction, parameters estimation and the construction of the predistorted waveform. The signal processing functions are always performed on a computer with the help of CAD tools. The test bed also includes two blocks for transforming the baseband waveform into a RF signal and vice-versa, usually achieved by a signal generator and spectrum analyzer. However, the development platform presented here was designed to take

into account the challenges associated with real hardware, such as limited resources and the lack of floating-point arithmetic.

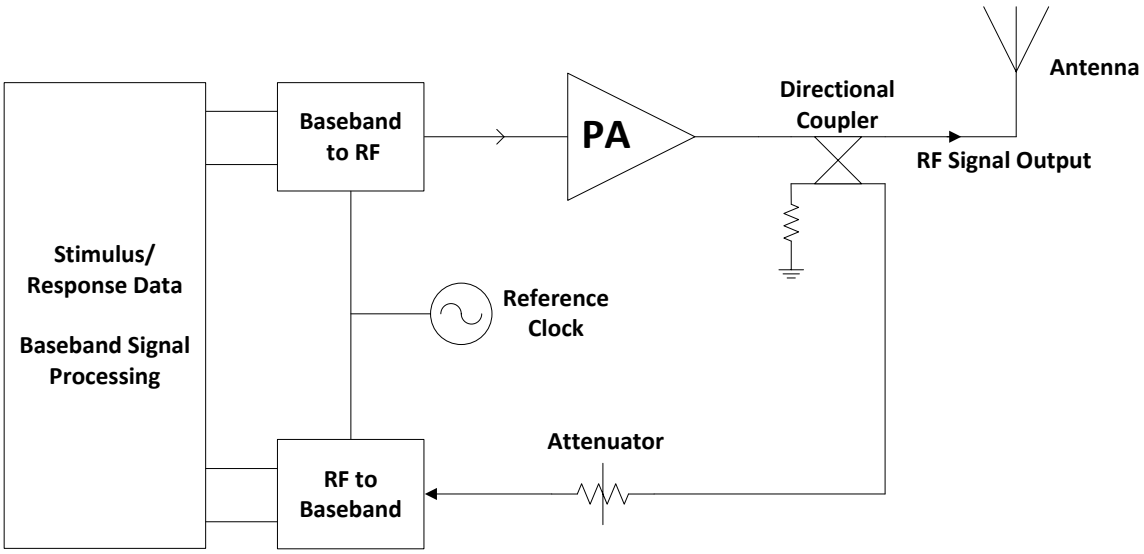


Figure 4.1: Conventional Test Bed Diagram.

In this chapter, a description of this novel system, including its different components and its theory of operation, is presented. The proposed development platform design and implementation is discussed including the baseband transceiver implementation, the proposed phase-coherent frequency synthesizer, the DPD model implementation (LUT DPD, memoryless polynomial DPD and memory polynomial DPD) and the MATLAB dashboard used to control and monitor the system. A new technique was also used to calibrate the frequency response of the feedback-receiver to improve the wideband performance. Finally, the measurement results of the DPD linearization models are reported.

4.2 System Overview and Theory of Operation

The system hardware consists of several components: a field-programmable gate array (FPGA) which allows reprogrammability of the baseband transceiver and execution of the DSP algorithms; a signal conversion stage for analog-to-digital conversion and vice-versa;

an RF front-end for filtering, frequency translation, signal amplification and attenuation; and a host computer (PC) to control the hardware and software.

The signal conversion stage and the RF front-end consist of an Analog Devices' Mixed-Signal Digital Pre-Distortion System Board (MSDPD) and a PA. This MSDPD development board utilizes a direct conversion architecture transmitter with a complex intermediate frequency (IF). It consists of a dual digital-to-analog converter (DAC) (AD9122) with a maximum speed of 1.2GSPS, followed by a wideband quadrature modulator (ADL5375), a bandpass filter to remove unwanted signals and a variable gain amplifier (VGA) stage which provides 12dB of gain control. The MSDPD includes a feedback path (called also an observation path) which implements a digital-IF receiver. Through this receiver, the received signal is filtered, attenuated, downconverted to an IF frequency, amplified with an IF VGA and then digitized by an analog to digital converter (ADC) with a maximum speed of 250MSPS[39]. A full diagram of the system is shown in Figure 4.2.

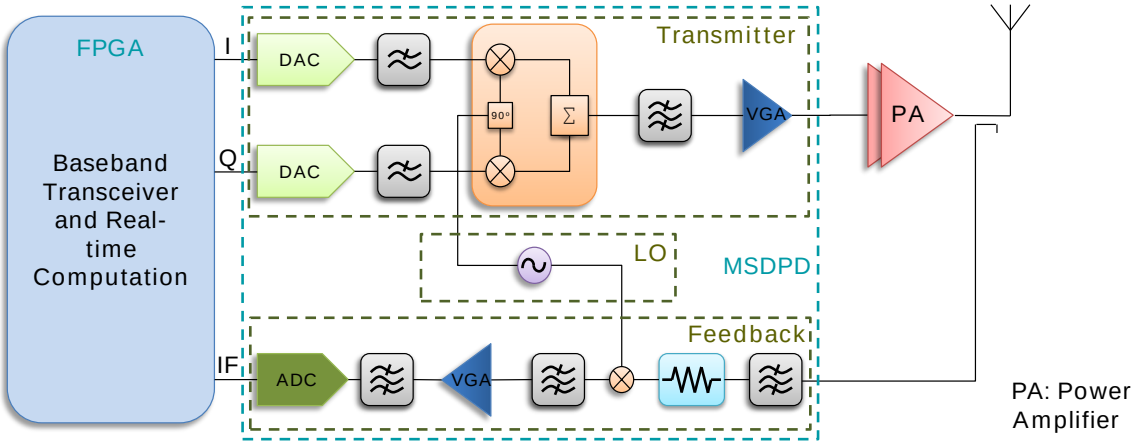
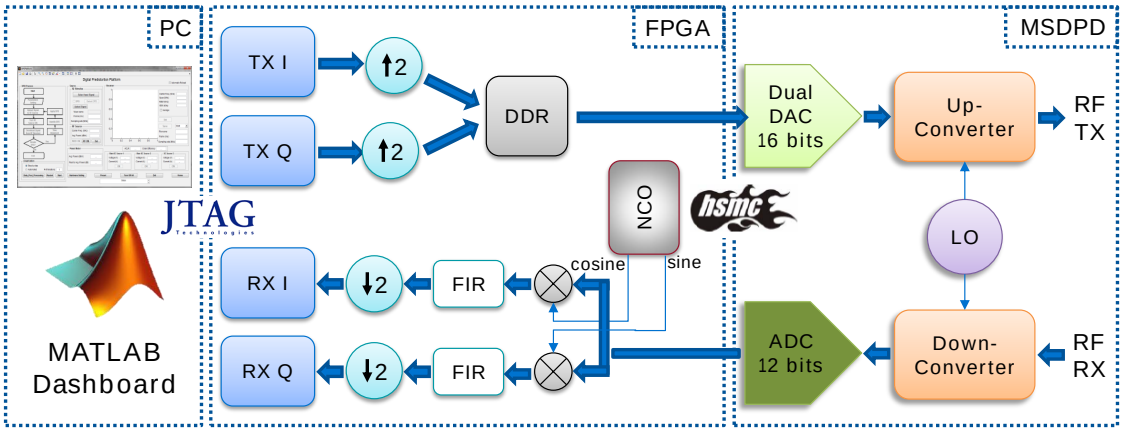


Figure 4.2: Multimode Transmitter and Feedback Receiver Diagram.

The combination of a MATLAB dashboard linked to a FPGA, a flexible RF transmitter and feedback receiver allows for the generation and acquisition of multimode signals. The dual DAC is used to convert the digital I and Q components into analog waveform components, which are subsequently up-converted to RF and filtered before being fed through a VGA.

The feedback path implements the reverse procedure. A sample of the transmitter/PA output signal is filtered, down-converted to an IF, passed through a VGA, and subsequently digitized through the ADC. Various parameters of the transmitter and feedback paths, such

as bandwidth and gains, can be adjusted based on the desired mode of operation via a USB link with the MATLAB dashboard. A PA may also be connected to the output of the transmitter. Such a set-up allows for a realistic testing environment for different DPD schemes.



DDR: Double-Data Rate
NCO: Numerically-Controlled Oscillator
FIR: Finite- Response Filter
HSMC: High-Speed Mezzanine Connector
JTAG: Joint Test Action Group

Figure 4.3: Detailed Representation of the Multimode Transmitter and Feedback Receiver.

While the MSDPD is comprised of the analog side of the system, an FPGA provides the link between the transceiver and the MATLAB dashboard, as shown in Figure 4.3. The dashboard uses a JTAG interface to program and configure the FPGA, based on the desired preprocessing needs, upload waveforms to be synthesized and download waveforms that are received.

The FPGA generates the I and Q components of the signal, digitally predistorts these components according to the programmed scheme, and uploads them to the transceiver via Altera's High-Speed Mezzanine Connector (HSMC). Waveforms received from the feedback's ADC are digitally demodulated from an IF to recover their I and Q components. The received waveforms are then made available to the MATLAB dashboard for viewing and further post-processing.

4.3 Development Platform Design and Implementation

4.3.1 Baseband Transceiver Implementation

In order to accommodate the MSDPD with an adequate signal, the FPGA transmitter has to have a suitable architecture. The clock generated by the MSDPD-EVB was utilized to feed a PLL inside the FPGA. Thus, the FPGA transmitter and the DAC are synchronized together. The PLL is then used to clock the two random access memory (RAM) blocks containing the I and Q components. Since the DAC works in double data-rate (DDR) mode, the data provided has to be converted; therefore, the I component is sent during the high clock cycle and the Q component is sent during the low clock cycle.

Figure 4.4 shows the architecture of the transmitter implemented in the FPGA and how it interfaces with the MSDPD-EVB.

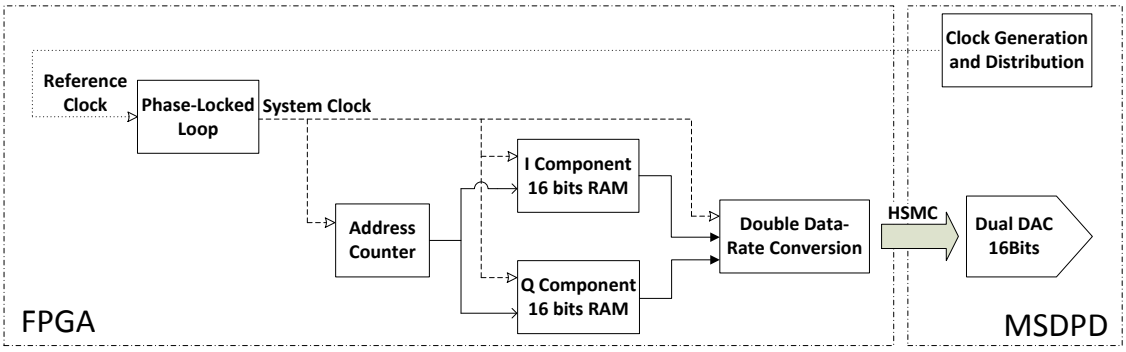


Figure 4.4: Basic Baseband Transmitter Architecture.

The above baseband transmitter is a simplified version of the full transmitter. The full transmitter actually has the signal processing block on top of the simplified one. The signal processing block implemented was a predistortion component, detailed in following sections of this chapter, which transforms the waveform stored in the memory to another waveform that helps to linearize the PA as shown in the previous chapter. Its architecture is shown in Figure 4.5.

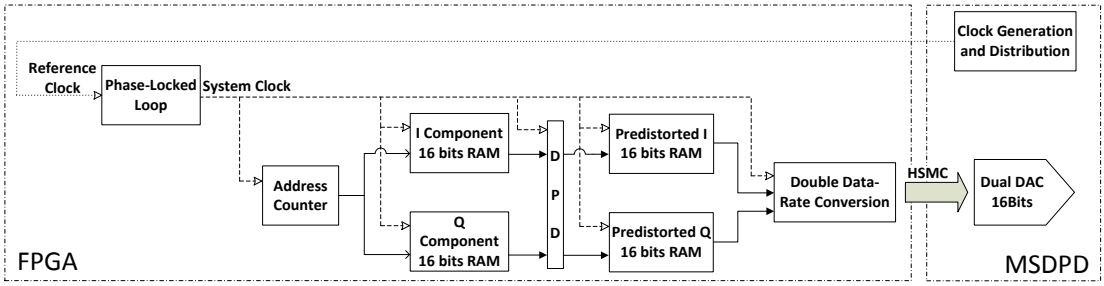


Figure 4.5: Advanced Baseband Transmitter Architecture.

For the receiving side, the MSDPD-EVB is providing the FPGA board with an IF signal. This signal should be demodulated in order to recover the I and Q components. The baseband-receiver PLL is clocked by the output clock of the ADC. The output clock of the PLL is then fed to a numerically controlled oscillator (NCO), which generates the sine and cosine waves to be used as the digital quadrature demodulator local oscillator (LO) input. After the down-conversion, high-frequency components are generated and need to be filtered out; a finite impulse response (FIR) filter is used for that purpose. Finally, the I and Q received waveform components are saved in memory blocks to be processed later.

Figure 4.6 presents the architecture of the implemented receiver and the interface with the MSDPD-EVB.

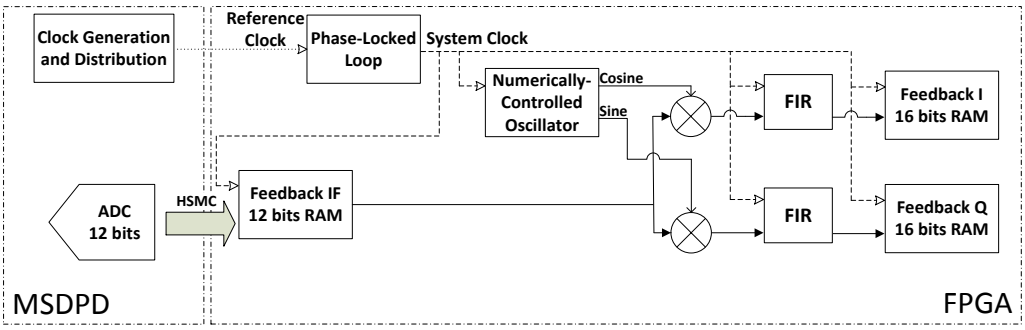


Figure 4.6: Baseband Receiver Architecture.

4.3.2 Phase Coherent Frequency Synthesizer

To extend the flexibility of the RF transmitter, a reprogrammable and phase-coherent synthesizer was designed. This component is used to separately control the LO frequency of the transmitter and the feedback, or to synthesize two phase-coherent sine waves to serve as two LOs in a dual-band transmitter topology.

Different architectures for a multimode, multi-band frequency synthesizer were examined. One option [40], is two dual-band 802.11 radios integrated on a single chip achieved by using a shared fractional-N synthesizer. However, this architecture does not guarantee that the two PLLs would be phase-coherent. In fact, Rogers et al. acknowledge that the use of common reference for the used PLLs does not avoid phase drift. However, additional chips can be introduced to a system by phase synchronizing the signal paths through a bidirectional LO porting scheme developed for this application. Other investigators have resorted to using the frequency divider to address the issue of multi-bands since it offers more options for the implementation of the frequency synthesizer[41, 42]. Unfortunately, this solution does not achieve the required frequencies. Another technique [43] makes use of a comb generator, based on a step-recovery diode, to generate the harmonics of an input signal. The required frequency is then filtered from the signal. However, the usage of the filters limits the flexibility of this type of frequency synthesizer.

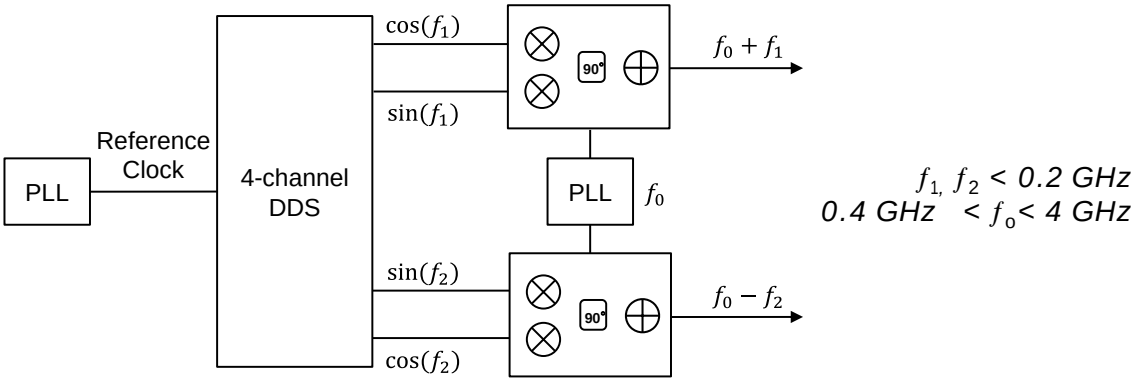


Figure 4.7: The Proposed Frequency Synthesizer Block Diagram.

The proposed frequency synthesizer combines two types of frequency synthesizers, PLL and direct digital synthesizer (DDS). In addition, the design is based on Hartley modulator architecture, which helps to remove one side of the generated bands after frequency con-

version. This allows versatility by making side-band elimination independent of frequency, which would not be possible with conventional filtering.

The frequency synthesizer block diagram is presented in Figure 4.7. The first PLL is used as a reference clock for the DDS with a value of 500 MHz, which is the maximum frequency of the DDS used. Each DDS channel pair was chosen to have a phase shift of 90 ° to feed the quadrature modulator as an IF component, which is used to offset the frequency of the LO set by the second PLL. The PLLs and the quadrature modulator used in this design are wideband components to allow for greater flexibility of the output frequency.

As can be seen in Figure 4.7, only the upper side-band component is kept for the first modulator, as opposed to the second modulator, where only the lower side band is kept. Hence, the two output frequencies can be separated by twice the maximum frequency of the DDS, which is 200 MHz (for a 400 MHz separation).

Since the DDS channels are synchronized and fed by the same reference clock, their output is inherently phase-coherent. After multiplying them by the same LO, the final outputs are also phase-coherent.

The synthesizer was validated through measurements, reported in Figure 4.8, which show that by making fine changes in the DDS output channel phase and magnitude, the lower side-band was suppressed by 50 dB and only one side was kept.

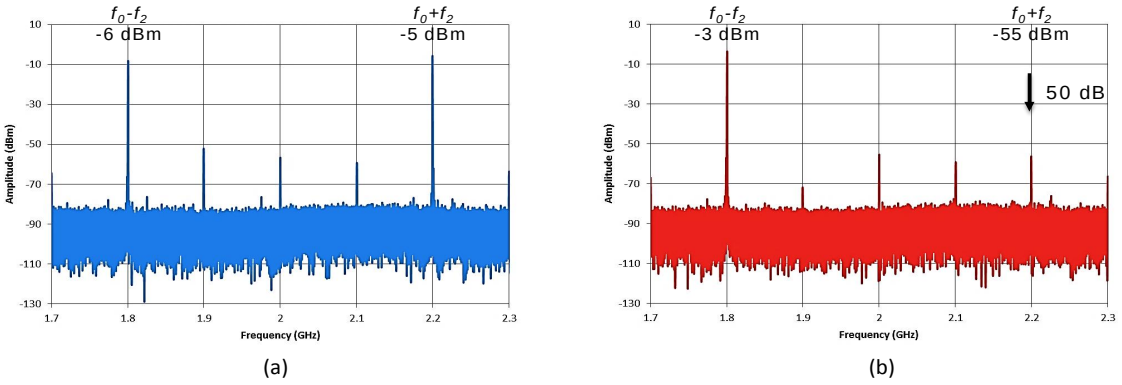


Figure 4.8: Spectrum of the Modulator Output: (a) Before and (b) After Side Channel Suppression for the Lower Frequency output ($f_0 - f_2$).

4.3.3 Memoryless Digital Predistortion Implementation

Look-Up Table Digital Predistortion Implementation

As explained in Chapter 3, the LUT DPD model uses a gain response for different input power levels to predistort the signal. The implementation is well addressed in the literature[44–47] and it was performed here as a step of familiarization with the platform. The LUT entries were coded using 18-bit fixed-point representation (one sign bit, two decimal bits and the rest for fractional bits); this range covers the typical compression of the PA. Moreover, the address for each entry, which represents the power of the input signal, was coded using 16 bits which maintain good resolution as the step is small. Consequently, the number of entries in the LUT was equal to 2^{16}.

The structure of the implemented LUT DPD is shown in Figure 4.9. The I and Q waveform components were first squared and then added together in order to get the signal input power. The obtained value was used as an index for the LUT. The next step was the multiplication of the input signal components by the respective predistortion complex gain. Only the 18 most significant bits (MSB) were kept. Before uploading the signal to the MSDPD-EVB, the predistorted 18-bit signal was normalized by a factor, α, to accommodate the 16 fractional signed bits required at the input of the DAC, where α is given by the following expression:

$$\alpha = \frac{1}{\sqrt{G_I^2 + G_Q^2}} \tag{4.1}$$

where G_I and G_Q are the real and imaginary gains, respectively, of the peak input power deduced from the LUT values.

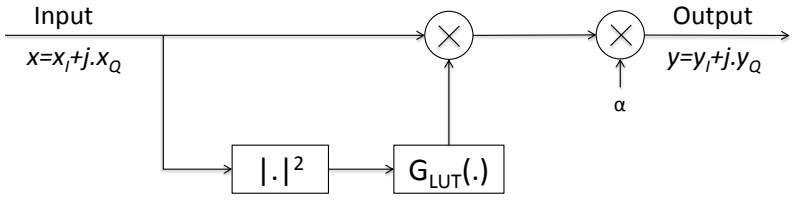


Figure 4.9: Structure of the Implemented LUT DPD.

The performance of this implementation is presented in the results section of this chapter and is compared to the memoryless polynomial implementation detailed in the next section.

Memoryless Digital Predistortion Implementation

As explained previously, memoryless polynomial models are good approximators for nonlinear functions. Unlike LUTs, when applied to PA behavioral modeling or DPD, memoryless polynomial model do not require a large memory size to store the different gains for different input signal powers to accurately approximate the predistorted function.

The memoryless polynomial model is a good alternative to LUT models with low number of coefficients. However, one major problem of the memoryless polynomial implementation when using fixed point arithmetic, such as in a FPGA, is that preservation of the resolution is not trivial, as it is in the LUT case. Indeed, recall that every multiplication in Equation 3.2 doubles the number of required bits to preserve the initial resolution; as N gets higher the required number of bits to preserve the computation resolution gets very large. This issue was overwhelmed through a new reformulation of the memoryless polynomial model proposed in [48] and detailed below.

The identification of the coefficients of Equation 3.2 is performed using samples of the input and output signals of the device under test (DUT) and the least square error (LSE) algorithm. Usually, a high-order polynomial is required to fit the input and output signals of the DUT with good accuracy. This leads to high accumulative error inside the FPGA, if the polynomial is implemented as shown in Equation 3.2.

The issue of successive multiplication of the absolute value of the input was tackled using Horner's rule with a reformulation of Equation 3.2 as shown in Equation 4.2. The formulation in Equation 4.2 limits the number of consecutive multiplications to a maximum of two, leading to a reduced number of bits at the output of the memoryless polynomial to preserve the precision of the computation.

$$y(n) = x(n)\left(a_1 + \left(|x(n)|\left(a_2 + \cdots + \left(|x(n)|\left(a_{n-1} + a_n|x(n)|\right)\right)\right)\right)\right) \tag{4.2}$$

Moreover, the large variation in magnitude of the polynomial coefficients is dealt with by taking the ratios of adjacent coefficients when further factorizing the Equation 4.2 as follows:

$$y(n) = a_1 x(n)\left(1 + \left(\frac{a_2}{a_1}|x(n)|\left(\cdots 1 + \left(\frac{a_{n-1}}{a_{n-2}}|x(n)|\left(1 + \frac{a_n}{a_{n-1}}|x(n)|\right)\right)\right)\right)\right) \tag{4.3}$$

It can be remarked that the ratios of the coefficients were used instead of the coefficients themselves. In essence, the coefficients were rescaled. In fact, the range of the coefficients

was reduced from 10^8 to 10^2, for a nonlinearity order of 9, which is a good improvement since that range requires only 7 decimal bits to be represented.

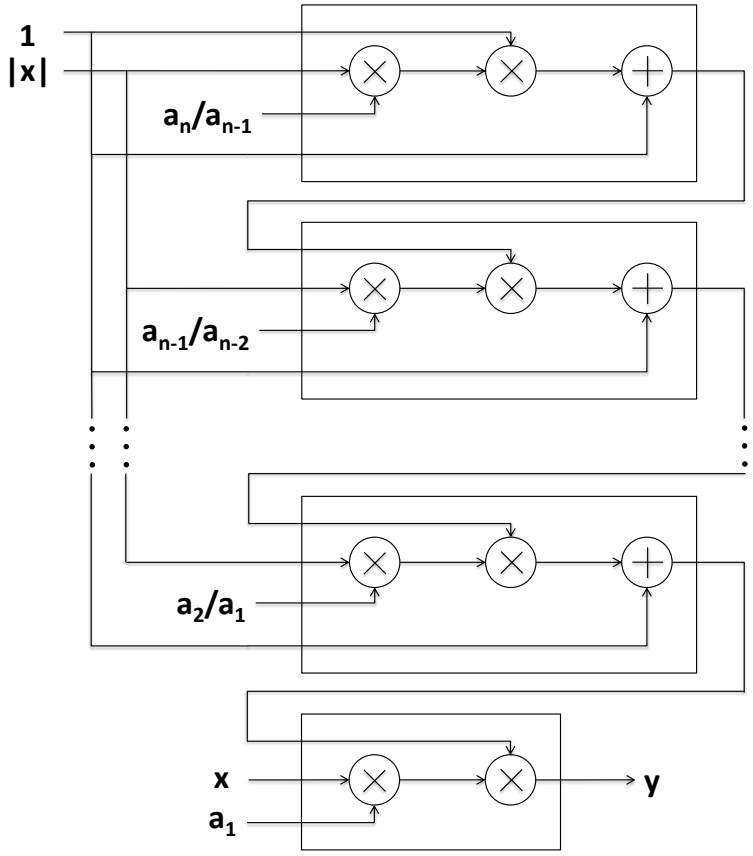


Figure 4.10: Structure of the Implemented Memoryless Polynomial DPD.

Figure 4.10 shows a block diagram of the equivalent memoryless polynomial model (Equation 4.3) inside the FPGA. It is clear that a replica of one common block was needed to implement the full memoryless model of Equation 4.3 with the exception of the last block. These manipulations allow for a reduced number of bits required for the implementation of Equation 3.2, while keeping a high accuracy in its computation.

4.3.4 Memory Polynomial Digital Predistortion Implementation

The implementation of this model was based on the memoryless polynomial structure. Figure 4.11 shows a block diagram of the implemented model where the memory depth was fixed to 5 and the highest polynomial order was 9.

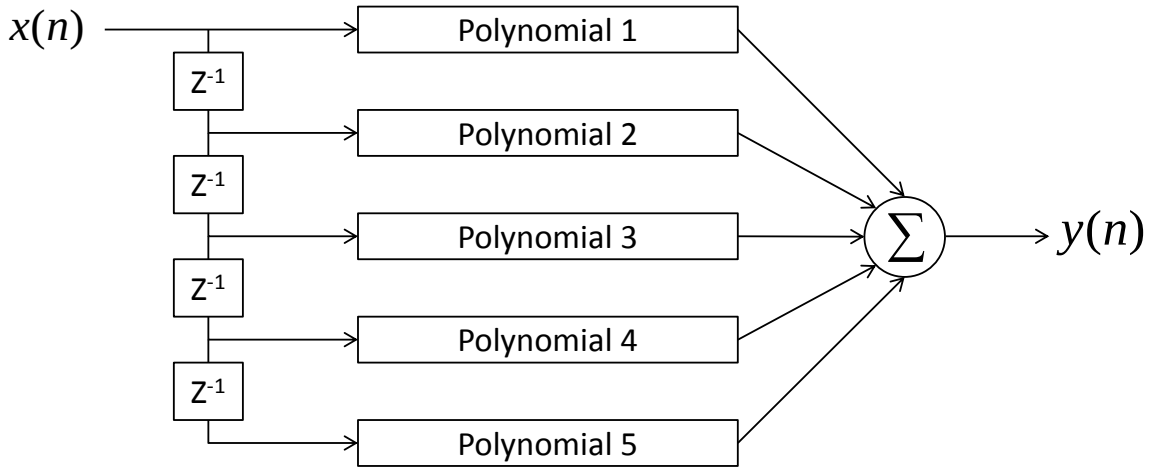


Figure 4.11: Structure of the Implemented Memory Polynomial DPD.

The first branch represents the memoryless polynomial; and, a delay was introduced before each of the other branches, in order to construct the MP model. The delay was performed using a flip-flop D latch. At the end, the output was rescaled in order to provide suitable input to the DAC. The results of the MP implementation, along with those of the LUT and memoryless polynomial models, are presented in the last section of this chapter.

4.3.5 Mixed Signal Multimode Dashboard

The mixed-signal multimode dashboard is a multifunctional and evolving interface that allows for seamless control of the platform and execution of the required pre-processing and post-processing algorithms. These algorithms can be implemented in the software (MATLAB), on the hardware (FPGA), or can be a combination of the two.

The dashboard has a built-in computer-based graphical user interface (GUI) through which the user can control lab equipment or an FPGA development kit. For example,

Figure 4.12 illustrates the dashboard developed for the purpose of implementing a DPD module. This module of the GUI performs the different steps required for automatically characterizing and linearizing an RF PA.

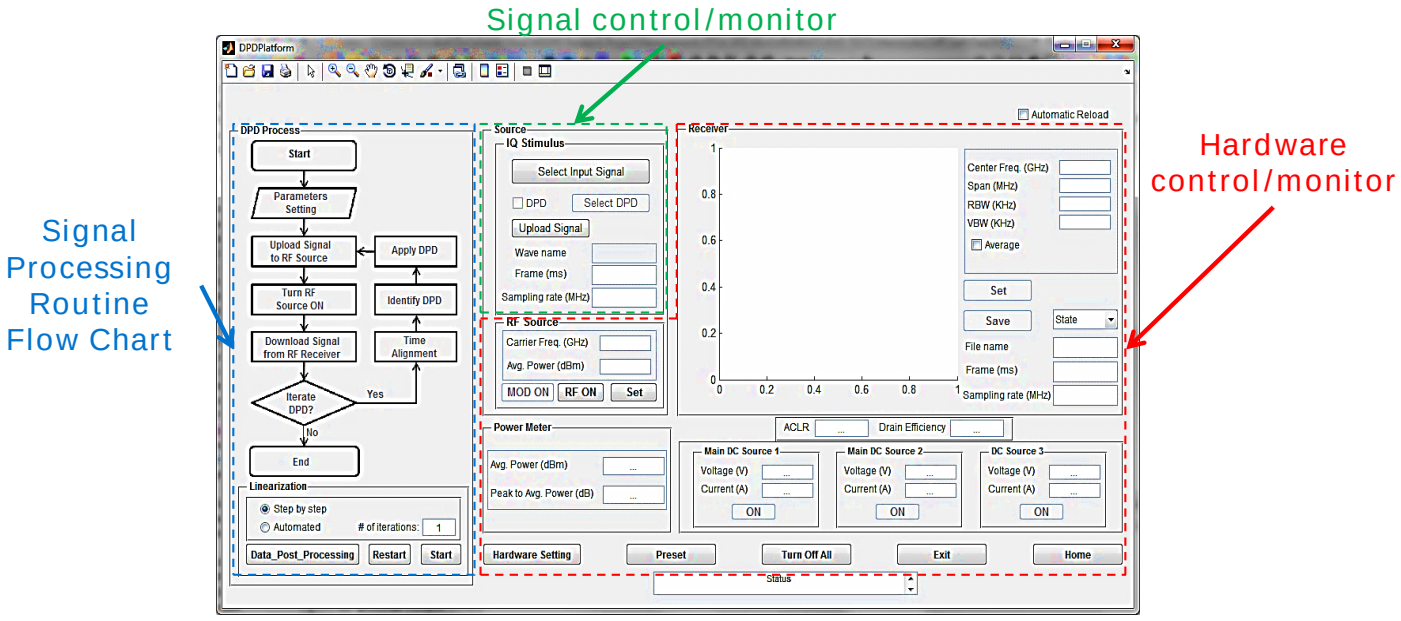


Figure 4.12: Mixed Signal Multimode Dashboard.

The dashboard guides the user through the steps of uploading the signal, controlling and monitoring the relevant equipment, choosing the model parameters and so forth. As such, the software provides the tools and signal processing algorithms necessary for:

- Signal timing analysis: Delay adjustment, offset alignment, etc.
- Signal pre-distortion: Computation of DPD parameters for a variety of DPD schemes and creation of the pre-distorted waveform.
- Data post-processing: Calculation of EVM and ACLR, among others.

On the hardware side, the dashboard is directly linked to an FPGA board, on which various DPD schemes are hardware implemented as previously discussed. The control and

programming of the FPGA are done through a JTAG interface, allowing the user to load and download waveforms, program DPD implementations, etc. On the analog front-end, the dashboard is used to modify and fine-tune various parameters such as the frequency and the power level.

4.4 Feedback-Receiver Calibration

For successful linearization of the PA, the transceiver hardware should be first calibrated for a linear response. Wisell and Händel proposed a method to de-embed the transmitter and receiver amplitude frequency ripples[49] in order to separately correct for them. This technique stimulates the receiver with multi-tones with known initial phases and uniform frequency spacing. Three different measurements were performed to deduce the frequency response of the transmitter and the receiver. First, data were collected where the transmitter and feedback receiver carrier frequencies were the same. For the second and third measurements, data were collected when the transmitter carrier frequency was kept fixed and the feedback receiver carrier frequency was shifted positively and negatively, respectively, with a value equal to the tone spacing. All the data recorded were used to separately determine the transmitter and the receiver ripples[49].

Before explaining the principle of the method used, there are some definitions that should be presented. Let assume that we have a linear system with a transfer function, H. The amplitude ripple of that system over a certain frequency range is defined as:

$$R_A(\omega) = \frac{|H(\omega)|}{G}, \qquad \omega_{start} \leq \omega \leq \omega_{stop} \tag{4.4}$$

where

$$G = \frac{\max_\omega |H(\omega)| + \min_\omega |H(\omega)|}{2}$$

Equation4.4 is illustrated in Figure 4.13 below.

This method is divided into two steps: the first step consists of determining the amplitude ripple of the whole system; the second step consists of separating the amplitude ripple of the two cascaded systems.

The stimulus signal is a M tone complex-valued signal, where M is an even integer so that the tones are equally distributed around the center frequency. The complex envelope of the signal is given by the following equation:

$$u(n) = \frac{1}{M} \sum_{k=0}^{M-1} e^{j(\omega_k n + \phi_k)}, \qquad n = 0, 1, \cdots, N-1 \tag{4.5}$$

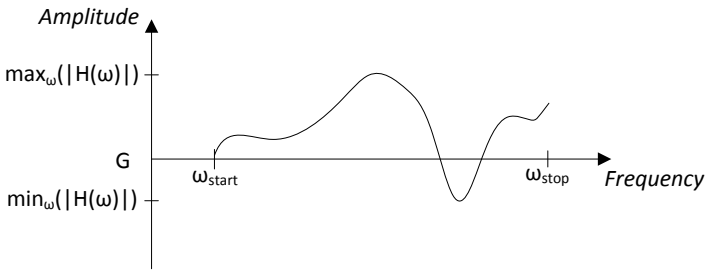


Figure 4.13: Amplitude Ripple.

where ϕ_k are the initial phases of the tones; $\omega_k = (2k - (M-1))\omega_d$, ω_k and ω_d are the normalized angular frequencies; and, $\omega_d = \frac{2\pi F_d}{F_s}$, where F_s is the sampling frequency and F_d is a half separation of the tones.

After passing through the system the output signal is given by:

$$y(n) = \frac{1}{M} \sum_{k=0}^{M-1} H(\omega_k) e^{j(\omega_k n + \phi_k + \omega_k \tau + \alpha)} + w(n) \tag{4.6}$$

where α is the phase difference between the transmitter and the receiver, τ is the delay between the sent and received signal, and w is the additive noise.

Let us assume that

$$H(\omega) = |H(\omega)| e^{j \angle H(\omega)} \tag{4.7}$$

$$\theta_k = |H(\omega)| e^{j(\phi_k + \omega_k \tau + \alpha + \angle H(\omega))} \tag{4.8}$$

Thus, the output can be reduced to:

$$y(n) = \frac{1}{M} \sum_{k=0}^{M-1} \theta_k e^{j\omega_k n} + w(n) \tag{4.9}$$

Then, the Equation 4.9 can be written as follows:

$$Y = \frac{1}{M} V\theta + w \tag{4.10}$$

where

$$\begin{aligned} Y &= [y(0)\, y(1) \cdots y(N-1)]^T \\ \theta &= [\theta_0\, \theta_1 \cdots \theta_{N-1}]^T \\ w &= [w(0)\, w(1) \cdots w(N-1)]^T \end{aligned}$$

and V represents a matrix with a Vandermonde structure:

$$V = \begin{bmatrix} 1 & 1 & \dots & 1 \\ e^{j\omega_0} & e^{j\omega_1} & \dots & e^{j\omega_{M-1}} \\ \vdots & \vdots & \ddots & \vdots \\ e^{j\omega_0}(N-1) & e^{j\omega_1}(N-1) & \dots & e^{j\omega_{M-1}}(N-1) \end{bmatrix} \tag{4.11}$$

For $N \geq M$, the LSE algorithm gives an estimate of θ:

$$\theta = M \cdot pinv(V) \cdot Y \tag{4.12}$$

Hence, the amplitude ripple at each angular frequency is deduced from Equation 4.4:

$$R_A(\omega_k) = \frac{2|\theta_k|}{\max_k |\theta_k| + \min_k |\theta_k|} \tag{4.13}$$

After determination of the amplitude ripple of the cascaded systems, the amplitude ripple of each system can be extracted separately. The idea consists of making more measurements at different RF center frequencies to enlarge the equation system. For example, three different measurements can be made: one at a center frequency F_c, another one at $F_c + 2F_d$, and a third one at $F_c - 2F_d$. Figure 4.14 illustrates the measurement steps in more detail.

The transfer function of the transmitter and receiver is cascaded as

$$H(\omega) = H_1(\omega) \cdot H_2(\omega) \tag{4.14}$$

Then the ripple of the cascade is

$$R(\omega) = R_1(\omega) \cdot R_2(\omega) \tag{4.15}$$

Let R^0, R^+ and R^- be the ripples of the three measurements previously cited. Hence, the following system equation could be written

$$R^0(\omega_k) = R_1(\omega_k) \cdot R_2(\omega_k) \tag{4.16}$$

$$R^+(\omega_k) = R_1(\omega_k - 2\omega_d) \cdot R_2(\omega_k) \tag{4.17}$$

$$R^-(\omega_k) = R_1(\omega_k + 2\omega_d) \cdot R_2(\omega_k) \tag{4.18}$$

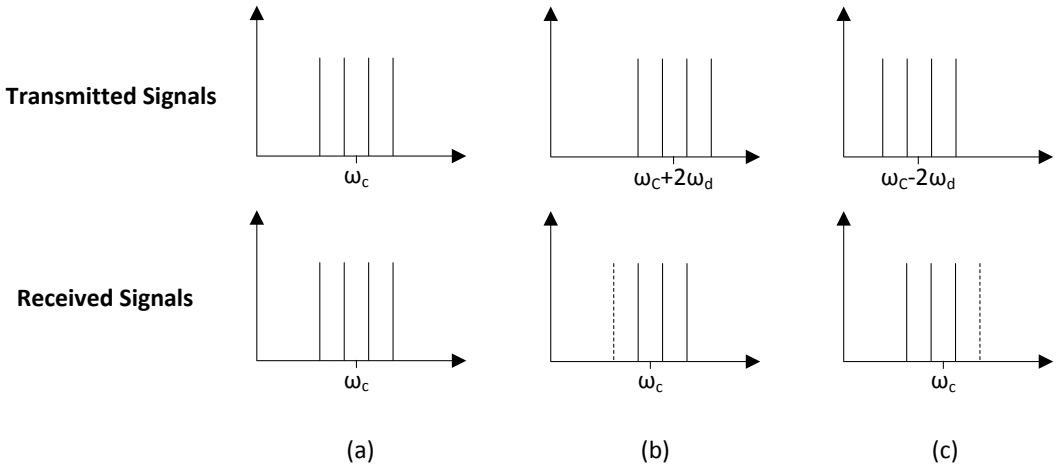


Figure 4.14: Example of Three Measurements Taken for a Four-Tone Signal: (a) the two systems have the same center frequency; (b) the center frequency of the transmitter is raised by the spacing frequency; (c) and then lowered by the spacing frequency.

To transform the system given by the previous equations, the Neper scale is used. Thus, Equation 4.16 to 4.18 could be written as follows:

$$\left[R^0(\omega_k)\right]^{Np} = \left[R_1(\omega_k)\right]^{Np} + \left[R_2(\omega_k)\right]^{Np} \tag{4.19}$$

$$\left[R^+(\omega_k)\right]^{Np} = \left[R_1(\omega_k - 2\omega_d)\right]^{Np} + \left[R_2(\omega_k)\right]^{Np} \tag{4.20}$$

$$\left[R^-(\omega_k)\right]^{Np} = \left[R_1(\omega_k + 2\omega_d)\right]^{Np} + \left[R_2(\omega_k)\right]^{Np} \tag{4.21}$$

This system of equations has more equations than unknowns. Hence, it can be solved easily. This system could be simplified into one equation:

$$R^{Np} = \Lambda \cdot b \tag{4.22}$$

where

$$R^{Np} = \left[\left[R^0\right]^{Np} \left[R^-\right]^{Np} \left[R^+\right]^{Np}\right]^T$$

$$b = \left[\left[R_1(\omega_1)\right]^{Np} \cdots \left[R_1(\omega_{M-1})\right]^{Np} \left[R_2(\omega_1)\right]^{Np} \cdots \left[R_2(\omega_{M-1})\right]^{Np}\right]^T$$

and

$$\Lambda = \begin{bmatrix} I_M & I_M \\ [I_{M-1}\, 0_{M-1}] & [0_{M-1}\, I_{M-1}] \\ [0_{M-1}\, I_{M-1}] & [I_{M-1}\, 0_{M-1}] \end{bmatrix}$$

Consequently, the vector containing the separate ripples of the two cascaded systems is estimated using the LSE algorithm as follows:

$$b = pinv(\Lambda) \cdot R^{Np} \tag{4.23}$$

There are some required conditions in order for Equation 4.23 to be solved: the two systems should have a linear phase in the interval of $[-\omega_d, +\omega_d]$ and the magnitude of one of the ripple is equal to 1 at $-\omega_d$. The explanation of these conditions has been omitted for simplification.

This technique was applied to investigate the amplitude ripple of the transmitter and receiver of the MSDPD-EVB. The parameters of the measurements were set as follows:

- The number of tones was 30,
- The tone spacing was 3MHz,
- The number of samples was 216, and
- The sampling rate was 245.76 MHz, which was the speed of the DAC.

For the proposed mixed-signal multimode radio hardware, the amplitude ripple of the transmitter was about ± 0.1 dB as shown in Figure 4.15, which is considered insignificant. However, the amplitude ripple of the feedback receiver was significant, about ± 1.3 dB, as shown in Figure 4.16.

A vector correction was applied to compensate for the feedback imperfection, while the transmitter response was left as is. A finite impulse response (FIR) filter was introduced to post-distort the feedback receiver's output waveforms. Figure 4.16 shows the frequency response of the feedback before and after correction. This correction provided an improvement of more than 1 dB shown in Figure 4.16, allowing for a flatter frequency response of the feedback over a 90-MHz span. This step of calibration ensures that the transceiver will introduce as little distortion as possible to the signal, thereby resulting in a more accurate PA characterization.

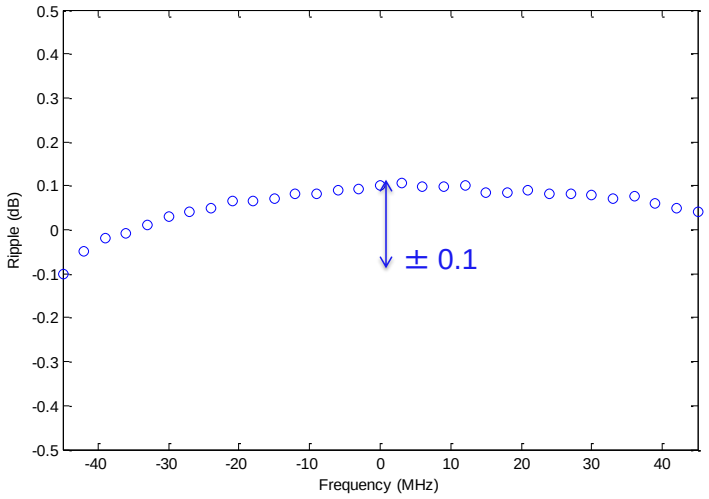


Figure 4.15: Transmitter Ripple Versus Frequency.

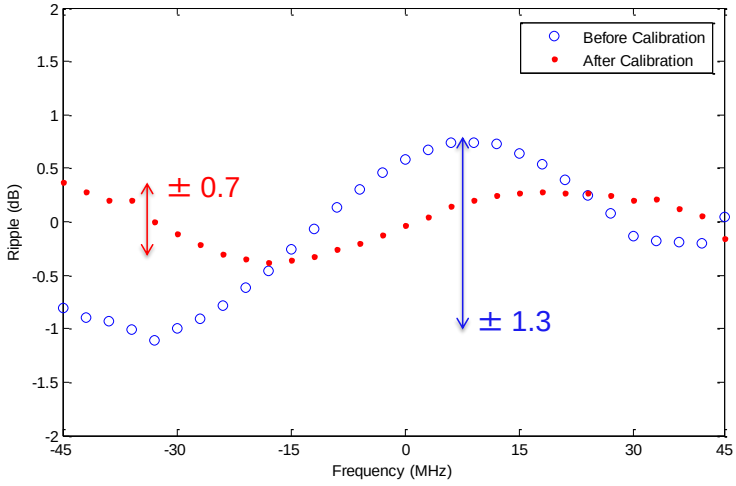


Figure 4.16: Feedback Receiver Ripples Versus Frequency Before and After Calibration.

4.5 Measurement Setup and Results

To validate the implementation of the different DPD models presented previously, the normalized mean square error (NMSE) between the floating-point computation using MATLAB and the fixed-point computation using the FPGA were evaluated. The NMSE of the LUT model was -78 dB; and, the NMSE of the memoryless model was also -78 dB for a nonlinearity order to 9. However, the MP model had an NMSE of -62 dB for a nonlinearity order of 9 and memory depth of 5. These previously mentioned values validate the DPD models' implementation in the FPGA.

Test measurements were then conducted using a 250-Watt Doherty PA driven by one-carrier and multi-carrier WCDMA signals, with respective PAPR equal to 7.2 dB and 7.4 dB. The PA was operated at an average power equal to 45.7 dBm (1.5 dB back-off), resulting in a 2-dB compression.

For an accurate evaluation of the DPD performance, the PA output spectra were collected using Agilent's PXA signal analyzer in order to guarantee that the receiver response did not interfere in the linearization results. The evaluation of the proposed closed-loop DPDs were performed using the ACLR and EVM criteria.

The LUT and memoryless polynomial models were tested using a one-carrier WCDMA signal, as these models do not correct for PA memory effects. The power spectrum densities (PSDs) of the results obtained before and after DPD linearization are illustrated in Figure 4.17 which displays improvements to the ACLRs of the linearized PA using the LUT and memoryless polynomial models. In fact, the ACLR is reduced by almost 20 dB, as shown in Table 4.1.

Table 4.1: ACLR & EVM for LUT and Memoryless DPD

	No DPD	**Look-Up Table DPD**	**Memoryless Polynomial DPD**
ACLR (dBc)	-27.1	-48	-46
EVM (dB)	-24	-50	-47.2

The MP implementation was tested using a wideband signal, which usually result in higher memory effects, namely a two-carrier WCDMA separated by 10 MHz and four-carrier WCDMA signals. From Figure 4.18 and 4.19, it is clear that the spectrum regrowth caused by the nonlinearity of the DUT was reduced considerably. Table 4.2 shows an improvement of more than 20 dB in the ACLR.

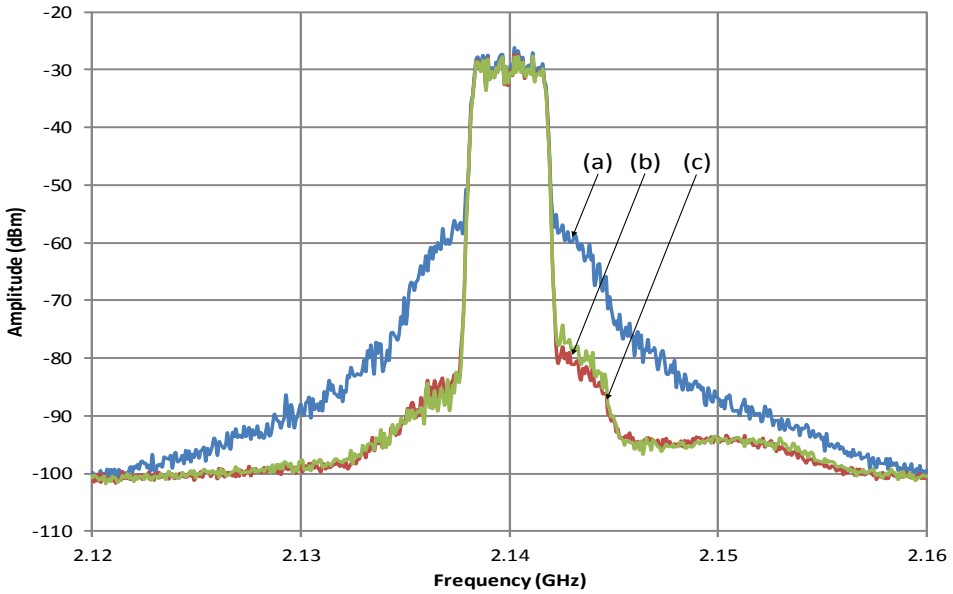


Figure 4.17: One-Carrier WCDMA Linearization Using Memoryless Models: (a) Look-Up Table and (b) Memoryless Polynomial.

To further evaluate the linearization performances, the EVMs were computed before and after linearization. Tables 4.1 and 4.2 show an EVM enhancement of 26 dB for the LUT model, 23 dB for the memoryless polynomial model and 20 dB for the MP model.

Table 4.2: ACLR & EVM for Memory Polynomial DPD

	4C-WCDMA		**2C-WCDMA**	
	No DPD	**MP DPD**	**No DPD**	**MP DPD**
ACLR 2MHz (dBc)	-30	-50	-33.1	-52.3
ACLR 10MHz (dBc)	-37	-58.5	-29.4	-58.8
EVM (dB)	-27.5	-43.5	-25.2	-45.2

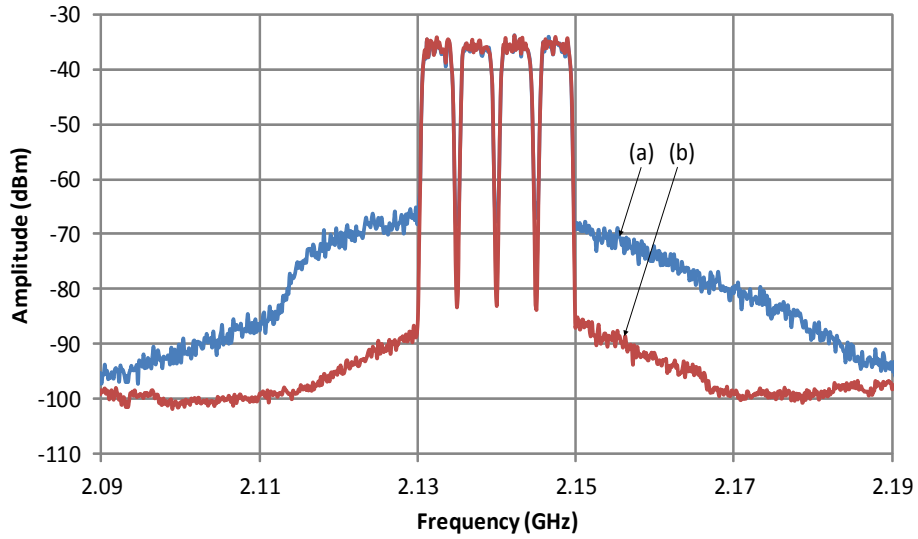


Figure 4.18: Four-Carrier WCDMA Linearization Using Memory Polynomial DPD.

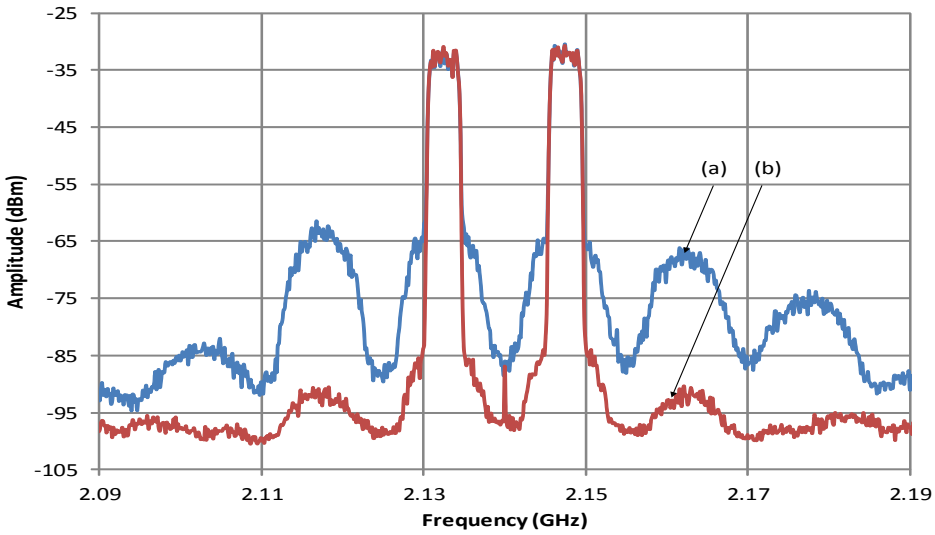


Figure 4.19: Two-Carrier WCDMA Linearization Using Memory Polynomial DPD.

4.6 Conclusion

Throughout this chapter, the mixed-signal, multimode radio transceiver development platform was presented from two perspectives; the designed hardware (i.e., the transmitter, feedback receiver, frequency synthesizer and the DPD implementation) and software (i.e., the dashboard and signal processing tools). The feedback-receiver calibration improved the frequency response flatness. Furthermore, the DPD model implementations were validated using two different metrics which are the ACLR and the EVM. In fact, the linearity of the PA improved considerably.

Chapter 5

Conclusion

The aim of this work has been the implementation of a development platform for wireless system applications. This platform comprises a digital part responsible for generating and capturing a multimode waveform signal and signal processing, namely the application DPD, to linearize the PA in real-time. The real-time DPD system takes into consideration the challenges and imperfections related to implementing PAs in the real world. The designed platform was enhanced through the improvement of the hardware performance (the calibration of the feedback-receiver to improve its frequency response flatness) and the development of a dashboard to control and monitor the platform. Consequently, the implemented development platform is a good candidate for software defined radio (SDR) systems.

In this thesis, theories about RF PA, especially nonlinear PA, and characterization were reviewed with a focus on distortion and memory effects phenomena. Techniques to improve RF systems were considered to improve power efficiency at back-off, through the use of a Doherty PA and extend the linearity of the PA through the implementation of a real-time DPD.

The developed system showed good linearization performance for both memoryless models, namely the LUT and memoryless polynomial models, and memory polynomial models thanks to the new reformulation of the memoryless model which made it suitable for a real-time system while preserving the required accuracy. In fact, an improvement of the signals' ACLR and the EVM quantities by more than 20dB was achieved when DPD was applied. The phase-coherent frequency synthesizer presented will allow extending the capability of the platform. Indeed, this frequency synthesizer can be used to feed two transmitters to build a dual-band architecture. Moreover, it can be used to feed the

transmitter and the feedback receiver to allow for multiband characterization where the carrier frequency of the receiver can be changed to capture several bands.

There are many paths in which this work may be continued. One could attempt to increase the bandwidth of the system since the current version allows for the linearization of up to 100MHz. This could be achieved by using higher speed ADC and improving the throughput of the existing DPD models' implementation. Another possibility would be to implement another DPD model, such as Volterra series, to further improve the linearization capability. In fact, this technique was implemented in FPGA using look-up tables based design[50] which has the drawbacks of large memory consumption and limited Volterra series order. Hence, there is a need for a new Volterra series reformulation that is suitable for real-time system implementation.

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