High Resolution/Wideband on-Chip Phase-Shifting

by

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Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Javad Khajehpour

Abstract

A new active LO phase shifter was introduced and implemented in a 2x2 wide band MIMO receiver. The chip was designed with STMicroelectronics 90nm technology. The main advantages of the proposed phase shifter over previous works included a wide band range, high resolution and small area.

The phase shifter is based on the dependency of the inverter propagation delay on the load capacitance. Simply, by changing the load capacitance of an inverter, a different propagation delay is generated. A number of these controllable delay cells are cascaded to provide the required phase-shift. In order for the delay cells to reduce the required amount of phase-shifting the I&Q swap circuit is introduced. The I&Q swap circuitry reduces the phase-shifting by one fourth of the original range.

The wide band phase shifter is suitable for multi-standard radios, since just one phase shifter is needed to support all standards. This capability of the phase shifter could potentially reduce the size of the die and simplify the design. The measurement shows that the phase shifter is able to provide 360˚ of phase-shifting at the output base band signal when the LO is varying from 1.5GHz to 6GHz. A wider range of the phase shifter is achievable by reducing the capacitance load and increasing the number of cascaded delay cells.

The proposed phase shifter is capable of achieving a very high resolution. The resolution of the phase shifter is a function of the inverter current capability and the load capacitance. The measurements show the average resolution of the proposed phase shifter is about 1.32ps.

Passive components usually take up a large area on the chip. A MOS capacitor is used as the load to reduce the area of the proposed phase shifter.

A method is proposed to improve the phase shifter stability over the temperature and process variations. This method is based on the fact that the propagation delay of an inverter is inversely proportional to the power supply. Therefore, the phase shifters' power supply must be varied to maintain a relatively constant phase shifter resolution over the temperature and process variations.

Acknowledgements

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I have to express my gratitude to my parents who have always believed in me and taught me to do my best. I also would like to thank my brother Professor Amir Khajehpour for his support and encouragement.

I am deeply indebted to my wife Tahmineh who encouraged me to enter the PhD program and also my son Arad who brought us lots of love and joy.

Dedication

I would like to dedicate this thesis to my wife Tahmineh and my son Arad.

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Chapter 1 Introduction

Increasing demands for high rate data communication systems make the antenna array an attractive candidate, because using an antenna array system can increase the data rate without increasing the bandwidth. The antenna phased array system is capable of increasing the sensitivity of the receiver while attenuating undesired signals and interferences. Phased array systems have been used for years in radar and satellite communication systems. The main challenge in adopting an antenna phase array for consumer applications is the high cost of the conventional phased array systems which use discrete low noise amplifiers, microwave phase shifters, and power combiner/divider circuits.

The most essential process in a phased array antenna beam-forming system is phase-shifting very weak RF signals. Many types of phase shifters have already been developed, such as switch transmission lines [1, 2, 5], periodic loaded lines [3, 4], 90˚ coupled lines [6, 7] and reflective type phase shifters [8, 14]. Although these traditional phase shifters can achieve time delay and phase shift along the line, their physical sizes are too big to integrate them into a multi-channel array system targeted for consumer applications [27]. The problem has motivated a massive effort to reduce the size of the phase shifters enough such that they can be integrated into multiple-antenna array systems, while still achieving the required phase shift.

The phase shifter can be implemented in RF (Radio Frequency), LO (Local Oscillator), IF (Intermediate Frequency) or in a digital processing sub-system. Performing beam-forming in the digital domain allows the capability of applying different algorithms [3 1, 32, 33, 10, 9], however, this method requires a large chip area and an increased power consumption. In addition, all blocks in a receiver chain need to be designed with high linearity, which is a very challenging task.

In IF phase-shifting, beam-forming is performed in an intermediate frequency. In this architecture, if the phase shifters use passive elements it uses a very large area on the chip since the value of passive components is inversely proportional to the operation frequency.

RF phase-shifting uses the most shared blocks, since after combining all the phase shifted signals, the rest of the receiver is just a single path receiver [19, 20, 21, 22, 23, 24, 25, 26, 11, 15, 12, 13, 14]. This method requires less area and consumes less power than other approaches, and the linearity requirement for receiver chain blocks after beam-forming is relaxed because undesired and interference signals are attenuated. The drawback of the passive RF phase shifters is the reduction of the receiver sensitivity due to the added insertion loss. Active phase shifters does not introduce any loss in the RF path therefore does not degrade the receiver performance. However, any noise introduced from the active phase shifters will impact on the receiver noise performance. Also, active phase shifters need to be highly linear to avoid limiting the dynamic range of the receiver. Another problem with active phase shifter is the resolution changes with phase.

A promising alternative is the local oscillator (LO) phase-shifting method, where the required phase shift for each antenna is applied to a copy of the LO signal, which is then mixed with the RF signal from that particular antenna. In this method, the phase shift is actually introduced in the down-converted IF signal from each antenna. The main advantage of the LO phase-shifting approach is that the phase shifters are not implemented in the signal path. Therefore, the receiver performance does not suffer from the aforementioned degradations of RF phase-shifting, and the linearity of the phase shifter is not an issue anymore. The challenging aspect of LO phase-shifting is that the mixers need to be highly linear since the beam-forming is performed after the mixer stage. LO phase-shifting can be performed in the local oscillator (VCO) or after the oscillator [17, 16, 28, 29]. Performing the phase-shifting within the oscillator requires a large chip area. Moreover, achieving a high resolution phase shift within the oscillator is not possible especially in a high operating frequency. Compared to VCO phase-shifting, performing phase-shifting after the VCO is more advantageous because it does not impose any restriction on the VCO architecture. The tradeoff is the need for large chip area if high resolution phase-shifting is required.

The on-chip beam-former radio architecture proposed here introduces a high performance LO phase-shifting configuration that simultaneously achieves a high phase resolution. Since it does not use passive components, the required chip area is small. In

addition, the proposed phase-shifting method is suitable for wide band or multi-band applications.

The next chapter presents a review of existing phase-shifting techniques. Chapter 3 provides a detailed description, performance analysis, and application of the proposed approach to an *m*-by-*n* MIMO receiver architecture. Chapter 4 is focused on the practical implementation of the proposed approach in a 2-by-2 MIMO receiver using CMOS 90nm technology. All main blocks of the receiver are explained with some simulation results. The next chapter is focused on the measurement results and characterization of the proposed phase shifter and receiver chain performance. The phase shifter is characterized in terms of resolution, bandwidth and power consumption versus frequency. The gain variation of the receiver and also the output baseband signal power versus phase difference of the input RF signals has been measured. To reduce the dependency of the phase shifter performance on process and temperature variation, a new stabilization method is proposed in which effectively reduced the phase shifter variation. The last chapter concludes with some comments on the research results achieved, the future work and the direction of the research.

Chapter 2 Literature Review

The smart (adaptive) multi-antenna radio system is considered to be a promising method to meet the demand of a higher data rate and better communication quality without increasing the bandwidth. A radio with adaptive beam-forming capability is believed as the only way to improve the spectral efficiency of future wireless networks. The phased-array antenna, a key subsystem of an adaptive radio has been used in radar systems for years. The high cost of microwave discrete phase shifters (modules), and the complexity of its associated feed circuit have been one of the main hurdles in applying this technology to the consumer mass market. There is no doubt that a low cost integrated phased array will open up the market for the extensive application of general purpose multi-antenna radio systems. The principle operation of a phased array system is shown in Fig. 2.1. An array of *n* antennas receives the radiated signal with different time-delays because of the different spatial locations of the antennas.

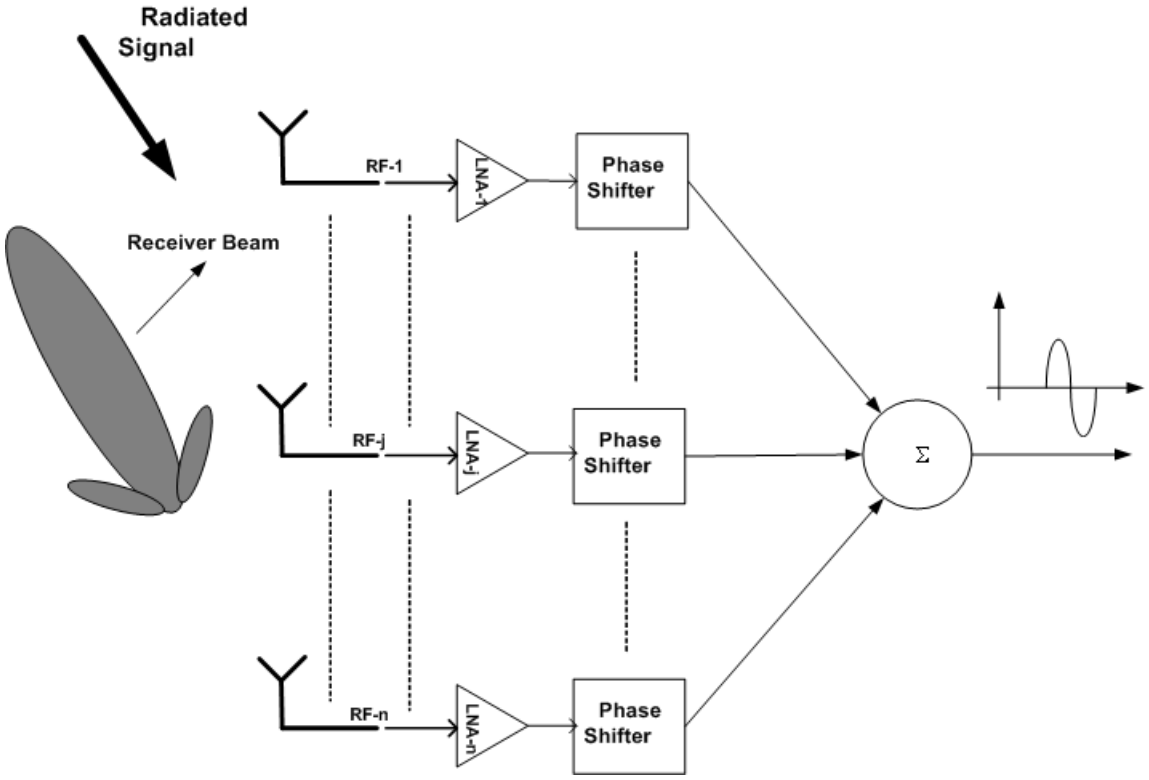


Fig. 2.1: Receiver Phase Array [17]

By adjusting the delay or the phase of each received signal individually, all the received signals from a particular direction will become in-phase (same time delay) and add constructively. On the other hand, signals received from other directions add destructively and are rejected by the phase array receiver system. In transmit mode, because of the beam-forming capability of the array system, the transmitter generates less radiation and therefore less interference in non-targeted receivers as it is shown in Fig. 2.2.

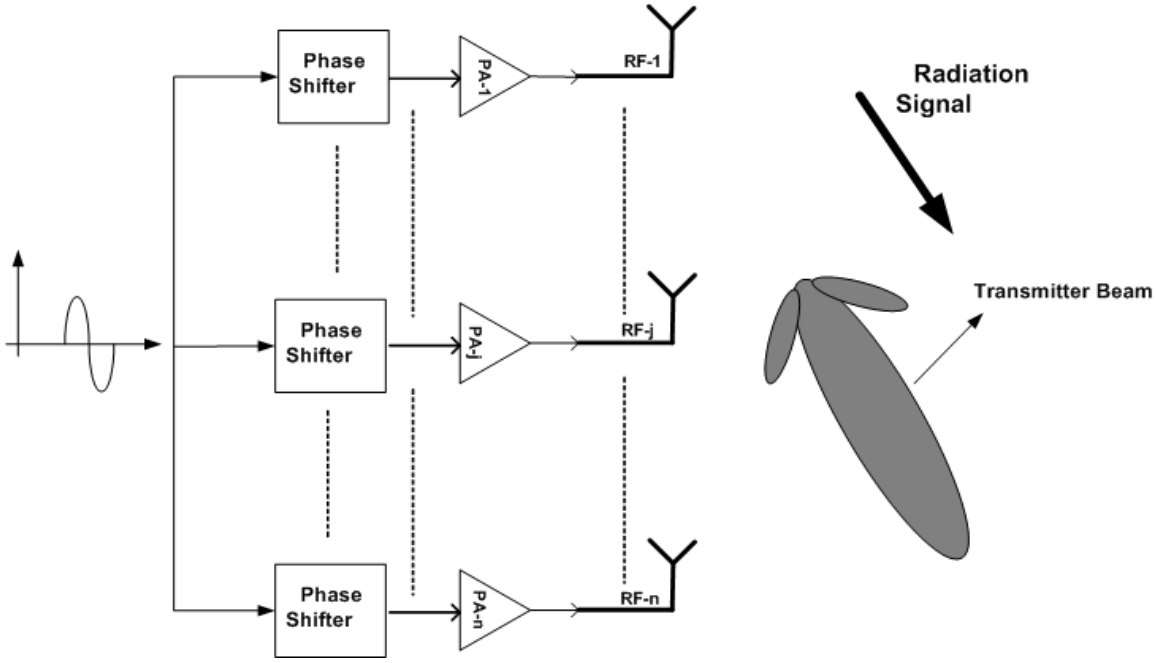


Fig. 2.2: Transmitter Array Systems [17]

For a given power level at the receiver, the required transmitter power is lower than a non-phased array system.

In general, the phased array system improves the dynamic range of the receiver by improving the noise performance. The receiver sensitivity is a function the receiver's noise factor, and reducing the noise factor increases the sensitivity and dynamic range of the receiver. The noise factor (*F)* is defined as the ratio of the input Signal-power-to-Noise-power-Ratio (SNR) to the output SNR [18],

$$F = \frac{(\frac{S}{N})_{in}}{(\frac{S}{N})_{out}} \qquad (2.1)$$

The noise factor expressed in decibels is called the Noise Figure (NF).

Fig. 2.3 shows an RF phase-shifting system which is composed of n antennas, n LNAs and n phase shifters followed by a single combiner. The noise of each antenna is shown by n_{ant}. The input referred noise of the LNA and the phase shifter in each path is shown by n_{rec}. It is also assumed that G is the gain of each LNA. The strength of the signal at the input of the receiver is shown by s in volts. The noise factor of a single receiver can be expressed as,

$$F = \frac{(\frac{S}{N})_{in}}{(\frac{S}{N})_{out}} = \frac{\frac{s^2}{n_{ant}}}{\frac{s^2 G}{(n_{ant}+n_{rec})G}} = \frac{n_{ant}+n_{rec}}{n_{ant}} \qquad (2.2)$$

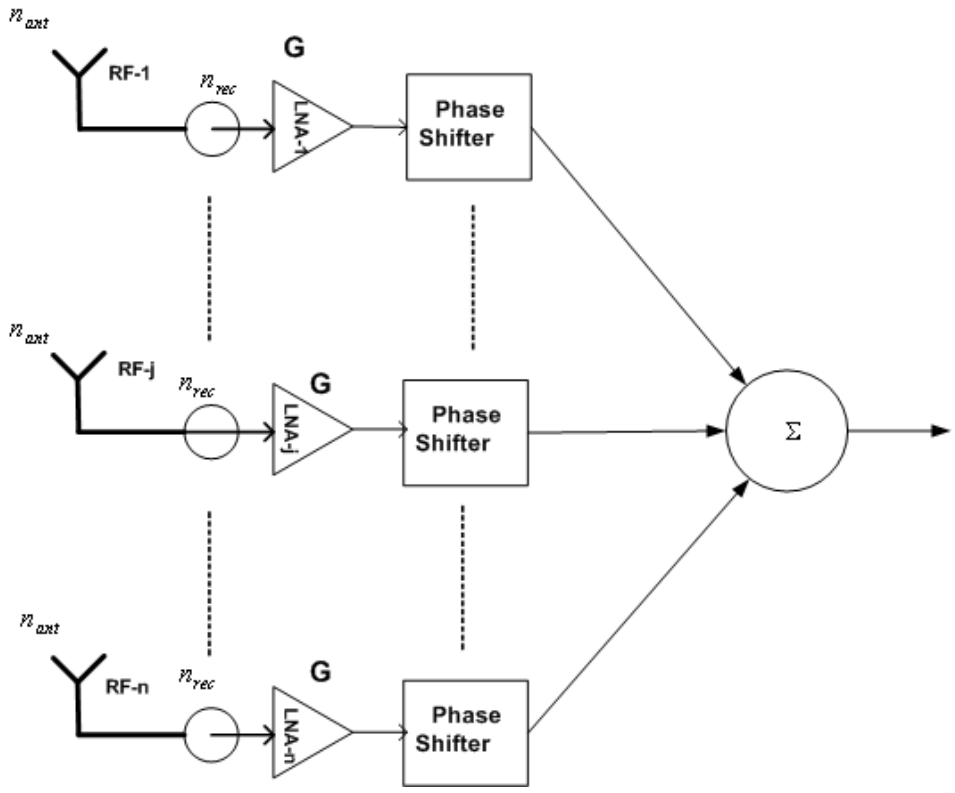


Fig. 2.3: Noise Model of Array

In this equation s^2 is the power of the input signal s. For an array of n antennas, as shown in Fig. 2.3, the noise factor is expressed as follows,

$$F = \frac{(\frac{S}{N})_{in}}{(\frac{S}{N})_{out}} = \frac{\frac{s^2}{n_{ant}}}{\frac{n^2 s^2 G}{n(n_{ant}+n_{rec})G}} = \frac{n(n_{ant}+n_{rec})s^2 G}{n^2 s^2 n_{ant} G} = \frac{n_{ant}+n_{rec}}{n n_{ant}} = \frac{1}{n}(\frac{n_{ant}+n_{rec}}{n_{ant}})$$

(2.3)

It is seen that the noise factor of an array system made of n antennas is lower than that of a single antenna receiver by a factor of n. This can be argued as follows, since the input signal voltage added in-phase at the output of a phase-adjusted array, the array output power is: $(ns)^2 = n^2 s^2$, but the noise signals are incoherent and their power will be added at the array output. The total noise power is therefore *n* times that of a single receiver. The following equation shows the noise figure of an array system of *n* antennas in terms of a single path receiver noise figure.

$$NF_{array} = NF_{Single-Path} - 10\log n \qquad (2.4)$$

The above equation is valid only if the phase shifters are ideal. The insertion loss of the phase shifter degrades the noise performance of the array antenna system.

Phased array systems are classified by where the phase-shifting or delay compensation is performed. This process can be implemented in the RF front-end, IF section, LO, or in the digital signal processor.

2.1 RF Phase-Shifting

Fig. 2.4 illustrates the RF (Radio Frequency) phase-shifting approach.

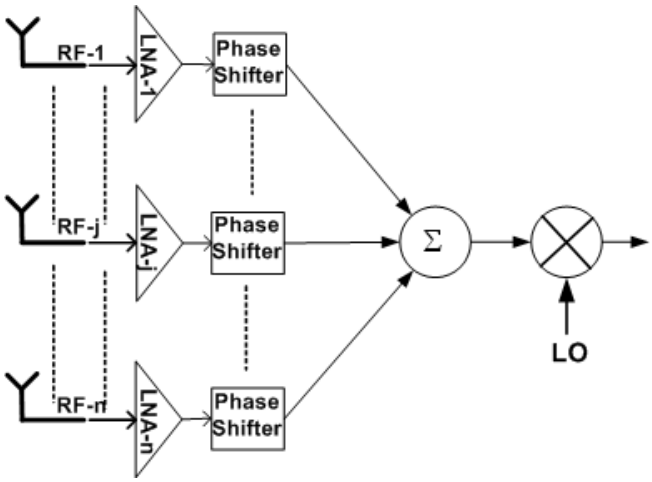


Fig. 2.4: RF Phase-Shifter Architecture

As shown in Fig. 2.4, the signal received from each antenna is amplified in a low noise amplifier, and phase-compensated in the phase shifter, then all received signals are added in-phase. In this architecture, the phase shifter can be either passive or active.

A common way to realize the required phase shift is to split the input signal into two equal amplitude quadrature signals [20]. Each signal then goes to a variable gain amplifier. By summing up the two amplified signals, the variable phase shift can be achieved as shown in Fig. 2.5. This approach is referred as a Cartesian or a phase rotator.

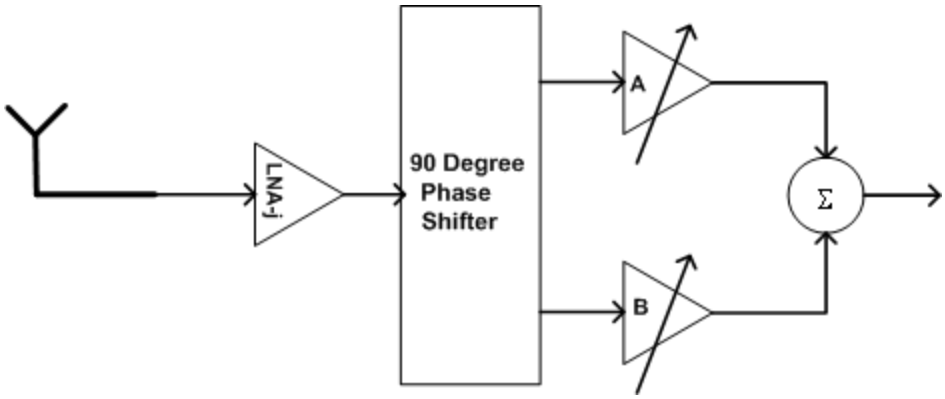


Fig. 2.5: RF Phase Shifter

The quadrature signals can be generated by using RC-CR filters. The amount of the phase shift is determined by the ratio of the gains of the amplifiers as it is shown in Fig. 2.6.

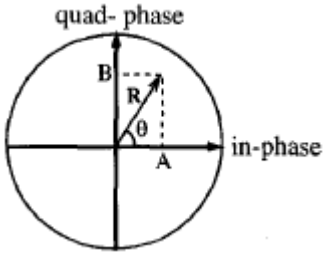


Fig. 2.6: Vector Diagram [19]

The phase shift depends on the amplitude of the quadrature signals. The vector R which is the sum of two quadrature signals can be described in polar form as [19],

$$R = \sqrt{A^2 + B^2} \angle \tan^{-1} \frac{B}{A} \qquad (2.5)$$

In order to cover the 360˚ phase shift, the polarity of the input signals to the amplifiers or the output of amplifiers should be changed. One drawback of this RF phase-shifting method is the dependence of the sum signal amplitude on the phase value. In fact, phase-

shifting causes amplitude distortion, which requires a complicated gain control on the variable gain amplifiers to reduce the distortion of the output signal. Another drawback is the insertion loss of the RC-CR circuit degrades the sensitivity of the receiver. To compensate for the loss, the gain of the LNA needs to be increased. This makes the design of the LNA particularly challenging to meet the linearity requirement. Higher linearity requires more power consumption as well. Another issue with a RC-CR filter is the quadrature signal's amplitude dependency on the absolute values of R and C, which vary with the fabrication process and temperature. To avoid these issues, it is reported that an active vector generator has been used [22, 23]. The active vector generator consists of two paths as it shown in Fig. 2.7. Path1 and path2 are composed of a differential amplifier with a resistive load. In path2 there is an additional differential amplifier A2. A differential amplifier inherently makes a 180˚ phase shift at low frequencies, but because of the gate-drain capacitance and RC load at the drain node, at high frequencies (20-30GHz) the RF signal in the second differential amplifier in path2 experiences a -70˚ to -80˚ phase shift [22]. The total phase shift between path1 and path 2 is between 100˚ to 110˚.

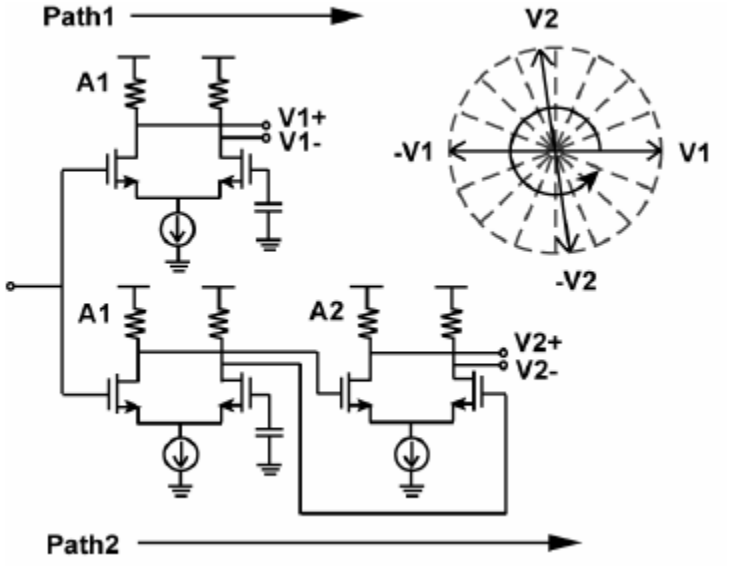


Fig. 2.7: Active Vector [22]

The drawback of an active vector generator is its dependency of the output vector signals to the process variation. The phase difference between the two paths can vary because of

the process variation, which increases the phase error. In addition, the active vector generator should be highly linear so that it does not limit the dynamic range of the receiver. Another drawback of the active vector generator is the resolution of the phase shift in different regions because the vector generator does not generate quadrature vectors.

Another approach to perform RF phase-shifting is a second-order all-pass filter with the following transfer function [25],

$$H(s) = \frac{s^2 - \frac{\omega_o}{Q}s + {\omega_o}^2}{s^2 + \frac{\omega_o}{Q}s + {\omega_o}^2} \qquad (2.6)$$

where ω_o is the central angular frequency and the Q is the quality factor. The phase of this second-order all-pass filter is [25],

$$\phi = -2\tan^{-1}\{\frac{\omega\omega_o}{Q({\omega_o}^2 - \omega^2)}\} \qquad (2.7)$$

As shown in 2.7, the phase variation depends on the frequency, and there is no gain variation with the frequency. For a given input frequency, an all-pass filter can operate as a variable phase shifter by varying the center frequency ω_o. Fig. 2.8 shows the all-pass phase variation versus frequency.

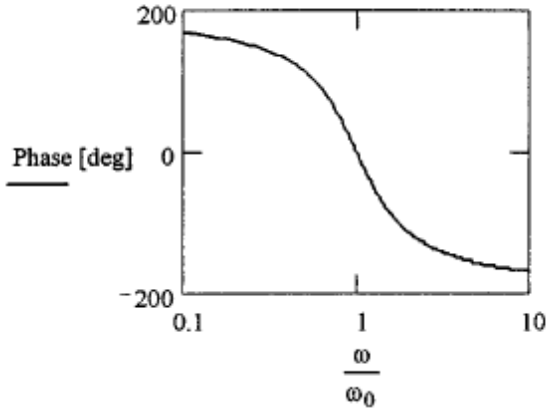


Fig. 2.8: All-Pass Phase Variation versus Frequency [24]

Many active second-order all-pass filters have been proposed [24, 25, 26]. Fig. 2.9 shows one of the proposed active second-order all-pass filters.

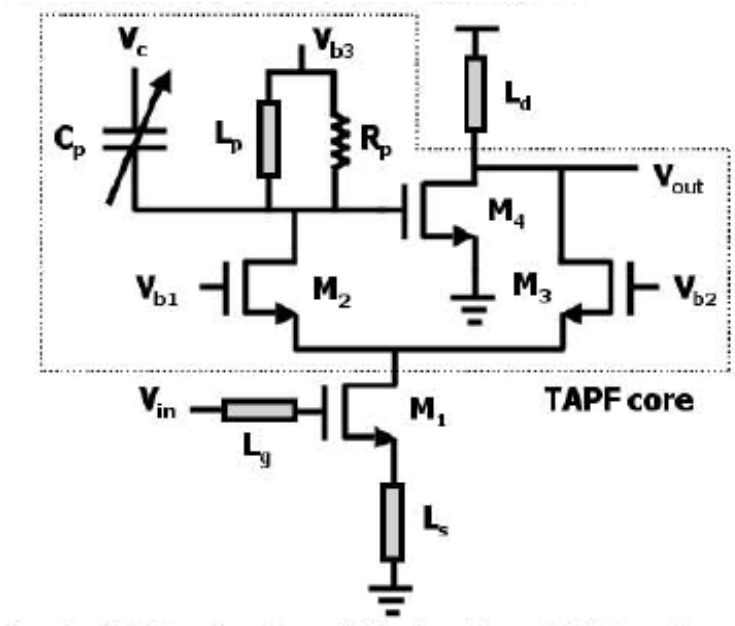


Fig. 2.9: CMOS Active phase Shifter [25]

By properly designing the component values and the transconductance of the transistors for a given input frequency, this circuit works as a second-order all-pass filter. The phase of input RF signal can be varied by changing the capacitance of the varactor.

The second-order all-pass filter approach has an advantage over the Cartesian method. This approach does not need a vector generator; also the gain of the phase shifter is fairly constant over the phase variation. The large chip area is the main drawback of this phase shifter. The fact that at least one inductor is needed for each input RF signal, makes this approach less attractive for large antenna arrays.

2.2 IF Phase-Shifting

Alternatively, the phase shifters can be implemented in the IF section. The RF signal is amplified by a Low Noise Amplifier (LNA) and down-converted to a lower frequency, as shown in Fig. 2.10.

As the phase shifters move to the back end of the receiver, the number of shared blocks is reduced. Therefore it requires a higher current consumption and bigger area on the chip.

With a lower operation frequency, an IF phase shifter introduces less loss and consumes less power.

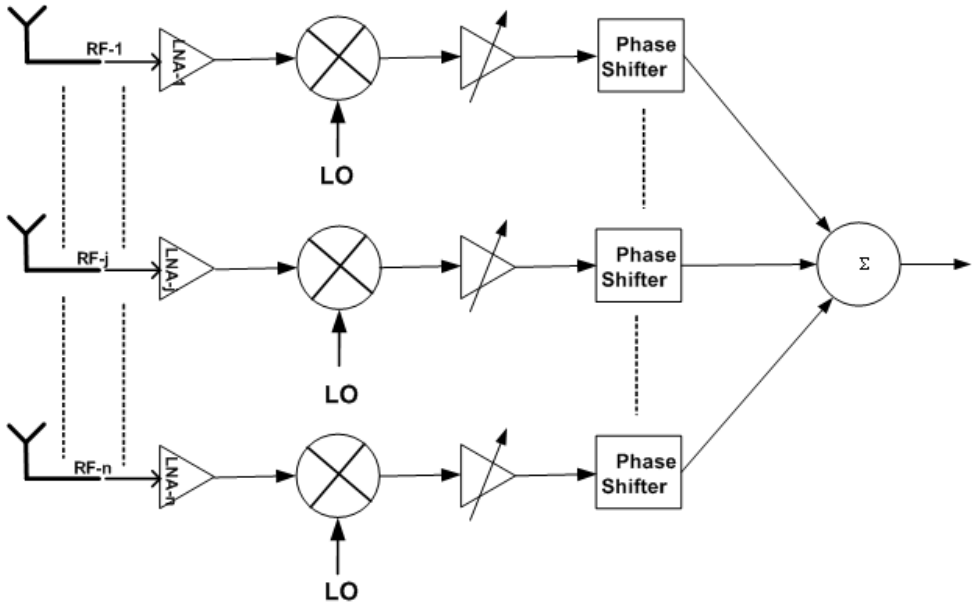


Fig. 2.10: IF Phase Shifter Architecture

If the IF phase shifter uses passive elements, it will take up a larger chip area since the value of the passive components is generally inversely proportional to the operating frequency. Since the signals are added in IF, the mixers in this architecture need to be more linear than the mixers in the RF phase-shifting architecture. Generally the IF phase shifters need a bigger die area than the RF phase shifters.

2.3 LO Phase-Shifting

Fig. 2.11 shows the LO phase-shifting architecture, in this architecture the delay compensation is implemented in the LO path. By changing the LO signal delay of each mixer, the phases of the IF signals will be adjusted so that they add in-phase (synchronized) or constructively.

This is due to the fact that the phase of the mixed signal is a linear function of the input RF and the LO phase, and can be described as follows,

$$V_{out}(t) = \cos(\omega_{RF} t + \varphi_{RF}) \cos(\omega_{LO} t + \varphi_{LO})$$
$$= \frac{1}{2}\cos[(\omega_{RF} + \omega_{LO})t + (\varphi_{RF} + \varphi_{LO})] + \frac{1}{2}\cos[(\omega_{RF} - \omega_{LO})t + (\varphi_{RF} - \varphi_{LO})]$$

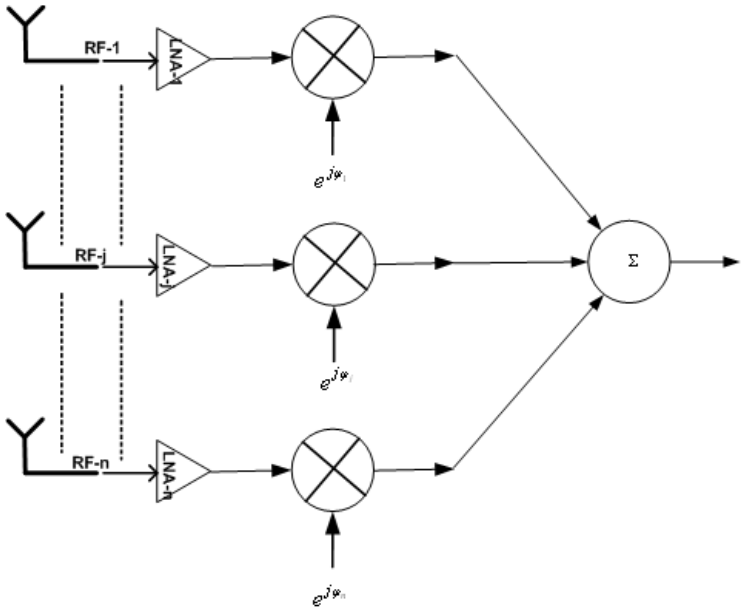


Fig. 2.11: LO Phase Shifter Architecture

Since the phase shifters are not implemented in the RF path, this architecture does not suffer from the phase shifter insertion loss. The loss of the phase shifter in the RF path should be compensated by increasing the gain of the LNA or the gain of another amplifier prior to the phase shifter [27]. Both solutions increase power consumption, but the nonlinearity of the phase shifter is not an issue in LO phase-shifting. Since the signals are added in IF, undesired interference will be rejected in IF. The result is the mixers should have a higher dynamic range in this architecture compared to those in RF phase-shifting [28]. In this architecture the phase of the LO signal for each mixer is controlled independently, and the amplitude of the RF signal can be adjusted by varying the LNA's gain.

Two methods can be used to generate phase-shifting in the LO path. One approach is to generate multiple phase shifts after the oscillator [29], or generate multiple phases in the oscillator [28, 17].

Fig. 2.12 shows a double bridge phase shifter which is consists of two RC-bridge circuits. A RC-bridge phase shifter is used after the oscillator to generate multiple phase-shifting [29]. The output signal of the buffers has the same amplitude for all frequencies, since the bridge is an all-pass filter. Bridge1 produces a $\pi/2+\varphi/2$ phase shift in the output and bridge2 produces a $\pi/2-\varphi/2$ phase shift. Fig. 2.13 shows the phase frequency response and phase difference of the two double bridge circuits. The phase-shifting in the two bridges are different because R_1 and C_1 are smaller than R_2 and C_2. The phase difference can change from 0˚ to 180˚.

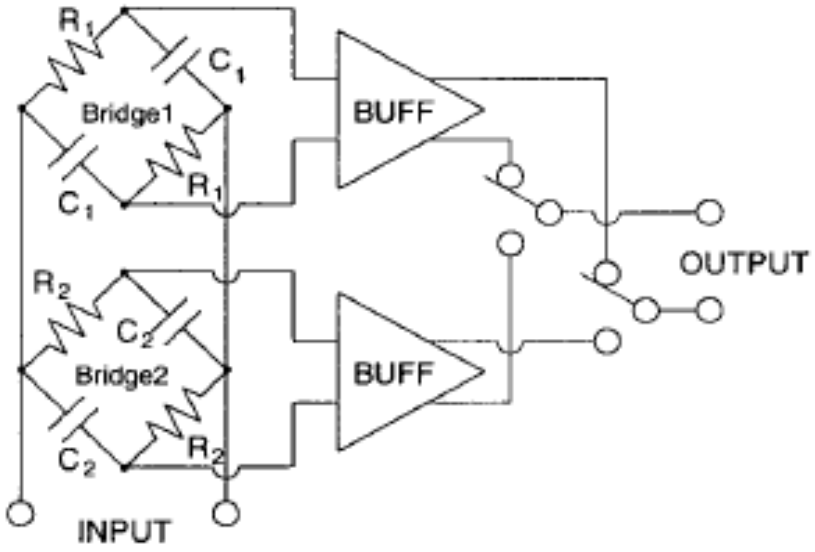


Fig. 2.12: Two Double RC-Bridge [36]

To have multiple phase-shifted LO signals, the output of the VCO could be connected to a number of double RC-bridges. The phase-shifted LO in the output buffers of the RC-bridge circuits drive the mixers through a phase shift selector to change the angle of the incoming RF signals.

The double RC-bridge is passive and introduces loss on the LO path that needs to be compensated with the buffers, which will increase the power consumption. Another drawback is that a double RC-bridge is narrow band, which is not a suitable option for wide band applications.

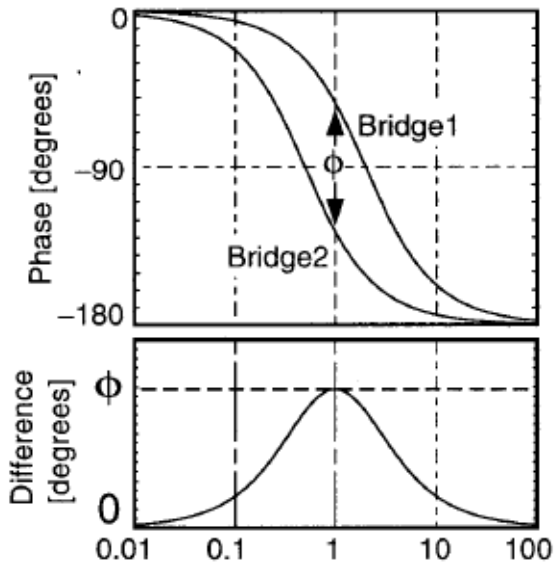


Fig. 2.13: Phase Response and Phase Difference of Two Double RC-Bridge Circuits [29]

Fig. 2.14 shows a ring oscillator. The VCO is composed of eight fully differential CMOS amplifiers that are capable of generating sixteen phases [30].

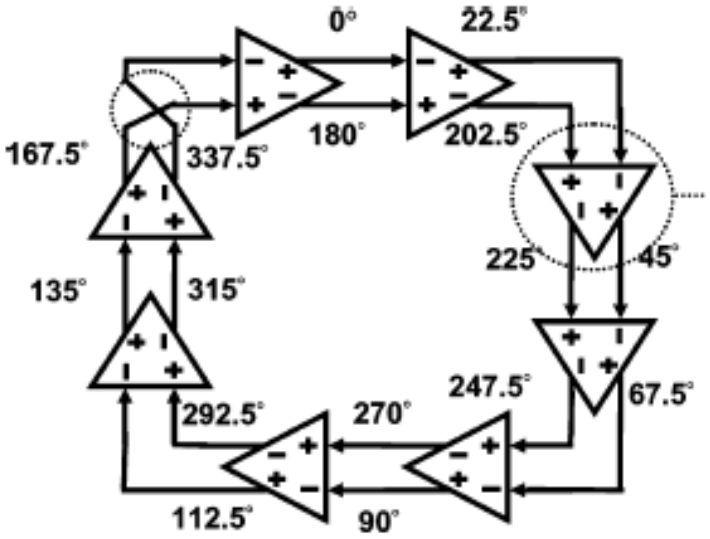


Fig. 2.14: Ring Oscillator [30]

By changing the polarity of one of the amplifiers, the number of amplifiers to generate given phases is cut to half [28]. Generated phased LO signals go to the phase selectors and then are applied to the mixers.

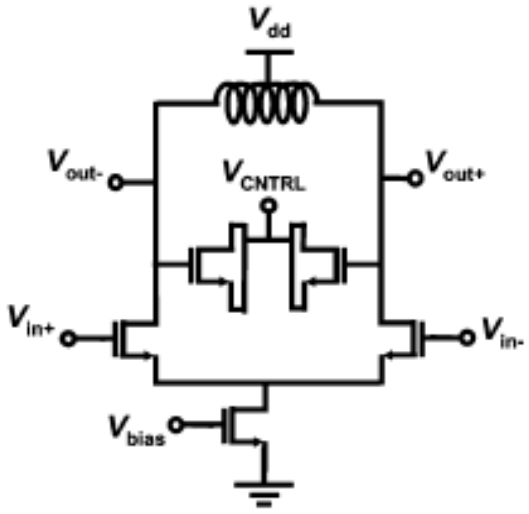


Fig. 2.15: Oscillator Buffer [30]

Fig. 2.15 shows the buffer that is used in the oscillator. Each buffer has a tuned circuit and the center frequency can be varied by changing the control voltage of the MOS varactor.

However there are two drawbacks. The first drawback of the VCO phase-shifting is the large chip area needed by the inductors. To achieve a 22.5˚ resolution, the oscillator needs eight inductors. This will take up a huge area on the chip. The second drawback of implementing this phase-shifting method is its high frequency limitation due to the fact that the total delay around the ring is the period of the oscillation. This means for a given frequency of operation, the maximum number of delay cells is limited, and is a function of the transistor speed. In addition, VCO phase-shifting is only possible with the ring oscillator architecture. Since the phase shift is a function of the number of buffers, a higher resolution requires a larger number of buffers which leads to more phase noise.

2.4 DSP Phase-Shifting

Controlling the phase and amplitude of an array system can be performed in DSP (Digital Signal Processing) [31, 32, 33, 9]. In this architecture, for an array of *n* antenna there are *n* receiver paths as it is shown in Fig. 2.16.

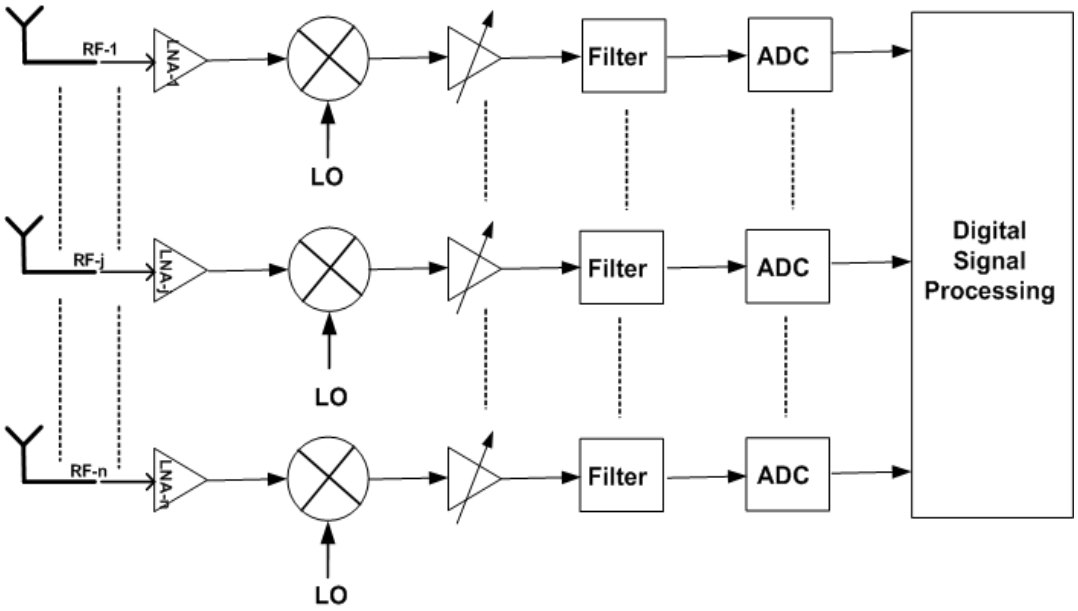


Fig. 2.16: Digital Phase Shifter Architecture

The main advantage of beam-forming in a digital signal processing section is its flexibility in implementing various beam-forming algorithms. This is particularly true for applications that require access to complex signals, and information from each antenna. The main drawback of this architecture is that one full transceiver chain is needed for each antenna. This makes any large array system extremely complex, costly and consumes power. Furthermore, because of the large number of Analog-to-Digital Convertors (ADC) required, the needed chip area will be excessively large. In addition, the undesired signals are canceled out only after the analog-to-digital conversion occurs in the DSP, therefore the receiver chain needs to be highly linear, which is difficult to realize.

2-5 Summary

An adaptive array and radio system is an effective way to improve the performance of the communication systems and to enhance the spectral efficiency of wireless networks. Phased-array architecture with amplitude control capability is the most promising approach for antenna beam adaptation and intelligent radio systems. On-chip phase/amplitude control and beam-forming is essential for implementing the

aforementioned intelligent radio concepts in portable devices for mass market applications. The phased-array concept can be implemented in the RF front-end, IF section, LO, or in digital signal processing. The RF paths' phase-shifting is the best choice in terms of the number of shared blocks. This reduces the die size and power consumption. The other advantage of RF phase-shifting is that the linearity requirements of the following blocks will be relaxed because of the cancellation of the undesired signals. The drawback of RF phase-shifting is the dependency of the receiver performance on the phase shifter's linearity and noise.

IF phase-shifting has an advantage over RF phase-shifting, as the sensitivity of the receiver is less depended on the noise performance of the phase shifters. The tradeoff of using a passive phase shifter is that the area of the phase shifter is bigger than that of the RF phase shifter, and IF phase-shifting suffers from less shared blocks compare to RF phase-shifting.

DSP phase-shifting is not a practical option especially for the high number of antenna arrays. This method suffers from very high power consumption and large chip area.

Another method of beam-forming is performing the phase-shifting in the LO path. The main advantage of this method is that the performance of the receiver does not depend on the phase shifter, since phase-shifting does not perform in the signal path. In this method, the phase-shifting can be done in the VCO or after the VCO. The drawback of this method over RF phase-shifting is increasing the number of non-shared blocks.

In summary, all the phase shifters either suffer either from large chip area, low resolution, high power requirements or narrow bandwidth. The following table shows a qualitative comparison between the different methods of on-chip phase-shifting in terms of area, power consumption, multi-standard and resolution. In this table, higher number of " * " means better performance.

Table 2.1: Phase Shifters Summary

Phase Shifter / Criteria	RF Phase-Shifting			IF Phase Shifting	LO Phase Shifting		DSP Phase Shifting
	Passive Quadrature	Active Quadrature	All Pass Filter		VCO	LO Path	
Area	***	****	**	**	***	****	*
Power	*****	****	****	**	****	***	*
Multi Standard	***	***	****	***	****	***	*****
Resolution	****	****	****	***	*	****	*****

Chapter 3 On-Chip Local Oscillator Path Beam-Forming

On-chip beam-forming is a promising way to improve the wireless communication performance without increasing the bandwidth or using a more complicated modulation scheme. In the LO phase-shifting architecture, the beam-forming is performed in the LO path after the local oscillator. Then, it is applied to the down-convertor mixers in the receiver chain or to the up-convertor mixers in the transmitter chain. The phase shift is based on the time compensation using *active delay cell*. This method has a few advantages over other methods as follows:

First, the proposed phase-shifting method is achieving a high phase shift resolution. Second, the phase shifter does not introduce any loss on the LO path, therefore it does not need extra buffers to compensate for the loss. Third, the phase shifter has a very wide band and it is suitable for wide band and multi-band applications. Finally, the area required for the proposed phase shifter is less than most existing published phase shifters, since it does not need any inductor or resistor which takes up a large area on the chip.

3.1 Scalable Receiver Beam-Forming Architecture

Fig. 3.1 shows the *n* by *m* receiver architecture, which means there are *n* input paths coming from an array of *n* antenna and it creates *m* base band output signals. Each output is a combination of *n* inputs RF signals with different amplitude values that down-convert in a set of *n* I&Q mixers with a different LO phase which add together to create one I&Q output. The LO signal is generated in a synthesizer and is passed to a *mxn* phase shifter and I&Q generator block. This is capable of shifting the phase from 0 to 360 degrees and generates differential I&Q LO signals. The output of each LNA is connected to an amplifier, which splits the input signal to the *m* output signals such that the amplitude of each output signal can be adjusted independently. In general, each set of mixers down-convert *n* RF signals coming from an array of *n* antenna by multiplying them with *n* differential I&Q phase controllable LO signals and combine all the down-converted signals to create one differential I&Q base band signal.

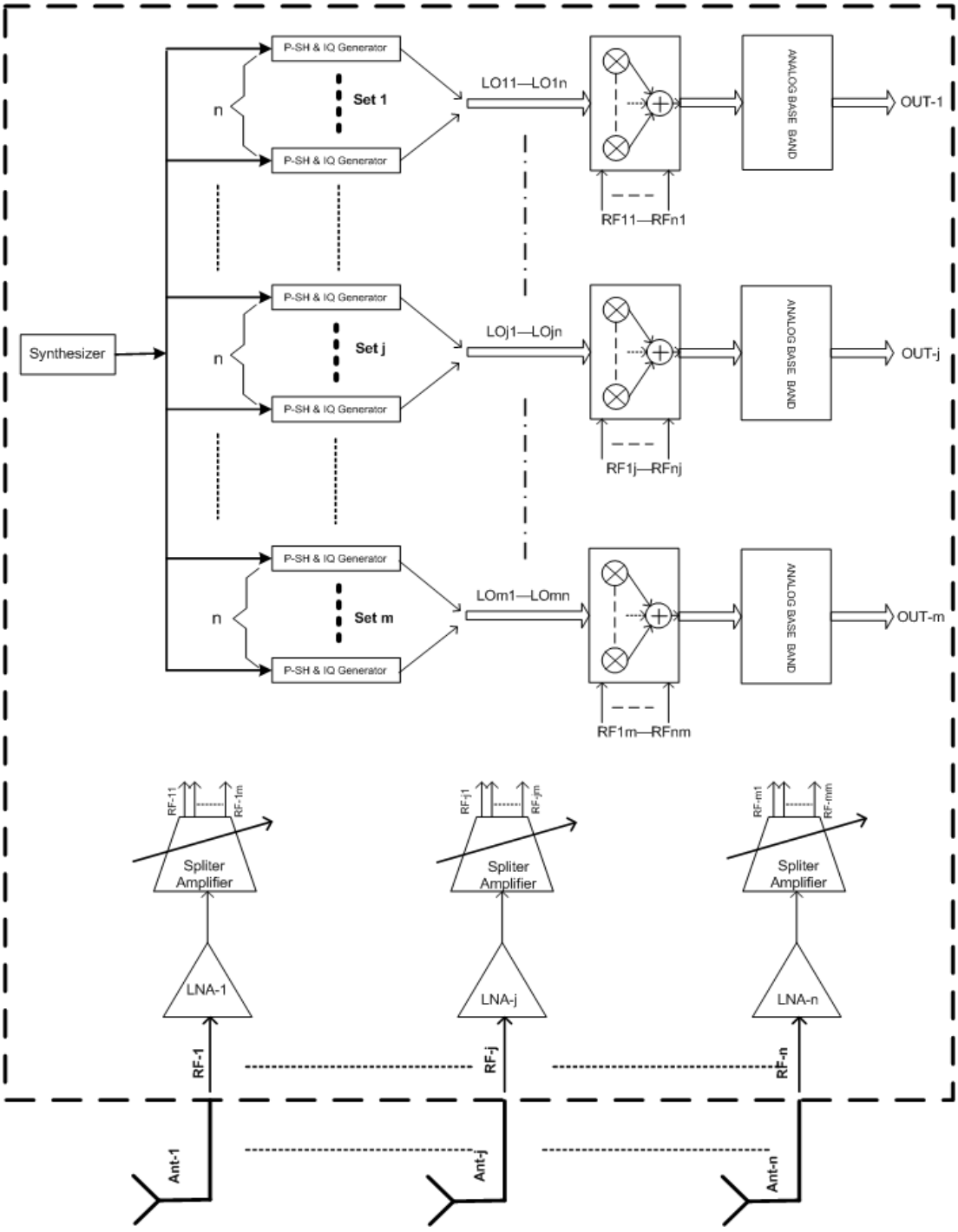


Fig. 3.1: n-by-m Scalable Receive Beam-Forming Architecture

3.2 Phase Shifter

The phase shifter is the key block for on-chip beam-forming applications. This block should be able to make the required phase-shifting on the LO signal, while having minimum effect on the LO phase noise. The phase noise of the LO is a key spec in wireless radio design. On the receiver side, the skirt of the LO down-converts the adjacent channels together with any strong interference (blocker) onto the desire signal band. This causes degradation of the signal-to-noise-ratio (S/N) which in turn affects the Bit Error Rate (BER). Fig. 3.2 shows the ideal LO, and LO with phase noise and the effect of the local oscillator's phase noise on the wanted signal.

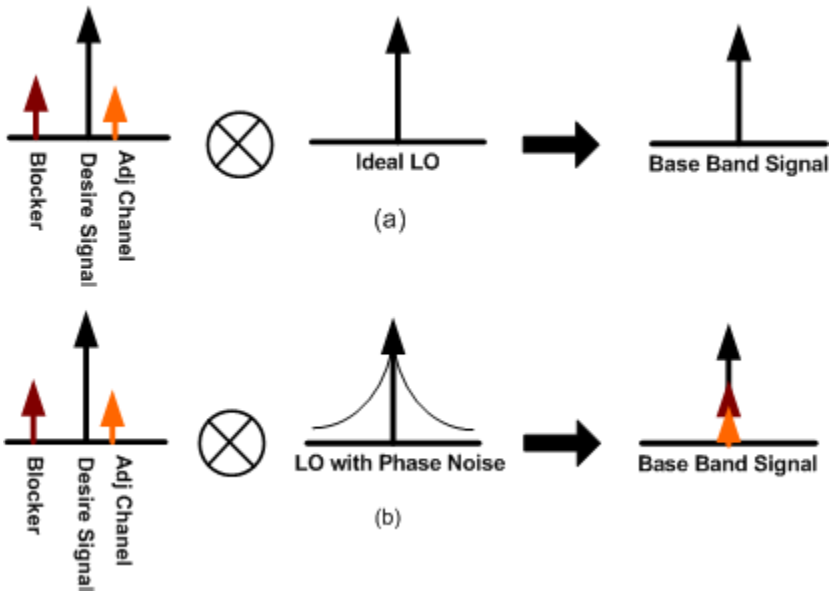


Fig. 3.2: Effect of the Phase Noise on Down-Converted Signal (a) Ideal LO (b) LO with Phase Noise

A new aspect of the scalable architecture is that the phase shifter functions are based on the delay. By changing the delay of the LO signal, its phase relative to the other LO paths changes. Fig. 3.3 shows the basic idea of having a variable delay on the LO path. By cascading the delay blocks and changing the capacitor load, C_L, of each delay block, the overall delay can be changed. The propagation delay (t_p) is measured between the 50% transition points of the input and the output waveforms as shown in Fig. 3.4 [34].

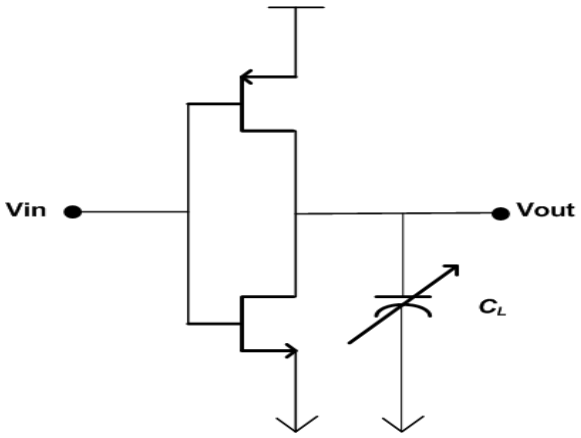


Fig. 3.3: Inverter with Variable Capacitive Load

Since the rise and fall time might experience a different delay, the overall propagation delay t_p is defined as the average transitions of low-to-high and high-to-low output respectively. If t_{pLH} and t_{pHL} refer to low-to-high and high-to-low output transitions, the overall delay t_p, defined as the average of two delays [34], is:

$$t_p = \frac{t_{pLH} + t_{pHL}}{2} \qquad (3.1)$$

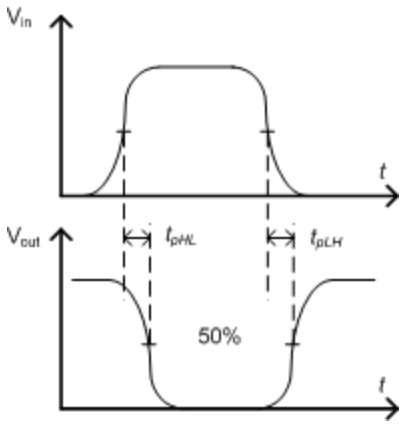


Fig. 3.4: Definition of Propagation Delay [34]

The propagation delay of the inverter shown in Fig. 3.4 can be calculated by integrating capacitor charge or discharge current as follows[34],

$$t_p = C_L \int_{v1}^{v2} \frac{dv}{i(v)}$$

where v is the voltage across the load capacitor, and v_1 and v_2 are the initial and final values of this voltage respectively. Computation of this integral is complex, since $i(v)$ is a nonlinear function of v. Fig. 3.4 shows when the input (V_{in}) changes from zero to one, the output (V_{out}) changes from one to zero in a non-linear fashion even if a linear voltage is applied to the input of the transistor. If the input voltage is less than the threshold voltage (sub-threshold region), the output current is an exponential function of the input voltage. On the other hand if the input voltage is higher than threshold voltage, the output current is a square function of the input voltage. The above equation can be simplified by replacing the $i(v)$ by a fixed current I_{av}, which is an average current over transition time. So the propagation delay can be simplified as [34],

$$t_p = \frac{C_L(v_2 - v_1)}{I_{av}}$$

Since the propagation delay is defined as the time required for the output voltage to reach 50% of the final value, the low-to-high transition voltages are $v_1 = V_{OL}$ and $v_2 = (V_{OH} + V_{OL})/2$, and the high-to-low transition voltages are $v_1 = V_{OH}$ and $v_2 = (V_{OH} + V_{OL})/2$. As a result, t_{pLH} and t_{pHL} are expressed as [34],

$$t_{pLH}, t_{pHL} = C_L \frac{(V_{OH} - V_{OL})}{2I_{av}} \qquad (3.2)$$

In order to calculate the propagation delay of the inverter, t_{pLH} and t_{pHL} should be calculated. If the input signal abruptly changes from VDD to 0, the NMOS transistor in the inverter turns off immediately, and only the PMOS transistor charges the output capacitance load C_L. Since the PMOS transistor is in the saturation region, the average charging current is given by [37],

$$I_{av} = \frac{k_p}{2}(V_{GS} - V_T)^2,$$

$$\text{where } k_p = \mu_p C_{0x} \frac{W}{L}, \; V_{GS} = VDD$$

And therefore by using equation 3.2 the t_{pLH} is [34],

$$t_{pLH} = \frac{C_L (V_{OH} - V_{OL})}{k_p (V_{DD} - V_T)^2} \quad (3.3)$$

Since the $V_{OH} = V_{DD}$ and $V_{OL} = 0$, then equation 3.3 can express as [34],

$$t_{pLH} = \frac{C_L V_{DD}}{k_p (V_{DD} - V_T)^2} \quad (3.4)$$

A similar relation can be derived for t_{pHL} [34],

$$t_{pHL} = \frac{C_L V_{DD}}{k_n (V_{DD} - V_T)^2} \quad (3.5)$$

Where k_n is given by [37],

$$k_n = \frac{\mu_n C_{ox}}{2} \frac{W}{L}, \; V_{GS} = VDD$$

By using equations 3.1, 3.4 and 3.5, the overall propagation delay relation is given by [34],

$$t_p = \frac{1}{2}(t_{pLH} + t_{pHL}) = \frac{C_L}{2V_{DD}}(\frac{1}{k_p} + \frac{1}{k_n}) \quad (3.6)$$

Most of the time it is desirable to have the same rise and fall times respectively by scaling the PMOS transistor to make the k_p and k_n equal. In this case the t_p is given by [34],

$$t_p = \frac{C_L}{V_{DD} k} \quad (3.7)$$

Equation 3.7 shows that the delay of an inverter is proportional to the load capacitance.

The inverter delay given in 3.7 is based on the square-law MOSFET model. The square-law model is not accurate for submicron MOS transistors because a number of short-channel effects degrade the transistor behavior. One of the short-channel effects on the transistor behavior is the carrier velocity saturation in submicron technology. The velocity of the carries is given by [37],

$$v \cong \frac{\mu E}{1 + E / E_c} \quad (3.8)$$

where μ is the mobility of the electrons or holes and E is the electric field and E_c is the critical electric field. In a short-channel device the carriers enter the channel and at the present of a high electric field, they reach saturated velocity which is about$10^7 cm/s$ [39]. Fig. 3.5 shows the impact of the velocity saturation on the I-V characteristic of the CMOS transistor. As it shows, for given $V_{GS} - V_{TH}$, the short-channel device output current is less than that of the long- channel one, since the carries reach the saturated velocity with a lower V_{DS} value.

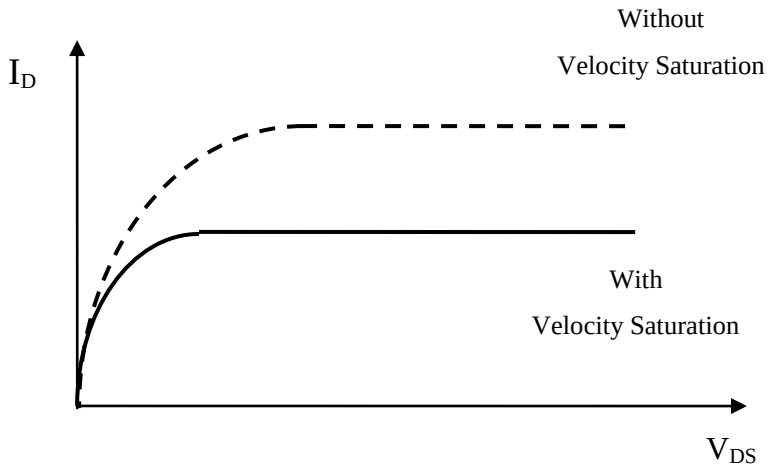


Fig. 3.5: Effect of Velocity Saturation [39]

Velocity saturation directly impacts on the transistor current drive capability and therefore the delay of the inverter. Another important short-channel effect on the MOS behavior is due to the large gate-channel vertical electric field. In fact, the voltage cross the gate-source creates a high electrical field between the gate and channel. This strong field confines the carries below the oxide-silicon and causes more collisions, thereby reducing the mobility of carriers [39]. The effective mobility is a function of the gate voltage and it is modeled by an empirical equation [39],

$$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_{GS} - V_{TH})} \qquad (3.9)$$

where μ_0 is the mobility with a low electric field, V_{GS} is the gate-source voltage, V_{TH} is the threshold voltage and θ is given by [41],

$$10^{-7} / t_{ox}(V^{-1}) \qquad (3.10)$$

where t_{ox} is the thickness of the oxide. As it is shown in 3.9, the mobility of the carriers is degraded by increasing the gate-source voltage and therefore reduce the drain-source current for a given gate-source voltage. The velocity saturation and mobility degradation in a submicron technology impacts on the I-V characteristic of transistor. As a result, the inverter delay given in 3.7 is not accurate for short channel devices. The delay of an inverter has been derived for short-channel transistors and it is given by [42],

$$t_{pShortCh} = (\frac{1}{2} - \frac{1-v_T}{1+\alpha})t_T + 0.5\frac{C_L V_{DD}}{I_{D0}} \qquad (3.11)$$

And,

$$t_T = \frac{t_{r/f}}{0.8} = \frac{C_L V_{DD}}{I_{D0}}(\frac{0.9}{0.8} + \frac{V_{D0}}{0.8V_{DD}}\ln\frac{10V_{D0}}{eV_{DD}}) \qquad (3.12)$$

where, α (alpha-power-law) is a fitting model parameter to make the drain current proportion to $(V_{GS} - V_{TH})^{\alpha}, v_T = \frac{V_{TH}}{V_{DD}}, I_{D0}$ is the drain current at $V_{GS} = V_{DS} = V_{DD}, V_{D0}$ is the drain saturation voltage at $V_{GS} = V_{DD}$ and t_T is the input signal transition time.

By using this observation, a chain of these inverters is proposed as a tunable delay line whose delay can be changed by turning on or off the capacitor load of each inverter. These inverters could be cascaded in binary, thermometer or hybrid fashion. Fig. 3.6. shows the cascaded delay cells in a binary way.

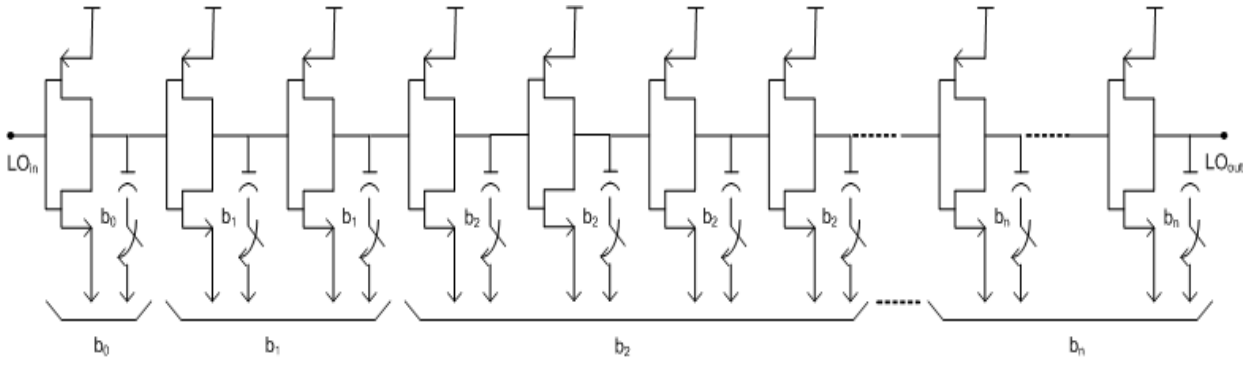


Fig. 3.6: Delay Chain

The difference between LO signals in the output of the delay chain when all switches are off (minimum delay) and on (maximum delay), is the total delay of the chain as shown in Fig. 3.7.

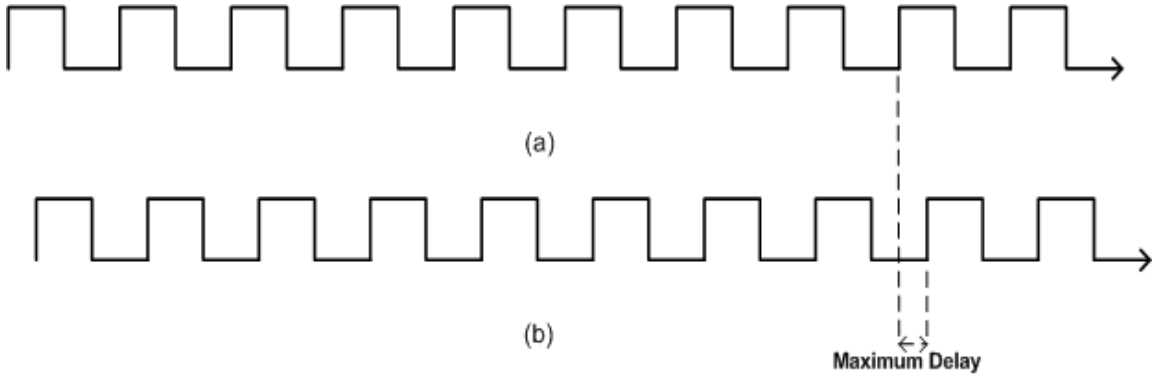


Fig. 3.7: (a) LO Signal in the Output of Delay Chain when All Switches are Off. (b) LO Signal when All Switches are on

The delay resolution (LSB) is a function of the load capacitance C_L. A small C_L reduces the minimum delay (LSB).

One could use the 3.7 or 3.11 to design the delay cell for the desire LSB delay. Fig. 3.8 shows the delay cell with an input and output load. As it is shown, transistor "*c*" is used as a load capacitor and transistor "*s*" works as a switch by setting its gate voltage high or low (*sw*=high/low on/off).

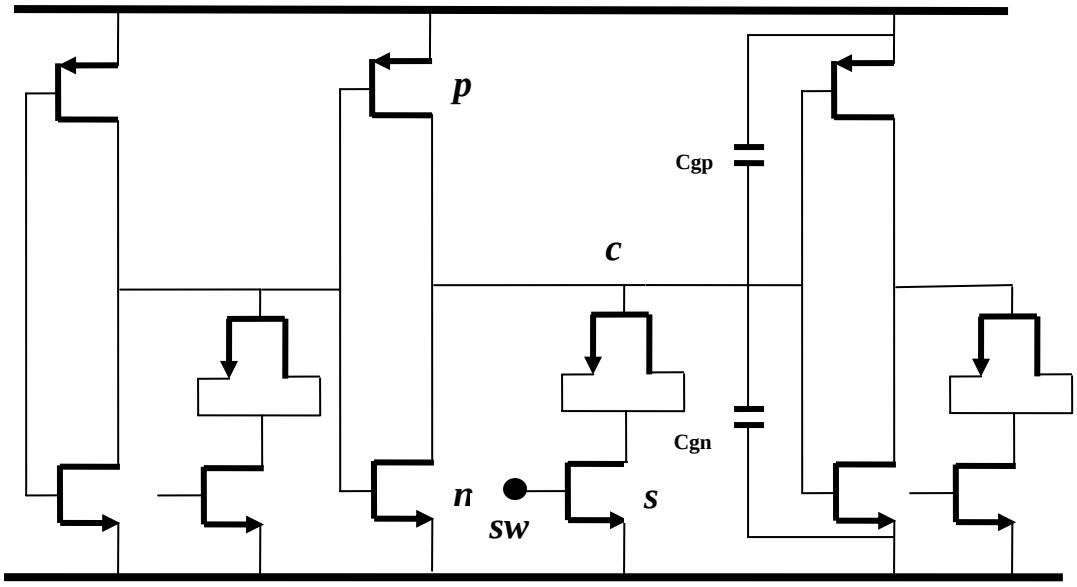


Fig. 3.8: Delay Cell

The actual load at the output of the inverter is composed of the gate capacitance of transistor "*c*" and the gate capacitors of "*p*" and "*n*" transistors of the next stage. So, the total load capacitance when the *sw*=high is,

$$C_{L-on} = C_{ox}W_cL_c + \frac{2}{3}C_{ox}(W_nL_n + W_pL_p) \qquad (3.13)$$

Matching the rise and fall time of the inverter is obtained by making the $\frac{(W_p / L_p)}{(W_n / L_n)}$ equal to the ratio of $\beta = \mu_n / \mu_p$ where μ_n and μ_p are the mobility of the electrons and holes respectively. Therefore the load capacitance is,

$$C_{L-on} = C_{ox}W_cL_c + \frac{2}{3}C_{ox}(\beta+1)W_nL_n \qquad (3.14)$$

If *sw* is set to low (switch off), the load capacitance of the inverter is reduced by the gate capacitance of the "*c*" transistor then,

$$C_{L-off} = \frac{2}{3}C_{ox}(\beta+1)W_nL_n \qquad (3.15)$$

So, the LSB delay is,

$$t_{LSB} = t_{p-on} - t_{p-off} \qquad (3.16)$$

By using 3.11 the LSB delay is calculated as,

$$t_{LSB} = (k_P k_T + 0.5)\frac{(C_{L-on} - C_{L-off})V_{DD}}{I_{D0}} = (k_P k_T + 0.5)\frac{C_{ox}W_cL_cV_{DD}}{I_{D0}} \qquad (3.17)$$

where k_P, k_T are,

$$k_P = \frac{1}{2} - \frac{1-v_T}{1+\alpha}, k_T = \frac{0.9}{0.8} + \frac{V_{D0}}{0.8V_{DD}}\ln\frac{10V_{DD}}{eV_{DD}} \qquad (3.18)$$

And I_{D0} is the drain current when $V_{GS} = V_{DS} = V_{DD}$, so I_{D0} is given by,

$$I_{D0} = \frac{1}{2}\mu_{eff}C_{ox}\frac{W_n}{L_n}(V_{DD} - V_{TH})^{\alpha} \qquad (3.19)$$

Therefore, the LSB delay is given by,

$$t_{LSB} = (k_P k_T + 0.5)\frac{2W_cL_cV_{DD}}{\mu_{eff}\frac{W_n}{L_n}(V_{DD} - V_{TH})^{\alpha}} \qquad (3.20)$$

If $A_n = W_n L_n$ and $A_c = W_c L_c$, therefore the minimum delay is expressed by,

$$t_{LSB} = (k_P k_T + 0.5)\frac{2L_n^2 A_c V_{DD}}{\mu_{eff} A_n (V_{DD} - V_{TH})^{\alpha}} \qquad (3.21)$$

where μ_{eff} is given in 3.9.

The LSB delay can be calculated by using the long-channel model given in 3.7 as follows,

$$t_{LSB} = \frac{2L_n^2 A_c}{\mu_0 A_n V_{DD}} \qquad (3.22)$$

For a given LSB delay, one could use 3.21 or 3.22 to calculate the ratio of c / n transistors area. The integrity of the LO signal needs to be investigated at the operating frequency as well. If the delay cell is supposed to work at different frequencies in a multi-standard radio, the integrity of the LO signal should be checked for the maximum frequency operation. Fig.3.9 shows how the rise/fall time could impact the LO signal integrity. Picture (a) in the Fig.3.9 is the input LO signal to the delay cell. Picture (b) shows how LO signal is getting attenuation along the delay cell chain since the rise/ fall time is larger than the pulse width. In fact, the LO signal does not reach full swing and experience more attenuation in the following delay cells. The last graph (c) shows the LO signal passing through the delay cells with the transition time less than the LO signal's pulse width. As it is shown in (c), the signal integrity is maintained along the delay chain. In fact, in order to maintain the integrity of the LO signal, one should make sure that the rise/fall time of the delay cell is small enough to let the LO signal well settle down within the pulse width. The transition time in an inverter is given in 3.12 for the short-channel device [42].

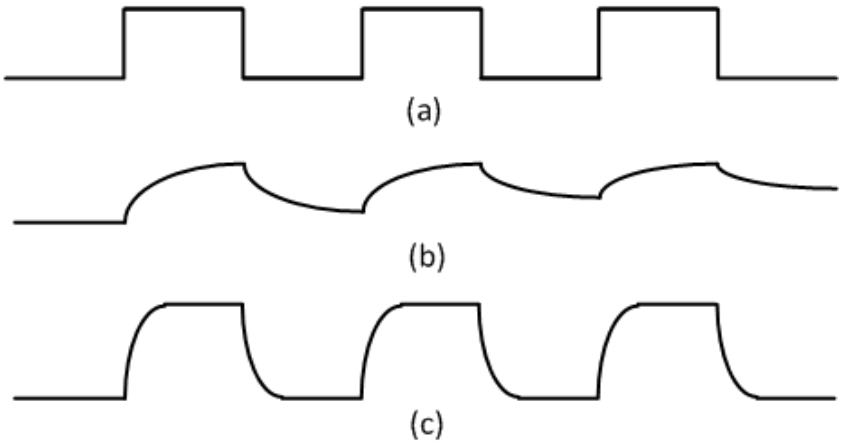


Fig. 3.9: (a) LO Signal (b) Rise/Fall Time Larger Than Pulse Width (c) Rise/Fall Time Within Pulse Width

By using 3.12, 3.14 and 3.19, the transition time can be written as follows,

$$t_T = \frac{2L_n^2\left(\frac{W_c L_c}{W_n L_n} + \frac{2}{3}(\beta+1)\right)V_{DD}}{\mu_{eff}(V_{DD}-V_{TH})^{\alpha}} k_T \qquad (3.23)$$

where,

$$k_T = \left(\frac{0.9}{0.8} + \frac{V_{D0}}{0.8V_{DD}} \ln\frac{10V_{D0}}{eV_{DD}}\right) \qquad (3.24)$$

The transition time of the inverter given in 3.23 shows that the minimum length for NMOS and PMOS transistors (*n*, *p*) is required in order to minimize the transition time. Therefore,

$$L_p = L_n = L_{\min} \qquad (3.25)$$

The transition time can be expressed in terms of the ratio of the "*n*" and "*c*" transistors areas as follows,

$$t_T = \frac{2L_{\min}^2\left(\frac{A_c}{A_n} + \frac{2}{3}(\beta+1)\right)V_{DD}}{\mu_{eff}(V_{DD}-V_{TH})^{\alpha}} k_T \qquad (3.26)$$

If the delay chain is supposed to work at the maximum frequency of $f_{\max}$, one should make sure that the transition time given in 3.26 is less than the pulse width within a reasonable margin. Then,

$$f_{\max} = \frac{1}{p} \qquad (3.27)$$

where p is the period of the LO signal at the maximum operating frequency. By assuming there is a 50% duty cycle for the LO signal, the pulse width is,

$$Pulse\,Width = \frac{1}{2p} \qquad (3.28)$$

Then,

$$t_T = \frac{2L_{\min}^2 (\frac{A_c}{A_n} + \frac{2}{3}(\beta+1))V_{DD}}{\mu_{eff}(V_{DD} - V_{TH})^{\alpha}} k_T < \frac{1}{2p} \quad (3.29)$$

Therefore, by assigning a value to the transition time that is less than the pulse width, the $\frac{A_c}{A_n}$ ratio can be calculated by using 3.29 as follows,

$$\frac{A_c}{A_n} = \frac{t_T \mu_{eff}(V_{DD} - V_{TH})^{\alpha}}{2L_{\min}^2 k_T V_{DD}} - \frac{2}{3}(\beta+1) \qquad (3.30)$$

By knowing the $\frac{A_c}{A_n}$ ratio, the LSB delay (minimum delay) can be calculated by using 3.21.

The channel resistance of the transistor "*s*" in Fig.3.8 might impact on the rise and fall time of the delay cell. The channel resistance of the "*s*" transistor when the *sw* is set to high is given by [37],

$$R_{ON} = \frac{1}{\mu_{eff} C_{ox} \frac{W_s}{L_s}(V_{DD} - V_{TH})} \qquad (3.31)$$

To minimize the impact of the "*s*" transistor on the rise and fall time of the delay cell, one should use a minimum length for the "*s*" transistor and make sure the time constant

due to the channel resistance is much smaller than the transition time given in 3.29. Therefore,

$$R_{ON}C_L << t_T \quad (3.32)$$

And,

$$L_s = L_{\min} \quad (3.33)$$

The power consumption of an inverter is composed of dynamic and direct path power consumption as follows [34],

$$P = P_{dyn} + P_{dp} = C_L V_{DD}^2 f + t_{r/f} V_{DD} I_{peak} f \quad (3.34)$$

where f is the frequency of the operation and I_{peak} is the maximum current from the PMOS to NMOS transistor. By using 3.12, 3.13 and 3.23 and some manipulations, the power consumption is expressed by,

$$P = C_{ox}(1 + k_{dp})(A_c + \frac{2}{3}(\beta + 1)A_n)V_{DD}^2 f \quad (3.35)$$

where,

$$k_{dp} = \frac{0.8\mu_{eff2}(\frac{V_{DD}}{2} - V_{TH})^{\alpha}}{\mu_{eff1}(V_{DD} - V_{TH})^{\alpha}} k_T \quad (3.36)$$

And μ_{eff1} and μ_{eff2} are the mobility of the electrons at $V_{GS} = V_{DD}$ and $V_{GS} = \frac{V_{DD}}{2}$ respectively. As it is shown in 3.35, the total power consumption of a delay cell is directly a function of the load capacitance (c) and the inverter transistors (n and p) sizes. So, to minimize the power consumption, the size of transistors in the delay cell (n, p and c) should be minimized for the given $\frac{A_c}{A_n}$ ratio.

3.3 Phase Shifter Temperature Calibration

The delay of the phase shifter varies by temperature since the inverter current is a function of the temperature. The current of a CMOS transistor in the saturation region is given by [37]

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)^2 = \frac{1}{2}\mu C_{ox}\frac{W}{L}V^2{}_{eff} \qquad (3.37)$$

where μ is the mobility of the electrons or holes, and depends on the type of transistor; V_T is the threshold voltage, C_{ox} is the gate capacitance per unit area and W and L are the width and the length of the gate. In equation 3.37, the C_{ox}, W, and L are independent of the temperature, but the mobility and threshold voltage varies by temperature. So the current of the CMOS transistor is a function of the temperature. This means the delay of the phase shifter which is given by 3.7 varies with temperature as well. In the case of the inverter, the V_{GS} is basically the power supply voltage (V_{DD}), in addition V_T is relatively small compare to V_{DD}. Therefore $V_{eff} \cong V_{DD}$ and it can be considered independent of the temperature variation.

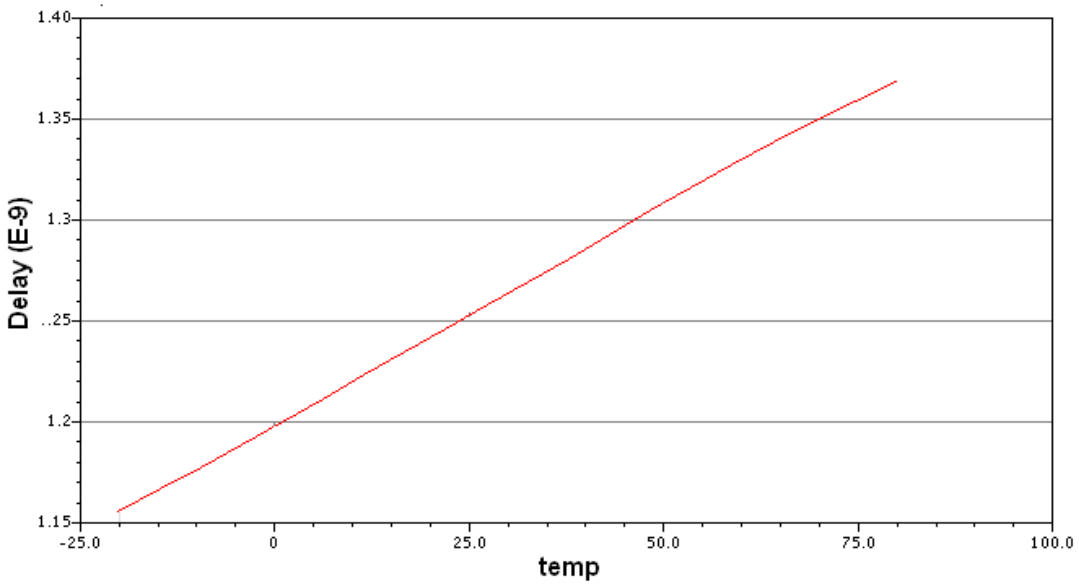


Fig. 3.10: Delay versus Temp for the Phase Shifter

Since the mobility reduces by increasing the temperature it means the delay of the phase shifter, which is given by 3.7 or 3.11, increases with the temperature. Fig. 3.10 shows the simulation result of the delay of an inverter using STMicroelectronics 90nm technology versus the temperature between -20˚ to 80˚.

In order to calibrate the phase shifter, the minimum delay of the phase shifter (LSB) should be measured once during the start-up time of the system. For an effective calibration, the temperature of the chip, which is continuously measured by an on-chip

temperature sensor, should be monitored at all times. These tasks are performed by a DSP which can calibrate the phase shifter by knowing the slope of the delay versus the temperature, like in Fig. 3.10, the initial LSB delay is measured by the DSP in the system initialization.

3.4 Quadrature Signal Generator

The synthesizer has a differential output and needs to be converted into a differential I&Q, or to a quadrature signal. There are two common ways of generating quadrature signals from the LO. One way to generate quadrature signals is having a VCO operating at twice the required frequency and then dividing it by two. The other way is using a RC-CR network. In this case, the oscillator is operated at the required frequency and the I&Q signals are generated by shifting the phase of the LO signal.

3.4.1 Divide-by-two I&Q Generator

Divide-by-two method is widely used to generate quadrature signals. Fig. 3.11 shows a divide-by-two that is composed of two latches. In this figure, the quadrature signals are generated as I_p, I_n and Q_p, Q_n from CLK and $\overline{CLK}$ which is basically coming from the differential local oscillator [35].

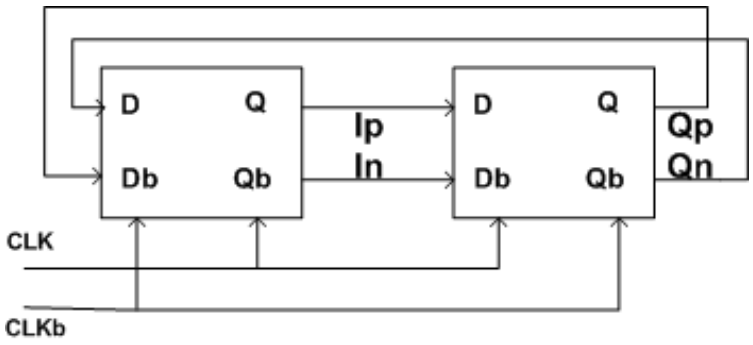


Fig. 3.11: Divide-by-Two Quadrature Generator [35]

Fig. 3.12 shows the CLK, $\overline{CLK}$ and the quadrature signals.

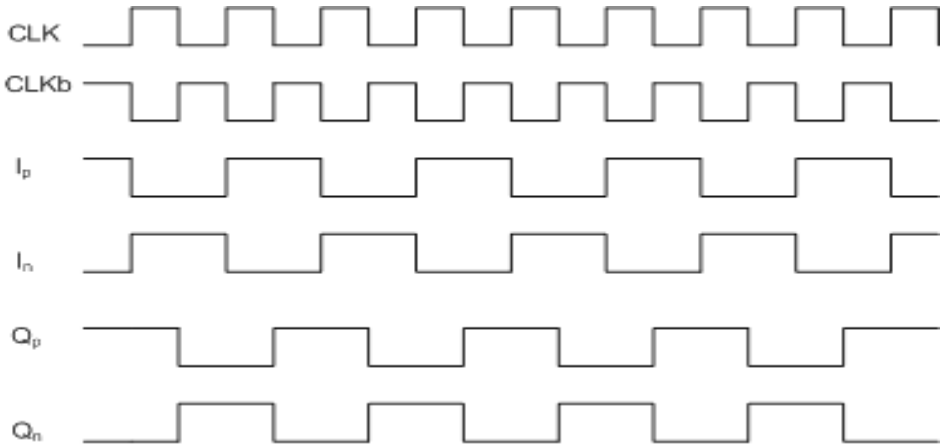


Fig. 3.12: Quadrature Signal Generated by Divide-by-Two

Latches can be implemented in different ways. CMOS implementation of the latch is based on the JK flip-flop as shown in Fig. 3.13.

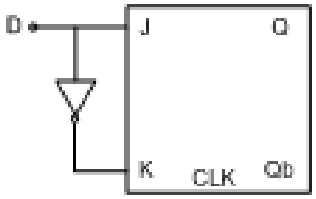


Fig. 3.13: D-Latch Based on JK-FF [34]

The JK flip-flop is built from a SR flip-flop as shown in Fig. 3.14.

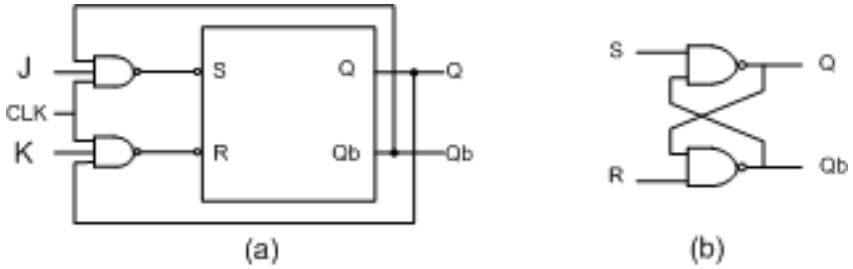


Fig. 3.14: (a) JK-FF (b) SR-FF [34]

The CMOS divide-by-two latch is used for sub-gigahertz applications due to the speed limitation.

For a high speed application, the CML (Current Mode Logic) latch is preferable as it can operate in high speed with low power consumption. Fig. 3.15 shows the CMOS implementation of a latch in CML topology.

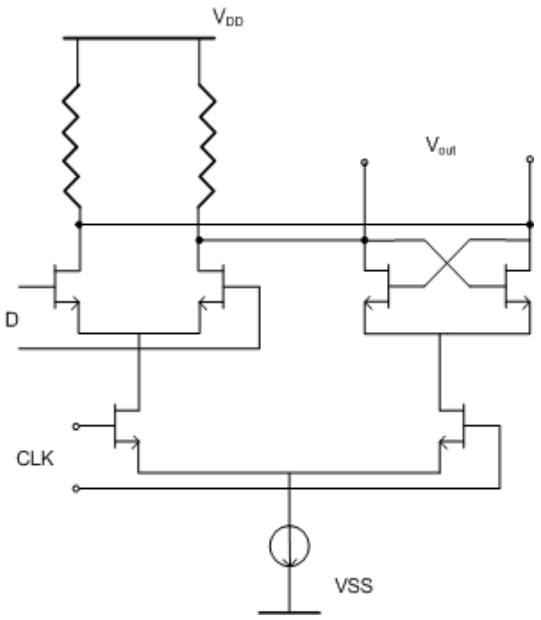


Fig. 3.15: (a) JK-FF (b) SR-FF [34]

The accuracy of quadrature signals depends on how close the two latches match and also the accuracy of the complimentarily of CLK and $\overline{CLK}$, which is basically the output of the differential VCO that operates at twice the required operation frequency.

3.4.2 RC-CR Quadrature Generator

Another popular way of generating quadrature signals is using an RC-CR network as shown in Fig. 3.16. For a sinusoidal input signal, the output phase for V_{out1} and V_{out2} are given by [35],

$$V_{out1} = \frac{j\omega RC}{1+j\omega RC}.V_{in} \Rightarrow \angle V_{out1} = \frac{\pi}{2} - \tan^{-1}(\omega RC)$$

$$V_{out2} = \frac{1}{1+j\omega RC}V_{in} \Rightarrow \angle V_{out2} = -\tan^{-1}(\omega RC)$$

And therefore,

$$\angle V_{out1} - \angle V_{out2} = \frac{\pi}{2} \qquad (3.38)$$

As it is shown in 3.38, the phase difference for two outputs, V_{out1} and V_{out2}, is 90 degrees for all frequencies.

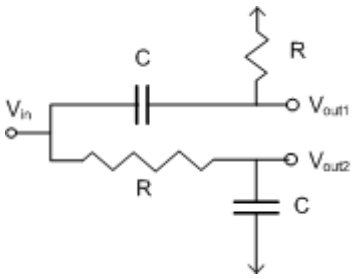


Fig. 3.16: RC-CR Quadrature Signal Generator

Only if the amplitude is the same for V_{out1} and V_{out2}, Given that:

$$\omega = \frac{1}{RC}$$

Therefore, if the absolute value of RC varies with the temperature or process, the frequency, wherein the amplitudes of quadrature signals are equal, varies as well.

In the LO path since there is no information in amplitude, the mismatch in amplitude can be equalized by using a limiting amplifier that is shown in Fig. 3.17. Amplitude equalizing in a high frequency application becomes difficult and requires several stages of limiting amplifiers.

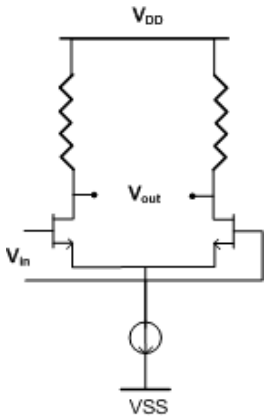


Fig. 3.17: Limiter Amplifier

Another issue with an RC-CR is the harmonic content of the input signal, namely V_{in}. If the V_{in} contains the *n*th harmonic, then V_{in} can be expressed as [35],

$$V_{in} = A_1 \cos \omega t + A_n \cos n\omega t$$

To shift the input signal by 90˚, t should be replaced by [35],

$$t = t - \frac{T}{4}$$

where T is the period and it is given by [35],

$$T = \frac{2\pi}{\omega}$$

Therefore [35],

$$V_{in}(t - \frac{T}{4}) = A_1 \cos(\omega t - \frac{\pi}{2}) + A_n \cos(n\omega t - n\pi/2)$$

So shifting the V_{in} by 90˚ requires shifting the nth harmonic by $n\pi/2$. For the RC-CR network, the equation 3.38 has shown that the phase-shifting is equal to 90˚ for all frequencies, meaning that the harmonic content of the V_{in} will cause a phase imbalance between V_{out1} and V_{out2} [35].

.

3.5 Reduction Require Phase-Shift in LO Path

In the receiver side, the local oscillator signal is multiplied by the RF signal in the down-convertor mixer to generate the base band signal. By assuming that the LO is a square wave, and the RF signal is represented by the cosine functions, the base band signal, which can be zero IF or low IF, can be expressed as,

$$V_{bb}(t) = A_{rf} \cos(\omega_{rf} t) S_{lo}(t)$$

By expanding the square LO to its harmonics, $V_{bb}(t)$ can be shown as,

$$V_{bb}(t) = A_{rf} \cos(\omega_{rf} t) 2 \sum_{n=1}^{\infty} \frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}} \cos(n\omega_{lo} t + \varphi_n)$$

where φ_n is the phase-shifting in the LO path. Due to the base band filtering, all higher harmonics are eliminated and only the fundamental LO signal multiplied by the input RF signal will remain as follows,

$$V_{bb}(t) = \frac{4}{\pi} A_{rf} \cos(\omega_{rf} t).\cos(\omega_{lo} t + \varphi_1) \quad (3.39)$$

By manipulating 3.39,

$$V_{bb}(t) = \frac{2}{\pi} A_{rf} [\cos((\omega_{rf} - \omega_{lo})t - \varphi_1) + \cos((\omega_{rf} + \omega_{lo})t + \varphi_1)] \quad (3.40)$$

Since the second term in 3.40 has a very high frequency and is therefore is filtered out by the base band filter, the base band signal becomes,

$$V_{bb}(t) = \frac{2}{\pi} A_{rf} \cos((\omega_{rf} - \omega_{lo})t - \varphi_1) \qquad (3.41)$$

The phase shown in 3.41 reveals the base band signal can be changed by varying the phase of the LO signal. It means that the LO signal is required to be variable from 0˚ to 360˚, which needs a large number of delay cells. LO phase-shifting should be done before the quadrature generator because doing phase-shifting on I&Q signals increases the mismatch of the quadrature signals significantly due to the mismatch of phase shifters in the quadrature paths. Fig. 3.18 shows the LO path in the two approaches, first, (a) is starting with twice the required oscillator frequency, passing through the phase shifter, and using divide-by-two to generate quadrature LO signals. The second, (b) starting with the LO operating at the required frequency, passing through the phase shifter, and then using a RC-CR network to generate the quadrature signals.

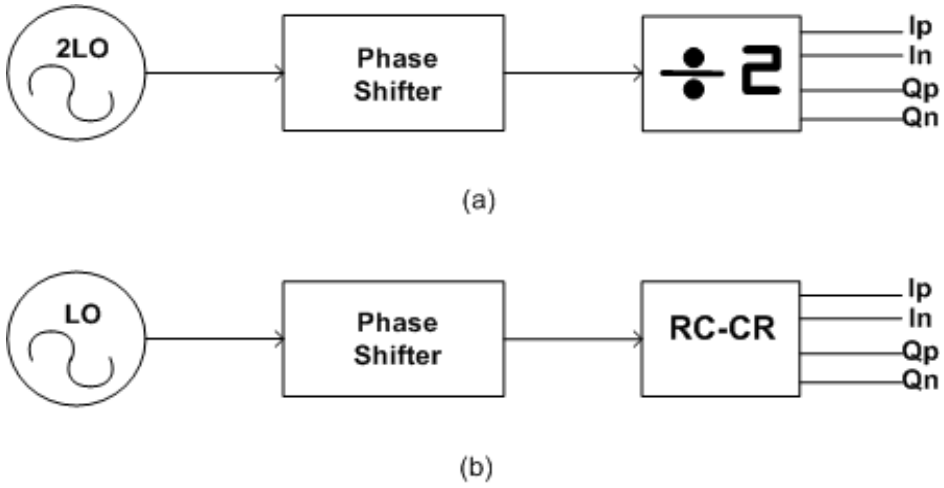


Fig. 3.18: LO Path (a) 2LO with Divide-by-Two (b) LO with RC-CR Network

In order to achieve 360˚ phase-shifting at base band, approach (a), requires 0˚-720˚ phase-shifting, because of the divide-by-two operation. In approach (b), the required phase-shifting is limited from 0˚ to 360˚. Phase-shifting with a high resolution in high frequency requires many delay cells that increase the die size and power consumption.

This is the main difficulty with approach (a), which needs a 720˚ phase-shift at a frequency twice the operational one.

3.5.1 I&Q Swap

In order to reduce the phase shift range, the phase characteristics of the I&Q signals are examined. Fig. 3.19 shows the phases of differential I&Q signals relative to each other.

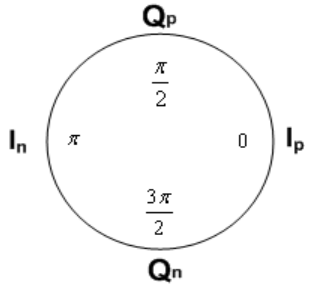


Fig. 3.19: I&Q Relative Phase Diagram

Here I_p, I_n and Q_p, Q_n are differential quadrature LO signals generated by either divide-by-two or by a RC-CR network.

Assuming that the phase shifter is able to change the phase from 0˚ to 180˚ like in the case of (a) and 0˚-90˚ like in the case of (b) in Fig. 3.15, the I&Q signals in both cases (a) and (b) change from 0˚ to 90˚ as shown in Fig. 3.20.

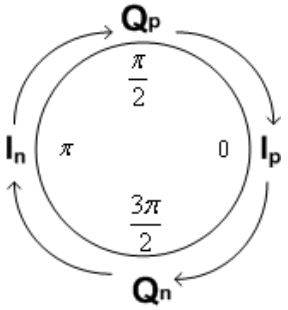


Fig. 3.20: Phase shifter Change the Phase of I&Q by 90 Degree

Now to cover the second range, $\frac{3\pi}{2} - \pi$, the I and Q signals should rotate by 90 degree clockwise. So, I_p is swapped with Q_n, Q_n with I_n and I_n with Q_p and then by varying the phase of the LO by phase shifter from 0˚ to 90˚. The I&Q phase changes from

$\frac{3\pi}{2}$ to π relative to their original phase as shown in Fig. 3.21 (arrows outside the circle represent the phase shift of the I&Q signals due to the phase shifter).

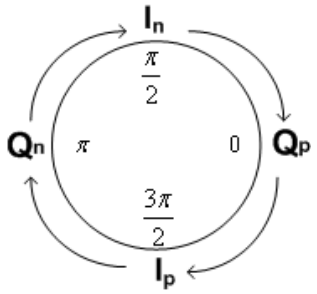


Fig. 3.21: Phase of I&Q Signals Varying from 270 to 180 Degree Relative to Their Original Phase

Swapping I_p with I_n and Q_p with Q_n (rotate 90 degree clockwise), the third range, $\pi - \frac{\pi}{2}$ relative to the original phase of the I&Q, can be covered if the LO phase is varying from 0˚ to 90˚ as shown in Fig. 3.22.

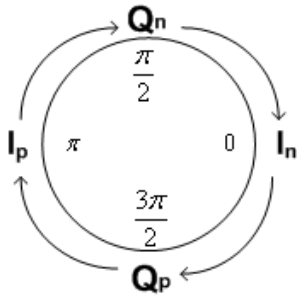


Fig. 3.22: Phase of I&Q Signals Varying from 180 to 90 Degree Relative to Their Original Phase

By following the same idea (rotating I&Q by 90 degree), the last range, $\frac{\pi}{2} - 0$, can be covered by swapping I_p with Q_p, Q_p with I_n, I_n with Q_n and Q_n with I_p as it shown in Fig. 3.23.

It has been shown so far that by proper I&Q swapping the required phase-shifting range for the phase shifter in Fig. 3.18, reduces approach (a) to 180˚ from 720˚ and for approach (b) it reduces to 90˚ from 360˚ respectively, which is one fourth of original ranges for both approaches.

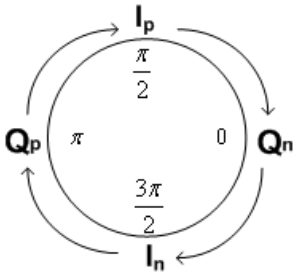


Fig. 3.23: Phase of I&Q Signals Varying from 90 to 0 Degree Relative to Their Original Phase

Table 3.1 shows the swapping summary for each region.

Table 3.1: I & Q Swap in Different Regions

Region	$0-\frac{3\pi}{2}$	$\frac{3\pi}{2}-\pi$	$\pi-\frac{\pi}{2}$	$\frac{\pi}{2}-0$
I_p Swap	$I_p \rightarrow I_p$	$I_p \rightarrow Q_n$	$I_p \rightarrow I_n$	$I_p \rightarrow Q_p$
Q_p Swap	$Q_p \rightarrow Q_p$	$Q_p \rightarrow I_p$	$Q_p \rightarrow Q_n$	$Q_p \rightarrow I_n$
I_n Swap	$I_n \rightarrow I_n$	$I_n \rightarrow Q_p$	$I_n \rightarrow I_p$	$I_n \rightarrow Q_n$
Q_n Swap	$Q_n \rightarrow Q_p$	$Q_n \rightarrow I_n$	$Q_n \rightarrow Q_p$	$Q_n \rightarrow I_p$

Fig. 3.24 shows the complete LO Chain for both approaches (a) and (b) in Fig. 3.18.

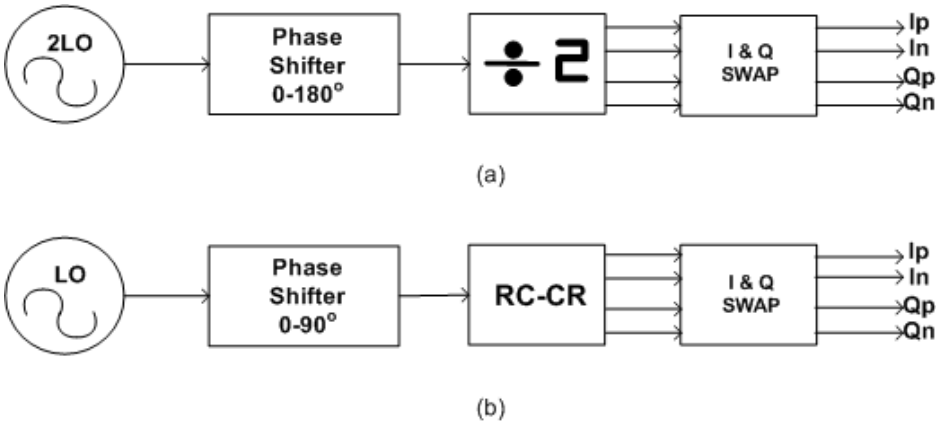


Fig. 3.24: Complete LO Chain with Required Phase-Shifting for Phase Shifters in Case (a) and (b)

Practically, the phase shifter should cover a larger range due to the process variability and temperature variations. Since the I&Q swap technique is used to cover the whole range from 0˚ to 360˚, the phase shifter needs to be calibrated in order to determine at what

digital input setting the phase is changed by 90˚. One way is to leak the output of the transmitter through a switch to the receiver input (LNA) and measure the digitized base band signal phase in the DSP when the phase shift is set to zero. Then change the phase of the phase shifter to achieve 90˚ phase-shifting. This process can be done in the initialization time or in idle time of the system.

3.6 Mixer and Combiner

As shown in Fig. 3.1 for a *n*-by-*m* beam-forming receiver, there are *m* mixers and combiners. Each mixer receives *n* LO signals with different phases and *n* RF signals from the splitters. The mixer is based on the Gilbert mixer concept shown in Fig. 3.25.

It is seen that the input differential RF signal is applied to the bottom transistors that modulate the biasing current going to the top transistors. The LO signal is applied to the top transistors that switch the modulated current.

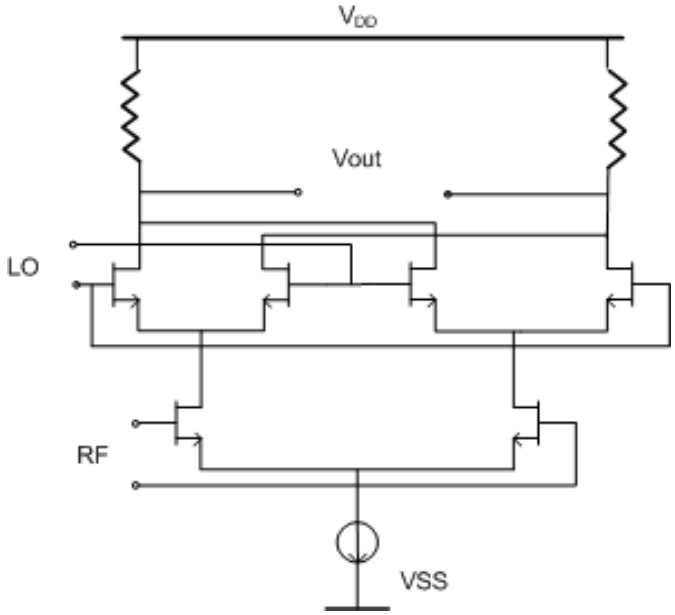


Fig. 3.25: Gilbert Mixer

The switched current converts to an output base band voltage in the resistive load. By using *n* of these mixers that share the same resistive load, the *n* input RF signals with *n* LO signals down-converts and combines together. Fig. 3.26 shows the core of the Gilbert mixer and its symbol.

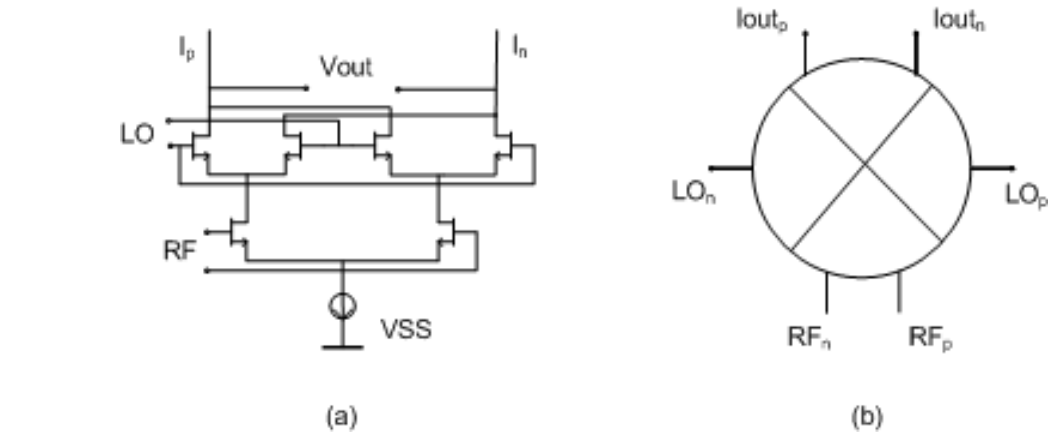


Fig. 3.26: Complete LO Chain with Required Phase-Shifting for Phase Shifters in Case (a) and (b)

Fig. 3.27 shows down-convertor mixers and a combiner which is composed of *n* mixers that share the output load. The switched current of each mixer is added in the output resistive load.

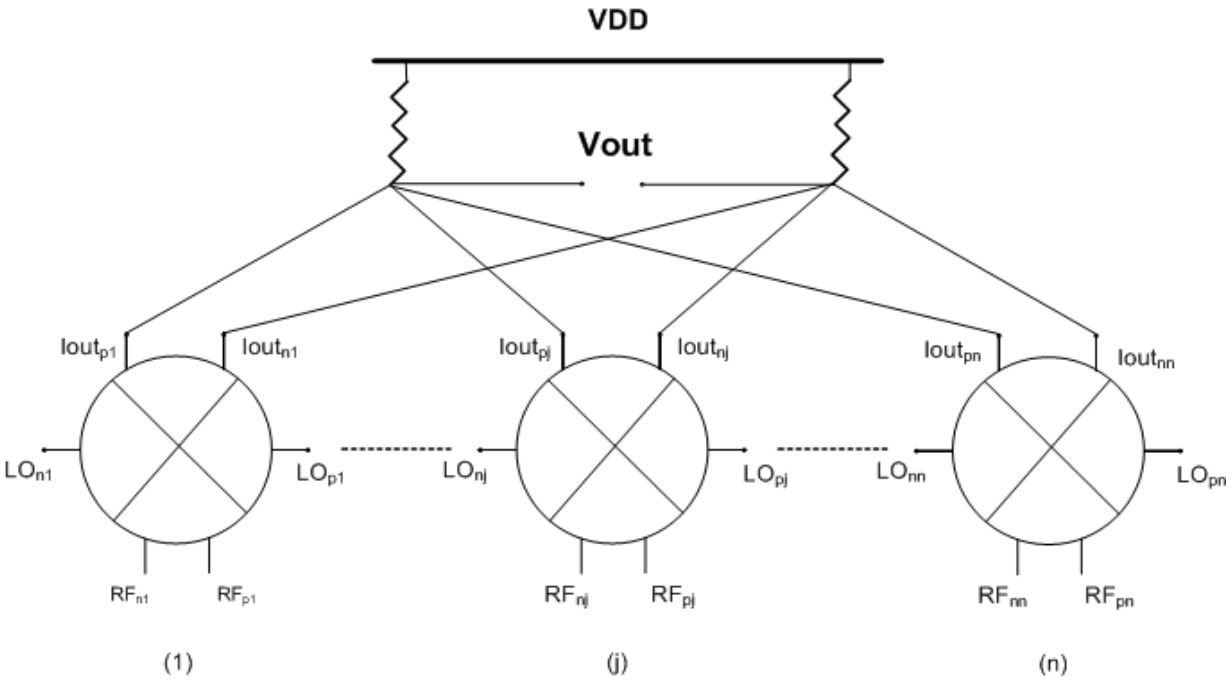


Fig. 3.27: Output of *n* Mixers Combined Together in Resistive Load

3.7 LNA and Splitter

The LNA (Low Noise Amplifier) is the first stage in the receiver. The LNA has a major impact on the overall receiver noise figure as is shown from Firii's equation [18].

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} ..... + \frac{NF_n}{G_1 ..... G_{n-1}} \qquad (3.42)$$

Where NF_1 and G_1 are the noise figure and gain of the LNA (first stage of amplification) respectively. It is obvious from (3.42) that the noise figure of the LNA is directly added to the overall receiver noise figure with no attenuation. This proves having a low noise amplifier at the input of the receiver is necessary to achieve the required signal to noise ratio at the output. The simplified circuit shown in Fig. 3.28 is the cascode differential LNA, which is the most popular topology. A differential architecture improves the power supply rejection and cascoding helps to increase the input-output isolation. Depending on the linearity requirements the LNA load can be a resistor or a resonance tank.

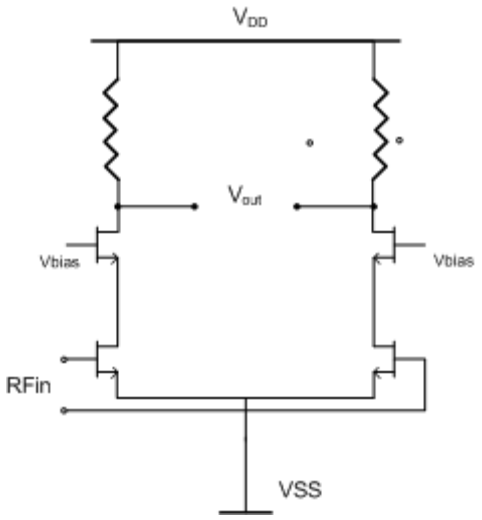


Fig. 3.28: Cascode Differential LNA

The resonance tank increases the output swing and improves the linearity of the LNA, but using a resonance tank makes the LNA narrow band due to the frequency response of the resonance tank.

A splitter amplifier is needed to provide a controllable amplified signal from each antenna to the mixers in the on-chip beam-forming receiver that is shown in Fig. 3.1. For m beams or separate base band signals, the signal received from each antenna after

amplification by the LNA should split to m outputs. Fig. 3.29 shows the splitter amplifier with two outputs. The number of outputs can easily increase by adding more cascode transistors. The gain of each output can be adjusted by adding some cross switches to reduce the gain of each output independently.

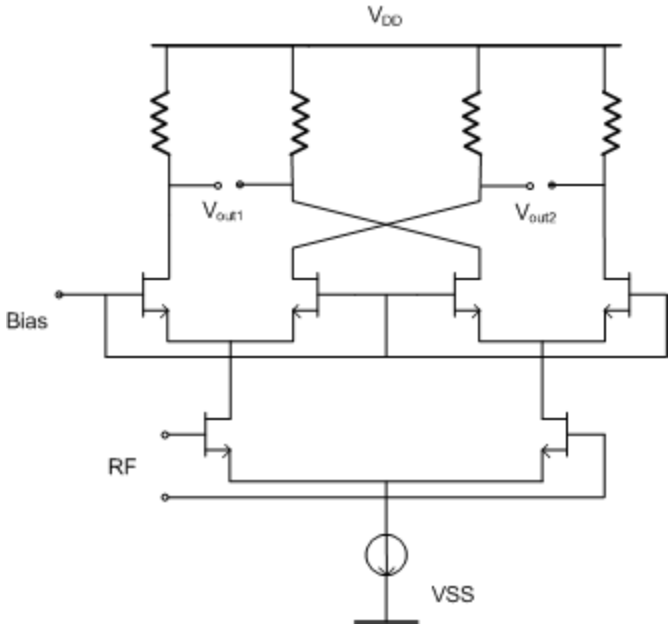


Fig. 3.29: Splitter Amplifier with Two Outputs

Chapter 4 2-by-2 MIMO Receiver

In this chapter, the ideas developed in the previous chapter are applied to a specific example of a 2-by-2 MIMO (Multiple Inputs Multiple Outputs) receiver.

Fig. 4.1 shows the block diagram of the 2-by-2 MIMO wide band receiver that was designed using STMicroelectronics 90nm CMOS technology. There are two LNAs connected to an array of two antennas. Each LNA has two control bits to set their gain.

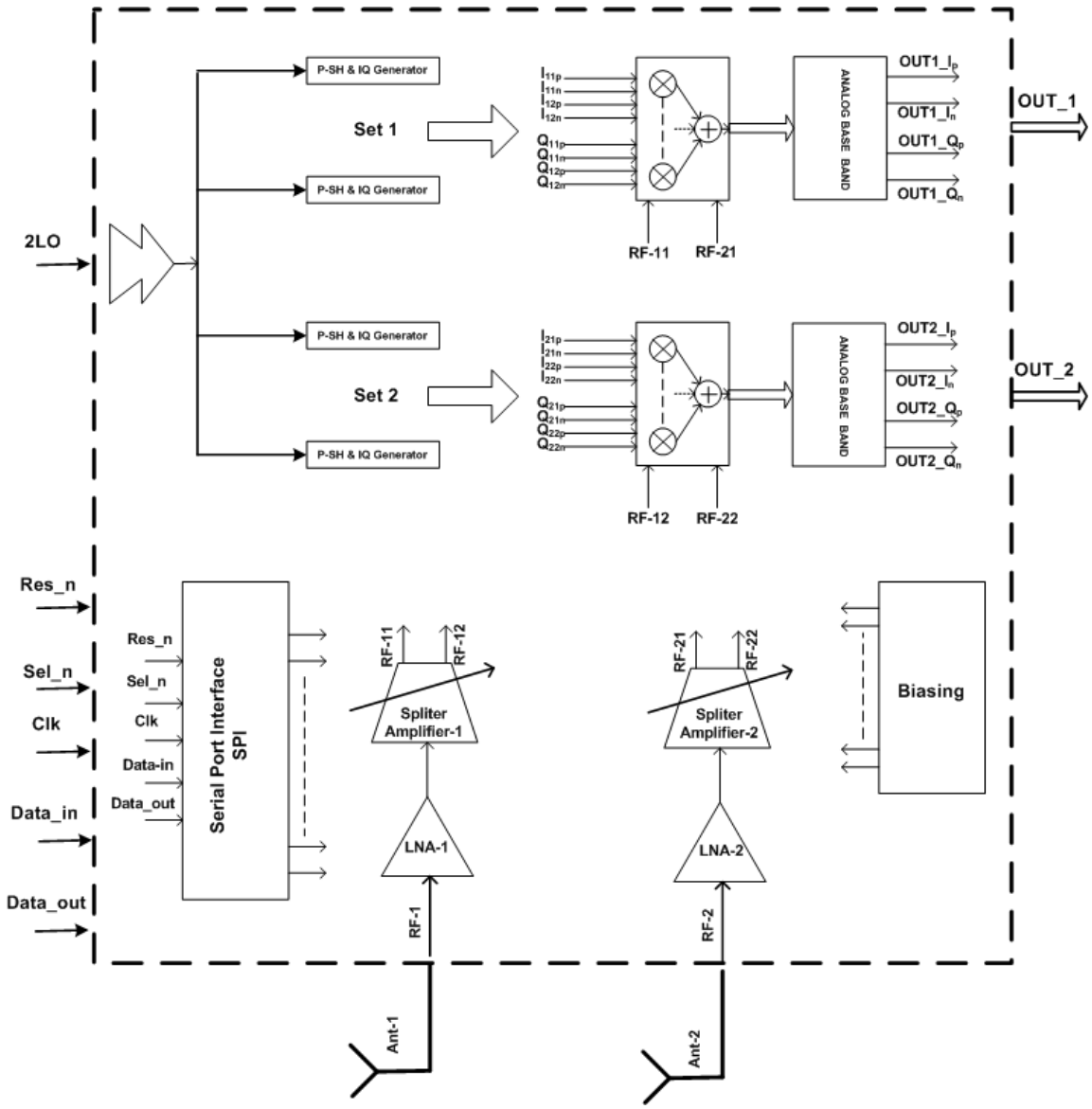


Fig. 4.1: Top Level Schematic of 2-by-2 Receiver

The gain of the LNA can change from 34dB to 22dB in about 4dB steps with less than a 2dB noise figure. The output of each LNA goes to the splitter amplifier that has two outputs going to the two sets of mixers and combiners. The gain of each splitter amplifier output has 12dB of dynamic range with eight different gain settings that are controlled by three bits. There are two sets of I&Q mixers and combiners that create two base band signals going to the base band buffers. The LO chain is based on the 2LO architecture that is shown in Fig. 3.18 (a). The 2LO signal is applied to the chip from the external signal generator. To communicate with the chip to set about 60 control bits, there is an on-chip digital Serial Peripheral Interface (SPI). There are two different power supplies using in the chip. The 1.2V power supply is used by the LO-Chain and SPI, and the 2.5V is used by the RF and Analog blocks.

4.1 LO Chain

Fig. 4.2 shows the LO chain which is composed of the phase shifter, divide-by-two and I&Q swap. Four of these individual LO chains are needed because the chip has two inputs and two outputs.

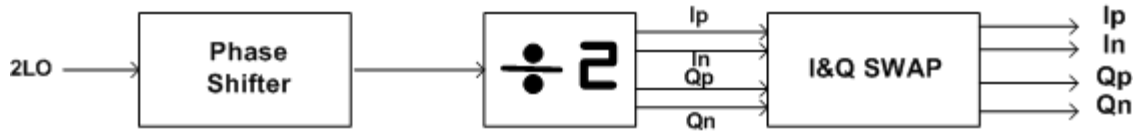


Fig. 4.2: Top Level of LO Chain

The external signal, 2LO, is applied to the chip and after buffering, it passes to the four LO chains. Fig. 4.3 shows the top level diagram of the phase shifter which is based on the 2LO phase shifter approach illustrated in Fig. 3.18 (a).

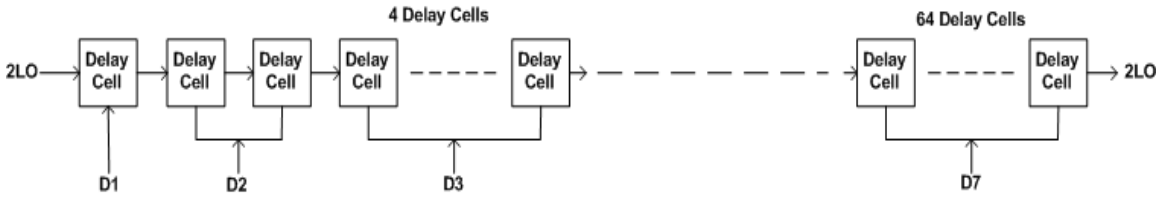


Fig. 4.3: Top Level of Phase Shifter

The phase shifter is composed of the delay cells that are controlled by seven bits that change the delay of the 2LO signal in a binary fashion.

Fig. 4.4 shows inside the delay cell. The 2LO signal goes to the delay cells that are configured in binary code. Each delay cell works, based on the inverter with a variable capacitive load as shown in Fig. 3.3. The delay cell shown in Fig. 4.4, is composed of an inverter with a capacitor connected to the switch, which is digitally controlled by seven delay bits. By setting the delay bit to one, the switch turns on and the bottom plate of the capacitor connects to ground. It increases the capacitive load of the inverter, and in turn increases the delay of the 2LO input signal. By setting the control bit to zero, the effective capacitor at the output of the inverter is reduced and so does the delay.

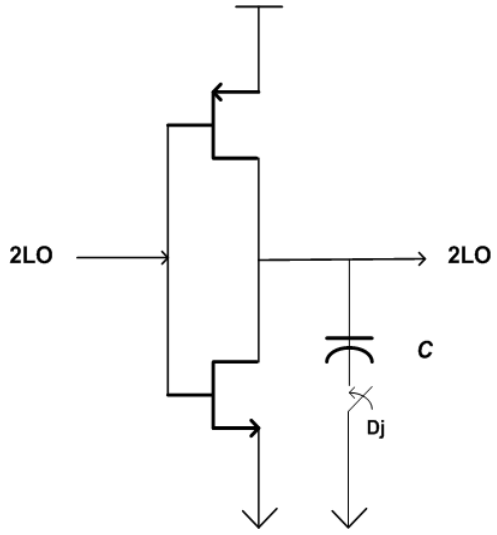


Fig. 4.4: Delay Cell

The LSB defines the minimum achievable delay, which is a linear function of the capacitive load when the VDD and k, are given.

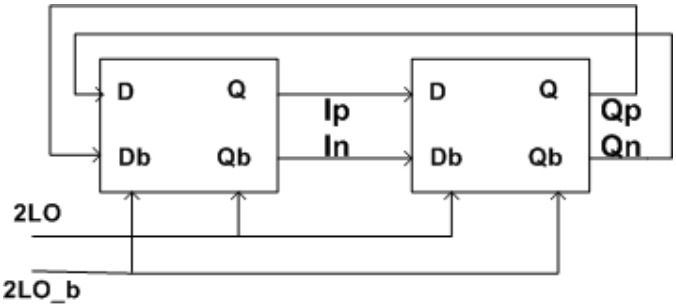


Fig. 4.5: Divide-by-Two for Creating I&Q LO signals

The second block in the LO chain is the divide-by-two circuit shown in Fig. 4.5. This circuit divides the 2LO signal by two to generate the LO signal as well as the differential I&Q signals required for the quadrature receiver.

The 2LO output of the delay block is single-ended; this can be used to generate the differential 2LO by inverting that single-ended output. An adequate buffer should be added though in order to adjust for the extra delay introduced by the inverter.

The last stage is the I&Q swap circuit to reduce the required phase-shifting by the phase shifter. This block shown in Fig. 4.6, used three bits to swap the differential I and Q signals.

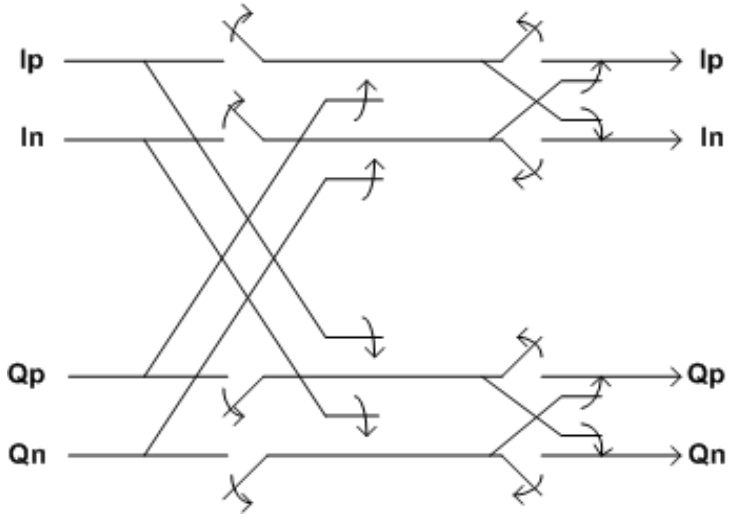


Fig. 4.6: I&Q Swap

The switches that are used in the I&Q swap block are transmission gate switches composed of a NMOS and PMOS transistor.

Fig. 4.7 shows two phase shifter delay states. The red plot shows the case where all the delay bits are set to zero. The case where only LSB is set to one is shown by the blue plot. For this simulation, there was a 5GHz signal applied as a 2LO to the LO chain and one of the outputs is plotted. As it is shown in the simulation result, the delay is about 1ps which is equivalent to 0.9° for LO=2.5GHz and 0.54° for LO=1.5GHz as calculated below,

$$\text{PhaseShift} = (1ps / \frac{1}{2.5GHz}) * 360^\circ = 0.9^\circ$$

$$\text{PhaseShift} = (1ps / \frac{1}{1.5GHz}) * 360^{\circ} = 0.54^{\circ}$$

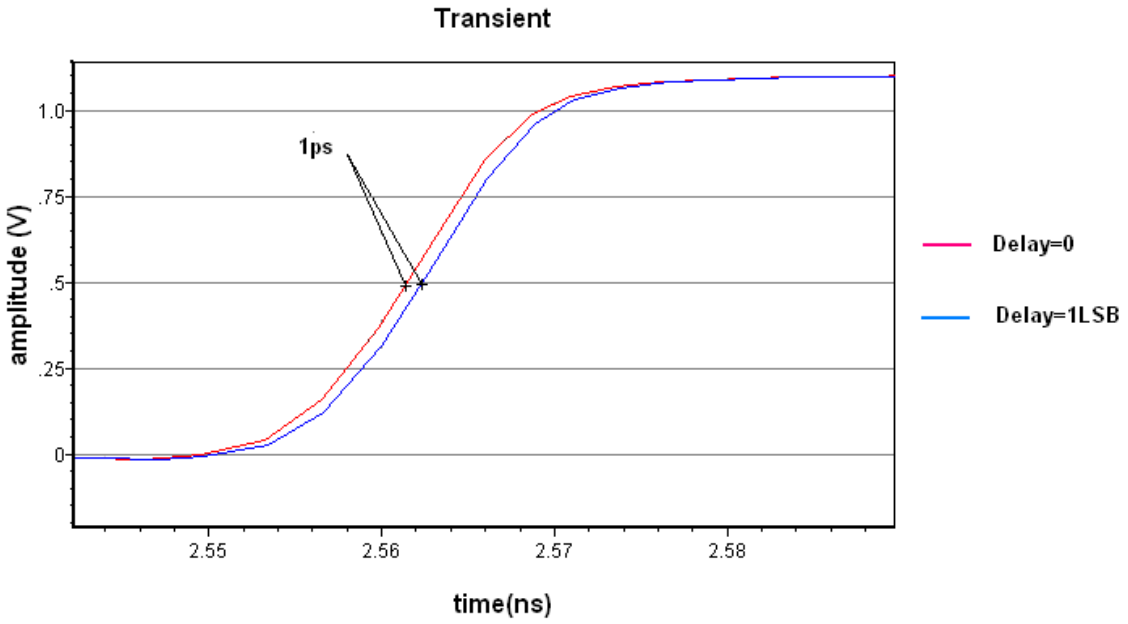


Fig. 4.7: LSB Delay

The resolution of the phase shifter (delay block), is much higher than required for most of the applications.

The delay (phase shifter) circuit should be able to phase shift the LO by 90˚ before the I&Q swap block. This can be easily achieved by using seven bits for 2.5GHz ($127 * 0.9^{\circ} \cong 114^{\circ}$). The minimum LO frequency that the delay chain can phase shifts by 90˚ can be calculated as follows:

$$1ps * 127 = 127\,ps \qquad (4.1)$$

To calculate the period of the LO the (4.1) should be multiplied by 4, so

$$127\,ps * 4 = 508\,ps \qquad (4.2)$$

Therefore, the minimum LO frequency that the delay chain can shifts by 90˚ is

$$LO_{minimum} = 1/(508\,ps) \approx 2GHz \quad (4.3)$$

$$\text{So, } 2LO \approx 4GHz \quad (4.4)$$

The maximum 2LO frequency that can be applied to the phase shifter is limited by the

speed of the delay cell. Simulation shows (schematic view) that the phase shifter operates up to 7GHz, so the MIMO receiver's upper input frequency would be 3.5GHz.

One of the advantages of using the active delay cell in the LO path over other proposed phase shifters is the capability of phase-shifting over a wide range of frequencies as it is shown in the above simulation.

The Monte Carlo simulation on the LO chain showed that due to the mismatch of the LO chain the delay variation could be higher than the minimum delay of the phase shifter as shown in the following picture. In this simulation, the phase shifter ran two hundred combinations while being set for a minimum delay (LSB).

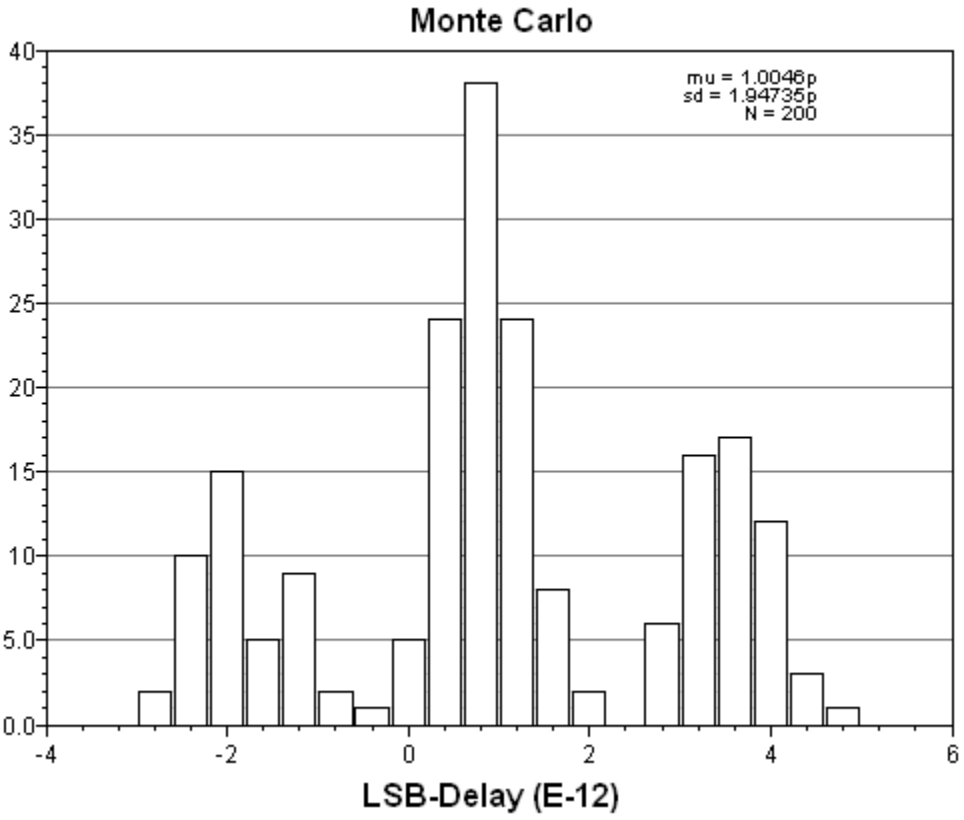


Fig. 4.8: Monte Carlo Simulation of LO Chain

The result shows a mean delay of 1ps and a standard deviation of 2ps. Therefore, the mismatch of the LO chain is limiting the minimum achievable phase-shifting of the LO chain.

Fig 4.9 shows the phase noise simulation result of the LO chain which included the phase shifter, divide-by-two and the I&Q swap. In this simulation, the 2LO signal which is applied to the phase shifter was set to 5GHz, therefore the frequency of the signal at the output of the LO chain is 2.5GHz. Fig 4.9 shows the single ended phase noise simulation result offset from 2.5GHz. As it is shown, the phase noise due to the LO chain is very low, so it has no impact on the phase noise of the VCO.

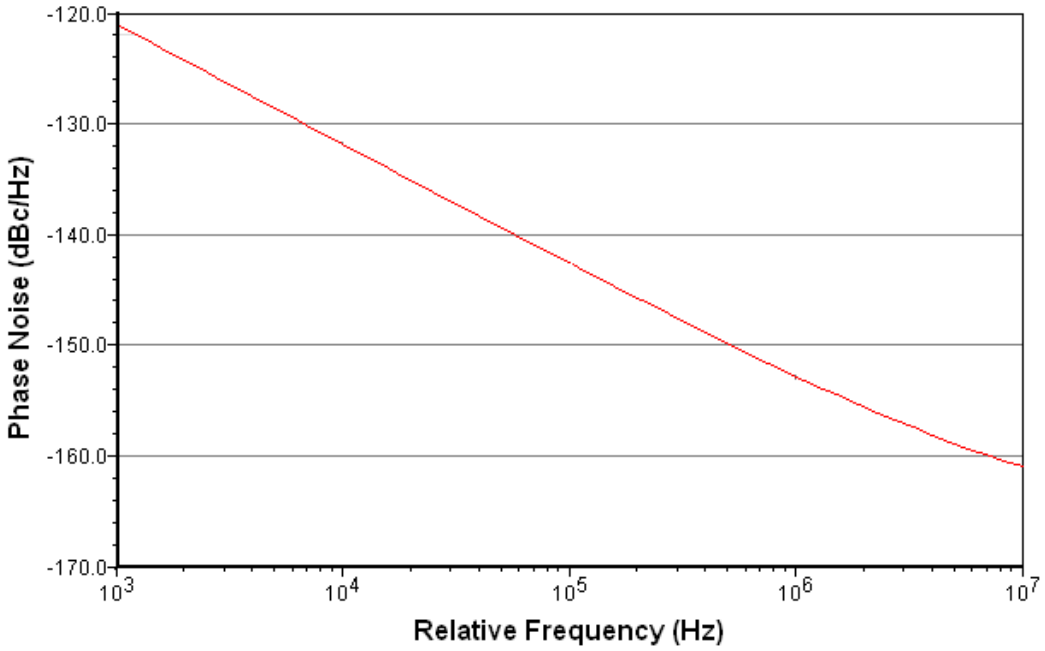


Fig. 4.9: Phase Noise of the LO Chain

For example, the phase noise requirements for the synthesizer in the GSM standard which is one of the toughest standards in consumer products, is given in the following table [40]. Comparing the GSM requirements with the phase noise result of the LO chain shows that LO phase noise has no impact on the GSM synthesizer performance.

Table 4.1: GSM Phase Noise [40]

Offset (kHz)	Phase Noise (dBc/Hz)
400	-101
600	-116
1600	-126
3000	-133

Fig. 4.10 shows the use of the I&Q swap to make, 90˚, 180˚ and 270˚ phase-shifts. The blue graph is one of the outputs of the I&Q swap block (I_p) when the I&Q block does not introduce any phase-shifting.

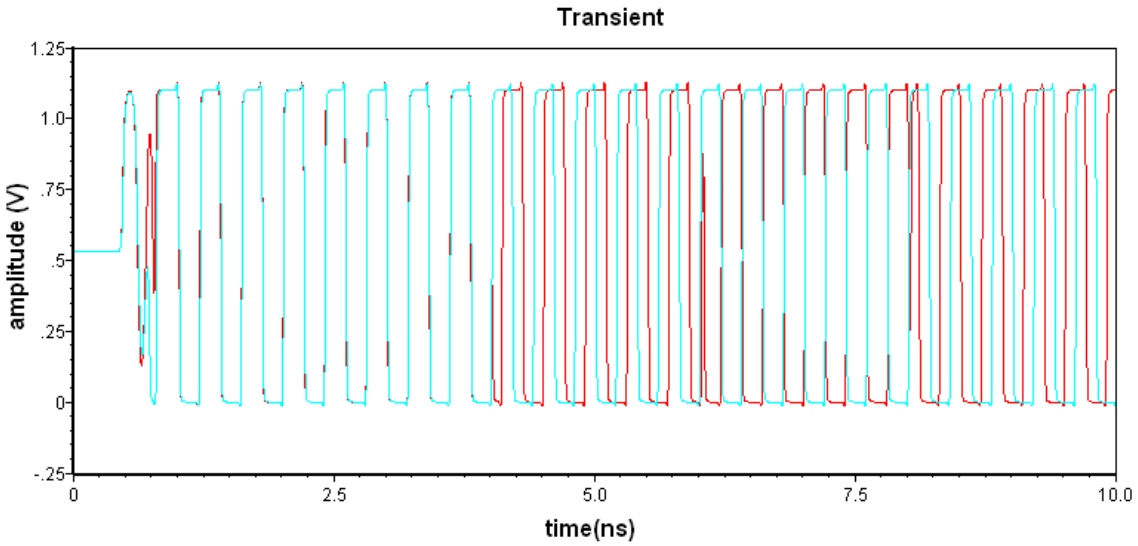


Fig. 4.10: I&Q Swap Phase-Shifting

The red graph shows the effect of the I&Q swap on the phase of the LO signal. From 0 to 4ns, the I&Q block does not make any phase-shifting. The result is both graphs, blue and red overlap each other. At 4ns, by properly setting the I&Q block control bits, it made a 90˚ phase-shift and again at 6ns by swapping I and Q signals it made a 180˚ phase-shift. Finally at 8ns the I&Q swap it made a 270˚ degree phase-shift. This process was described in Section 3.5.1.

Fig. 4.11 is the same simulation except the phase shifter is set to make a 90˚ phase- shift after 2ns of simulation. Both graphs, blue and red are in-phase up to 2ns and then there is about a 90˚ phase-shift up to 4ns. At 4ns, the I&Q swap block made another 90˚ phase-shift making the total phase-shifting to about 180˚. At 6ns the I&Q swap made a 180˚ phase-shift which made the total phase-shifting about 270˚. Finally from 8ns to 10ns the I&Q swap produces a 270˚ phase-shift and made the total phase about 360˚ causing the two graphs to fully align again.

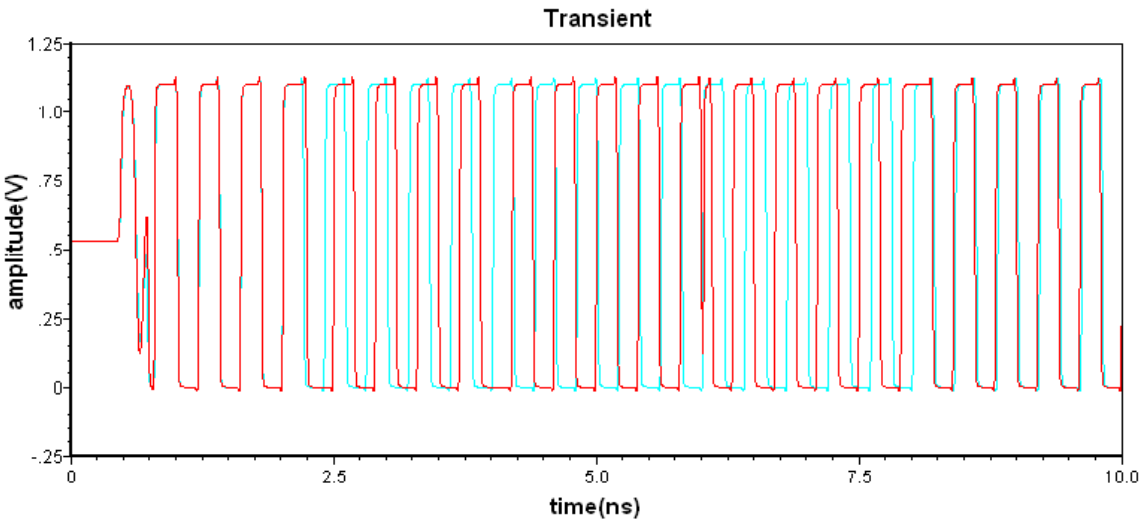


Fig. 4.11: Using Delay Cell and I&Q Swap Block

The following figure shows the settling time of the LO chain, phase shifter, divide-by-two and I&Q swap to the new phase shift. The top graph shows when the new phase shift is applied to the LO chain at the rising time of the pulse.

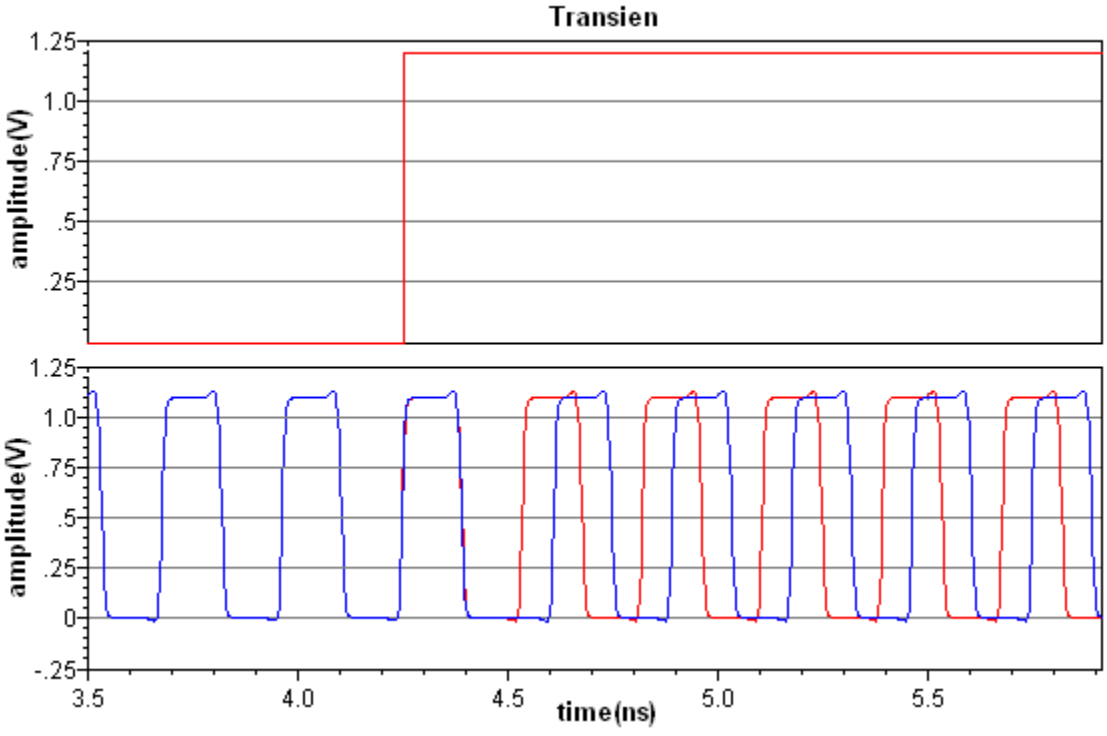


Fig. 4.12: Settling Time of the LO Chain

The red graph in the bottom picture is the output of the LO chain with no delay change which is used as a reference. The blue graph which is on top of the red graph before the new delay is applied is the output of the LO chain. The graph shows the new phase shift settled down in about one period of the signal. In this simulation 7GHz was applied as a 2LO to the delay block and therefore the output of the LO chain is 3.5GHz.

4.2 Mixer and Combiner

Fig. 4.13 shows the core of the mixer, which is based on the Gilbert mixer concept. The two bottom transistors convert the input RF signals coming from the splitter amplifier into the current. The current is then switched by the LO signals and the switched current is converted to the output voltage in the resistive load.

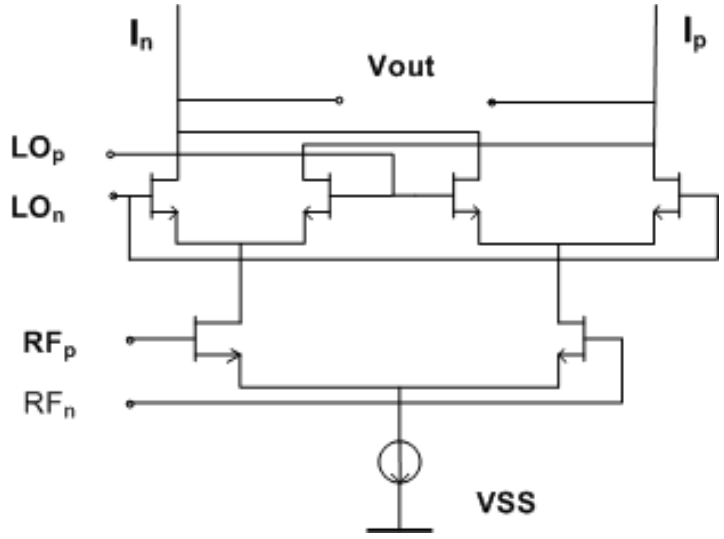


Fig. 4.13: Core of the Mixer

Fig. 4.14 shows one set of mixers that generate one of the quadrature base band signals (I_p, I_n , and $Q_p, \mathrm{Q_n}$).

For a 2-by-2 MIMO, two sets of these mixers are required to generate two base band quadrature outputs. The inputs to these mixers are one of the two outputs of each splitter amplifier and the quadrature outputs of the two LO chains.

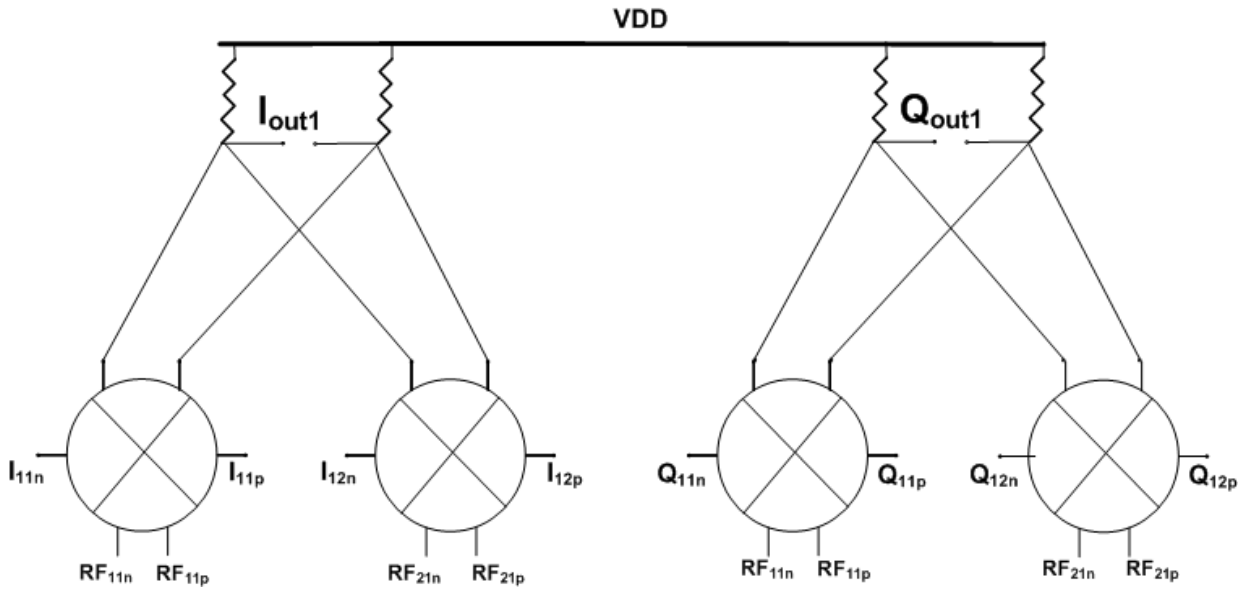


Fig. 4.14: Set of Four Mixers to Generate One Quadrature Output

The switched RF currents from the mixers core combine in the resistive load as it is shown in Fig. 4.14. The outputs of the combined signals are DC-coupled to the base band buffers.

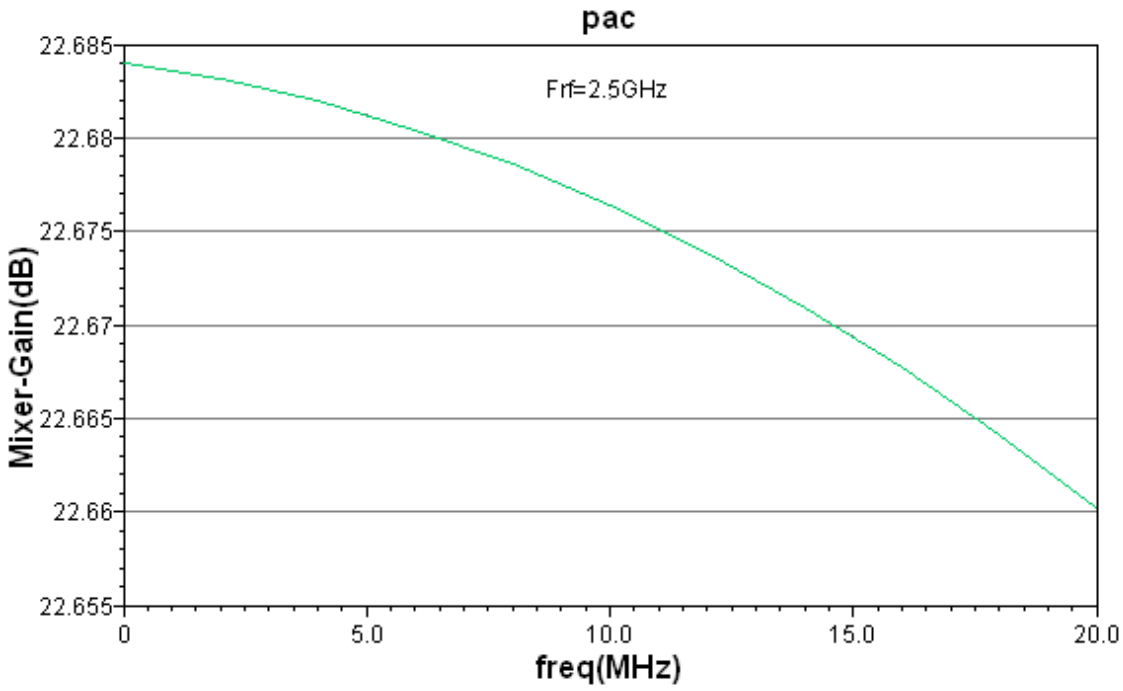


Fig. 4.15: Single Path Mixer Gain

The common mode voltage at the output of the combiner is set to 1.2V and some circuitry has been added to maintain the output common mode voltage versus temperature and process variation. Fig 4.15 shows the gain of the single path mixer where the input RF was set at 2.5GHz.

4.3 LNA

The LNA is designed to provide a high gain with a very low noise figure for a wide range of frequencies. For a 2-by-2 MIMO, two of these LNAs are used to amplify the input signals from the antenna array. Fig. 4.16 shows the core of the LNA which is based on the cascode architecture with a resistive load.

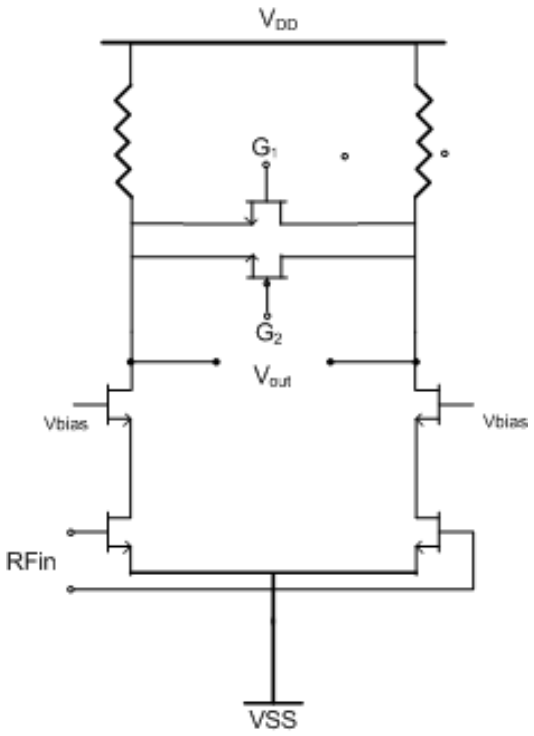


Fig. 4.16: Core of LNA

Using the resistive load makes the LNA wide band and therefore usable for a wide range of frequencies. The drain of the input transistor pairs are connected to the source of the cascode transistors. As shown in Fig. 4.16, there are two transistors in the top that are used to control the gain of the LNA. These transistors can turn on or off by using two control bits G_1 and G_2.

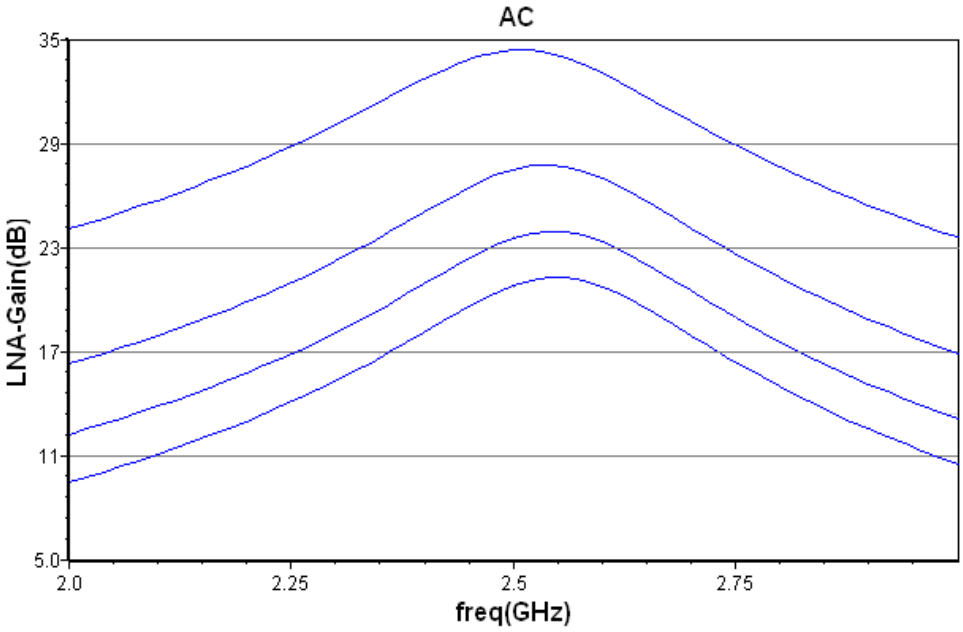


Fig. 4.17: Gain of LNA versus Control Bits

By turning the transistor on, it makes a path between the differential outputs signals to reduce the gain of the LNA. Fig. 4.17 shows that the gain of the LNA can change from 34dB to 22dB in 4 steps by two control bits.

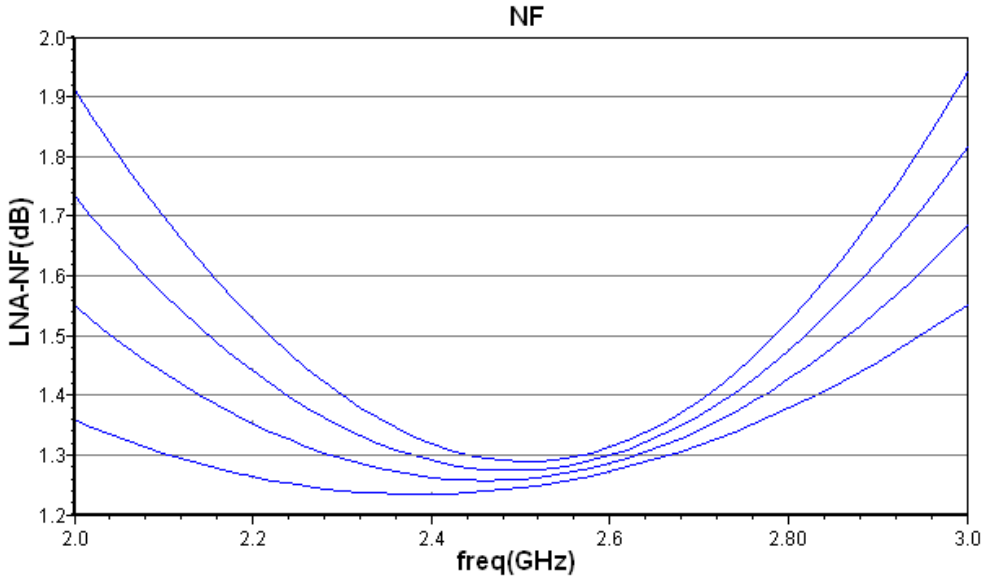


Fig. 4.18: Noise Figure of LNA for 2.5GHz Band

This simulation is done at the 2.5GHz. If the strength of the input signal is high, the gain of the LNA can be reduced by a base band processor in order to maintain the required

signal to noise ratio. The noise of the LNA is the most critical component in the overall noise of the receiver chain. Firii's equation 3.14 shows the LNA noise is directly added to the overall noise figure of the receiver chain with no attenuation. This means the noise figure of the LNA should be low enough to minimize the system noise figure. Fig. 4.18 shows the noise figure of the LNA for a 2.5 GHz band versus the gain control bits. As it is shown, the noise figure is less than 1.4dB for all the gain settings.

4.4 Splitter Amplifier

For on-chip beam-forming with m base band outputs, each RF input needs to split into m outputs with independent gain control as shown in Fig. 3.1. Then for a 2-by-2 MIMO, each RF input needs to split into two outputs to drive the two sets of mixers.

Fig. 4.19 is the core of the splitter with a three bits gain control for each output. By using three bits one can generate eight different gain levels. The gain is set by turning on or off the three transmission gate switches in the output that are binary coded. The input differential RF signals coming from the LNA goes to the input differential pairs and the output is connected to two sets of cascoded pairs.

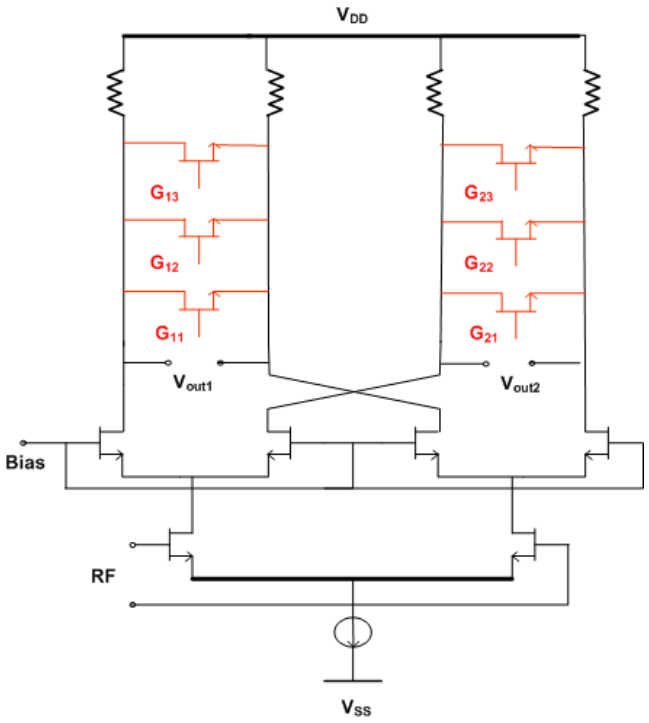


Fig. 4.19: Core of Splitter Amplifier

This architecture can be easily extended to higher number of outputs by increasing the number of the cascode pair transistors. The output of cascoded transistors goes to two sets of resistive loads.

Fig. 4.20 shows the gain of one of the outputs versus the control digits at 2.5GHz. In this example the total gain of the LNA and splitter amplifier has been simulated.

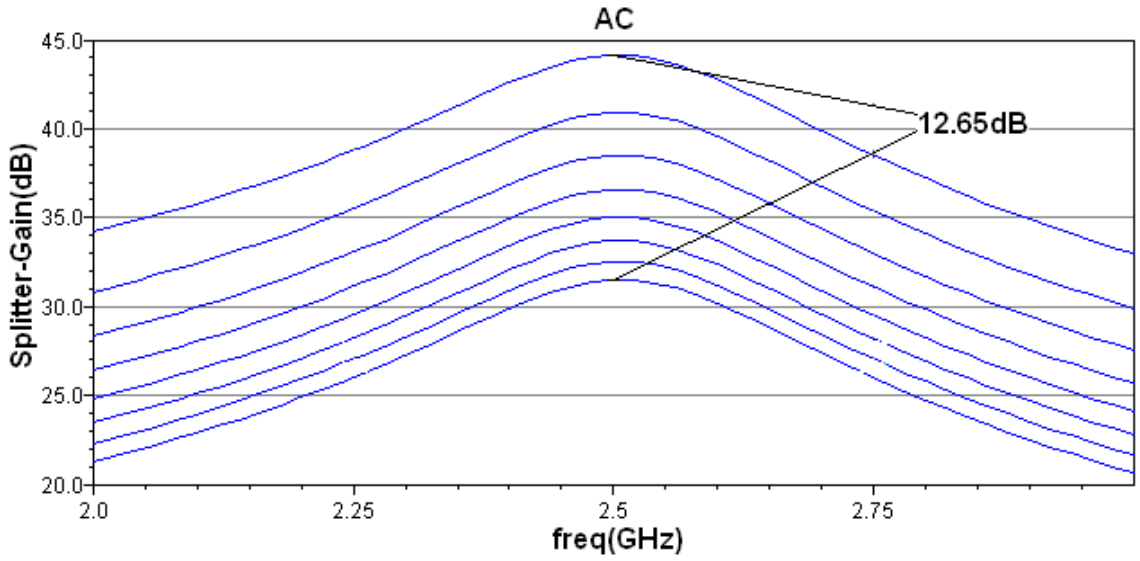


Fig. 4.20: Gain of Splitter versus 3 Bits Controllers

While the LNA gain is constant and set to maximum, the splitter gain is varying by three control bits. It is seen that there is about a 12dB gain variation that is controlled by these bits.

4.5 Base Band Buffer

The base band buffer is needed in order to drive off-chip components and capacitors, as well as the on-chip parasitic capacitor of the pad. The base band buffer is composed of the unity gain Op-Amp and output driver. The unity gain buffer isolates the output of the mixers from the output driver. The output driver is capable of driving capacitive load up to 100pF at 20MHz.

4.6 Serial Peripheral Interface

A digital control interface is needed since there are about 60 control bits. This makes it impossible to have separate pins for each of them. The SPI is controlled and

programmed by the DSP or computer through the Clk, Data_In, Data_Out, Sel_n and Res_n pins as shown in Fig. 4.21. The SPI is capable of being written or read by the DSP through the Data_In and Data_Out pins. The Res_n pin is used to reset the SPI and the Sel_n pin is used by the DSP to start sending data to the SPI as a read or write request. The SPI includes 16 registers, each with a length of 11 bits, which makes it capable of writing to 16x11=176 control bits. Four bits are used to address these registers starting from 0000 to 1111. In order to write or read a register, the DSP sets the Sel_n to low and at the same time starts sending data.

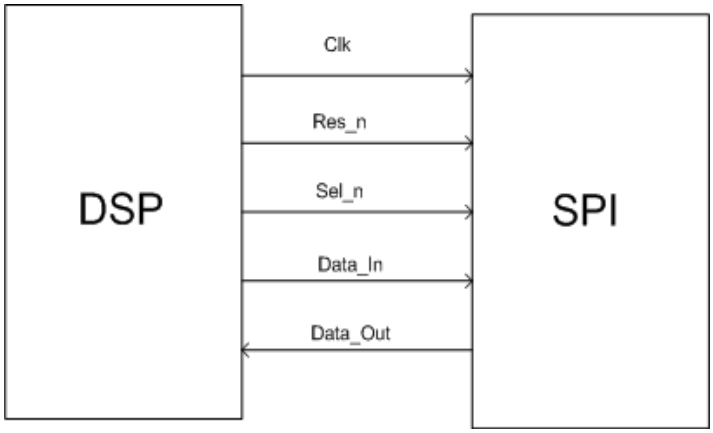


Fig. 4.21: SPI Connection to DSP

The first bit is used to determine whether it is a write or read request. If the first bit is 0, it indicates the DSP is willing to write to the register and if it is 1, it will read a register. The next 4 bits are the address starting from the MSB to the LSB and then there are 11 bits of data starting from the MSB to the LSB. As soon as the last bit is sent, the Sel_n goes to high in the next rising edge of the Clk as shown in the following picture.

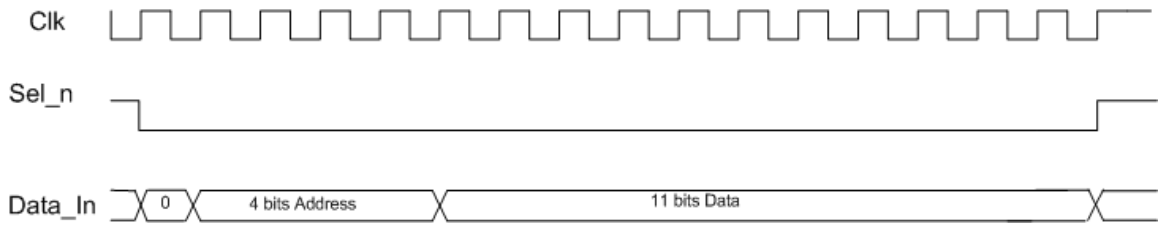


Fig. 4.22: Timing for Write on SPI

In the write mode, the SPI is designed to dump all data on the controllers at once if the DSP sends data for more than one register to the SPI. All data is dumped to the controllers as soon as the Sel_n pin set to 1 by the DSP as shown in Fig. 4.23. Having this feature helps the DSP to calculate the new values for the phase shifters faster since all of them change at the same time.

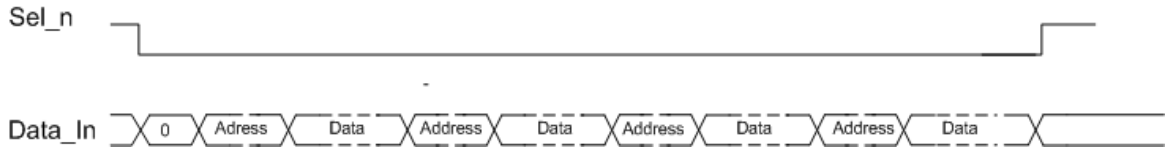


Fig. 4.23: Multiple Write on SPI

The read procedure is shown in Fig. 4.24. It shows that the first bit is 1 which means the DSP requests for reading a register, and then four address bits start from the MSB to the LSB. The Sel_n is set to low on the rising edge of the Clk and at the same rising edge of the Clk, the address is sent to the SPI. The Sel_n goes high on the next rising edge of the Clk after the last bit of address (LSB) has been sent. The requested register data is sent to the DSP on the Data_Out pin on the next falling edge of the Clk starting from the MSB to the LSB. The DSP starts reading the DATA on the next rising edge of the Clk right after Sel_n has gone high. The following picture illustrates the reading procedure.

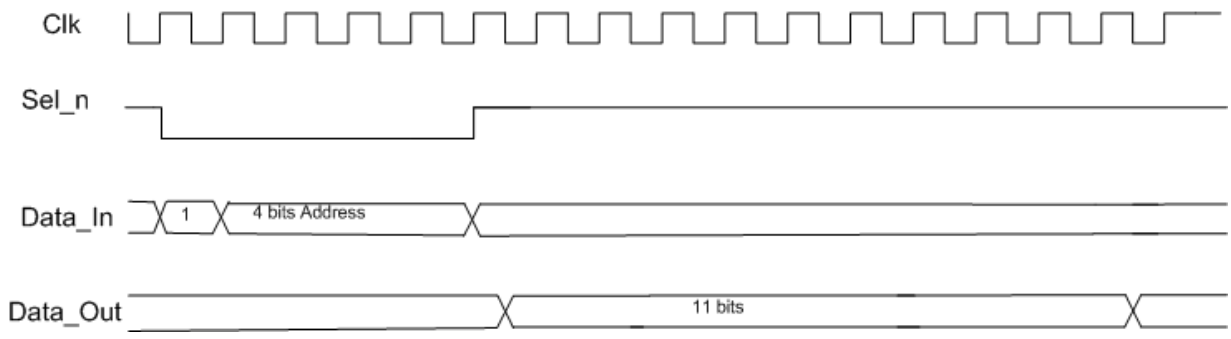


Fig. 4.24: Reading Register

4.7 Top Level Layout

Fig. 4.25 shows the layout of the 2-by-2 MIMO chip. The LO chains blocks are located on the left side of the chip and it outputs after buffering, drives the mixers and

combiners that are located at the center of the chip. The outputs of the mixers are connected to the base band buffers, which are connected to the output pads on the right side of the chip. The RF inputs coming from the antennas array are going to the two LNAs at the lower part of the chip.

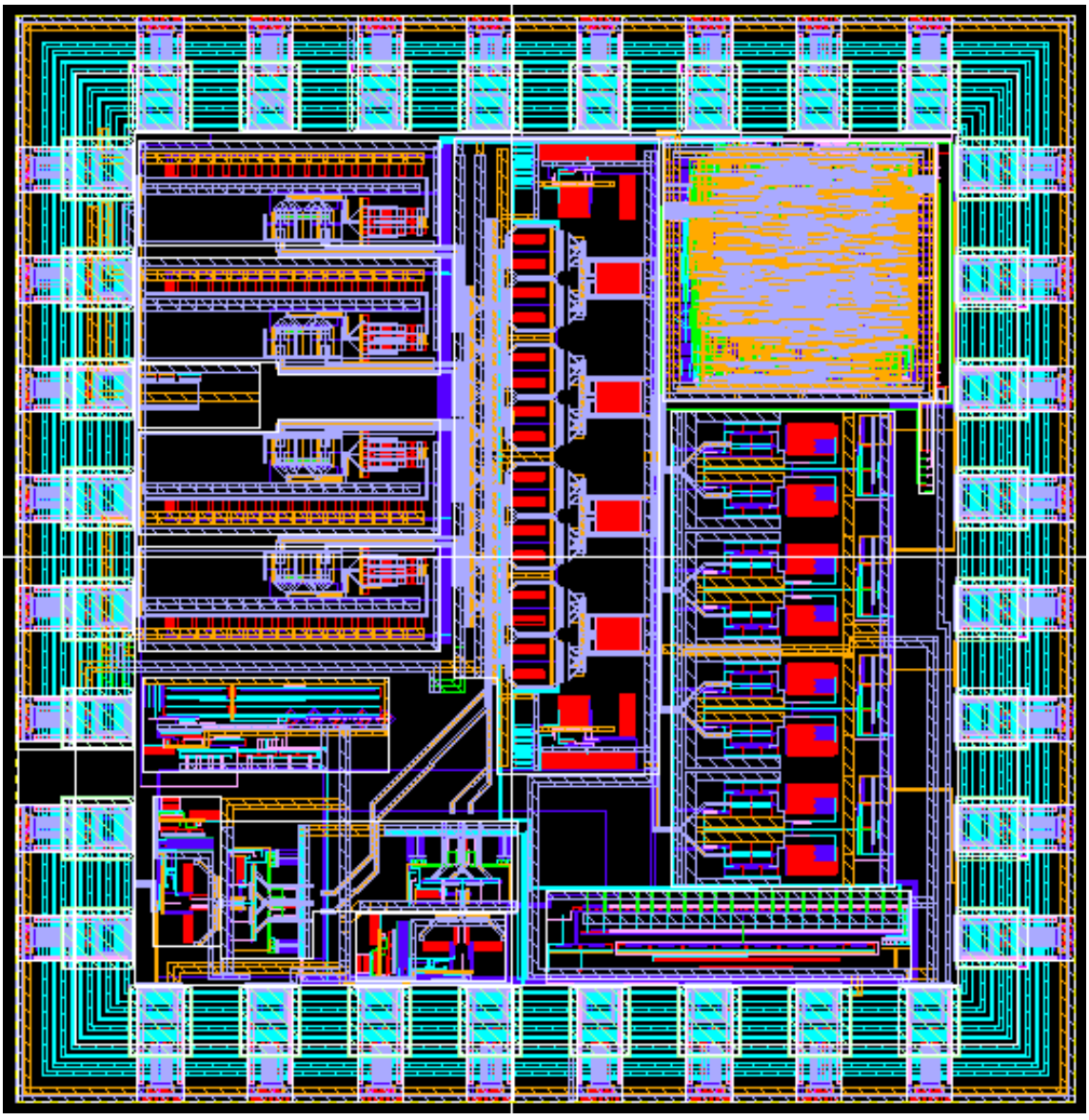


Fig. 4.25: Layout of 2-by-2 MIMO

The outputs of the LNAs are connected to the splitter/amplifiers, which are located above the LNAs. The SPI is at the top right corner of the chip and the control signals are going

to all of the blocks. The chip has a total area of $2\,\mathrm{mm}^2$ and has been designed in CMOS 90 nm using STMicroelectronics technology.

4.8 Top Level Simulation Results

Fig. 4.26 shows the output base band signals, OUT_1 and OUT_2 as it is shown in Fig. 4.1. When phase-shifting is applied just to one of the base bands, OUT_1, and another base band, OUT_2, is used as the reference. In this simulation the RF input signals to the LNAs are set at 2.52GHz and the 2LO signal is set at 5GHz which is applied to the phase shifters. Therefore, the base band signals' frequency is 20MHz.

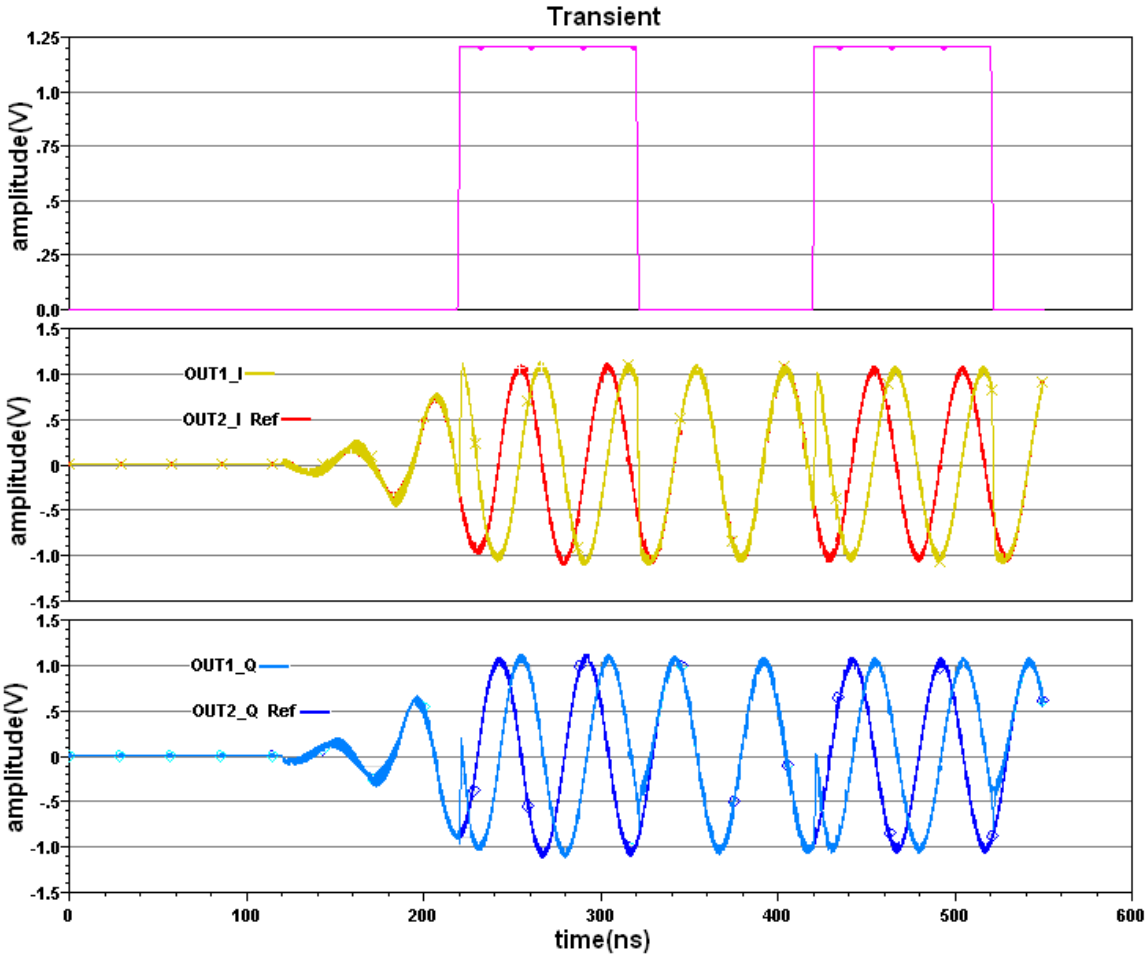


Fig. 4.26: Base Band Phase-Shifting

In this graph OUT1_I, OUT2_I and OUT1_Q, OUT2_Q are the single ended of the I&Q quadratures signals of the base bands OUT_1 and OUT_2 respectively. The top graph shows how 90˚ phase-shifting is applied to the OUT_1 base band signal. When the pulse goes high, the phase shifters change the phase of the OUT_1 base band signal by 90˚ and when it goes down, phase shift goes back to zero. The two bottom graphs show how the phase of OUT1_I and OUT1_Q are changing with respect to the OUT2_I and OUT2_Q that are not phase-shifted. It is observed, the phase of the base band signals at OUT1 have changed by 90˚ as soon as the LO phase is changed by the phase shifters.

The second simulation shows how the I&Q swap, changes the phase of the base band signals. Again the OUT2 has no phase-shift and is used as a reference.

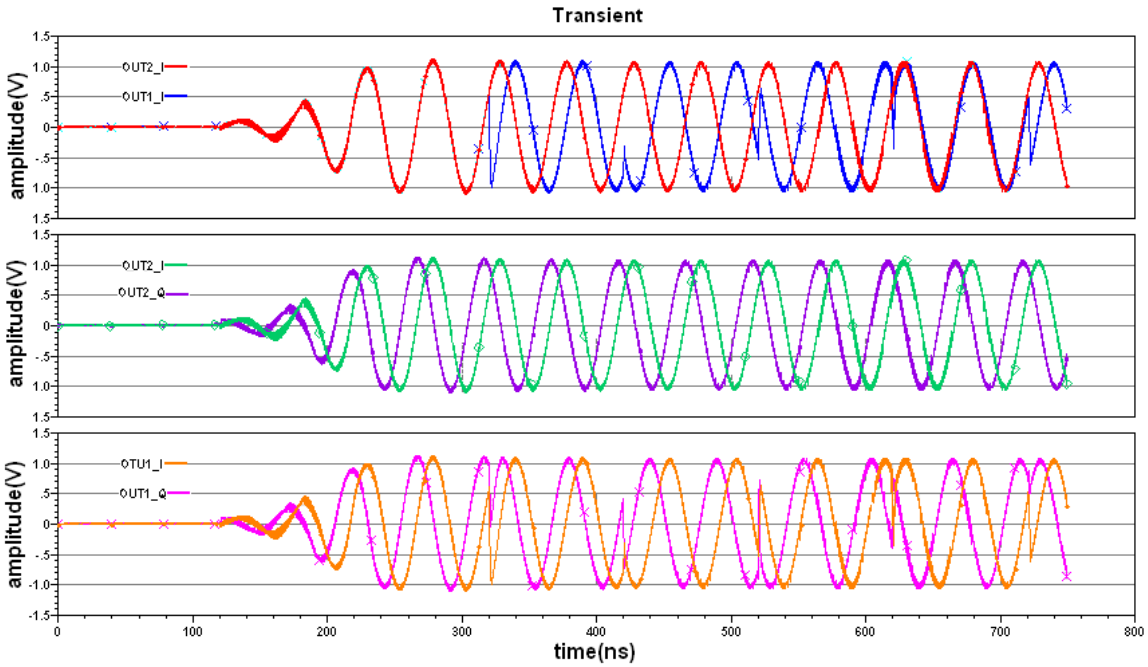


Fig. 4.27: Base Band Phase-Shifting Using I&Q Swap

In Fig. 4.27 the middle graph is OUT2 that experiences no phase-shift and is used as a reference. The top graph shows how the phase of OUT1_I (blue) changed relative to that of OUT2_I (red), which is considered as a reference. Both graphs have the same phase and covered each other from 0 to 32ns. At this point, I and Q of the OUT1 phase shifters are swapped to make a 90˚ phase-shift. Fig. 4.27 shows that the phase of the OUT1_I changed by 90˚ from 320ns to 420ns. At 420ns the I and Q changed to make a 180˚ phase-shift, and again at 520ns the phase of the OUT1_I relative to the OUT2_I becomes

270˚. Finally, at 620ns the I and Q swapped back to the original position and both graphs fully align again. The bottom graph shows the OUT1_I and OUT1_Q's quadrature signals maintain their phase difference through the I&Q swap.

Chapter 5 Measurement Results

Fig.5.1 is the picture of the die that was designed using STMicroelectronics 90nm CMOS technology. The chip is not packaged and it is wire bonded onto the test board as shown in the Fig. 5.2. The test board is 10.1cm by 7.4cm with two layers of metallization. There is a microcontroller on the test board that is able to communicate with the MIMO chip through the SPI.

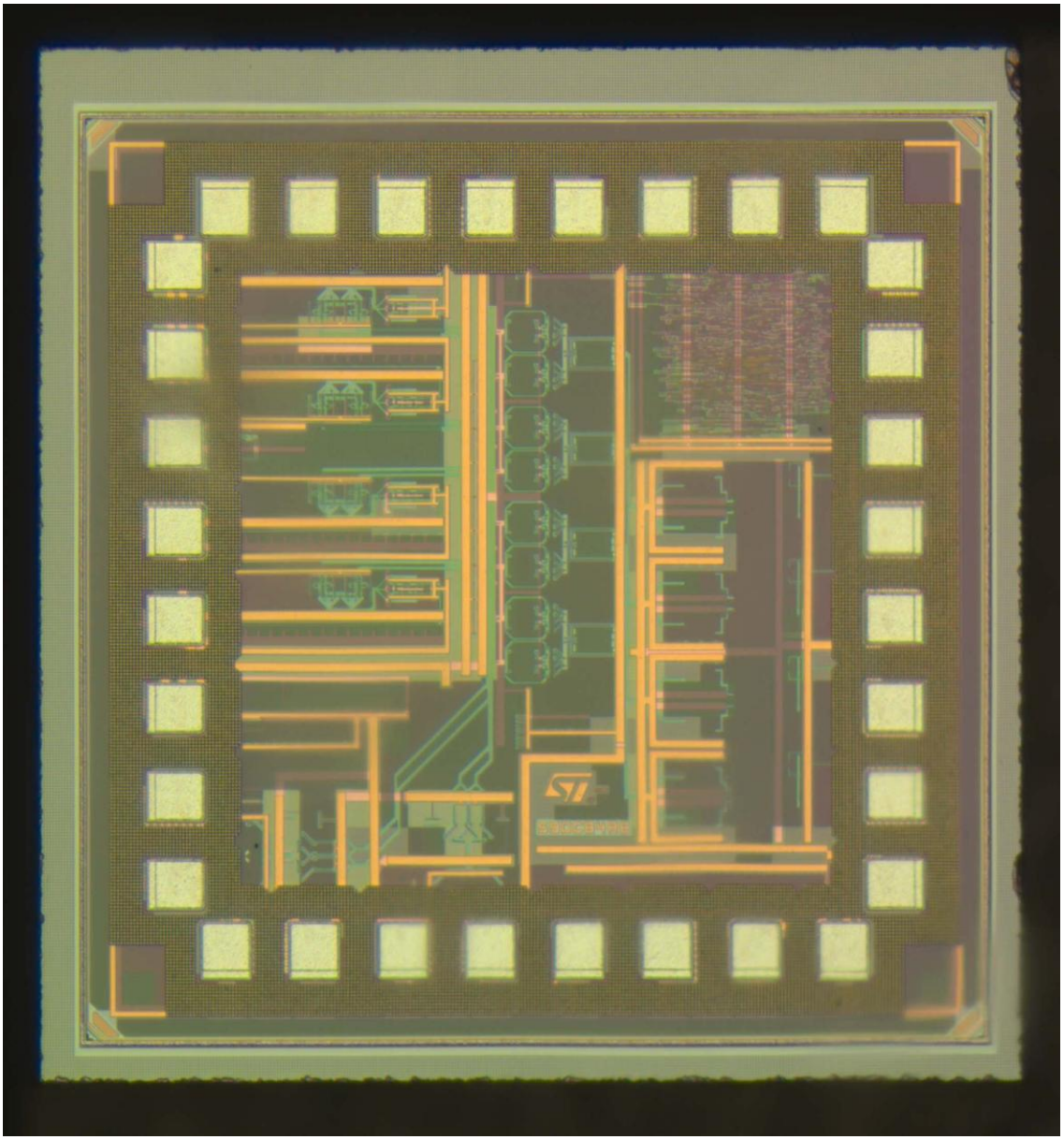


Fig. 5.1: Picture of the Die

There are also three regulators on the test board that provide the 3.6V, 2.5V and 1.2V voltages to supply power to the microcontroller, analog and digital blocks on the chip respectively. The chip is wire bonded to the test board and the two base band output signals are routed to the one side of the test board as shown in Fig. 5.2.

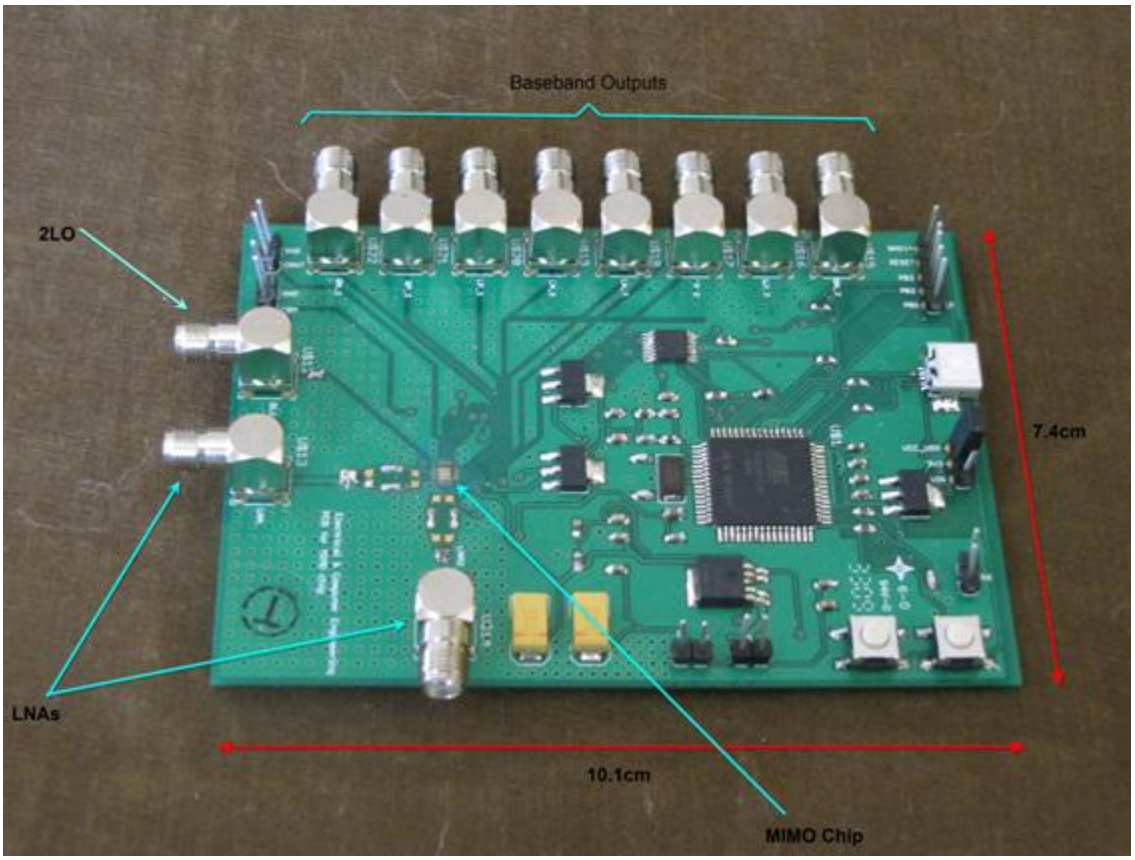


Fig. 5.2: Test Board

The inputs to the LNAs are routed perpendicularly to minimize the coupling between them. An application program has been developed in order to communicate with microcontroller as shown in Fig. 5.3. All the control bits on the chip can be set by the application program. This included enabling the LNAs, the LNAs gain setting, the splitter amplifiers gain setting, the mixers enables, the I&Q swap controllers and the delay of four phase shifters. There is also a reset button that is used to reset all the registers on the chip. This program is capable of reading back the last control bit that is sent to the chip, or read back all the SPI registers to make sure the registers are programmed properly. In addition, the program is able to write all registers at the same time by first sending the all

data to the SPI and then by clicking on the “Write All MIMO Registers” button, the SPI then sends data to the registers.

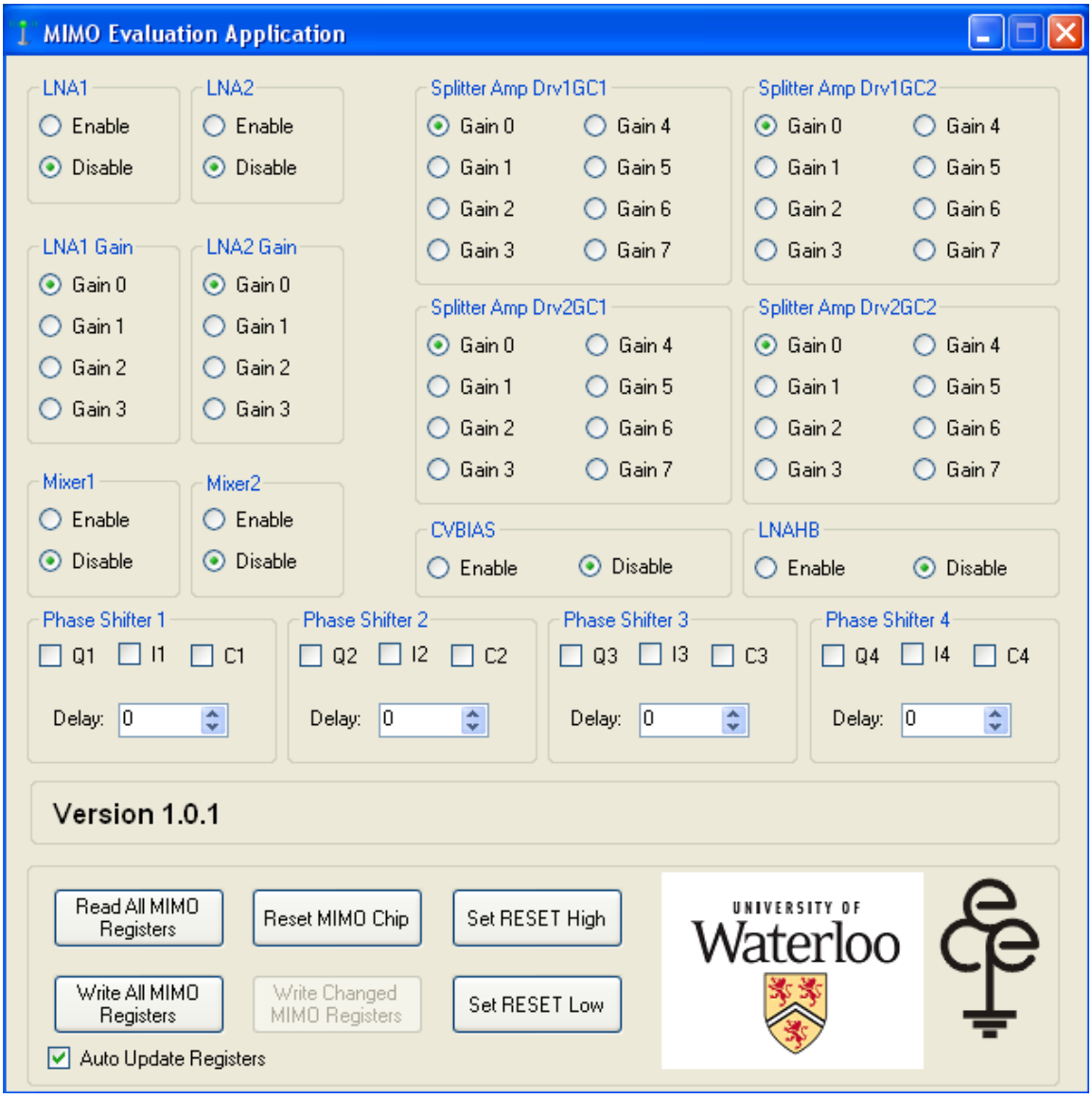


Fig. 5.3: MIMO Chip Application Program

Fig. 5.4 shows the test setup that was used to measure the chip. As shown, the output of one of the signal generators passes through a splitter to supply the LNAs, and another signal generator is used to provide the 2LO signal. The outputs of the chip connect to the oscillator or spectrum analyzer depending on the test requirements. The test board is also connected to the PC in order to set the control bits of the chip. There is also a power supply to provide a 6V voltage to the on board regulators.

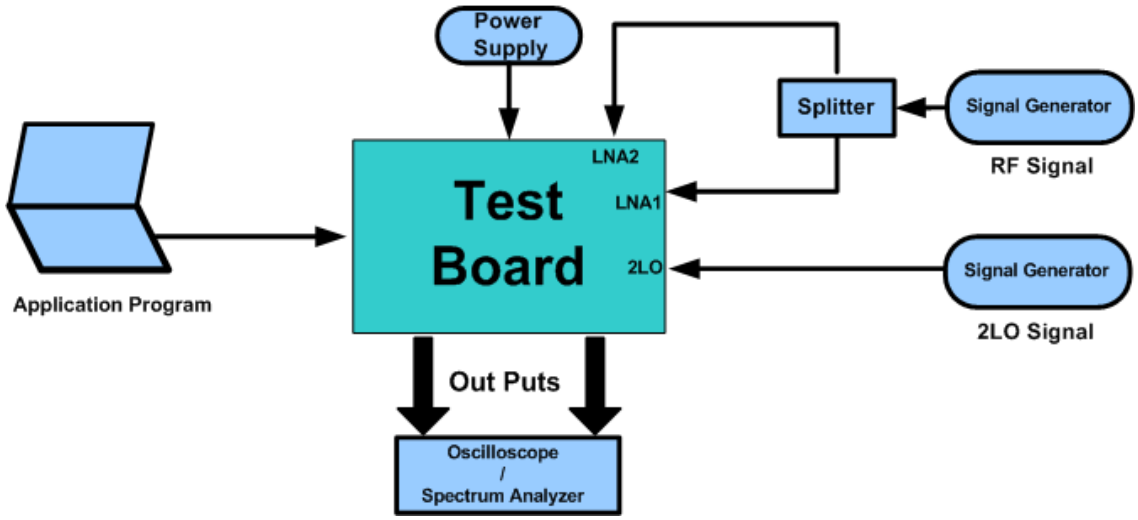


Fig. 5.4: Test Setup

5.1 Phase Shifter Measurement

The different characteristics of the phase shifter have been measured included the I&Q swap functionality, phase shifter resolution, phase shifter frequency coverage for both architectures (a) and (b) in Fig. 5.5 and the phase shifter's current consumption versus frequency.

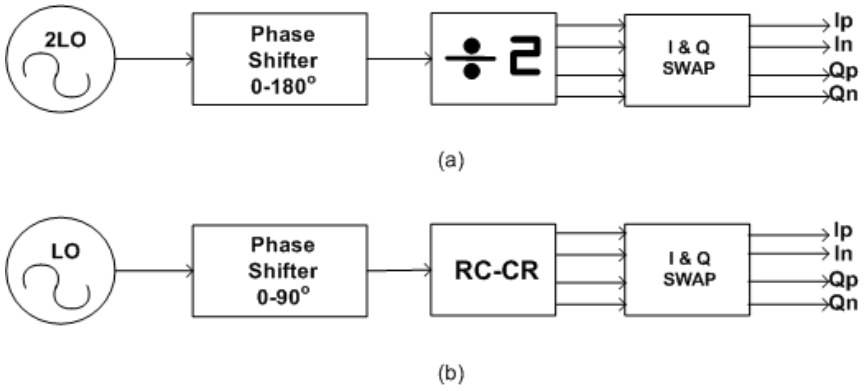


Fig. 5.5: LO Chain Architectures

The I&Q swap is a major feature in the LO chain to reduce the phase shifting requirement for both architectures shown in Fig.5.5. As it was explained in Chapter 3, the I&Q swap reduces the required phase shift to 180˚ for case (a) and 90˚ for case (b). Fig. 5.6 shows the measurement results of the I&Q blocks functionality.

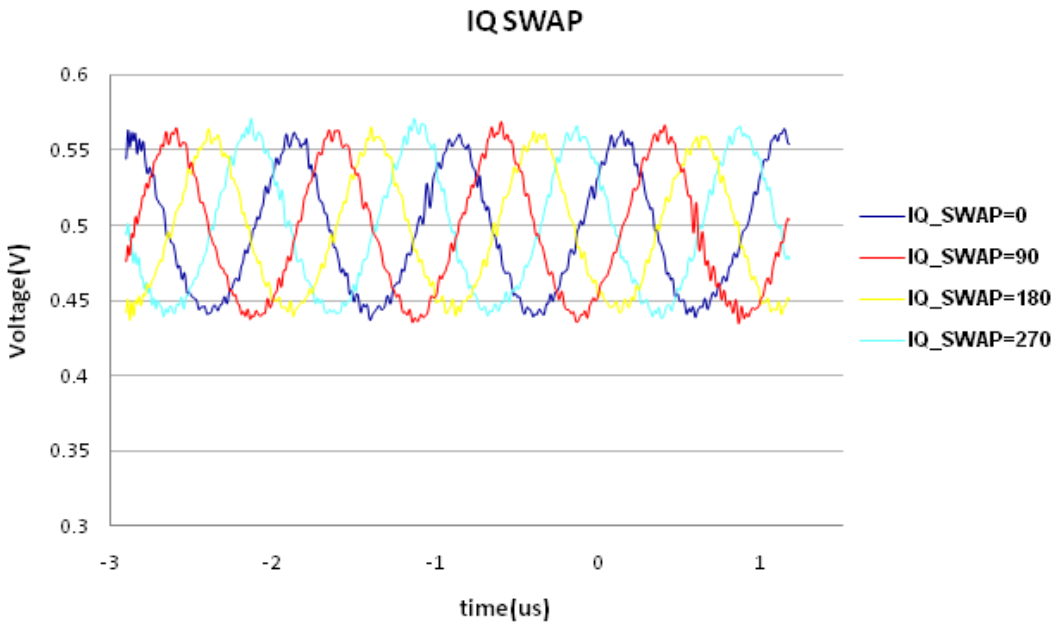


Fig. 5.6: I&Q Functionality

The dark blue waveform is the original output base band signal where the I&Q block does not change the phase. The red waveform is generated by rotating the I and Q signals by 90 degree clockwise. As it was expected, the phase was changed by 90˚. The yellow waveform is generated by swapping the I_p with I_n and Q_p with the Q_n making it 180˚ out of phase compare to the original signal (dark blue). The light blue waveform is created by swapping the I with the Q signal and then Q_p with the Q_n to make a 270˚ phase shift.

It was not possible to accurately measure the minimum delay of the base band signal when the phase shifter changed by 1LSB (resolution of the phase shifter) due to the high resolution of the delay cell. Therefore, the phase shifter was set to introduce a higher delay and then the total delay was divided by the phase shifter's control bits value. This measurement has been repeated for different frequencies and on several dies; the results were pretty consistent. The average resolution of the proposed phase shifter at the output base band signal was 1.32ps which is close to the simulated 1ps result in Chapter 4. The simulation was done on the schematic view of the LO chain; therefore the effects of the layout parasitic capacitors were not taken into account. The digital kit was used to design the chip, so the modeling might not be very accurate at high frequencies. These can explain the differences found between the measurement and simulation results.

The measurements also show that the phase shifter is able to work properly to about 6GHz which is less than simulation result of 7GHz. To calculate the maximum delay that the phase shifter can make in the output of the I&Q block, all 7 phase shifter control bits were set to one, then

$$Delay_{MAX} = 127 * 1.32\,ps = 167.64\,ps \qquad (5.1)$$

Now, to calculate the minimum frequency for which the phase shifter can achieve a 90˚ phase shift, the maximum calculated delay in 5.1 should be multiplied by four, so:

$$LO_{Period} = Delay_{MAX} * 4 \approx 671ps \qquad (5.2)$$

$$\text{Then, } RF_{MIN} = LO_{MIN} = \frac{1}{LO_{Period}} \approx 1.5GHz \qquad (5.3)$$

$$\text{And therefore, } 2LO_{MIN} = 3GHz \qquad (5.4)$$

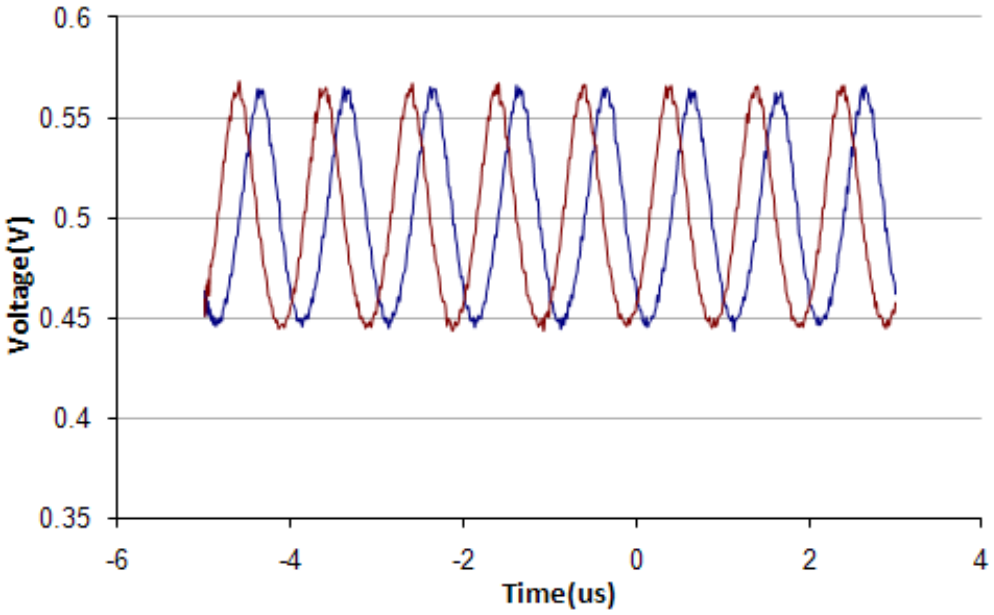


Fig. 5.7: Minimum Frequency Coverage for Architecture (a)

The chip was measured when the 3GHz signal was applied as a 2LO, and a 1.501GHz was applied as the input to the LNAs. The base band signal was measured for two cases. The first case, all the phase shifters control bits were set to zero and the second case, all control bits were set to one. The measurement results in Fig.5.7 show that the base band

signal phase changed by about 90˚ as expected. The red signal is the result of setting all phase shifter control bits to zero, and the blue one is with all bits set to one.

Fig. 5.8 shows the same measurement but with a different setting for the phase shifter control bits. In this measurement, the control bits are set to 0dec (decimal), 15dec, 31dec, 63dec and 127dec. As shown in Fig.5.8 the phase changed accordingly.

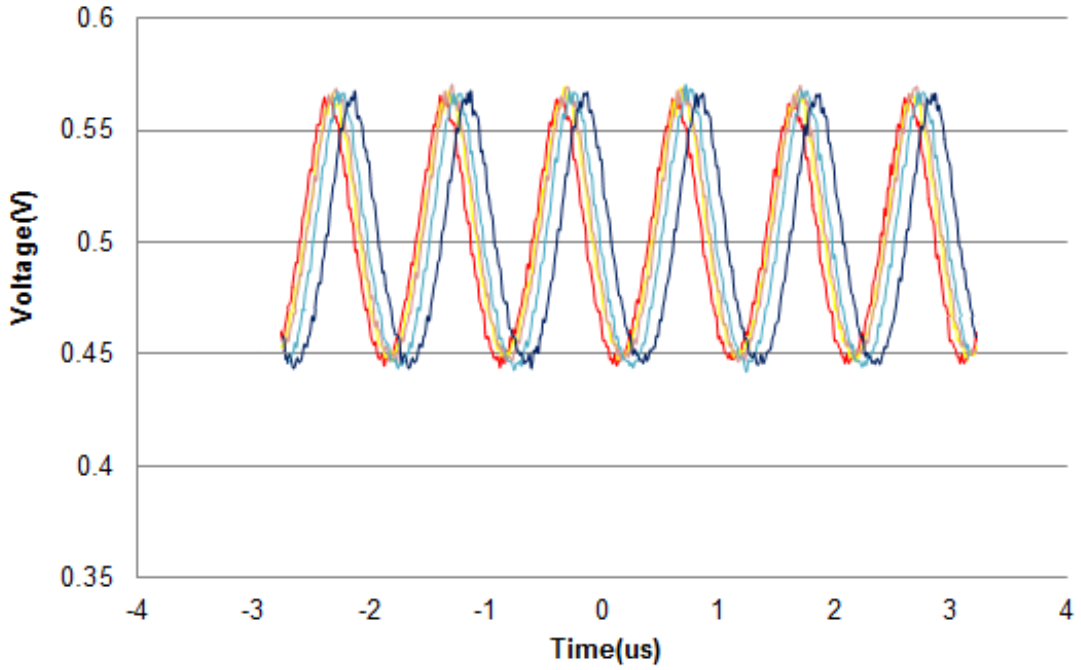


Fig. 5.8: Phase Shifting for Different Control Bits Setting

In this picture the red is the measurement result of setting all bits to zero, and the dark blue is when all bits are set to one (127dec), and the other control bits setting measurement results lay between these two results. As it is calculated in 5.3, the minimum frequency required for the phase shifter to be able to create a 90˚ phase shift for both architectures (a) and (b) when referred to the input of the LNA is 1.5GHz. Based on the measurement results, the phase shifter is able to work properly to about 6GHz. It means the maximum frequency of the RF signal when referred to the input of the LNA is about 3GHz and 6Hz for architecture (a) and (b) respectively.

The current consumption of the phase shifter has been measured for different frequencies as shown in Fig. 5.9. The measurement result is matched with the simulation result for the frequencies lower than 5GHz and then the current started to drop. The phase shifter was not able to work properly as it gets close to 6GHz and eventually stops operating.

Although in the simulation the phase shifter was able to work properly up to 7GHz. The discrepancy is due to the parasitic capacitors of the layout which were not included in the simulation. To make the phase shifter work in a higher frequency, the delay cell should be designed with a higher speed as is explained in section 3.2. Also, by adding more delay cells to the phase shifter, one could increase the lower end frequency coverage of the phase shifter.

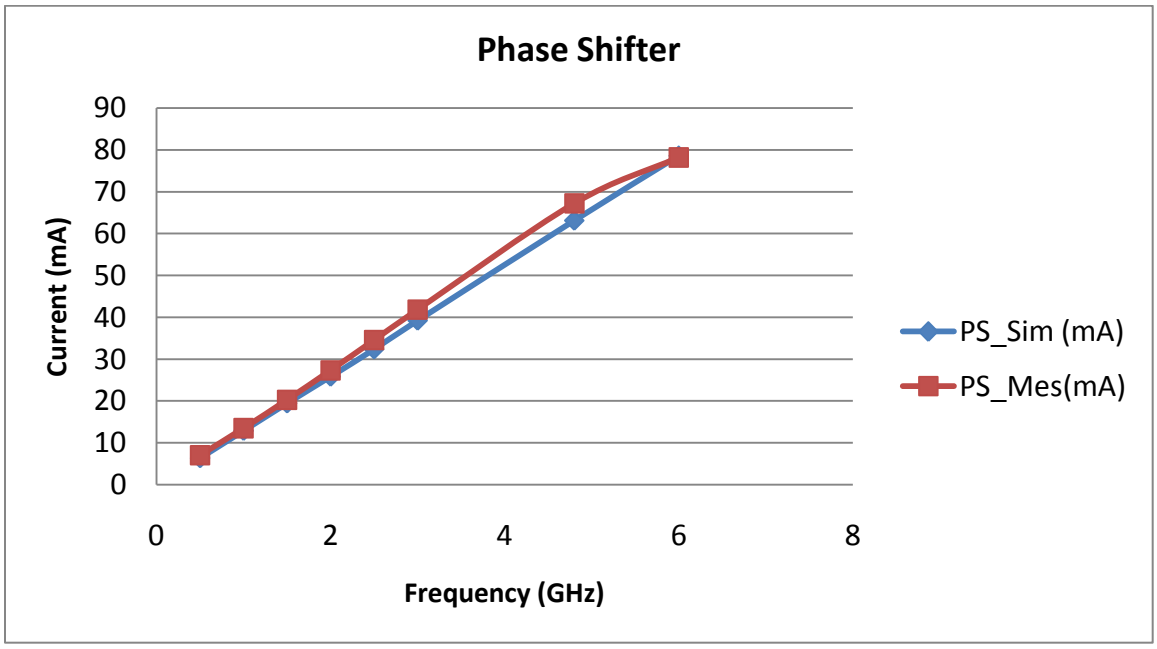


Fig. 5.9: Phase Shifter Current Consumption

5.2 Receiver Measurements

The gain of the receiver can be changed by adjusting the gain of the LNA and splitter amplifier. The gain of the LNA is changed by two control bits. The following table shows the measurement and simulation results of the LNA gain variation versus the control bits. As it shows, the total gain variation of the LNA is 12.5dB and 10.5 dB for the simulation and measurement respectively.

The receiver gain can be also be adjusted by using the splitter amplifier control bits. There are three bits that are used to change the gain of the splitter amplifier.

Table 5.1: LNA Gain Variation versus Control Bits

LNA	Amplitude	Δ Gain	Δ Gain	GV	GV
	Measurement	Measurement	Simulation	Measurement	Simulation
Control Bits	mV	dB	dB	dB	dB
00	84	-	-	10.5	12.5
01	40	6.4	6.6		
10	31	2.2	3.5		
11	25	1.9	2.4		

The following table is the measurement and simulation results of the gain variation of the splitter amplifier versus the three control bits. As it is shown, the gain variation is about 8.2dB and 12.6dB for the measurement and the simulation results. The source of the discrepancy between simulation and measurement is mostly due to the parasitic capacitance of the long traces that connect the output of the splitter amplifiers to the mixers.

Table 5.2: Splitter Amplifire Gain Variation versus Control Bits

Splitter Amplifier	Amplitude	Δ Gain	Δ Gain	GV	GV
	Measurement	Measurement	Simulation	Measurement	Simulation
Control Bits	mV	dB	dB	dB	dB
000	84	-	-	8.2	12.6
001	70	1.6	3		
010	59	1.5	2.6		
011	52	1.1	1.8		
100	46	1.1	1.6		
101	41	1.0	1.4		
110	37	0.9	1.2		
111	33	1.0	1		

The amplitude of the output base band signal can be controlled by changing the phase of the LO signals through the phase shifters. The two input RF signals are amplified by the LNAs and splitter amplifiers before mixing and combining in the mixer. By adjusting the phase of the LO signal, one could minimize the phase difference of the

two RF signals and therefore maximize the amplitude of the output base band signal. In fact, the amplitude of the output base band signal is a function of the phase difference between the input RF signals to the mixer which are controllable by the LO signals. Fig. 5.10 shows how the power of the output base band signal varies by the phase of the LO signal. In this measurement, 3GHz was applied as a 2LO signal and 1.501GHz was applied as the input RF signal. As it shows, when the phase difference is 180^0, the output signal is attenuated by about 25dB. In this measurement, the phase of one of the input RF signals relative to the other one is changed from 0˚-360˚. The maximum attenuation of the output signal at 180 degree phase difference is limited by couple of factors. The amplitude mismatch of the two input RF signals at the input of the mixers reduce the attenuation. The other factor is the quadrature LO signals phase error due to the transistors and layout mismatches.

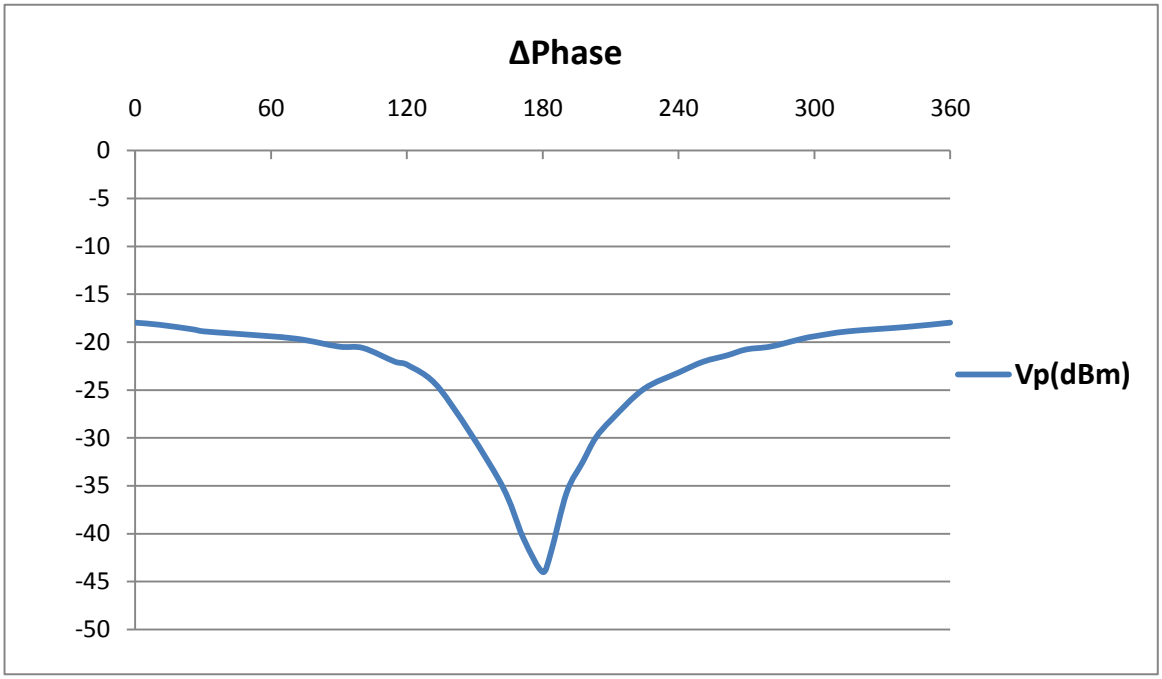


Fig. 5.10: Output Power Variation versus Phase Difference

5.3 Proposed Method to Reduce Phase Shifter Variation versus Temperature and Process Variations

As shown in Chapter 3, the delay of the delay cell is a function of the temperature. Increasing the temperature increases the delay since the mobility of the electrons or holes depend on the absolute temperature. Fig.3.10 shows the variation of the delay versus the temperature. Equation 3.7 shows that the delay is changed due to the process variation as well. The process variation might change the width, length or the threshold voltage, and therefore changes the delay of the phase shifter. The other parameter that could potentially change the delay of the phase shifter is the power supply. As equation 3.7 shows, the delay of an inverter is inversely proportional to the power supply. Therefore, by adjusting the phase shifter power supply, one could significantly reduce the variation of the phase shifter versus the temperature and process variation. Fig. 5.11 is a block diagram that illustrates the proposed method for improving performance stability.

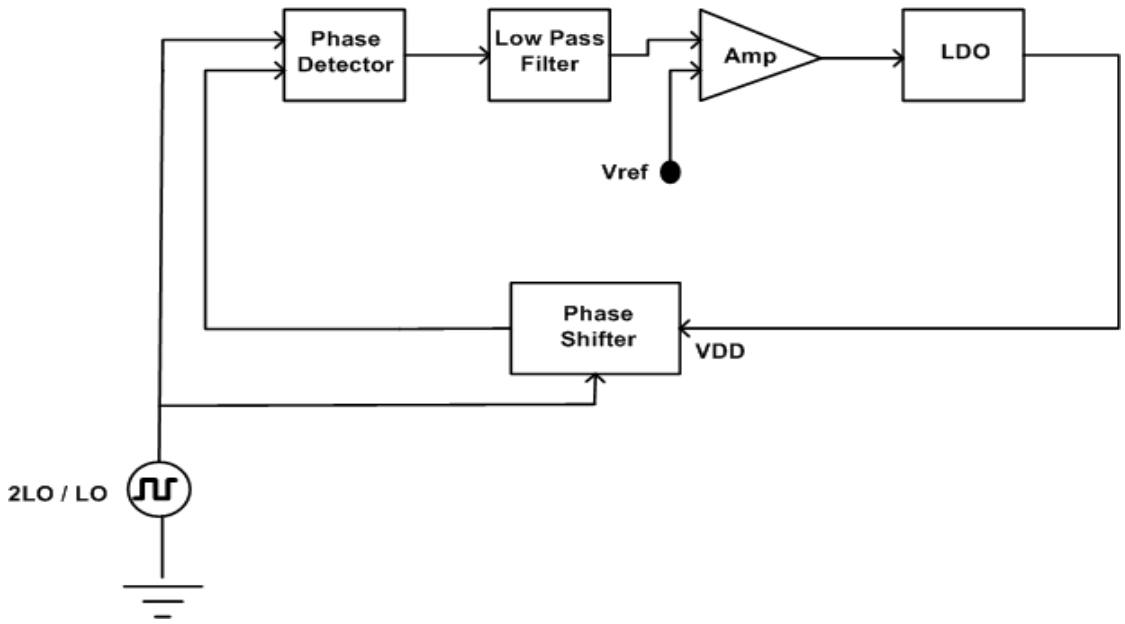


Fig. 5.11: Proposed Method to Reduce Delay Variation

In order to control the power supply of the phase shifters, a dummy phase shifter is used to monitor the delay variation. The 2LO signal (or LO in case of using architecture (b) in Fig. 5.5) is applied to both the phase shifter and to the phase detector. In this architecture a JK flip-flop was used as the phase detector. The output of the phase detector is a

function of the phase difference between the 2LO signal and the phase shifted 2LO at the output of the phase shifter. The output of the phase detector is averaged by the low pass filter which is linearly proportional to the phase difference between the 2LO and the phase shifted 2LO signals. The operation and the transfer characteristics of the JK flip-flop phase detector are shown in Fig.5.12 [40]. The output of the low pass filter is zero when both input signals to the phase detector are in phase, and it increases if the phase difference increases. In fact, the output voltage of the low pass filter represents the delay between the 2LO and the phase shifted 2LO signal. As shown in Fig.5.12, the transfer function of the phase detector is given by

$$k_{pd} = \frac{V_o}{2\pi} \qquad (5.5)$$

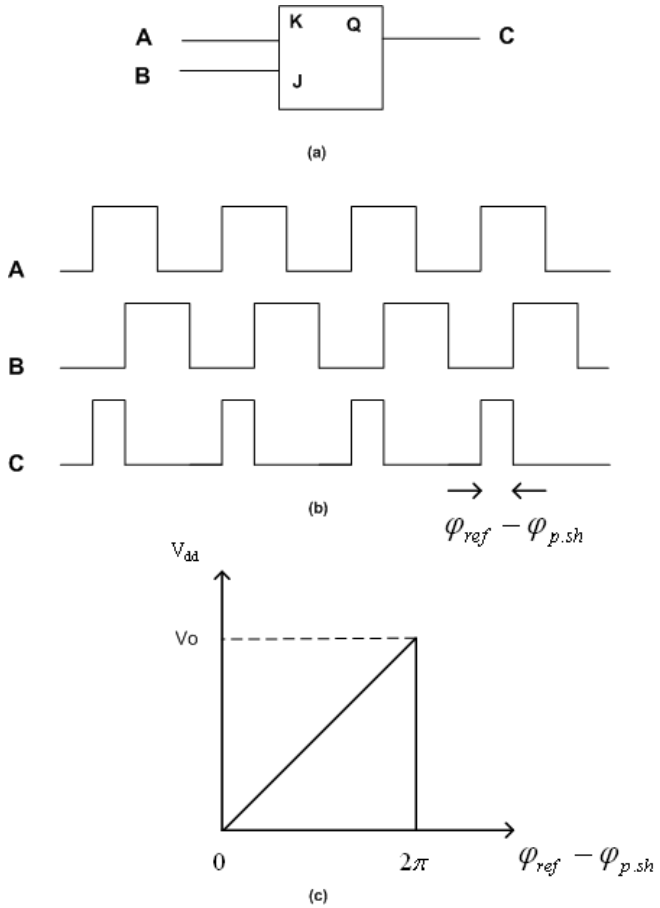


Fig. 5.12: (a) JK flip-flop (b) operation of JK flip-flop (c) transfer characteristic

The low pass filter is a RC filter and its transfer function is given by,

$$G_{lpf}(s) = \frac{1}{1 + \frac{s}{p_{lpf}}} \qquad (5.6)$$

$$\text{where, } p_{lpf} = \frac{1}{RC} \qquad (5.7)$$

The amplifier is the next block in Fig.5.11 that amplifies the difference between the reference voltage (Vref) and the output voltage of the low pass filter. The value of the Vref is basically defined by the phase difference between the 2LO and the phase shifted 2LO. The amplifier transfer function is given by,

$$G_{amp}(s) = \frac{G_{amp}}{1 + \frac{s}{p_{amp}}} \qquad (5.8)$$

where G_{amp} and p_{amp} are the gain and the dominant pole of the amplifier respectively.

The output of the amplifier is used as the reference voltage for the LDO (Low Drop Out) regulator in Fig.5.11. The LDO is based on a unity gain Opamp and its transfer function is given by,

$$G_{ldo}(s) = \frac{1}{1 + \frac{s}{p_{ldo}}} \qquad (5.9)$$

As it is shown in Chapter 3, the delay of the delay cell is given by,

$$t_{psh} = \frac{C_L}{kV_{LDO}} \qquad (5.10)$$

where C_L is the total load capacitance and k is given by,

$$k = \frac{\mu C_{ox}}{2} \frac{W}{L} \qquad (5.11)$$

By assuming that the loop is in a steady state mode, the V_{LDO} is,

$$V_{LDO} = V_o + v$$

where V_o and v are the nominal DC supply voltage and variable voltage respectively. Therefore 5.10 can re-written as,

$$t_{psh} = \frac{C_L}{k(V_o + v)} \qquad (5.12)$$

By using the Maclaurin Series we have,

$$t_{psh} = \frac{C_L}{kV_o} - \frac{C_L}{kV_o^2}v + \frac{C_L}{kV_o^3}v^2 ..... \qquad (5.13)$$

Therefore, by ignoring the high order terms in 5.13, the variation of the delay due to the LDO voltage is given by,

$$t_{psh} \approx \frac{-C_L}{kV_o^2}v \qquad (5.14)$$

So, the phase variation of the 2LO signal at the output of the phase shifter is calculated as,

$$\varphi_{psh} = \frac{-2\pi C_L}{kV_o^2 T}v \qquad (5.15)$$

where T is the period of the 2LO signal. By using 5.15, the transfer function of the phase shifter becomes,

$$k_{psh} = \frac{-2\pi C_L}{kV_o^2 T} \qquad (5.16)$$

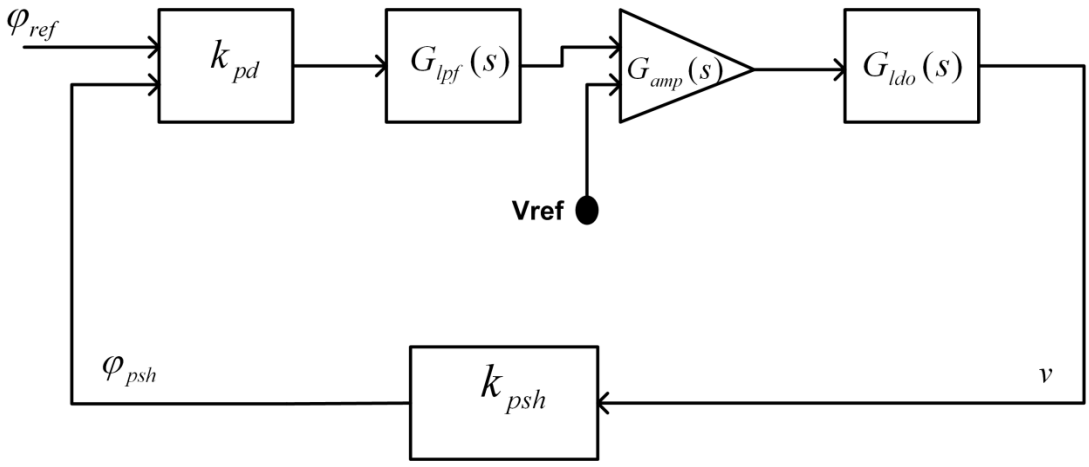


Fig. 5.13: Linear Model

The linear model of the proposed circuit is shown in Fig.5.13 and can be viewed as a standard feedback system. Then, the open loop transfer function is given by,

$$H_{ol}(s) = \frac{k_{psh}k_{pd}G_{amp}}{(1+\frac{s}{p_{lpf}})(1+\frac{s}{p_{amp}})(1+\frac{s}{p_{ldo}})} \qquad (5.17)$$

The bode plot of the open loop transfer function is shown in Fig.5.14.

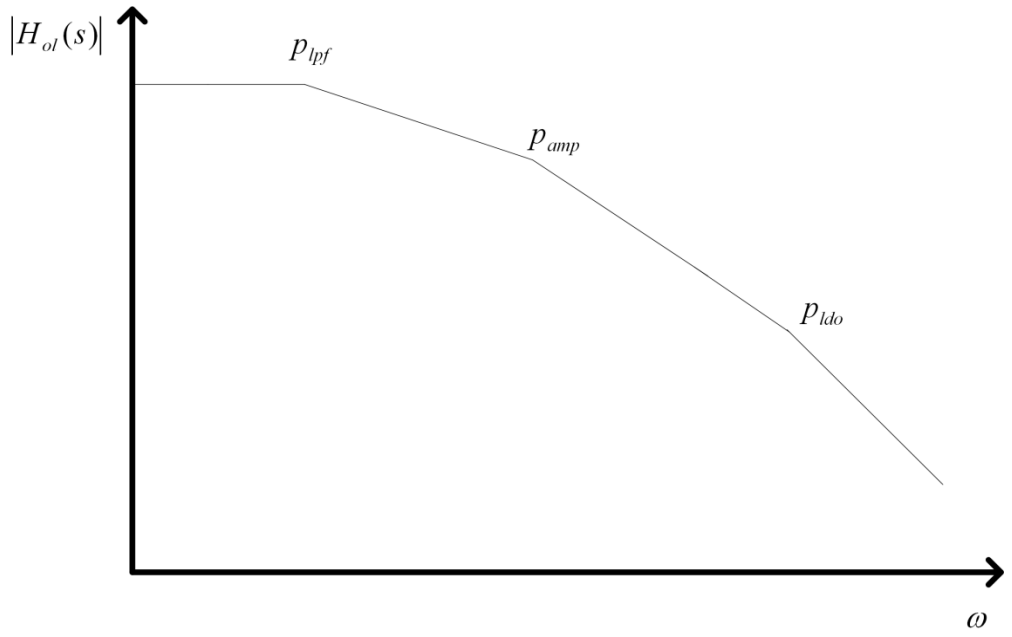


Fig. 5.14: the Bode Plot of Open Loop Transfer Function

As it is shown in 5.17, there are at least three poles and since each pole introduced a 90˚ phase shift, the loop is unstable. One could stabilize the loop by moving the low pass filter pole (p_{lpf}) towards a lower frequency to make a dominant pole. In order to calculate the location of the low pass filter pole, the amplifier pole (p_{amp}) should cross the frequency axis [39]. Given the $G_{(dB)}$ as the total DC loop gain, one can calculate the pole of the low pass filter as shown in Fig.5.15. In order to make sure that the pole of the amplifier crosses the frequency axis, the pole of the low pass filter should be located at,

$$p_{lpf} = \frac{p_{amp}}{10^{\frac{G}{20}}} \qquad (5.18)$$

This method of stabilizing the loop reduces the bandwidth and therefore the tracking speed of the loop. Since the temperature changes at a very slow rate, this method is a practical and suitable way to control the temperature variation effects on the delay cell. Having the second pole (p_{amp}) crossed the frequency axis, provides a 45˚ phase margin. The phase margin can be improved by moving the pole of the low pass filter further towards a lower frequency.

If a high DC gain is needed for a small steady-state error with a high speed tracking capability, a lag-lead filter which is shown in Fig.5.16 can be used.

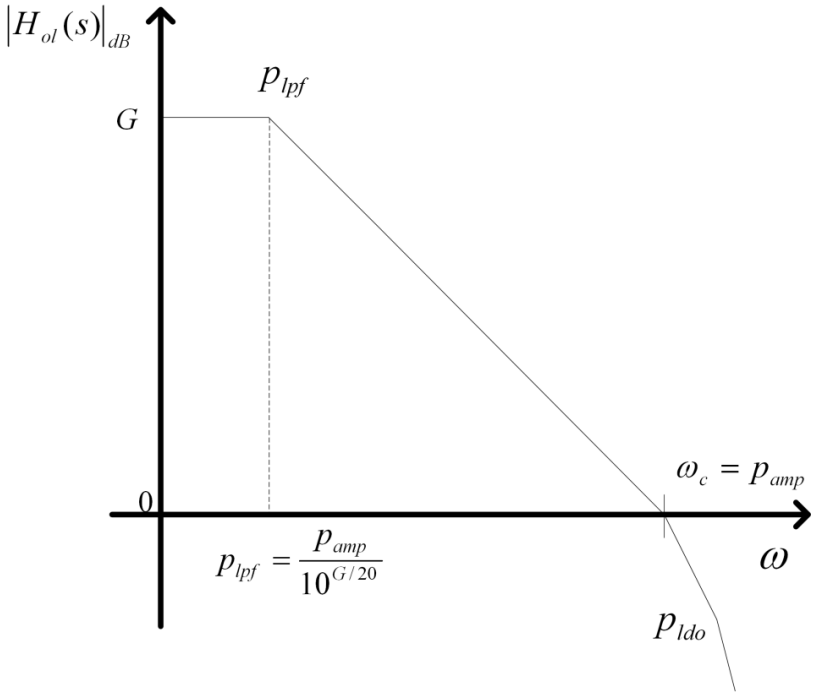


Fig. 5.15: Low Pass Filter Pole Location

The lag-lead filter transfer function is given by [40],

$$G_{lpf}(s) = \frac{1+\frac{s}{z_{lpf}}}{1+\frac{s}{p_{lpf}}} \qquad (5.19)$$

with $z_{lpf} = \frac{1}{R_2 C}$ and $p_{lpf} = \frac{1}{(R_1 + R_2)C}$

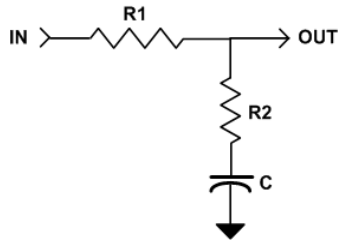


Fig. 5.16: Lag-Lead Filter

The zero in the transfer function of the low pass filter gives more design flexibility to increase the bandwidth or the DC gain of the loop.

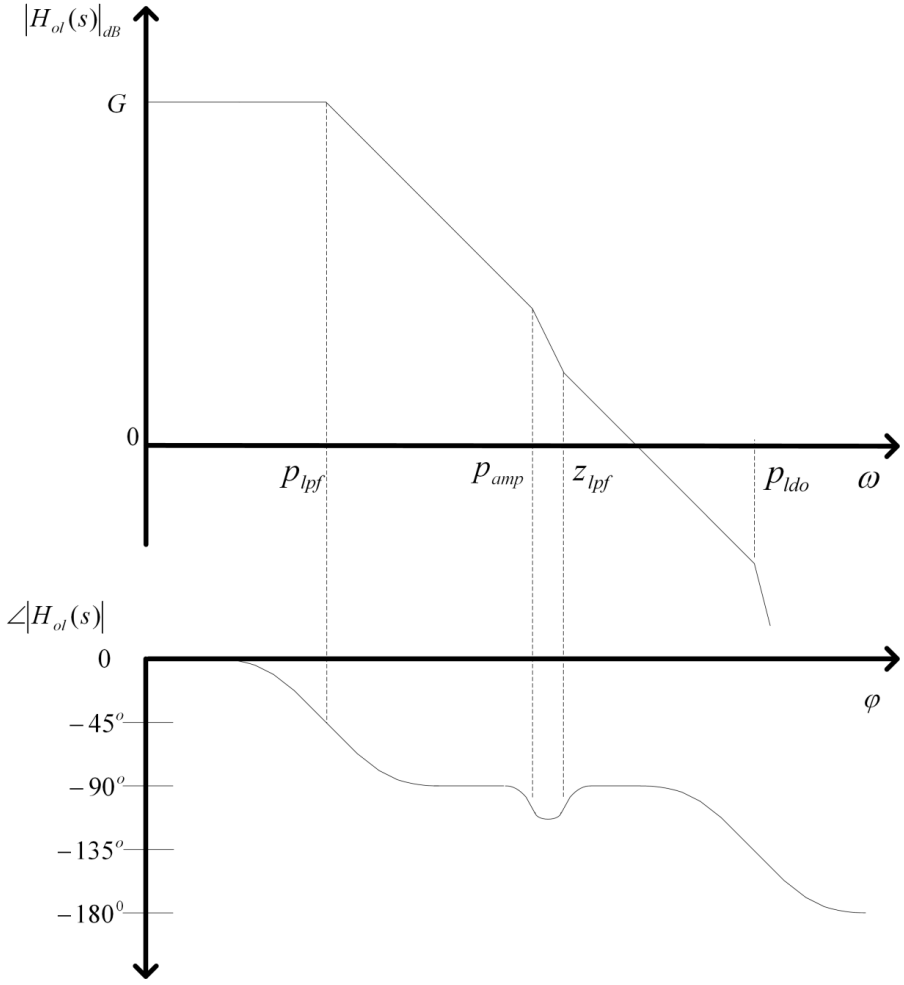


Fig. 5.17: Bode Plot

Fig.5.17 shows the Bode and the phase plot of the open loop transfer function. As shown, the zero helps to mitigate the impact of the amplifier pole on the phase margin. Therefore, a higher bandwidth or DC gain can be achieved.

5.3.1 Simulation Results

The proposed method to reduce the phase shifter variability has been evaluated by simulation using STMicroelectronics 90nm CMOS technology. Fig.5.18. shows the test bench that was used to simulate the phase shifter phase variation over temperature with a fixed power supply. For this simulation, the 2LO signal frequency was set to 4GHz and a 1.2V fixed power supply was used to supply the phase shifter. The phase difference between the 2LO signal and the phase shifted 2LO at the phase shifter's output at 25˚ Celsius was about 185˚.

Then, the temperature was swept from -10˚ to 100˚ and as shown in Fig.5.19, the phase varied from 170˚ to 215˚.

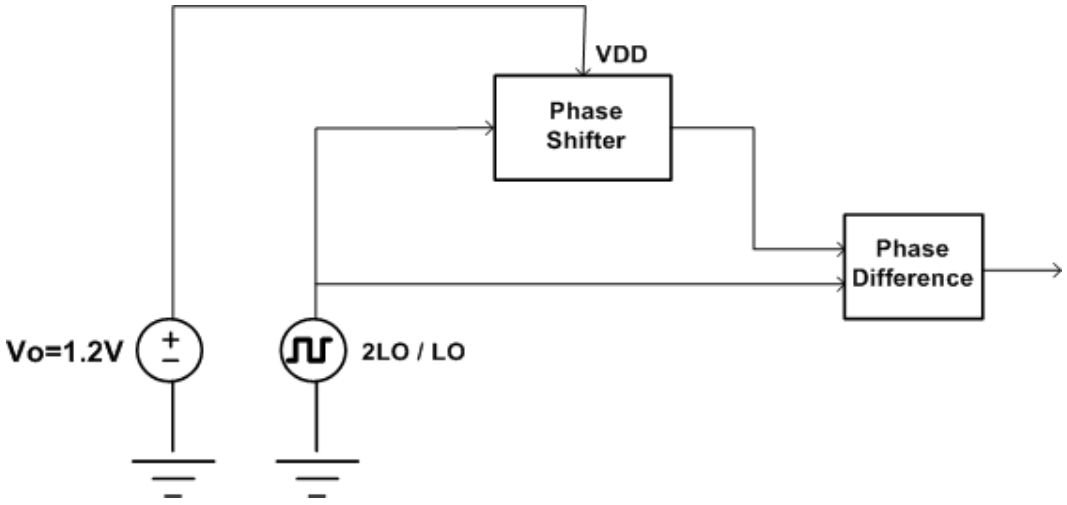


Fig. 5.18: Phase Shifter with Fixed Power Supply

This much variation in the phase might not be an issue for some applications that are not sensitive to the resolution of the phase shifter. However, the phase variation might not be compensated through an adaptive system because of the limitation of the phase shifter's total phase-shifting capability.

A simulation test bench was implemented based on the linear model in Fig.5.13. In this test bench, the 2LO frequency was set to 4GHz. The JK flip-flop was used as the phase detector and all bits of the phase shifter were set to one.

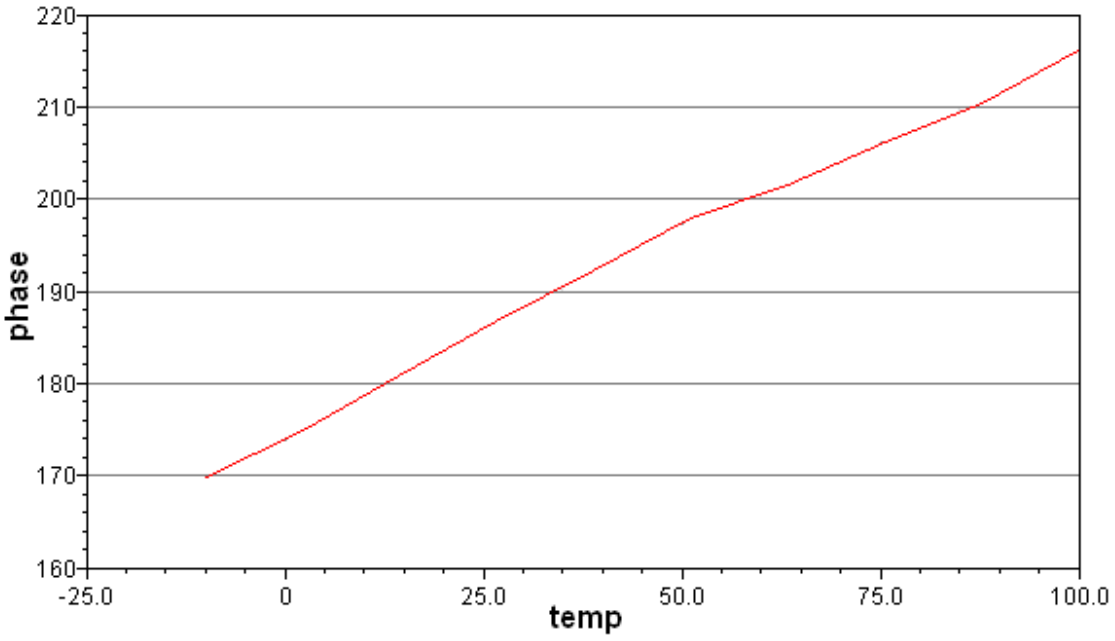


Fig. 5.19: Phase Variation over Temperature

At room temperature with a 1.2V power supply, the phase shifter made about a 379ps delay. Therefore the transfer function of the phase shifter (k_{psh}) is calculated as follows,

$$t_{psh} = \frac{C_L}{kV_o}$$

$$\Rightarrow \frac{C_L}{k} = V_o t_{psh}$$

$$\Rightarrow \frac{C_L}{k} = 379\,ps * 1.2V = 455\,psV$$

Then,

$$k_{psh} = \frac{-2\pi C_L}{kV_o^2 T}$$

$$T = \frac{1}{4GHz} = 250\,ps$$

So,

$$k_{psh} = \frac{-2\pi * 455\,psV}{1.2^2 * 250\,ps} \approx -8 \qquad (5.20)$$

Since the JK flip-flop has been used for this simulation, the transfer characteristic of the phase detector (which is supplied with a fixed 1.2V power supply) is given by,

$$k_{pd} = \frac{V_o}{2\pi} = \frac{1.2}{2\pi} \qquad (5.21)$$

The loop gain of the open loop transfer function given in 5.17 is set to $60dB$; therefore the gain of the amplifier is calculated as follows,

$$G = 1000 = k_{psh} k_{pd} G_{amp}$$

$$\Rightarrow G_{amp} = \frac{G}{k_{psh} k_{pd}} \approx 655$$

Then,

$$G_{amp}(dB) = 56dB \qquad (5.22)$$

The amplifier provides a minimum 56dB of gain with a pole located at 50MHz. In order to stabilize the loop, the dominant pole method was used. The low pass filter pole is calculated by using 5.18 as follows,

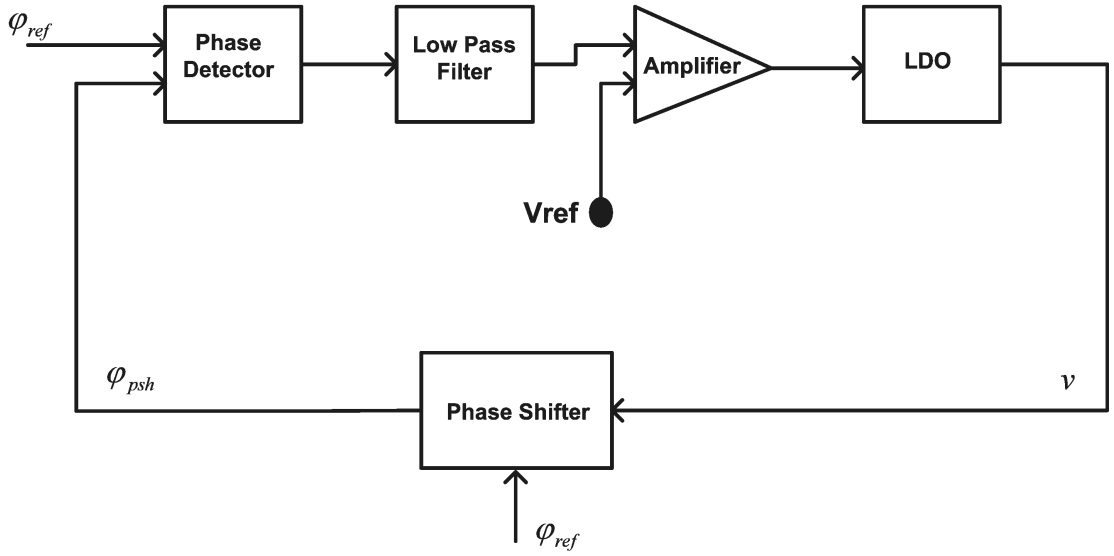
$$p_{lpf} = \frac{p_{amp}}{10^{\frac{G}{20}}}$$

$$\Rightarrow p_{lpf} = \frac{2\pi * 50MHz}{10^{\frac{60dB}{20}}} = 2\pi * 50KHz \qquad (5.23)$$

As it is calculated in 5.23, by locating the pole of the low pass filter at 50KHz, the pole of the amplifier crossed the frequency axis as shown in Fig.5.15 which provides a 45˚ phase margin. In order to improve the phase margin, the pole of the low pass filter is moved to 20KHz and provides about a 70˚ phase margin. Fig.5.20 shows the test bench which is based on the calculated parameters for each block. The transfer function of each block is given as well.

The test bench in Fig. 5.20 was used to check the stability of the loop in the time domain. The reference voltage was set at 550mV which is equivalent to a 165˚ phase difference between the 2LO signal and the phase shifted 2LO at the output of the phase shifter. As it shows in Fig.5.21, it took 10us for the output of the low pass filter to reach 550mV and locked onto the reference voltage (Vref). To see how the loop responses to the step signal, the Vref was abruptly changed from 550mV to 650mV (which is an equivalent to

a 195˚ phase difference) and the low pass filter output voltage locked onto the new Vref value in about 5us with no sign of instability in the transient response as expected.



$$k_{pd} = \frac{1.2}{2\pi}$$

$$G_{lpf}(s) = \frac{1}{1 + \frac{s}{2\pi.20kHz}}$$

$$G_{amp}(s) = \frac{G_{amp}}{1 + \frac{s}{2\pi.50MHz}}$$

$$G_{ldo}(s) = \frac{1}{1 + \frac{s}{p_{ldo}}}$$

$$k_{psh} = -8$$

Fig. 5.20: Test Bench

Fig. 5.22 shows the phase shift variation when the temperature is swept from -10˚ to 100˚ Celsius. The top graph in Fig.5.22 is the phase difference and the bottom one is the output voltage of the LDO that supplies the phase shifter. As it is shown, the LDO output voltage is changed accordingly to maintain the delay of the phase shifter relatively

constant over the temperature variation. The total phase variation is less than 1˚ compare to the open loop simulation result which is about 45˚. In this simulation the reference voltage Vref was set to 620mV which is equivalent to a 186˚ phase difference.

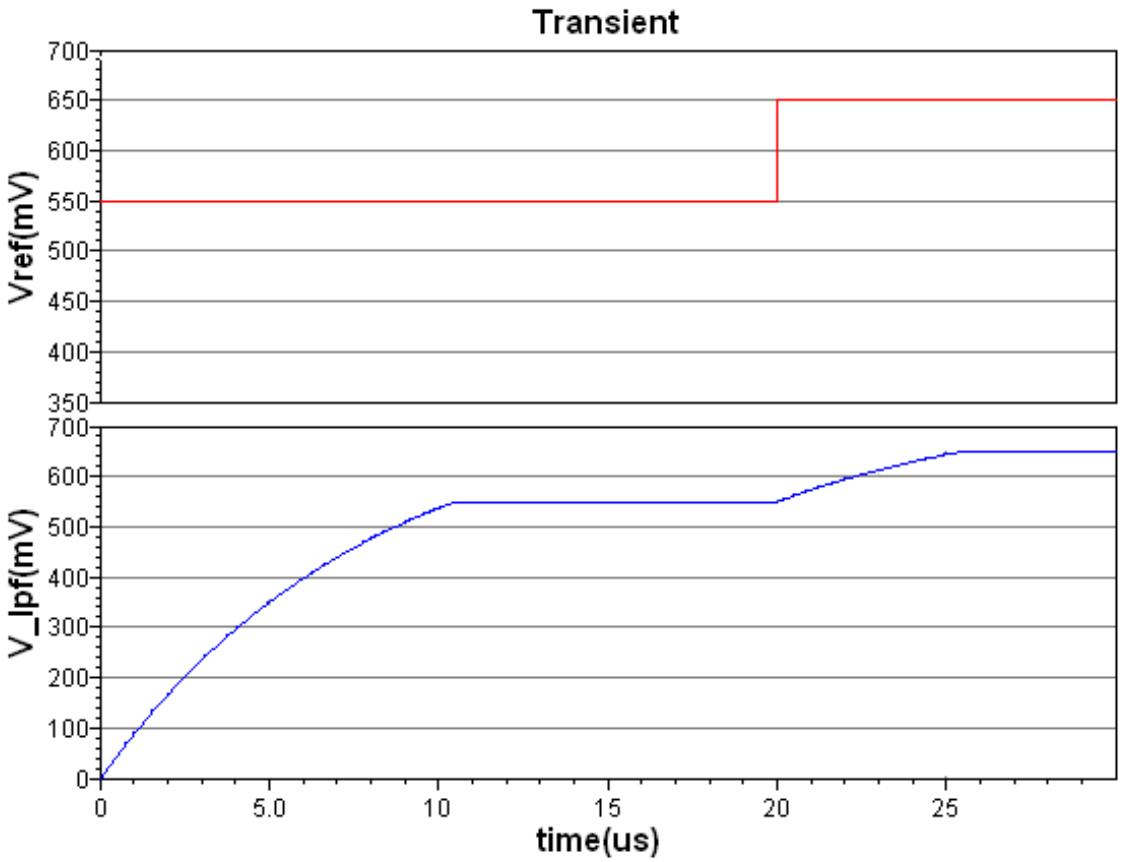


Fig. 5.21: Transient Response

The process variation is another source of the phase shift variation. The proposed method could dramatically reduce the impact of the process variation on the phase shifter's performance. Fig. 5.23 shows the simulation results for the TT (NMOS typical, PMOS typical), SS (NMOS slow, PMOS slow), FF (NMOS fast, PMOS fast), SF (NMOS slow, PMOS fast) and FS (NMOS fast, PMOS slow) process corners. In this simulation, the reference voltage (Vref) was set at 400mV which is equivalent to a 120˚ phase difference.

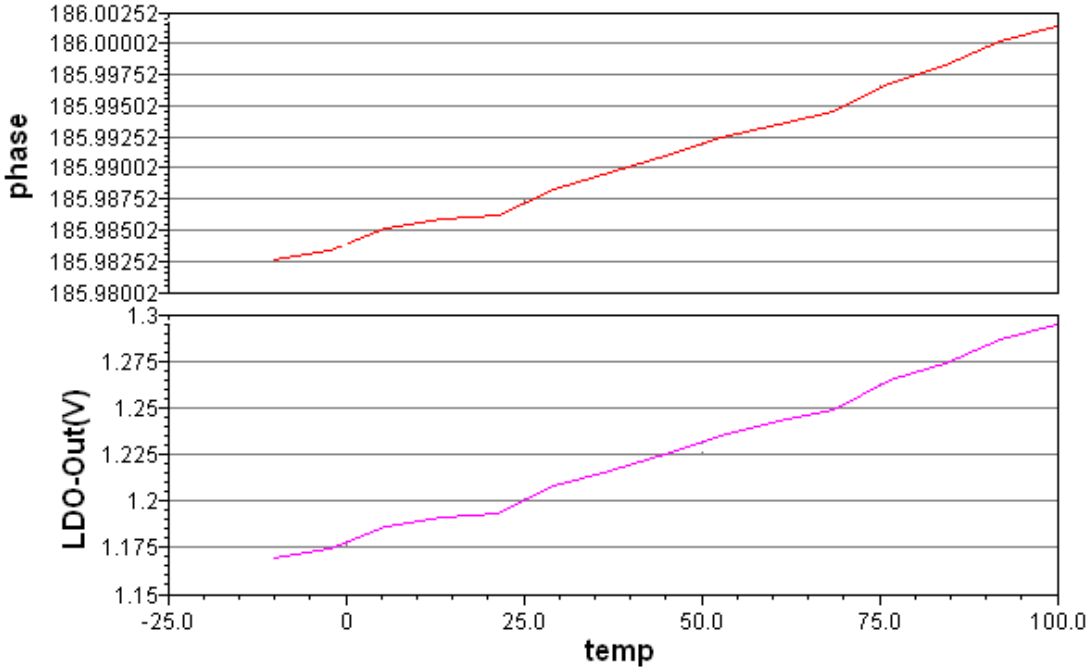


Fig. 5.22: Phase and LDO Voltage Variation over Temperature

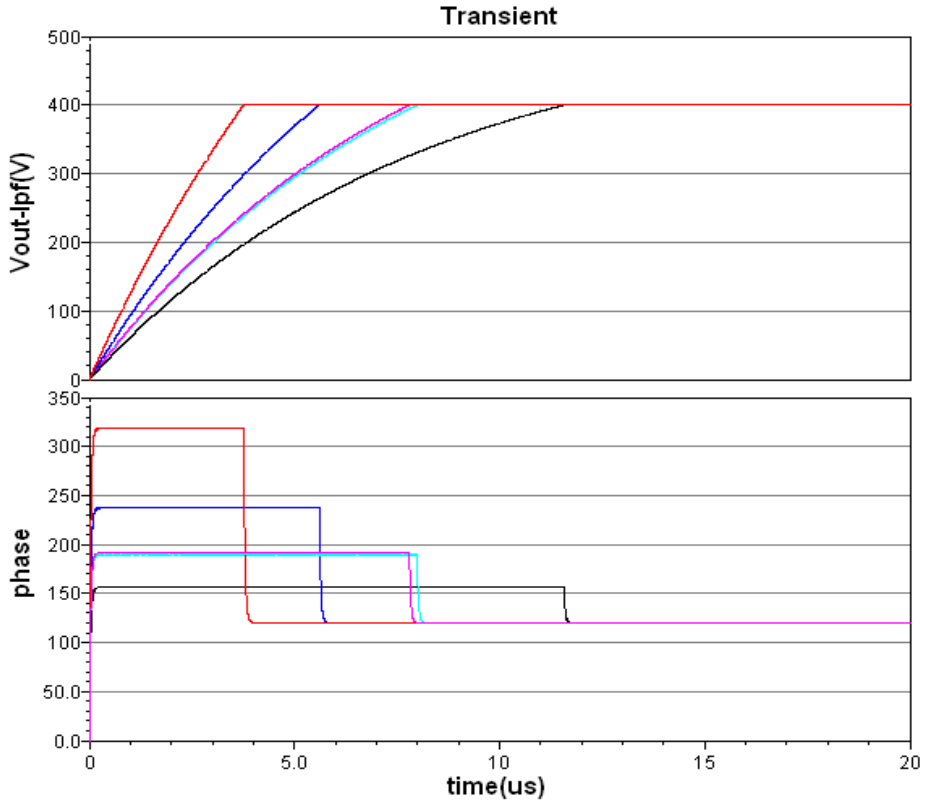


Fig 5:23: Performance of the Proposed Method on Process Variations

The top graphs in Fig. 5.23 shows how the output voltage of the low pass filter is locked at the 400mV reference voltage (see Vref in Fig. 5.20) for different process corners. The bottom graphs shows the corresponding phase differences and all of them are locked at the 120˚ phase difference.

The simulation results show that the proposed method is an effective way to maintain the phase shifter delay constant over the temperature and process variation. This method can be used to control the total delay of the phase shifter by adjusting the reference voltage of the amplifier (Vref) as well.

Chapter 6 Conclusion and Future Work

The new active phase shifting scheme which was developed and verified during the course of this research has a few advantages over the other existing approaches and can be applied to a wide variety of intelligent integrated multi-antenna radio systems. The proposed phase shifter is fully transistor based and it is capable of achieving a very high phase shift resolution over a wide range of frequencies. To reduce the dependency of the phase shifter performance on process variations and temperature changes, an effective new stabilization method was proposed. However, the proposed phase shifter consumes more power and its maximum operating frequency is less than that of the other LO phase shifters. The following table compares the new phase shifter with other published LO phase shifters.

Table 6.1: LO Phase Shifters Summary

Phase Shifter / Criteria	**Proposed Phase Shifter**	**VCO Phase Shifter**	**RC-Bridge Phase Shifter**
Resolution	✓	✗	✓
Bandwidth	✓	✗	✗
Stability	✓	✓	✗
Area	✓	✗	✗
Power consumption	✗	✓	✓
Maximum Frequency	✗	✓	✓

Since we wished to file a patent application for the proposed phase shifter, we have not submitted any paper for publication before this thesis is finalized.

Being based on time-delay, the proposed approach is inherently wide band and can potentially be extended to Ultra-Wide-Band (UWB) systems. The beam-forming of a UWB antenna system is an important but highly challenging problem. Although the

present work has been focused on phase-shifting, the LO delay circuit can be modified for very broadband applications. This is another fruitful research direction.

Although the developed topology and integrated circuit was aimed at lower frequency (below 6 GHz) applications such as wireless communication and sensor network, there is a huge potential to extend the proposed techniques to much higher frequencies by investigating high frequency delay cells like the CML buffer. In fact, there is an ever increasing interest and R&D activity in low-cost/complex smart integrated antenna array technologies for emerging microwave/millimeter-wave systems and applications (such as the newly released 60 GHz band for Gbps data communication, 20GHz/30GHz land mobile satellite internet, etc.). High quality low-cost phase-shifting techniques, which can easily be integrated with the rest of the radio on the same chip, or in the same package, is a key enabler for such systems for mass market applications. One possible and very promising approach, is to use the developed method as an IF phase-shifting block for the whole system.

In addition, the proposed scheme can be extended to large antenna arrays. For this purpose, the architecture should become modularized and scalable. It is possible although, in principle to increase the number of channels on one chip. However, the rapid increase in complexity, cost, and reliability issues may make the multi-chip configuration a more feasible approach. Also, the proposed stabilization technique can be implemented to increase the robustness of the phase shifter.

The integration of the developed phase-shifting technique with multi-band antenna array modules for phased-array and adaptive MIMO applications can be investigated as well.

References

[1] R. G. Stewart and M. N. Giuliano, " X band integrated diode phase shifter, " in *G-MTT Int. Microwave Symp. Dig.,May 1968.pp. 147-154.*

[2] R. P. Coast, "An octave-band switched-line microstrip 3-b diode phase shifter,"*IEEE Trans. Microw. Theory and Tech.,* vol. MTT-21, no. 7, pp.444-449, Jul, 1973.

[3] J. F. White, " High power, p-i-n diode controlled, microwave transmission phase shifters,"*IEEE Trans. Microw. Theory and Tech*. vol. MTT-13, no. 2, pp. 233-242, Mar. 1965

[4] M. E. Davis, "Integrated diode phase-shifter elements for an X-band phase-array antenna," *IEEE Trans. Microw. Theory and Tech*, vol. MTT-23, no. 12, pp. 80-84, Dec. 1975.

[5] F. Ellinger, H. Jackel, and W. Bachtold, "Varactor-loaded transmission-line phase shifter at C-band using lumped elements," *IEEE Trans. Microw. Theory and Tech.* vol. 51, no. 4, pp. 1135-1140, Apr. 2003.

[6] R. N. Hardin, E. J. Downey, and J. Munushian, "Electronically variable phase shifters utilizing variable capacitance diodes, " *Proc. Inst. Radio Eng.,* vol. 48, pp. 944-945, May 1960.

[7] J. P. Srarski, "Optimization of the matching network for hybrid coupler phase shifter," *IEEE Trans. Microw. Theory and Tech.* vol. MTT-25. no. 8, pp. 662-666, Aug. 1977.

[8] F. Ellinger, R. Vogt, and W. Bachtold, "Compact reflective type phase shifter MMIC for C-band using lumped element coupler," *IEEE Trans. Microw. Theory and Tech.* vol. 49, pp. 913-917, May 2001.

[9] F. Beaudoin et at., "A fully integrated tri-band, MIMO transceiver RFIC for 802.16e," *IEEE Radio Freq. Integrated Circuit Symp.* pp. 113-116, 2008.

[10] J. D. Fredrick, Y. Wang, and T. Itoh, "A smart antenna receiver array using a single RF channel and digital beamforming," *IEEE Trans. Microw. Theory and Tech.* vol. 50, NO. 12, pp. 3052-3058, December 2002.

[11] J. Nisbet, "Polar modulators for 1 and 2GHz power amplifier correction," *IEEE BCTM 5.4,* pp. 94-97, 2001.,

[12] P-Y. Chen et at., "K-band HBT and HEMT monolithic active phase shifters Using vector sum method," *IEEE Trans. Microw. Theory and Tech.* vol. 52, no. 5, May 2004.

[13] S. J. Kim, and N. H. Myung, "A new active phase shifter using a vector sum method," *IEEE Microw. and Guided Wave Letters,* vol. , no. 6, June 2000.

[14] F. Ellinger, R. Vogt, and W. Bachtold, "Ultra compact, low loss, varactor tuned phase shifter MMIC at C-band," *IEEE Microw. and Wireless Components letters,* vol. 11, no. 3, March 2001.

[15] J. Paramesh, R. Bishop, K. Soumyanath, and D. Allstot, "A 1.4V 5GHz four-antenna Cartesian combining receiver in 90nm CMOS for beamforming and spatial diversity applications," *IEEE Int. Solid-State Circuit Conference,* pp.2-212. Feb. 2005.

[16] A. Hajimiri, A. Komijani, A. Natarajan, R. Chuara, and X. Guan, "Phase array systems in silicon," *IEEE Communications Magazine,* pp. 122-130. Aug. 2004.

[17] A. Hajimiri *et al.,* "Integrated phased array systems in silicon" *Proceedings of the IEEE,* vol. 93, no. 9, pp. 1637-1655, Sep. 2005.

[18] H. T. Friis, "Noise figure of radio receivers," *Proceedings. IRE,* Vol. 32, pp. 419-422, July 1944.

[19] M. Chua and K. W. Martin, "1 GHz Programmable analog phase shifter for adaptive antennas" *IEEE Custom Integrated Circuits Conference,* pp. 71-74, 1998.

[20] K. Nakahara *et al.,* "A novel three phase-state phase shifter," *IEEE int. Microw. Sym. Dig.,* pp.369-372, 1993.

[21] M. J. Gingell, "Single sideband modulation using sequence asymmetric polyphase networks," *Elect. Commun,* vol 48, pp21-25, 1973.

[22] T. Yu and G. M. Rebeiz, "A 24 GHz 4-channel phased-array receiver in 0.13um CMOS," *IEEE Radio Freq. Integrated Circuit Symp.,* pp.361-364, 2008.

[23] T. Yu and G. M. Rebeiz, "A 24 GHz 6-bit CMOS phased-array receiver," *IEEE Microw. and Wireless Components Letters,* vol. 18, no. 6, pp. 422-424, 2008.

[24] D. Viveiros, Jr., D. Consonni and A. K. Jastrzebski, "A tunable all-pass MIMIC active phase shifter," *IEEE Trans. Microw. Theory and Tech.* vol., 50, no. 8, pp. 1885-1889 August 2002.

[25] M. Chu *et al., "*A 5Ghz wide-range CMOS active phase shifter for wireless beamforming applications," *IEEE TU3B-5.* pp. 47-50, 2006.

[26] H. Hayashi and M. Muraguchi, "An MMIC active phase shifter using a variable resonant circuit," *IEEE Trans. Microw. Theory and Tech.,* vol., 47, no. , pp. 2021-2026, October 1999.

[27] K. J. Koh, and G. M. Rebeiz, "0.13um CMOS phase shifters for X-, K*u*-, and K-band phased arrays," *IEEE Journal of Solid-State Circuits,* vol., 42, no. 11, pp. 2535-2546, November 2007.

[28] H. Hashemi *et al., "*A 24-GHz SiGe phased-array receiver LO phase-shifting approach," *IEEE Trans. Microw. Theory and Tech.,* vol. 53, no. 2, pp. 614-626, February 2005.

[29] T. Yamaji, D. Kurose, O. Watanabe, S. Obayashi, and T. Itakura, "A four-input beam-forming downconverter for adaptive antennas," *IEEE Journal of Solid-State Circuits,* vol. 38, no. , pp. 1619-1625 October 2003.

[30] J. Savoj and B. Razavi, "A -Gb/s CMOS clock and data recovery circuit with a half-rate binary phase-frequency detector," *IEEE Journal of Solid-State Circuits,* vol. 38, no. 1, pp. 13-21, January 2003.

[31] Y. Palaskas *et al., "*A 5-GHz 8-Mb/s 2x2 MIMO transceiver RFIC with fully integrated 20.5-dBm P1dB power amplifiers in 90-nm CMOS," *IEEE journal of Solid-State Circuits,* vol. 41, no. 12, pp. 2746-2756, Dec. 2006.

[32] T. W. Nuteson, and G. S. Mitchell, "Digital beamforming for smart antennas," *IEEE MTT-S Digest,* pp. 125-128, 2001.

[33] Z. Shenghua, X. Dazhuan, J. Xueming, "A new receiver architecture for smart antenna with digital beamforming," *IEEE Int. Sym. On Microw., Antenna, Propagation and EMC Tech. for Wireless Communication Proceedings,* pp. 38-40, 2005.

[34] J. M. Rabaey, " Digital Integrated Circuits, " *Prentice Hall Electronic and VLSI Series, 1996*

[35] B. Razavi, “RF Microelectronics,” *Prentice Hall, 1997*

[36] T. Yamaji, H. Tanimoto, S. Obayashi, and Y. Suzuki, “A Si 2-GHz 5-bit LO phase-Shifting downconverter for adaptive antennas, “*in Proc. Symp. VLSI Circuits,* 2000, pp. 66-67.

[37] David A. Johns, Ken Martin, “Analog Integrated Circuit Design,” *John Wiley & Sons, 1997*

[38] Paul R. Gray, Robert G. Meyer, “Analysis and Design of Analog Integrated Circuits, “*John Wiley & Sons, 1997*

[39] B. Razavi, “Design of Analog CMOS Integrated Circuits,” *McGra-Hil, 2000*

[40] Bram De Muer and Michiel Steyaert, “CMOS FRACTIONAL-N SYNTHESIZERS,” *Kluwer Academic Publishers 2003*

[41] C.G Sodin, P.K. Ko and J.L. Moil, “The Effect of High Field on MOS Device and Circuit Performance,” *IEEE Tran. on Electron Devices, vol. 31, pp. 1386-1393, Oct. 1984.*

[42] T. Sakurai and A. Richard Newton, “Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas,” *IEEE Journal of Solid-State Circuits, vol. 25, no. 2, April 1990.*