Development of Low-Temperature Epitaxial Silicon Films and Application to Solar Cells

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

Solar photovoltaic has become one of the potential solutions for current energy needs and for combating greenhouse gas emissions. The photovoltaics (PV) industry is booming, with a yearly growth rate well in excess of 30% over the last decade. This explosive growth has been driven by market development programs to accelerate the deployment of sustainable energy options and rapidly increasing fossil fuel prices. Currently, the PV market is based on silicon wafer solar cells (thick cells of around 150–300 µm made of crystalline silicon). This technology, classified as the first-generation of photovoltaic cells. The second generation of photovoltaic materials is based on the introduction of thin film layers of semiconductor materials. Unfortunately, the conversion efficiency of the current PV systems is low despite the lower manufacturing costs. Nevertheless, to achieve highly efficient silicon solar cell devices, the development of new high quality materials in terms of structure and electrical properties is a must to overcome the issues related to amorphous silicon (*a* -Si:H) degradation. Meanwhile, to remain competitive with the conventional energy sources, cost must be taken into consideration. Moreover, novel approaches combined with conventional mature silicon solar cell technology can boost the conventional efficiency and break its maximum limits. In our approach, we set to achieve efficient, stable and affordable silicon solar cell devices by focusing on the development of a new device made of epitaxial films. This new device is developed using new epitaxial growth phosphorous and/or boron doped layers at low processing temperature using plasma enhanced chemical vapor deposition (PECVD). The junction between the phosphorous or boron-doped epitaxial film of the device is formed between the film and the p or n-type crystalline silicon (c-Si) substrate, giving rise to (n *epi-Si*/p c-Si device or p *epi-Si*/n c-Si device), respectively. Different processing conditions have been fully characterized and deployed for the fabrication of different silicon solar cells architectures. The high quality epitaxial film (up to 400 nm) was used as an emitter for an efficient stable homojunction solar cell. Extensive analysis of the developed fine structure material, using high resolution transmission electron microscope (HRTEM), showed that hydrogen played a crucial role in the epitaxial growth of highly phosphorous doped silicon films. The main processing parameters that influenced the quality of the structure were; radio frequency (RF) power density, the processing chamber pressure, the substrate temperature, the gas flow rate used for deposition of silicon films, and hydrogen dilution. The best result, in terms of structure and electrical properties, was achieved at intermediate hydrogen dilution (HD) regime between 91 and 92% under optimized deposition conditions of the rest of the processing parameters. The conductivity and the

carrier mobility values are good indicators of the electrical quality of the silicon (Si) film and can be used to investigate the structural quality indirectly. The electrical conductivity analyses using spreading resistance profile (SRP), through the detection of active carriers inside the developed films, are presented in details for the developed epitaxial film under the optimized processing conditions. Measurements of the active phosphorous dopant revealed that, the film has a very high active carrier concentration of an average of 5.0×10^{19} cm^{-3} with a maximum value of 6.9×10^{19} cm^{-3} at the interface between substrate and the epitaxial film. The observed higher concentration of electrically active P atoms compared to the total phosphorus concentration indicates that more than half of dopants become incorporated into substitutional positions. Highly doping efficiency η_d of more than 50 % was calculated from both secondary ion mass spectroscopy (SIMS) and SRP analysis. A variety of proposed structures were fabricated and characterized on planar, textured, and under different deposition temperatures. Detailed studies of the photovoltaic properties of the fabricated devices were carried out using epitaxial silicon films. The results of these studies confirmed that the measured open circuit voltage (V_{oc}) of the device ranged between 575 and 580 mV with good fill factor (FF) values in the range of 74-76 %. We applied the rapid thermal process (RTP) for a very short time (60 s) at moderate temperature of $750^{o}C$ to enhance the photovoltaic properties of the fabricated device. The following results were achieved, the values of V_{oc}, and the short circuit current (I_{sc}) were 598 mV and 27.5 mA respectively, with a fill factor value of up to 76 % leading to an efficiency of 12.5 %. Efficiency enhancement by 13.06 % was achieved over the reference cell which was prepared without using RTP. Another way to increase the efficiency of the fabricated device is to reduce the reflections from its polished substrate. This was achieved by utilizing the light trapping technique that transforms the reflective polished surface into a pyramidical texturing using alkaline solutions. Further enhancements of both V_{oc} and I_{sc} were achieved with values of 612 mV and 31mA respectively, and a fill factor of 76 % leading to an increase in the efficiency by up to 13.8 %. A noticeable efficiency enhancement by ~20 % over the reference cell is reported for the developed devices on the textured surfaces. Moreover, the efficiency of the fabricated epitaxial silicon solar cells can be boosted by the deployment of silicon nanocrystals (Si NCs) on the top surface of the fabricated devices. In the course of this PhD research we found a way to achieve this by depositing a thin layer of Si NCs, embedded in amorphous silicon matrix, on top of the epitaxial film. Structural analysis of the deposited Si NCs was performed. It is shown from the HRTEM analysis that the developed Si NCs, are randomly distributed, have a spherical shape with a radius of approximately 2.5 nm, and are 10-20 nm apart in the amorphous silicon matrix. Based on the size of the developed Si NCs, the optical band

gap was found to be in the region of 1.8-2.2 eV. Due to the incorporation of Si NCs layer a noticeable enhancement in the I_{sc} was reported.

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Dedication

To my parents, my wife and my sons, Mohamed, Abdurrahman, Omar and Moaaz.

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Chapter 1: Introduction, motivation and research methodology

Introduction

Energy plays a vital role in our life and our economy, however, our consumption of it can have a lasting and damaging effect on the environment. Nowadays, the main energy sources for human activity are fossil and mineral fuels, and nuclear. Though, these sources are important they are very harmful to the environment because they cause global warming, ozone layer depletion, biosphere destruction, and ecological devastation. Consequently, the actual energy production has been considered harmful, both in terms of pollution and the impact on the environment, since the industrial revolution in the 18th century [1–3]. On the one hand around 80 wt% of CO_2 emissions in the world are originated from the energy sector, but on the other hand, clean power generation processes are a suitable form of renewable energy sources such as solar, wind, geothermal, and ocean thermal. Clean energy generation has become increasingly important with a growing significance of environmental issues but it also faces a significant number of restrictions. For example, solar energy is a clean energy source, but it is intermittent in nature and does not persist continually for long durations at a given location. A considerable amount of money has been invested in research and development, several governments set up substantial market introduction programs, and the industry has also invested in large energy production facilities. Photovoltaic (PV) is the technological symbol for a future sustainable energy supply system around the world. No other renewable energy technology has received a strong appreciation by the public, and more importantly by the politicians, as well as, the industrial and financial sectors. This is a remarkable situation since PV electricity is regarded as much too expensive compared to conventional grid electricity. Solar photovoltaic and thermal applications appear to be some of the potential solutions for current energy needs and to combat greenhouse gas

emissions. The high and justified recognition of PV may be understood on the basis of a description of the main positive features of this kind of solar electricity conversion. The PV industry is booming, with a growth rate well in excess of 30% per year over the last decade [4]. This explosive growth has been driven by market development programs to accelerate the deployment of sustainable energy options and rapidly increasing fossil fuel prices. Even if solar energy is free and abundant, still, PV technology represents only around 0.04% of the fuel share of world's total primary energy supply [5]. Continuous advances in PV technology lead to a decrease in the PV energy cost in the last 20 years. Currently, PV market is based on silicon wafer solar cells (thick cells of around 150–300 nm made of crystalline silicon). This technology, classified as the first-generation of photovoltaic cells, accounts for more than 86% of the global solar cell market. The second generation of photovoltaic materials is based on the introduction of thin film layers for cell fabrication of semiconductor materials. Although the cost of manufacturing solar cells has gone significantly, the conversion efficiency remains very low this needs more effort to enhance the efficiency through the development of new materials and simple fabrication schemes.

1.1 Motivation for the research

Hydrogenated amorphous silicon (*a* Si:H) has been used as the main material for the fabrication of low cost solar cell devices. However, *a* Si:H presents a serious problem of metastability, due to its degradation when it is exposed to light. The physics of instability of an *a* Si:H are associated with its non-equilibrium state, and external disturbances, either thermal or optical, these will induce structural changes at the macro-or microscopic levels. When *a* Si:H is exposed to light, electron-hole pairs are generated. The photo-generated electron-hole pairs combine in the film and release energy, which breaks weak Si-Si and /or Si-H bonds and creates defects, which causes deterioration in the conductivity of the film. For *a* Si:H solar cells, these photo-generated mid-gap defects act as recombination centers, thereby reducing the lifetime of both electrons and holes. These defects also

act to reduce the electric field in the middle portion of the "intrinsic" i-layer, and this in turn reduces the field assisted drift length or range and decreases the collection of the carriers in i-layer. In order to improve the stability of *a* Si:H, all kinds of research have been carried out, including the development of new deposition materials, new fabrication methods, and new structures for the solar cell devices.

The most used semiconductor material in PV is silicon (Si) which is the most abundant material on the earth crust. Silicon is also the most used material in microelectronics due to its excellent electronic properties. In PV technology mono-crystalline silicon (c-Si) has been the first material for solar cell fabrication, and c-Si solar cells still represent the larger photovoltaic market share. A combination of monocrystalline silicon with *a* Si:H, gives rise to the a-Si/c-Si heterojunction solar cell with efficiencies up to 15-16 % for industrial market. The maximum thermodynamic efficiency for the conversion of unconcenterated solar cells was calculated by Shockley and Queisser [6, 7] to be nearly 31% due to the involved loss mechanisms. One of the major loss mechanisms, leading to low energy conversion efficiencies of solar cells, is the thermalization of charge carriers generated by the absorption of high-energy photons. Nevertheless, new approaches and new materials can lead to the break of the fundamental limits and maximum efficiency conversion. To achieve highly efficient silicon solar cells, the development of new high quality materials, in terms of structure and electrical properties, is a must to overcome the issues related to *a* Si:H. At the same time the fabrication of solar cell devices must compete with the conventional energy sources in terms of price.

In our approach, we set to achieve efficient, stable and affordable silicon solar cell devices by focusing on the development of a new device made of epitaxial films that are deposited at low temperature using industrial systems as plasma enhanced chemical vapor deposition PECVD. In this device the junction between a p-doped epitaxial layer and n-doped epitaxial layer is formed between the epitaxial grown layer and the c-Si wafer substrate, giving rise to (*p* epi-Si/n c-Si device or *n* epi-Si/p c-Si device). Moreover, silicon nanocrystals (Si NCs) have been known to possess interesting

properties such as bandgap modulation with NC size, as a result of their wide gap, the new photovoltaic (Si NCs) is a good alternative to enhance the efficiency of the conventional devices by the absorption of a specific range of the solar spectrum. Hence, the efficiency of the fabricated epitaxial silicon solar cells can be boosted by the deployment of silicon nanocrystals for band gap engineering.

1.2 Methodology of the research:

The workhorse for the photovoltaic devices is the material used to fabricate the designed devices. So, the main objectives are divided into two main parts (i) Material development at low temperature using PECVD system and detailed characterization tools (ii) Device fabrication, full analysis, and measurement schemes:

- The material quality (from structure, optical, and electrical properties point of view), is crucial for stable and highly efficient solar cells devices. The development of new high quality epitaxial phosphorous and boron doped silicon films, to be used as an emitter in homo and/or heterojunction devices, will be the main focus in the first part of this research.
- A full characterization and analysis schemes are applied to investigate the growth mechanisms, crystallinity, and any related structure defects, such as twins and stacking faults, and electrical properties such as conductivity, mobility, resistivity and minority carrier diffusion length.
- Optimize a full scheme of the rapid thermal annealing process (RTP) profiles, and then apply these profiles on some low quality films. Explore the benefits of using different heating and cooling rates and the maximum heating temperature used, taking into account thermal stress, some issues such as the hydrogen effusion from the film, and surface roughness of the film due to the annealing process.

- Fabrication of silicon solar cells under different deposition, annealing and preparation conditions in order to achieve stable and efficient silicon solar cells. Explore the PV properties of the fabricated devices using standard characterizing techniques, such as spectral response and solar simulators.
- Moreover, silicon nanocrystals, embedded in amorphous silicon matrix, were developed and characterized to enhance the efficiency of the developed solar cells devices. The benefit of using silicon nanocrystals on top the developed epitaxial silicon cell is to harvest most of the incident solar spectrum; the results are presented as a future work.

1.3 Structure of This Thesis

The aim of this thesis is to develop and examine the structural, optical an electrical properties of epitaxial phosphorous and boron doped silicon films for high efficiency silicon solar cells, and the enhancement of the efficiency of the developed silicon solar cell devices by deployment of silicon nanocrystals.

In Chapter 2 we review the monocrystalline silicon and thin film technology, physics of the solar cells with more focus on homo and heterojunction structures. Different techniques used to deposit thin films are reviewed with a focus on PECVD, which will be our main processing system for silicon film development. A focused review of the basic physics and chemistry of non-equilibrium glow discharges, and the description of the influence of ions on the developed films, and the different characterization tools involved in this thesis.

In Chapter 3 and 4 we focus on the development of low temperature phosphorous doped epitaxial Si films and boron doped quasi-epitaxial Si films using trimethylboron (TMB). The optimization of the rapid thermal annealing temperature profiles, analysis of the influence of the variety of heating, cooling rates, and peak annealing temperature are investigated in detail. Techniques including high

resolution transmission electron microscopy (HRTEM), micro-Raman spectroscopy, secondary ion mass spectroscopy (SIMS), spreading resistance profile (SRP) were employed to gather structural information, growth mechanisms, chemical and electrical properties of the developed epitaxial phosphorous and boron doped silicon films.

Chapter 5 is dedicated to the fabrication procedure of efficient, stable epitaxial silicon solar cells, under different processing conditions. Full photovoltaic characterization properties are achieved as current-voltage analysis, external quantum efficiency (EQE), and internal quantum efficiency (IQE) characterization under different processing conditions.

Chapter 6 is dealing with the development of silicon nanocrystals to enhance the efficiency of the developed epitaxial cells, full material structure analysis using HRTEM, X-ray diffraction (XRD), and Micro-Raman spectroscopy were employed to gather structural information about the silicon nanocrystals, the results and recommendations for future work will be presented in this chapter.

Chapter 7 summaries and conclusions of this thesis, discussion of possible directions, and extension of this work in the near future at the Centre for advanced photovoltaic devices and systems (CAPDS) lab.

Chapter 2

Background on experimental procedure and silicon technology

Introduction

The workhorse of the photovoltaics industry is silicon. More than four out of five amperes of solar-module produced current come from crystalline silicon modules. So, the first part of this chapter is dedicated to silicon, its extraction, purification, and different preparation techniques and summary of the processes involved. The second part is underlying the physical principle and operation of the solar cells and the description of the basic operating characteristics, which used to define the basic solar cell figures of merit, namely, the open-circuit voltage (V_{oc}), the short-circuit current (I_{sc}), the fill factor (FF), and the conversion efficiency (η). In the third part, we present a brief summary of the different processing techniques for thin film technology, with more details for plasma-enhanced chemical vapor deposition technique (PECVD), emphasizing issues as the variety of different deposited films by this technique and a review of the basic physics and chemistry of non-equilibrium glow discharges, and describe the influence of ions on the development films. A description of the highest reported crystalline silicon solar cell and thin film silicon solar cells technologies are discussed including the issues and problems related to each type. Finally, the characterization tools used for the material analysis and devices characterization are described in details.

2.1 Silicon Material Feedstock

2.1.1 Production of metallurgical grade silicon

Silicon is the most commonly occurring element on the earth. It mainly occurs as silicon dioxide (SiO_2) in quartz and sand. Its synthesis has been familiar for many decades. It is extracted from (mainly) quartzite reduction with carbon in an arc furnace process. The process occurs at high

temperature (>1600°C), and the gaseous byproduct is evacuated from the furnace leaving behind silicon powder referred to as metallurgical grade silicon (MG-Si) [8]. Metallurgical silicon (MG-Si) is the starting material for most fabrication methods of single crystalline silicon. MG-Si itself is an extremely "impure" material (≈98.5% purity) and hence is unsuitable for direct fabrication of electronic devices, including photovoltaic cells.

The MG-Si must be further purified, this is usually achieved by hydrochlorination of silicon. The ultra-high purity is needed to ensure exacting semiconductor properties in the grown silicon crystals. This is achieved first by the preparation of a volatile silicon hydride and its purification generally using fractional distillation. This is followed by the decomposition of this hydride to hyper pure elemental silicon by reductive pyrolysis or chemical vapor deposition. The preparation of the volatile Si compound involves external reactants and its decomposition generates by-products, which need to be recycled. The various polysilicon routes therefore must control four successive steps; (i) preparation/synthesis of the volatile silicon hydride, (ii) purification, (iii) decomposition to elemental silicon, and (iv) recycling of by-products. Three main large commercial processes are currently active for polysilicon production:

Siemens process

In the first stage pulverised metallurgic silicon is exposed to hydrochloric gas in a fluidized-bed reactor. Trichlorosilane and hydrogen are produced by the chemical reaction;

$$Si + 3\,HCl = SiHCl_3 + H_2 \quad (2.1)$$

Since trichlorosilane is a liquid at temperatures below 30°C it can easily be separated from hydrogen. The chlorides of the impurities from the process must now be separated from the trichlorosilane. In a second stage the trichlorosilane is freed from these impurities in fractional distillation columns. The other silicon chlorides are also removed. Trichlorosilane distilled in this way fulfils the requirements for electronic grade silicon

A mixture of hydrogen (which must also be high-purity) and trichlorosilane ($SiHCl_3$) is introduced into the reactor vessel. Trichlorosilane is reduced to silicon on the hot surface of the

silicon, which deposits itself on the rod surface. The process takes place according to the following formula:

$$4\ SiHC1_3 + 2\ H_2 = 3\ Si + SiC1_4 + 8\ HCI \qquad (2.2)$$

Thus, high-purity polycrystalline silicon is produced in a continuous process to rod diameters up to 30 cm and rod lengths up to approximately 2 m in this process.

Union Carbide Chemicals

In a more recent process developed, the trichlorosilane has been replaced by monosilane SiH_4, but the principle of decomposition on a heated silicon rod inside a closed deposition chamber is maintained.

$$SiH_4 = Si + 2H_2 \qquad (2.3)$$

Ethyl Corporation process,

Finally, in the third process, also making use of monosilane SiH_4, the heated silicon rod in the closed reaction chamber has been replaced by a fluidised bed of heated silicon particles. The particles act as seeds on which SiH_4 is continuously decomposed to larger granules of hyper-pure silicon.

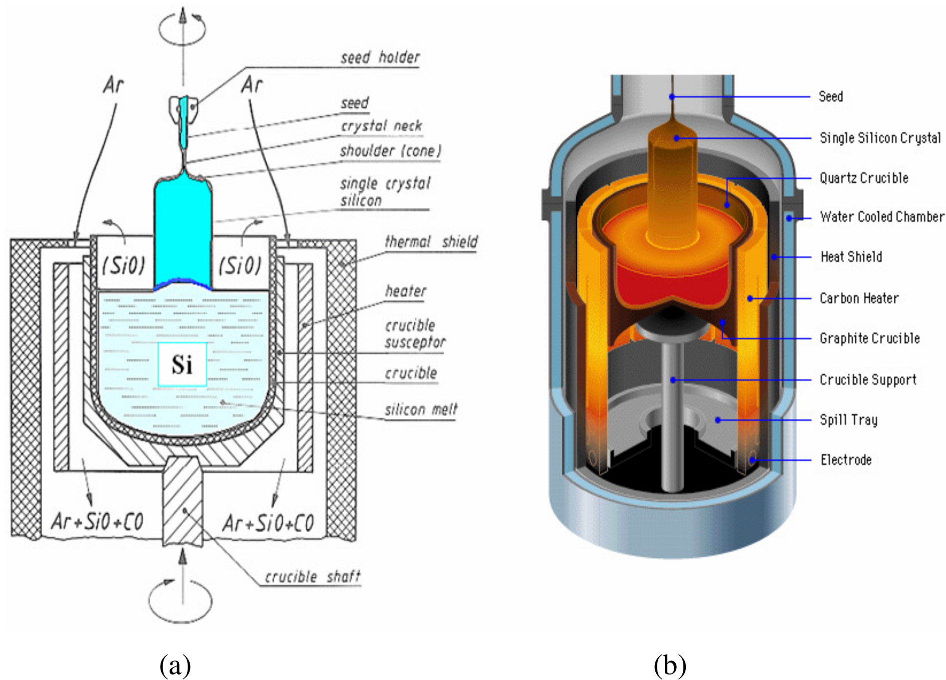
2.1.2 Crystal Pulling Process

For the manufacture of semiconductor devices, as well as having high purity levels, the silicon should be in single crystal form and free of defects. Two processes have become established, the crucible pulling process, also known as the Czochralski Process [9] and the float zone pulling process.

The Czochralski (CZ) Process

Polycrystalline material in the form of fragments obtained from polysilicon is placed in a quartz crucible, which is itself located in a graphite crucible, and melted by induction heating under inert gases. Figure 2.1 shows the schematic diagram of single crystal pulling by the Czochralski process. The pulling process begins with the immersion of the single crystal silicon seed. The vertical pulling movement and the rotary movement silicon to grow in monocrystalline form on

the seed crystal. Extremely precise balancing and control of both movements and precise control of the temperature of the silicon melt allows the diameter of the crystal to be precisely adjusted. Adding highly doped silicon fragments permits the simultaneous adjustment of the desired doping, dependent upon level and type of conductivity. It is unavoidable that a certain amount of oxygen, originating from the quartz crucible, is incorporated in the crystal during this process. In Cz reactors, quartz (silica) is used as the crucible material because its product of reaction, silicon monoxide (SiO), evaporates easily from the melt. However, Cz-grown Si crystals contain 10^{17} – 10^{18} cm^{-3} of interstitial oxygen. For most semiconductor applications this is of minor importance, and in some cases is even used to good effect to achieve gettering. For high efficiency solar cells, however, it is a disadvantage as oxygen forms precipitates, which act as recombination centers and reduce the lifetime of charge carriers.



(a) (b)

Fig. 2.1: Single crystal pulling by the Czochralski process, (a) schematic diagram, left (b) cross section of the pulling system (right), adapted from [9].

Today crystals with diameters of 30 cm and more are grown routinely for the semiconductor market. For solar cells, smaller diameter crystals are grown because the usual solar cell

dimensions are 10 cm x 10 cm. The round crystals are usually shaped into squares with rounded corners in order to obtain a better usage of the module area. Recently, interesting results have been obtained with an advanced technique, magnetically grown Czochralski (MCz) silicon [10]. The magnetic field interacts with the free electrons of the silicon and retards convective melt flows. The transport of oxygen from the crucible walls is minimized. Furthermore the distribution of impurities is more uniform.

Float Zone Pulling (FZ)

In the float zone pulling (FZ), the starting point is a polycrystalline rod, produced by the CVD process. The principle is explained in more detail based on Figure 2.2. Figure 2.2 shows the single crystal pulling by the float zone pulling method. The puller is located within an enclosure flushed with inert gas. At the lower end a single crystal seed is again melted onto the polycrystalline rod by induction heating. After melting, a region of liquid silicon is propelled upwards by the vertical movement of the induction coil whilst being rotated. When the silicon cools, it solidifies in single crystal form. The desired doping is achieved by the addition of a suitable dopant in gaseous form (e.g. phosphine or diborane) to the inert gas. One advantage of this process is the additional cleaning of the crystal. Impurities (in particular metallic impurities) possess a very low segregation coefficient), i.e. their solubility in liquid silicon is some orders of magnitude higher than in solids. One major advantage of the FZ process is that there is no crucible to have contact with, and hence minimal risk of contamination. Obviously, FZ-grown Si has much less oxygen compared to CZ silicon which cannot be avoided with the Cz-material because of the quartz crucible. However, it is very difficult to produce large wafer sizes by the FZ method. This material is of exceptional purity because no crucible is needed but is more costly than Czochralski (Cz) material. Float zone (Fz) material is frequently used in R&D work. Record efficiency solar cells have been manufactured with float zone material but it is too expensive for regular solar cell production, where cost is of overriding importance. Hence CZ remains the most widely used method.

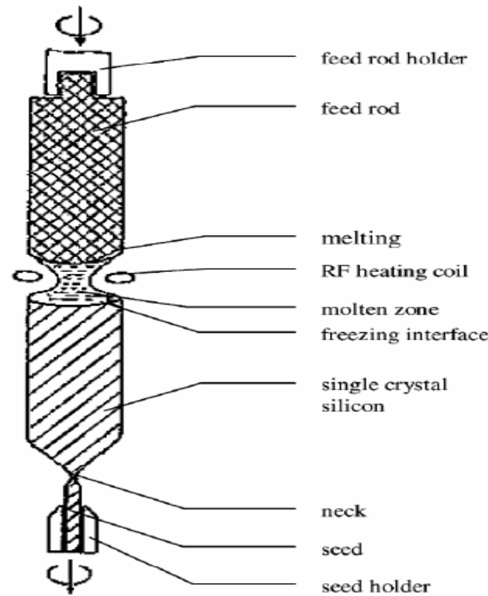


Fig. 2.2: Single crystal pulling by the float zone pulling method [11].

2.2 Ribbon silicon

The goal of crystalline ribbon technologies is to reduce cost by eliminating the costly silicon sawing process and at the same time minimizing the amount of silicon due to a reduced layer thickness. Supposing sufficient bulk quality, the resulting ribbons can be used directly as wafers for solar cell processing. If low quality materials like metallurgical grade silicon are used, a subsequent epitaxial growth of a highly pure active silicon layer is mandatory. In this case, the ribbons are used as a mechanical substrate and an electrical conductor to the back electrode.

Out of over 20 different approaches which had been under investigation, there are mainly four which are still under development or are about to be commercialized. They will be described in the following section;

Edge defined film fed growth process (EFG)

In the EFG process a self-supporting silicon ribbon is pulled from the melt through a die which determines the shape of the ribbon [12, 13]. Today octagonal tubes of 5.3 m in length at a nominal average wall thickness of 280 mm are pulled out of a graphite crucible containing liquid silicon and are subsequently separated by a neodymium yttrium aluminum garnet (Nd:YAG) laser

[14]. The resulting sheets of 10 cm x 10 cm have a somewhat lower material quality than single crystals, and they have a wavy surface. Nevertheless, conversion efficiencies of up to 14.8% were achieved in the production line with an excellent overall yield of over 90% at the moment and 95% expected in the near future.

String ribbon process

In a fairly simple procedure, silicon ribbons of variable thickness are pulled with two temperature resistant strings directly out of the melt and are cut subsequently into the desired length with diamond tools. The growth speed is up to 25 mm/min resulting in ribbons with a thickness of below 100 mm and a conversion efficiency of 15.1% on a lab cell of 1 cm^2 area [15]. The string ribbon process is under development since 1994 and the principles are described in [16, 17]

Ribbon growth on substrate (RGS)

The main difference of the RGS approach compared to all other processes is that the crystallization direction of the silicon ribbons is not parallel but perpendicular to the pulling direction [18]. The crystallization of the melt is induced by a cooled substrate pulled along the bottom of the crucible. This results in a columnar growth of the grains along the plane normal which enables high pulling speeds and, thus, high production rates [19],

Silicon sheets from powder (SSP)

The method is originally based on a two-step melting process of silicon powder which is poured onto temporary carrier plates. This result in grains of several mm width and some centimeters length and conversion efficiencies of up to 13% were achieved [20].

2.3 Solar cell device physics

Semiconductor solar cells are fundamentally quite simple devices. Semiconductors have the capacity to absorb light and to deliver a portion of the energy of the absorbed photons to carriers of electrical current, electrons and holes. A semiconductor diode separates and collects the carriers and conducts the generated electrical current preferentially in a specific direction. Thus, a

solar cell is simply a semiconductor diode that has been carefully designed and constructed to efficiently absorb and convert light energy from the sun into electrical energy. A metallic grid forms one of the electrical contacts of the diode and allows light to fall on the semiconductor between the grid lines and thus be absorbed and converted into electrical energy. The semiconductor diode is fashioned when an n-type semiconductor and a p-type semiconductor are brought together to form a metallurgical junction. This is typically achieved through diffusion or implantation of specific impurities (dopants) or via a deposition process. The diode's other electrical contact is formed by a metallic layer on the back of the solar cell. All electromagnetic radiation, including sunlight, is composed of particles called photons, which carry specific amounts of energy determined by the spectral properties of their source. The sun has a surface temperature of 5762 K and its radiation spectrum can be approximated by a black-body radiator at that temperature. Figure 2.3 shows the radiation spectrum for a black body at 5762 K, an AM0 spectrum, and an AM1.5 global spectrum [8]. However, the Earth's great distance from the sun means that only those photons emitted directly in the direction of the Earth contribute to the solar spectrum as observed from Earth. Therefore, for practical purposes, the light falling on the Earth can be thought of as parallel streams of photons. Just above the Earth's atmosphere, the radiation intensity, or Solar Constant, is about 1.353 kW/m^2 [21] and the spectral distribution is referred to as an air mass zero (AM0) radiation spectrum. The AM1.5 global spectrum takes into account the light reflected, diffused and absorbed by the atmosphere. The number 1.5 is the air mass, defined as, air mass = $1/cos\theta$, where θ is the angular position of the sun with respect to the zenith. AM1.5 Global is a standard spectrum used to characterize photovoltaic devices. The integrated power density of AM1.5 spectrum is normalized to a conventional value of 1 kW/m^2, very close to the maximum power received at the earth surface for air mass = 1.5, i.e. $\theta = 48.2^o$ [21].

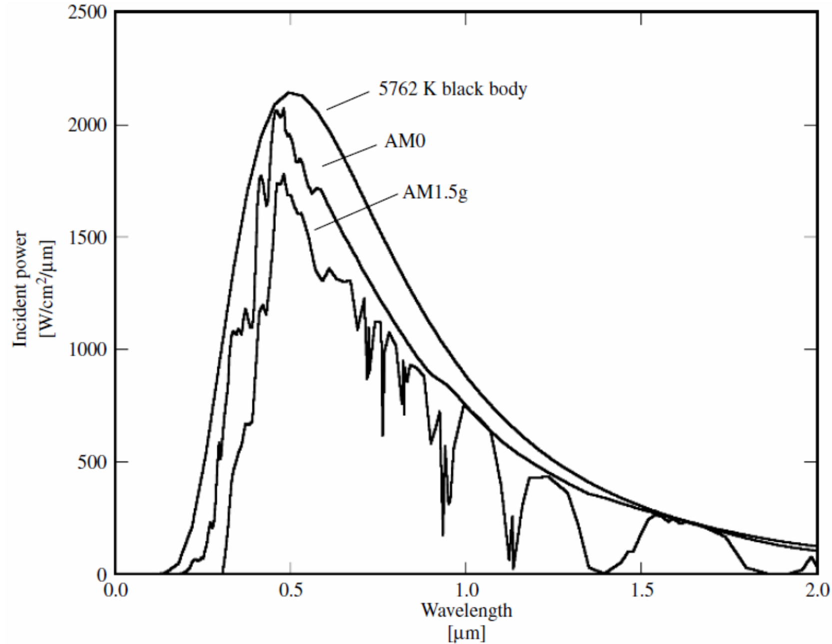


Fig. 2.3: The radiation spectrum for a black body at 5762 K, an AM0 spectrum, and an AM1.5 global spectrum [8].

2.3.1 Homojunction structure

The most common device fabricated to realize the photovoltaic conversion is the semiconductor solar cell. The “classical” solar cell consists of a p-doped and an n-doped semiconductor material (usually the same material, homojunction), forming a p/n junction. Figure 2.4 shows the energy band structure of a p/n junction diode. When the metallurgical junction between the semiconductor domains with different doping is formed, a majority carrier diffusion transport (holes in the p-doped layer and electrons in n-doped layer) is present through the junction, due to a charge carrier concentration gradient. To reach thermal equilibrium, electrons/holes close to the metallurgical junction diffuse across the junction into the p-type/n-type region where hardly any electrons/holes are present. This process leaves the ionized donors (acceptors) behind, creating a region around the junction, which is depleted of mobile carriers (which called depletion region). The charge due to the ionized donors and acceptors causes an electric field, which in turn causes drift of carriers in the opposite direction. The diffusion of carriers continues until the drift current balances the diffusion current, thereby reaching the thermal equilibrium as indicated by a constant

Fermi energy [22]. The electric field is opposite to the diffusion gradient and at thermodynamic equilibrium the diffusion flux of free carriers is counterbalanced by the flux due to the electric field in the depletion region. In a first approximation the depletion region can be considered abrupt, i.e. outside the charged region the semiconductor is neutral (quasi-neutral regions). When the junction is in equilibrium as shown in Figure 2.4 an electrostatic potential (diffusion potential or built-in potential, V_{bi}) can be detected at the ends of the device coming from the electric field of the depletion region.

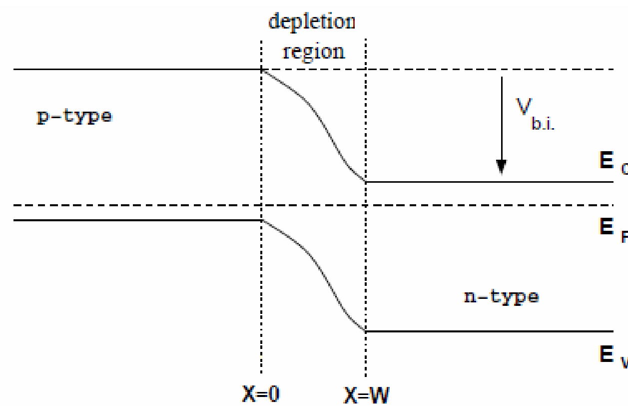


Fig. 2.4: Energy band diagram at thermodynamic equilibrium for a p/n junction adapted from [23, 24].

Carrier Transport in dark conditions

Electrons in the conduction band, being negatively charged, move in the opposite direction of the applied field and holes in the valence band, being positively charged, and move in the same direction of the applied field in other words, electrons sink and holes float. This is a useful conceptual tool for analyzing the motion of holes and electrons in semiconductor devices. With nothing to impede their motion, the holes and electrons would continue to accelerate without bound. However, the semiconductor crystal is full of objects with which the carriers collide and are scattered. These objects include the component atoms of the crystal, dopant ions, crystal defects, and even other electrons and holes. On a microscopic scale the carriers are constantly bouncing (scattering) off objects in the crystal, but generally moving in the direction prescribed

by the applied electric field. The net effect is that the carriers appear to move, on a macroscopic scale, at a constant velocity, v_d, the drift velocity. The drift velocity is directly proportional to the electric field. In a simple p/n junction the current density for electrons and holes is given by the sum of the drift and diffusion components as shown in Eqs (2.4) and (2.5) [23];

$$J_n = ne\mu_n E + eD_n \nabla_n \tag{2.4}$$

$$J_p = pe\mu_p E - eD_p \nabla_p \tag{2.5}$$

where E is the electric field, D_n and D_p are the diffusion coefficients, μ_n and μ_p are the mobility coefficients, and p, n are the hole and electron concentrations, respectively. The total current density is $J = J_n + J_p$. At thermodynamic equilibrium, using the Einstein relationship between diffusion coefficient and mobility; $D_n = (kT/e)\mu_n$, and the Boltzmann distribution for the electron concentration $n = n_i\, exp[(E_F\text{-}E_i)/kT]$, Eqs. 2.4 and 2.5 can be written as [24].

$$J_n = n\mu_n \nabla E_{Fn} \tag{2.6}$$

$$J_p = p\mu_p \nabla E_{Fp} \tag{2.7}$$

where E_{Fn} and E_{Fp} are the quasi-Fermi levels for electrons and holes. The governing equations for the charge transport are:

1- the Poisson equation for the electric field in the depletion region, Eq. (2.8).

$$\nabla E = \frac{\rho}{\varepsilon} = e\left(\frac{p - n + N_D^+ - N_A^-}{\varepsilon}\right) \tag{2.8}$$

where N_D^+ and N_A^- are the ionized donor and acceptor density, respectively and ε is the permittivity,

2- the continuity equation for electrons and holes which is the condition for charge conservation, Eqs. (2.9) and (2.10).

$$\frac{1}{e}\nabla \cdot J_n - \frac{\partial n}{\partial t} = -(G_n - R_n) \tag{2.9}$$

$$\frac{1}{e}\nabla \cdot J_p - \frac{\partial p}{\partial t} = G_p - R_p \qquad (2.10)$$

where, G_n and G_p are the generation rates for electrons and holes due to the external influences, as the applied voltage and the electromagnetic radiation, R_n and R_p are the recombination rates in the material. In an ideal diode the fundamental equations are solved using some common assumptions as; (i) the Boltzmann distribution for the occupation of the energy states of electrons holds true, (ii) the junction is abrupt, and also the depletion region boundaries, (iii) the semiconductor is neutral outside the charged region and (iv) the thermodynamic equilibrium applies all over the device. The total current (Shockley equation for an ideal diode [25] is given by Eq. (2.11).

$$J = J_o(e^{\frac{qv}{kt}} - 1) \qquad (2.11)$$

2.3.2 Solar cell output parameters

Three important parameters that are usually used to characterize solar cell outputs are the short-circuit current, I_{sc}, the open-circuit voltage, V_{oc}, and the fill factor, FF. The current-voltage J-V characteristic of an ideal cell can be written as the sum of the diode current density, Eq. 2.11 and the photogenerated current density;

$$J = J_o(e^{\frac{qv}{Akt}} - 1) - J_L \qquad (2.12)$$

where A is the ideality factor which takes into account the non-ideality of the diode ($1 < A < 2$, $A = 1$ for the Shockley equation). The short-circuit current, I_{sc}, under ideal conditions, is equal to the light-generated current I_L.

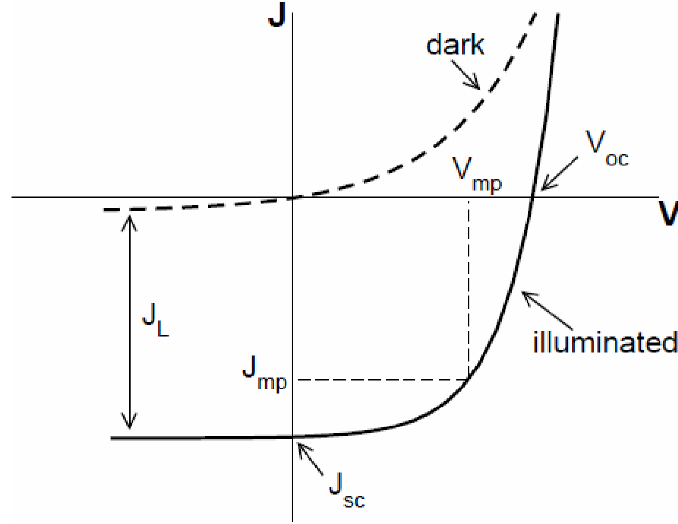


Fig. 2.5: J-V characteristics of a p/n junction in the dark conditions and under illumination [8].

An expression for an ideal value for the open-circuit voltage, V_{oc} , is obtained by setting the total current , J , to zero in equation (2.12) and then the following Eq (2.13) will result;

$$V_{oc} = \frac{AkT}{e} \ln \left(\frac{J_L}{J_o} + 1\right) \tag{2.13}$$

Another parameter used to evaluate the solar cell performance is the fill factor FF, which is a measure of the "squareness" of the J-V curve and defined as presented in Eq (2.14);

$$FF = \frac{V_{mp} I_{mp}}{V_{oc} I_{sc}} \tag{2.14}$$

The power output for any operating point on the I-V curve is computed from the area of the rectangle indicated in the fourth quadrant shown in Fig. 2.5. One particular operating point (V_{mp}, J_{mp}) will maximize this power output, where (V_{mp}) is the maximum power voltage J_{mp} is the maximum power current density. For cells of reasonably efficiency it has a value in the range of 0.7 to 0.85. The efficiency of the cell η is the maximum power divided by the input solar power and is given by Eq. (2.15) as;

$$\eta = \frac{V_{mp} I_{mp}}{P_{in}} \tag{2.15}$$

where P_{in} is the total power in the light incident upon the cell, and is given by:

$$p_{in} = A\int_{0}^{\infty} F(\lambda)(hc/\lambda)\,d\lambda \tag{2.16}$$

Here A is the device area, F(λ) is the number of photons per square centimeter per second per unit bandwidth incident on the device at wavelength λ , and hc/λ is the energy of each photon. Energy-conversion efficiencies of the commercial solar cells generally lie in the 12–14 % range. Other important figure of merits are the spectral response and the quantum efficiency of the solar cell. The spectral response is defined as the short circuit current divided by the input solar power as a function of wavelength and the quantum efficiency is defined as the number of collected charge carriers divided by the number of incident photons on the top of the cell. A full analysis and understanding of the solar cell device is completed considering the equivalent circuit for the device as shown in Figure 2.6.

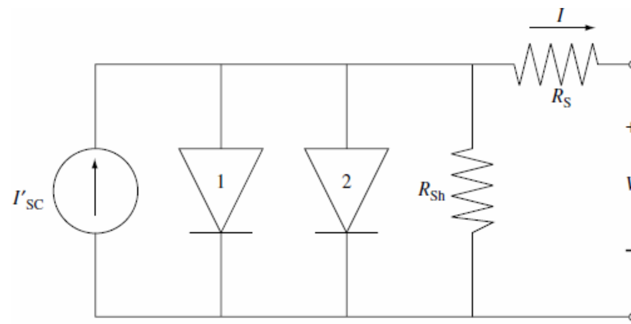


Fig. 2.6: Simple solar cell circuit model

It is apparent that a solar cell can be modeled by a current generator in parallel with two diodes – one with an ideality factor of “1” and the other with an ideality factor of “2” as shown in Figure 2.6. Diode 1 represents the recombination current in the quasi-neutral regions, while diode 2 represents recombination in the depletion region. In any real cell there are also a series resistance $R_s > 0$ and a parallel (shunt) resistance $R_{sh} < \infty$ which give some power losses. The series resistance R_s is related to the intrinsic resistivity of the materials used, the resistance of metallic contacts and interconnections, and the resistance of the metal/semiconductor junction. The parallel resistance R_{sh} is usually related to the shunt currents present in the junction driven by

defect states through the device. Both the effects of R_s and R_{sh} are visible in the cell fill factor and the J-V shape: high series resistance and low parallel resistance have an unfavorable effect on the cell fill factor [23]. For most of the deposited silicon films as (amorphous, microcrystalline silicon and/or nanocrystalline Si) by PECVD, the junction created between the silicon substrate and the reverse doped films is actually hetrerojunction due to the bandgap difference the substrate and the deposited material. So, in the next part we will define some general concepts related to heterojunctions.

2.3.3 Heterojunction (a-Si/c-Si) structure;

The band gap of *a*-Si: H is different than the bandgap of c-Si material and the *a*-Si/c-Si junction is actually a heterojunction. Intrinsic amorphous silicon/crystalline silicon (i)*a*-Si/c-Si heterojunction is normally considered as an abrupt classical heterojunction. Matsuura et al. [26] demonstrated that the Anderson's abrupt HJ model [27] without any interface states was valid for the intrinsic *a*-Si:H and (p) c-Si. A more accurate physical model was proposed by Rubineli et al. [28] a schematic diagram of energy band is shown in Figure. 2.7. In this work, the built-in potential, the distribution of the potential barrier between both semiconductors, the depletion widths, and the electric field at the interface have been evaluated in an (n) a-Si / (p) c-Si heterojunction. Unlike Matsuura et al., they considered a continuous density of states (DOS) (both U-shape and V-shape distributions) inside the bandgap of a-Si semiconductor [29]. Finally they showed that the U-shape model provided a better approximation for amorphous side of the junction.

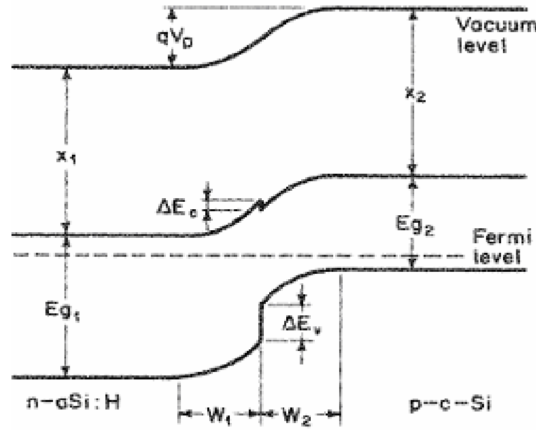


Fig. 2.7: Energy band diagram of amorphous-crystalline silicon heterojunction at equilibrium, proposed by Rubineli [28].

The effect of the interface states was taken into account in this work and its effect on the barrier potential, depletion widths in both amorphous and crystalline sides. Based on Rubineli's model, the presence of the interface states result in a shift in high frequency CV characteristics. This means that the Anderson's HJ model is not valid for the a-Si/c-Si heterostructure with significant interface states. However, a good interface with very low interface state densities can be constructed under highly controlled deposition conditions by PECVD systems [30]. Hence, the Anderson model, for a-Si/c-Si HJs can be used as an explanation tool for this structure. Many transport mechanisms have been proposed to introduce a satisfied explanation for the measured IV characteristics of a-Si:H /c-Si heterojunctions. Space Charge Limited Currents (SCLC) were proposed by Smid et al. [31] as the dominant mechanisms in a-Si:H/(p)c-Si diodes. Matsura et al has been proposed the Multi Tunneling Capture Emission (MTCE) mechanism for heterojunctions with undoped *a*-Si:H on (p) c-Si at low forward bias regime [26]. Mimura and Hatanaka proposed the MTCE model for the low forward bias IV behavior and the SCLC model for the high bias regime of the diode [32]. Jensen et al. [33] suggested that the recombination at the interface and the intrinsic region can explain the profile of the dark IV characteristics in a p-i-n HJs based on amorphous and crystalline silicon.

2.4 Processing Techniques for thin film technology

Various deposition techniques were used for the epitaxial growth of silicon at low temperatures (here T_{dep}<650°C). Based on the underlying physical processes during deposition, they can be divided into four different categories [34]: Chemical vapor deposition (CVD), physical vapor deposition (PVD), liquid phase epitaxy (LPE) [35] and solid phase epitaxy (SPE) [36]. The decomposition of a gaseous silicon source, such as SiH_4 is the basic principle of all CVD-processes.

2.4.1 Physical vapor deposition (PVD)

In PVD processes, elementary silicon is used for growth which is in PVD only dependent on the rate of silicon atoms or ions that impinge on the substrate surface. Molecular beam epitaxy (MBE), sputter deposition, ion-assisted deposition (IAD), or ion-beam deposition (IBD) are the most important PVD processes. MBE is the most commonly used one and to ensure that a high mean free path of the particles and to avoid contaminations from the gas phase, ultra high vacuum (UHV) conditions must be employed. A wide range of materials systems are grown epitaxially by MBE, e.g GaAs for optoelectronics. For sputter deposition processes, a Si-target is bombarded with an ion beam, e.g. Ar^+ ions. Silicon atoms and ions are sputtered from the target and reach eventually the substrate. Application of a substrate bias voltage or glow discharge plasma allows for control over additional deposition parameters, such as the ion energy in sputter processes. Ion-beam deposition (IBD) uses only Si-ions for film growth. Special ion beam sources allow for a precise control of the ion mass and energy. However, only low deposition rates of the order of 1Å/s are obtained by IBD due to the low effectively of the sources [37].

2.4.2 Chemical vapor deposition (CVD)

In the chemical vapor deposition, the decomposition usually is achieved by the thermal energy of the substrate. However, at low temperatures, a wide variety of excitation methods for the decomposition of the gases is in use, e.g. plasma enhanced CVD (PECVD), hot wire CVD

(HWCVD), and electron cyclotron resonance CVD (ECR-CVD). Growth processes in CVD include the formation of precursors, consisting of Si-radicals in the case of SiH_4 as source material. Subsequently, these precursors are physisorbed on the surface, followed by the chemisorptions of the silicon atom and the evaporation of the remaining hydrogen atoms. However, the surface reaction of the precursors is common to all CVD processes, unless they generate a high amount of Si-radicals that may be directly physisorbed. This surface reaction is thermally activated by the substrate temperature, and consequently, the deposition rate of CVD-reactions is limited by the substrate temperature [38].

2.4.3 Plasma Enhanced Chemical Vapor Deposition (PECVD)

Plasma Enhanced Chemical Vapor Deposition (PECVD) has become an established commercial technique for the deposition of a number of important materials, especially insulating films such as silicon nitride and silicon oxide [39]. The major advantage of PEVCD is its lower temperature capability compared to that of thermally driven CVD. For example, deposition temperatures of 700 to 900°C are required to deposit silicon nitride films by thermal CVD, whereas only 250 to 350°C is sufficient to deposit similar films by PECVD [39, 40]. This lower temperature capability is made possible by the addition of electrical energy to the CVD environment, and the effective substitution of this electrical energy for thermal energy. Applications of PECVD thin films and coatings range from electronics to optics and metallurgy. PECVD is used for low temperature (<350ºC) deposition of amorphous silicon (*a*-Si), nanocrystalline silicon (nc-Si), microcrystalline silicon and silicon nitride ($Si_x N_{1-x}$) thin films. PECVD is also investigated for the deposition of crystalline films for microelectronics, such as polycrystalline silicon [41-42].

Decomposition process of a gaseous silicon source, such as SiH_4, is the basic principle of all CVD-processes. In the simplest case, this decomposition is achieved by the thermal energy of the substrate, as we discussed in the previous section. This thermal CVD is a commonly used in semiconductor industry and results in high quality silicon films with acceptable high deposition

rates. However, at low temperatures, a wide variety of excitation methods for the decomposition of the gases is in use. Different kinds of PECVD techniques that are used for deposition of Si-based thin films are radio-frequency (RF) PECVD, direct current (DC) PECVD, and very high frequency VHF-PECVD, electron cyclotron resonance CVD (ECR-CVD). Among them, the 13.56 MHz (RF PECVD) is widely used in industrial scale. Figure 2.8 shows the schematic diagram of a typical RF PECVD reactor. The reactor comprises gas input lines, a chamber, gas output lines, and an RF generator. The parallel plates in the figure are separated by a certain distance in the reactor. One of the plates is grounded and the other one is connected to the RF generator by RF matching interfaces. The samples are placed on the ground electrode (bottom electrode), which is enabled by a heater for controlling the deposition temperature.

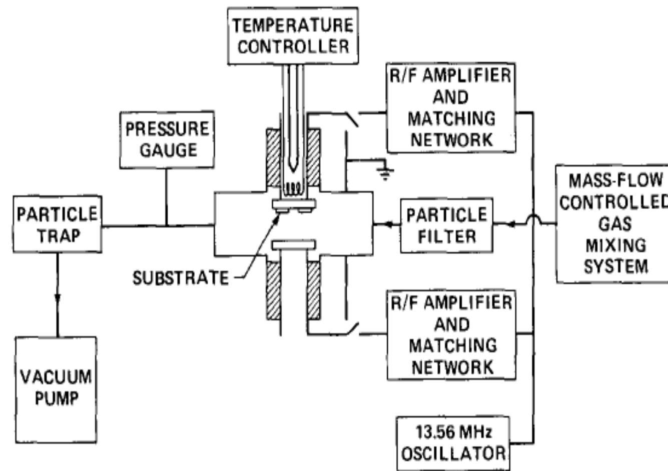


Fig. 2.8: Schematic diagram of a PECVD system [43].

This technique takes advantage of a high energy electrons present in glow discharges to dissociate and ionize gaseous molecules, thereby forming chemically active radicals and ions. Since thermal energy is not needed to break chemical bonds, a variety of film materials can be formed on temperature-sensitive substrates (e.g. polymers or low melting point metals). The plasma environment in PECVD performs two basic functions. First, reactive chemical species are generated by electron impact collisions, thereby overcoming kinetic limitations that may exist in CVD processes. Second, the discharge supplies energetic radiation, primarily positive ions, but

also neutral and metastable species, electrons, and photons, which bombard surfaces immersed in the plasma and thereby alter surface chemistry. Specifically, ion bombardment of growing film surfaces plays a key role in nucleation, growth kinetics, film composition, structure, and stress.

Plasma physics and chemistry in PECVD system

Plasmas can be generated by subjecting gases to very high temperatures or to strong electric or magnetic fields. In thermal plasmas, electrons, ions, and neutral species are in local thermodynamic equilibrium. In nonequilibrium or "cold" plasmas, the electrons and ions are more energetic than the neutral species. Most of the glow discharges used for thin film plasma deposition is created by subjecting the gas to a radio-frequency (rf) electric field; they are nonequilibrium glow discharge plasmas. The electric field initially reacts mostly with the free electrons present in the gas. While the electric field also interacts with ions, these species initially remain relatively unaffected because of their much heavier mass. The accelerated electrons do not lose much energy in elastic collisions with gas species because of the large mass difference. In addition, these electrons do not lose much energy in inelastic collisions, such as excitation and ionization, unless their energies are higher than the relevant threshold energies (e.g., 11.56 eV for excitation and 15.8 eV for ionization in the case of argon [44]. Inelastic collisions between high-energy electrons and gas species generate highly reactive species, such as excited neutrals and free radicals, as well as ions and more electrons. By this mechanism, the energy of the electrons creates reactive and charged species without substantially increasing the gas temperature. The potential in the central region, or bulk plasma, is slightly positive with respect to the electrodes, due to the small surplus of positive ions. The plasma potential is the maximum value with which ions can be accelerated from the edge of the sheath towards the substrate, located at the grounded electrode. This may cause ion bombardment that may induce ion-surface interactions such as enhancement of adatom diffusion, displacement of surface atoms, trapping or sticking of incident ions, sputtering, and implantation. The bulk plasma is characterized by a constant potential. Electrons are expelled from the sheaths, so all ionization and dissociation processes must occur in

the plasma bulk. Plasma light as a result emission from excited molecules is only present from the plasma bulk, the sheaths are dark. The reactive species that are generated in the plasma have lower energy barriers to physical and chemical reactions than the parent species, and consequently can react at lower temperatures. The positive ions and the radicals reach the substrate by drift and diffusion, respectively, and undergo surface and subsurface reactions during deposition. In PECVD, these reactive species are utilized to form thin films at temperatures lower than those possible with thermally activated CVD. The charged species in the glow discharge may also affect the properties of the deposited films [45].

Role of ions

Ion bombardment is either beneficial or has an adverse effect, depending on the deposition conditions. It is reported that ions can contribute up to 70% of the growth in PECVD deposition of microcrystalline silicon [46]. Suppression of the ion energy is effective in improving the crystallinity, particularly at high growth rates. The ion energy depends on gas pressure, exciting frequency and the electrode configuration. The ion density in the plasma is determined by the electron density, whereas the kinetic energy of the ions is determined by the electron temperature. High excitation frequencies result in a greater electron density and a lower electron temperature [47]. The average electron energy decreases with increasing frequency [48]. In a diode type reactor, the frequency of the plasma excitation source has a direct correlation with the ion energy. Radicals are considered to be the main precursors for the growth of both amorphous and microcrystalline silicon in a PECVD deposition process. It is agreed from many reports that SiH_3 is the main precursor for the device quality films. Low lifetime radicals, higher silane radicals (Si_2H_5, Si_3 H_8, etc.) and reactive radicals (SiH_2, SiH, etc.) are considered a hindrance to microcrystalline deposition. However, it is mainly the ions which determine the final film quality. The ion flux density reaching the substrate is determined by the ion density in the plasma (electron density), whereas the kinetic energy of individual ions reaching the substrate is determined by the electron temperature in the plasma. In fact, it has been shown that with the

same type of plasma it is only the presence or non-presence of ions (at the growing film), which determines whether it is amorphous or microcrystalline. However, it has to be emphasized that the presence of ions is not as bad an effect as their energy [49] in a high ion flux in the high-frequency case would give rise to enhanced surface diffusion of impinging species, even at a low substrate temperature (T_s), which is a necessary condition for good crystallinity. One of the methods for varying the ion bombardment is to choose the frequency of the power source generating the plasma. An earlier report [49] in the case of VHF PECVD explained high crystallinity in the VHF process compared to 13.56MHz samples as due to the presence of high-energy ions in the latter case. This model is based on the criterion that the energy of the impinging particles on the growth surface must not exceed the threshold energy of defect formation. The plasma contains both silicon and hydrogen ions, but the effect of the latter is considered negligible. The peak of the ion energy distribution is a function of excitation frequency. As a result, the peak ion energies for excitation at 70MHz or higher frequencies are around 14 eV, which is lower than the threshold energy of 16 eV for Si impact. In contrast to this, for the case of 13.56MHz excitation, the peak of the ion energy value is around 45 eV. Another way of controlling ions which has been proposed is to use deuterium instead of hydrogen dilution. In PECVD, this has shown to improve the crystallinity and decrease the defect density. The reason suggested is that deuterium dilution leads to lower ion bombardment, due to a lower electron temperature in the plasma formed. This is attributed to the heavier mass of deuterium, which results in a lower electron loss rate [50].

The second method to manipulate the ion bombardment at the growing surface is through the design of the electrode configuration. An attempt to grow microcrystalline films by suppressing ions from reaching the substrate surface has shown promising results, as proposed by Veprek et al. [51]. A triode technique, in which there is a negatively biased mesh electrode between the plasma and the substrate, as proposed by Matsuda [52], is very effective. The effect of ion bombardment on the deposition is best observed in the case of the electron cyclotron resonance

(ECR) CVD process. Here, due to remote deposition, the ion energy and flux at the substrate can be independently modified without affecting the plasma. De Boer et al. [53] using the ECR process, observed that even when growing crystalline Si epitaxial layers on Si wafers, high ion bombardment (increasing bias voltage) led to an increase in the Raman line width and a decrease in the electron mobility in the film. Nozawa et al. [54] observed in the case of ECR CVD that increasing the positive DC bias to the substrate improved the crystallinity. This was attributed to a decrease in the ion flux to the substrate.

Epitaxy Growth modes in PVD process

Atoms impinging on the substrate surface are adsorbed and then they migrate on the surface as so called adatoms (or addimers). At substrate temperatures Ts>800°C no desorption of the adatoms occurs, i.e. the sticking probability is close to one and all atoms remain on the substrate [55]. Incorporation of the adatoms occurs at kinks in step edges due to the high coordination of these sites. In physical vapor deposition processes, growth is dominated by the adatom mobility and the deposition rate, i.e. the number of atoms impinging on the surface per time unit. These two factors determine the mean free path time of the adatom before it reaches either a surface step, where it is attached and migrate to a kink, or collides with other adatoms and forms a cluster which may result in the nucleation of a new terrace on the surface. The potential energy of the adatoms determines the migration and incorporation probabilities. The most favorable site for incorporation of an adatom on the lower terrace is a kink in the step edge. Here the potential energy shows a minimum, as the atom has the most neighbors satisfying dangling bonds. At low deposition temperatures three different growth modes are distinguished in homoepitaxial growth as illustrated in Figure 2.9 [56]; i) island growth ii) layer by layer growth and (iii) step flow growth , these modes are temperature dependent.

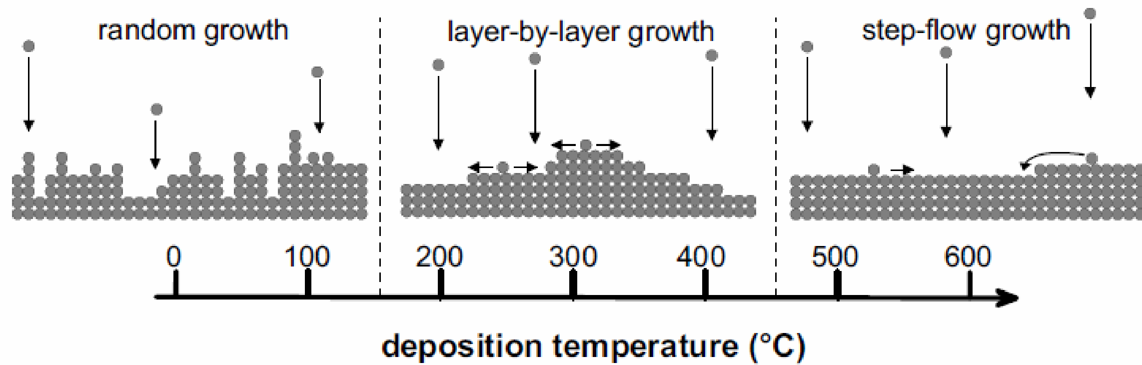


Fig. 2.9: Growth modes [56].

2.5 A new route to epitaxy growth at low temperature by PECVD

2.5.1 PECVD Hydrogenated amorphous silicon

The beneficial of hydrogenated amorphous silicon for device application was appeared after successfully deposited using SiH_4 plasma in 1969 [57]. It was confirmed that glow discharge *a*-Si:H has low density of states (DOS) in the gap compared to sputtered or evaporated *a* Si [58]. The reduction in DOS in the gap is now understood by the fact that hydrogen from SiH_4 decompostion passivates most of the unsaturated Si dangling bonds, thereby reducing the defect density in the band gap. The deposition process in PECVD is based on electron impact dissociation of a process gas such as silane in plasma. Low-pressure weakly ionized plasma created between two electrodes contains positive, negative and neutral species (radicals). The powered electrode is called the cathode and the grounded anode electrode is where the substrate is attached for deposition. As the substrate and electrodes are slightly negative with respect to the plasma bulk, negative ions are trapped in the plasma. Under high-pressure conditions, this creates dust by reacting with the silane. The positive ions and the radicals reach the substrate by drift and diffusion, respectively, and undergo surface and subsurface reactions during deposition. Although there are many reactions leading to the dissociation, the most important reactions with low energy is [29]

$$e^{-}+SiH_4 \Rightarrow SiH_3+H+e^{-} \rightarrow 4.0\ ev \quad (2.17)$$

The resulting radicals and ions collide with each other and with SiH_4 during their transport to the substrate leading to more complex species due to the secondary reactions. Primary reactions are SiH_3 producing which has the longest lifetime and highest density, thereby controlling the final material properties. Neutral radical diffuse on to the surface, adsorbed migrate and/or chemisorptions to form *a*-Si:H film. Contrary to monocrystalline silicon (c-Si), the absence of long-range order in *a*-Si:H causes a relaxation in the transition rules, so that it behaves as a direct gap semiconductor with a band gap between 1.6 and 1.8 eV. Where, in the crystalline structure, silicon atoms occupy specified locations with a uniform bond length and angle, while in the amorphous case, there are missing atoms and slight variation in bond length and angle as shown in Figure 2.10.

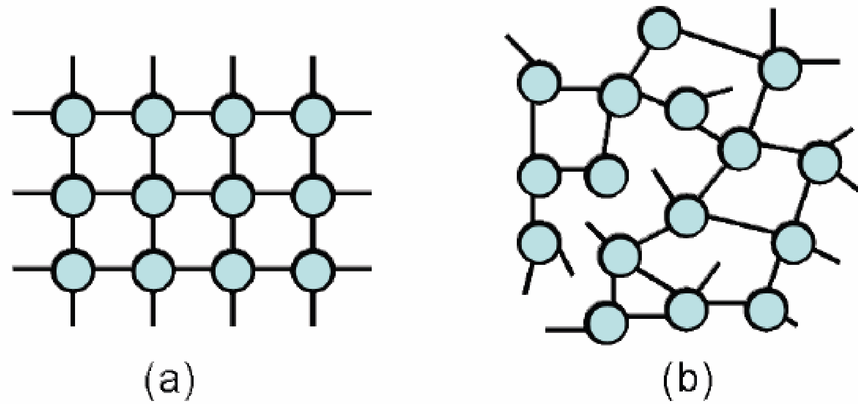


Fig. 2.10: Two dimensional representation of atomic bonding in (a) crystalline silicon and (b) a-Si:H adapted from [29]

This behaviour results in a much larger absorption in the solar spectrum range, so much less material is needed to collect the same amount of incoming light. Hence, active (intrinsic) layer thicknesses below 0.5 μm are commonly used in *a*-Si:H solar cells. Regarding the above mentioned gap, it must be taken into account that this term can not be understood in the same way as when dealing with c-Si, where no electronic states can be found between the valence and conduction bands. A significant density of electronic states, which limit the

mobility of photogenerated carriers, can be observed in *a*-Si:H in the so-called band gap, thus giving place to the commonly used expression mobility gap instead of band gap. The mobility gap is defined as the energy range between the mobility edge in the conduction band E_c and that in the valence band E_v. The Fermi energy is located just above the mid-gap which means that *a*-Si:H is slightly n-type Two different mechanisms account for the presence of electronic states in the mobility gap. On one hand, the lack of order in the material causes a broadening of the valence and conduction bands leading to band tails, where localized energy states exist. On the other hand, unpassivated dangling bonds give rise to defect states near the centre of the band gap as also seen in *a*-Si [29]. The band-tails states and the deep states are localized states where carriers are usually confined. A schematic diagram of the a-Si:H density of states (DOS) can be observed in Figure 2.11.

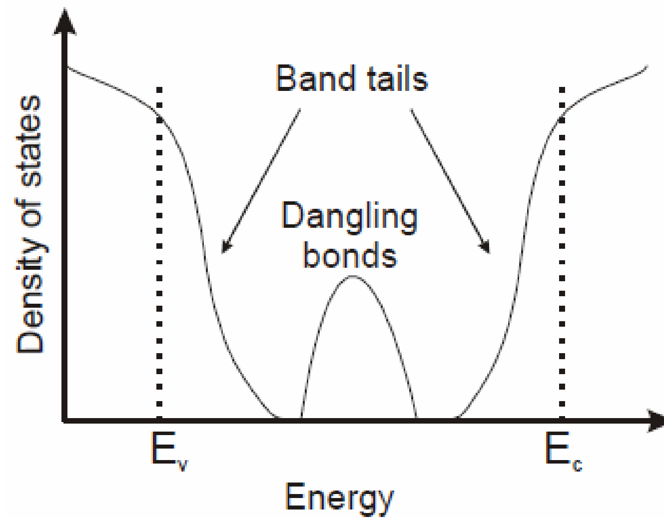


Fig. 2.11: Schematic representation of the density of states (DOS) in *a*-Si:H, E_v and E_c are the mobility edges of the valnce and conduction band, respectively adapted from [29].

The above-mentioned density of states in the band gap results in the low mobility of the carriers in *a*-Si:H due to the significant recombination probability. As a result, drift current drives thin film solar cells whereas the performance of bulk solar cells relies on diffusion current [59]. Drift current requires an intense internal electric field, so that carriers photogenerated in the intrinsic

layer can be effectively collected. Unfortunately, this electric field is also degraded by the defect states in the centre of the mobility gap, thus influencing the device performance. This is related to a very critical phenomenon to *a*-Si:H since first studies were reported by Staebler and Wronski [60]. This effect consists in the worsening of the material properties after prolonged light exposure due to the creation of metastable defects. Such defects act as recombination centers and degrade the internal electric field, so that collection is hindered and drift current is therefore reduced. The microscopic mechanism behind this degradation has not been fully clarified yet, though different models have been proposed over the years [60-67]. Anyway, hydrogen has been accepted to play a very important role, as high hydrogen content promotes the degradation of the samples. Hence, samples exhibiting low hydrogen content experience weaker degradation after light exposure [64], On the other hand, the use of thinner intrinsic layers in solar cells leads to lower collection distances and more intense electric fields, so they can partially compensate the degradation process after illumination. Unfortunately, the intrinsic layer must be thick enough to absorb an important fraction of the incoming light in order to create electron-hole pairs, so a compromise between light absorption and carrier collection must be reached. Commercial cells have to be designed around the 'stabilized' quality of the material after light exposure, rather than the initial 'as-deposited' quality. Laboratory devices can be designed around the latter, however, giving a large difference in performance between the best 'unstabilised' laboratory devices and what can be produced commercially, leading to relatively low efficiencies of the commercial single-junction amorphous silicon cells. Nevertheless, and despite the satisfactory performance of solar cells obtained by PECVD, some drawbacks arise from its use especially degradation after light soaking as mentioned earlier, are typically required to deposit PECVD device-quality material.

2.5.2 Microcrystalline silicon

In recent years, microcrystalline silicon (μc-Si:H) has been successfully produced by PECVD using hydrogen-diluted Si precursor gases such as SiH_4, Si_2H_6 and SiF_4. Microcrystalline Si has been widely applied as the window layer for *a*-Si:H solar cells and for c-Si-based heterojunction solar cells. The recent popularity of microcrystalline silicon (μc-Si:H) began with the first successful applications of this material as an absorber layer in thin film solar cells [68-70] and, most importantly, when it was reported [67] that such solar cells did not suffer from the notorious light-induced degradation, known as the Staebler–Wronski effect (SWE),which is observed in amorphous silicon [60] as discussed in the previous section. Considerable progress has been made since then concerning the fabrication of μc-Si:H material and solar cells and the improvement of device quality. Microcrystalline silicon is a mixture of various amounts of different structural components; crystalline grains, amorphous or disordered regions including grain boundaries and voids as shown in Figure 2.12 [68].

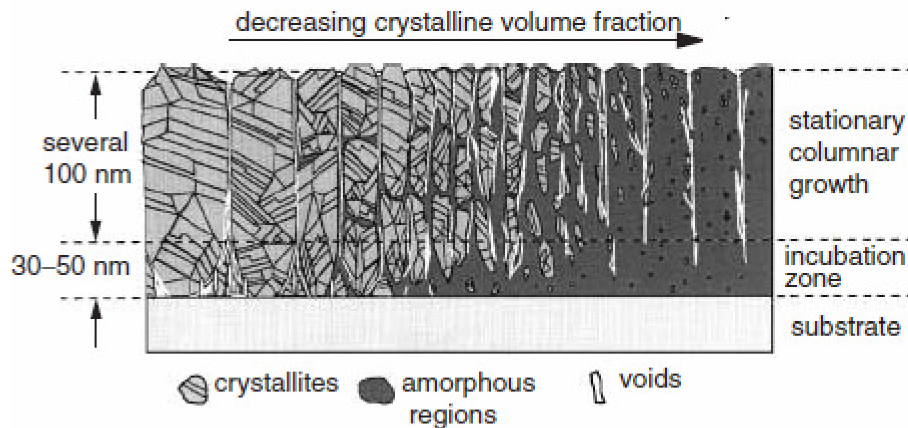


Fig.2.12: Schematic diagram showing the prominent microstructure features of μc-Si:H, from left to right the film composition changes from highly crystalline to predominantly amorphous [68].

In addition, structural inhomogeneity along the growth axis and a very critical substrate dependence of the nucleation process is observed. These material properties and the resulting

devices were investigated in great detail and it soon became clear that under certain conditions in the material preparation process, or with respect to the material itself, instability or metastability phenomena may also occur in μc-Si:H and may affect solar cell efficiency. Structural investigations on optimised solar cells showed very little to no amorphous components in material grown by PECVD [75, 76]. The investigations are complicated by the substrate dependence of growth, which results in different structures for material grown on glass or Si wafers and material grown in solar cells on highly crystalline contact layers. In any case, the presence of an amorphous phase could result in light induced metastability, which has now been confirmed [70]. A second point of concern is related to the porosity in μc-Si:H, in particular in material with a high crystalline volume fraction. Also attempts to grow material with large grain size, usually at higher deposition temperatures in order to improve carrier mobility, frequently result in porous material with poor grain boundary passivation. The temperature and the silane/hydrogen mixture are found to be the most critical deposition parameters to determine the structure and the electronic properties. The instabilities and metastabilities of the porous structure of the highly crystalline material on the one hand, and amorphous inclusions in 'threshold' material on the other, encourage to explore new high quality materials (in terms of structure and electronic point of view) under low temperature process and affordable for industrial mass production.

2.5.3 Epitaxy growth using PECVD

Low-temperature Si epitaxy is of broad scientific and technological interest. It is required for fabrication of nanoscale junctions and shows promise for producing highly strained heterojunctions. The growth of epitaxial silicon films at low substrate temperatures has been an issue of interest for the past two decades. Low temperatures are needed in order to suppress bulk diffusion and surface segregation of dopants, as well as dislocation introduction and propagation

in the case of strained layers. Very low-temperature epitaxial growth is possible within certain limits by molecular beam epitaxy (MBE) [71]. Processing temperatures could also be reduced in chemical vapor deposition (CVD) to 650 °C by lowering the gas pressures from atmospheric pressures into the mbar regime ~low-pressure chemical vapor deposition, (LPCVD) [72]. Alternatively, substrate temperatures can be as low as 550°C in atmospheric pressure CVD under ultraclean conditions [73]. The use of an UHV system and reactive gas pressures in the 10^{-3} mbar range in a technique called UHV-CVD allowed a further reduction of substrate temperatures to below 550 °C [74]. So far, a few studies have shown the application of LT epitaxial Si layers to solar cells. Centurioni et al. [75] applied very thin Si epitaxial like film to p^+ emitters and intrinsic thin buffer layers on n-type c-Si substrates and discussed the passivating properties of epitaxial buffer layers. These epitaxial layers were deposited by very high-frequency plasma-enhanced chemical vapour deposition (VHF-PECVD). Lips et al. [76] reported the application of doped and undoped epitaxial Si layers to c-Si solar cells. They adopted electron-cycle-resonance chemical vapour deposition (ECR-CVD) to prepare epitaxial Si layers, and the substrate temperatures were more than 300°C. There is a need to develop epitaxial highly doped films (phosphorous or boron) to tackle the degradation issue on one hand and boost the efficiency of the conventional solar cells on the other hand.

2.6 Rapid Thermal annealing process

However, we are targeting high quality (phosphorous and boron doped) doped epitaxy silicon emitters for high efficiency solar cells at low temperature using PECVD system. We used rapid thermal annealing process RTP to activate the dopants, especially for boron dopant in Si films. The most general definition of RTP is a tool enabling rapid thermal cycles which cannot be performed with conventional quartz tube furnaces. In particular, conventional furnace processing restricts the maximum heating and cooling rates to several °C/min and the minimum process time to several minutes. These restrictions are imposed by the high thermal mass of the system as well

as the way the energy is transferred to the wafers. In contrast, RTP offers the possibility to apply heating and cooling rates up to several hundred ^{o}C/s and to conduct processes in the range of 10^{-8} to 10^{1} s [77]. This can be achieved because each wafer is heated individually and uniformly. Naturally, RTP tools have to make use of a fast method of transferring energy to and away from the wafer. Hence, energy sources based on radiation are used as lasers, electron and ion beams, and incoherent light from arc and tungsten halogen lamps [78]. In this study a single-wafer RTP reactor shown in Figure. 2.13 is used to activate the dopants in the developed silicon films, especially for the boron doped films. The wafer rests on three small quartz pins which in turn are mounted on a quartz tray. The tray is pushed into and pulled out of the quartz chamber manually. The wafer is heated from both sides by tungsten halogen lamps of 1.5 kW electrical power each, in nitrogen ambient with controlled mass flow rate. The process gas flows into the chamber through the gas inlet at the back where it encounters distribution plates leading to a laminar gas flow. The position of the upper lamps is shifted with respect to the lower lamps in a way to yield a homogeneous field of irradiation. Each wafer are divided into four equal pieces to be sure that the films have the same deposition conditions and annealed using different conditions. The chamber is surrounded by water-cooled walls.

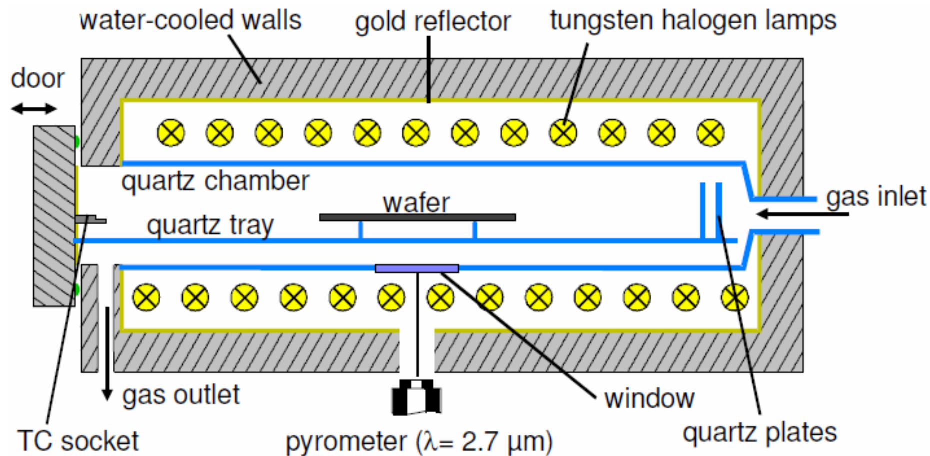


Fig. 2.13: Schematic diagram of a cross section through the single-wafer RTP reactor (adapted from) [79]

The wafer temperature can be measured by means of a pyrometer with a working wavelength of 2.7 μm. It looks at the wafer through a quartz window and measures the intensity of the light emitted by the wafer. For temperature measurement accuracy, in contrast to the rest of the quartz chamber, the window is not made of hydroxylated quartz and hence transparent for light at the working wavelength of the pyrometer. This arrangement ensures that light from the lamps does not disturb the pyrometer signal. The temperature of the annealed pieces is measured by highly sensitive thermocouple attached to the unpolished back side of the silicon wafer pieces.

2.7 Issues related to annealing process: Hydrogen effusion process

Hydrogen atoms play a very important role in reducing the density of dangling bonds in hydrogenated amorphous silicon *a*-Si:H and enhance the electrical properties of the growth silicon films through high crystallinity films. Where, we are using the rapid thermal annealing process, hence, the hydrogen effusion should be studied in detail. There are two peaks for hydrogen evolution from silicon films for the films deposited at different substrate temperatures as shown in Figure 2.14 [80].

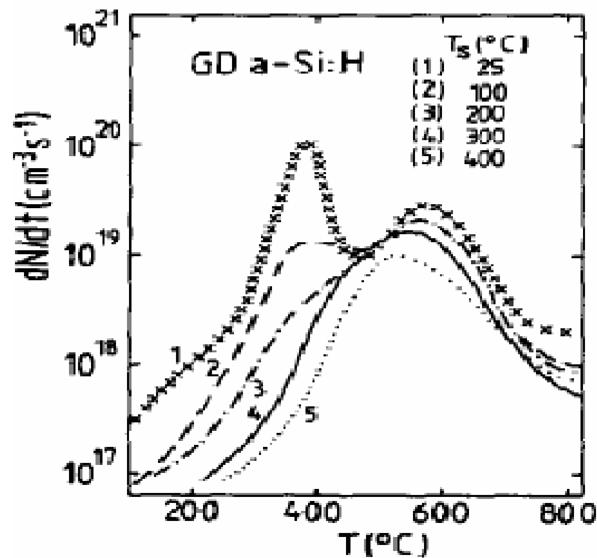


Fig. 2.14: Hydrogen evolution rate versus temperature for undoped GD *a*-Si:H films, film thickness ~ 0.6 μm [80].

The high temperature peak is considered to be limited by the diffusion of hydrogen atoms in the bulk of the sample [81]. Since practically all hydrogen is bonded to silicon according to infrared absorption and Raman scattering measurements [82] a considerable reconstruction of Si-Si bonds must take place. So, most of the hydrogen in *a*-Si: H is incorporated at positions breaking Si-Si bonds and that diffusion proceeds via breaking and reconstructing of silicon bonds. If the Si-Si and Si-H binding energies are both approximately 3 eV, the 1.5 eV diffusion energy is easily explained by the energy step for the release of atomic hydrogen. The actual diffusion would be a fast interstitial process similar to hydrogen diffusion in crystalline silicon [83] This mechanism would not lead to the production of dangling bonds. Only at high temperatures, when most of the diffusing hydrogen has been released, dangling bonds will be formed if isolated Si-H bonds are broken without Si-Si reconstruction.

2.8 Device structure

2.8.1 Crystalline silicon: passivated emitter, rear locally-diffused (PERL) structure

Highest efficiencies are achieved with a 400-µm single-crystal float zone (FZ-Si) material , which in addition to extreme crystalline perfection shows the lowest contamination levels of both metallic and light (O, C, N) impurities. This translates into the longest post-processing lifetimes in the millisecond range. Figure 2.15 shows the passivated emitter, rear locally-diffused (PERL) cell with a double layer and-reflection coating [84]. Passivated emitter and rear locally diffused (PERL) cells were reported to improve when going from 280- to 400-µm thickness because of a (relatively) high rear surface recombination and nonideal light-trapping [84]. Very high diffusion steps temperature (>1000°C) are involved, combined with double antireflection coating and, rear locally diffused high-low junction. A total of 6 to 8 photo masking steps are required for the cell

processing which lead to a very complicated process in industrial point of view. In consequence the idealised efficiency of about 25% indicated for silicon in Figure 2.15 is not realisable in practice the very best silicon cell, is fabricated as a technical exercise rather than as a production device. Hence, a low temperature and simple fabrication processing steps actually needed to afford a final competitive product in energy market in terms of low cost, simplicity and affordable for mass production.

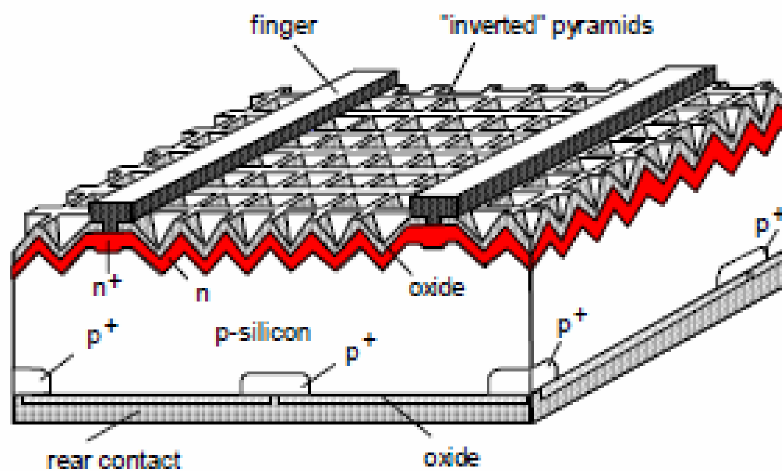


Fig. 2.15: Passivated emitter, rear locally-diffused (PERL) cell with a double layer and-reflection coating [84].

2.8.2 Thin film silicon solar cells

Some useful and practical approaches appeared towards simple and processed at low temperature < 350°C are investigated in the lab and in module production. Since 1994, encouraging cell efficiencies have been reported for μc-Si thin-film solar cells deposited on glass by Kaneka and the University of Neuchatel. Yamamoto et al. [85] obtained an efficiency of 10.7% for an n–i–p cell in a configuration called a second-generation ''STAR'' (naturally Surface Texture and enhanced Absorption with back Reflector) structure. Figure 2.16 shows a schematic view of Kaneka's new thin-film poly-Si solar cell with STAR (naturally Surface Texture and enhanced Absorption with back Reflector [86]. The first generation poly Si STAR cells were in the configuration glass/back reflector/n-layer/i-poly Si/p-layer/surface texture/ITO/Ag gridline,

whereas the second-generation cells employed texture at the back reflector. The i-layer (grown at ~550°C) was deposited by PECVD. Though the i-layer was meant to be intrinsic (without intentional doping), actually it was slightly n-type (phosphorus content of 5x10^{15} at/cm^{3}) and the incorporation of oxygen impurities was also assumed. Quantum efficiency (QE) of 60% at 800nm explains the beneficial effect of good light trapping. It was shown that the carrier concentration and thickness of the i-layer sensitively affects the V_{oc}; and that a higher V_{oc} is achieved with a higher carrier concentration (achieved by phosphorus in the i-layer). In a later development [86]. Kaneka Co. has tried a p–i–n superstrate configuration, for which a low temperature approach was used. However, the performance of an n–i–p poly Si cell is better in single-junction cells, because of the wider process windows for forming both back reflectors and each layer of the Si film.

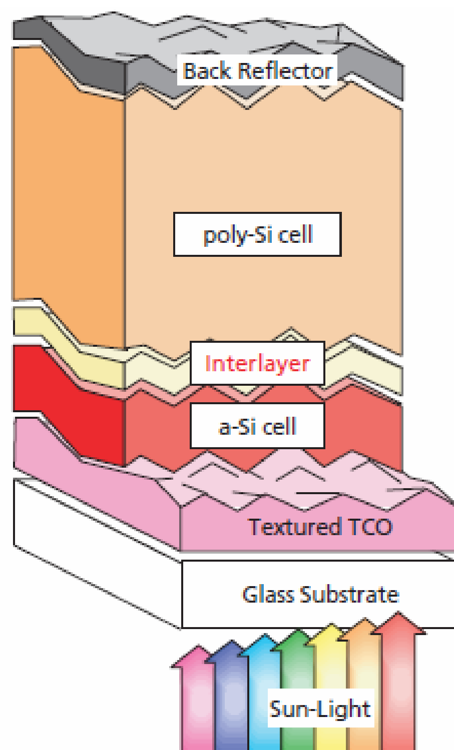


Fig. 2.16: Schematic view of Kaneka's new thin-film poly-Si solar cell with STAR (naturally Surface Texture and enhanced Absorption with back, Reflector adapted from [86].

Enhancing on the previous STAR structure, Sanyo developed a Heterojunction a-Si/c-Si structure with intrinsic thin layer (HIT) of efficiency 21.0% [87]. This structure features a very thin intrinsic a-Si layer inserted between p-type a-Si and n-type c-Si. Figure 2.17 shows the structure of the HIT cell. The *pn* junction is realized by the deposition of non doped a-Si and p-type a-Si layers on an n-type c-Si substrate with a PECVD system. On the bottom side the Back Surface Field (BSF) structure is used with non-doped a-Si and n-type a-Si layers. Since the conductivity of even heavily doped amorphous silicon is quite low, due to poor carrier mobility, transparent conducting oxides are required on both front and rear surfaces to allow lateral carrier transport to metal contacts screen-printed on both surfaces. However, the HIT structure is composed of at least eight thin layers which may influence the deposited film quality, especially at the interfaces, and hence affect on the efffciency of the fabricated devices.

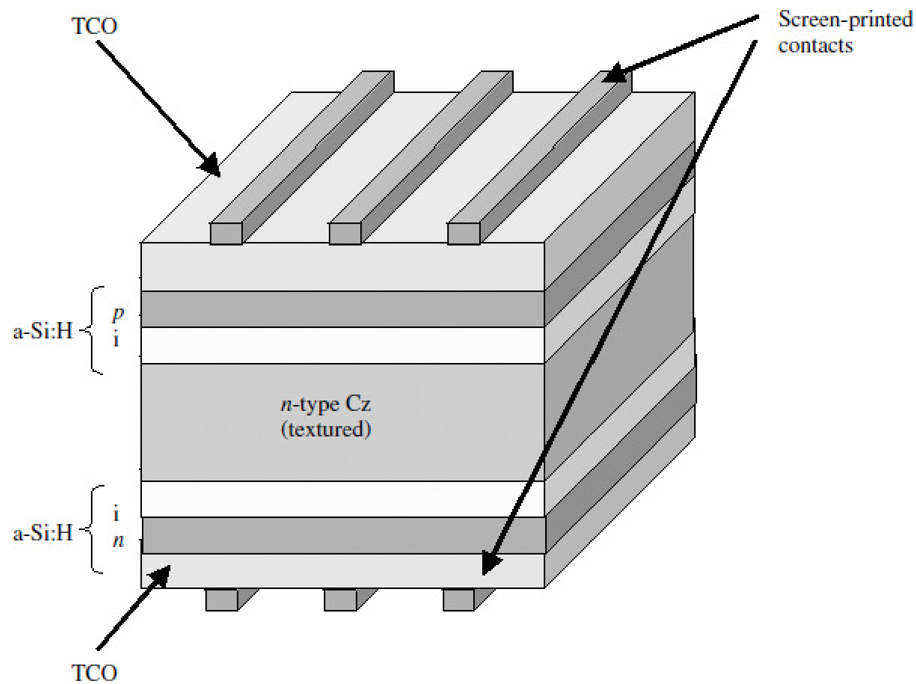


Fig. 2.17: The structure of the HIT cell [87].

2.9 Structural and Material Characterization:

2.9.1 High resolution transmission Electron microscope (HRTEM)

The investigation of multilayered thin films requires specialized experimental techniques that must cover a wide range of properties, both chemical and physical, and with very high spatial resolution. In a typical experiment, it is important to ascertain combination of the following parameters: layer thickness, crystallographic orientation in and out of the plane of the films, short- or long-range order, epitaxy with the substrate and other layers, grain size and orientation, physical roughness, chemical interdiffusion, and atomic-scale structure and defects. In addition, it may even be necessary to know the oxidation state and bonding environment of the individual atoms. Neutrons, photons, and electrons are all capable of obtaining much of the a aforementioned information, but TEM is unique in its ability to combine real- and reciprocal-space information from the same spatial location and at very high resolution. Electrons interact more strongly with matter than do neutrons or photons and can readily lose energy in the interaction. This means that, like neutrons and photons, electrons are sensitive not only to structure but also to chemistry such as local bonding environment and oxidation state. However, the real strength of electrons is that they can be focused into a much finer probe and can therefore provide such chemical information on a finer local scale.

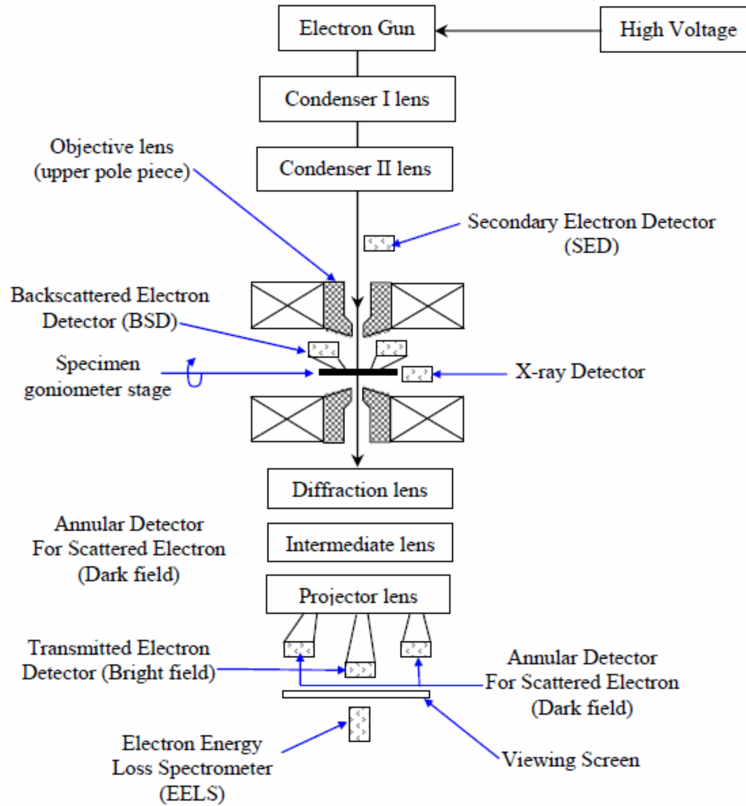


Fig. 2.18: Schematic diagram of TEM, adapted from [88].

A schematic diagram of a typical TEM is shown in Fig. 3.18 [88]. In a conventional TEM, electrons are emitted from an electron gun and are focused by a condenser lens to form a beam, which illuminates the specimen. The electron beam interacts with the specimen and is scattered or diffracted by the crystal atoms. The electron wave at the exit face of the specimen, thus, contains information about the potential distribution in the specimen. A modern TEM may have the capability of imaging the variations in the diffraction across the specimen (diffraction contrast imaging), imaging the phase contrast of the specimen (high-resolution imaging), obtaining diffraction patterns from selected areas of the specimen, and electron energy loss spectroscopy (EELS) measurements with a small, focused electron beam. The three primary imaging modes are bright-field, dark-filed, and high- resolution microscopy. An HRTEM image is formed in the image plane (as opposed to the back focal plane, which contains reciprocal-space information, i.e., the diffraction pattern) when two or more Bragg reflected beams, selected by a suitably large

objective aperture, interact (interfere) to form an image. Because the contrast arises from the difference in phase of the beams as a result of their interaction with the specimen, HREM imaging is a type of phase-contrast imaging and can be used to resolve the crystalline lattice, columns of atoms, or, in the case of the most modern aberration corrected transmission electron microscopes, sub-angstrom imaging of the lattice [89] and even single atoms [90]. Nevertheless, the HRTEM can be used in the analysis of the chemical composition of the prepared specimens through Energy-Filtered TEM (EFTEM) /Electron Energy Loss Spectroscopy (EELS). Where, in their interaction with a specimen, electrons scatter both elastically and inelastically. Elastically scattered electrons are the primary basis for imaging and diffraction in the TEM, whereas inelastically scattered electrons are the basis for EELS and EFTEM. The energy spread of inelastically scattered electrons in a TEM experiment carries a wealth of chemical information on the electronic structure of the specimen, including both localized core levels as well as the outermost delocalized atomic orbitals. When an incident electron interacts with the specimen and loses a small amount of energy (typically <50 eV), it can reveal specifics such as the thickness of the specimen, valence-electron density, and surface and interface states through analysis of the plasmon losses. In addition, the high-loss region of the EELS spectrum (typically 50–1000 eV) can be used to analyze the atom type through analysis of characteristic ionization edge energies, elemental concentration and distribution from the integrated intensity of the edge, the chemical state, local structure, coordination, and bonding through analysis of the shape of the near-edge structure; and bond distances through the analysis of the extended energy loss fine structure [91]. The combination of high spatial resolution and high energy resolution of EELS in a TEM is unique, and state-of-the-art aberration-corrected transmission electron microscopes have recently been used for single-atom spectroscopy [89].

Specimen Preparation for HRTEM

The main tool for the structure analysis for our developed films will be HRTEM micrographs, so it is beneficial to describe the specimen preparation for TEM images as well. Specimen preparation is an important aspect of the transmission electron microscopy (TEM) analysis of electronic materials. Specimen preparation techniques are very material dependent, therefore, it is important to initially select the technique that is most beneficial for the individual specimen. Electropolishing is a time-proven technology for the preparation of most metallic specimens and is also applicable to preparing high-T_c superconductors. For most electronic materials, a common sequence of preparation techniques is ultrasonic disk cutting, dimpling, and ion-milling. A critical aspect of preparing a specimen from the bulk state to a 3 mm disk is the ability to rapidly capture the specific area of interest and to preserve it in an unaltered state. When the analysis of an interface is required, it is beneficial to obtain a disk whereby an interface is situated near the disk's center. Three main steps are applied to prepare the sample for TEM analysis. (i) Grinding, a thinning process for the thicker samples down to ~150-200 µm, (ii) Dimpling is a preparation technique that produces a specimen with a thinned central area and an outer rim of sufficient thickness to permit ease of handling. This specimen configuration is achieved by the simultaneous rotation of both the specimen and a grinding wheel containing abrasive slurry (typically diamond) whose axes are orthogonal and intersecting. Advancements in process control have greatly increased the capabilities and performance of the dimpling process, (iii) Ion milling is traditionally the final form of specimen preparation. In this process, charged argon ions are accelerated to the specimen surface by the application of high voltage. The ion impingement upon the specimen surface removes material as a result of momentum transfer. In our analysis two different UHRTEM systems with different capabilities are used to study the developed structures at the atomic scale in terms of bulk, orientations and interface. UHRTEM Titan II 80-300 and JEOL 2010F (operated at 200kV and capable of point resolution of 1.4Å.) were used to

analysis and observe the developed specimens in nanoscale regime. Specimens were prepared by grinding and polishing techniques up to a thickness of 20 μm followed by a final thinning to electron transparency using an ion mill with Ar+ beam at 5o and 5 kV.

2.9.2 Micro-Raman Spectroscopy

Raman spectroscopy is another vibrational spectroscopic technique that can detect local atomic arrangements through bond frequencies and the lattice-vibration (phonon) frequencies of the Si-Si bond. Raman spectroscopy is based on the Raman effect [92], which is the inelastic scattering of photons by molecules. This powerful analytical technique is based on the analysis of the inelastic scattering of light interacting with the material under test. Raman spectroscopy provides spectra characteristic of molecular vibrations (or of phonons in solids) that can be used for sample identification and/or phase quantification. Light (photon) passing through a sample is weakly scattered from an individual atom by dipole interaction. The oscillating atomic dipoles re-radiate light in all directions. The majority of the light undergoes Rayleigh scattering which radiates at the incident wavelength but a small fraction of incident photons are re-radiated at different wavelengths at very low intensities. The wavelength change is due to an interaction of the incident light with the material. The interaction of the incident light with optical phonons is called Raman scattering whilst the interaction between light and acoustic phonons is called Brillouin scattering. A Raman spectrum represents the intensity of the scattered light as a function of the shift in frequency (i.e. energy) from the excitation light frequency. This “Raman shift” is directly linked to the vibrational energy of the bonds between the atoms within the probed material. In the case of silicon thin-films, Raman spectroscopy is particularly well suited to discriminate between the amorphous phase and the crystalline phase. Therefore, this analysis technique allows quantifying the degree of crystallinity. In Raman spectroscopy, the crystalline volume fraction (X_c) of a sample is defined as:

$$X_c = V_c / V_{exp} \quad (2.18)$$

where V_c is the crystalline volume and V_{exp} is the total scattering volume in the Raman experiment for a mixed phase material (i.e. $V_{exp} = V_a + V_c$, with V_a the amorphous volume). Due to a correlation between scattering volume and the integrated Raman scattered intensities [93], the crystalline volume fraction of Eq.2.18 can also expressed in the following manner:

$$X_c = I_c / (I_c + y \cdot I_a) \quad (2.19)$$

where y is defined as the ratio of the integrated Raman cross-sections [94]. Where I_c and I_a can be directly measured from the Raman spectra and values of y is 0.88 [94]. Furthermore, y depends on the size of the crystallites (δ) and on the excitation wavelength [93]. In our study, Raman measurements achieved with a Renishaw Microscope System 2000, equipped with a Leica microscope, excited by different wavelengths (442, 514 , 630 nm), depending on the film thickness.

2.9.3 X-ray Diffraction (XRD)

X-ray diffraction (XRD) is a nondestructive technique for structural characterization of crystalline materials. Structural information is related to the crystal structure of silicon, including lattice constants, geometry, orientation of single crystals, preferred orientation of polycrystals and stresses, etc. [95]. In XRD, a beam of X-rays, with a wavelength typically ranging from 0.7 to 2Å is incident on a specimen and is diffracted by the planes of atoms in the specimen. The diffracted intensity is measured as a function of 2θ, where θ is the incident angle. The diffraction pattern is used to identify the specimen's crystalline phases and to measure its structural properties. When there is constructive interference from X-rays scattered by the atomic planes in a crystal, a diffraction peak is observed. The condition for the constructive interference from planes with spacing d_{hkl} is given by Bragg's law:

$$\lambda = 2d_{hkl} \sin\theta_{hkl} \quad (2.20)$$

where d_{hkl} is the spacing between atomic planes in the crystalline phase, λ is the X-ray wavelength, and θ_{hkl} is the angle between the atomic planes and the incident X-ray beam.

2.10 Impurity analysis and active dopant characterization

2.10.1 Secondary ion mass spectroscopy (SIMS)

In secondary ions mass spectroscopy (SIMS) positively and negatively charged atomic and molecular particles, emitted from a surface during ion bombardment, are mass analyzed. These secondary ions give important information about the impurity inside the deposited films. The process of secondary ion emission from a solid may be divided into energy and momentum-transfer, fragment formation (e.g. formation of a positively or negatively charged or neutral particle), and the subsequent electronic transitions which take place during the removal of the particle from the surface. In SIMS, a primary ion beam impacts on the sample and atoms from the sample are sputtered or ejected from the sample. Both charged and neutral particles are ejected. A small fraction of the ejected ions (positive or negative ions) are extracted into a mass spectrometer and separated according to their mass-to-charge (m/e) ratio by their bending moment in a large magnetic field. The mass spectrum reveals the elements present at the sample surface. The composition as a function of depth is obtained by continuing the bombardment to sputter erode the sample, and by simultaneously recording the mass spectrum with time and hence at various depths. Dynamic SIMS is simultaneously etching and analyzing the particles sputtered. Depth profiling has a depth of up to 10 μm and the depth resolution is 20 Å to 50 Å with sputter rates down to 1 Å/sec

2.10.2 Spreading resistance profile (SRP)

Spreading resistance profile (SRP) is basically a comparative technique for the determination of the in-depth resistivity (and active dopant) profile of an unknown silicon structure. As such, it gives direct access to the electrically active portion (mobile electrons and holes) of the dopant profile, opposite to chemical profiling techniques, such as secondary ion mass spectrometry (SIMS), which probe the fixed dopant ions of pre-selected impurity species. In the early days, for

thick structures, one could extract the unknown depth profile by direct comparison with a set of calibrated homogeneous samples, covering the resistivity range of interest, with little additional calculations. The practical implementation of the SRP technique is therefore as follows (see Fig. 2.19). A small piece of the material is mounted on a bevel block with an angle appropriate for the depth scale. Next, the bevel block is mounted onto a piston (with a thumbscrew) and placed into a polishing cylinder, within which it can move up- and downward. The latter is then pressed against a rotating frosted glass plate lubricated by a high grade of diamond paste. Typically, a few minutes of polishing are sufficient to obtain the bevelled surface needed to get in-depth access to all sub-layers. Subsequently, the bevel block with the sample is mounted on the SRP tool and the two metal measurement probes (typically consisting of a tungsten–osmium alloy) are properly aligned with the bevel edge. Finally, the measurement itself involves stepping both probes along the bevelled surface, starting on the original surface before the bevel, until the substrate depth is reached. At each step, the resistance at low bias (5 mV) is recorded. This procedure results in a one-dimensional raw data profile, which initially consists of the measured resistances versus their respective lateral positions (expressed as measurement point number).

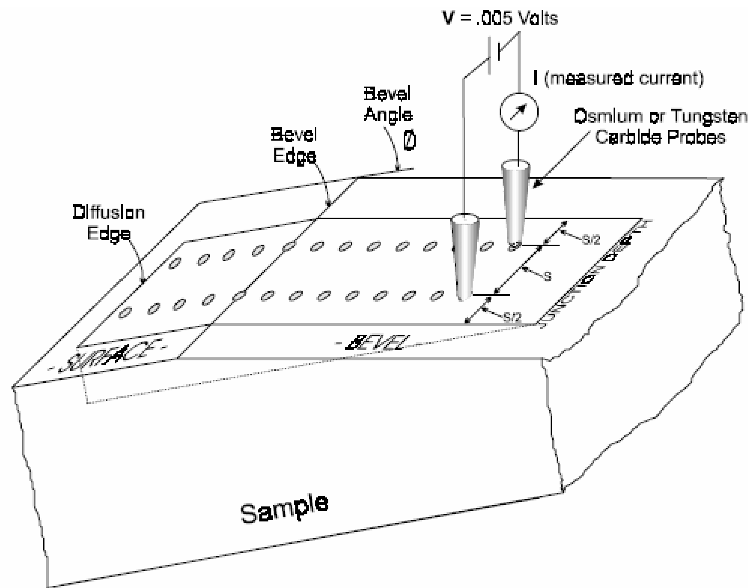


Fig. 2.19: Illustration of a Spreading Resistance Measurement on a Beveled Sample [96]

Given the lateral probe step size set on the tool and after the measurement of the actual bevel angle with a profilometer, it is, in principle, straightforward to convert the lateral position scale into the real depth scale. The starting point of the depth profile, i.e. the point with depth zero positioned exactly at the bevel edge, is typically determined with a high-magnification optical microscope (in the absence of a capping oxide). The conversion of the measured resistance scale into the underlying resistivity scale, which represents the actual physical variable is being sampled by SRP. One must, however, realize that the characteristics of the probe–semiconductor contact change continuously. Therefore, each day reference (calibration) measurements need to be made.

2.11 Summary

The different methods for monocrystalline silicon feedstock fabrication are presented. Physics of the solar cells are reviewed with more focus on homo and heterojunction structures. Different techniques used to deposited thin films are reviewed with more focus on PECVD, where it will be our main processing system for silicon film development. A focused review of the basic physics and chemistry of non-equilibrium glow discharges, and the description of the influence of ions on the development films are discussed. Description of the highest reported crystalline silicon solar cell and thin film silicon solar cells technologies are discussed including the issues and problems related to each type. It is obviously clear that, there is a need to develop new materials at low temperature with high electronic quality to overcome the issues related to amorphous silicon and microcrystalline silicon and be compatible with the industry production, with high deposition rate, and good electrical properties. To do so, many characterization tools are involved in the characterization of the structural, impurity, doping, and electrical properties of the selected and optimized films were presented.

Chapter 3: Experimental Work: Development of phosphorous doped LT PECVD epitaxial Si films

Introduction

Plasma enhanced chemical vapor deposition (PECVD) for low-temperature homoepitaxial growth of silicon, has been an active area of investigation for the past two decades in hopes of meeting the needs of future semiconductor device fabrication [97–100]. The well known profit of low temperature processing [101], coupled with avoiding dopant redistribution at low temperature, so that the abrupt transition regions can be obtained [102]. As well, the bulk diffusion, surface segregation of dopants and dislocations is suppressed by using low temperature deposition process. However, this may result in other processing difficulties, which could compromise both the epitaxial and electrical quality of the material. For example, epitaxial films with very high doping concentrations add to the challenge of obtaining high crystallinities in the low temperature Si thin films. Conductivity in n^+ Si film depends on electron mobility and the free electron density, which depends on active doping density. Meanwhile, carrier mobility is a critical property of the absorbing layer which used in optoelectronic devices such as thin film silicon solar cells. High crystallinity is the key factor towards obtaining highly conductive films. Improvement in the crystallinity can lead to enhancement in both the carrier mobility and also the active carrier density and hence the doping efficiency of the developed films. Therefore, epitaxial growth of silicon thin films can achieve both high conductivity and mobility due to almost defect free active layer and can improve both the carrier mobility and also the doping efficiency. The highly doped Si material is obtained either by high temperature diffusion process or by ion implantation followed by a high temperature annealing process [103], or grows by using high

sophisticated deposition techniques as molecular beam epitaxy (MBE), which is not compatible with the large scale production for the promising photovoltaic market. In [104,105] for instance, the authors have reported the development of highly doped epitaxial Si film growth on Si substrate at LT using PECVD technique. Silicon thin films with a maximum reported conductivity value of less than 100 $\Omega^{-1}cm^{-1}$ have been reported by using PECVD [106-108]. Our motivations and goals are to develop and deposit novel high efficiency $n^{+}p$ and $p^{+}n$ homojunctions through the growth of epitaxial phosphorous and boron doped emitters, respectively. This chapter is dedicated to thorough study of the development and a full characterization of highly phosphorous doped epitaxial silicon films at low temperature by PECVD for potential and stable solar cell devices.

3.1 Development of surface preparation schemes

We selected monocrystalline Cz silicon with (100) orientation as the starting substrate. So, the film growth under the developed processing deposition parameters will be discussed in details on (100) substrate orientation, and different substrate orientations such as (111) and (110) will be investigated. One-sided polished boron doped substrates with resistivity of 1-10 Ω cm and about 420 μm in thickness will be used. The substrate surface is of crucial importance for high quality epitaxial growth film. It is therefore very important to obtain a clean and defect-free silicon substrate surface prior to deposition process, since contaminants and defects may result in the epitaxial films with high defect density [109]. To do so, two cleaning processes were applied to the substrate prior to the deposition in order to study their influence on the growth mode, the film structure and its quality. The cleaning processes that will be used in this research are *in-situ* and *ex-situ*. The *ex-situ* cleaning process can be achieved through the wet cleaning process while the *in-situ* is achieved through the dry process.

3.1.1 *Ex-situ* surface preparation process

We Applied standard RCA I (NH_4OH: DIW H_2O: H_2O_2 =1:5:1) and RCA II (HCl: DIW H_2O: H_2O_2=1:5:1) solutions to remove organic and metallic contaminations from the surface of the substrate [110], then rinsed it with de-ionized water for 4 min, and then blown dry with nitrogen gas. To remove the thin oxide layer and to leave the wafer surface passivated with hydrogen, the substrate is dipped in 3% hydrofluoric acid (HF) for 20s [111]. If HF dip was not used, the films would turn out to be microcrystalline silicon with rough surfaces. This observation is consistent with the model proposed by Meyerson [112]. Once etched, the wafers, loaded immediately into LT PECVD to keep the surface very clean and depressing the creation of any native oxide layer. The final coverage of c-Si surface with hydrogen preserves the substrate surface against the risk of contamination from environment, and reduces the rate of oxide formation. This *ex-situ* surface preparation scheme is investigated for epitaxial growth, without any combination of *in-situ* substrate cleaning schemes.

3.1.2 *In-situ* surface preparation process

In addition to the *ex-situ* wet cleaning, *in-situ* cleaning process for the substrate was applied on the substrate surface after loading in PECVD. Soft hydrogen plasma treatment under very low RF power density regime was applied exactly prior to the film growth. The use of plasma generates reactive ions and neutrals for efficient *in-situ* cleaning of substrates prior to epitaxy process. Hydrogen plasma treatment leads to the removal of oxygen, carbon and other surface impurities due to the chemical etching effect of atomic hydrogen as reported in [113], which may enhance the epitaxy growth. The plasma treatment also may result in surface roughening due to inhomogeneous etching which can lead to the breakdown of the epitaxial growth process. Care, however, must be taken to avoid damage to the substrate during *in-situ* cleaning processes. Since ion energies often exceed the binding energy of the substrate constituents, extended defects may result in the substrate and in the epitaxial layers. So,

we used a very low power density hydrogen plasma treatment of 6 mW/cm^2. On the other hand, we applied this process for a very short time 20 and 60 sec, at 200 mTorr processing chamber pressure, and 150 sccm hydrogen flow at 300°C to investigate the influence of the *in-situ* hydrogen plasma treatment.

3.2 Development and Optimization of LT-PECVD process for epitaxial films

We used (100) p-type Cz crystalline Si substrate as the starting material for the epitaxial process development. The substrate properties are as follows, one-sided polished boron doped with resistivity of 1-10 Ω cm and about 420 μm thick. As we mentioned earlier the cleaning process is one of the key parameters in low temperature epitaxial growth. So, a particular attention was paid to the cleaning process of the silicon substrate to perform epitaxial films at low temperature. In between the RCA's cleaning process a 3% HF dip for 20s was used. The substrate was rinsed for at least 5 minutes with de-ionized water (DIW) between the two standards RCA's cleaning processes for efficient cleaning, it was then blown dry with nitrogen gas. Native oxide etching which formed on the wafer surface was performed directly before loading the Cz-Si substrate to the PECVD system. To ensure that the cleanest interfaces were obtained, fresh HF solutions were prepared and applied on the substrate surface. Fifteen second of 2% HF in DIW was used to remove the native oxide. Once etched, the wafers are loaded immediately into the PECVD to keep the surface very clean and to prevent the creation of any native oxide layer. After pumping down to processing pressure of nearly 2-3 x 10^{-6}, an ultrahigh purity processing gases of 99.99% were introduced into the chamber for the deposition process. There are many parameters which affect Si growth in low temperature PECVD system. The most important parameter is the hydrogen dilution (HD) ratio inside the processing PECVD reactor which was studied extensively as the main parameter for the epitaxial growth under low temperature regime (= 300°C) and even at a very low temperature (200 and 150°C). Other parameters are, the RF

power, chamber pressure, silane flow rate, substrate temperature and phosphine flow (for doping), are presented in table 3.2.

Table 3.2: Different processing conditions for phosphorous doped epitaxial growth silicon films.

	Doping (Phosphorous)	SiH_4 flow (sccm)	Hydrogen Dilution (%)	Power density (mW/cm^2)	Chamber Pressure (mTorr)	Temperature (^oC)
EP1	doped	25	0-96	47	400	300-200-150-25
EP2	doped	5	99	70	900	300
EP3	doped	25	90.16	11.75	400	300
EP5	doped	5	97.02	47	900	260

The Growth mechanisms, bulk structure analysis in atomic scale using high resolution transmission electron microscope (HRTEM), Raman spectroscopy will be discussed in details. The specimen preparation for HRTEM analysis were applied for the whole characterized films as follows; grinding and polishing technique down to a thickness of approximately 150 µm and dimpling down to 20 µm. Specimens were finally thinned to electron transparency using an ion mill with Ar^+ beam at an angle of 5° and 5 kV. Bright field (BF)/dark field (DF) images can be obtained using HRTEM analysis. For a detailed analysis, the JEOL 2010 HRTEM system equipped with a selected area diffraction patterns (SADP) and convergent beam electron diffraction (CBED) was used. The JEOL 2010 HRTEM system operated at 200kV and is capable of a point resolution of 1.4Å. Extensive HRTEM analyses were performed at the Canadian centre for electron Microscopy (CCEM). Moreover, we extensively used Raman spectroscopy to investigate the fine structure of the developed films. Raman scattering is a powerful light scattering technique used to diagnose the internal structure of molecules and crystals.

The measurements were achieved using a Renishaw Microscope System 2000, equipped with a Leica Microscope. UV Raman (328 nm laser line) was used to investigate the structure of thin films down to 10 nm on crystalline substrate without any contribution from the substrate. This laser line is radiated from Helium-Cadmium (HeCd) laser with spot size equal to nearly 1.0 μm^2 at room temperature and 2.0 cm^{-1} resolution. The spectrometer was calibrated with monocrystalline silicon wafer as a reference before the measurements. Impurity and doping concentrations of the developed epitaxial silicon films are characterized using the well established secondary ion mass spectroscopy (SIMS) analysis at Surface Science Western facilities at University of Western Ontario. The free carrier concentration in the developed layers plays a crucial role in the development of Si films, the fabricated junctions, and consequently the fabricated solar cell devices. We used the spreading resistance profile (SRP) to measure the free carrier concenteration inside the epitaxial films. The influence of the optimized rapid thermal process (RTP) profiles, and the related issues such as hydrogen effusion, and their effect on the developed new devices will be addressed and discussed in detail. This chapter can not be completed without carefully investigating the influence of the substrate orientation and the growth process at low temperature. We will name these processes as EP1, EP2, EP3, etc… (Abbreviation for the epitaxial growth processes). In EP1 process, hydrogen dilution (HD) between 85 and 95% was used to investigate its effect on the epitaxial growth under constant power density 47 mW/cm^2, chamber pressure 0.4Torr, a ratio of (PH_3/SiH_4=0.4), and substrate temperature of 300^oC. The substrate temperature was varied to investigate its influence on the growth mode and film structure using EP1. While, for EP2, a very high hydrogen dilution regime HD $\geq$ 99% is applied, under relatively high chamber pressure (0.9Torr) at a temperature of 260^oC. In the following sections we will discuss each process in detail from structure and electrical point of view.

3.3 Films deposited with intermediate H-dilution regime

3.3.1 HRTEM analysis

An intermediate hydrogen dilution regime HD (85-95%) was applied in EP1 process. This variation of HD has been used to investigate both the film quality from structure and electrical point of view. Figure 3.1 shows a low resolution TEM image of the prepared sample from the deposited silicon film. We can identify three regions that should be investigated carefully inside the growing structure. Two of these regions are the bulk and interface between the growing film and the substrate. The third region is the area at the upper surface of the growing films, on which the sputtering metal contacts will take place for n^+p homo and heterojunction device contacts. The cross section of the growing films probed by HRTEM electron beam coincides with the [110] zone axis. The growing films at 91.6 % (HD) were studied using selected area electron diffraction pattern SADP equipped in HRTEM. The samples prepared for this HRTEM are cleaned and treated using *ex-situ*, a wet cleaning process as described previously. Figure 3.2 shows the [110] HRTEM lattice image of highly phosphorous-doped developed film. The film was deposited on p-type crystal silicon (100) oriented substrate. During successive TEM sample preparation by grinding, dimpling and ion milling, the sample temperature kept less than 150 ^{0}C, hence, the solid phase epitaxy, SPE is negligible. Extended crystallographic perfection and orientation of the substrate through the growing layer of the epitaxial films is detected by cross-section HRTEM image. At an optimum value of 91.6 % (HD), we investigated the structure of the growing films at 300°C using EP1 process conditions.

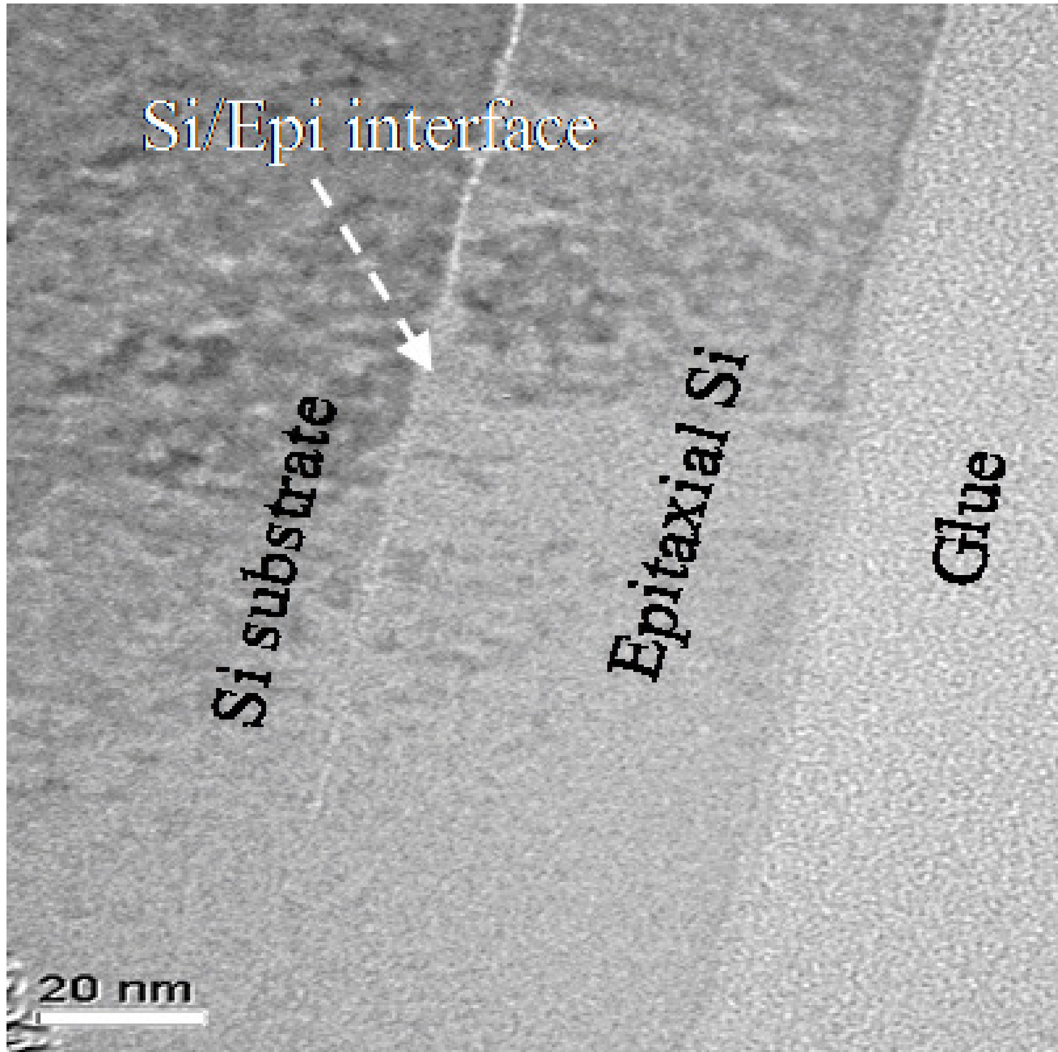


Fig. 3.1: Relatively low resolution cross-Sectional TEM Bright Field micrograph of epitaxial growth sample deposited at 91.6 % hydrogen dilution using EP1 processing conditions; (Notice the smooth interface between the substrate and the epitaxial film).

High resolution TEM micrograph confirmed the epitaxial growth as presented in Figure 3.2. Lattice planes of the growth films have exactly the same inter plane distance, d=3.14 Å, for Si substrate. The thickness of the growing films was measured directly by HRTEM and it is in coincidence with the values calculated from the deposition rate under different HD using the surface profile techniques. The bulk of the growing films up to 50 nm with relatively high deposition rate 0.9 Å/s are presented

on the same image. Defect free bulk of the growing films was noticed till the last deposited layer, which confirmed the epitaxial quality of the deposited films.

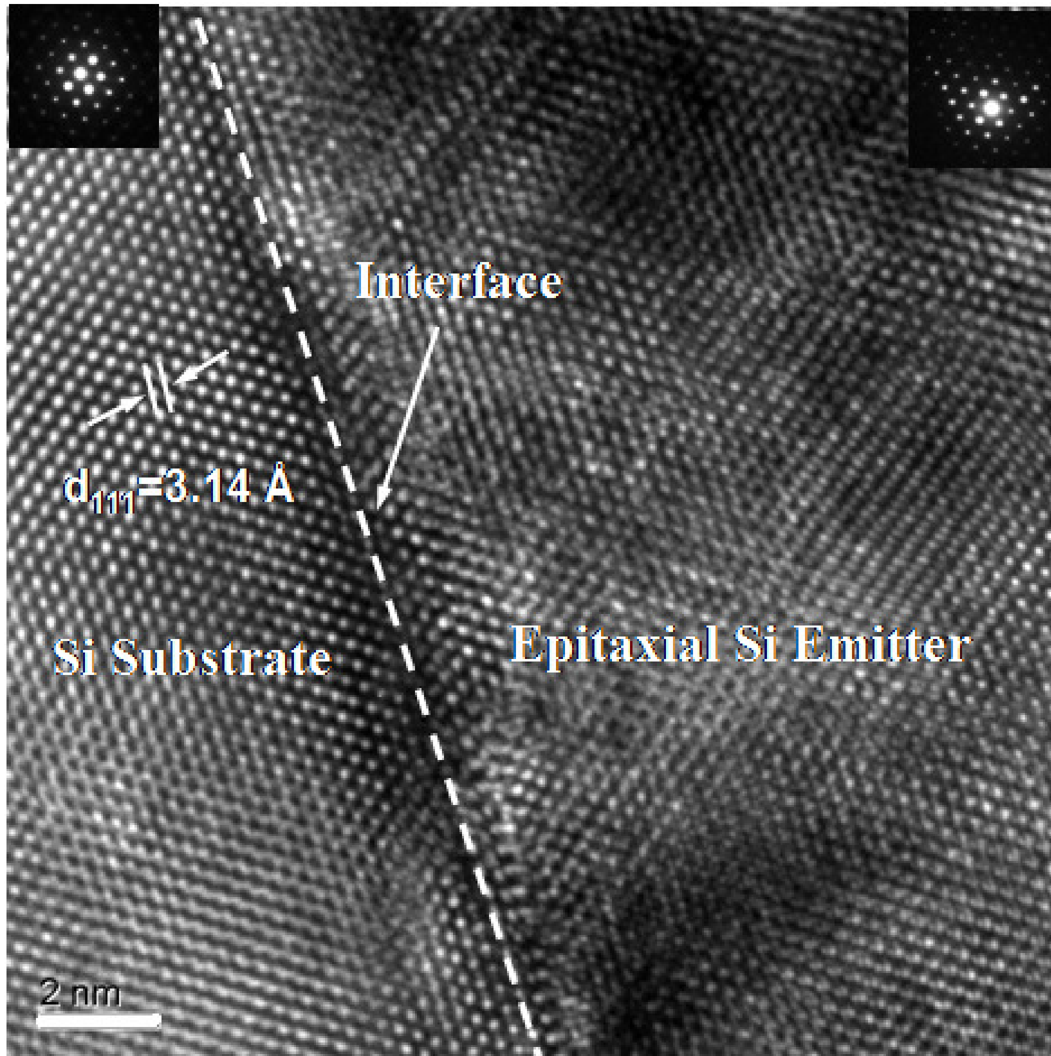


Fig. 3.2: Cross-sectional HRTEM micrographs of epitaxial emitters developed at 300°C using LT PECVD, and using EP1 conditions, the <111> planes shown in both single crystal substrate and in Epitaxial emitter, (SADP is shown: the left for Si substrate and the right for the developed epitaxial emitter (scalable bar=2nm).

Selected area electron diffraction pattern (SADP) from the films growing at 91.6 % hydrogen dilution shows a spot pattern without any interference of ring pattern (for polymorphous structures) or twin

crystal-structures. These patterns confirmed the high quality of the first deposited layers as the final layers which in contact with the glue. Interestingly, the SADP of the monocrystalline Cz wafer is nearly the same as the epitaxial film. A good fit between the lattice planes of the substrate and the growing film lead to a high quality, coherent, and dislocation free interface as confirmed in Figure 3.2. Highly smooth and mirror like interface between the Si substrate and epitaxial films can also be seen in the same figure. A slight contrast (less than one atomic layer) at the interface which may be caused by stress was observed. No residual native oxide appear at or near the epitaxial/Si substrate interface which is sharply defined to the level of atomic resolution. This obviously, confirmed that, the *ex-situ* cleaning process is a very effective in the removal of the residuals, native oxide and the promotion of defect free epitaxial growth even at low temperatures using our developed processing conditions. This result disagrees with Reidy et al. [114] who demonstrated the difficulty in performing epitaxial growth by PECVD without the use of an *in-situ* cleaning process. However, to the best of our knowledge we are the first group to develop and produce this epitaxial structure without applying an *in-situ* process at 300°C. Meanwhile, the interface needs to be characterized by SIMS analysis to define the different elements and their concentration as we will discuss later. Figure 3.3 shows the internal bulk structure of the developed film. It is confirmed from the HRTEM micrograph that, a well defined epitaxial growth is achieved under these processing conditions. The structural quality of the growing epitaxial Si is as good as the substrate as seen in SADP on the top right of Figure 3.3. Not only the bulk of the developed films which have this epitaxial structure but the structure configuration extended up to upper surface of the film in contact with the glue which used for sample preparation for TEM, as shown in Figure 3.4.

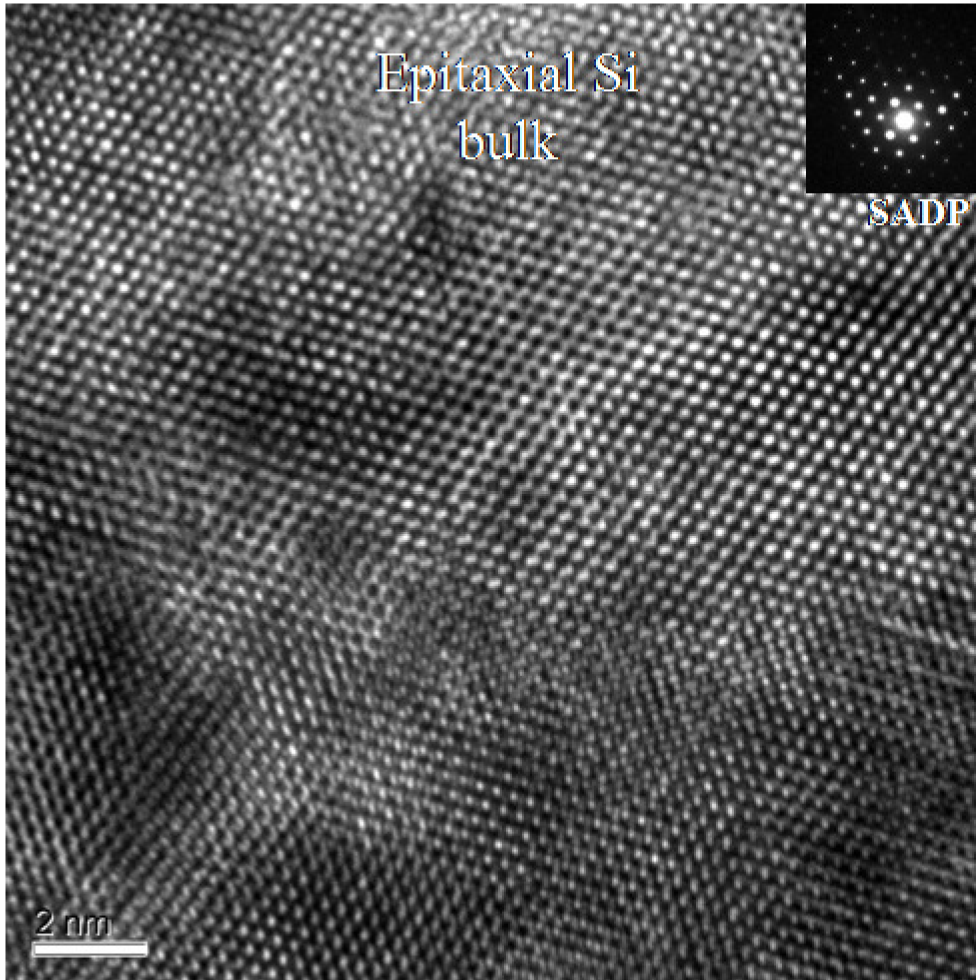


Fig 3.3: High resolution TEM bright filed image of the epitaxial bulk showing the lattice atomic structure and extended crystallographic perfection and orientation of 50 nm thick films, combined on the top right with selected area electron diffraction (SAED) pattern using (CBED) convergent beam electron diffraction. (EP1 conditions is applied).

Figure 3.4 shows the upper atomic lattice structure of the growing film, as we see the epitaxial growth extended till the upper surface. Growing films at the upper surface are found as perfect as the initial layers as seen in Figure 3.4. The structure of the growing films was analyzed by the fast Fourier transformation (FFT) analysis and the pattern is presented in the upper left image of Figure 3.4. From this pattern, we noticed that, there is no other extra spots which specified for defects inside the

film as twins. Consequently, the upper surface of the growing film has the same epitaxial structure as the deposited initial layers. Hence, the film preserves the same fine structure and it is defect free as the initial lattice structure. We succeeded to develop epitaxial films up to 400 nm, at 300°C and at intermediate hydrogen dilution regime. Breakdown phenomenon was noticed in films with a thickness > 400 nm with teeth like structure developed at this thickness. Different models have been used to explain the role of hydrogen chemistry on the developed film structure [115, 116]. According to the etching model [115], which is specifically used to describe the development of micro and nanocrystalline Si (~99-99.9% hydrogen dilution), atomic hydrogen at the film-growth surface preferentially breaks weaker Si-Si bonds in the amorphous network structure. The broken site is replaced by a new precursor, forming a rigid and strong Si-Si bond. Columnar growth mode with grain size of 20-40 nm can be developed using high hydrogen dilution regime in the range of 99-99.9 % on glass substrates. In the surface diffusion model [52], sufficient density of atomic hydrogen from H_2-diluted SiH_4 plasma causes a full surface coverage by bonded hydrogen and also produces local heating through hydrogen-recombination reactions on the growth surface of the film. We believed that for our film growth, the diffusion model is the proper model that can explain the epitaxial structure of the developed films. Moreover, we used Raman spectroscopy to investigate the fine structure of the developed films under this hydrogen dilution regime. This analysis will be discussed in detail in the next section.

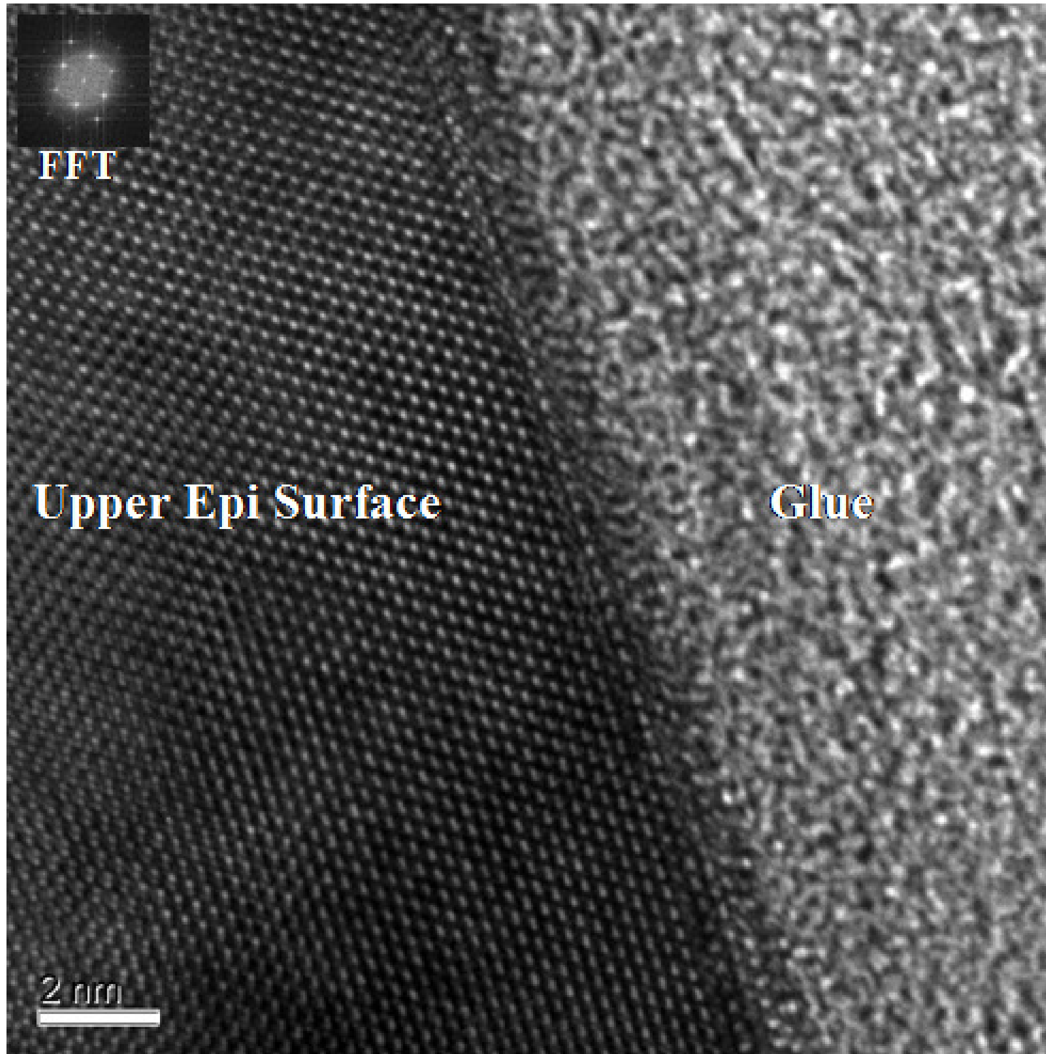


Fig 3.4: HRTEM of lattice structure of the upper surface (in contact with the glue) of 50 nm film and included the Fast Fourier transformation analysis (FFT) near the surface, (EP1 conditions are applied), the 91.6 % HD is used.

3.3.2 Micro-Raman Analysis

The structure analysis of the selected samples developed by EP1 process conditions, under different hydrogen dilution regime were characterized using Raman spectroscopy. Raman measurements are achieved using a Renishaw Microscope System 2000, equipped with a Leica microscope, excited by

different laser lines, 442 and 328 nm. For 442 nm laser, the radiation from Helium-Cadmium HeCd laser with spot size equal to nearly 1.0 um^2 at room temperature and 2.0 cm^{-1} resolution. The spectrometer was calibrated with monocrystalline silicon wafer used as a reference before sample measurements. The network structure of the growing films was probed also by 328 nm (UV Raman) for very thin films. The penetration depth of the UV laser used for testing the films is less than 8 nm. Therefore, the Raman signal in this experiment originates from the 50 nm thickness deposited film rather than the crystalline substrate. Monocrystalline (100) oriented Cz Si was used as the substrate for the development of these films at 300°C.

Hydrogen dilution influence on the film structure

Figure 3.5 shows the micro-Raman analysis of the developed epitaxial silicon films deposited in PECVD at 300°C. The processing conditions EP1 were applied using 91.6 and 95 % HD. The characteristic peaks which represent the Raman spectrum of amorphous silicon structure (*a* Si:H) is characterized by four bands, the most intense peak is the [Transverse optic (TO)] mode located at 480 cm^{-1}. The other bands are located at about 380 cm^{-1} [longitudinal optic (LO)], 310 cm^{-1} [longitudinal acoustic (LA)], and 150 cm^{-1} [Transverse acoustic (TA)]. The Raman peak for crystalline silicon (c-Si) is a sharp and nearly Lorentzian band centered at 520 cm^{-1} and with a full width at have maximum (FWHM) of about 3 cm^{-1}. A very strong intensity Raman peak was observed at 520 cm^{-1} for the both epitaxial films at 91.6% and 95 % HD similar to the Raman signal from the monocrystalline Si substrate reference. The other peaks that are related to *a* Si:H did not appear in this processing regime. This measurement confirmed that, there is no amorphous tissue between the interatomic crystalline structures of the epitaxial film. The appearance of the characteristic Si peak with nearly the same width as silicon wafer confirmed the epitaxial growth by using EP1 processing conditions. However, the electrical conductivity, as will be discussed in the next sections, was

decreased, this might be attributed to changes in the role of hydrogen at relatively high HD (95%) regime which is more likely to be dominant by etching mode.

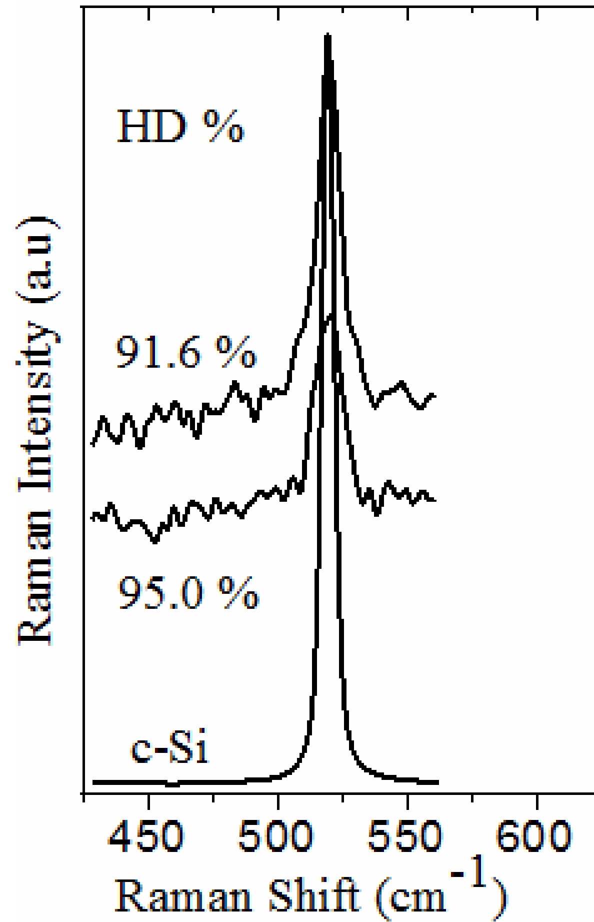


Fig 3.5. Micro-Raman analysis of the developed epitaxial silicon films deposited in PECVD at 300°C under different hydrogen dilution regime, the structure probed using 328 nm UV laser. (Note: the processing conditions EP1 are applied).

RF power density influence on the film structure

Figure 3.6 shows the micro-Raman analysis of the developed epitaxial silicon films deposited in PECVD at 300°C under different power densities (8 and 47 mW/cm^2) at constant hydrogen dilution,

using EP1 deposition conditions. Meanwhile, by decreasing the power density, we expect a decrease in the deposition rate, which may enhance the structure more. Nevertheless, we could not detect any change in the micro-Raman peaks, which means the effect of the power density at this processing regime is almost negligible.

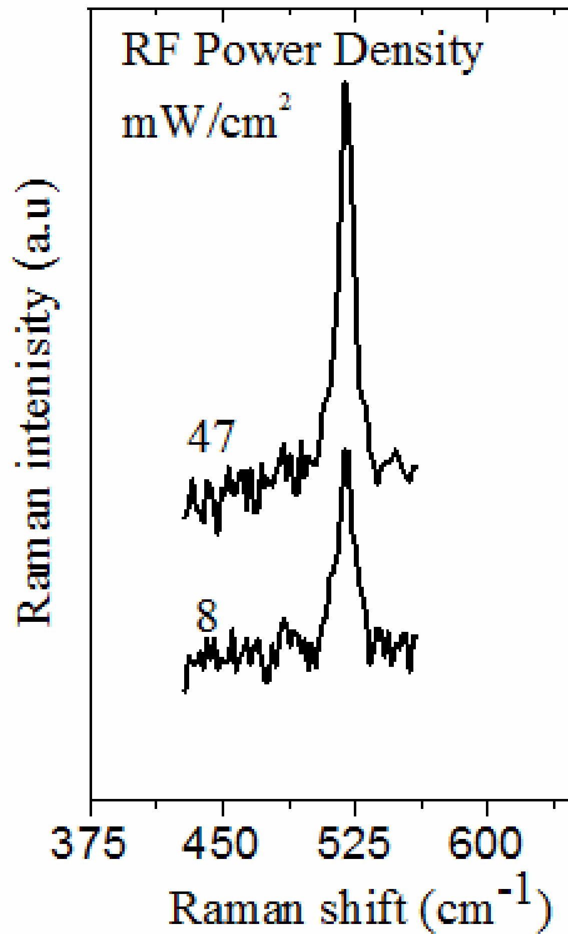


Fig 3.6: Micro-Raman analysis of the developed epitaxial silicon films deposited in PECVD at 300°C under different power density at constant hydrogen dilution, using EP1 deposition conditions, the structure probed using 328 nm UV laser.

3.4 Film deposited with high H-dilution regime

3.4.1 HRTEM analysis

We studied the structural properties of silicon thin films developed under very high hydrogen dilution regime ≥ 99%. The deposition conditions for this process are summarized in EP2 process conditions listed in table 3.2. In this process regime, a higher power density of 70 mW/cm^2 was applied, which is higher than the power density used in EP1, and the chamber pressure kept at 0.9 Torr at 300°C. Figure 3.7 shows the HRTEM micrographs of the bulk of the developed silicon films. It is clear that, we have epitaxial growth at this processing conditions using high hydrogen dilution. However, the bulk of this EP2 process did not have the same structure quality as the epitaxial grown films in the intermediate HD regime discussed in EP1 at 91.6 % HD. We noticed defective areas which composed of twins and stacking faults that appeared in the HRTEM micrograph. For this very high hydrogen dilution regime ≥ 99 % the hydrogen etching may be the dominant growth mode of the developed films [117]. Under high power density and high hydrogen dilution regime (more than 99%), the highly energetic electrons and other energetic reactive species can cause damage to the crystal structure at the interface. Hence, degrading the epitaxial layer and leading to defective epitaxial structure and may lead to the breakdown of the epitaxial growth even for thinner films.

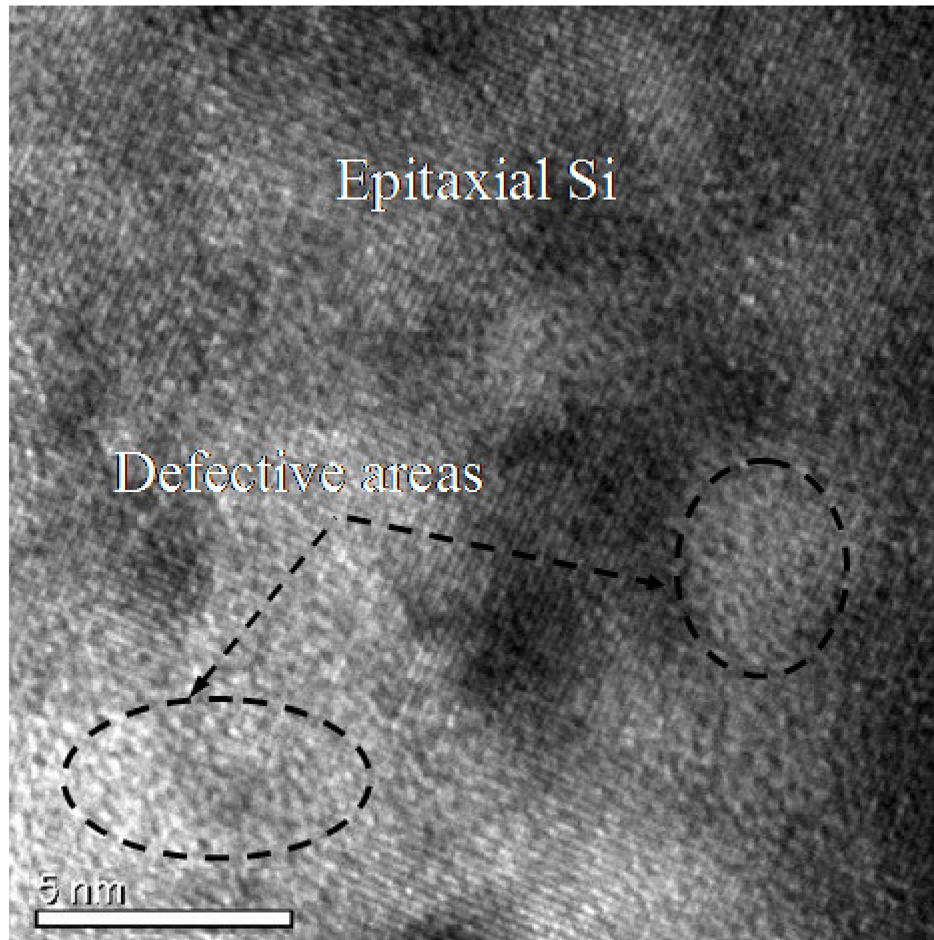


Fig. 3.7: High resolution TEM micrographs of phosphorous doped silicon films, developed using very high hydrogen dilution regime 99% and developed using EP2 processing conditions.

3.5 Film deposited at different temperatures

3.5.1 HRTEM analysis

We investigated the influence of the substrate temperature on the developed films using the optimum conditions of the process EP1 using LT PECVD. We used different processing temperatures, for example 200 and 150°C. We pushed the processing conditions in EP1 to the limits by trying to investigate the possibility to develop these films at the lowest processing temperature of (25°C).

Figure 3.8 shows the developed films at intermediate hydrogen dilution 91.6 % and applying the processing conditions described in EP1, at room temperature (25°C). It is obviously clear that, the substrate temperature has a great influence on the film growth. However, there is a very thin layer of epitaxial near the interface between 1-2 nm with maximum of 3 nm of isolated epitaxial domains near the interface, except that the developed film is completely amorphous. Nevertheless, we think that by optimizing the deposition conditions, especially the power density, hydrogen dilution and hence the deposition rate, the development of epitaxial films even at room temperature can be possible.

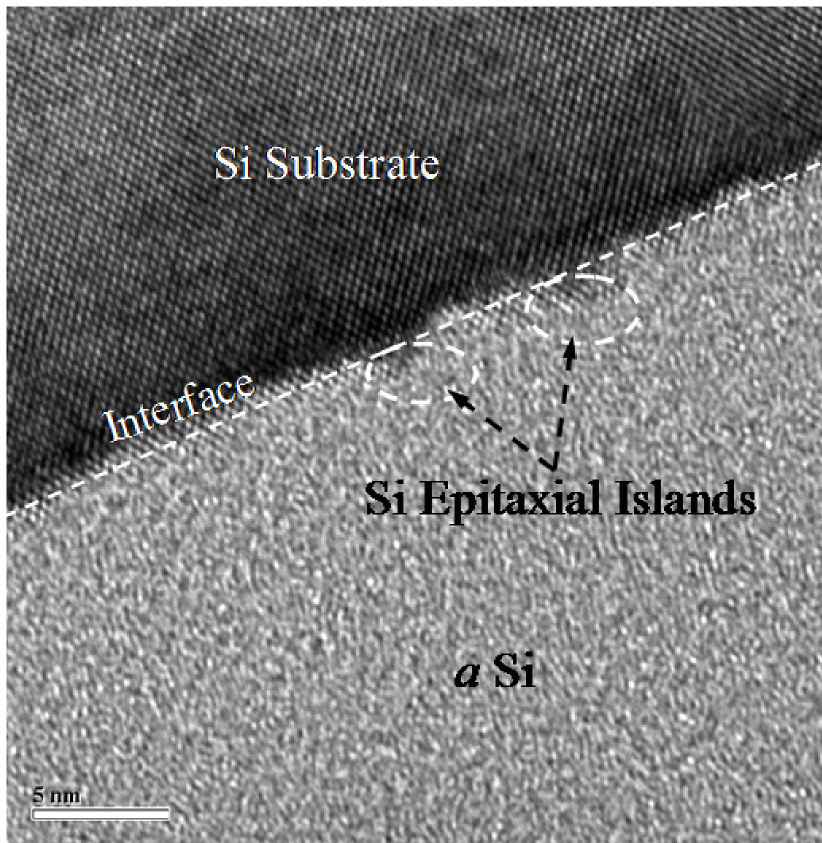


Fig 3.8: High resolution TEM bright filed images of the developed silicon films at room temperature (25°C) on (100) Cz-Si and using process conditions EP1, (scalable bar=5nm).

3.6 Impurity analysis of the deposited films

3.6.1 SIMS analysis

The impurity analysis of the developed epitaxial films is a very critical issue, especially if the developed films are to be used as an emitter for the solar cell applications. If there is any contamination or unnecessary impurities, this will initiate recombination centers in the bulk and at the interface of the developed films, and hence degrades the designed solar cells. We used secondary SIMS technique to analyze these impurities inside the developed films. For this analysis we deposited highly phosphorus doped (n^+) films on Cz-Si wafer with resistivity of 1-10 Ω-cm. Relatively thick films of 380-390 nm have been prepared for these analyses, especially for the doping concentration. Cameca IMS-3f ion microprobe using a Cs^+ beam less than 450 V is used to analysis the different elements and impurities inside the epitaxial films. Figure 3.9 shows the depth profile of the phosphorous concentration in the bulk and at the interfacial region of the developed films using EP1 processing conditions. Phosphorous profile is flattened through the bulk of the growing films at the level of 2.5×10^{20} cm^{-3}. A very sharp decline of phosphorous profile is noticed at the epitaxial/substrate interface. This very sharp decrease of the phosphorous dopant at the interface affords an abrupt *pn* junction for high efficiency silicon solar cells.

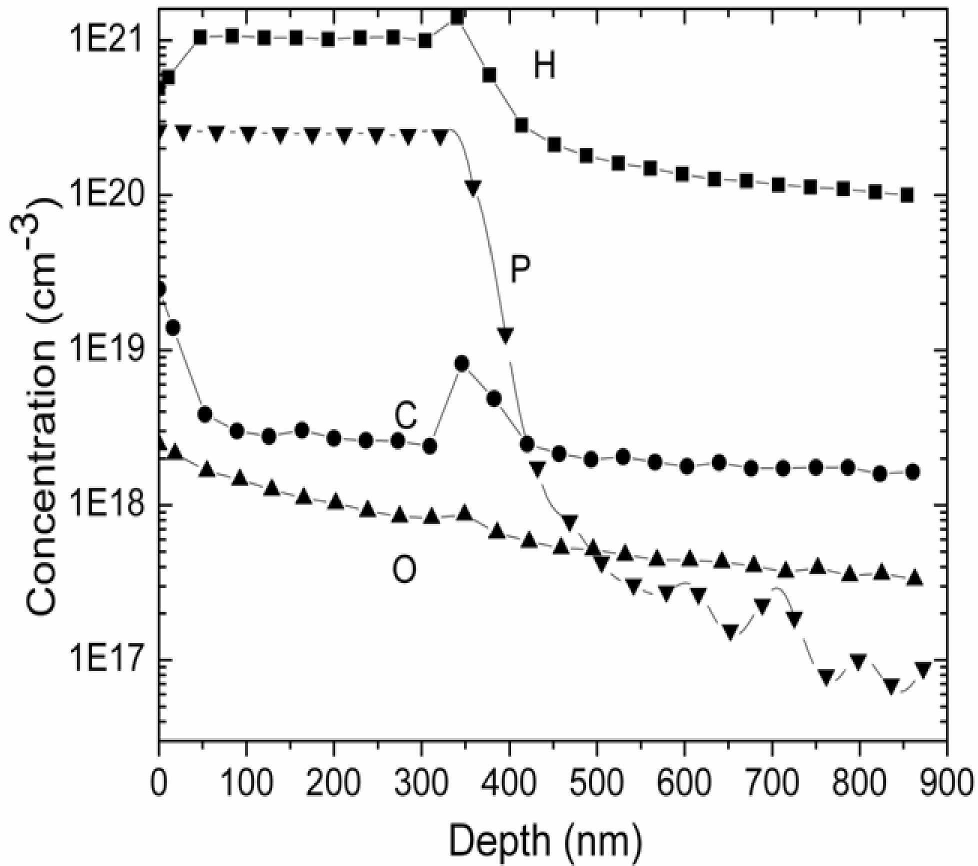


Fig 3. 9. SIMS analysis of phosphorous, oxygen, carbon and hydrogen in the bulk and at the interface of nearly 400 nm thick epitaxial Si films grown at 300°C by PECVD using EP1 condition. (Notice; the abrupt phosphorous profile which provides a perfect steep junction for solar cells).

High levels of carbon and oxygen can have a bad effect on the mobility of electrons in the growing silicon films. Hence, the levels of these elements should be monitored and kept at an acceptable level. The concentration levels of both carbon and oxygen are monitored and detected using SIMS measurement. Consequently, oxygen and carbon are detected throughout the bulk of the epilayer and interfacial region. The depth profile and the concentration of the phosphorous, hydrogen, carbon and oxygen are presented in Figure 3.9. For oxygen, no peaks are detected near the interface and the concentrations flatten through the bulk of the film with concentration of 6.57×10^{17} cm^{-3}. If we recall

back the perfect epitaxial growth which was presented in the HRTEM analysis in Figure 3.2. We can conclude that, the wet cleaning process combined with a 3 % HF dip for 20 s is an efficient cleaning process for the surface preparation for epitaxial growth. This interesting result is in contradiction with previous reports that indicate that thin-film plasma processes that rely solely on an *ex-situ* surface are highly unreliable [114, 118]. For carbon concentration, there are two peaks. The first peak is at the upper surface of the film with a carbon concentration of 2.49 x 10^{19} cm^{-3}, then the concentration of carbon is flattened after 53 nm through the bulk of the epilayer with concentration of 2.7 x 10^{18} cm^{-3}. The second peak appears at the epilayer/substrate interface with a carbon concentration of 8.21 x 10^{18} cm^{-3}. Relatively high concentration of carbon at the interface might be attributed to organic impurities contained in the cleaning solutions, or uncertainties in the measurements. The depth profile of hydrogen concentration was shown on the same figure. The hydrogen concentration at the top surface is 4.9 x 10^{20} cm^{-3}, this concentration gradually increased and started to flatten at 47 nm of the film thickness with a concentration of 1.04 x 10^{21} cm^{-3}. The concentration of hydrogen slightly increased to 1.4 x 10^{21} cm^{-3} at the interface between the epilayer and the p-type silicon substrate. Hydrogen has a very important role in the passivation of the dangling bonds at the interface and results in a high quality interface between the epilayer and the substrate. The quality of the interface between the film and the substrate is crucial, where the defects at the interface create recombination centers which have their impact on the photovoltaic efficiency.

3.7 Analysis of the dopant activation in the deposited films

3.7.1 Spreading resistance profile

The conductivity and carrier mobility values are good indicators of the electrical quality of the Si film and can be used to investigate the structural property indirectly. In this section, we present the electrical conductivity analysis through the detection of the active carriers inside the developed

emitters by spreading resistance profile (SRP). The effect of hydrogen plasma treatment, wet cleaning processes and their influence on the epitaxial growth, and the composition of the epitaxial structure at the interface will be presented in this section. The conductivity of the developed films is measured through different techniques, one of the most reliable and accurate method is the resistivity measurements using spreading resistance profile (SRP). The spreading resistance analysis is obtained by comparing measured values with measurements on standard bulk samples of known resistivity and appropriate crystal orientation. Each data point in four-point probe measurements has been derived from a statistical analysis of over 2000 current-voltage measurements. The (n^+) films were deposited and analyzed on Cz-Si with resistivity of 1-10 Ω cm under different hydrogen dilution (0 - 95 %). An example of the measured resistivity using SRP of the two selected samples at 0 and 91.6% HD is presented in Figure 3.10 for 220 nm thick films. Interestingly, seven orders of magnitude between these two selected hydrogen dilution regimes are noticed using the same processing conditions of EP1. The resistivity of the growing epitaxial layers in the range of 1.53×10^{-3} Ω cm is measured using SRP as shown in Figure 3.10. This low resistivity, lead to highly conductive epitaxial layers of conductivity up to 10^3 Ω^{-1} cm^{-1}. Very low sheet resistance of the epitaxial growing film was measured to be 70 Ω □ which is suitable for low cost solar cells without using transparent conductive oxide (TCO). The low resistivity of the developed silicon films deposited at the optimum conditions, EP1 at 91.6 %, can give an indirect indication about the epitaxial structure and high quality developed films, which are confirmed by HRTEM analysis. The full range of hydrogen dilution between 0 and 95 % is extensively characterized by using SRP technique which can give good indication about the structure quality, and the electrical properties of the developed films. To do so different samples with the same thickness and under EP1 conditions were prepared.

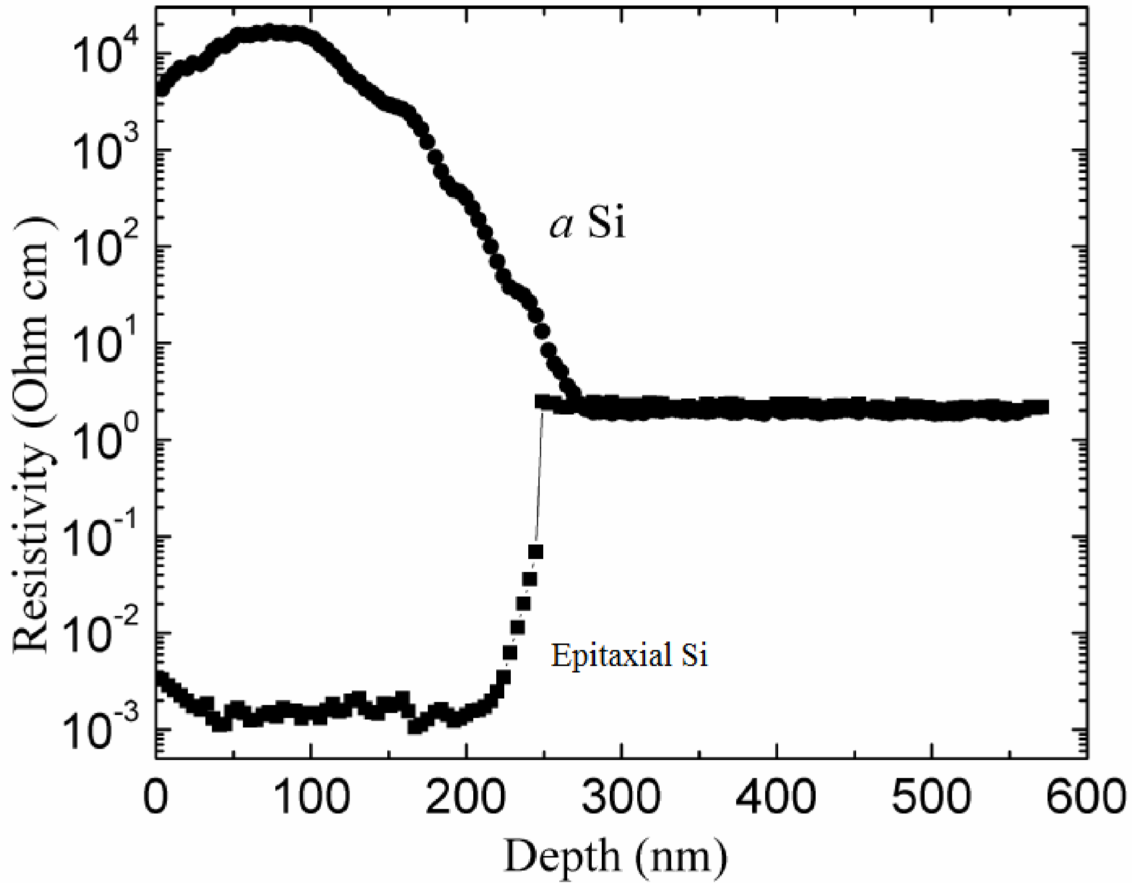


Fig 3.10 Measured resistivity of the developed epitaxial (91.6% HD) and *a* Si:H (no hydrogen dilution), of 200 nm thickness films deposited using PECVD on (100) oriented substrate, under EP1 processing conditions.

Figure 3.11 shows the measured conductivity of the developed epitaxial silicon films under different hydrogen dilution regime on (100) oriented substrate using LT PECVD system. We notice four different regimes through this wide window of hydrogen dilution: (1) The films deposited with HD < 80% show very low conductivities, between 0.0008 and 0.01 $\Omega^{-1}cm^{-1}$, comparable to the conductivity of *a*-Si:H films. (2) A very sharp transition occurs in the range of HD between 80% and 85%, where, the conductivity increased by 5 orders of magnitude. Consequently, this sharp transition indicates that, there is a phase transformation and structure evolution in this range. We expect that the deposited films transformed from completely amorphous phase to polymorphous structure. (3) The

films grown with 85% > HD < 91% show very high film conductivities, where, the films deposited between 91% and 92% hydrogen dilution have the highest reported conductivity of ~10^3 $\Omega^{-1}cm^{-1}$ comparable to the conductivity of highly doped high temperature diffused c-Si films.

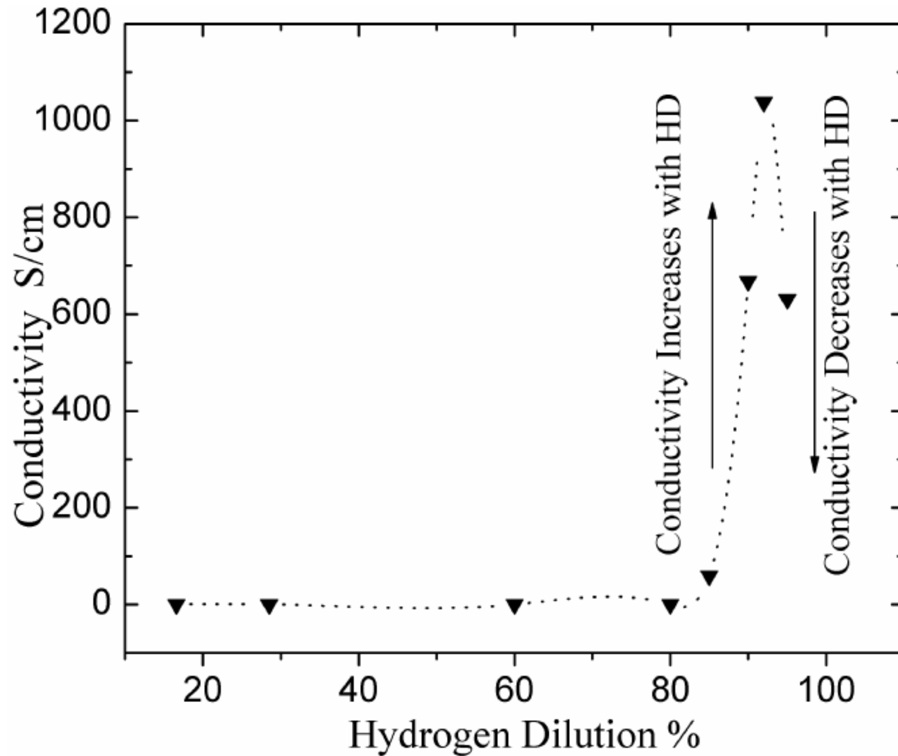


Fig 3.11 Measured conductivity of the developed epitaxial silicon films under different hydrogen dilution regime on (100) oriented substrate using LT PECVD chamber, (EP1 deposition conditions is applied).

Interestingly, by varying the hydrogen dilution from 90 to 91.6% the conductivity was doubled. So, hydrogen plays an extremely important role in the growth mechanisms, first by organizing the surface for epitaxial growth of the developed films, and second by enhancing the bulk structure of the growing films. The films deposited in this narrow hydrogen dilution range are epitaxially grown as confirmed by HRTEM and SADP insets. (4) Decreasing the conductivity in comparison to the maximum conductivity at 91.6 % HD, where the conductivity at 95% HD is 630 $\Omega^{-1}cm^{-1}$ which is almost equal to the conductivity at 90% HD. However, the bulk structures of the growing films are

still epitaxial. Hall measurement was used to characterize the mobility of the high conductivity films (HD > 85%). The films developed with HD of 91.6% showed electron mobility between 45 and 55 $cm^2/V.S$ and an average free electron density of 1.2 x 10^{20} cm^{-3}. Such high electron mobility with electron density of about 1.2 x 10^{20} cm^{-3} is very high and can be also compared with the electron mobility values in (n^+) c-Si material [119].

3.7.2 Doping efficiency

The doping efficiency η_d was defined by Street and co-workers [121] as the number of excess charge carriers introduced by electronically active dopants/dopant atomic concentration ratio, (phosphorous in this case). The ratio between the free electron concentration using SRP and atomic concentration using SIMS analysis represents the doping efficiency. The active dopant is measured using spreading resistance profile (SRP) technique. Spreading resistance profile (SRP) technique only measures dopants that are active and excludes inactive dopants. Hence, the free carriers inside growing layers could also be measured. Epitaxial films were grown using EP1 processing conditions and using wet cleaning process. Relatively thicker films of approximately 200 nm are prepared to measure the active phosphorous dopant inside the developed films. Figure 3.12 shows the measured active dopant (SRP) and dopant concentration (SIMS) profiles of heavily doped phosphorous with thickness of 200 and 400 nm at 300°C respectively (EP1 processing conditions is used at 91.6 % HD). The figure reveals that, the films have a very high active carrier concentration of average 5.0 x10^{19} cm^{-3} with a maximum at the interface of 6.9x10^{19} cm^{-3} as shown in Figure 3.12. It is obliviously clear that the epitaxial layer has a uniform depth profile of carrier concentration, which represents a uniform distribution of phosphorous dopants along the epitaxial growth direction. The interface of the *pn* homojunction grown epitaxially is very steep. This very high concentration of free carriers at the interface enhances the mobility even further. It confirms that an enhancement of the epitaxial growth,

especially for the first few nanometers of the growing films near the interface. The observed higher concentration of electrically active P atoms compared to the total phosphorus concentration indicates that almost all dopants become incorporated into substitutional positions. Highly doping efficiency η_d of more than 50 % is calculated from both SIMS and SRP analysis.

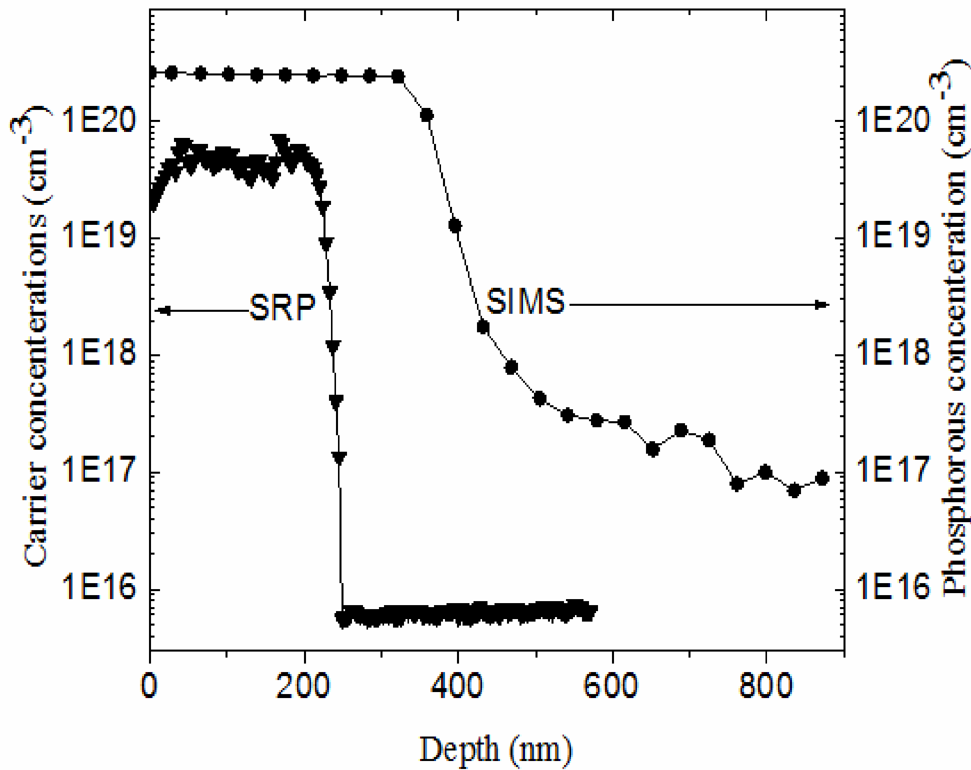


Fig. 3.12 Measured active dopant (SRP) and dopant concentration (SIMS) profiles of heavily phosphorous doped 200 and 400 nm epitaxially grown emitters at 300°C, respectively.(EP1 processing conditions is used).

3.7.3 Effect of H-plasma treatment

Different growing films of 200 nm in thickness were prepared using the same conditions for epitaxial growth, a pre-hydrogen plasma treatment (HPT) is applied on some of these samples before the deposition process for 20 and 60 sec. Spreading resistance profile (SRP) technique is most sensitive

to insufficient cleaning conditions, as the mobility at the interface degrades [120]. So, we analyzed the deposited films after applying HPT. Figure 3.13 shows the free carrier concentration of the phosphorous doped epitaxial silicon films using wet cleaning process (solid line) and hydrogen plasma treatment (dotted line), at $300^{o}C$ and 91.6 % HD. Interestingly, the doping efficiency has increased to 85 % by applying 60 sec HPT. The free carrier concentration was measured using SRP technique and we found that it has increased to $1.2x10^{20}cm^{-3}$ especially near the interface. This very high concentration of free carriers at the interface enhances the mobility, which indicates an enhancement of the epitaxial growth at the interface by applying HPT. However, some research groups reported on the formation of {111} platelet defect, in case of *in-situ* hydrogen plasma cleaning is applied, which may create more defects in the substrate and impact the epitaxial layer through the growing defects inside the substrate which extended to the growing films as well [99, 122]. However, the active dopant at the upper surface of the growing films in HPT films is lower than the films without hydrogen plasma, which indicates that the growing films are still epitaxial but with low quality at the upper surface of 200 nm films

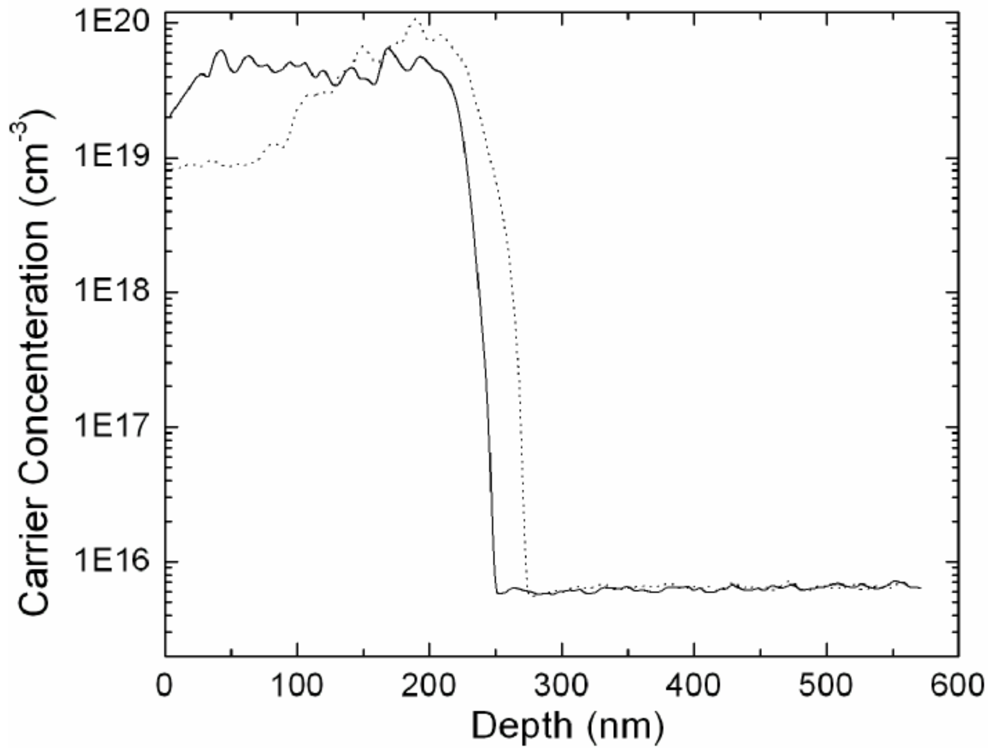


Fig 3.13 Free carrier concentration of the phosphorous doped epitaxial silicon films using wet cleaning process (solid line) and hydrogen plasma treatment (dot line), at 300°C and applying EP1 processing conditions under 91.6 % HD.

3.7.4 Substrate temperature-dependence of conductivity

The substrate temperature and its influence on the conductivity of the developed films is a very important issue, especially for low temperature solar cells. A selected very low temperature window between 25-300°C is investigated to study the effect of the substrate temperature (under EP1 epitaxial conditions) on the conductivity, and hence the structure quality of the developed films.

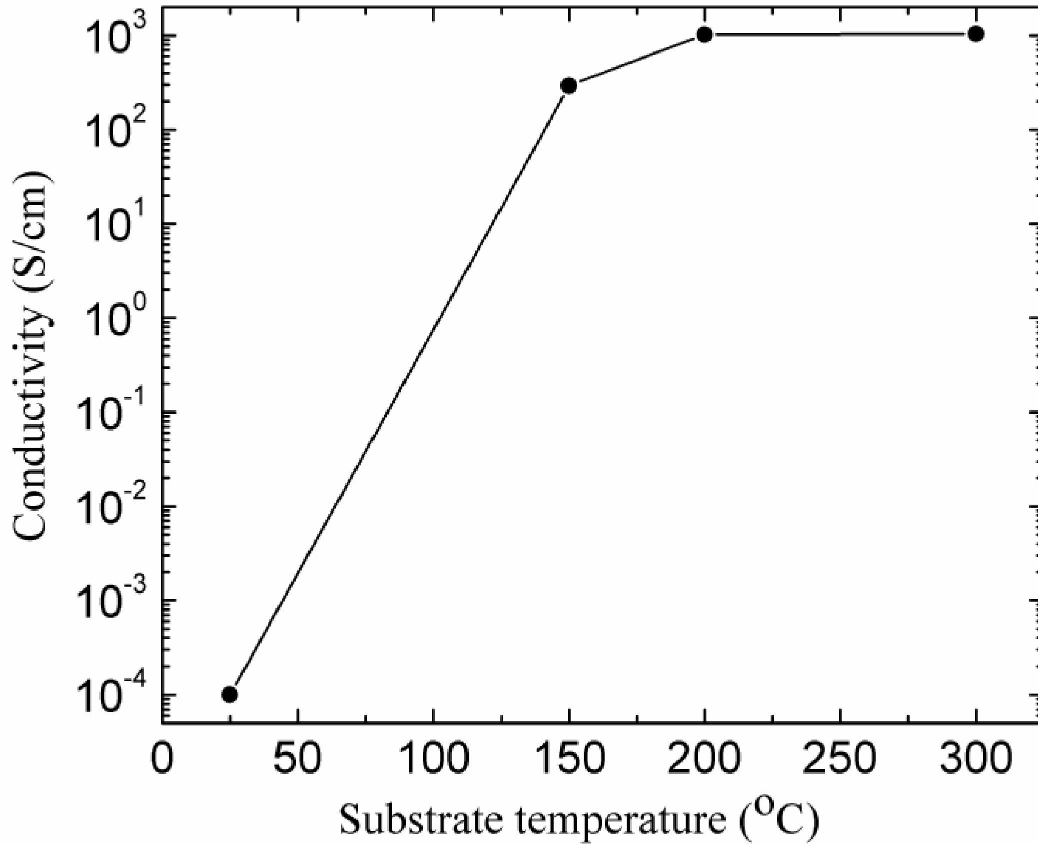


Fig 3.14 Conductivity-substrate temperature dependent of the developed silicon films deposited on (100) oriented silicon substrate at 91.6 % HD under varied temperature using EP1 processing conditions.

The selected low processing temperature range (25-300°C) is suitable for solar cells developed on low cost substrate. We monitored the film quality through the conductivity measurement, and the structure of the developed silicon films. Figure 3.14 shows that the electrical conductivity exhibits an increase of seven orders of magnitude when the substrate deposition temperature is increased from room temperature ~25°C to 300°C. Even at 150°C the developed films exhibit high conductivity of 292 Ω^{-1} cm^{-1}, which confirms that the growth at this low temperature is still epitaxial. The conductivity of the film developed at 150°C (292 Ω^{-1} cm^{-1}) is less than the conductivity of the films that are developed at 300°C. This can be attributed to the fact that some of the phosphorous atoms did not activated due to

the low substrate temperature, which directly affects the structure of the deposited films. Meanwhile, the films developed at very low substrate temperature (at room temperature=25°C) show very low conductivity ~10^{-4} Ω^{-1} cm^{-1} (comparable to the conductivity of *a* Si:H). The conductivity values measured at room temperature coincide with the structure characterization by HRTEM as presented in Figure 3.8, where the deposited films are almost amorphous except for a very thin fraction near the interface.

3.8 Effect of substrate orientation

3.8.1 HRTEM analysis

This part investigates the influence of the substrate orientation on the film quality during the low temperature epitaxial growth using the developed deposition conditions described in EP1 process on non-(100)-oriented substrates. Different substrate orientations as Si (111) and Si (110) were used. Deposition temperature kept at 300°C (the same as epitaxy on ((100) to avoid the influence of the substrate temperature on the growth mode and the developed films). Meanwhile, *ex-situ*, wet cleaning processes RCA I and RCA II, are only applied on the substrate before loading into PECVD system. Figure 3.15 shows the developed silicon films using EP1 processing conditions on (110) oriented silicon substrate at 300°C under 91.6 % HD.

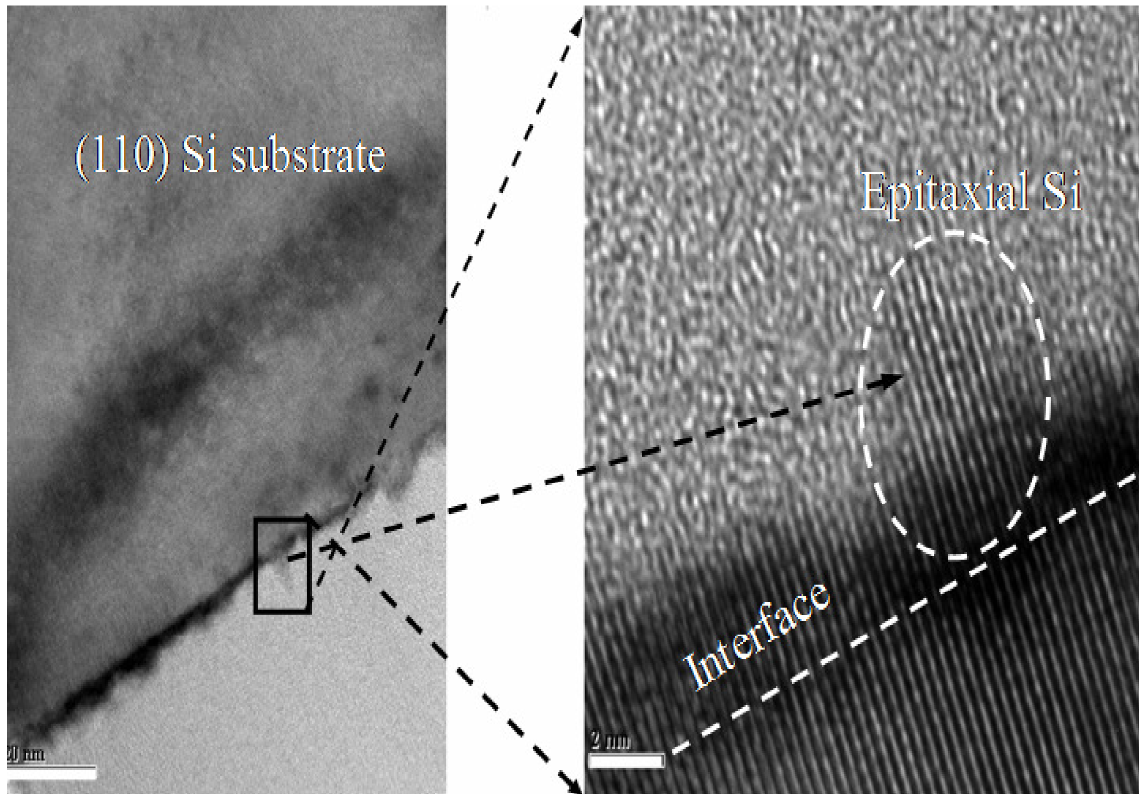


Fig 3.15 HRTEM micrograph of the developed silicon films on (110) oriented substrate at 300°C at 91.6 % HD and using EP1 deposition conditions. (scalable bar in the right micrograph=2nm).

It is confirmed from HRTEM analysis presented in Figure 3.15 that the substrate has a great influence on the growth of the developed films under the selected processing conditions (EP1 in this case). Although, the same deposition conditions are applied on both loaded (110) and (100), it is found that the structure is completely different. For the film developed on (100) oriented substrate the growth process is epitaxial as we discussed in detail in the previous section 3.3, meanwhile for the films developed on (110) and (111), the film is amorphous with some monocrystalline fractions (appeared in the dark field images, not included here). The first few nanometer layers of the film have the same crystalline structure as the substrate but it turned to amorphous film after 4-5 nanometers. Growth on non-(100)-oriented substrates, such as Si (111) and Si (110), is dominated by the formation of high

densities of extended defects, in particular stacking faults, resulting in significantly lower electronic quality of the film. This has its influence on the photovoltaic efficiency parameters for the prepared device on (110) and (111), if it is used as a substrate. So, we used (100) oriented substrate to be the main platform for our devices preparation under our developed processing recipes.

3.8.2 Spreading resistance profile

Resistivity and hence free carrier concentration are detected in the developed silicon films on the different orientation substrate using SRP. Figure 3.16 shows the resistivity and the free carrier concentration of the developed silicon films on (110) and (111) silicon substrate at 300°C for (EP1 processing conditions is used) measured by SRP. However, the two substrates are loaded in the same deposition run, and processing time, it seems that the film developed on (111) orientation is thicker than that the one deposited on (110) substrate. This behavior is noticed from the shifted junction in Figure 3.16b. Spreading resistance profile presented in Figure 3.16 shows that the deposited films developed on (111) and (110) substrate orientations have almost the same resistivity as the films developed on (111) substrate orientation, with a slight decrease in resistivity, which is approximately 0.1 Ω cm. The resistivity of the developed films near the surface is very high (~10^4 Ω cm) compared to the values near the interface, which confirms that the portion of the film near the interface is more likely to have a very narrow epitaxial films. The free carrier concentration for the films developed on (111) and (110) substrate orientation near the interface is equal to 4 $x10^{16}$ and $2x10^{16}$ cm^{-3}, respectively.

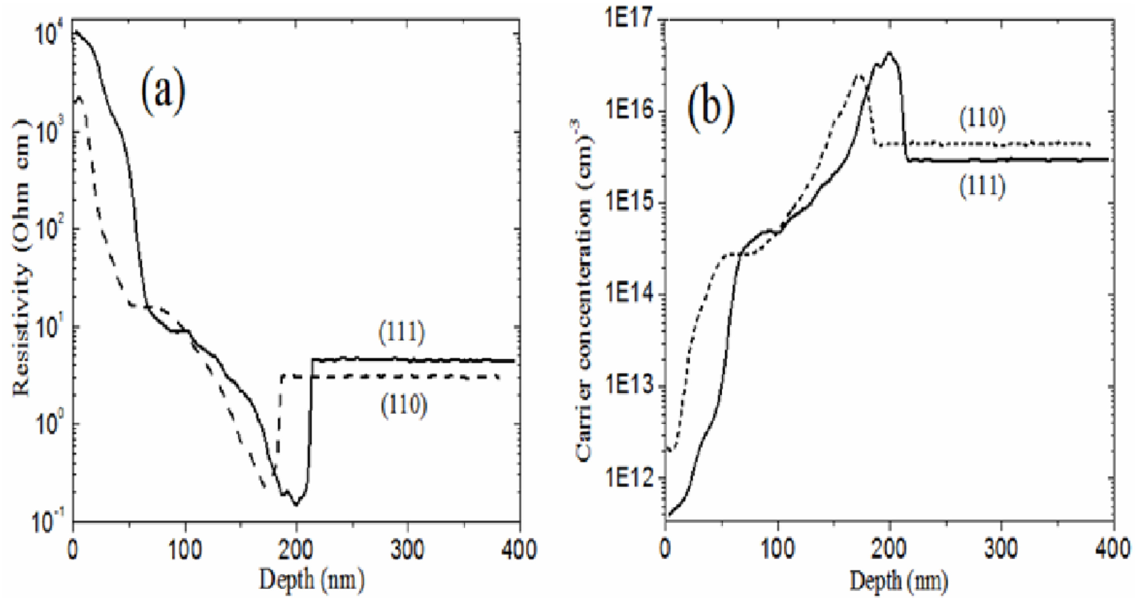


Fig 3.16 Spreading resistance profile (SRP) of the developed silicon films on (110) and (111) silicon substrate at 300°C (a) resistivity and (b) and carrier concentration, (EP1 processing conditions is used).

3.9 Post-deposition rapid thermal annealing

Rapid thermal annealing, with low defects and faster processes for higher yield and throughput has significant advantages for silicon processing, especially for amorphous Si cells. Rapid thermal processing (RTP) based on incoherent radiation as the source of optical and thermal energy is emerging as the most promising low thermal budget processing technique [123]. The annealing process is one of the most critical steps that determine the properties of these films after deposition. However, there are some issues related to annealing process which may degrade the cell efficiency such as the hydrogen effusion, minority carrier diffusion length, and dopant redistribution. The fine structure of the as deposited epitaxial films confirmed a high quality silicon films and very high active dopant concentration, especially at intermediate hydrogen dilution regime. However, we

investigated the influence of intermediate annealing temperature using rapid thermal annealing process (RTP) on the structure and the electrical properties of the growing film at LT PECVD.

3.9.1 Optimization of the RTP annealing profiles

A rapid thermal annealing system 600S series was used for the annealing process of the epitaxially grown phosphorous doped emitters. The maximum heating and cooling rates are 200-150°C/s, respectively. This system uses high-intensity visible radiation to heat a single wafer for a short time at precisely controlled temperatures. These capabilities, combined with the heating chamber's cold-wall design and superior heating uniformity, provide significant advantages over conventional furnace processing. Tungsten-Halogen Lamps (THL) are used inside the RTP system chamber, heating up the samples in nitrogen ambient with controlled mass flow rates. Each wafer is divided into four equal pieces to be sure that the films have the same deposition conditions and annealed under different programmed temperature profiles that will be describe later. The temperature of the annealed pieces is measured by highly sensitive thermocouple attached to the unpolished back side of the silicon wafer piece. Since, the developed epitaxial films (using EP1 at 91.6 % HD) is the most promising films to be used as emitters for high quality, high efficiency solar cells, most of the RTP annealing process is applied on these films. Structure and surface morphology of the annealed films by these programmed RTP temperature profiles have been studied extensively by HRTEM, scanning electron microscope (SEM), atomic force microscope, and high resolution optical microscope. Hydrogen evolution from a-Si:H films at 365 and 694°C determined by differential scanning calorimetry (DSC) are taken into account in the design of the different RTA profiles. However, the amount of hydrogen that evolved at 365°C (less than 1 % of total hydrogen evolved from the film) was so little that no DSC peak was observed at that temperature [123]. The hydrogen that evolved at 365°C has been attributed to the release of molecular hydrogen residing in the voids of the *a* Si:H [124]. So, we take into consideration

the hydrogen effusion temperature to develop the temperature profiles used to anneal the developed silicon films. This process enabled us to minimize the H effusion and its influence on the film structure, and hence the electrical properties of the developed films. Figure: 3.17 shows the applied temperature profile, (A) RTP, with pulsed heating and cooling steps annealed at a peak temperature of 750°C applied in 4 cycles for 25 sec.

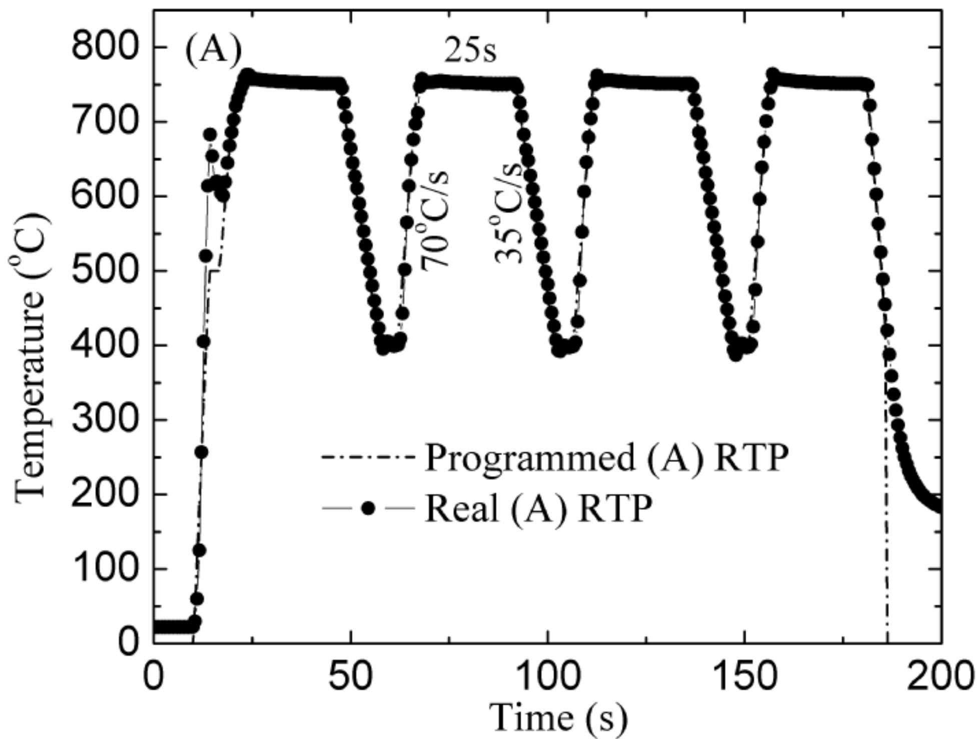


Fig: 3.17 Applied temperature profile, (A) RTP, with pulsed heating and cooling steps annealed at a peak temperature of 750°C applied in 4 cycles for 25 sec.

Three main temperature profiles were applied on the epitaxially grown silicon emitters; (i) "Pulsed Profile" (A) RTP, with high heating and cooling rates of 70 and 35°C/s and a peak temperature of 750°C applied in 4 cycles of 25 s each as shown in Figure 3.17, in this temperature profile the influence of very high heating and cooling rates were examined. (ii) "Two-Steps Profile" (B) RTP, where the temperature is ramped up to 400°C at a heating rate of 37.5°C/s, stabilized for relatively

long time, ramped again to 750°C where the epitaxial emitters were annealed for 60s as shown in Figure 3.18. In this designed (B) RTP temperature profile, a thermal stress for a long time (10 min at 400°C) is investigated. Figure 3.17 shows the temperature profile (B) RTP, (iii) "Multi-step Profile" (C) RTP, in which a peak annealing temperature of 850°C (750°C peak temperature is used as well) is reached after undergoing several intermediate temperatures and different ramping rates. In this profile an intermediate heating and cooling rates are studied, this temperature profile is shown in Figure 3.19. These three different temperature profiles were applied on the epitaxially LT PECVD grown emitters separately to study the influence of each one. A perfect coincidence between the real and the programmed annealing RTP was noticed except for the spike in the first step of the pulsed profile (A) RTP due to the very high heating rate which has been used.

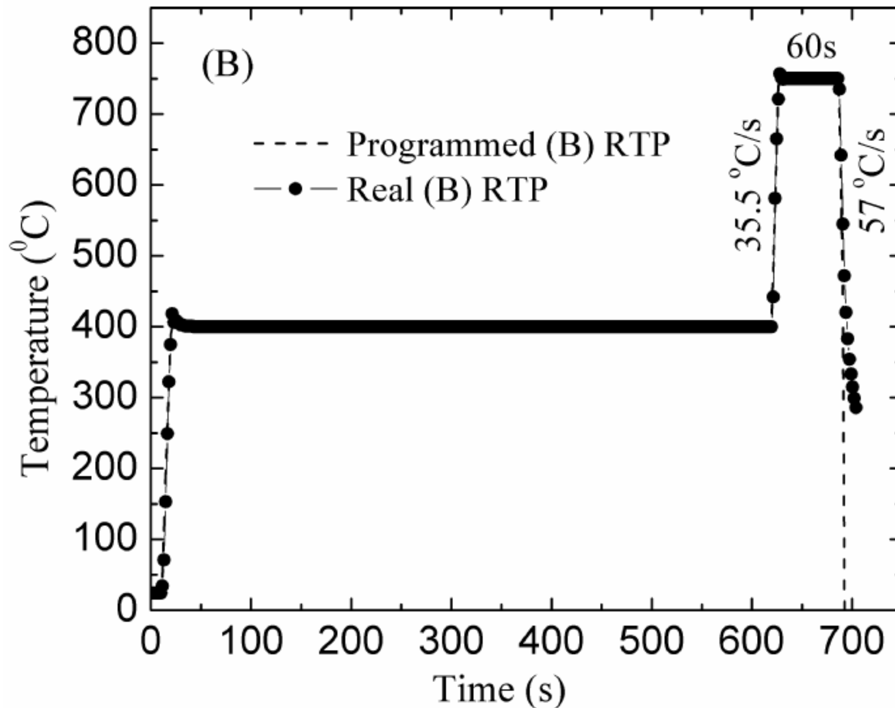


Fig 3.18 Applied temperature profile, (B) RTP, with two-steps annealing profile (10 min at 400°C) with a maximum annealing temperature of 750°C for 60s.

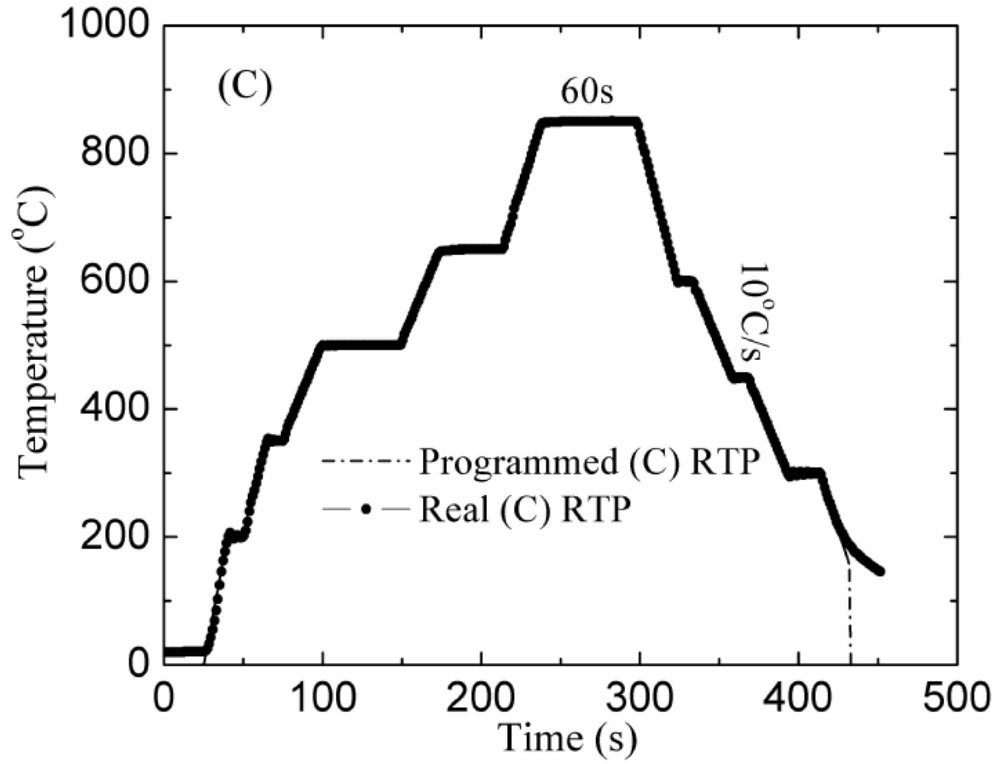


Fig. 3.19: Applied temperature profile, (C) RTP, with multisteps and different heating and cooling rates with a peak temperature at 850°C for 60s.

3.9.2 Impurity analysis of the annealed films

The depth profile of the phosphorous doped epitaxial grown emitters (using EP1 process) and applying the designed RTP profiles was measured by SIMS and is shown in Figure 3.20. A flat distribution of phosphorous is detected by SIMS analysis through the whole film thickness. It is shown that the junction depth of the epitaxial emitters is 400 nm which coincides with the emitter thickness as seen in Figure 3.20. Applying the annealing process using the different temperature profiles on the epitaxially grown emitters resulted in a deep diffusion of the phosphorous dopant. This result is noticed more in the pulsed (A) RTP profile, which increases the junction depth by nearly 35 nm, while for the two-step (B) RTP profile the junction shifted by 17 nm.

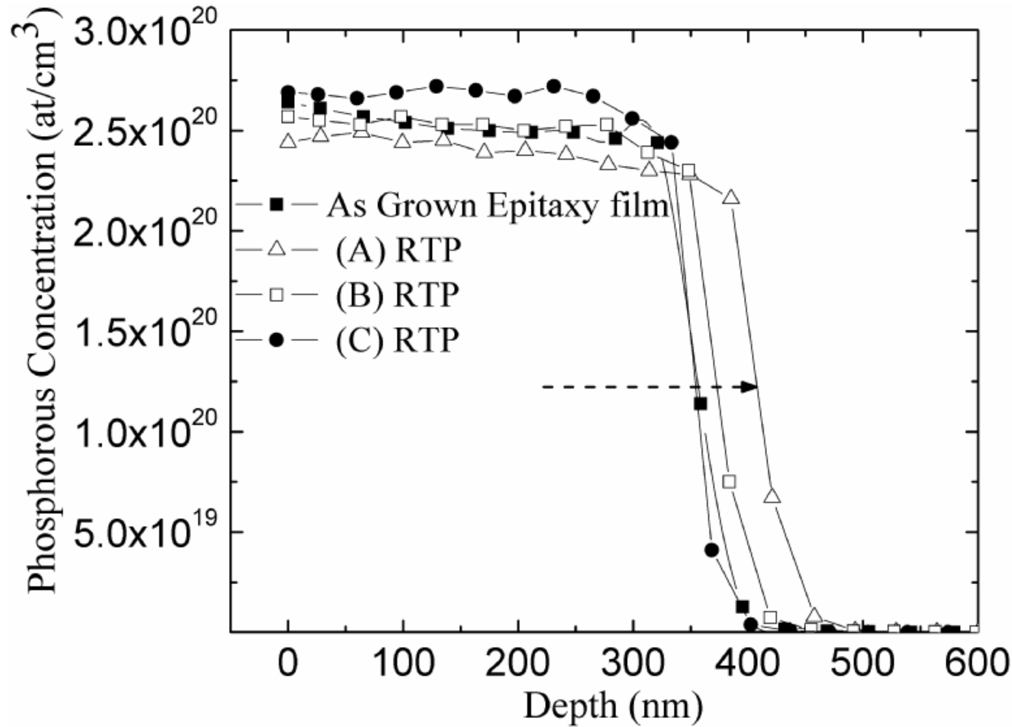


Fig 3.20: Phosphorous concentration and junction depth for epitaxial Si films after applying the different RTP temperature profiles, (EP1 processing conditions were used).

3.9.3 Hydrogen effusion analysis from the annealed films

Figure 3.21 shows the hydrogen content inside the as-deposited epitaxially grown emitters and after applying different RTP temperature profiles (EP1 processing conditions were used). As we mentioned in the previous section, the hydrogen evolution from Si films at 365 and 694°C was determined by differential scanning calorimetry (DSC) [123, 124]. Hydrogen concentration in the epitaxial emitters is measured to be 1 x 10^{21} cm^{-3} as shown in Figure 3.21. The hydrogen content decreased after the annealing process and its concentration changed depending on the applied RTP temperature profile. In the cases (B) and (C) RTP temperature profiles, the hydrogen content was almost the same and equal to 3x 10^{20} cm^{-3}. Under (A) RTP annealing profile the hydrogen concentration was measured to

be 8 x 10^{19} cm^{-3} which is an order of magnitude lower compared to the epitaxial emitters developed under 91.6 % HD using EP1 processing conditions. This hydrogen effusion under (A) RTP temperature profile may affect the interface, and/or the emitter bulk structure quality which will be analyzed in the next section using the high resolution TEM characterization.

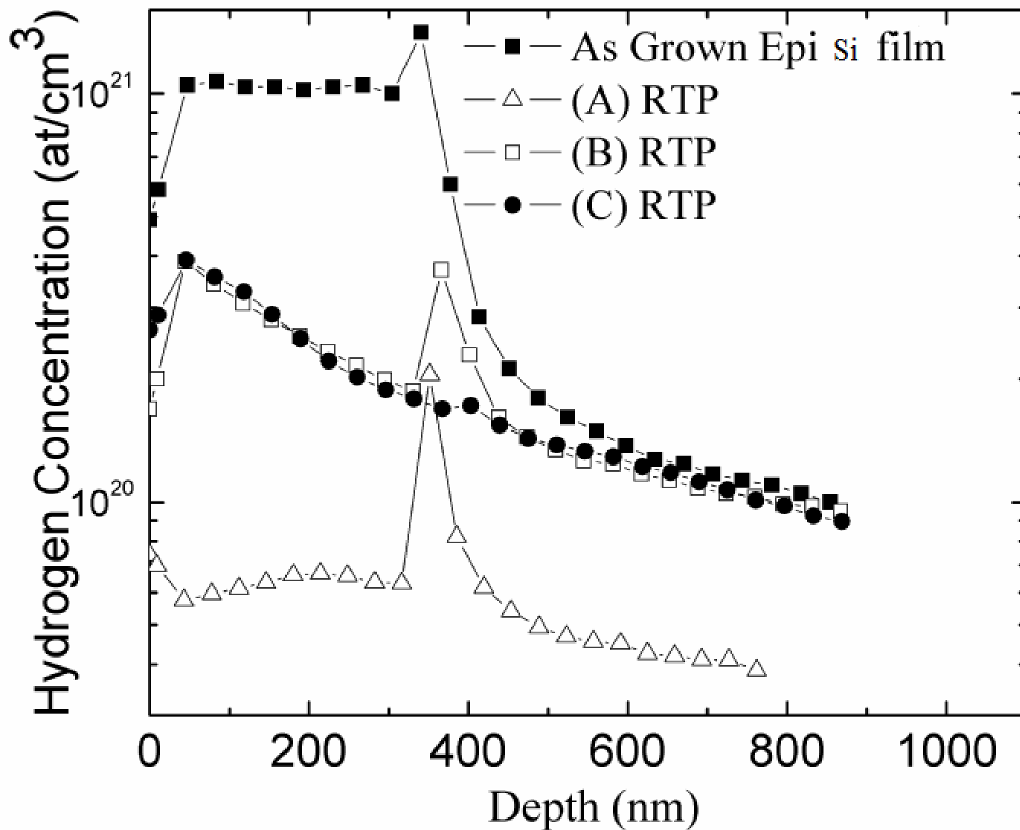


Fig. 3.21: Hydrogen content of the as grown epitaxial Si emitters and under different selected RTP profiles, (EP1 deposition conditions were used).

3.9.4 Structural analysis of the annealed films

3.9.4.1 HRTEM analysis

As we discussed in the previous sections, we developed a very high quality single crystal epitaxial emitters using LT PECVD. Figure 3.22 shows the cross-sectional HRTEM micrographs of Si/epitaxial emitter interface and the fine structure of the bulk after applying (A) RTP profile. It is notice that, after applying the (A) RTP profile, a change in the structure occurred near the interface region towards the internal bulk of the epitaxial emitter as seen in Figure 3.22. A slight mismatch between the single crystalline substrate and the first layers of the epitaxial emitter was detected at the interface after applying (A) RTP temperature profiles as shown in HRTEM micrograph. Due to this mismatch in this defective layer near the interface, the defect density increased and resulted in more recombination centers at the interface on the one hand. On the other hand, the atomic lattice structure in the bulk of the epitaxial emitter was highly defective after applying the (A) RTP, which might be related to the strong hydrogen effusion from the bulk and the interface of the emitter, and this mainly due to the very high heating and cooling rates.

Fig 3.23 shows the cross-sectional HRTEM micrograph of epitaxial emitter/Si interface and the fine structure of the bulk after applying (B) RTP profile. The atomic lattice structure in the bulk and at the interface of the epitaxial emitter is shown in Figure 3.23 after applying (B) RTP profile. While, the epitaxial emitter is annealed under relatively long time using the (B) RTP profile the structure quality is almost the same as the original epitaxial emitter. The amount of the hydrogen evolved from this epitaxial emitter under the (B) RTP profile is much less than the (A) RTP profile.

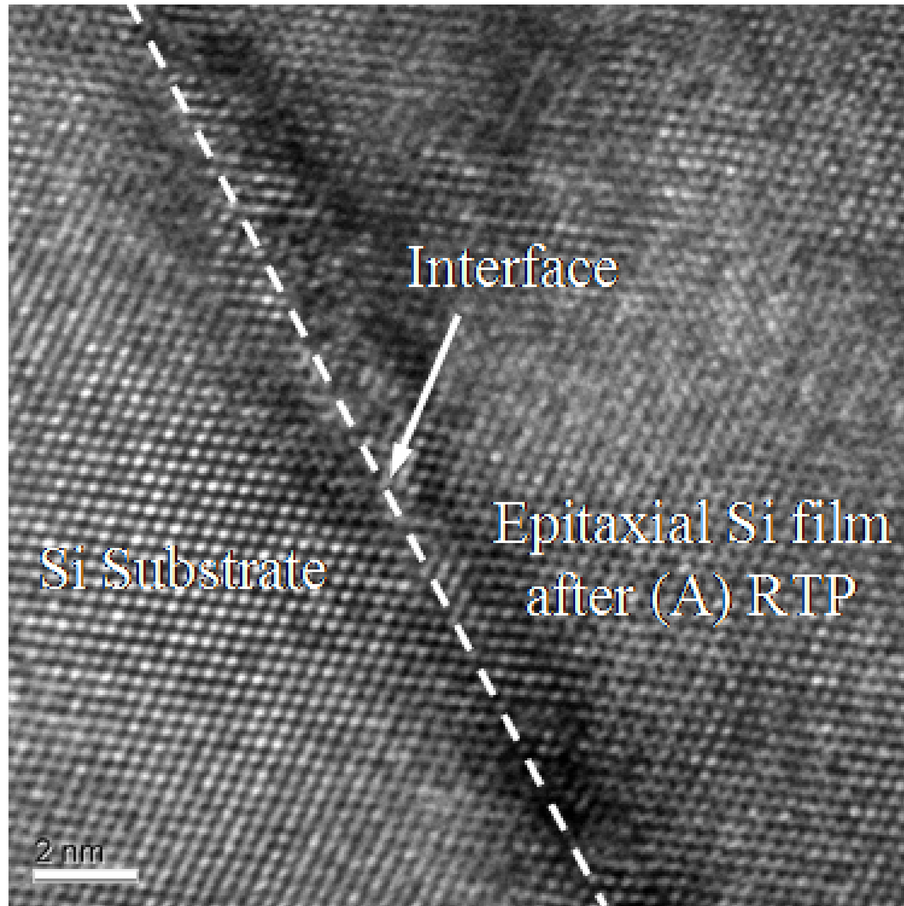


Fig. 3.22: Cross-sectional HRTEM micrographs of epitaxial emitter/Si interface and the fine structure of the bulk after applying (A) RTP profile.

So, applying a very long thermal stress at 400°C for 10 min did not have a big effect on the interface quality as well as on the bulk structure of the epitaxial emitter as seen from the HRTEM in Figure 3.23. We noticed that the bulk quality is comparable to the original epitaxial emitter without applying any RTP process.

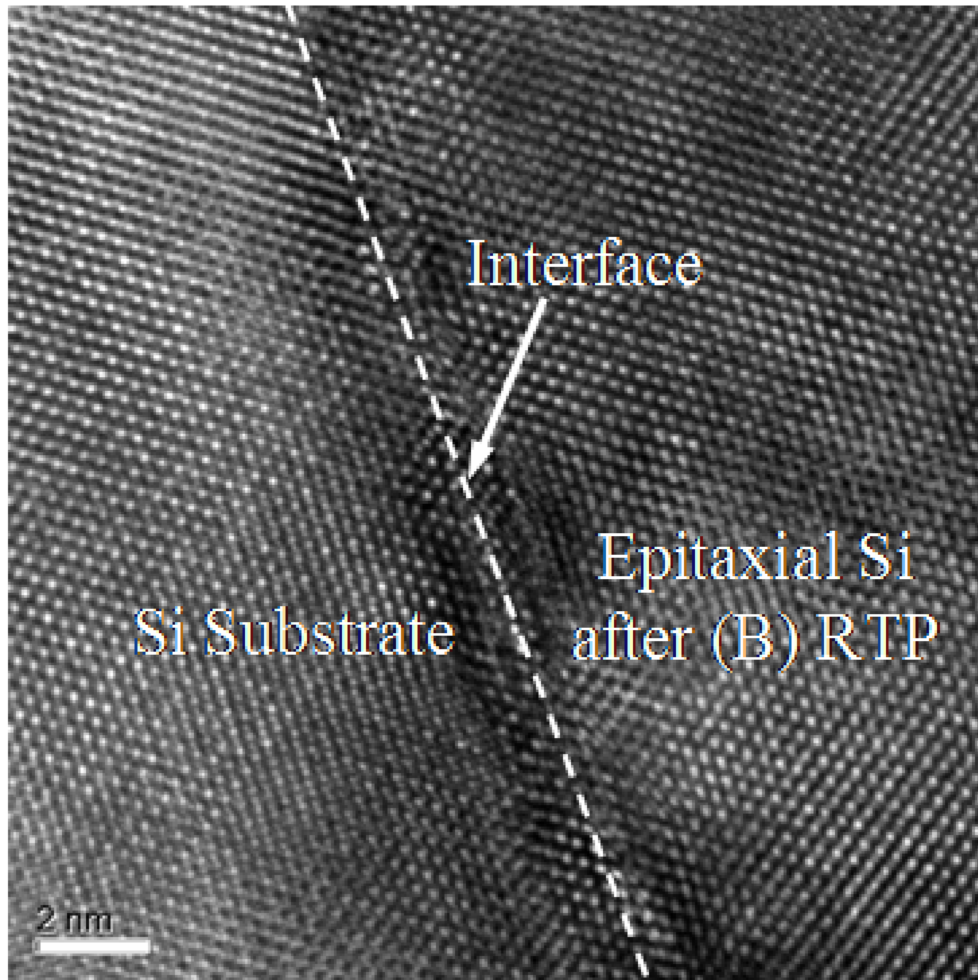


Fig 3.23 Cross-sectional HRTEM micrograph of epitaxial emitter/Si interface and the fine structure of the bulk after applying (B) RTP profile. (scalbar=2 nm).

Figure 3.24 shows the cross-sectional HRTEM micrograph of epitaxial emitter/Si interface and the fine structure of the bulk after applying the (C) RTP profile. Very low heating and cooling rates were applied in the designated temperature profile combined with the annealing at 850°C afforded a better chance for the bulk structure, as well as the first epitaxial layers to be enhanced at the interface as seen in Figure 3.24. Therefore, the atomic lattice structure of the epitaxial emitter is well arranged without any noticeable dislocation or bulk defects.

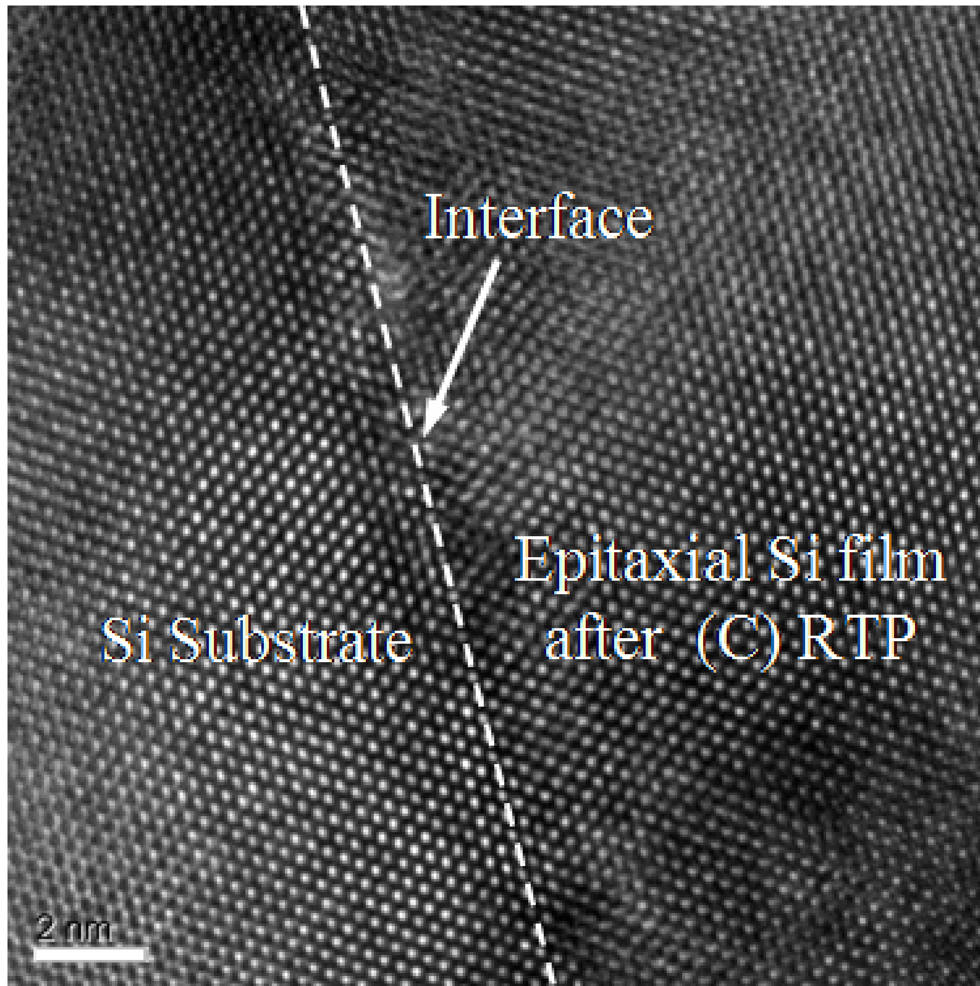


Fig 3.24: Cross-sectional HRTEM micrographs of epitaxial emitter/Si interface and the fine structure of the bulk after applying (C) RTP temperature profile.

3.9.5 Electrical properties of the annealed films

We applied the optimized rapid thermal annealing process on the developed epitaxial grown films which that was obtained using EP1 process conditions. Figure 3.25 shows the free carrier concentration measured by SRP technique for the epitaxial silicon films deposited at 300°C, 91.6 % HD, before and after applying (C) RTP, (EP1 deposition conditions were applied). We used (C) RTP

temperature profile which has very low heating and cooling rates compared to the other developed temperature profiles.

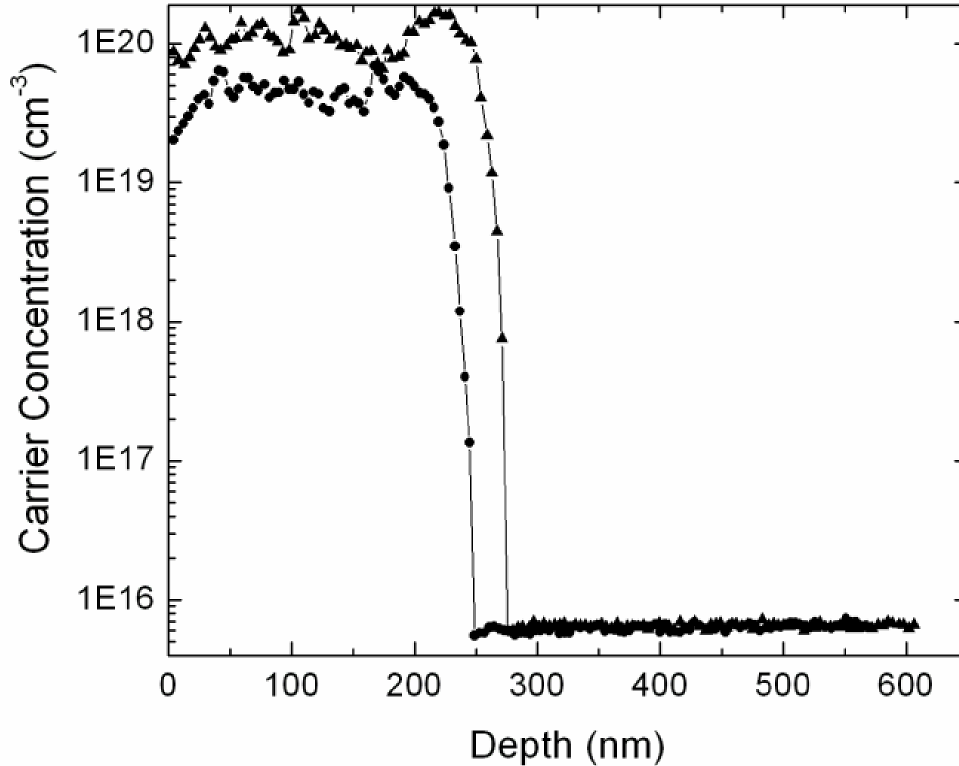


Fig. 3.25: Spreading resistance profile for the free carrier concentration of epitaxial silicon films deposited at 300°C, 91.6 % HD, before and after applying RTP (C), (EP1 deposition conditions are applied).

Applying RTP for 60 sec at 750°C on the developed epitaxial films dropped the resistivity slightly to 7.6 x 10^{-4} Ω cm (almost one order of magnitude). The sheet resistance of the developed epitaxial film after RTP annealing process is 38 Ω □. Moreover, the doping efficiency η_d was significantly enhanced by 10~20 % by applying RTP for 60 sec at 750°C using (C) RTP temperature profile.

3.10 Summary and conclusions

We developed high quality epitaxial films that can be used as emitters for high quality homojunction solar cells. Hydrogen dilution plays a crucial role in epitaxial growth of highly phosphorous doped

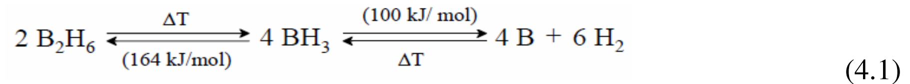
silicon films. The best developed films, in terms of structure and electrical properties, were achieved at intermediate hydrogen dilution regime ~ 91% HD. The deposited silicon films at higher hydrogen regime is more likely to have defective areas, and this can be attributed to the change in the role of hydrogen to etching mode which influences the growth mode and hence the structure of the developed films. Nevertheless, we can not ignore the role of other parameters as substrate temperature, orientation and power density. Obviously, the processing conditions for the epitaxial growth at low temperature in PECVD system must be optimized to find suitable recipes and the best combinations between the different processing parameters. It is clear that by changing the substrate temperature and keeping the other parameters unchanged, the conductivity of the developed epitaxial films gradually degraded especially for temperatures lower than 150°C. This result was confirmed by HRTEM analysis for the films developed at nearly room temperature (by keeping the processing conditions without changing for EP1). Not only the substrate temperature but also the substrate orientation has its influence on the epitaxial growth. We found that the best substrate to promote epitaxial growth is (100) orientation substrate over the other orientations which was confirmed by different analysis such as HRTEM, SRP, and micro Raman. To tackle the issue of low quality films, due to substrate temperature, orientation and/or other processing parameters, we applied low thermal budget RTP technology to enhance the structure, and hence the electrical properties of the developed films for photovoltaic devices. Different RTP temperature profiles were tested. It was evidently noticed from the extensive analysis that the temperature profiles, with low heating and cooling rates, were more beneficial to the annealed films.

Chapter 4: Experimental work: Development of LT PECVD boron doped (TMB) Quasi-Epitaxial Si films

Introduction

Epitaxial growth of heavily boron doped layers at low temperature is a promising area for thin film solar cells. It can yield high conductive layers due to the expected high doping efficiency. The values of room-temperature conductivities for boron-doped silicon films are one order lower than those of phosphorous-doped silicon films. It is very challenging to obtain high boron doping concentration with high crystallinity for the samples prepared by PECVD system, where the films become amorphous at boron concentration in the order of 10^{20} cm^{-3} [125]. Furthermore, for the PECVD samples, the boron doping efficiency is also very low (10–20%) [126]. Therefore, the highest conductivity reported for p-type nc-Si:H prepared by PECVD is only around 10 S/cm [127]. Meanwhile, there are conflicting requirements for p type thin film layers. For example, the layer conductivity increases considerably with thickness due to the development of crystallinity with film thickness, i.e. an incomplete crystalline structure at the substrate/film interface [128, 129]. The requirements for a good boron doped layer suitable for solar cell application are quite rigorous. These layers must be (i) thin (low absorption), (ii) highly conducting and (iii) sufficiently crystalline to promote acceptable electrical properties suitable for solar cell applications. Thicker p-layers will be less transparent, and the adverse effects of the high levels of boron doping on the development of crystalline structure. Thus the thickness, crystalline structure, and conductivity of the developed films should be optimized while the absorption in the p-layer should not be too high. The reason for selecting Trimethlyboron (TMB) as the main dopant gas source for the prepared films is that there are still fundamental problems in particular when B_2H_6 diborane (DB) is used. In this case, an excess of deep defects is created in the doped silicon films, and it is very difficult to master the doping in a

systematic way, because of the thermal instability of the diborane [130-132]. However, the density of the deep defect states introduced by B doping is appreciably reduced when using TMB instead of DB, especially at high doping levels. This accompanied by an increase of the optical gap for the same B/Si ratio in the gas phase which can be tentatively attributed to the carbon incorporation by CH_3 radicals [133]. Another issue with B_2H_6 is its low thermal stability (decomposition energy of only 164 kJ/mol). Furthermore, the source-gas B_2H_6 also underlies the self-decomposition within the gas bottle leading to the formation of molecules with higher boron coordination during storage that appear as powder. Diborane B_2H_6 underlies a reversible equilibrium (Eq 4.1) that shows decomposition to boron as well as the reverse reaction, under the applied working conditions.



(4.1)

The chemical thermolysis reaction of B_2H_6 to BH_3 is initiated at elevated pressure and temperatures (> 300 °C without plasma) and then keeps on reacting directly to boron (B) and hydrogen (H_2) [134]. The back reaction also needs an initiation energy (100 kJ/mol) which can be supplied by the plasma. Thermally initiated boron contamination, even without any plasma, has to be presumed at all hot spots (> 100 °C) in the system. So, in our processes we select Trimethylboron ($B(CH_3)_3$) (TMB) as the boron doping gas owing to its thermal stability, less toxic properties compared to diborane, and the previously mentioned advantages. In this chapter, we will focus on the development of boron doped layers for single junction solar cell structure. Microstructural analysis in atomic scale will be investigated in detail using HRTEM and micro-Raman analysis. Chemical composition, dopant activation and the electrical properties will be characterized and investigated. The developed films will not only be used as an emitter in a p^+n single junction solar cell but they will also be used as a back surface field (BSF) layer in n^+pp^+ structure that can enhance the efficiency of the fabricated

devices (will be discussed in chapter 5). Different processing parameters such as HD, the applied power density, and the optimized RTP process will be investigated and analyzed in detail.

4.1 Development of LT-PECVD quasi-epitaxial boron doped Si films

Series of experiments were carried out by systematic variations of the deposition parameters like power density, SiH_4 gas flow concentration, processing chamber pressure and HD. Meanwhile, we will apply the optimum processing conditions used for the development of phosphorous doped films (EP1 at 90.16% HD), which will shed some light on the dopant gas influence on the structure and the electrical properties of the developed films. Detailed deposition parameters are listed in Table 4.1. It should be mentioned that these investigations were performed on quite relatively thick films to have a wide investigation window range on the structure and the electrical properties of the developed films. The low temperature PECVD p-type silicon films were deposited on one sided polished n-type silicon wafer, (100) oriented of 1-2 Ω cm resistivity. Process 2 was applied at intermediate hydrogen dilution and low pressure regimes (HD=90.16 % and 0.4 Torr, respectively). Please note that, this is the same deposition conditions used for the development of the phosphorous doped epitaxial silicon films discussed in chapter 3 (EP1). This will give us a good opportunity to compare between the two films under exactly the same deposition conditions except that for this process the boron was used the doping gas. High resolution TEM is used to analyze the structure of the developed boron doped films under different processing regime.

Table 4.1: The deposition parameters used for the low temperature boron doped quasi-epitaxial silicon films on (100) n-type Cz wafers.

	c(TMB)*=F(TMB)/F(SiH_4)	Hydrogen Dilution (%)	Power density (mW/cm^2)	Pressure (mTorr)	Temperature (^oC)
Process 1	2.0	97.02	47	900	260
Process 2	0.4	90.16	47	400	300
Process 3	0.6	99	70	900	260
Process 4	1.0	96.66	47	400	300
Process 5	0.5	90.1	11.75	400	260
Process 6	2.0	99	70	400	300

*c(TMB)=F(TMB)/F(SiH_4); where F denotes the flow of respective gases

We selected another processing regime, process 1, to investigate the influence of different processing parameters, such as lower processing temperature (260°C), high HD regime 97.01% and low silane concentration on the structural and electronic properties of the deposited films. Meanwhile, the mass flow rate of the doping gas (TMB) is kept constant and the silane flow changed depending on which process is used, leading to the change in the ratio of TMB/SiH_4. The starting material is one sided polished (100) n-type Si substrate, with resistivity of 1-2 Ω cm and about 410-420 μm in thickness. The *ex-situ* cleaning process was applied before wafer loading into the processing chamber. After pumping down to the base pressure of nearly 2-3 x 10^{-6} Torr, the ultrahigh purity processing gases (99.99%) pumped into the processing chamber. The RF power density, chamber pressure, substrate temperature, silane and TMB concentration, were kept at 47 mW/cm^2, 400 mTorr, 300°C, 0.09 and 0.0363 %, respectively, under 90.16 %HD. Process 2 is applied at relatively intermediate hydrogen dilution and low pressure regimes (HD=90.16 % and 0.4 Torr), respectively. The structural analysis at atomic scale using HRTEM will be discussed in the following section.

4.2 Structural analysis of the TMB quasi-epitaxial boron doped films

4.2.1 HRTEM analysis

Figure 4.1 shows high resolution TEM micrographs of a typical boron doped silicon layer deposited under the deposition condition parameters described in table 4.1 for the process 1. HRTEM images confirmed that an epitaxial layer is formed on the crystalline substrate. Fast Fourier transformation (FFT) pattern confirmed that a thin layer of the deposited film has exactly the same structural atomic arrangement as the substrate. It is noticed that, the film is composed of three regions as seen in Figure 4.1 and confirmed by FFT insets; (i) the first region is an epitaxial layer for approximately 12-15 nm thickness starting from the interface between the substrate and the deposited film. This layer has the same inter-atomic structure as (100) silicon substrate, especially near the interface as confirmed by high resolution micrographs in Figure 4.1. Structural defects such as twins, stacking faults and mismatch between the different inter-atomic layer structures appear between 8-10 nm regions leading to the breakdown of the epitaxial structure region and the appearance of a second region (ii), the transition region. In the second region, the periodic lattice fringes terminate in FFT insets, which indicate the existence of amorphous-crystalline interface structure.

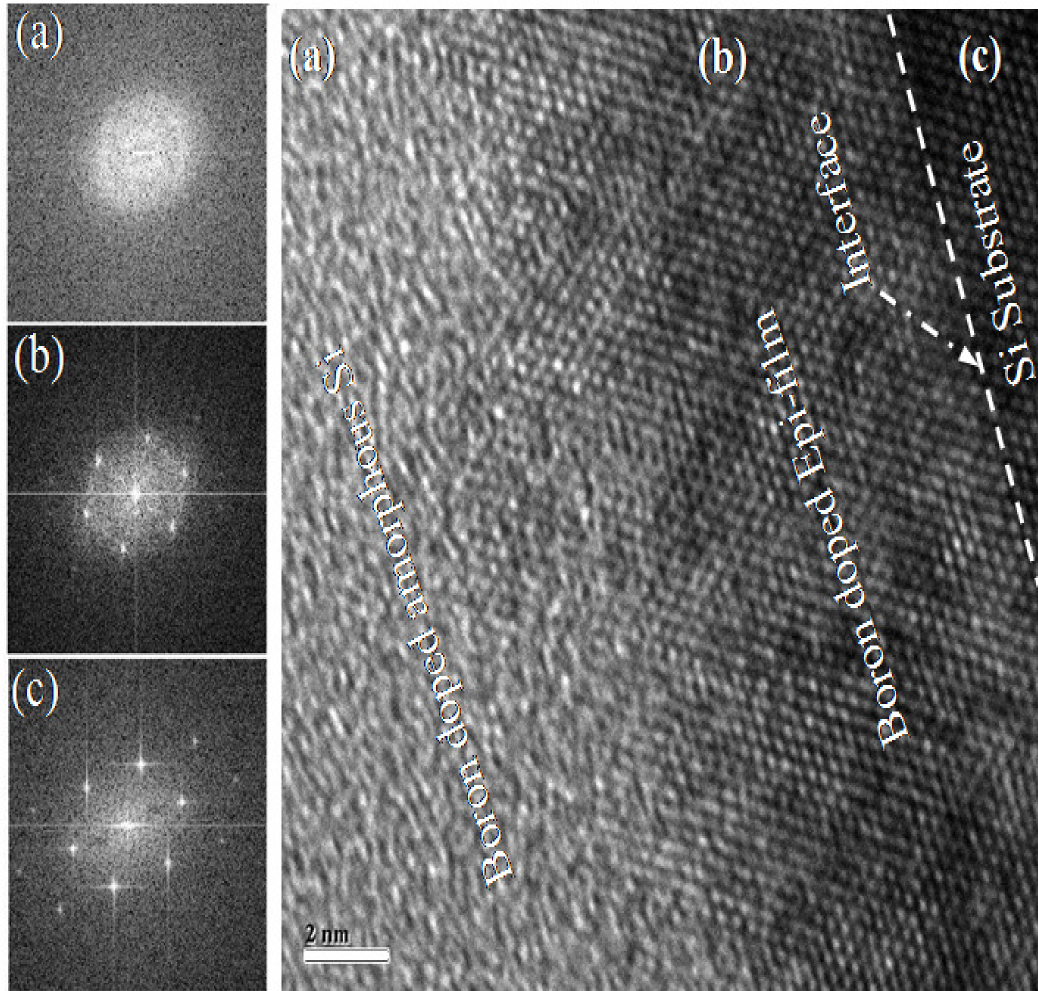


Figure 4.1: Bright Field micrograph of a very high resolution TEM Cross-Sectional image using process 1, deposition conditions as follows, 97 % HD, 900 mTorr, 47 power density and 2 of c(TMB) at 260°C, inset FFT for the different areas of interest (a) the amorphous phase, (b) the epitaxial interface and (c) the crystalline silicon substrate.

This termination takes place at nearly the same thickness from the substrate, yielding an abrupt transition from epitaxial to amorphous phase, (iii) A mixture of crystalline structure separated by amorphous silicon areas is the main feature of the third region in which a completely amorphous phase is noticed as seen from both low and high resolution HRTEM micrographs in Figure. 4.1 and the FFT inset images. This result coincides with the different research groups where at low deposition

temperatures the maximum thickness of the epitaxial films is limited. Jorke et al. [135] and Eaglesham et al. [136] showed the existence of a critical epitaxial thickness h_{epi} even in MBE-epitaxy beyond which the growth mode changed from crystalline to amorphous; this was also shown in ECR-CVD [137]. Different models have been proposed to explain the limited epitaxial thickness at low temperature; (a) Defect accumulation model, in which a defect accumulation picture for the breakdown of epitaxy would involve a continuous build up of lattice disorder during low-temperature growth until eventually the amorphous phase forms, (b) Roughing model, in principle roughness could limit crystallinity either energetically or kinetically where the accumulation of surface energy until the crystalline phase becomes thermodynamically unstable, and (c) Impurity segregation model where segregation of a background impurity to some critical surface coverage is an obvious possible mechanism for limited thickness epitaxial. Other potential explanations of breakdown other than surface roughening in CVD epitaxy processing have been suggested by Thiesen et al. [138] who proposed that H build up in the film bulk leads directly to the breakdown. Platen et al. [139] implicate the build up of both bulk hydrogen and strain in the breakdown of CVD-grown films. To date, the few CVD experiments that focused on the mechanisms of epitaxy have not conclusively determined the cause of breakdown. In our process, we can not ignore the incorporation and influence of the dopant gases on the promotion and/breakdown of the epitaxial growth. If we compare the results of HRTEM micrographs for phosphorous doped epitaxial silicon films (discussed in chapter 3) and the one for the TMB boron doped films under the same deposition conditions, we will find that the incorporation of the boron dopant gas has its impact on the promotion of the amorphous phase through the early formation of isolated conically shaped amorphous regions rather than the epitaxial growth. The structural analysis of the process 2 is characterized by using HRTEM under the same characterization conditions as the films developed using the process 1. An epitaxial growth is confirmed in this processing regime as confirmed in the high resolution HRTEM micrographs as

presented in Figure 4.2 and the FFT insets therein. The epitaxial thickness (t_{epi}) is almost equal to the thickness of process 1. Teeth like structure were noticed using process 2. Obviously this is due to the high silane concentration for process 2 which is 4 times more than the amount used in process 1. The availability of SiH_4 precursor in the processing chamber leads to a high deposition rate 7.65 nm/min for process 2 (double the deposition rate in the process 1, 3.8 nm/min). This relatively high deposition rate combined with the 90.1% HD regime used in process 2 could not afford a suitable etching rate for the defective deposited Si-Si bond in the developed film [140]. This leads to the creation of a teeth like interface between the epitaxial layer and the amorphous leading to a breakdown of the epitaxial phase, and transform it into a completely amorphous structure. Hence, for high quality epitaxial growth of TMB boron doped layers, from structure point of view, it is better to use a low flow rate of both TMB and SiH_4.

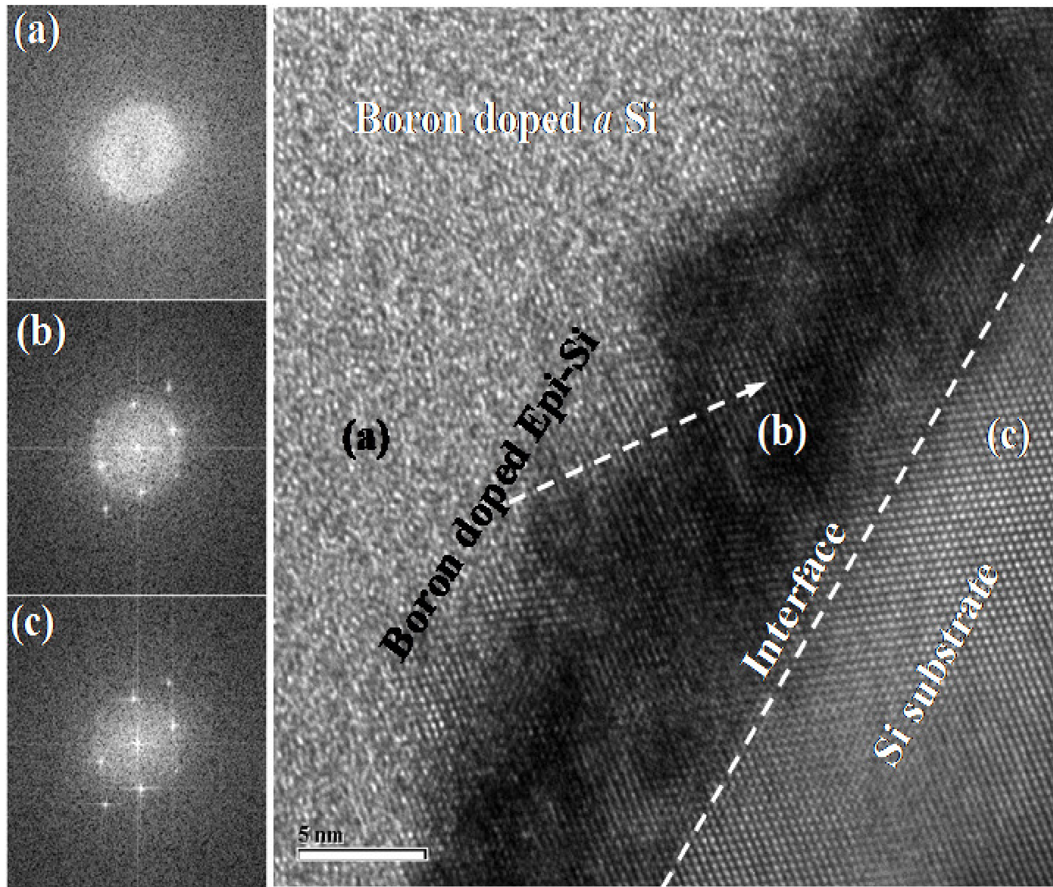


Figure 4.2: Bright Field micrograph of a very high resolution TEM Cross-Sectional image using process 2 deposition conditions as follows, 90.16 % HD, 400 mTorr, 47 power density and c(TMB)=0.4 at 300°C ; (Note: the teeth like structure), with FFT for the different areas of interest (a) the amorphous phase, (b) the epitaxial interface and (c) the crystalline silicon substrate.

4.2.2 Micro-Raman analysis

The structure analysis of the selected processing regimes, process 2 and 3, are characterized using micro-Raman spectroscopy. Both films are deposited on crystalline n-type silicon wafers (100). For process 2 and 3, a thickness of 67 and 23 were deposited respectively, and used for this analysis. For amorphous silicon a significant decrease of penetration depth is expected compared to the crystalline silicon. So, to avoid the thermal or crystallization influence on the samples due to laser irradiation, the excitation power on the samples was kept below 0.26 mW/cm^2 [141]. Figure 4.3 shows the micro-

Raman measurements of the deposited quasi-epitaxial TMB boron doped silicon films for process 2 and 3. A pronounced peak appeared near the characteristic peak of crystalline silicon by using process 3 deposition conditions. This has a perfect indication about the role of hydrogen in the film development. At this high hydrogen dilution regime, the etching process of the weak Si-Si bonds by hydrogen is the dominant process. The process left the strongest deposited films on the substrate and etched away the weaker spots. The Raman peak for crystalline silicon (c-Si) is sharp and nearly Lorentzian band centered at 520 cm^{-1} with a full width at have maximum (FWHM) of about 3 cm^{-1} [142]. It is noticed that, the characteristic peak for the crystalline silicon is presented here in the measurements shown in Figure 4.5 centered at 517.0 cm^{-1} and shifted by 3 cm^{-1} wave number. The quasi-epitaxial fraction (X_c), the crystalline part of the film and any other crystalline portion in the mixed phase, could be easily calculated from the integrated intensities of the crystalline and amorphous bands, I_c and I_a respectively in Raman spectra using Eq. 4.2 as follows;

$$X_c = \frac{I_c}{I_c + yI_a} \tag{4.2}$$

where y is the ratio of the Raman efficiencies of crystalline and amorphous silicon [141].

Meanwhile, a broad transverse optic (TO) peak around 476.5 cm^{-1} corresponding to typical amorphous silicon is presented in the Figure 4.3 for process 2. However, an epitaxial layer with thickness between 12-15 nm for process 2 was confirmed using HRTEM analysis. This a contradiction between the measurements of the Raman spectroscopy and the HRTEM analysis, and is due to the collected information from the developed epitaxial film that takes place from the first few nanometers at the surface of the deposited films. The first layers near the surface of the developed epitaxial films are amorphous as shown by HRTEM. Hence, the collected data represents the amorphous Si layers only, where the penetration depth of laser into silicon films depends on the

crystallinity of the film. For amorphous Si structure the penetration depth is less than that of crystalline silicon.

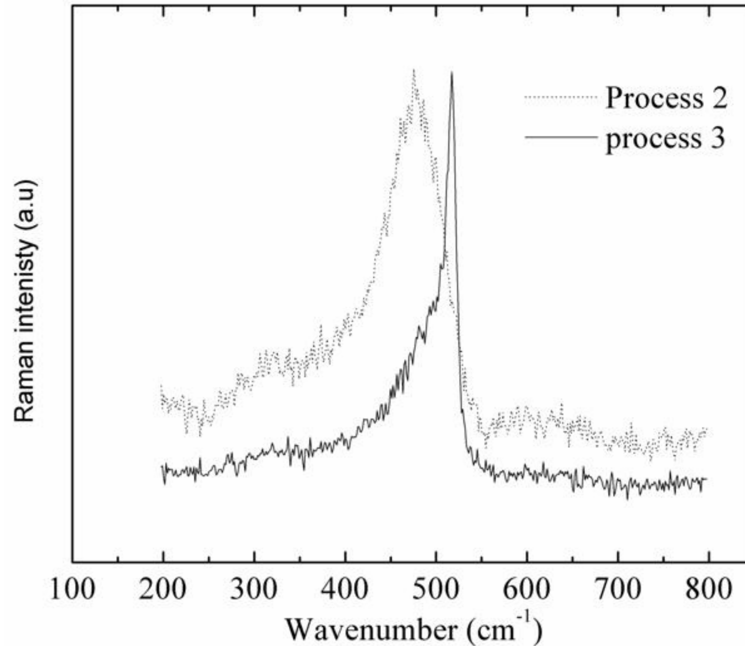


Fig. 4.3 Raman measurements for the selected processes 2 and 3, at 90.16 and 99 % hydrogen dilution, respectively.

4.3 Impurity analysis of TMB boron doped films

Electrical properties of the developed silicon boron doped emitters such as resistivity and conductivity are crucial and have their influence on the efficiency parameters and photovoltaic properties of the developed silicon solar cells. Hence, we will investigate the characteristics of the developed films using spreading resistance profile (SRP). SRP can be used as an indirect method to study the structure of the developed TMB films. In this section, we will study the influence of different deposition parameters on the active dopant concentration, such as hydrogen dilution, the applied power density and the optimized rapid thermal annealing process and its influence on the dopant redistribution and activation. The flow rate of the TMB gas as a dopant source is kept constant for all processes to investigate its influence at very high doping regime under different processing

conditions. So, the value for the TMB concentration presented in table 4.1 depends mainly on SiH_4 gas flow, which varied between 5 to 25 sccm. Relatively thick films have been deposited, up to 200 nm.

4.3.1 Spreading resistance profile analysis

Figure 4.4 shows the measured free carrier concentration using SRP of the two different films processed using two different processing conditions, (process 1 and process 6). Both curves can be divided into three regions; (i) near the interface region (up to 20 nm) with relatively high free carrier concentration of approximately 1.8 $x10^{16}$ and 4.6 x 10^{16} cm^{-3}, for process 1 and 6 respectively. This region revealed that, a quasi-epitaxial layer is created near the interface between 12-15 nm thickness as confirmed by HRTEM micrographs and the fast Fourier transformation (FFT) insets. However, the same TMB doping concentration was used for both processes, but we noticed that the active carrier concentration for process 1 is less than that of process 6. This indicates a good crystallinity of the thin epitaxial layer near the interface for process 6. The power density for process 1 is 47 mW/cm^2 which is less than that of the power density in process 6 (70 mW/cm^2), which ensures that HD and/or the power density are the main dominant controlling parameters that influence the thickness of the deposited quasi-epitaxial layer in this processing regime. (ii) the transition region 15nm < film thickness < 40 nm, the free carriers decreased gradually in both films, where in this region the structure of the deposited films seems to have a mix of nanostructures and amorphous phase. (iii) The third region (completely amorphous silicon layer > 50nm) which has the minimal free carrier concentration. The active free carrier concentration measured is in the region of 10^{17} cm^{-3} as shown in Figure 4.5.

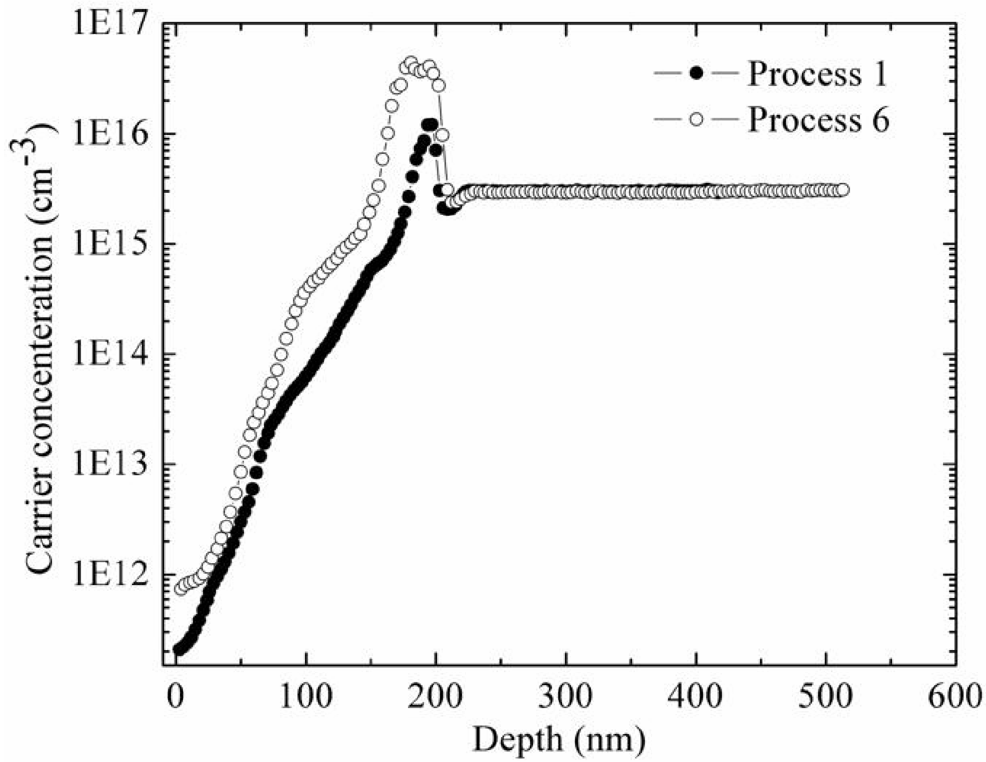


Fig 4.4 Measured free carrier concentration using spreading resistance profile (SRP) of the two different films processed using two different processing conditions, (process 1 and process 6).

The measured resistivity using SRP of the two selected processes 1 and 6 is presented in Figure 4.5 for 210 and 150 nm thick films respectively. It is noticed that, the resistivity of the deposited films using the processing conditions listed in process 1 is approximately 10^{-1} Ω cm, with conductivity of 10 Ω^{-1} cm^{-1}. Due to the relatively low conductivity, the use of the RTP is crucial to enhance the crystallinity of the amorphous layer that appeared after the breakdown of the quasi-epitaxial layer and to activate the boron therein which could yield higher free carriers.

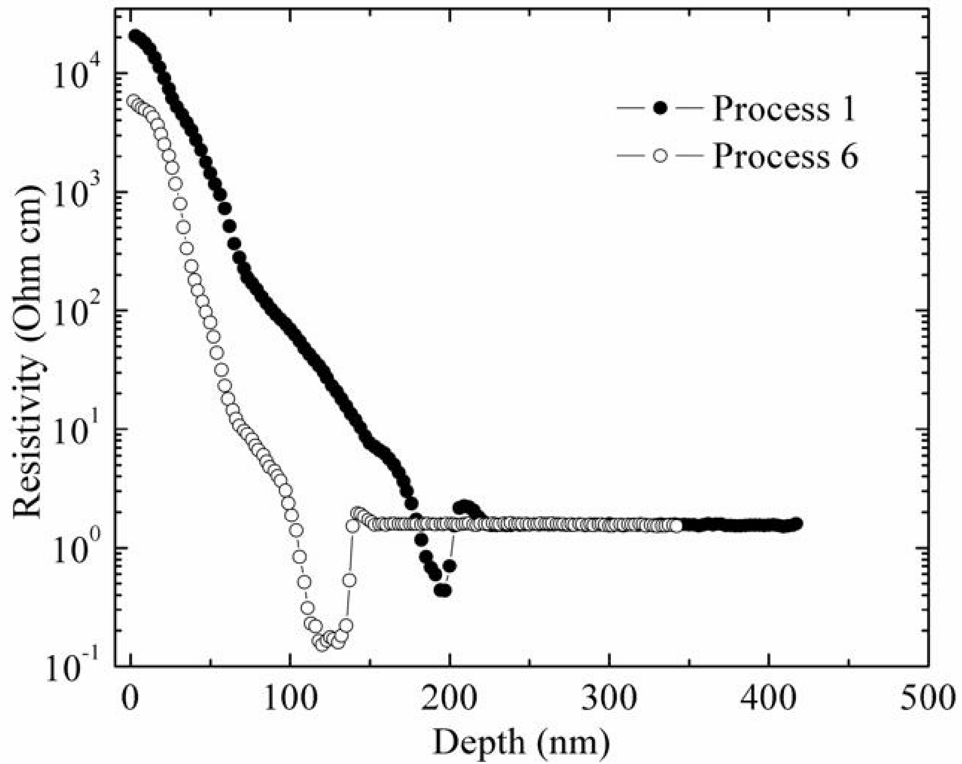


Fig. 4. 5: Measured resistivity using of by spreading resistance profile (SRP) for two different films under two different processing conditions, (process 1 and process 6).

4.3.2 Post-deposition rapid thermal annealing

4.3.2.1 Spreading resistance profile analysis

We used (C) RTP temperature profile that has multisteps heating and cooling, with different heating and cooling rates. The annealing process is applied for 60 sec at 750°C. Figure 4.8 shows the carrier concentration in the developed quasi-epitaxial high boron doped emitters by using processes 2 and 4 deposition conditions after applying the optimized RTP process. The major difference between process 2 and 4 is that, HD is 90.16 and 96.66 % respectively. Interestingly, the annealed boron doped films developed with low 90.16% HD lead to a higher free carrier concentration compared to the one with more 96.66% HD. This result indicates that the more amorphous phase the film has the

higher crystallinity the film will gain after applying the optimized RTP process. It is noticeable that, the annealed boron doped silicon films under process 2 conditions has a uniform and flat distribution of boron depth free carrier profile dopants along RTP annealed film. Moreover, the interface of the annealed boron doped films is very steep after applying the selected RTP temperature profile. The free carrier increased up to 9 $x10^{19}cm^{-3}$ by applying the RTP process. This very high concentration of free carriers through the annealed boron doped films enhances the conductivity and the mobility of the free carriers. The observed higher concentration of electrically active boron compared to the total boron concentration indicates that almost all dopants become incorporated into substitutional positions. We expected a very high doping efficiency by up to 60% for these boron doped annealed films. However, the same annealing RTP profile applied on the boron doped silicon films prepared using process 4 deposition conditions, the free active carriers is less than in process 2, and the distribution of the free carriers is not uniform. Near the interface of the developed films using process 4 followed by the application of RTP, the film has the highest free carrier concentration of approximately $1x10^{18}$ cm^{-3}. The free carrier concentration then started to decrease gradually from the interface with 8 x 10^{16} cm^{-3} towards the surface.

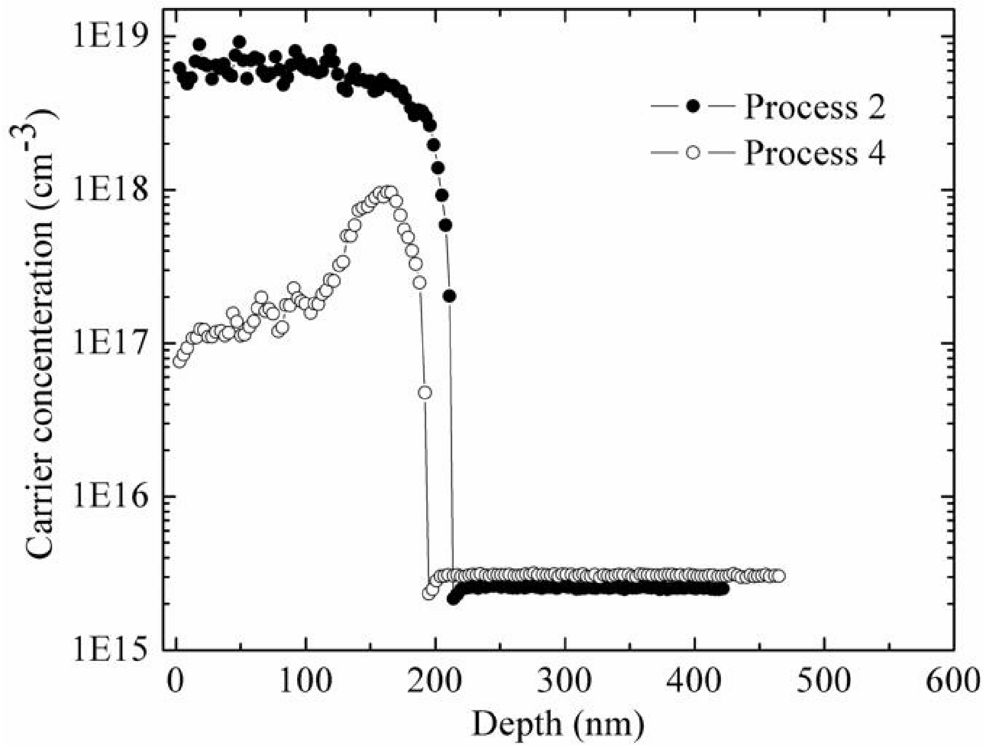


Figure 4.6 Active carrier concentration profiles measured by SRP technique, deposited using process 2 and 4 process conditions, and annealed in RTP for 60 sec at 750°C.

The resistivity of a series of different boron doped silicon films after applying the optimized RTP temperature profile is shown in Figure 4.7. While the resistivity for process 2 is quite uniform after applying the RTP annealing, the resistivity for processes 4, 5 and 6 is not uniform and has the lowest values near the interface. A minimum resistivity of 8×10^{-3} Ω cm is obtained with maximum conductivity value of 120 S/cm for process 5 near the interface.

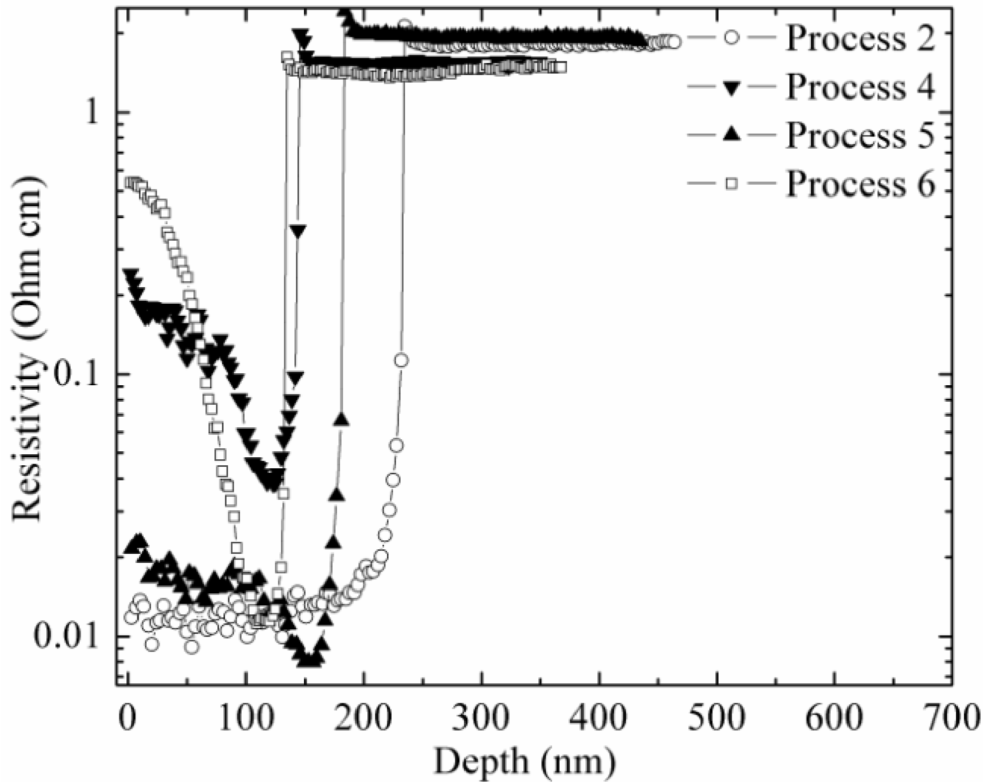


Figure 4.7 Resistivity of the annealed boron doped silicon films using different processing conditions.

4.4 Summary and conclusions

This chapter presented the development of new Si films at low temperature using PECVD and TMB as a dopant source for boron dopant. Quasi-epitaxial boron doped silicon films were developed and characterized using different structural and electrical characterization techniques. Different processing parameters such as the power density, processing pressure, substrate temperature and the hydrogen dilution under constant doping gas flow were used. Microstructural of the developed silicon films were analyzed in atomic scale using HRTEM analysis. It is revealed that the structure consists of an epitaxial layer of up to 15 nm thickness, followed by a breakdown region with mixed zone of amorphous and nanocrystalline structure, and an amorphous silicon phase for the rest of the developed films. Low doping efficiency is noticed for these films due to the breakdown of the

epitaxial growth and the change to amorphous phase. Hence, activation of the dopant using RTP process at moderate temperature is crucial for the developed boron doped films. The free carrier concentration measured using SRP technique increased by up to 9 $x10^{19}cm^{-3}$ after applying RTP annealing process for a very short time (60 sec) at 750^oC. This very high concentration of free carriers through the annealed boron doped films enhances the conductivity and the mobility of the free carriers which achieve acceptable electrical properties for photovoltaic application.

Chapter 5: Experimental Work: Fabrication, and characterization of homo and heterojunction diodes and epitaxial Si solar cells

Introduction

The development of LT PECVD epitaxial growth Si films and the fabrication of homojunction solar cells are key factor for the developing of novel devices with high conversion efficiency. Low temperature process was used to develop the film and the junction realization instead of conventional methods, such as high energy ion implantation and annealing at high temperature to overcome the amorphous layer created on the surface of the substrate. To understand the characteristics of the developed novel homojunction solar cell devices prepared using the epitaxial LT PECVD process, we need a full understanding of the dark current-voltage characteristics. This offers essential information about the solar cell device itself. The properties of the ultra shallow junction formed by epitaxial growth using LT PECVD, its fabrication and analysis will be discussed in detail in this chapter. To the best of our knowledge, the electrical analysis of the ultra-shallow junction prepared using LT PECVD was not achieved or discussed before. This is mainly due to its novel processing conditions under LT PECVD for the high quality epitaxial structure as presented in detail in chapter 3.

In this chapter we will describe the fabrication process of the fabricated homojunction diodes and a full electrical analysis will be presented. Furthermore, the influence of the hydrogen evolution (by applying RTP) on the electrical properties of the fabricated diodes profiles will be described in chapter 3. In addition, a detailed description of the fabrication schemes of the developed epitaxial solar cells using n-type emitters, with and without light trapping schemes, under different processing temperature conditions will be presented in this chapter. We will also investigate the influence of the soft hydrogenation process on the photovoltaic properties of the developed devices. We will use different characterization schemes to characterize the fabricated devices such as the current-voltage,

and the external and internal quantum efficiency. The developed boron doped silicon films which was studied in detail in chapter 4 will be used to fabricate solar cell devices. The photovoltaic properties of these devices and the proposed enhancement techniques will be presented in this chapter.

5.1 Homojunction Diode Fabrication

5.1.1 Processing Conditions and Diode fabrication

In the fabrication of the junction and the device, we will limit the analysis to the homojunction diodes prepared using wet cleaning process without hydrogen plasma treatment. The prepared diodes were fabricated on Cz crystalline silicon wafers of (100) orientation and have a resistivity of 1-10 Ω cm. Highly phosphorous doped epitaxial Si thin films deposition was carried out in one chamber Plasmatherm 790 PECVD system. Process parameters such as precursor gas (SiH_4, PH_3, H_2) flow ratios, chamber pressure, RF plasma power have been varied in several sets of experiments for the development and study of the Si films under different conditions. However, for the diode fabrication we will restrict our fabrication to the EP1 and EP2 processes described in chapter 3.

Four steps will be needed to configure the junction, and each step will need a different processing technique. The first step is the deposition of the optimized silicon thin films by PECVD system. After the cleaning process, a fifteen second HF dip must be followed just before loading the wafers into PECVD system to decrease the risk of formation of the native oxide on the wafer surface. The wafers are immediately dried using nitrogen gas and then loaded into the PECVD system at 130°C. To minimize the contamination of the substrate, a very fast evacuation of the particles from the PECVD chamber took place directly after loading the sample. PECVD system was bumped down for nearly 3-5 hours to achieve a suitable process pressure of nearly 2 x 10^{-6} Torr. The deposition temperature was slowly increased and stabilized at 300°C.

The second step is the front and back contacts using Al sputtering system under the optimized recipes using MV sputtering systems. The thickness of the sputtered Al is between 1.5-2 µm. The sputtering of Al was started after reaching 10^{-6} Torr which enabled a pure Al metallization without any contamination from the processing chamber. The optimized Al metallization parameters that were used are; DC power of 250 W, processing chamber pressure of 10-15 mTorr, and Argon flow of 50 sccm. The third step is the patterning of the front Al metallization using lithography. Wet chemical Al etching was applied to etch the exposed Al areas. Hence the metallization of the diode is protected by the front and back positive photoresist. The fourth is the isolation of the designed diodes using soft reactive ion etching (RIE) and the optimized recipe to enhance the etching process. The isolation process of the fabricated diodes is done using dry etching by soft RIE Trion system under the optimized etching conditions as shown in table 5.1 (Al used as a mask in the soft etching process).

Table 5.1 the optimized etching conditions using reactive ion etching (RIE) for diodes isolation

DC voltage (V)	Pressure (mTorr)	SF_6 (sccm)	O_2 (sccm)	Etching Rate (nm/sec)
-40 to - 45	50	25	4	8

Different size diodes using designed emulsion mask were prepared on the same wafer for IV fabrication. The diode test structures prepared for IV characteristics and different characterizations as CV is shown in Figure 5.1. These structures were tested for the dark IV using Keithely 4200 semiconductor characterization system with four source-measure units.

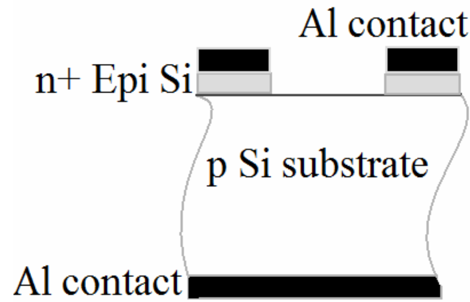


Fig 5.1. Schematic diagram of the prepared LT PECVD homojunction test structure diodes.

We selected two recipes to perform the IV characteristics and these are; EP1 and EP2 (see table 3.2 presented in chapter 3). EP1 presents the processing conditions of the developed epitaxial growth film at 91.16 % HD, and EP2 presents processing conditions of the developed epitaxial films at very high hydrogen dilution 99 % HD. In addition, the RTP process is performed on the developed films after deposition to investigate its influence on the IV characteristics. We selected two of the developed RTP temperature profiles which were presented in chapter 3; the pulsed (A) RTP and the Multi-step Profile (C) RTP using a peak annealing temperature of 750°C for 60s. These two temperature profiles provide a variety of different annealing conditions as we discussed in the previous chapters.

5.1.2 Current-Voltage characteristics of the illuminated diodes

Figure 5.2 shows the dark current-voltage (I-V) characteristics of the diodes fabricated using the following structure; *Al front contact/(n^{+}Si epitaxial film)-EP2conditions /(p) c-Si/Al back*. The diode characteristics under 99% HD (EP2 process conditions) are presented in Figure 5.2. The solid lines and the dashed lines represent the I-V characteristics using the deposition conditions of EP2 without RTP and under RTP process, respectively. Measurements were performed on 2 x 2mm diodes. The uniformity of the I-V characteristics for both kinds of diodes is good as shown in Figure 5.2. The measurements reveal that by applying the selected RTP process at 750°C for 60s improves the ideality

factor of the diodes. We noticed that there were no significant changes related to the hydrogen evolution from the film.

Table 5.2 lists the double diode model parameters of the first and second diode, for the epitaxial films and after applying the selected (C) RTP temperature profile.

Table 5.2: Diode parameters using EP2 process conditions and after applying selected RTP (C) temperature profile.

	First Diode		Second diode	
	J_{01} (A/cm^2)	n_1	J_{02}(A/cm^2)	n_2
Epitaxial under EP2 conditions	3.31x10^{-10}	1.16	2.65x10^{-8}	1.93
RTP (C) profile	2.01x10^{-10}	1.00	1.13x10^{-8}	1.71

The ideality factors of the as deposited diode in low forward bias and medium forward bias regions are 1.93 and 1.16, respectively. Improvements of the ideality factor after applying the selected (C) RTP temperature profile especially for the first diode was noticed. This result suggests that the annealed films should result in solar cells with a higher fill factor. A slight change in the saturation current was observed as well after applying the selected RTP temperature profile. An improvement in the ideality factor but not much improvement in saturation current of the diodes can result in the losses in the open circuit voltage (V_{oc}) of the fabricated solar cells. As a result, the annealing can improve the fill factor but reduce the V_{oc} of the developed solar cells.

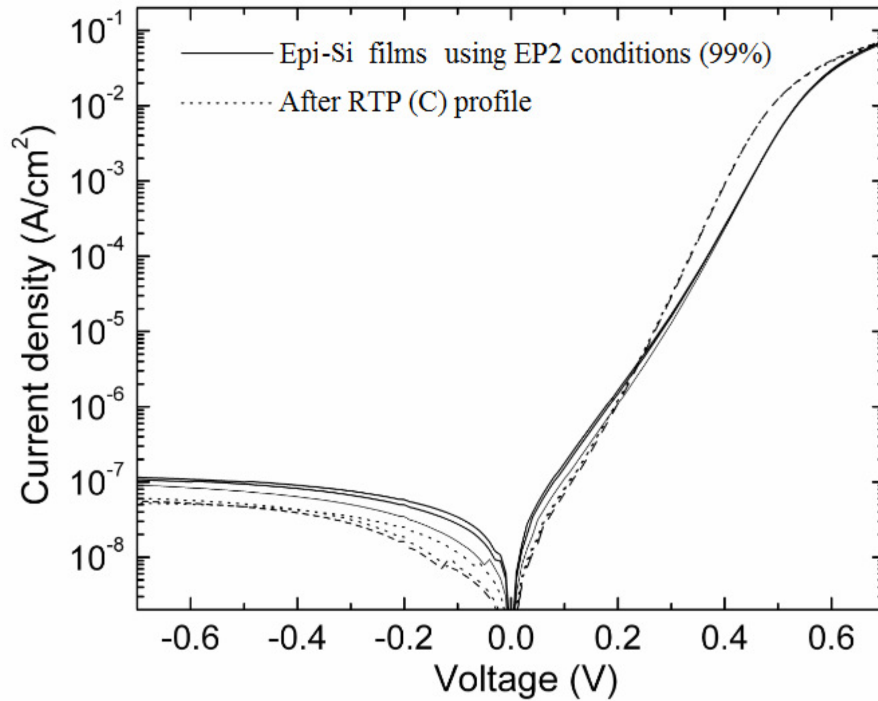


Fig 5.2 I-V characteristics of the *Al front contact/ (n^+Si epitaxial film)-EP2 conditions / (p) c-Si/Al back contact* structure with the as deposited films.

Figure 5.3 shows the I-V characteristics of the fabricated diodes using the *Al front contact/ (n^+Si epitaxial film)-EP1 conditions / (p) c-Si/Al back contact*. The uniformity of the I-V curves is very good, especially for the as deposited epitaxial diode structures, without applying RTP annealing process. However, some of the annealed diodes show a little leaky I-V characteristic. This is due to the fact that the annealing process by the applied (C) RTP temperature profile creates some pinholes resulting from the hydrogen evolution from the epitaxial structure under the EP1 processing conditions. However, on the other diodes structures, the annealing process using (C) RTP temperature profile enhances the ideality factor.

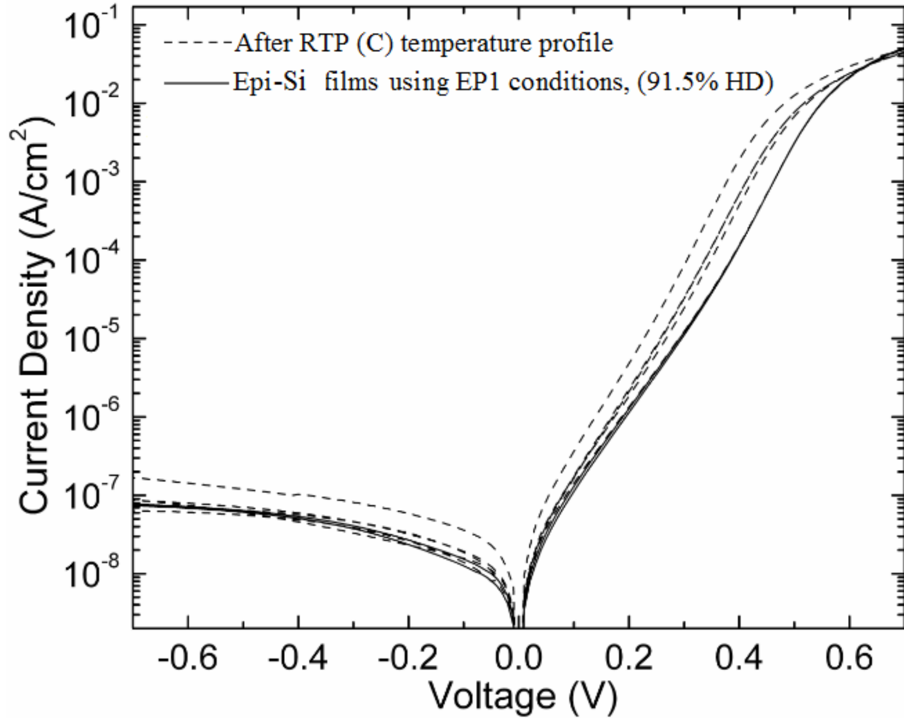


Fig. 5.3 I-V characteristics of the *Al front contact/ (n^+Si epitaxial film)-EP1 conditions / (p) c-Si/Al back contact* structure with the as deposited films.

5.1.3 High Frequency Capacitance-Voltage Characterization

Deep Level Transient Spectroscopy (DLS-83D) system, with high frequency 1.0 MHz has been used to characterize the capacitance-voltage of the prepared diodes. The diode area of 4 mm^2 and 50 nm thickness is used for this measurement. The influence of the RTP temperature profiles is shown in Figure 5.4, where we used two annealing processing profile (A) RTP and (C) RTP. The relationship between the capacitance and applied voltage is shown in Figure 5.4. The built in potential can be determined by the interception point of the W^{-2} (where W is the depletion width) and voltage curve. We found that this value was equal to 0.74 V for as-deposited epitaxial grown films, for the annealed diodes the built-in potential was much higher and was nearly 0.89 (see Figure 5.5). The built in

potential for the annealed films by (A) RTP is comparable to the built in potential of an *n+p* homojunction. This is indicate that there is no density of charged traps at the interface

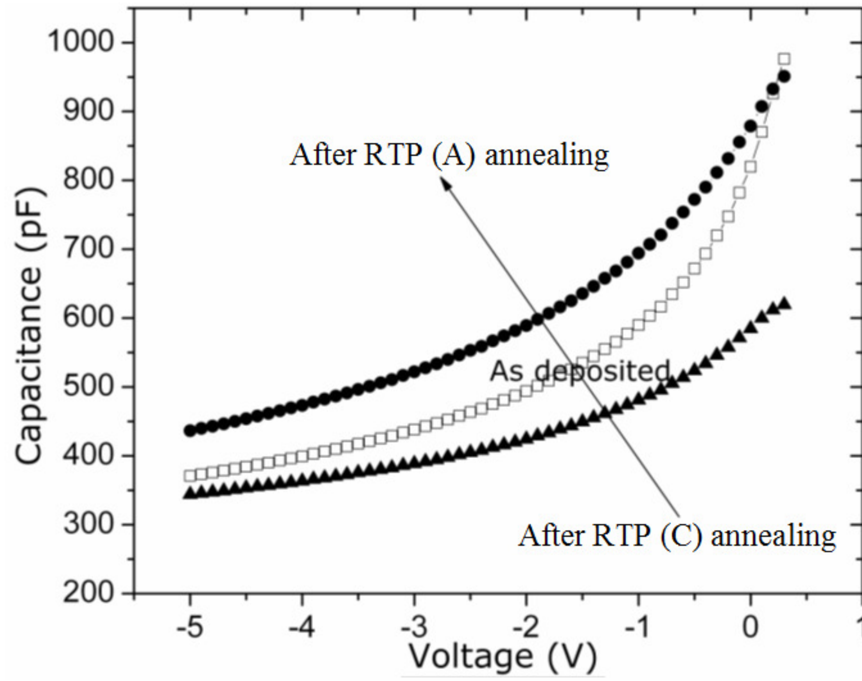


Fig 5.4 High frequency, capacitance-Voltage characterization of the fabricated 4mm^2 diodes using the epitaxial films under EP1 processing conditions and after applying RTP (A) and (C) temperature profiles. (film thickness = 50 nm).

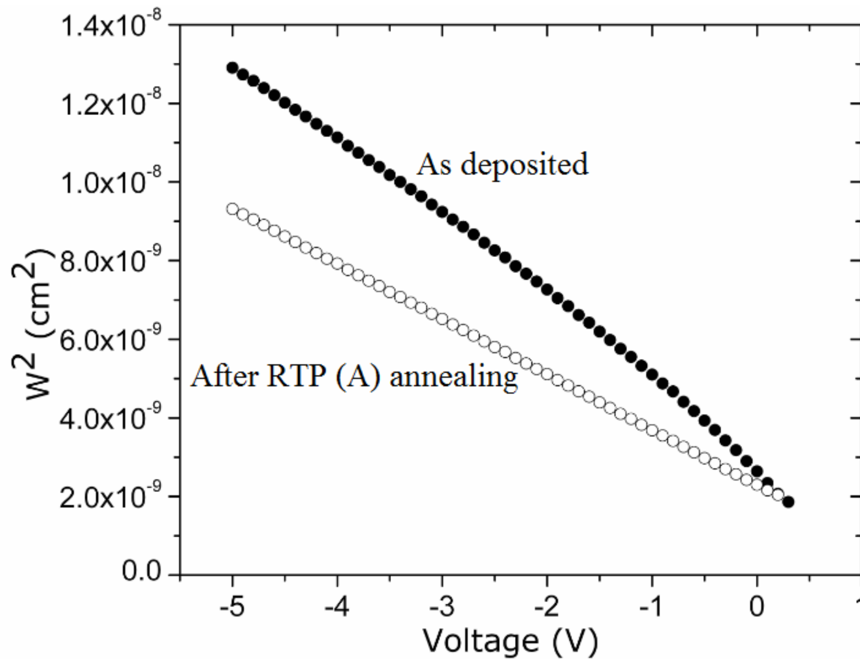


Fig. 5.5: Relationship between W^2 and V for n^+Si epitaxial films / p-type homojunction using process conditions EP1 for as deposited and after applying RTP (A), (film thickness = 50 nm).

5.2 Epitaxial Si Solar cell fabrication

The promising IV characteristics of the fabricated diodes using the developed LT PECVD epitaxial growth films shed some light on the high quality of the developed material and encouraged us to use it as an emitter for a novel device (epitaxial cells) under different processing and fabrication conditions. In the next sections different conditions such as planar surface, textured surface, different emitter thickness and at different temperature will be studied in detail. In the following section, we will discuss in detail the fabrication routes to realize devices using the developed epitaxial films.

5.2.1 Anti-reflection coating and passivation schemes

To enhance the absorption of the incident photons on the fabricated solar cell devices, antireflection coating should be used to decrease the reflection from the surface and to passivate the upper layers. Thermal silicon dioxide is very effective in the passivation of the diffused Si surfaces and deposited

silicon thin films. However, there are issues arising from the high temperatures during the thermal oxide growth that can severely degrade the bulk carrier lifetime. Hence, in recent years, significant efforts have been devoted to the development of low temperature surface passivation schemes as an alternative to the high temperature oxidation of Si. The most successful of these approaches turned out to be the plasma enhanced chemical vapor deposition PECVD of silicon nitride (SiN_x:H). So, in our process, a low temperature SiN_x:H films were used as passivation and antireflection coating films at low temperature. Recently, SiN_x:H was found to be very essential in this application because it can accomplish multiple functions, such as eliminating several additional process steps in the fabrication of high-efficiency solar cells. In a typical commercial solar cell processing sequence, a thin layer of silicon nitride is deposited on an *np* junction by a PECVD process. A nitridation process also produces an accumulation of positive charge at the SiN_x: H-Si interface that helps in surface passivation. Furthermore, it introduces H into Si, which resides within a thin plasma-damaged surface layer. The multipurpose role of nitride demands a low-absorption anti reflection coating (ARC), serve as a barrier layer for control in metallization, and promote favorable electronic processes that can passivate the surface, as well as the bulk, of the device. It is imperative that SiN_x:H deposition and processing be designed carefully to optimize optical and electronic properties of the solar cell. Meanwhile, the full deposition and fabrication process can be achieved at low processing temperature $\leq 300^oC$. Two deposition schemes were selected to deposit SiN_x:H, hence the consequences of the fabrication will be different accordingly; (i) the continuous deposition of SiN_x:H directly after the growing of the epitaxial n^+ or quasi p^+ emitter in the same deposition run. This will ensure a high interface quality between the developed epitaxial emitter and the deposited SiN_x:H. However, the realization of the fabricated solar cell devices will need two mask process steps. (ii) the deposition of SiN_x:H after the Al metal grid patterning, which may need extra cleaning process after Al front grid patterning (before loading into PECVD chamber). The advantages of this process is that it needs only

one mask process, which add more simplicity for the fabrication process and hence low cost in large scale fabrication. Table 5.3 shows the different SiN_x:H antireflection processes conditions used for cells processing. In the ARC 2 process, the hydrogen content is less than in the ARC 1 which may lead to more amorphous structure and a good passivation for the upper n^+ or p^+ layers. SiN_x:H was deposited on the front sides of the samples in one chamber PECVD system. The gas flow ratio of SiH_4 and NH_3 was varied to achieve a range of different refractive indices, and the deposition duration was varied to achieve the optimum antireflection coating thickness. However, no separate qualitative analysis for the SiN_x:H will be considered here except for the observation and the influence of the deposited films on different fabricated devices under the same conditions.

Table 5.3 Different SiN_x: H antireflection processes conditions used for cells processing.

	H_2 (sccm)	NH_3 (sccm)	SiH_4 (sccm)	Pressure (mTorr)	RF power density (mW/cm^2)	Temperature (^{o}C)
ARC 1	5	50	5	150	20	260
ARC 2	10	60	5	200	14	260

5.2.2 Fabrication schemes for epitaxial silicon solar cells

Figure 5.6 shows the illustration of different routes for epitaxial growth silicon solar cell fabrication on polished and textured surfaces. In this process, a fabricated epitaxial silicon solar cell is defined and have the following structure *Al (front grid)/ SiN_x:H /n^+ epitaxial Si /p-type Cz/ Al (back contact)*. For the epitaxial cells fabricated on a polished planar silicon surface, a 3% HF is applied for 30 second. Standard RCAI and RCA II cleaning processes are applied to clean the surface. A heavily doped phosphorous epitaxial film is grown (15-80 nm) at ($2x10^{-6}$ Torr) followed by the deposition of (75-80 nm) SiN_xH antireflection coating. The first mask is applied to define the opening for Al

metallization. Aluminum sputtering using Ar and RF of 300 W was applied for 1 µm thickness on both front and back surfaces. The second mask was applied to define the spaces covered with anti reflection coating for the incident photons. A mechanical cutting separation using dicing saw was applied to separate the different cells from each other. Figure 5.7 shows a schematic diagram of the fabricated epitaxial silicon solar cells on planar polished Si surfaces (a) and the fabricated devices on textured surfaces (b). Please note that, the deposited films on the textured surfaces will have the same roughness as the textured surface (which is not shown in Figure 5.7) because the thickness of these films are in the nanometer range but the random textured are in the micrometer range thickness.

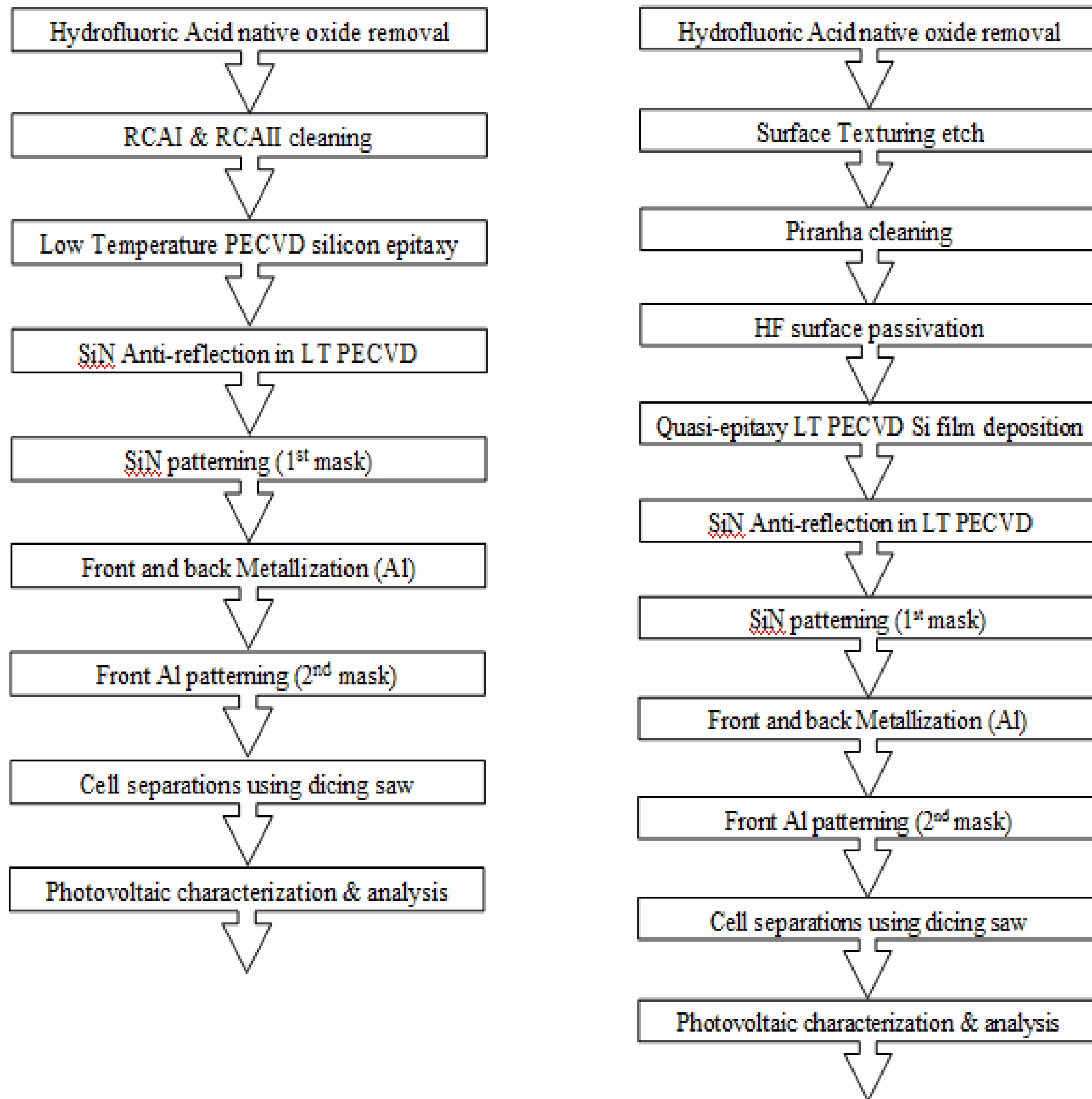
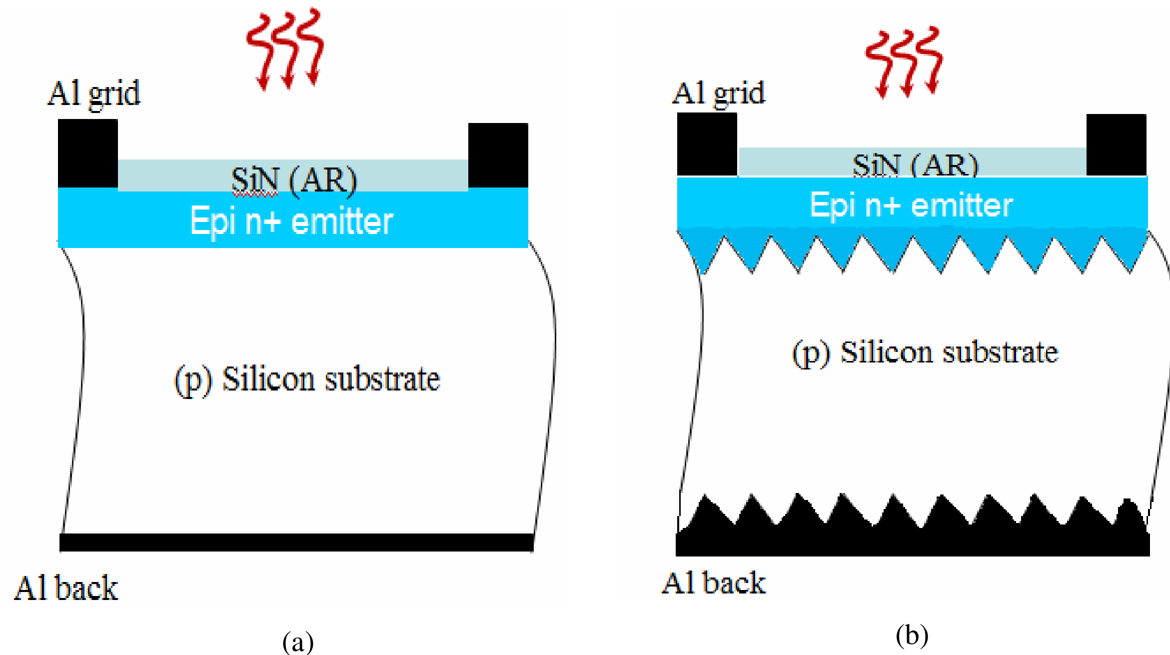


Fig. 5.6 Illustration of different routes of epitaxial growth silicon solar cell fabrication on planar and textured surfaces.



(a) (b)

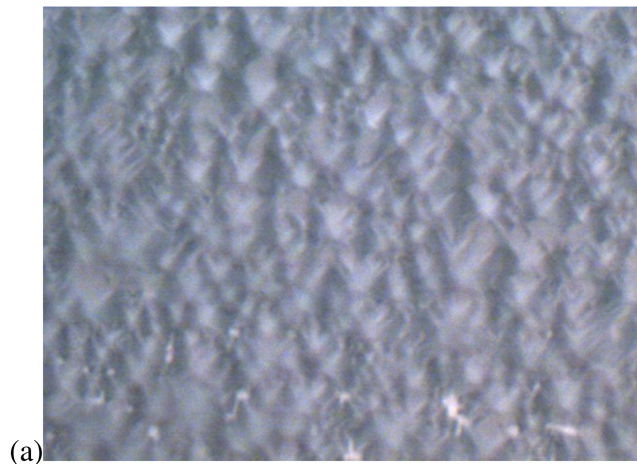
Fig. 5.7: Sketch of the structure of the fabricated devices (a) developed device on plane polished Si surfaces (b) developed devices on textured surfaces.

5.2.3 Surface texturing and Light trapping

One of the crucial problems in solar cells is that a significant part of the incoming radiation is reflected, which limits the efficiency of such devices. Reducing incident light-reflection is an important part of solar cell design and fabrication. According to the experimental and theoretical values given by Chelikowsky and Cohen [143], the reflectance of polished crystalline silicon is over 30% in the wavelength range from 400 to 1200 nm. Moreover, the reflection losses at ultraviolet range are 58% at 360 nm and 71% at 300 nm. To reduce these optical losses, many techniques have been developed [59]. One of these techniques is random texturing of the c-Si wafer, which is a standard technique to increase the light trapping in the substrate surface and maximizing the absorbed light into the device. Basically the light impinging on a textured substrate is subjected to multiple reflections on the rough surface, is being absorbed at each reflection. In this way the hemispherical wafer reflectance (the reflectance overall the half of the solid angle) is minimized. Silicon wafer

random texturing is usually achieved in commercial solar cells using anisotropic etching of the silicon network. The etching action is usually made by a concentrated alkaline solution at a controlled temperature. The most used alkaline solution is a low concentration (usually less than 5%) potassium hydroxide (KOH) and isopropyl alcohol (IPA) solution. KOH is widely used in microelectronics and photovoltaics as anisotropic etching solution. So, we used KOH and IPA as the main texturing technique. During the texturing process, large hydrogen bubbles (3mm size) stuck to the silicon surface, and created neither uniform textures (because of different sizes of pyramids) nor reproducible results. During etching, for aqueous chemical texturing with basic solution as KOH, the population and size distributions of the pyramids are governed by hydrogen bubbles [144-146]. These bubbles are generated during etching and easily stuck to the etched surface and cause the ‘‘pseudo-mask’’ phenomenon. Stuck bubbles suppress the chemical reaction between the etching solution and the silicon atoms to create pyramids. In this case, the control of the distribution and the size of hydrogen bubbles will be a key point to obtain uniform and low-reflecting surfaces. To avoid the formation of these large bubbles, it is preferred to use a surfactant to increase the hydrophilic nature of silicon surface toward hydrogen bubbles. Consequently, bubbles are less able to adhere to the etched surface [147]. So, we apply IPA because it is often used in industry with KOH. However, a problem with the random texturing solution (IPA and KOH) containing IPA is its low boiling point of 80°C, which is the typical temperature needed to perform texturing of the planar surface. This leads to evaporation of the alcohol during the etching process giving an unstable texturing system and reducing the reproducibility of the etching solution. So, we selected the process temperature to be well below the boiling temperature of IPA between 65 and 70°C. One sided polished Cz p-doped, 3” Si wafers of ~410 μm were used for texturing. HF acid dipping process (1%) for 60 seconds to remove the native oxide and clean the surface from any imperfections such as oxide and/or impurities, and achieve common conditions for random surface texturing. The mechanism for the pyramids formation on Si

(100) orientation, is through the etching and peeling of {111} facets [148]. Assuming that, a layer by layer peeling, this lateral etching begins from two edges and eventually summits at the center of the sidewall. In our observations, an average of 1.2-1.4 µm pyramids depth were formed under these conditions as confirmed by three dimensional image microscope and scanning electron microscope (SEM) images (not included here). Piranha cleaning process (Sulfuric acid and hydrogen peroxide, 4:1, respectively is applied for 10 minutes at 100°C) was used on the textured silicon surface for efficient cleaning process. Figure 5.8 shows the optical microscope images for the textured surface after applying alkaline etching process. Figure 5.8a shows the polished surface of Si (100) wafer after applying the random texturing chemical alkaline composition. The tips of the pyramids are clearly shown in this figure. Figure 5.8b represents the textured surface after applying Piranha cleaning process. Aluminum layers are sputtered on the textured surface and etched for the front Al grid for solar cells fabrications as seen in Figure 5.8c. It is also noticed that the grid lines are quite uniform and there is no disconnection in the Al metallization that need a thick Al layer between 1.5-2 µm on the front surface.

(a) 

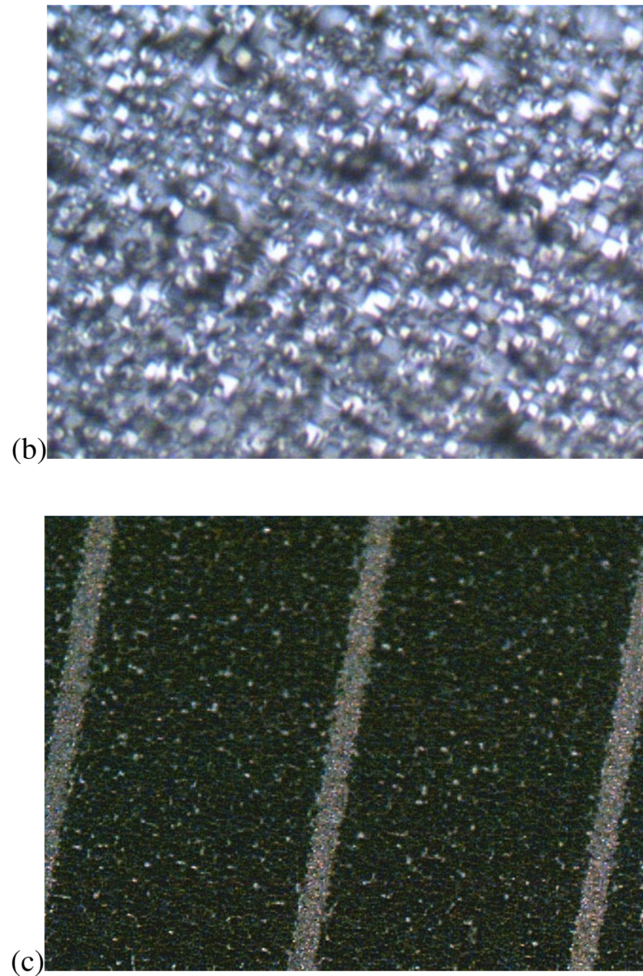


Fig. 5.8 Optical microscope images surface texturing using Alkaline (KOH and IPA, 7 and 3 %, respectively) composition for light trapping (a) surface morphology after 30 min at 70°C (b) After applying Piranha (c) Aluminium metal grid on the textured c-Si wafer.

The influence of the texturing surfaces on the developed epitaxial films and the photovoltaic parameters (such as external quantum efficiency and short circuit current J_{sc} using the developed epitaxial growth films) will be discussed in the following sections.

5.2.4 Metal grid configuration and mask design

Based on the information given in the literature [149, 150], the results show that conical contacts are better as compared to the rectangular contacts. They give lower resistive and shading power loss as compared to the rectangular shapes, which improve the efficiency of the cell at high concentrations. An overall decrease in power loss of about 20% is observed for conical bus-bar with respect to rectangular bus-bar at concentration ratio of about 8 Suns. Figures 5.9a and 5.9b show the top view and the 3D schematic diagram of the designed and selected grid layout which consists of conical like shape bus-bar and metal with finger spacing of average s_f fingers. The metal coverage is designed to be less than 10 % of the full coverage of the solar cells. An effective area of 1.0 cm^2 cells using chromium mask are fabricated with nearly 35 cells in one deposition run, which allow us to have a good quantitative analysis of the uniformity of the deposited films, and hence the fabricated solar cells on one wafer and from one deposition run to another.

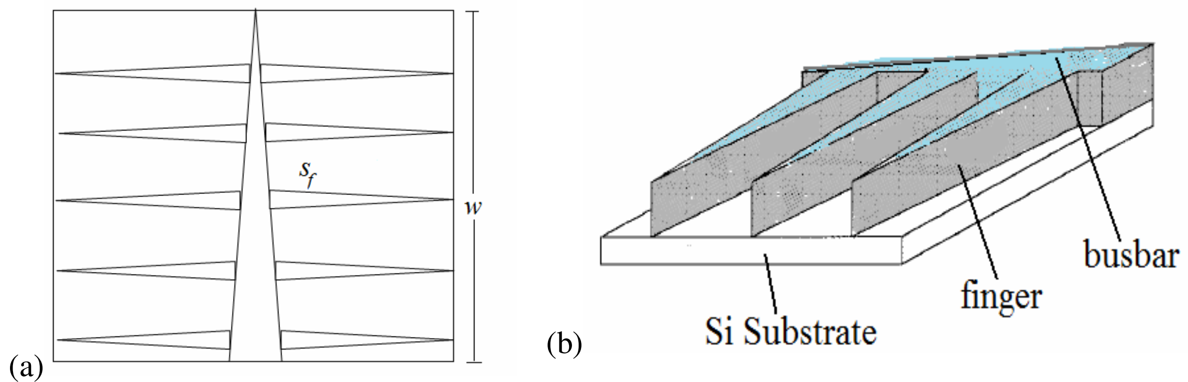


Fig. 5.9 Schematic diagram of the designed metal grid contact pattern for the fabricated epitaxial silicon solar cells (a) Top view of the designed metal grid (b) three dimensional metal grid (fingers and busbar).

5.3 Phosphorous doped epitaxial Si solar cell device characterizations

Solar simulator is used for the characterization of the photovoltaic properties of the fabricated solar cells. The simulator is calibrated using a standard solar cell and two reference cells measured and

calibrated at the National Renewable Energy Laboratory (NREL), Colorado, USA, under standard AM 1.5 conditions.

5.3.1 Emitter thickness influence

Several epitaxial solar cell devices (1 x 1 cm^2) have been grown using EP1 processing conditions with the structure *Al (front grid)/ SiN_x:H /n^+ epitaxial Si /p-type Cz/ Al (back contact)*, shown in Figure 5.10 with different emitter thicknesses (50 and 80 nm). Silicon nitride layer of 80 nm thickness was used as an antireflection coating. The standard electrical characterization method for a finished solar cell is the measurement of the current–voltage characteristics (I –V curve) under a sun simulator. Standard test conditions are the AM1.5G spectrum normalized to 100 mW/cm^2 and a solar cell temperature of 25°C. From these measurements the open-circuit voltage V_{oc}, the short-circuit current density J_{sc}, the fill factor (FF), and the energy conversion efficiency η are determined. Experimental I-V curves under standard measurement conditions (100 mW/cm^2 AM1.5 irradiance), of the fabricated epitaxial solar cells on commercial Cz planar wafers using EP1 process conditions are shown in Figure 5.10. Meanwhile, a very slight decrease in the short circuit current is noticed if the thickness of the emitter is increased from 50 to 80 nm. No change in the open circuit voltage (V_{oc}) is noticed, when increasing the thickness of the epitaxial emitter from 50 to 80 nm. These results are in contradiction with the results reported for the amorphous silicon emitters used in heterojunction structure, where a strong reduction of the photovoltaic properties is clearly visible due to the emitter thickness increase as reported in [151, 152]. This is expected for the amorphous emitter layer where more light is absorbed here and a minor part of the incident radiation arrives at the c-Si base where the photogenerated carriers are effectively collected, due to the high c-Si diffusion length. However, in our epitaxial device the case is completely different, this due to the fact that there was no change in the quality of the developed emitters even for thicker ones (80 nm), and hence the portion of the light spectrum absorbed in the emitter region was not influenced by increasing the thickness of the epitaxial emitter.

From the illuminated I-V curves, the measured V_{oc} values are in the range of 575-580 mV, and the calculated good fill factor (FF) values are in the range of 74-76 % giving a good indication of the low series resistance.

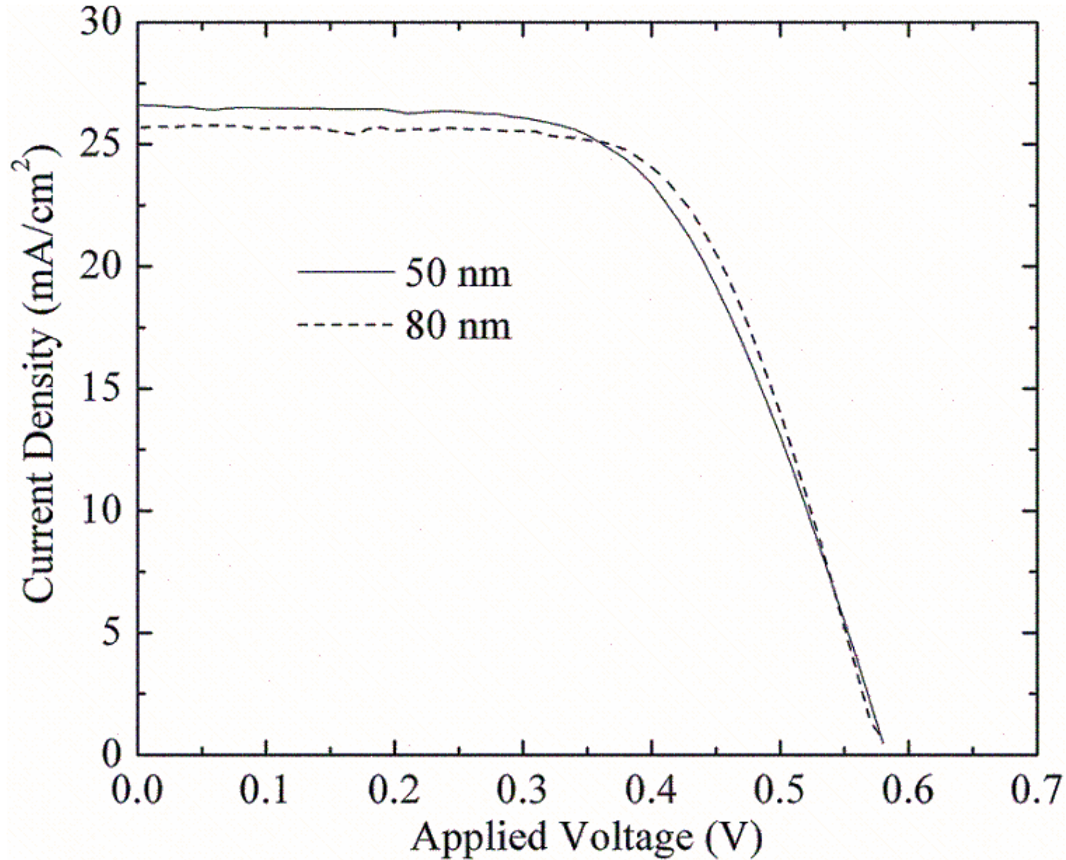


Fig. 5.10 Measured I-V curves under illumination for various emitter thicknesses using the following structure; *Al (front grid)/ SiN_x:H /n^+ epitaxial Si /p-type Cz/ Al (back contact)*, using EP1 processing conditions and developed at 300°C, on (100) flat silicon substrate.

The initial efficiency of the first prepared epitaxial silicon solar cell test structures are exceeding 11.5 % as calculated from the various measurements of the prepared structures using thick epitaxial emitters (80 nm). Although, no other enhancement features were applied to the designed solar cells, such as using transparent conductive oxide (TCO) layers. For most of our device structure stacks, 50 nm epitaxial emitter thicknesses were used. Figure 5.11 shows the internal quantum efficiency (IQE)

of 50 nm epitaxial silicon solar cell fabricated at 300°C under EP1 processing conditions on a planar substrate. The IQE was calculated using the measured external quantum efficiency (EQE) and the reflection data from the same solar cell.

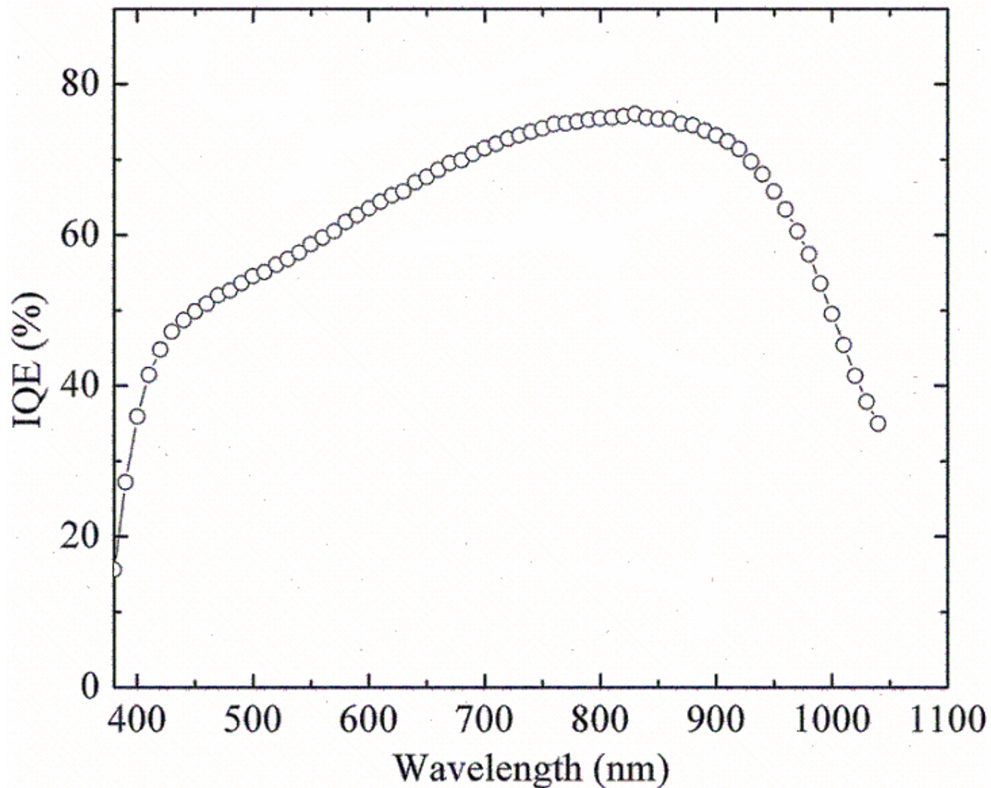


Fig 5.11 Internal QE of 50 nm epitaxial silicon solar cell fabricated at 300°C, using the following structure; *Al (front grid)/ SiN_x:H /n^+ epitaxial Si /p-type Cz/ Al (back contact)* and under EP1 processing conditions on (100) flat silicon substrate.

We noticed that a good reproducibility of the deposition process from the uniformity of the measured data processed on the same wafer and from one wafer to another (graphs not included here). In the short wavelength range (300 < λ <600 nm), the calculated IQE (as shown in Figure5.11) shows that the reduction of the thickness of the epitaxial layer can result in the reduction in losses caused by the absorption and the recombination, where in this wavelength region these are the most effective losses.

However, when thinner films were used no enhancement of the photovoltaic properties of the fabricated devices were noticed. So, we tried to enhance the short wavelength response, and hence the photovoltaic output using different techniques, such as RTP and/or hydrogenation in PECVD system at low annealing temperature as will be discussed in the next section.

5.3.2 RTP annealing influence on the photovoltaic properties

The IQE of 50 nm epitaxial silicon solar cell fabricated at 300°C using the same structure is presented in Figure 5.12. This result was obtained by applying a very fast annealing process, using RTP at 750°C for 60sec, on the deposited epitaxial films.

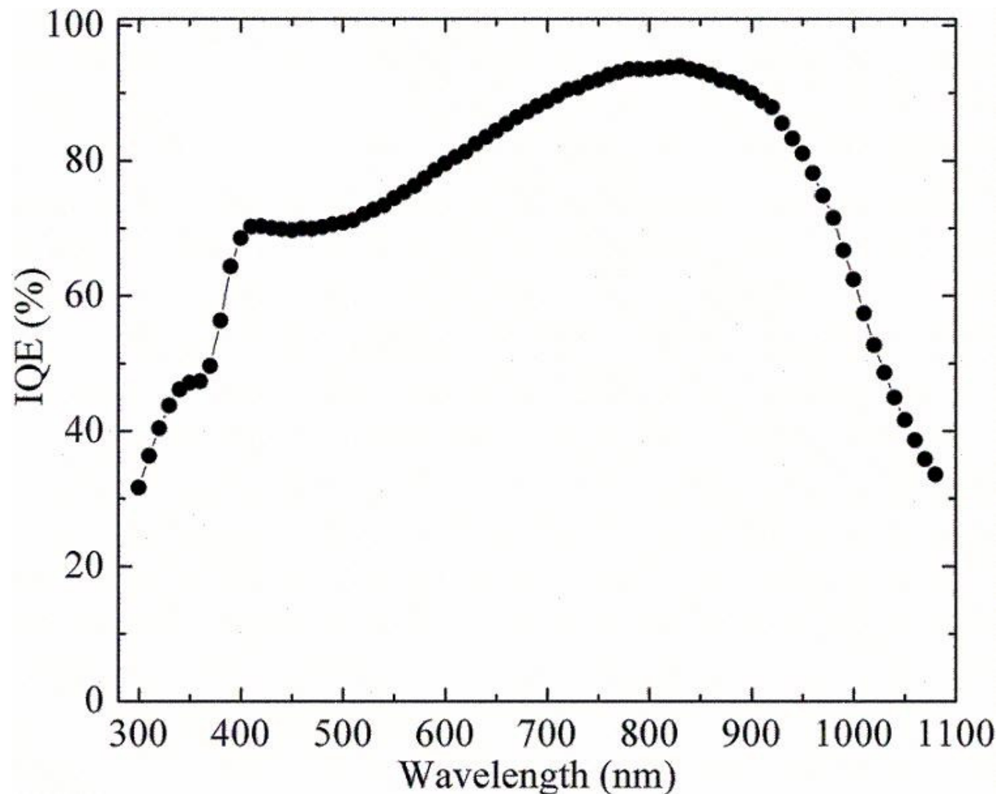


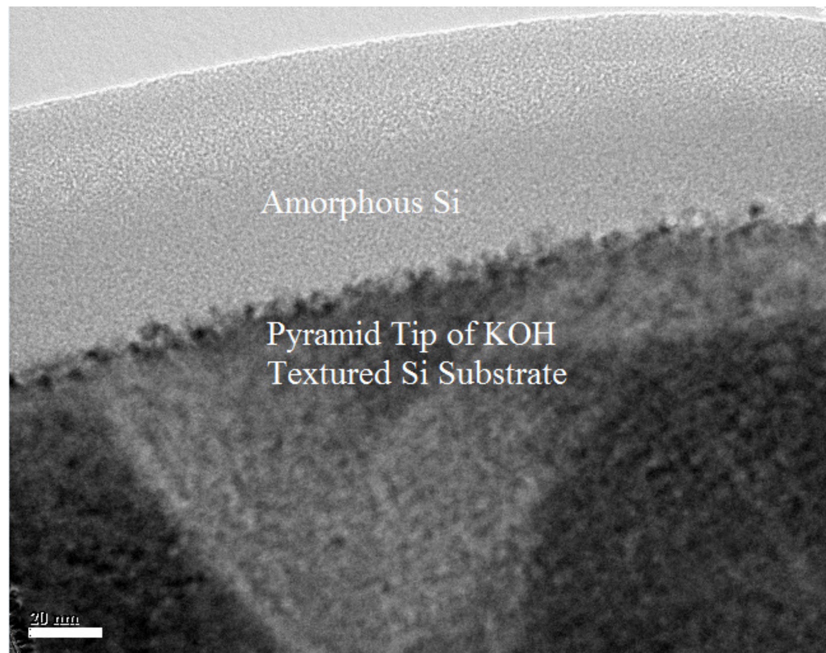
Fig 5.12 Internal QE of 50 nm epitaxial silicon solar cell fabricated at 300°C, using the following structure; *Al (front grid)/ SiN_x:H /(50 nm) n^+ epitaxial Si /p-type Cz/ Al (back contact)* and under EP1 processing conditions and annealed by RTP at 750°C for 60 sec, on (100) flat silicon substrate.

An enhancement in the green and blue wavelengths is noticed compared to the reference cell without applying the RTP annealing process. We believed that, the annealing process using RTP creates a submicron random surface roughness which enhances the light trapping in the shorter wavelengths (300 – 400 nm) of the spectrum. This comes as a result of better incoupling of the light into the absorber layer by introducing submicron textured units [153, 154]. This observation of surface roughness is confirmed by AFM and SEM micrographs analysis. We also noticed that, for most of the fabricated epitaxial solar cells have similar response for wavelengths $\lambda > 900$ nm. This is due to using exactly the same substrate with the same doping level, and hence almost the same diffusion length of the minority carriers. As confirmed by using HRTEM analysis reported in chapter 3, optimized annealing process (C) RTP with multisteps heating and cooling rates enhances more the epitaxial film and consequently minimizes the recombination losses. The V_{oc} and I_{sc} have values of 598 mV and 27.5 mA respectively, with a FF of up to 76% leading to an efficiency of approximately 12.5%, resulting in a significant efficiency enhancement of 8% over the reference cell without RTP annealing process is reported for the developed devices.

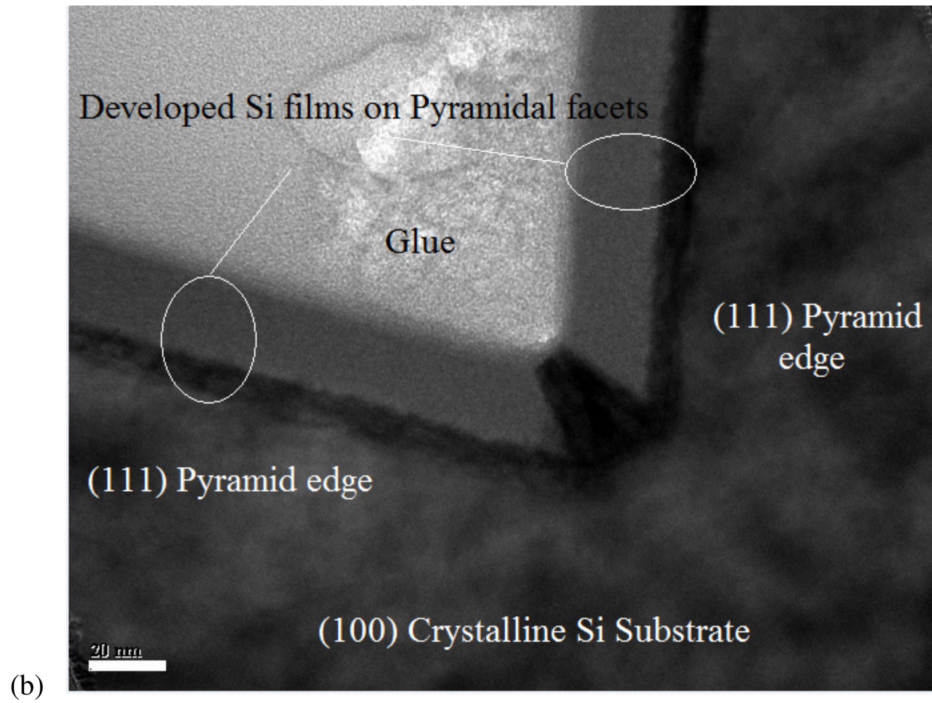
5.3.3 Textured surface influence

In the previous sections we discussed the macroscopic structure of the textured surface using optical microscope; it is worth here to analyze the structure of the developed epitaxial films using EP1 processing conditions on these textured surfaces. This analysis will not only help understand the characteristics of the developed films but will also shed some light on the photovoltaic properties on the textured surfaces. To the best of our knowledge, this the only reported characterization and analysis of the deposited silicon films under these conditions on textured surfaces using HRTEM analysis. Figure 5.13a shows HRTEM micrographs of the pyramidal tip. We noticed that the structure at this tip point and its surroundings is completely amorphous silicon with a few epitaxial islands (local epitaxial domains) near the interface. Whereas, on the pyramidal facets of the textured substrate

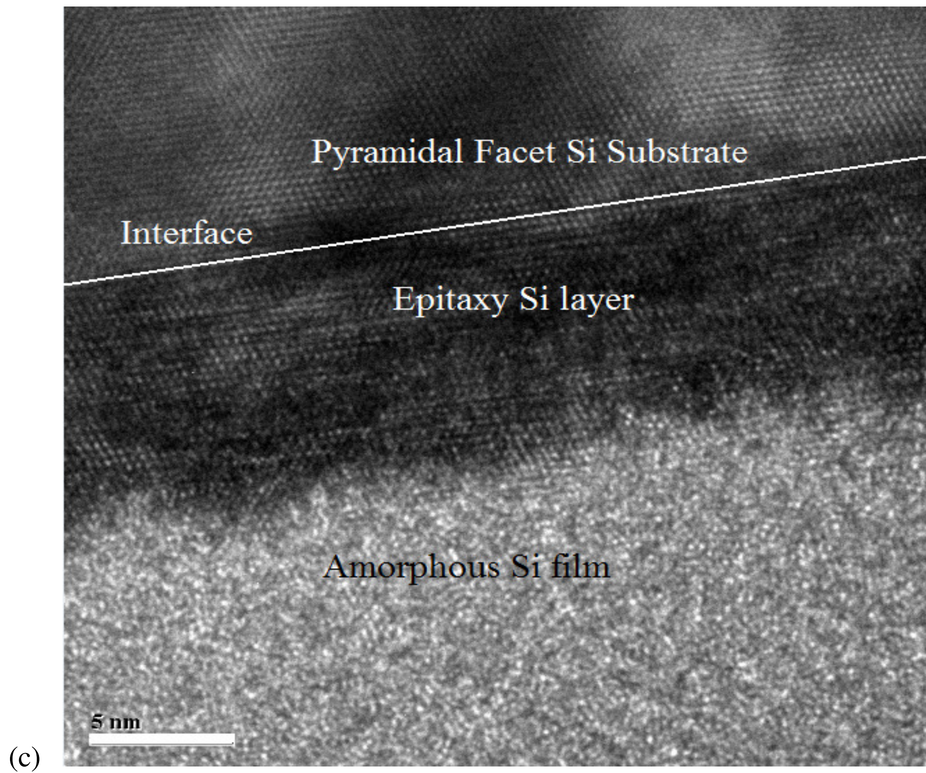
and at the bottom of the V shaped pyramid valleys the growth is a quasi-epitaxial with a thickness of 10-15 nm (almost 35% of the thickness of the deposited film) as confirmed by HRTEM analysis in Figure 5.13b and 5.13c. Hence, the junction between the textured substrate and the deposited silicon films is more likely to be heterojunction (HJ) due to the discontinuity in the epitaxial layer growth and the amorphous phases that appear on the pyramidal tip.



(a)



(b)



(c)

Fig. 5.13 HRTEM micrographs of epitaxial silicon films deposited using EP1 processing conditions on

(111) textured pyramidal facet inset bar=20nm, (a) the tip of the pyramidal, inset bar=20 nm (b) the V shaped pyramidal facet valley (c) Interface and quasi-epitaxial on pyramidal facet, inset bar=5 nm

Figure 5.14 shows the measured I-V characteristics under illumination for the textured (100) silicon wafer using the following structure; *Al (front grid)/ SiN_x:H /(50 nm)n^+ Quasi-epitaxial Si /textured p-type Cz/ Al (back contact)*, using EP1 processing conditions and developed at 300°C. The measured values of V_{oc} and I_{sc} for the textured cells are 612 mV and 31mA respectively, with a FF of 76% leading to an efficiency of up to 13.8%. A noticeable enhancement in the efficiency by approximately 20 % over the reference cell is reported for the developed devices on the textured surfaces without applying TCO.

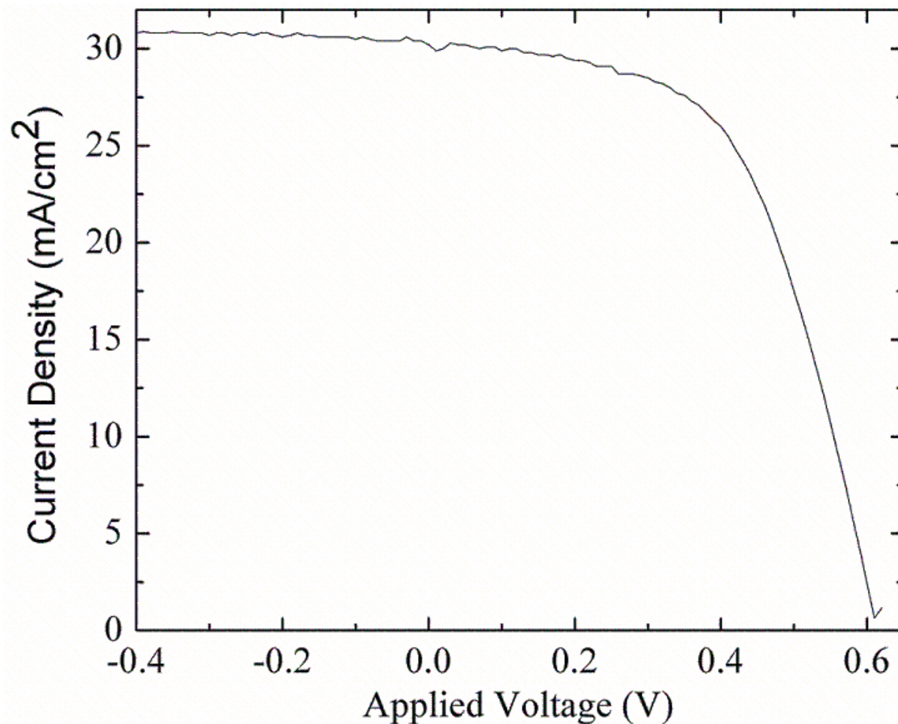


Fig. 5.14 Measured I-V curves under illumination for textured (100) silicon wafer using the following structure; *Al (front grid)/ SiN_x:H /(50 nm)n^+ Quasi-epitaxial Si /p-type Cz/ Al (back contact)*, using EP1 processing conditions and developed at 300°C.

Figure 5.15 shows the IQE for the textured (100) silicon wafer using EP1 processing conditions and developed at 300°C. In the wavelength range 650-1000 nm, the contribution of the textured cell to the IQE value is larger than that of the planar and the annealed cells. The IQE reached a maximum value and remained steady at this value in the range (650-1000 nm). The reason is, for a textured cell the light entering the substrate at a textured surface is tilted with respect to the cell normal, causing the light to travel in a slantwise making the light path longer than in the case of a planar cell. This means that the photogeneration takes place closer to the collection junction, which is very beneficial for the low-diffusion length cells, enhancing the collection efficiency of medium-to long wavelengths. The effect is equivalent to an increase of the absorption coefficient.

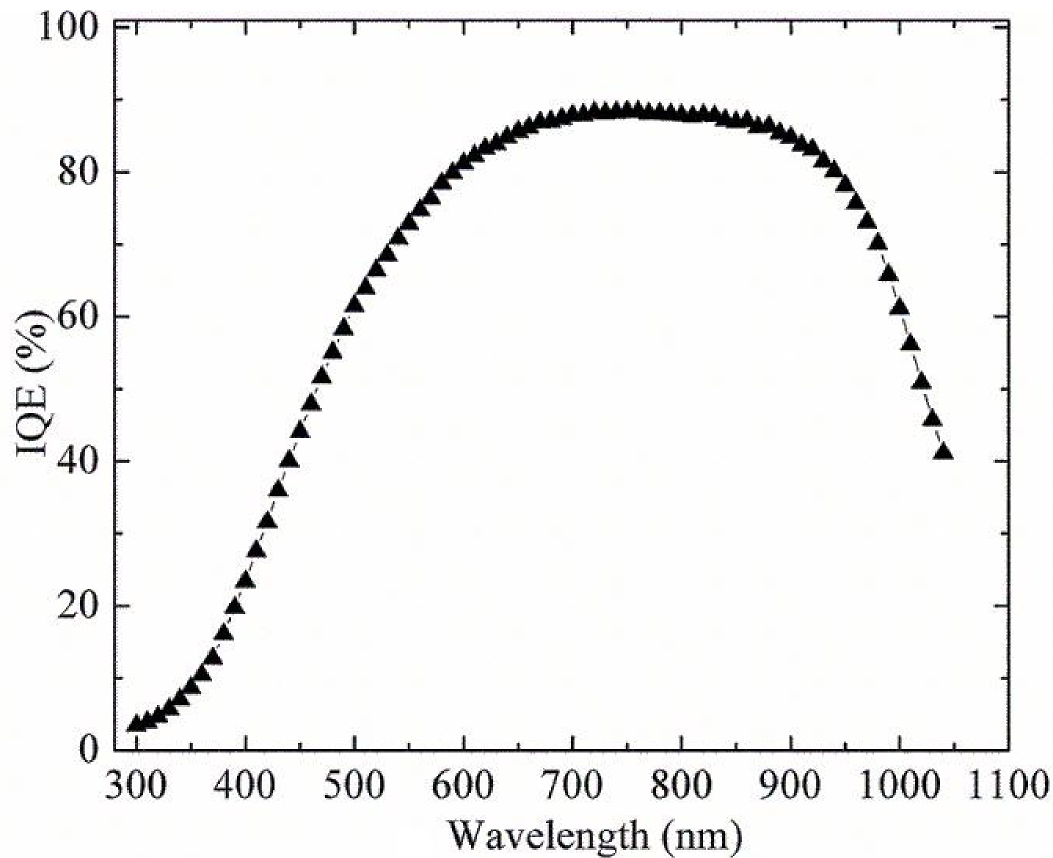


Fig. 5.15 Internal QE for textured (100) silicon wafer using the following structure; *Al (front grid)/ SiN_x:H /(50 nm)n^+ Quasi-epitaxial Si /textured p-type Cz/ Al (back contact)*, using EP1 processing

conditions and developed at 300°C.

5.3.4 Post-hydrogenation process

The hydrogenation process was applied on the developed epitaxial films deposited on (100) Si flat substrate to investigate its influence on the efficiency of the designed silicon solar cells. After the deposition, the temperature of the PECVD was raised up to 350°C with hydrogen flow of 50 sccm and the pressure was kept at 250 mTorr for 1.0 hr (without plasma ignition). The process was applied directly after the deposition of the film in LT PECVD system without unloading the wafer from the system. Figure 5.16 shows the measured I-V curves under illumination on the planar (100) silicon wafer using EP1 processing conditions and developed at 300°C. It was noticed that the hydrogenation process has its impact on the short circuit current (I_{sc}), decreasing it from 27.5 mA to almost 23 mA with 16.6% loss in I_{sc}. Whereas, the open circuit voltage V_{oc} increased by nearly 2-3 mV for the hydrogenated films and even for the annealed films at 350°C without the hydrogenation process.

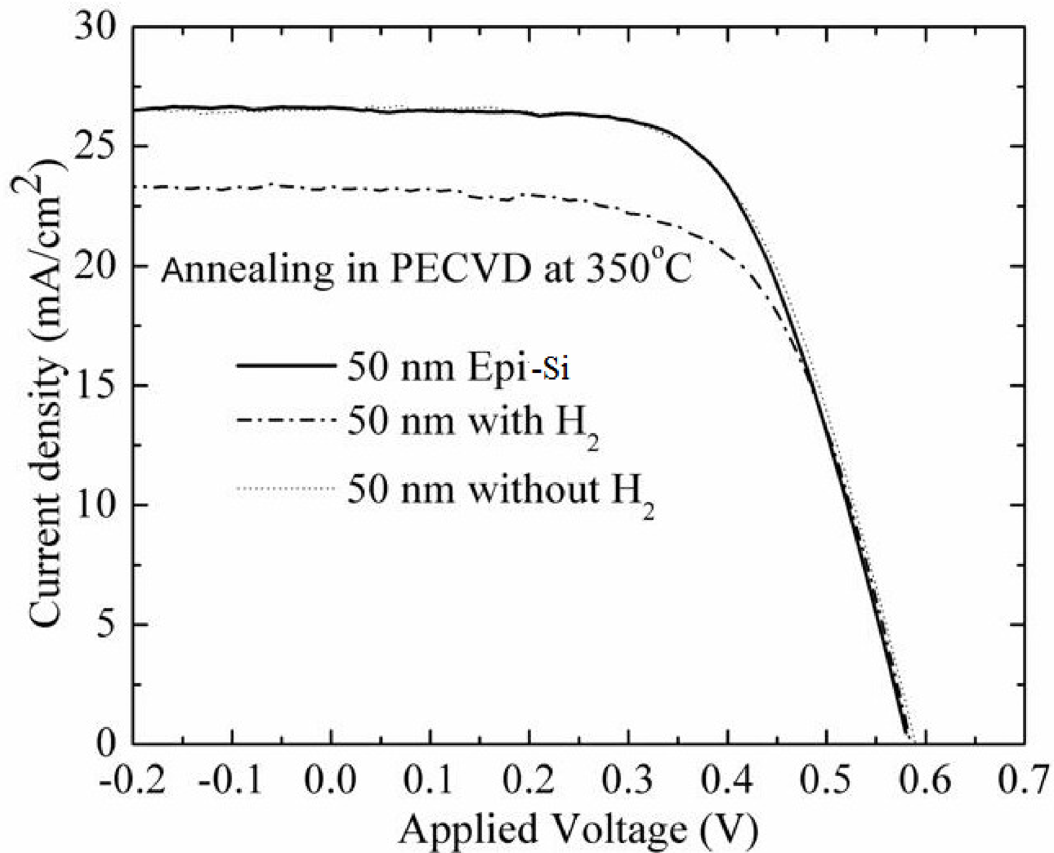


Fig. 5.16 Measured I-V curves under illumination for post-hydrogenated epitaxial silicon films, the hydrogenation process is, 350°C, hydrogen flow of 50 (sccm), the pressure was kept at 250 (mTorr) for 1.0 hr, (without plasma ignition), on (100) flat silicon substrate.

5.3.5 Devices fabricated at very low temperature

Several epitaxial fabricated silicon solar cells were developed at a very low temperature of 150°C and even at room temperature (25°C) using the same deposition conditions described in EP1. Figure 5.17 shows the IQE of 50 nm epitaxial silicon solar cell fabricated at 150°C under EP1 processing conditions on (100) silicon planar substrate. It was noticed that, the maximum peak of the IQE was shifted towards the lower wavelengths compared to the IQE for the developed epitaxial silicon films at 300°C. An enhancement of IQE in the lower wavelength range 450-700 nm was noticed for the prepared devices at low epitaxial temperature, and this is related to more hydrogen content at lower

processing temperature leading to more efficient passivation resulting in a decrease in the surface recombination velocity (SRV). The open circuit voltage V_{oc} and short circuit current I_{sc} are almost the same as in the epitaxial films developed at 300°C, and their values are 596mV and 27 mA respectively with lower FF of 60-62.

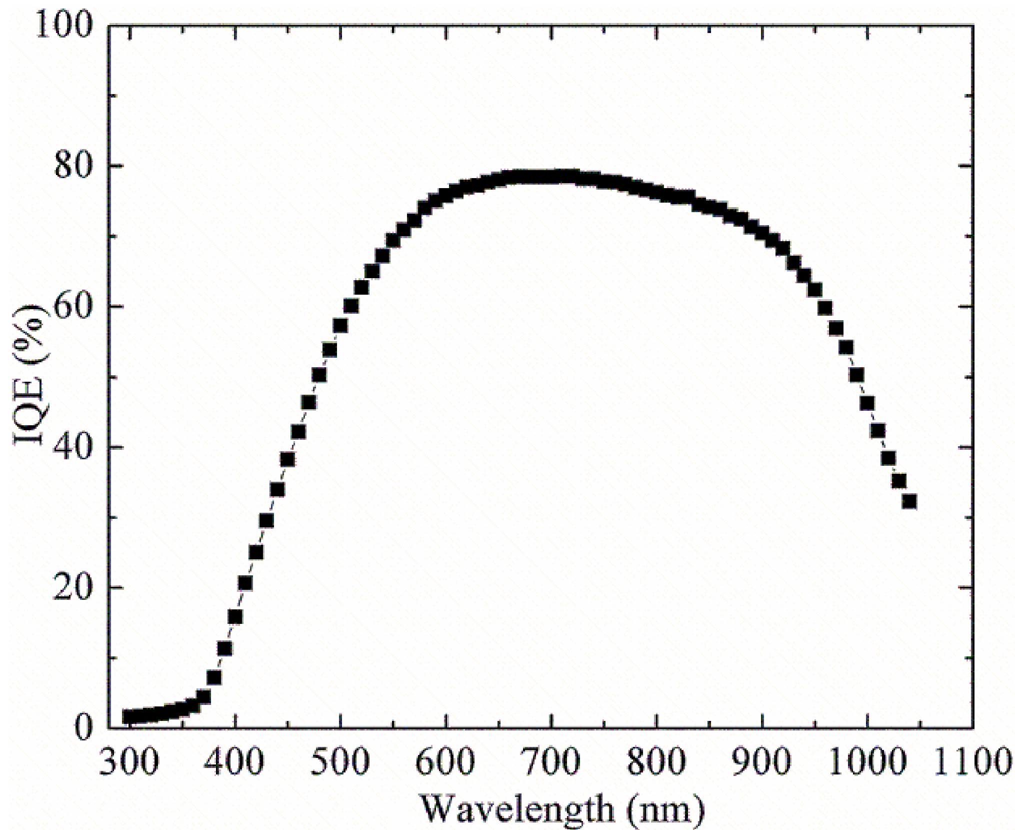


Fig. 5.17 Internal QE of 50 nm epitaxial silicon solar cell fabricated at 150°C, using the following structure; *Al (front grid)/ SiN_x:H /(50 nm) n^+ epitaxial Si /p-type Cz/ Al (back contact)* and under EP1 on (100) flat silicon substrate.

5.3.6 Room temperature fabricated and characterized cells

Moreover we tested the photovoltaic characteristics at room temperature for the developed films. The structure of these films were reported and discussed in chapter 3 using HRTEM analysis. As we discussed the majority of these films which were developed at room temperature were amorphous

with small epitaxial domains near the interface. Figure 5.18 shows the IQE of 20 nm epitaxial silicon solar cell fabricated at 25°C under EP1 processing conditions on (100) silicon planar substrate. The maximum value of the V_{oc} for the fabricated solar cells at room temperature was 440 mV, with a I_{sc} of 32 mA. A low FF was also calculated for these devices giving an indication of the low quality of the film fabricated at very low temperature conditions and the high series resistance. The main contribution for high resistance which has an affect on the FF for this device is expected to be from the deposited layer at room temperature.

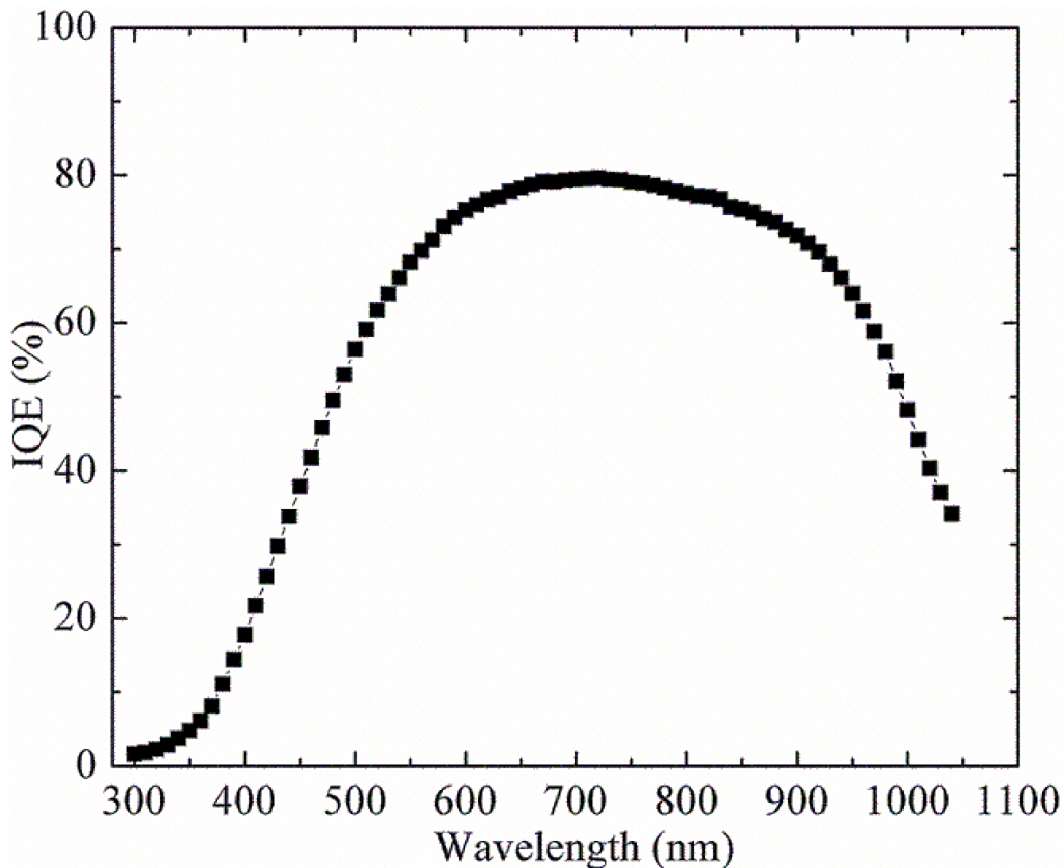


Fig. 5.18 Internal QE of 20 nm silicon solar cell fabricated at room temperature (25°C), using the following structure; *Al (front grid)/ SiN_x:H /(20 nm) n^+ Si films/p-type Cz/ Al (back contact)* and under EP1 on (100) flat silicon substrate.

5.4 Fabrication and characterization of Boron doped devices

We used the developed quasi-epitaxial TMB boron doped silicon films, under low temperature PECVD process conditions, as an emitter in a prototype silicon solar cell to investigate its photovoltaic properties. A variety of proposed structures were fabricated and characterized on planar, textured surfaces, and a thinned surface using back surface field. In this process, a fabricated epitaxial silicon solar cell was defined and has the following structure *Al (front grid)/ SiNx:H /p+ quasi-epitaxial Si /n-type Cz/ Al (back contact)*. The same fabrication steps were used for the fabrication process for the n-type boron doped quasi-epitaxial solar cells. Two percent HF was applied for 30 second, and the standard RCAI and RCA II cleaning processes were applied to clean the surface from any organic or metal contamination to passivate the surface before loading to the PECVD system. The main processing conditions used for the fabrication of solar cell were 91.6 % hydrogen dilution, 25 sccm of silane, TMB gas flow of 10 sccm, a processing pressure of 400 mTorr, and processing temperature of 300°C. A variety of heavily boron doped quasi-epitaxial emitters were grown with a thickness of (20-50 nm) followed by the deposition of (75-80 nm) SiN_x:H antireflection coating. The first mask was applied to define the opening for Al metallization. The second mask was applied to define the spaces covered with anti reflection coating for the incident photons. A mechanical cutting separation using dicing saw was applied to separate the cells, each cell has an area of 1.0 cm^2. No transparent conductive oxide was used for the fabrication process. We fabricated quasi-epitaxial boron doped silicon solar cells and analyzed the I-V characteristics of the prepared solar cells with relatively thicker emitters of 50 nm on planar surfaces. As we noticed from the films developed on the textured surfaces the film structure was changed from quasi-epitixial to a mixed phase, and then to a completely amorphous structure which yield a good structure for the light absorption.

This structure offered a good tandem structure with a wider band gap at the uppermost, which filter the incident spectrum. Figure 5.19 shows the IV characteristics of the fabricated devices using boron doped emitter.

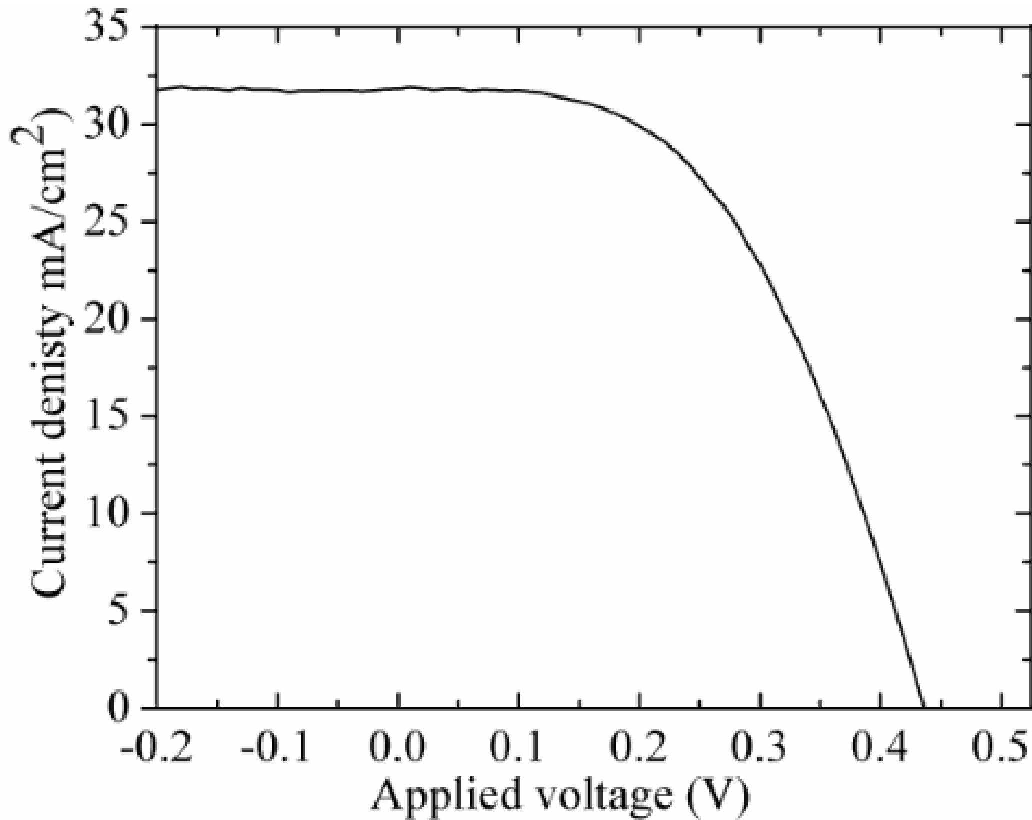


Fig. 5.19: Measured IV characteristics of 50 nm boron doped quasi-epitaxial silicon solar cells on n-type flat substrate and annealed using RTP (C).

It was also noticed that the value of the open circuit voltage was very low of approximately 440 mV, with a short circuit current I_{sc} of approximately 32mA and a low FF < 60%. So, in order to enhance the photovoltaic properties of the developed films, an activation process using RTP was applied directly after the deposition and before the metallization and lithography processes. We deposited an epitaxial highly phosphorous doped layer of 50 nm thickness to work as a back surface field layer. The structure and electrical properties of this layer were characterized in detail in chapter 3, where EP1 process conditions were used for this purpose. To benefit from the deposited back surface field

layer, the thickness of the processing monocrystalline silicon wafer must be thinned. To do so, the substrate is chemically etched and thinned down to 250 µm, and then the thinned substrate is textured using KOH solutions as described in detail in the previous sections. Figure 5.20 shows a schematic diagram of the fabricated solar cell device structure.

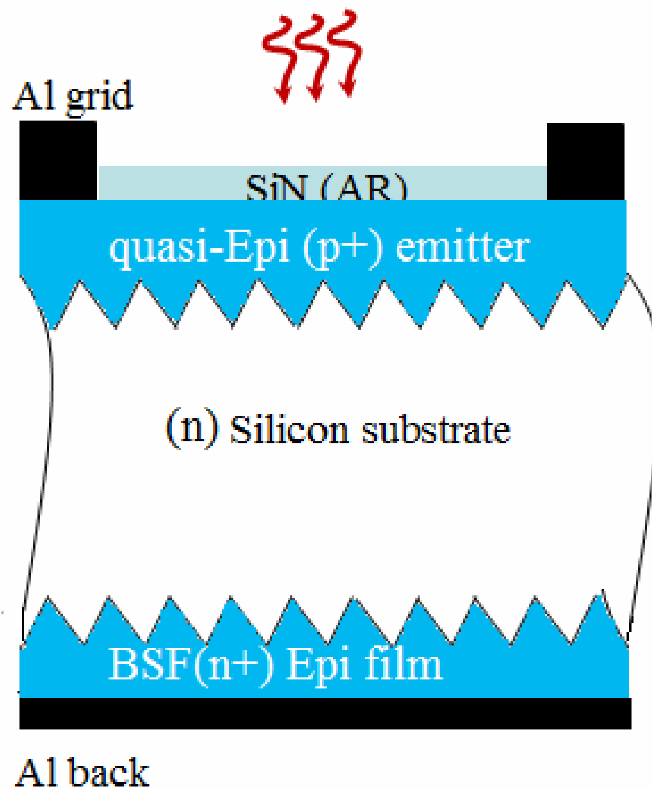


Fig. 5.20: Schematic diagram of the fabricated 20 nm boron doped quasi-epitaxial silicon solar cells on the textured surface and deposition of 50 nm phosphorous doped epitaxial layer (using EP1 conditions) as back surface filed.

Figure 5.21 shows the I-V characteristics of the fabricated devices for the structure presented in Figure 5.20. The V_{oc} for these devices is relatively high compared to the devices with thicker emitter, where for these devices we used 20 nm of the quasi-epitaxial boron doped films.

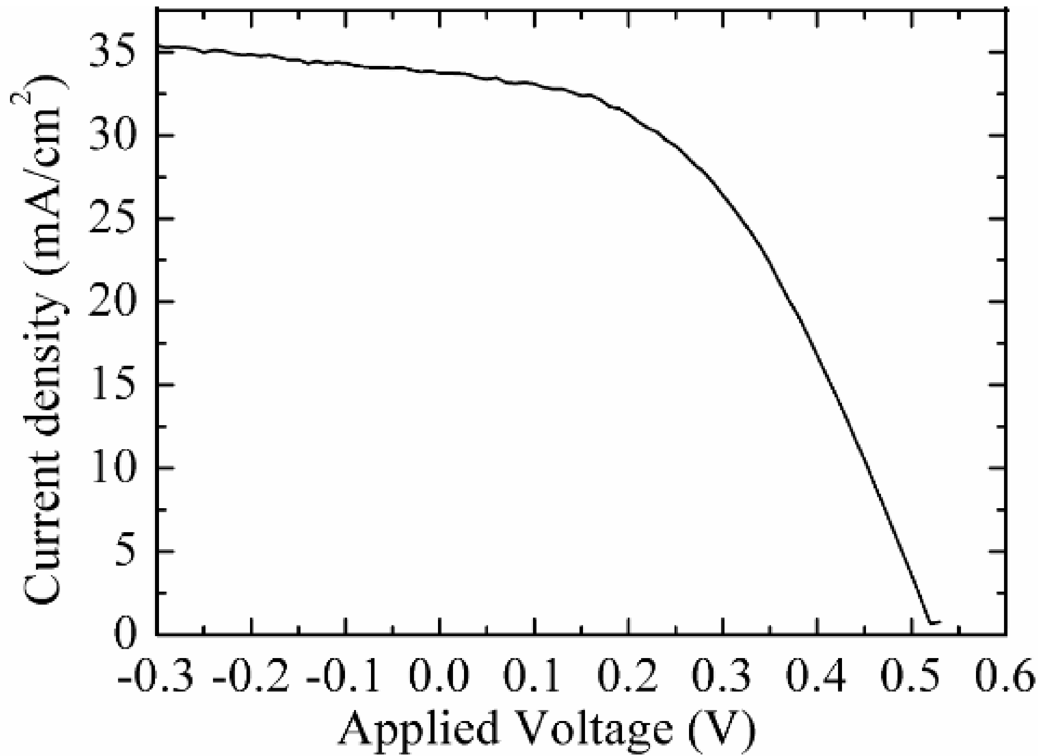


Fig. 5.21: Measured IV characteristics of 25 nm boron doped quasi-epitaxial silicon solar cells on n-type textured substrate and annealed using RTP (C) with 50 nm heavily doped epitaxial layer on the back surface to create BSF.

5.5 Summary and conclusions

In this chapter the photovoltaic properties of the developed phosphorous and boron doped silicon films deposited at low temperature using PECVD were investigated in detail. Different schemes for the fabrication and preparation process were presented which have the advantage of simplicity and compatibility with the industry for large scale production. Full diode characterizations were performed to investigate the electrical properties of the developed films under dark and illuminated conditions, before the fabrication process of the developed solar cells. Rapid thermal annealing process was applied to investigate its influence on the diode’s electrical properties, and hence the fabricated devices. The measurements revealed that, applying the selected RTP process at 750°C for

60 s improved the ideality factor of the diodes, especially for diodes fabricated at 99% HD, where there were no issues related to the hydrogen evolution from the film. The uniformity of the I-V curves was very good for the diodes prepared using EP1 conditions at 91% hydrogen dilution, especially for the epitaxial diode structures without applying RTP annealing process. However, some of the annealed diodes show leakage in the I-V characteristics due to the appearance of pinholes in the surface of the annealed films because of the hydrogen evolution from the surface of the epitaxial structure under EP1 processing conditions. As a consequence the photogenerated current was decreased. Detailed studies of photovoltaic properties under different processing conditions confirmed that, the measured V_{oc} values are in the range of 575-580 mV with FF values in the range of 74-76 % were calculated, giving a good indication of the low series resistance of the devices fabricated without applying RTP process or any enhancement features, such as BSF or TCO. The initial efficiency of the prepared epitaxial silicon solar cell on planar surface test structures is approximately 11.5%.

Applying the RTP annealing process for a very short time (60 s) at moderate temperature of 750°C enhances the V_{oc} and I_{sc} with values of 598 mV and 27.5 mA respectively, and a FF of up to 76 % leading to an efficiency of 12.5%, resulting in efficiency enhancement of 8 % over the reference cell without RTP annealing process.

Using the light trapping technique by random texturing using alkaline solutions enhances both V_{oc} and I_{sc} for the textured surface with 612 mV and 31mA respectively and FF of 75-76 % leading to an efficiency of up to 13.8 %. A noticeable efficiency enhancement by approximately 20 % over the reference cell (without RTP annealing process) was reported for the developed devices on the textured surfaces. We also investigated the epitaxial growth and photovoltaic properties at low temperature of 150°C. It was confirmed that, an enhancement in the lower wavelength range from (450-700 nm) was reported for the prepared devices at this very low epitaxial temperature, which is

related to more hydrogen content at lower processing temperature and leading to more efficient passivation. The open circuit voltage V_{oc} and short circuit current I_{sc} were almost the same as for the epitaxial films developed at 300°C, 596mV and 27 mA respectively. Devices fabricated and characterized at room temperature resulted in high short circuit current I_{sc} of 32 mA. Different designs of boron doped quasi-epitaxial films using TMB as the dopant source were fabricated and tested under low temperature process using PECVD system. From these detailed analysis, we can conclude in general that the most promising developed film was the phosphorous doped film using processing conditions EP1. Moreover, the boron doped films can be enhanced by the optimization of the processing conditions especially silane and the flow of the boron doping gas.

Chapter 6 : Variations of the LT-PECVD process to include Si nanocrystals: Future work

Introduction

Silicon nanocrystals (Si NCs) material is a potential candidate for photovoltaic applications. Silicon nanocrystals (Si NCs) have been known to possess interesting properties such as bandgap modulation with NC size and very fast optical transition which make them suitable for Si tandem solar cells that potentially enhance and lead to better performance. As a result of their wide gap, the new photovoltaic (Si NCs) is a good alternative to the high bandgap amorphous silicon carbide alloys which are essential intrinsic layers of the top cells in tandem structure. In the course of this PhD research we found a possible way to incorporate Si nanocrystals in a low-temperature film. This was achieved by depositing a thin layer of Si NCs embedded in amorphous silicon matrix, which can lead to efficient photon absorption and an efficient passivation of the front surface of the fabricated device. The preliminary results and some characterizations are presented in this chapter. This approach can be exploited to introduce a band-gap gradient in the film with decreasing bandgap from the top when employed in solar cell emitters.

6.1 Silicon nanocrystals (Si NCs) preparation

Atomic hydrogen plays an important role in the growth of a diversity high quality silicon films in silane-hydrogen plasma as we discussed in details in chapter 3. Different models have been used to explain the role of hydrogen chemistry on the microstructure and quality of the developed films. We succeeded in the development of an epitaxial grown silicon films in a hydrogen dilution regime of $> 91.5\%$, using conventional PECVD at LT as we discussed in chapter 3 and 4, explained by using this model. In this chapter, we fabricate silicon

nanocrystals by using another regime (70 and 90 % HD) away from high hydrogen dilution developed on a (111) silicon substrate. Moreover, an intermediate chamber pressure between 0.7- 0.8 Torr is used. At this high chamber pressure, the average energy of electrons increases and large amount of nascent hydrogen is generated in the plasma [155]. These energetic hydrogen atoms can supply a large amount of energy to the surface growing films which enhance the structure of the developed nanostructures and relaxation of amorphous silicon matrix. On the other hand, we used ion bombardment as a tool to control the size of the developed nanostructures. The ion bombardment could be controlled through different techniques, (i) changing pressure, (ii) modifying the reactor geometry, and (iii) applying a dc bias on the rf electrode. In our case we will use the chamber pressure as a technique to optimize the ion energy and hence the ion bombardment. For this purpose, crystalline Si substrates were used with resistivity between 1-10 Ω cm one sided polished about 420 μm thick. Different silicon substrate orientations were used to perform and develop these silicon nanostructures. Low deposition temperature < 300°C is used to develop these nanostructures to be compatible with low temperature industrial processing schemes. Standard cleaning process as RCA I and RCA II solutions are applied. Native oxide etching is performed using 2% HF directly before loading the Cz-Si substrate into high vacuum (10^{-6} Torr) PECVD system.

6.2 Characterization and analysis of the developed Si nanocrystals

6.2.1 HRTEM Analysis

Figure 6.1 shows a representative image of HRTEM micrograph, developed at ~ 88% hydrogen dilution, more than 10 % silane concentration, in 50 mW/cm^2 power density and 0.7 Torr chamber pressure on (111) silicon substrate. HRTEM of as-grown films confirm that the presence of Si NCs, as noticeable by circles in Figure 6.1, with an average size of 2.5 nm. Furthermore, the micrograph reveals that the film composed of crystalline Si NCs embedded in amorphous silicon matrix. The corresponding selected area electron diffraction pattern (SADP) in the upper right of Figure 6.1 verify the crystalline structure of the Si NCs with its different scattered dots on distinct rings giving a clue of the existence of both phases (the crystalline Si NCs and the amorphous silicon matrix). Spherical shape of Si NCs is the dominant structure spread in the amorphous silicon matrix. In contrast to the columnar-like growth mechanisms reported by Houben et al. [156] for nano and microcrystalline, the representative HRTEM shows that, Si and structure of silicon nanocrystals are isolated by 10 to 20 nm of amorphous silicon matrix. Moreover, some Si NCs may emerge leading to one big spherical Si (Si NCs). Instead, this regime for plasma pressure (0.7 Torr) is below the onset of agglomerations [157] which increase the density of nanostructure crystallites, and decrease the contribution of radicals. Moreover, the influence of the ion bombardment on the nano-size structure can not be ignored where, it plays an important role on the nanostructures size reduction due to film bombardment. Hamers *et al.* pointed out that in rf PECVD has a large contribution (up to 70%) of ions contributed to the growth compared to other deposition systems [158]. One of the leading ideas to vary the ion energy and hence the ion bombardment is the pressure change. Indeed, increasing pressure lowers the ion energy by increasing the kinetic energy losses through collisions with the neutral background gas, i.e., by reducing the ions mean free path [159]. However, the total pressure is high which help to reduce the ion bombardment influence, it still play an important role on the

developed nanostructures [160]. On the other hand, the high silane concentration regime (10-42%), and high power density is favorable conditions for separated Si NCs structure and avoiding the formation of columnar-like structure continuous nano or microcrystalline as seen from HRTEM image and the electron diffraction pattern inset in Figure 6.1.

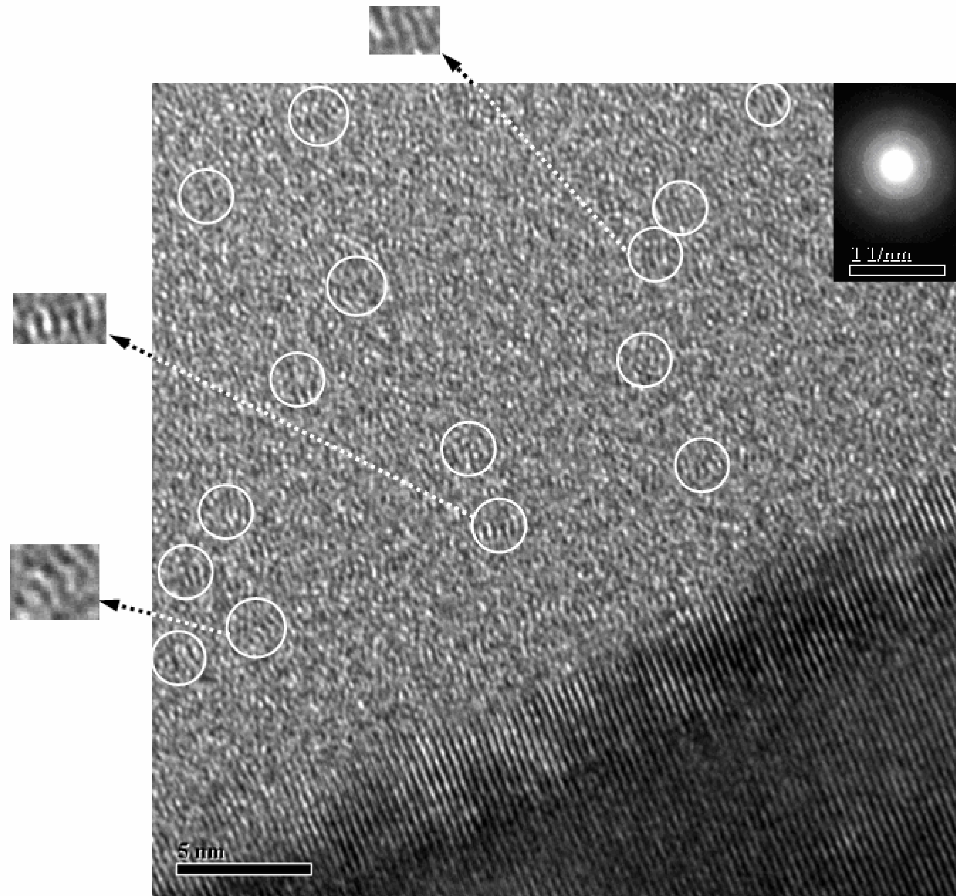


Fig.6.1: Representative of HRTEM images for the developed silicon nanocrystals at 300°C, the inset indicate the electron diffraction pattern.

6.2.2 XRD Characterization

6.2.2.1 As Deposited silicon nanocrystals

The broadening of X-ray diffraction lines is one of the most accurate indirect methods to determine the size of nano particles less than 100 nm and offers a non-destructive, highly strain-sensitive method for analysing low-dimensional structures. Many investigators work on the determination of

the size in nano scale from the x ray broadening line analysis [161-163]. Debye-Scherrer formula relates the crystallite diameter size (d) with the full width at half maximum of a Bragg peak in a 2 θ as presented by Eq. 6.1 [164].

$$L = \frac{K\lambda}{B\cos\theta_B} \tag{6.1}$$

where *L* is the mean dimension of the crystallites, *B* is the breadth of the pure diffraction profile on the 2θ scale in radians, λ is the wavelength of the incident X-ray (1.542 Å), and θ_B is the Bragg angle, *K* is a numerical constant approximately equal to unity and related both to the crystallites shape and to the way in which *B and L* are defined (we take K as 0.9 in our analysis) [165]. Different research groups work on the definition of broadening and used different approximation for this purpose. In our analysis, we will use the definition given for the line breadth *B*, by Cullity [166], as the full width at half maximum in radians. The size, orientation and fine structure of the developed SDs is deeply characterized using XRD technique. Bede D1 x-ray diffractometer is used for this purpose. The samples characterized using Cu Kα line with glancing incidence angle of 2.5^o and scanned between 15-70°. The contributions from Kβ were eliminated from the Cu x-ray source, using silicon crystal monochromater to ensure Kα is the only line incident into the sample. The acquisition time per angular step of 250–350 s is used. The detector ranges, step sizes, and duration were chosen to provide sufficient coverage in the vicinity of the well known diffraction peaks from Si. The crystallinity contribution and size of the embedded crystalline SDs in amorphous Si matrix are determined using Micro-Raman spectroscopy. Figure 6.2 shows the x-ray diffraction patterns for Si NCs grown by PECVD at 300°C, (no post-deposition annealing process).

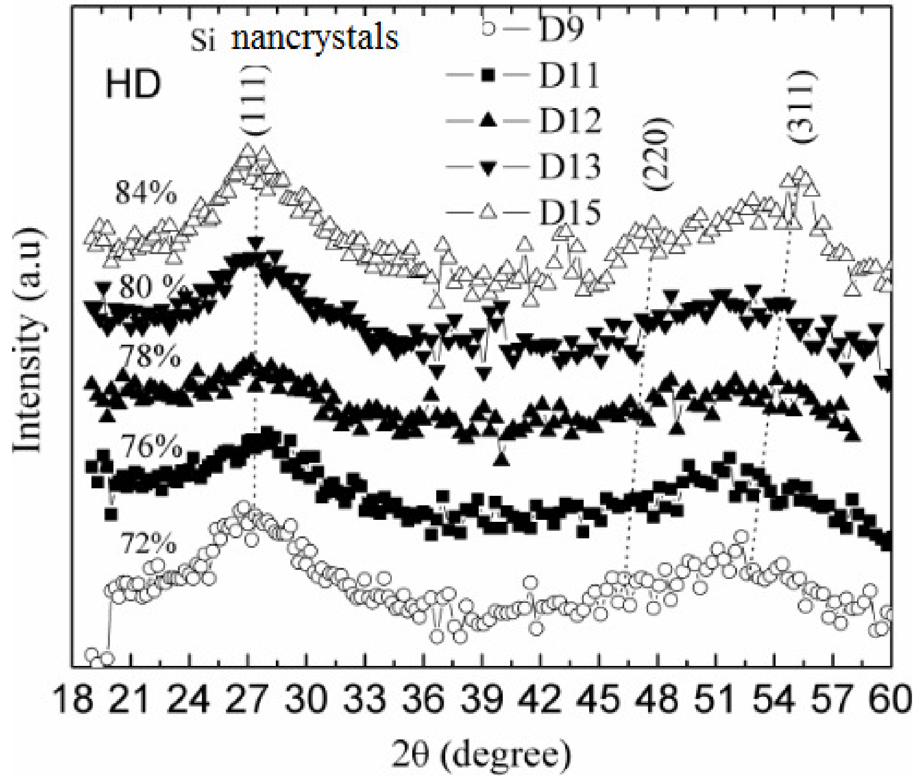


Fig. 6.2: X-ray diffraction pattern of the developed Si nanocrystals at 300°C, 0.7 Torr and 50 mW/cm^2 chamber pressure and power density, respectively on (111) silicon substrate.

A selected range of both chamber pressure and power density were optimized to in the range of 0.7 Torr and 50 mW/cm^2, respectively. An elevated hydrogen dilution ratio in constant flow of silane was used to develop nanostructures shown in Figure 6.2. A well resolved peak can be detected at ~ 27.07° which is associated to crystalline Si planes (111) at 28.47°. The broad shifting towards lower-angle side of the Bragg (111) is attributed to the expansion of the (111) lattice plane in the amorphous matrix [174] By increasing the HD ratio from 72% (sample D9) to 84% (sample D15) the peak position shifted by 0.5° and located at 27.5°. Furthermore, the FWHM of the peak at (111) lattice plane for D15 is narrower than the other samples giving an indication of larger Si NCs compared to other samples as calculated in table 6.1. A second broad peak is observed at ~ 51.88° (for D9, D11, D12 and D13). It is clear that, this peak is in fact a combination of two characteristic peaks of silicon

at 47.5 and 55.0 ^{o}C associated with (220) and (311) lattice planes. However, by increasing the flow ratio of hydrogen inside the chamber up to 84% (sample D15), an initial separation between the two peaks at (46 and 55.3^{o}) appears with more intense at 55.3^{o} corresponding to (311) lattice plane.

6.2.2.2 Post-deposition RTP process

Post-deposition annealing process was applied on the developed Si NCs using Lindberg system at 550°C for 0.5h in 500 sccm argon flow. Due to the stable structure of the developed Si NCs we could not spot major changes in x-ray diffraction pattern except for a pronounced small peak near 55^{0} that gives more indication of the stability of the developed structure as seen in Figure 6.3.

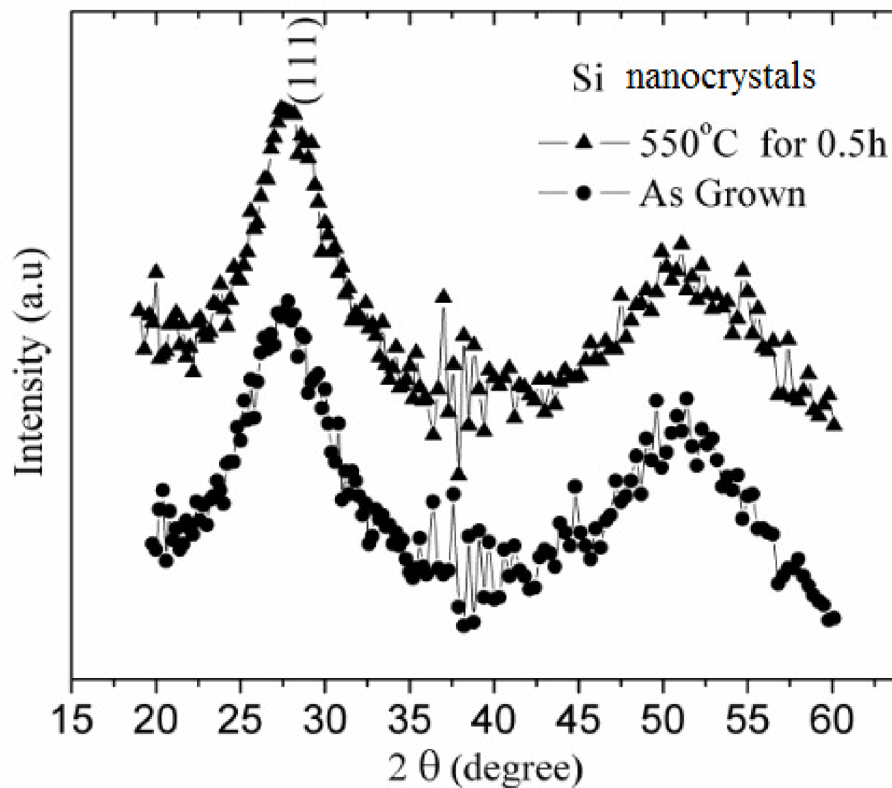


Fig. 6.3: Post-deposition thermal annealing influence on the developed Si nanocrystals at 550°C for 0.5h.

6.2.3 Micro-Raman Analysis

Figure 6.4 shows the Raman spectra of the developed structure. It is evident that the Raman spectra for the developed structures at this regime are composed of Si NCs embedded in amorphous silicon matrix. The spectra in general consist of a sharp peak related to the Raman crystalline peak and a very weak broadening peak corresponding to the amorphous silicon matrix. The position of the crystalline-like peak is found to be downshifted between 15.75 to 8.5 cm^{-1}, (compared to c-Si reference), depending on the HD ratio.

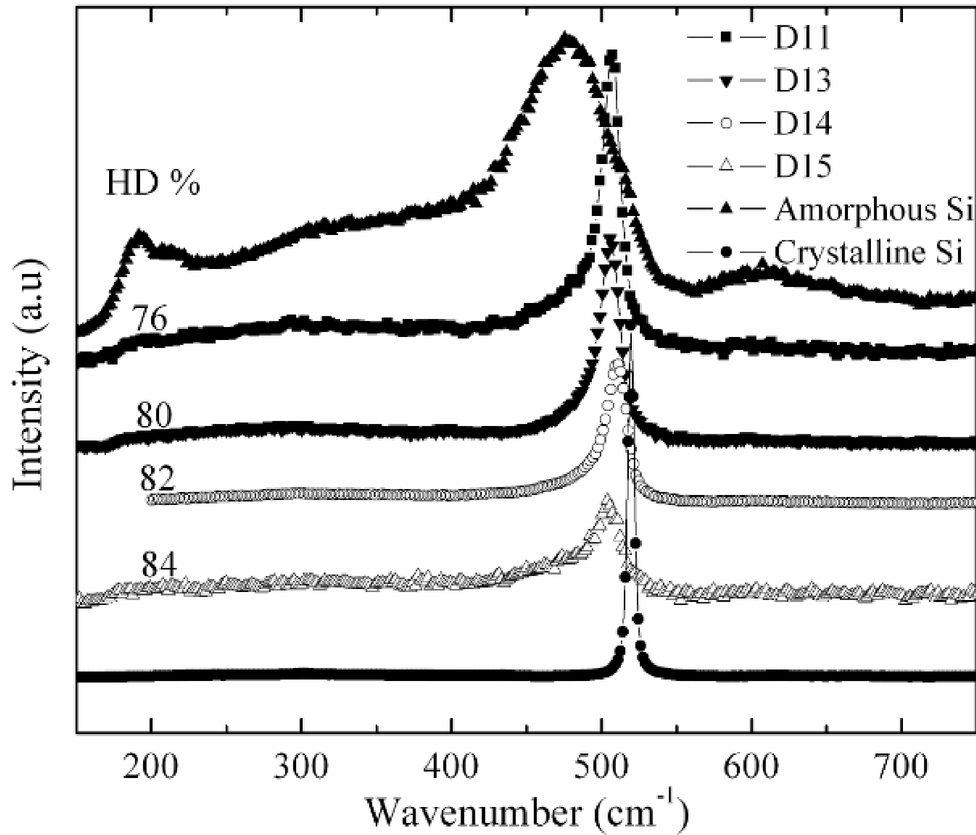


Fig. 6.4: Micro-Raman spectra of the developed Si nanocrystals, the spectra for *a* Si and crystalline substrate are presented.

Size of the embedded crystalline Si NCs in amorphous Si matrix can be studied using Raman spectroscopy (this analysis is not included here). Crystalline Raman peak exhibits a frequency shift and peak broadening due to the phonon confinement effect for Si nanostructures [51]. The band-shape modification of the Raman peak (for Si nanostructures) has been explained using different theoretical models. These models quantified the phonon confinement and allow the determination of the Si-crystallite size. The most widely used model is the correlation length model [142, 167]. Nevertheless, this model does not give an acceptable explanation of the Raman band-shape modification below 5 nm. Indeed, Zi's model (Eq. 6.2) [168] is adapted for crystallite size below 4–5 nm, while correlation length model gives a good description of the Raman band-shape modification for crystallite size between 4 and 20 nm [169]

$$\Delta\omega(L_z) = -A(\frac{\alpha}{L_z})^{\gamma} \tag{6.2}$$

where, $\Delta\omega(L_z)$ is the Raman shift in a nanocrystals with diameter L_z, a is the network constant of Si (α=0.543 nm), and A= 47.41 cm^{-1} and γ=1.44 are fit parameters that describe the phonon confinement in nanometric spheres of diameter [170]. According to our extensively crystallite size analysis using both HRTEM and X-Ray we deduce that, the average size of our structure is less than 5 nm. The crystallite size calculated using x-ray (111) peak analysis are shown in table 6.1

Table 6.1: Calculated Si nanocrystals Si NCs size from x-ray diffraction pattern.

Sample	Hydrogen Dilution (%)	Silane concentration (%)	*L*(111) (nm)
D11	76	31.6	1.2
D13	80	25.0	2.1
D14	82	21.9	1.7
D15	84	18.9	2.5

For Si nanostructures dispersed in *a* Si:H matrix, the band gap of Si NCs should be higher than that of a Si:H (~1.8) to prevent the carriers from recombining in the prepared nanostructures [171]. We expect the optical band gap of the developed Si NCs to be in the range of 1.8-2.2 eV [172] depending on the measured diameter from different techniques. These developed nanostructures are beneficial, especially if they used for advanced photovoltaic systems, like tandem structure.

6.3 Device integration and photovoltaic properties

Figure 6.5 shows a schematic diagram of the proposed structure for the deployment of the developed Si NCs on the conventional epitaxial silicon solar cell (which developed and presented in detailes in chapter 5). Where, the conventional procedure for the deposition process of the epitaxial layer exactly achieved as described in chapter 3 and 5. On the top of this developed epitaxial silicon solar cell a thin phosphorous doped (3-5 nm) of Si NCs is deposited on the top of the cells at the same chamber before unloading the wafer from the PECVD chamber, followed by 70-75 nm of SiN: H as antireflection coating (not shown on the schematic diagram). The purpose of the Si NCs layer is to enhance the photon absorption through its wide band gap. On the other hand, the amorphous silicon matrix is working as the passivation layer, since *a* Si:H is a very good candidate for the passivation process of the top surface of the developed epitaxial film.

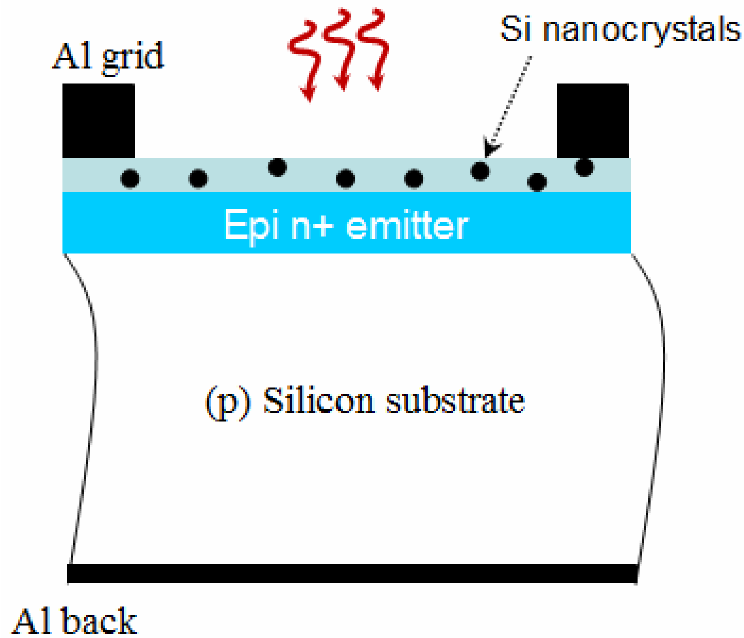


Fig. 6.5: A Schematic drawing of the fabricated device with Si nanocrystals embedded into amorphous silicon matrix.

We introduced this film in a test device structure, the I-V characteristic is shown in figure 6.6. Figure 6.6 shows one of the measured IV for the fabricated devices, composed of a conventional epitaxial silicon solar cell with 3 nm Si NCs layer on top. The open-circuit voltage (V_{oc}) did not change significantly, since there is no change in the electronic properties of the semiconducting material [173]. However the device emitter is far from optimal because of its increased thickness and poor metal contact with the amorphous surface may have contributed a low fill factor. Nevertheless, it is noticed that, the short circuit current I_{sc} value is enhanced by ~12% if we deposited the nanocrystals layer on top of the conventional devices. This enhancement in the short circuit current agrees with the calculated values by van Sark et al [174] for multi-crystalline using Si NCs on the front surface.

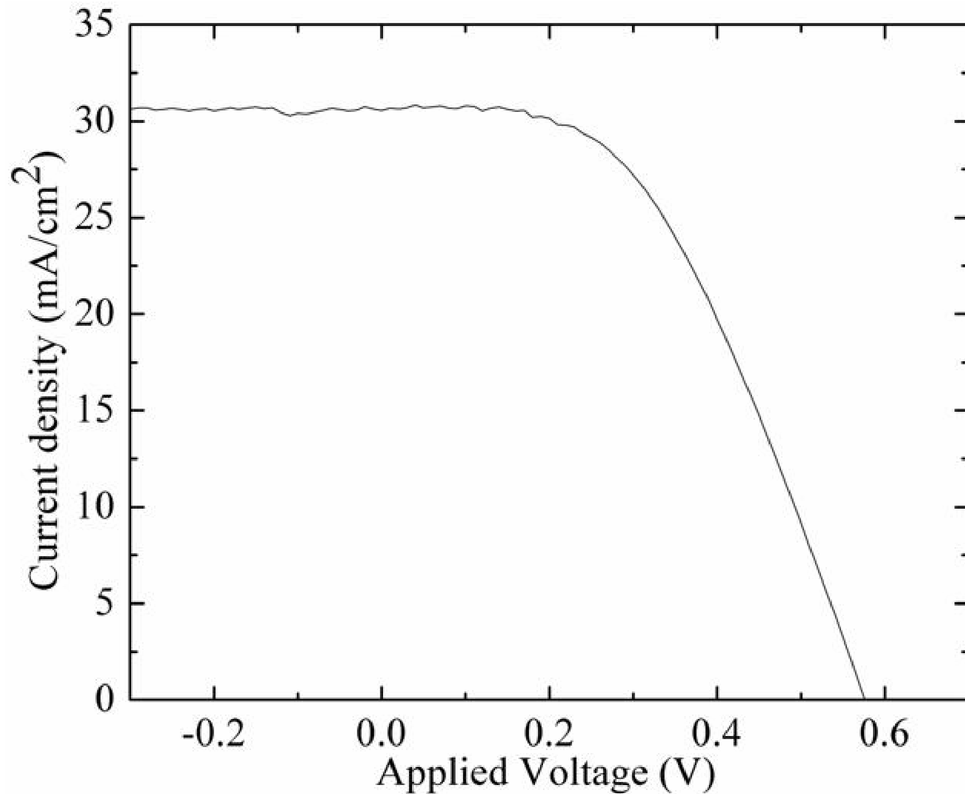


Fig. 6.6: Measured IV of the fabricated epitaxial silicon solar cell (dashed line) and with applying nanocrystals layer on cell front surface (solid line), using the following structure; *Al (front grid)/ SiN_x:H /3 nm nanocrystals layer-50 nm n^+ epitaxial Si /p-type Cz/ Al (back contact)* and under EP1 processing conditions on (100) flat silicon substrate.

6.4 Summary and conclusions

Embedded Si NCs in amorphous silicon matrix has been fabricated and extensively analyzed using cross sectional HRTEM to be used on LT *n+ epi/p* homojunction Si solar cells' top surface, by appropriately choosing the precursor compositions, plasma power density, chamber pressure, and controlled H_2 flow for the development of the nanocrystals embedded films. Crystallinity and interface properties are investigated for process variations. Ultra High resolution transmission electron microscopy (UHRTEM) was used to analyze the size, density, shape and structure of the developed Si NCs in the amorphous Si:H matrix. Micro-Raman spectroscopy and glancing angle x-

ray diffraction XRD were used to study the crystallinity and size of the developed Si NCs. A comprehensive calculation and analysis of the sizes of the developed nanostructures were presented depending on Micro-Raman and glancing x-ray measurements. It is shown from UHRTEM analysis the size of the Si NCs are in the average of 2.5 nm and isolated by 10-20 nm of amorphous silicon matrix, randomly distributed and have spherical shape. The optical band gap corresponding to this developed Si NCs is found to be 1.8-2.2 eV. The developed layers could be used as a good passivation scheme due to the amorphous silicon matrix. So, different devices were fabricated using the Si NCs layers on top of the conventional n-type epitaxial silicon solar cell. An enhancement in the short circuit current I_{sc} value is noticed for the devices fabricated using these nanocrystals.

Chapter 7: Conclusions and Contributions

In our research we developed an efficient, stable and affordable silicon solar cell device using epitaxial films. We used the developed epitaxial films to fabricate different silicon solar cells devices. We processed these devices at low processing temperature using plasma enhanced chemical vapor deposition (PECVD).

In this device the junction between the phosphorous or boron-doped epitaxial film is formed between the film and the p or n-type crystalline silicon (c-Si) substrate, giving rise to (n *epi-Si*/p c-Si device or p *epi-Si*/n c-Si device), respectively.

Different processing conditions were used to develop high quality epitaxial films that were used in the fabrication of different silicon solar cells architectures. The main processing conditions that influenced the quality of the structure were; radio frequency (RF) power density, the processing chamber pressure, the substrate temperature, the gas flow rate used for deposition of silicon films, and hydrogen dilution. Extensive analysis of the fine structure of the epitaxial films, using high resolution transmission electron microscope (HRTEM), showed that hydrogen dilution played a crucial role in the epitaxial growth of highly phosphorous doped silicon films. We achieved the best result, in terms of structure and electrical properties, at intermediate hydrogen dilution (HD) regime between 91 and 92% under the optimized deposition conditions.

-The network structure of the epitaxial films was probed using Raman spectroscopy by a laser beam with a wavelength of 328 and 442 nm. Raman Spectroscopy measurements revealed a very strong Raman intensity peak at 520 cm^{-1} for the developed films at 91.6% and 95 % HD, similar to the Raman intensity of the monocrystalline silicon substrate. During the analysis we did not observe the

characteristic peaks that are related to amorphous silicon (*a* Si:H), which confirmed there was no amorphous tissue in the interatomic crystalline structure of the epitaxial film.

-A full electrical characterization of the epitaxial film was carried out using spreading resistance profile (SRP) technique through the detection of active carriers inside the developed films. Measurements of the active phosphorous dopant revealed that, the film has a very high active carrier concentration of an average of 5.0 $x10^{19}$ cm^{-3}. From the SRP and SIMS analyses, we concluded that the epitaxial film has a uniform carrier concentration profile that represents a uniform distribution of phosphorous dopants along the epitaxial growth direction. Measurements of the free electron density inside the epitaxial phosphorous doped film showed that, at the interface between the substrate and the epitaxial film the density value increased to $1.2x10^{20}$ cm^{-3}. This very high concentration of free carriers at the interface enhanced the mobility of the developed epitaxial films. In conclusion, the developed epitaxial films deposited on Si substrate using the developed processing conditions at 91% and 92 % HD have the highest reported conductivity of approximately 10^3 $\Omega^{-1}cm^{-1}$ comparable to the conductivity of highly doped high temperature diffused c-Si.

-The epitaxial process at very high HD > 99 % was studied in detail on silicon substrate. However, these films deposited at a very HD regime it is noticed that the developed films have defective areas which confirmed by HRTEM analysis. So, we believe that the role of hydrogen is changing to the etching mode at HD that affects the film structure. The influence of the substrate orientation on the epitaxial growth was characterized and analyzed. The best substrate that promote epitaxial growth using our optimized processing conditions was found to be the (100) orientation substrate over the other orientations, as (111) and (110).

- Chemical impurities were extensively measured and detected by SIMS analysis. High levels of carbon and oxygen can affect on the mobility of electrons in the growing silicon films. Hence, the

levels of these elements should be monitored and kept in acceptable level. Oxygen concentration analysis revealed that, no peaks were detected near the interface and the concentrations flatten through the bulk of the film with a concentration of 6.57 x 10^{17} cm^{-3}. While for carbon concentration, we noticed two peaks, the first one is at the upper surface of the film with concentration of 2.49 x 10^{19} cm^{-3} and the second peak appeared at the epilayer/substrate with concentration of 8.21 x 10^{18} cm^{-3}.

- We developed different annealing temperature profiles using rapid thermal process (RTP) as a fast, clean and low thermal budget to enhance the structure, and the electrical properties of the low quality films that influenced by the substrate temperature and/or orientation. The RTP process was applied to activate the non-active dopant inside the epitaxial grown films. Three main temperature profiles were optimized and applied on the developed silicon films. A perfect coincidence between the real and the programmed annealing RTP profiles was noticed. Different heating and cooling rates were used and optimized to enhance the film structure. For example, we used the pulsed RTP profile with a very high heating rate up to 70 ^{o}C/s and cooling rates equal to 35°C/s. In addition we used the multisteps RTP temperature profile which characterized by the low heating and cooling rates. We noticed that, the temperature profiles with low heating and cooling rates are more beneficial for the annealed films due to the hydrogen effusion issue which has its influence on the film structures as confirmed by HRTEM and SIMS analysis. Where, the hydrogen concentration was measured in the epitaxial films using SIMS analysis and it is found to be 1 x 10^{21} cm^{-3}. After applying the RTP process the hydrogen content was decreased as confirmed by SIMS analysis. In addition, a slightly mismatch between the single crystalline substrate and the first atomic layers of the epitaxial films are detected at the interface after applying the pulsed RTP profile, as confirmed by HRTEM micrographs. This defective layer near the interface increases the defect density due to this mismatch (due to very high heating and cooling rates) and may resulting in more recombination centers at the interface. Moreover, applying the annealing process using the different temperature profiles on the epitaxially grown

emitters resulted in a deep diffusion of the phosphorous dopant. This result is noticed more in the pulsed RTP profile, which increase the junction depth by approximately 35 nm, while for the two step RTP profile the junction shifted by 17 nm. The electrical properties annealed films by RTP were characterized. The measured resistivity and sheet resistance of the developed epitaxial films by RTP were 7.6 x 10^{-4} Ω cm and 38 Ω □. These measured values for the developed epitaxial phosphorous doped films confirmed that the annealed film is a very good candidate that can be used as an emitter in the developed silicon solar cells. On the other hand, the doping efficiency η_d is enhanced by 10~20 % by applying RTP for 60 sec at intermediate annealing temperature (750°C) using RTP temperature profile.

-Not only we developed phosphorous doped epitaxial silicon films but also we developed and investigated the structure quality and electrical properties of the epitaxial boron doped silicon films using (Trimethylborane) TMB. The developed films could be used as an emitter in a p^+n single solar cell structure and as a back surface filed (BSF) layer in n^+pp^+, that can enhance the efficiency of the prepared devices. The extensive HRTEM analysis showed that, the structural defects as, twins, stacking faults and mismatch between the different inter-atomic layer structures appeared between 8-10 nm regions. These defects are leading to the breakdown of the epitaxial structure region. Obviously, we noticed that this termination takes place at nearly the same distance from the interface yielding an abrupt transition from the epitaxial layer to amorphous layer. A mixture of crystalline structure separated by amorphous silicon areas was the main feature of the third region; in which a completely amorphous phase was noticed as confirmed by HRTEM. The electrical properties and the free carrier density of the deposited boron doped TMB films was analyzed using SRP. We found that near the interface region (up to 20 nm) a free carrier concentration of ~ 4.5 x10^{16} cm^{-3} was detected. The measured film resistivity was ~ 10^{-1} Ω cm, with a calculated conductivity of 10 Ω^{-1} cm^{-1}. Due to the low film conductivity, the applying of the RTP is a crucial step to enhance both the crystallinity of

the amorphous layer, appeared after the breakdown of the quasi-epitaxial layer, and to activate the boron therein which will yield higher free carriers and conductivity. The annealed boron doped silicon films has a uniform and a flat distribution of boron depth free carrier profile. Free carrier density was measured using SRP technique and it was increased up to 9 $x10^{19} cm^{-3}$ after RTP. By applying the RTP we enhanced the conductivity and the mobility of the free carriers that can make the developed films a very good candidate for solar cell device fabrication. A minimum resistivity of 8 x 10^{-3} Ω cm is obtained with maximum conductivity value of 120 Ω^{-1} cm^{-1} after applying RTP process.

-Different sizes diode structures were fabricated using the developed highly phosphorous doped epitaxial films to investigate the electrical properties such as the ideality factor and the saturation current. The measured ideality factor of the as deposited epitaxial phosphorous doped diodes using the *Al front contact/ (n+Si epitaxy film)-EP1 conditions / (p) c-Si/Al back contac*t in low forward bias and medium forward bias regions are 1.93 and 1.16, respectively. We noticed a uniformity of the I-V characteristics for the as deposited and annealed diodes.

-The developed epitaxial Si films were used to fabricate different silicon solar cells using different architectures which have the advantage of simplicity and compatibility with the industry for the large scale production. Variety of proposed structures were fabricated and characterized on planar and textured surfaces. For the fabricated devices using the developed epitaxial phosphorous doped films, The photovoltaic properties of the fabricated solar cells were extensively characterized using solar simulator and using standard measurement conditions. The measured V_{oc} values were in the range of 575-580 mV for the devices developed on the planar surface with a good fill factor (FF) values in the range of 74-76 %. This good value for the fill factor is a good indication of the low series resistance, for the devices fabricated even without applying RTP. The applying the RTP for a very short time (60 s) at moderate temperature of 750°C, the V_{oc} and I_{sc} enhances with the values of 598 mV and 27.5

mA, respectively and a fill factor up to 76 % leading to an efficiency of 12.5 %. Hence, the efficiency is enhanced by 13.06 % over the reference cell.

-We used the light trapping technique (by surface texturing using alkaline solutions) to enhance both V_{oc} and I_{sc}. We found that V_{oc} and I_{sc} for the textured surface increased to 612 mV and 31mA, respectively and fill factor of 76 % leading to an efficiency of up to 13.8%. A noticeable efficiency enhancement by approximately 20 % over the reference cell without RTP annealing process is reported for the developed devices on the textured surfaces. Different device design of boron doped quasi-epitaxial growth films using TMB as the dopant source are fabricated and tested under low temperature process using PECVD system.

Moreover, we investigated another technique to enhance the efficiency of the fabricated epitaxial silicon solar cells by the deployment of silicon nanocrystals (Si NCs) on the top surface of the fabricated devices. By appropriately choosing the precursor compositions, plasma power density, chamber pressure, and controlled H_2 flow are used to develop the nanocrystals embedded films. The developed structure was extensively analyzed using cross sectional HRTEM. It is shown from the HRTEM analysis that the developed Si NCs, are randomly distributed, have a spherical shape with a radius of approximately 2.5 nm, and are 10-20 nm apart in the amorphous silicon matrix. Glancing angle x-ray diffraction XRD was used to study the crystallinity and size of the developed silicon nanocrystals. Based on the size of the developed Si NCs, the optical band gap was found to be in the region of 1.8-2.2 eV. The developed layers applied on the front surface of the developed epitaxial silicon solar cells. A noticeable enhancement of the I_{sc} was reported after applying this layer.

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