Investigation of Time Domain Modulation and Switching-Mode Power Amplifiers Suitable for Digitally-Assisted Transmitters

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Innovation in wireless communication has resulted in accelerating demand for smartphones using multiple communications protocols such as WiFi, Bluetooth and the many cellular standards deployed around the world. The variety of frequency, bandwidth and power requirements associated with each standard typically calls for the implementation of separate radio frequency (RF) front end hardware for each standard. This is a less-than-ideal solution in terms of cost and device area. Software-defined radio (SDR) promises to solve this problem by allowing the RF hardware to be digitally reconfigurable to adapt to any wireless standard. The application of machine learning and cognition algorithms to SDR will enable cognitive radios and cognitive wireless networks, which will be able to intelligently adapt to user needs and surrounding radio spectrum conditions.

The challenge of fully reconfigurable transceivers is in implementing digitally-controlled RF circuits which have comparable performance to their fixed-frequency counterparts. Switching-mode power amplifiers (SMPA) are likely to be an important part of fully reconfigurable transmitters since their switching operation provides inherent compatibility with digital circuits, with the added benefit of very high efficiency. As a step to understanding the RF requirements of high efficiency and switching PAs, an inverse class F PA in push-pull configuration is implemented. This configuration is chosen for its similarity to the current mode class D (CMCD) topology. The fabricated PA achieves a peak drain efficiency of over 75% with 42.7 dBm (18.6 W) output power at 2.46 GHz.

Since SMPAs cannot directly provide the linearity required by current and future wireless communications standards, amplitude information must be encoded into the RF signal in a different way. Given the superior time resolution of digital integrated circuit (IC) technology, a logical solution is to encode this information into the timing of the signal. The two most common techniques for doing so are pulse width modulation and delta-sigma ($\Delta\Sigma$) modulation. However, the design of $\Delta\Sigma$ modulators requires simulation as part of the design process due to the lack of closed-form relationships between modulator parameters (such as resolution and oversampling) and performance figures (such as coding efficiency and signal quality). In particular, the coding efficiency is often ignored although it is an important part of ensuring transmitter efficiency with respect to the desired signal. A study of these relationships is carried out to observe the tradeoffs between them. It is found that increasing the speed or complexity of a $\Delta\Sigma$ modulated system does not necessarily translate to performance benefits as one might expect. These observations can have a strong impact on design choices at the system level.

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Nomenclature

η_c	Coding efficiency
η_D	Drain efficiency
$\Gamma_{L,n}$	Load reflection coefficient at the n^{th} harmonic
λ	Wavelength
ω_c	Carrier frequency in rad/s
$\theta(t)$	Phase component of $g(t)$
ε_i	Quantization error
$A(t)$	Amplitude component of $g(t)$
A_p	Amplitude limit for PWM
C_{DS}	Parasitic drain-source capacitance
f_b	Baseband bandwidth
f_c	Carrier frequency in Hz
f_s	Sampling frequency in Hz
$g(t)$	Complex envelope signal
$I(t)$	Real (**I**n-phase) component of $g(t)$
I_0	DC component of drain current
I_Q	Quiescent current
I_{max}	Peak drain current

L_{ch}	RF choke inductance
n_i	Quantization noise of $\Delta\Sigma$ modulator
$p(t)$	PWM signal
$p_n(t)$	n^{th} pulse in a PWM signal
P_{DC}	Supplied DC power
P_{in}	RF input power
P_{RF}	RF (output) power
$Q(t)$	Imaginary (**Q**uadrature) component of $g(t)$
R_L	Load resistance
r_o	Small signal transistor output resistance
r_{on}	Switch on-state resistance
$s(t)$	RF signal
T_p	Pulse period
T_s	Sampling period
$T_{p,n}$	Duration of n^{th} pulse
V_{DD}	Drain supply voltage
V_{DS}	Drain-source biasing voltage
v_{DS}	Drain-source total voltage
V_{GG}	Gate supply voltage
V_{SS}	Source supply voltage
Z_0	Transmission line characteristic impedance
$Z_{L,n}$	Load impedance at the n^{th} harmonic
$Z_{S,n}$	Source impedance at the n^{th} harmonic
3GPP	3$^{\text{rd}}$ Generation Partnership Project

ΔΣ	Delta-sigma (modulation)
ADPLL	All-digital phase-locked loop
ADS	Agilent Advanced Design System
AM	Amplitude modulation
AMO	Asymmetric multilevel outphasing
BiCMOS	Bipolar CMOS
BPF	Bandpass filter
bps	Bits per second
CDMA	Code division multiple access
CIFB	Cascade of integrators with feedback
Class F^{-1}	Inverse class F (amplifier)
CMCD	Current-mode class D (amplifier)
CMOS	Complementary metal-oxide-semiconductor
CR	Cognitive radio
CWN	Cognitive wireless network
DAC	Digital-to-analog converter
DC	Direct current
DCXO	Digitally controlled crystal oscillator
DDRM	Direct digital RF modulator/modulation
DRFC	Digital-to-RF converter
DRP	Digital RF Processor
DSP	Digital signal processor/processing
EER	Envelope elimination and restoration
EM	Electromagnetic

EVM	Error vector magnitude
FDD	Frequency division duplexing
FEM	Front-end module
FIR	Finite impulse response
FPGA	Field programmable gate array
GaAs	Gallium arsenide
GaN	Gallium nitride
GPP	General purpose processor
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HEMT	High electron mobility transistor
IC	Integrated circuit
IF	Intermediate frequency
IS-95	Interim Standard 95
LDMOS	Laterally-diffused metal-oxide-semiconductor
LINC	Linear amplification with nonlinear components
LO	Local oscillator
LTE	3GPP Long Term Evolution
LUT	Lookup table
MMIC	Monolithic microwave integrated circuit
NTF	Noise transfer function
OFDM	Orthogonal frequency division multiplexing
OFDMA	Orthogonal frequency division multiple access
OSR	Oversampling ratio

PA	Power amplifier
PAE	Power-added efficiency
PAPR	Peak-to-average power ratio
PCB	Printed circuit board
PM	Phase modulation
PWM	Pulse width modulation
QAM	Quadrature amplitude modulation
RB	Resource block
RCE	Relative constellation error
RF	Radio frequency
SDR	Software-defined radio
SiGe	Silicon germanium
SMPA	Switching-mode power amplifier
SNR	Signal-to-noise ratio
STF	Signal transfer function
UE	User equipment
UMTS	Universal Mobile Telecommunications System
VMCD	Voltage-mode class D (amplifier)

Chapter 1

Introduction

In today's connected world, consumers and organizations are continually searching for more convenient ways of connecting with those around them. The demand for smartphones—capable of much more than just mobile telephony—has increased dramatically in the last decade and continues to accelerate. Such devices use multiple communications protocols and standards depending on the application. For example, cellular network standards, local area standards such as IEEE 802.11 (WiFi), short-range standards such as Bluetooth, and the Global Positioning System (GPS) are commonly found in today's smartphones. In addition, the standards in place vary among geographical locations, especially in the case of cellular networks. For example, the Global System for Mobile Communications (GSM) standard is a common cellular standard used all over the world. However, there are four major frequency bands used for GSM and which one is in use varies with location and service provider.

Each of the numerous wireless standards implemented in a particular mobile or base station transceiver has its own RF requirements in terms of carrier frequency, bandwidth and power level. A typical approach is to design and implement each standard separately, each with its own radio frequency (RF) front-end module (FEM), which are then incorporated into a single device as illustrated in Figure 1.1. Indeed, in the case of GSM, handsets supporting the four major bands include separate RF hardware for each band. This requires high cost and device area, both of which are important factors in the competitive mobile communications market.

A more suitable approach would be to use a single, highly reconfigurable FEM to incorporate all the desired functionality, with the possible exception of the ability to use multiple standards simultaneously. The configuration would be controlled through the use of software and, by extension, digital circuits. This can potentially eliminate a large portion of redundant circuitry and allow for adaptability to new wireless standards as they are finalized and deployed. Such software-defined radios (SDR) are the key to enabling cognitive wireless networks: systems allowing for intelligent adaptation of radio hardware and signal processing to the current needs

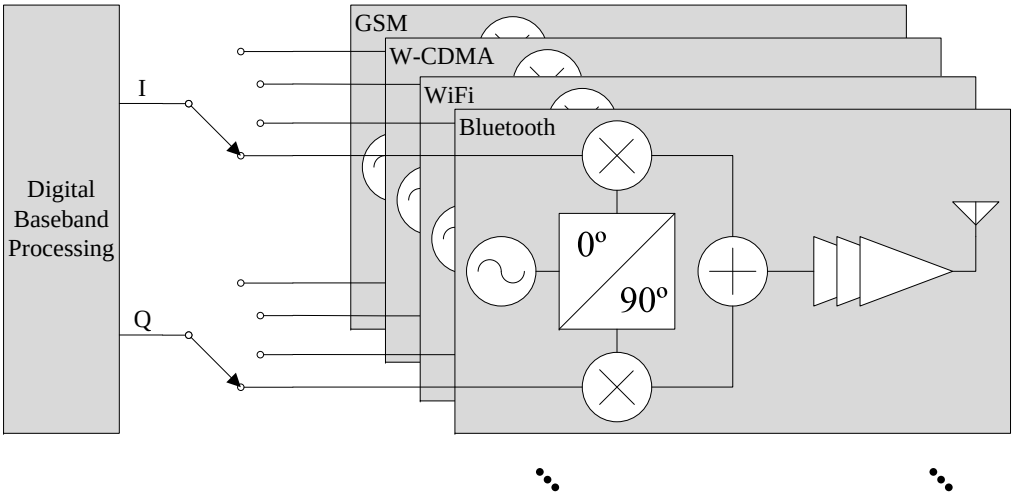


Figure 1.1: Multiple standards using multiple RF FEMs.

of the user and to the surrounding radio environment. These have the added benefit of using the radio spectrum in a more intelligent and efficient way than currently.

The defining challenge of software-defined radio lies in realizing digitally-controlled circuits which can achieve RF performance comparable to existing solutions in a robust and cost-efficient way. Conventional direct conversion transceivers place the digital-to-analog interface between the digital baseband signal generation (or decoding) circuitry and the mixers. The RF components including mixers, oscillators, amplifiers, switches, filters and antennas are implemented for a single carrier frequency and bandwidth with fixed-value or coarsely tunable components. This fundamentally limits their ability to adapt to the different RF requirements of different standards.

High-performance RF power amplifiers (PA) are a particular example of a challenging building block to implement in a reconfigurable manner. Efficient DC-to-RF power conversion and high linearity are the key performance metrics in a PA design, assuming the basic output power and gain requirements have been met. Since the PA is the most power-hungry RF component in any transceiver, high efficiency is required to maximize battery life in mobile handsets and minimize operating expenses (i.e., electricity) for the wireless infrastructure. In addition, the high peak-to-average power ratio (PAPR) demanded by wireless standards requires a highly linear PA. The linearity and the efficiency are two conflicting requirements, and a typical PA reflects a carefully considered tradeoff between the two. The complexity and difficulty of building reconfigurability into the PA presents an additional challenge.

Several innovations promise to help significantly in the implementation of reconfigurable RF front ends, and in particular PAs. For example, switching-mode PAs (SMPA) may be particularly well-suited for direct amplification of digital signals, due to the operation of the active device as a switch as in digital circuits. In addition to this inherent degree of compatibility with digital

electronics, most classes of SMPA have the advantage of theoretically being able to provide 100% efficiency. Advances in transistor technology have increased the switching frequency of transistors, thereby enabling implementations of high-performance SMPAs with ever-increasing efficiency. However, the amplification of signals with high PAPR remains an important limitation of SMPAs, due to the highly nonlinear switching operation of the transistor. Moreover, the advances in digital integrated circuit (IC) technology have led to lower and lower supply voltages, decreasing the available voltage headroom in which information can be encoded with an acceptable signal-to-noise ratio (SNR).

One solution is to take advantage of the extremely fast switching speeds of digital IC processes and encode information into the time domain, using the timing of the state transitions. For example, pulse width modulation (PWM) encodes amplitude information into the duty cycle of a square wave, and can additionally provide phase information using the positioning of the pulse. Delta-sigma ($\Delta\Sigma$) modulation similarly encodes information into pulse density in the case of two-level $\Delta\Sigma$ modulator.

This thesis explores the theory and design of SMPA and time-encoded signal generation techniques, and is organized as follows:

- Chapter 2 explains in further detail the key concepts of cognitive wireless networks, reconfigurable transmitters, SMPA and time-encoded signal generation.
- Chapter 3 presents the design and implementation of a class F^{-1} PA in push-pull configuration, as an example of a high efficiency PA.
- Chapter 4 studies the performance of $\Delta\Sigma$ modulation techniques with respect to key parameters.
- Finally, Chapter 5 concludes this thesis with a discussion of the potential for further research in these areas.

Chapter 2

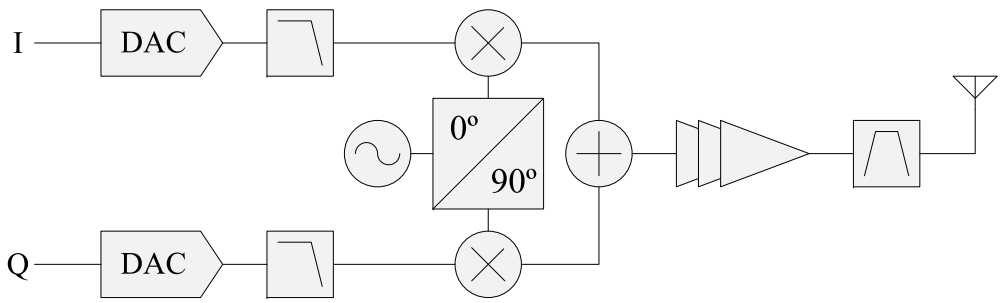
Background

As outlined in Chapter 1, all of the constituent RF—and intermediate frequency (IF)—blocks in a transceiver are typically designed and implemented with fixed-value electronic components. This approach allows only a fixed or limited frequency and bandwidth of operation, with the possible exception of the local oscillator (LO). Such components are targeted for a specific application or communications standard in a specific frequency band, so any handset or infrastructure supporting multiple standards must also incorporate an FEM for each supported standard.

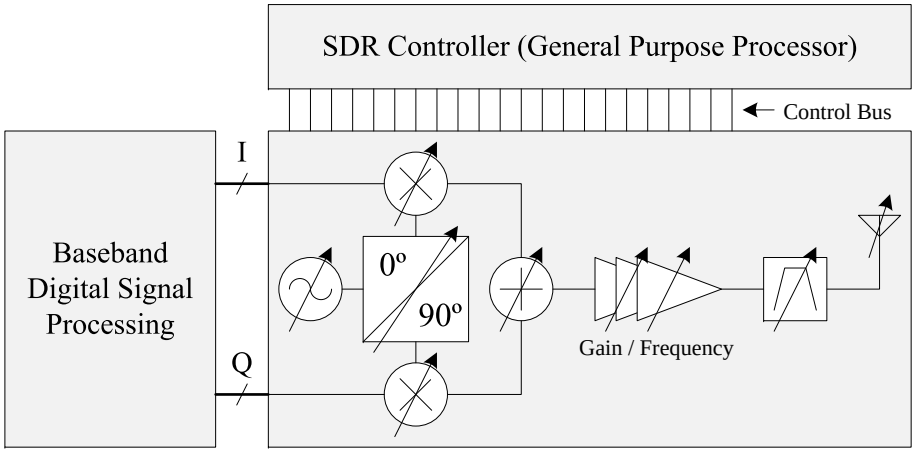
Highly reconfigurable RF devices and circuits, which are compatible with existing digital circuits, are an important part of enabling SDR and eventually cognitive wireless networks. This chapter provides relevant background information on cognitive radios (CR) as well as for the particular implementation details which are the subject of this thesis. Section 2.1 describes the concepts of ideal cognitive networks and the key enabling technology of SDR as compared to conventional transceiver techniques. Section 2.2 provides an overview of practical transmitter architectures and circuits which are suitable for reconfigurable and software-defined radio. Section 2.3 studies SMPAs in the context of their potential to provide high performance while being suitable for use in SDR. In particular, the current mode class D (CMCD) amplifier and the inverse class F (F^{-1}) amplifier are discussed in detail. Finally, Section 2.4 discusses time-domain signal modulation techniques, which have proven to be a suitable class of techniques for enabling compatibility between RF circuits and digital circuits.

2.1 Software-Defined Radio, Cognitive Radio and Cognitive Networks

The idea of SDR first appeared in the late 1990s. Programmable digital signal processors (DSP) and general purpose processors (GPP) were used to perform most of the signal generation, mod-



(a) Conventional Transmitter.



(b) Ideal SDR.

Figure 2.1: Comparison of conventional transmitter and ideal SDR.

ulation and related functions [1]. Manufacturers recognized the potential flexibility afforded by using general-purpose electronics and so used the term "software-defined radio" to express this potential. This functionality was, however, limited to baseband processing.

Over the years the definition of SDR has expanded to include the transfer of RF and IF functions to the digital domain in order to provide increased flexibility of the frequency and bandwidth characteristics of the transceiver. In an SDR the digital-to-analog interface is ideally located directly before the antenna, so that the only analog signal involved is that which is transmitted or received over the air. In the extreme case even the antenna may be digitally reconfigurable to the application at hand (e.g., [2]). Figure 2.1 illustrates the concept of the ideal SDR versus conventional transceivers.

The ideal SDR can support any wireless communication standard since the entire transceiver from baseband to antenna is fully tunable in frequency and bandwidth. Reconfigurable/tunable

implementation of the transceiver and its components is a broad and active area of research. The problem rests on implementing RF/IF components in a robustly reconfigurable way while achieving performance comparable to that of existing analog hardware. Today this is done to an extent by switching between multiple sets of RF/IF hardware depending on the desired frequency band, as is typical in multi-band GSM handsets for example. However, this is not a robust solution as it provides no support for competing standards or for wireless standards to be deployed in the future.

In his doctoral thesis [3] Joseph Mitola III envisioned a layer of machine learning and cognition algorithms to control the SDR: the *cognitive radio*. In this way a user's needs can be met in a broad variety of contexts and applications using a single, highly adaptive and reconfigurable radio. Ideally a CR can use whatever information is available to it through various sensors (e.g., spectral sensing, microphone or camera) to determine the current context and activities of the user and act accordingly. Note that although some confusion exists about the difference between SDR and CR, SDR refers solely to the digitally reconfigurable radio platform and CR refers to the additional cognitive and learning processes which may control an SDR [4].

The deployment and proliferation of CR enables cognitive wireless networks (CWN). One of the first descriptions of cognitive networks appeared in [4]. Thomas et al. defined the cognitive network as having

> a cognitive process that can perceive current network conditions, and then plan, decide and act on those conditions. The network can learn from these adaptations and use them to make future decisions, all while taking into account end-to-end goals.

The CWN should possess, among other things, the ability to manage spectral resource efficiently and effectively. RF spectrum shortage is increasingly problematic, especially given the accelerating demand for high-speed mobile data. CWNs are thus a highly active area of research as they promise a solution to this issue, assisting infrastructure operators in making the most effective use of their highly expensive licensed spectrum.

2.2 Practical Architectures for Reconfigurable Transmitters

As part of enabling SDR and CR, a number of modifications have been proposed to make the transmitter more reconfigurable and suitable for SDR applications. This section will highlight some examples of recent advances in digitally-assisted and reconfigurable transmitter technology. They fall into two distinct categories: quadrature modulation and polar modulation.

2.2.1 Quadrature Modulated Transmitters

The structure of a simplified conventional direct conversion radio transmitter is shown above in Figure 2.1(a) (page 6). Baseband information is encoded in a complex envelope signal

$$g(t) = I(t) + jQ(t). \tag{2.1}$$

This modulates the amplitude and phase of the carrier tone according to

$$\begin{aligned} s(t) &= \mathrm{Re}\left[g(t)e^{j\omega_c t}\right] && (2.2)\\ &= I(t)\cos(\omega_c t) - Q(t)\sin(\omega_c t) && (2.3)\\ &= I(t)\cos(\omega_c t) + Q(t)\cos\left(\omega_c t + \frac{\pi}{2}\right) && (2.4) \end{aligned}$$

where $s(t)$ is the transmitted signal and ω_c is the carrier frequency in rad/s. $I(t)$ and $Q(t)$ are known as the *in-phase* and *quadrature* components of the information, respectively. This modulation technique is known as quadrature amplitude modulation (QAM) or vector modulation, and is the basis of virtually all modern wireless communications systems.

The I and Q components arrive at the transmitter in digital form and are converted to analog using a digital-to-analog converter (DAC). They are then filtered to occupy only the allotted bandwidth, then upconverted to the carrier frequency using mixers. The LO for the Q mixer leads that for the I mixer by $\pi/2$ or 90°. The two components of the signal are then combined and amplified before being radiated by an antenna. There may also be additional filters and linearization techniques to attenuate unwanted emissions caused by nonidealities of various components, and an IF stage may also be used to suppress LO leakage.

Eloranta et al. proposed direct digital RF modulation (DDRM) as a highly flexible architecture for QAM [5–8], shown in Figure 2.2. The heart of the architecture is the digital-to-RF converter (DRFC) which itself consists primarily of two differently-weighted sets of unit Gilbert cell mixers as shown in Figure 2.3. This circuit moves the digital-analog interface closer to the PA stage by combining the functions of the DAC and mixers. Digital interpolation and filtering is performed on each component to ensure compatibility between the low sampling rate at baseband and the high sampling rate required by the DRFCs. The DRFCs then upconvert each signal component to RF and the two components are combined and amplified in the usual way. The specifications of the system depend primarily on the unsampling filter parameters which are easily reprogrammed. This is the system's principal advantage. However, this system does not address the PA stage, which is one of the most challenging blocks to implement in a reconfigurable way. Nevertheless, the DDRM architecture successfully increases the digital portion of the transmitter, thereby reducing the amount of hardware required for multi-mode operation.

Jerng and Sodini made use of the DRFC architecture in their work, adding a $\Delta\Sigma$ modulator to the I and Q paths as shown in Figure 2.4 [9]. The $\Delta\Sigma$ modulators use 3-bit quantizers to boost

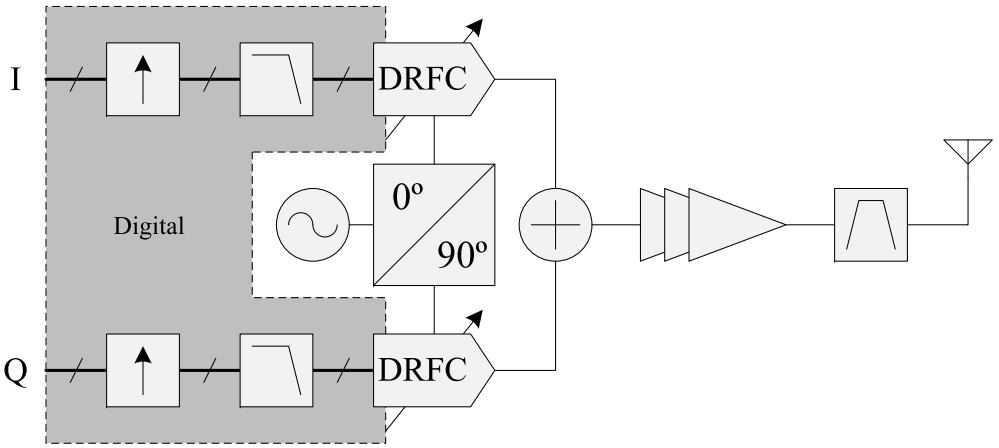


Figure 2.2: Direct digital RF modulator architecture [8].

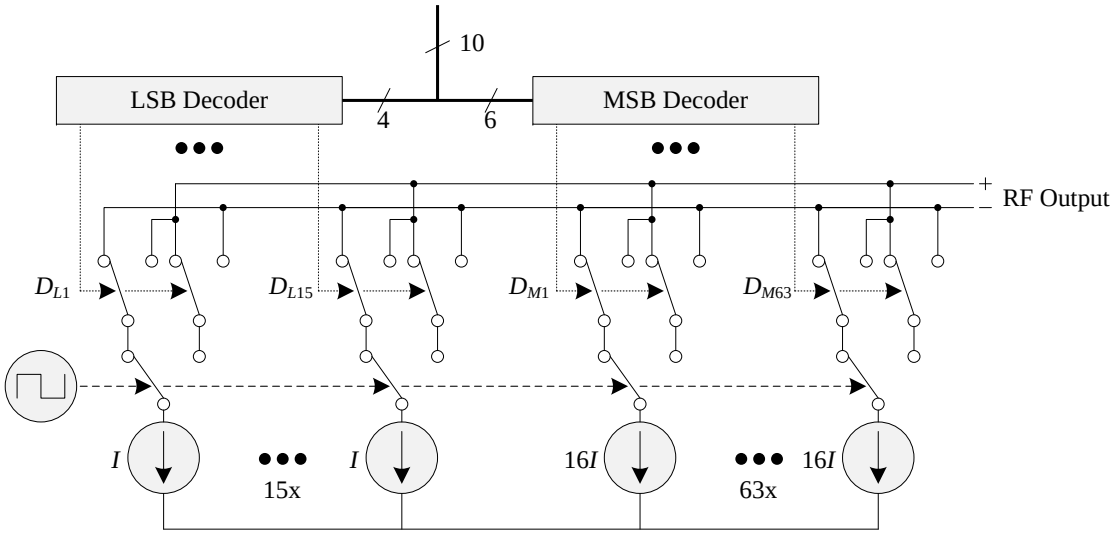


Figure 2.3: Digital-to-RF converter [8].

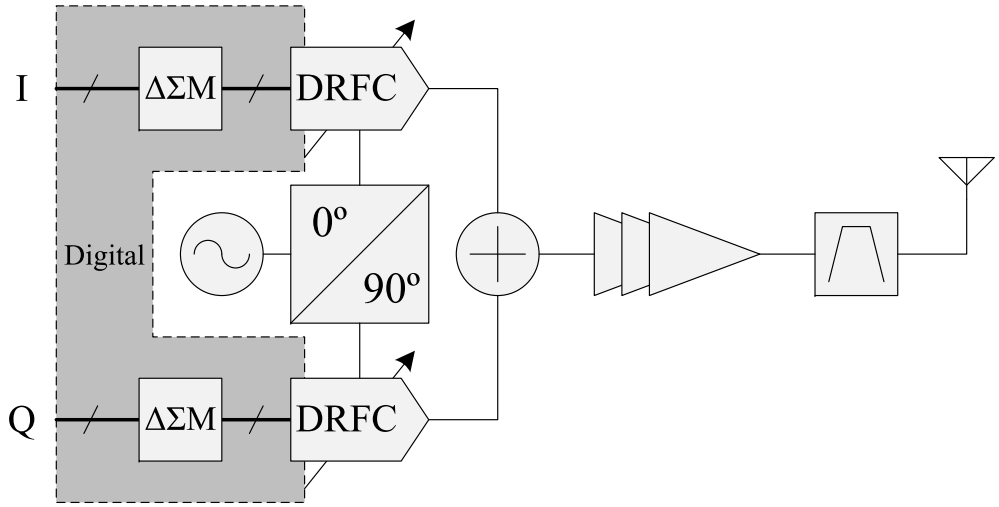


Figure 2.4: Delta-sigma RF modulator architecture using DRFC [9].

the SNR to an acceptable level. One could also use higher order 1-bit ΔΣ modulators to increase the SNR; however, this would result in more stringent reconstruction filter requirements due to the steeper close-in noise shaping. The ΔΣ modulator approach reduces the number of DRFC unit cells needed to achieve the required dynamic range. A quadrature IF stage is included in the digital domain to mitigate LO leakage and phase mismatch in the quadrature LO. This work also includes an integrated, high quality factor, self-tuned RF filter to attenuate the spurious products of the digital-to-RF conversion and the ΔΣ modulator quantization noise. The fabricated circuit achieved 1.2 gigabit-per-second (Gbps) using a 200 MHz bandwidth orthogonal frequency division multiplexing (OFDM) signal at 5.25 GHz, consuming 187 mW. The output RF power was -8 dBm, translating to a low system efficiency of about 0.1%. However, the power consumption of this modulator is likely to be insignificant compared to that of the PA, resulting in a low impact on the full transmitter efficiency.

In [10] Helaoui et al. proposed a similar quadrature ΔΣ modulator approach, but using digital multiplexers to upconvert and combine the I and Q components as shown in Figure 2.5. By multiplexing the 1-bit ΔΣ modulated components $I_{\Delta\Sigma}(t)$ and $Q_{\Delta\Sigma}(t)$ with their complements at a carrier frequency $f_c = Nf_s$ which is a multiple N of the ΔΣ modulator sampling frequency f_s. This amounts to a convolution with an RF pulse train at carrier f_c. The multiplexing of $Q_{\Delta\Sigma}$ is $\pi/2$ offset from that of $I_{\Delta\Sigma}$. The third multiplexer works at $2f_c$, combining the I and Q components into a single RF signal at f_c with odd-harmonic images. In addition to the flexibility gained through use of digital hardware, this transmitter demonstrated the ability to operate at a different f_c simply by changing the multiplexer frequency.

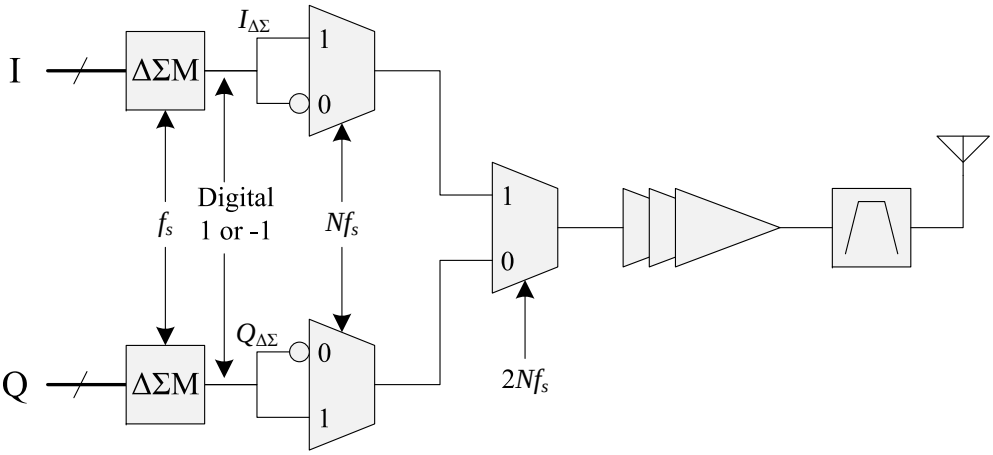


Figure 2.5: Delta-sigma RF modulator architecture using multiplexers [10].

2.2.2 Polar Transmitters

The complex envelope signal $g(t)$ (Equation 2.1) can be equivalently represented in polar form

$$g(t) = A(t)e^{j\theta(t)} \tag{2.5}$$

where

$$A(t) = \sqrt{I^2(t) + Q^2(t)} \tag{2.6}$$

$$\theta(t) = \tan^{-1}\left[\frac{Q(t)}{I(t)}\right]. \tag{2.7}$$

The transmitted signal then takes the form

$$s(t) = A(t)\cos[\omega_c t + \theta(t)]. \tag{2.8}$$

This form has been used successfully to implement polar transmitters, in which the dynamic range of the RF signal is eliminated from the main signal path and instead applied to separate power control and amplifier biasing circuitry. For reasons to be explained in Section 2.3 this allows efficiency enhancement of the PA stage without sacrificing signal linearity, a highly desirable feature for base station and mobile transmitters alike.

Kahn first demonstrated this technique in 1952 [11]. He proposed amplifying solely the phase-modulated (PM) component of the RF signal using a highly-efficient PA (e.g., class C) and varying the output power according to the signal envelope through the PA's DC bias. Because the

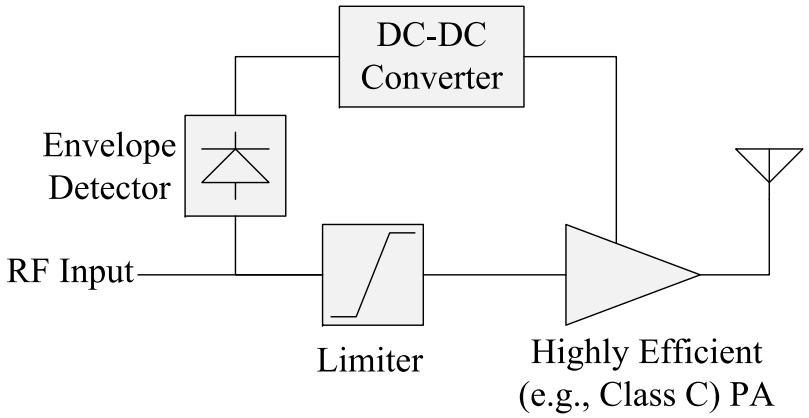


Figure 2.6: Simplified EER transmitter architecture.

signal at the input of the PA has a constant power envelope, this technique is sometimes called envelope elimination and restoration (EER) or simply the Kahn technique. Figure 2.6 shows the architecture of the EER system.

The main drawbacks of this structure are threefold. First, the amplitude and phase components of a complex modulated signal both generally have expanded bandwidth as compared to the rectangular (I and Q) components. This increases the frequency requirements of the PA as well as for the envelope amplifier, DC-DC converter and other components. Second, the bias-to-amplitude (DC-AM) characteristic of the PA may be nonlinear, necessitating the use of more than a simple envelope detector and amplifier to provide the proper DC bias for the desired output power. Moreover, the constant-envelope PM input signal can leak through the PA to the output even when the supposed envelope level is zero. Third, the envelope and phase paths through the transmitter are quite different, requiring careful consideration of the alignment at the output to keep the signal fidelity. This is further complicated by the possibly varying or even nonlinear bias-to-phase (DC-PM) characteristics of the PA. Nevertheless, the efficiency enhancement promised by EER and related techniques has encouraged efforts to mitigate these concerns.

One way to overcome the DC-AM nonlinearity is to digitize the envelope component of the signal, for example using a $\Delta\Sigma$ modulator [12,13]. This also augments the digital functionality of the transmitter making it more suitable for a fully reconfigurable system, and essentially replaces the envelope detection function in Figure 2.6. The architecture studied by Choi et al. in [13] is shown in Figure 2.7. This transmitter uses a three-level $\Delta\Sigma$ modulator for the envelope signal. The low number of discrete states makes it easy to correct for the PA distortions versus the drain-source bias voltage V_{DS} while increasing the SNR as compared to a two-level $\Delta\Sigma$ modulator. The system achieved 48% overall efficiency at a centre frequency of 40 MHz.

A $\Delta\Sigma$ modulator is just one way to digitize the envelope signal. In [14], Kavousian et al. demonstrated a polar transmitter in which the digitized envelope signal is used to activate a set of

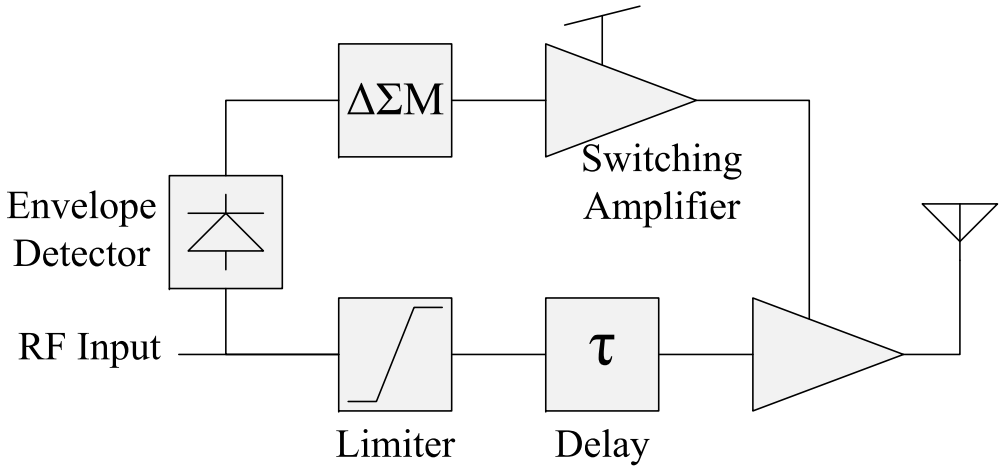


Figure 2.7: EER transmitter with ΔΣ digitized envelope signal [12, 13].

unit PAs which amplify the PM signal (Figure 2.8). In order to satisfy the linearity requirements for the IEEE 802.11g standard, a 6-bit envelope encoder is chosen and 64 unit PAs are included on the chip.

A notable highly digital platform based on the polar transmitter architecture has been the subject of many papers in the last decade: the Digital RF Processor (DRP[1]) by Texas Instruments [15–20]. Figure 2.9 illustrates the basic functionality of the transmitter portion of the chip. The DSP and predistortion functions are included on-chip in the digital domain. Notably, the circuit includes an all-digital phase-locked loop (ADPLL) and frequency synthesizer [21], functions traditionally implemented in analog circuits. The primary motivation in this case for such a digital architecture is compatibility with advanced digital complementary metal-oxide-semiconductor (CMOS) ICs. The limited voltage headroom of deep-submicron CMOS processes limits their suitability for RF circuits. The DRP cleverly exploits the superior time resolution of digital CMOS to mitigate this. However, although the DRP has been demonstrated as a highly reconfigurable platform, the reconfigurability is used primarily as a means to improve manufacturing yield and adaptability to environmental variation [20] rather than as a multi-mode/ multi-standard platform.

2.3 Switching-Mode Power Amplifiers

In future SDR systems one of the most challenging design problems will be the implementation of a highly reconfigurable PA which is both highly efficient and highly linear. The PA is the

[1]DRP is a trademark of Texas Instruments Inc.

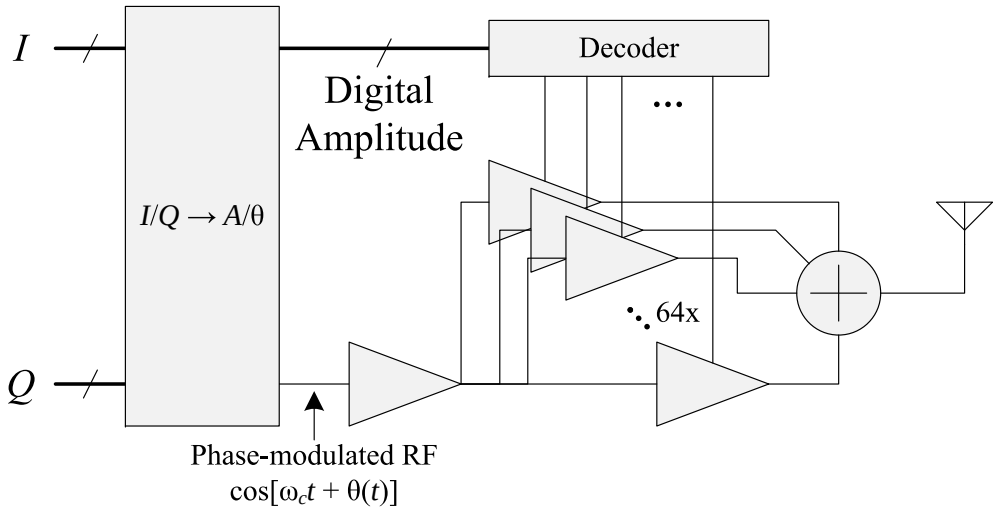


Figure 2.8: Polar transmitter using equally-weighted, digitally-controlled unit amplifiers [14].

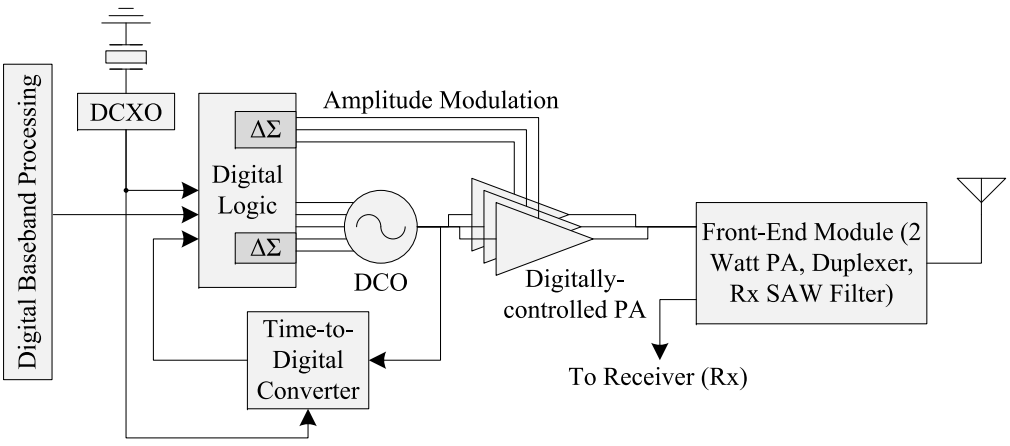


Figure 2.9: Simplified illustration of the Digital RF Processor platform [17].

component which consumes the most power in any RF transmitter, a necessity in order to transmit enough power to overcome the path loss and ensure the signal is received with adequate SNR. In mobile applications the PA should transmit the power efficiently to maximize battery life and minimize the heating, also reducing the chance of reliability issues related to overheating. In base stations and infrastructure low efficiency causes power to be wasted as heat in the PA, with the side effect of additional cooling requirements which use even more electricity. For a cellular infrastructure operator the additional cost of this wasted electrical power, multiplied by hundreds or thousands of base stations, is extremely high.

The continually accelerating demand for high mobile data rates and resulting scarcity of RF spectral resource has led to a situation where maximizing the spectral efficiency in terms of bits per second per Hz (bps/Hz) is the defining characteristic of emerging wireless communications standards. Such signals exhibit a high PAPR, meaning a large portion of the information is encoded in the signal amplitude in order to keep the channel bandwidth narrow. The PA must amplify the signal linearly in order to preserve this information, a requirement which is in opposition to the efficiency.

In a highly linear class A PA, the transistor acts as a voltage-controlled current source with a constant transconductance. In order to maintain highly linear operation, the transistor must be biased with a relatively high quiescent current and conducts current over the entire input cycle (i.e., its conduction angle is 2π). This class of PA can reach a maximum theoretical drain (or collector) efficiency η_D of only 50%. The drain efficiency is defined as the ratio of the output RF power to the DC power supplied:

$$\eta_D = \frac{P_{RF}}{P_{DC}}. \tag{2.9}$$

The maximum η_D occurs for maximum P_{RF}. Since the primary motivator for using a linear PA is the high PAPR of the signal, the *average* η_D is much lower. Nonidealities such as finite transistor small-signal output resistance r_o, output impedance matching network insertion loss and other factors further degrade the efficiency. The class A PA is therefore rarely used except in applications where linearity is the sole objective, such as in instrumentation and measurement.

Class AB, B and C have a reduced conduction angle as shown in Figure 2.10 [22]. The conduction angle defines for what portion of the input signal cycle the transistor is conducting current. Reduced conduction angle results in less overlap of the drain current and voltage waveforms, which represents power dissipated as heat inside the transistor. For class B, the conduction angle is π. Class AB signifies any conduction angle between π and 2π, and class C signifies a conduction angle of less than π. These PAs have reduced linearity compared to class A, but often a small tradeoff in linearity is acceptable for a relatively large gain in efficiency. This accounts for the relative popularity of class AB PAs in commercial applications.

These classes of PA all treat the transistor as a linear current source when the input is above the threshold voltage. An alternative is to treat the transistor as a switch capable of two states: on and off. This behaviour can be approximated by driving the transistor input with a large

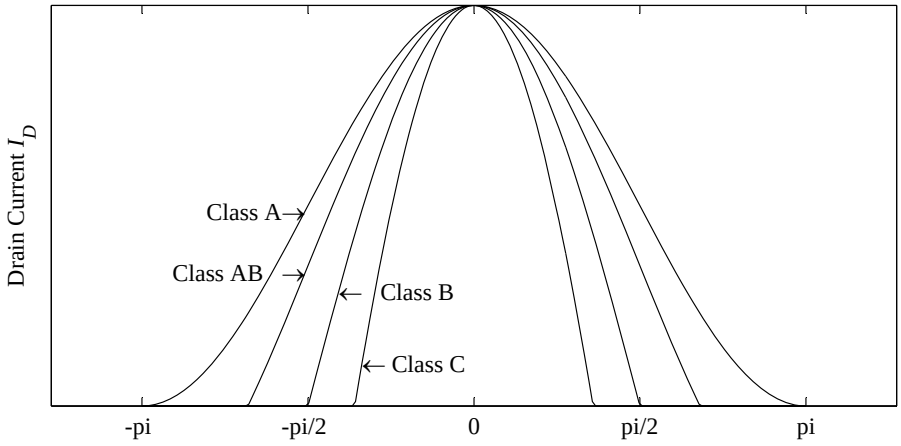


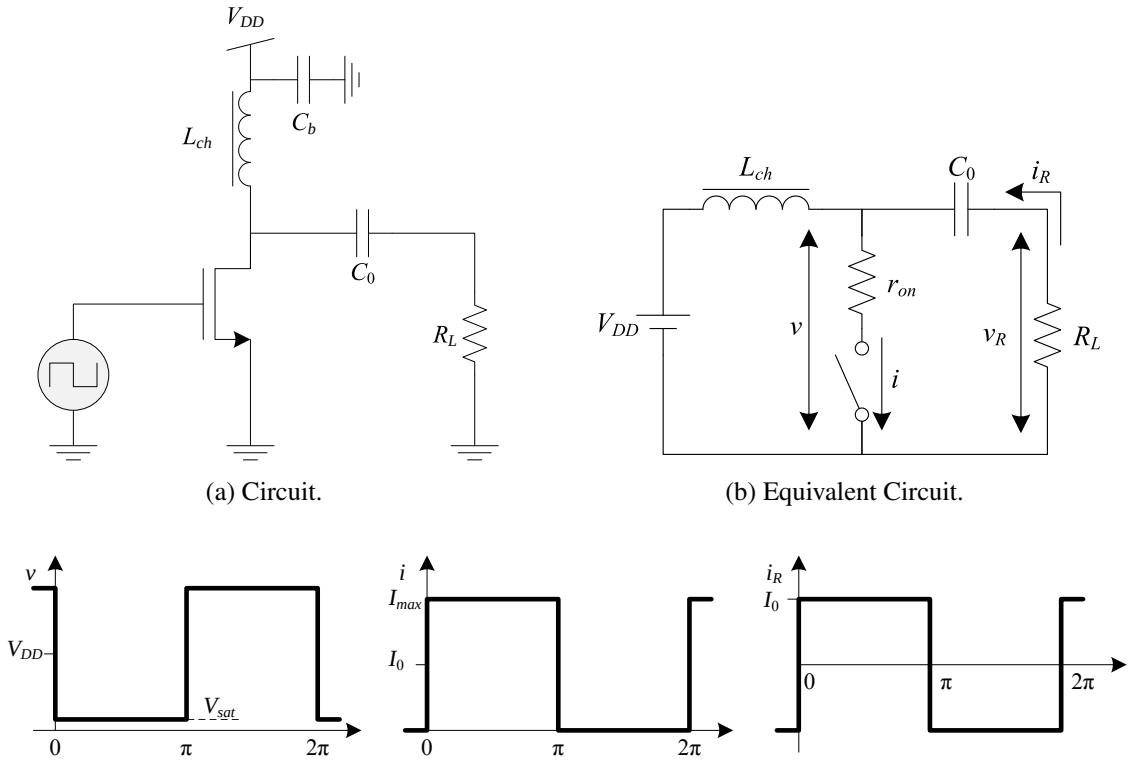
Figure 2.10: Illustration of conduction angle [22].

amplitude input signal or (more appropriately given the two possible switch states) a binary-level input. Such PAs are called switching-mode PAs (SMPAs), and can theoretically deliver 100% efficiency. Knowing the behaviour of an ideal switch, the reason for 100% efficiency is intuitive: when the switch is open, no current flows so no power is dissipated; and when the switch is closed, there is no voltage across the device so again no power is dissipated. In reality, 100% efficiency is not possible because the switch is not ideal. Two such nonidealities are the nonzero on resistance r_{on} and the finite leakage current in the off state. Despite this, very high efficiency ($> 60\%$) is regularly reported for continuous-wave input; for example, [23–26].

The principal limitation of SMPAs is their nonlinearity. Since the switch only has two states, there is no way to reduce or "back off" the input power without coming out of switching operation. Indeed, some high-efficiency PA designs in the literature which have been demonstrated under non-unity PAPR use SMPA techniques and principles for the PA design, and linearize the PA using other techniques; for example, the SMPA can be used in a polar transmitter architecture [13, 27]. Another approach is to amplify a digitized (e.g., bandpass $\Delta\Sigma$ modulated) version of the RF signal [28, 29] or employ the outphasing technique, also called linear amplification with nonlinear components (LINC) [30].

The switching behaviour of the transistor in an SMPA is a feature shared with digital circuits, making them a natural candidate for SDR/CR transmitters. Voltage- and current-mode class D, class F and inverse class F have all been demonstrated to provide very high efficiency operation. Class E is another popular SMPA configuration but will not be considered further in this thesis due to its limited frequency of operation and efficiency degradation under varying duty cycle [31].

Figure 2.11(a) shows a basic, single-ended SMPA with resistive loading, taken from [32]. R_L represents the resistive load, C_0 the output DC blocking capacitor, and L_{ch} the RF choke



(a) Circuit.

(b) Equivalent Circuit.

(c) Ideal Waveforms.

Figure 2.11: Single-ended SMPA with resistive load [32].

inductor. The transistor is driven as a switch by a square wave input centered about V_{GG}, the DC gate bias voltage which in the case of an SMPA is usually set to the threshold voltage. This causes the drain voltage v_{DS} to switch between the supply voltage V_{DD} and ground (or V_{SS}), and the current to switch between the peak I_{max} and 0 (Figure 2.11(c)). In the equivalent circuit of Figure 2.11(b), the transistor is represented by a small r_{on} in series with an ideal switch. Since the output voltage and current are not sinusoidal, harmonic power components are present in the spectrum of the signal delivered to the load. The power at the fundamental frequency is

$$P_{RF} = \frac{1}{2} i^2 R_L = \frac{8}{\pi^2} \frac{R_L}{(R_L + r_{on})^2} \frac{V_{DD}^2}{\left(1 + \frac{r_{on}}{R_L + r_{on}}\right)^2}. \tag{2.10}$$

which is *not* equal to the total DC power supplied to the circuit $V_{DD} I_0$. This is because additional power is delivered to the load at the harmonics.

2.3.1 Class D Power Amplifiers

Placing the previous SMPA in push-pull configuration and adding a fundamental-frequency series resonator at the output, the voltage-mode class D (VMCD) PA is formed as shown in Figure 2.12(a) and its equivalent circuit is shown in Figure 2.12(b) [32]. This structure is sometimes referred to as voltage-switching class D since the complementary switching of the top and bottom transistors have the effect of switching the voltage of the output node ① between V_{DD} and ground. The supply voltage is doubled due to the two transistors being in series. The series resonator passes only the power at the fundamental frequency, reflecting the rest and resulting in the waveforms being shaped as seen in Figure 2.12(c). The voltage is a square wave and the current is a half rectified sinusoid.

Assuming no losses except in the switch resistance r_{on} it can be shown [32] that the DC power supplied to the circuit is

$$P_{DC} = V_{DD} I_0 = \frac{2}{\pi^2} \frac{V_{DD}^2}{R_L} \frac{1}{1 + \frac{r_{on}}{R_L}} \tag{2.11}$$

and the fundamental-frequency power is

$$P_{RF} = \frac{2}{\pi^2} \frac{V_{DD}^2}{R_L} \frac{1}{\left(1 + \frac{r_{on}}{R_L}\right)^2}. \tag{2.12}$$

The drain efficiency is then

$$\eta_D = \frac{P_{RF}}{P_{DC}} = \frac{1}{1 + \frac{r_{on}}{RL}}. \tag{2.13}$$

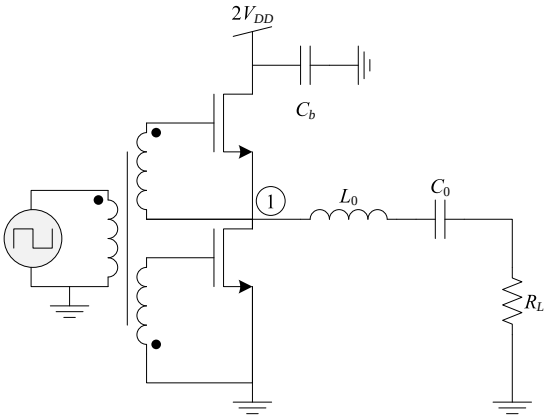
Clearly the VMCD can provide 100% efficiency assuming $r_{on} = 0$ and no other losses in the circuit. This high efficiency has made it a popular choice in audio applications.

In practice, not only are there finite losses throughout the circuit but the VMCD has a fundamental limitation that is a significant problem at high frequencies. Figure 2.13 shows a VMCD amplifier including the parasitic drain-source capacitances C_{DS} of the transistors. When the top transistor is on, current flows to node ① charging the C_{DS} of the bottom transistor and causing the voltage waveform to lose its ideal square shape [31]. The energy stored on this charge cycle is

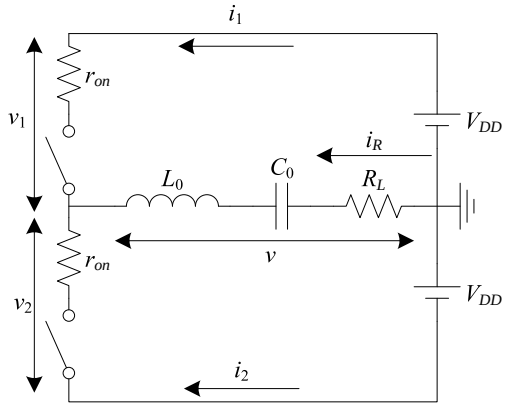
$$E = \frac{1}{2} C_{DS} V_{DD}^2. \tag{2.14}$$

On the second half-cycle the bottom transistor is on and the C_{DS} is discharged. This happens on every switching cycle corresponding to a lost power of

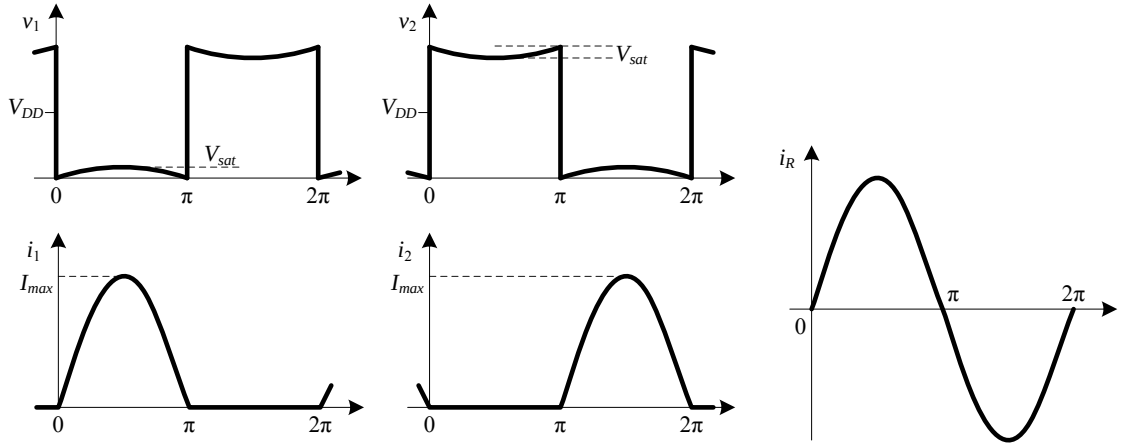
$$P_{lost} = \frac{1}{2} C_{DS} V_{DD}^2 f_c. \tag{2.15}$$



(a) Circuit.



(b) Equivalent Circuit.



(c) Ideal Waveforms.

Figure 2.12: Voltage-mode class D PA [32].

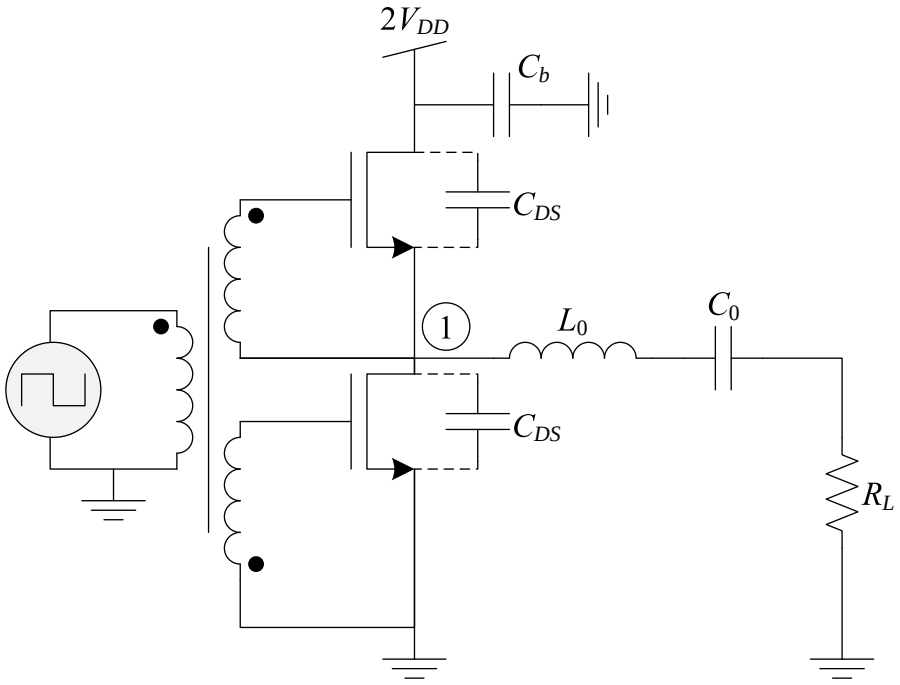


Figure 2.13: VMCD PA with parasitic capacitance [33].

Beginning at hundreds of megahertz this mechanism starts to dominate the losses of the VMCD and for this reason the VMCD is not a popular choice for RF applications [31].

A more appropriate structure for RF applications is the current-mode class D (CMCD), sometimes called current-switching class D or inverse class D. The basic structure of the CMCD is shown in Figure 2.14(a) and the waveforms at each transistor drain are shown in Figure 2.14(b) [32]. As suggested by the name, the current (rather than the voltage) is switched between I_{max} and 0. The voltage and current waveforms are interchanged with respect to the VMCD configuration. Again assuming no losses other than r_{on}, the fundamental frequency output power is

$$P_{RF} = \frac{\pi^2}{2}\frac{V_{DD}^2}{R_L}\frac{1}{\left(1+\frac{\pi^2}{2}\frac{r_{on}}{R_L}\right)^2} \tag{2.16}$$

and the DC power is

$$P_{DC} = \frac{\pi^2}{2}\frac{V_{DD}^2}{R_L}\frac{1}{1+\frac{\pi^2}{2}\frac{r_{on}}{R_L}}. \tag{2.17}$$

The drain efficiency is thus

$$\eta_D = \frac{1}{1+\frac{\pi^2}{2}\frac{r_{on}}{R_L}}. \tag{2.18}$$

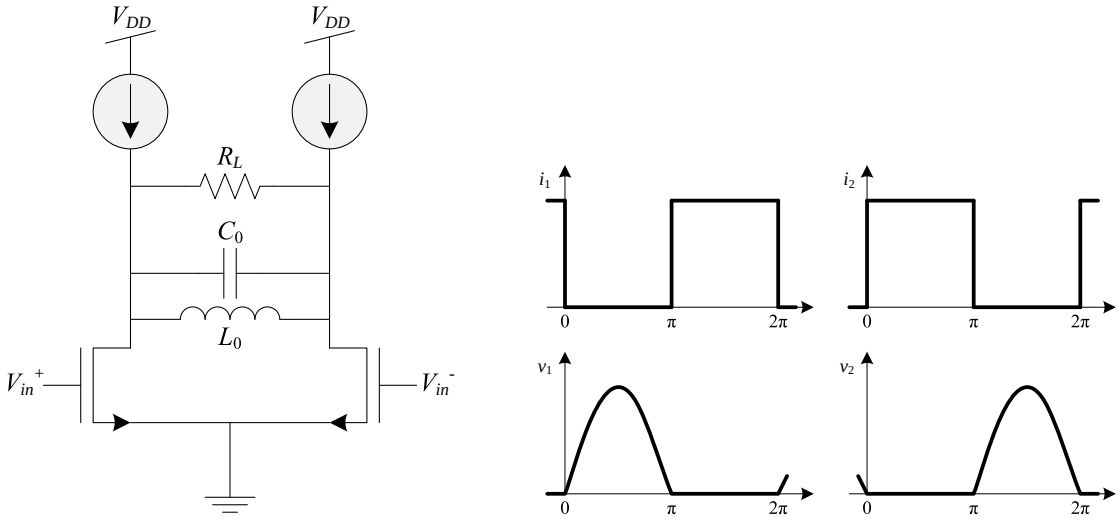
Note also that the parasitic C_{DS} of each transistor can now be absorbed into the output resonant network, eliminating its effect on the performance.

Several successful RF implementations of CMCD PAs have appeared in the literature [34–40]. In one particular example demonstrated by Long [36] a rat-race hybrid is used to transform a single-ended input into a differential input to each active device, and a second rat-race hybrid performs the differential to single-ended conversion at the output. Laterally-diffused metal-oxide-semiconductor (LDMOS) transistors were used as the switching devices. This PA output 13 W with a drain efficiency of 60% and gain of 14 dB.

A new approach at RF is to replace the resonant lumped-element output network with a transmission line network which provides the necessary impedances at a finite number of harmonics, resulting in a good approximation of CMCD behaviour and high efficiency. For example, Aflaki et al. demonstrated a CMCD at 2.35 GHz providing 65% power-added efficiency (PAE) while delivering 39.2 dBm [40]. The PAE is defined as

$$\eta_{PAE} = \frac{P_{RF} - P_{in}}{P_{DC}} \tag{2.19}$$

where P_{in} is the RF input power.



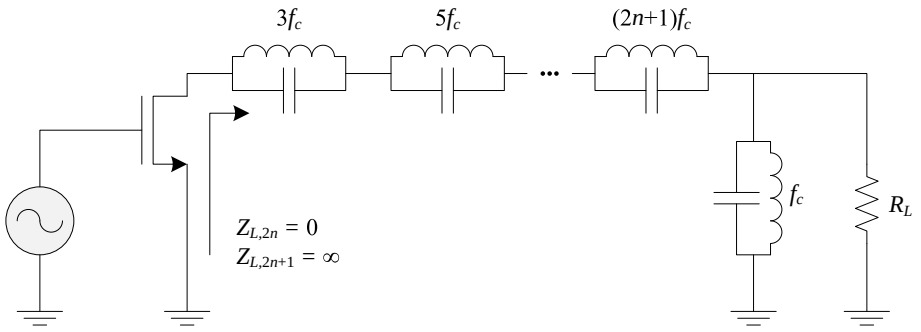
(a) Circuit. (b) Ideal Waveforms.

Figure 2.14: Current-mode class D PA [32].

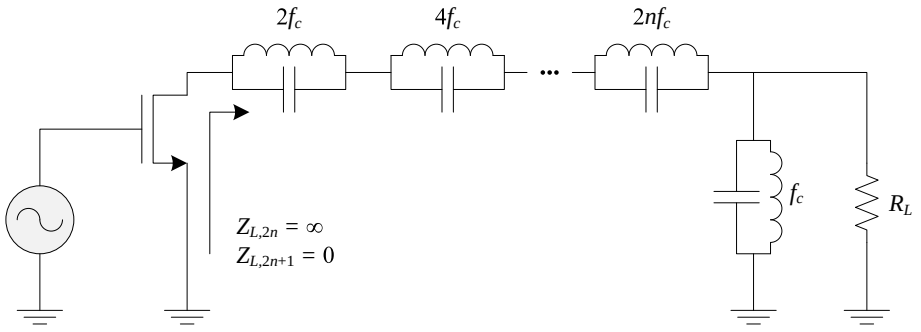
This multiharmonic matching strategy is similar to having two inverse class F PAs operating in push-pull. Whether this structure truly constitutes a CMCD amplifier is not agreed upon in the literature. Long proposes that a CMCD "uses a pair of switches operating in parallel, out of phase across a resonant tank circuit" [36]. The main points of contention are whether the harmonic matching networks of inverse class F are equivalent to the resonant tank of CMCD, and whether a high-power continuous-wave stimulus is an adequate approximation for switching operation. The latter point has implications on the design of the input matching network, which will be explored further in the next chapter.

2.3.2 Class F and Inverse Class F PAs

Closely related to the VMCD and CMCD amplifiers are the class F and inverse class F (class F^{-1}). The class F shares ideal drain waveform behaviour with the VMCD, as the class F^{-1} does with the CMCD. The class F PA structure is shown in Figure 2.15(a). It consists of a single transistor driven by a high-power input and a multiharmonic output impedance matching network. The high-power input drives the transistor into the nonlinear region, generating harmonic content at the output. The matching network transforms the load impedance into the required harmonic impedances to shape the voltage and current waveforms at the transistor drain into the same non-overlapping shapes as the VMCD (Figure 2.12(c)). Fourier analysis [32] shows the required



(a) Class F.



(b) Inverse Class F.

Figure 2.15: Ideal class F/F^{-1} power amplifier.

harmonic output impedances are

$$Z_{L,2n} = 0 \text{ (short circuit) for even harmonics, and}$$
$$Z_{L,2n+1} = \infty \text{ (open circuit) for odd harmonics.}$$

Usually in the design of class F (and F^{-1}) PAs, no assumption is made about the shape of the input signal being a switching signal. It must simply be large enough to generate harmonic content at the transistor output.

The dual of the class F PA is the class F^{-1} (Figure 2.15(b)). The current and voltage waveforms are interchanged from the class F case. Similarly, the required harmonic terminations are interchanged:

$$Z_{L,2n} = \infty \text{ (open circuit) for even harmonics, and}$$
$$Z_{L,2n+1} = 0 \text{ (short circuit) for odd harmonics.}$$

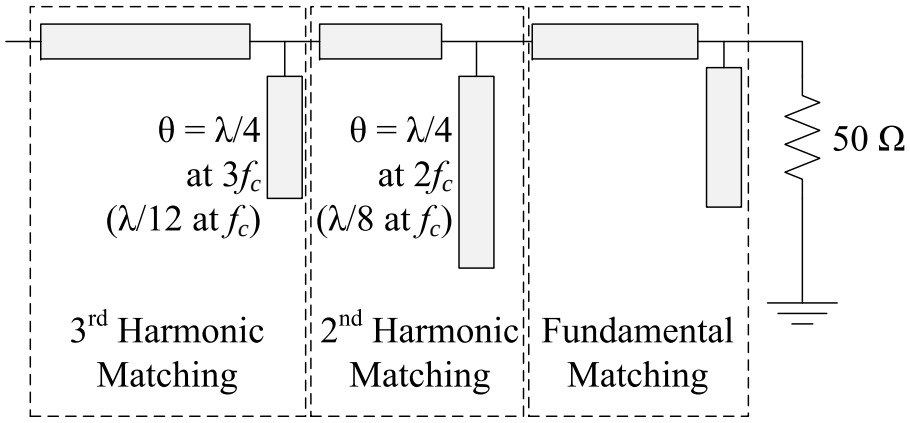


Figure 2.16: Three-harmonic output matching network structure for class F^{-1} [23].

Woo et al. showed that a class F^{-1} amplifier can achieve higher efficiency than a class F for a given P_{RF}, a difference that increases with r_{on} [41]. The class F^{-1} PA has thus become a popular choice when high efficiency is the primary design goal.

It is theoretically possible to achieve ideal class F or F^{-1} operation, including termination of an infinite number of harmonics, using a quarter-wave transformer [32]. This results in an inherently narrowband PA. A more practical approach is to terminate the first few harmonics, resulting in approximated waveforms at the device drain. More harmonics properly terminated results in better approximation of the ideal waveforms; however, the additional matching network complexity causes additional insertion loss and degrades the efficiency.

In practice, high efficiency can be achieved in class F^{-1} operation by terminating as few as three harmonics. For example, in [23] Helaoui and Ghannouchi demonstrated a 1 GHz class F^{-1} PA with three harmonic terminations at the output. The technique used for the matching network is illustrated in Figure 2.16. The harmonic matching conditions are achieved with quarter-wavelength stubs at the second and third harmonics, placed the proper distance away from the transistor to provide the correct open or short condition. The authors demonstrated a PAE of over 80% at 1.01 GHz. This matching technique was also used in [42] to achieve 71% PAE. This matching strategy is described more in-depth in Chapter 3, as applied to a class F^{-1} PA in push-pull.

Because of their identical drain waveforms the VMCD amplifier is sometimes considered as the push-pull configuration of the class F. Similarly, the CMCD shares drain waveforms with the class F^{-1}. However, as can be observed by comparing the ideal PA topologies in Figures 2.12, 2.14 and 2.15, the mechanism which creates these waveforms is subtly different. In the case of the class D PAs, the switching (square wave) behaviour of the waveforms is due to the switching of the transistor. But in the case of the class F/F^{-1} PAs, the waveforms are explicitly shaped by the chosen harmonic terminations formed by the output matching network.

These considerations combined with the energy dissipation problem of VMCD described by Equation 2.15 make the CMCD the most appropriate choice for direct amplification of binary-level signals. The design, implementation and testing of a class F^{-1} PA in push-pull, a topology very similar to the CMCD, is presented in Chapter 3.

2.4 Time Domain Modulation Techniques

Adding full reconfigurability to the already challenging RF PA requirements (i.e., linearity and efficiency) is a challenging proposition. In addition, the most advanced IC fabrication processes and technologies are optimized for high-speed digital applications. Deep submicron CMOS processes have limited power handling and low supply voltage, both of which are enormous advantages for digital circuits. However, these same features are also the major barriers that have prevented RF applications from reaping the benefits of process scaling which digital circuits have enjoyed for years. Interest in SDR and reconfigurable radio is nevertheless growing so there needs to be a means to reconcile the conflicting requirements of RF and digital circuits.

SMPAs are likely to be an important part of the solution. The active device in an SMPA is treated as a switch, providing a degree of inherent compatibility with digital circuits. Also, most classes of SMPA can theoretically provide 100% efficiency. The main limitation of SMPAs is their linearity. They are designed to amplify a constant-envelope input signal, but modern wireless communications standards provide high spectral efficiency by encoding information in the signal amplitude. Therefore, the amplitude information must be provided to the PA in a different way.

There are several ways of accomplishing this which may collectively be summarized as encoding the information into the timing of the level transitions of the switching signal. The time resolution of deep submicron CMOS is vastly superior to the voltage resolution, so the high-to-low and low-to-high transitions in a binary-level digital signal can provide the necessary dynamic range for high PAPR modulated signals. Given the functioning of SMPAs previously discussed, the concept of using a constant-envelope signal to encode varying amplitude (and phase) information is very useful. This enables the PA to become a "more digital" part of the transmitter system.

In order to simplify the RF amplification process, one important requirement is that no special decoding schemes are required to recover the RF signal from the digital signal; a bandpass or lowpass reconstruction filter must suffice.

This section outlines the theory behind two particular time-domain modulation techniques: pulse width modulation, and $\Delta\Sigma$ modulation. Several examples of successful PA implementations incorporating each technique are also presented.

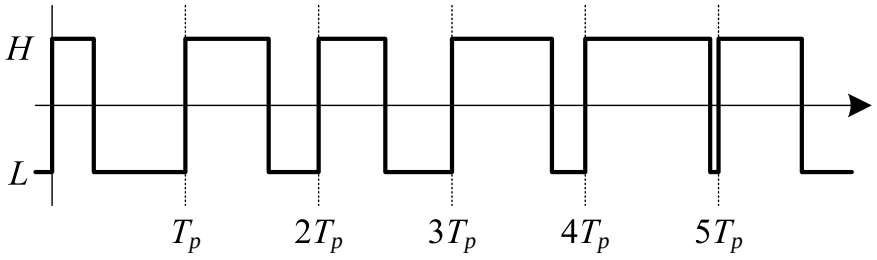


Figure 2.17: Pulse width modulation.

2.4.1 Pulse Width Modulation

One of the simplest forms of constant envelope modulation is pulse width modulation (PWM). In this scheme the modulated signal takes the form of a digital pulse train with each pulse varying in width according to the sampled input amplitude:

$$p_n(t) = \begin{cases} H, & nT_p < t \leq \left(n + \frac{A_p + a_n}{2A_p}\right) T_p \\ L, & \text{otherwise} \end{cases} \tag{2.20}$$

where

$$\begin{aligned} L &= \text{ digital “0”,} \\ H &= \text{ digital “1”,} \\ T_p &= \text{ the pulse period,} \\ a_n &= \text{ the input signal sequence, and} \\ A_p &= \text{ a signal limit such that } -A_p \leq a_n \leq A_p. \end{aligned}$$

This is illustrated in Figure 2.17. Summing the entire pulse sequence gives the overall signal:

$$p(t) = \sum_n p_n(t). \tag{2.21}$$

One of the main benefits of PWM is its simple method of generation. The slowly varying input signal may simply be compared to a triangular or sawtooth wave. Depending on the shape of the triangular wave, three types of PWM can be generated:

- The rising edge of each pulse is synchronous and the position of the falling edge is modulated (as in Figure 2.17).
- The falling edge of each pulse is synchronous and the position of the rising edge is modulated.

- The pulse centres are synchronous and both edge positions are modulated around the pulse centre.

A PWM signal is essentially a clock with varying duty cycle. By placing the pulse frequency at the carrier frequency, a varying duty cycle corresponds to a varying envelope for the RF signal, plus varying degrees of harmonic content which can be filtered. Fourier expansion of the PWM signal [43] shows the RF envelope and pulse width are related by

$$A_n = \frac{2(H-L)}{\pi} \sin\left(\pi \frac{T_{p,n}}{T_p}\right) \tag{2.22}$$

where A_n is the RF amplitude and $T_{p,n}$ is the pulse duration. Thus the maximum fundamental (RF) envelope occurs when the duty cycle $T_{p,n}/T_p = 50\%$. Duty cycles greater than 50% generate the same RF envelope as duty cycles less than 50% by the same amount; that is, a 60% duty cycle has the same fundamental frequency component as a 40% duty cycle.

Several papers have described successfully implemented RF PWM systems for PA applications. For example, Nielsen and Larsen presented an RF PWM for a 100 MHz carrier frequency [43] summarized in Figure 2.18. The mapping described by Equation 2.22 is performed in DSP and the comparison in this case is done between the post-mapped amplitude signal $A_M(t)$ and a phase modulated sinusoid, thereby encoding phase information into the timing of each pulse. To compensate for performance variations due to drift and other causes, which are sources of nonlinearity in the system, feedback is introduced in the envelope path. This is a lowpass rather than bandpass feedback to avoid reducing the system bandwidth. The linearity was an acceptable 17 dB below the emission mask for a Universal Mobile Telecommunications System (UMTS) signal, and the error vector magnitude (EVM) was below 1%. The meaning of EVM is explained in Section 2.4.2.

More recently, Yang et al. presented the gate-bias-modulated PWM-based polar transmitter system [44] shown in Figure 2.19. The baseband signal is represented in polar form with the normalized I and Q components generating the phase-modulated RF portion. The envelope component is modulated with PWM and used to pulse the input to two class E PAs. Adequate linearity was achieved without any predistortion and the transmitter showed over 49% peak drain efficiency and PAE over 40% under code division multiple access (CDMA) Interim Standard 95 (IS-95) modulated input.

Also recently, Chung et al. applied the concepts of LINC and PWM to two class E PAs [45], as shown in Figure 2.20. The LINC or outphasing technique attempts to enhance the transmitter efficiency by using two PAs to amplify two constant envelope signals which when recombined produce the desired amplitude and phase through vector addition. Traditionally this technique suffers from poor efficiency at large power backoff (i.e., large outphasing angle), which can be mitigated by using *asymmetric multilevel* outphasing (AMO) [46], where the power level for each branch is chosen from a discrete set of values and the bias level of the PA switched accordingly

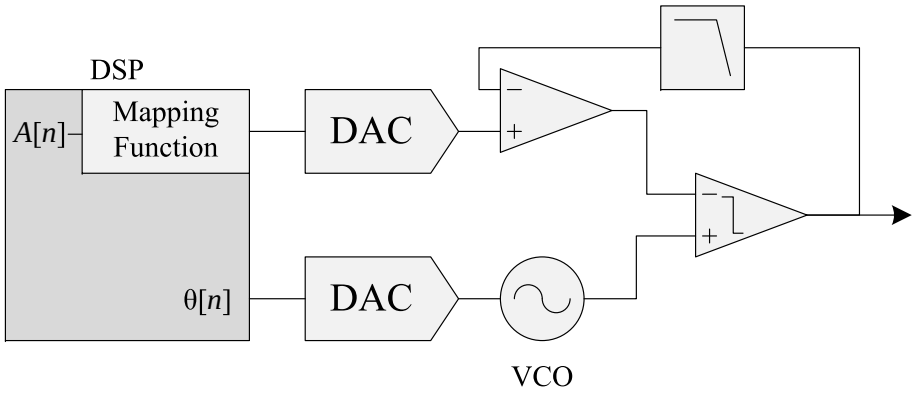


Figure 2.18: PWM system presented by Nielsen and Larsen [43].

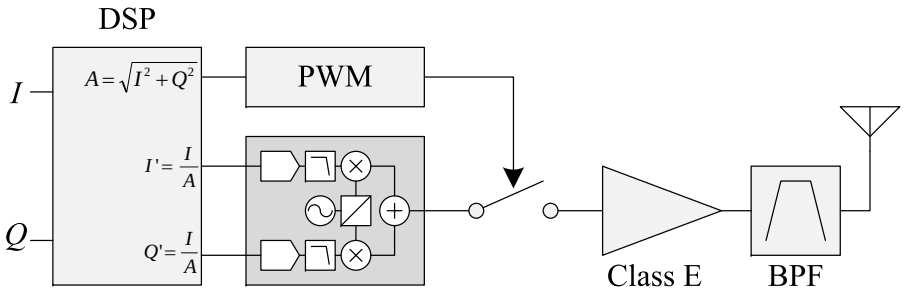


Figure 2.19: PWM-based polar transmitter presented by Yang et al. [44].

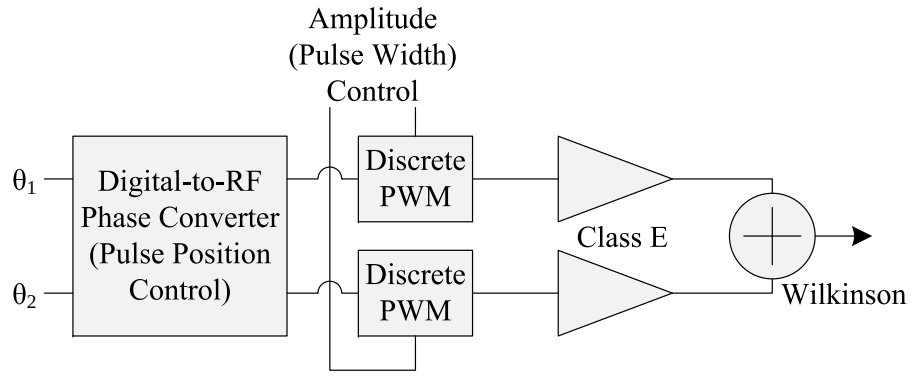


Figure 2.20: AMO transmitter with discrete PWM [45].

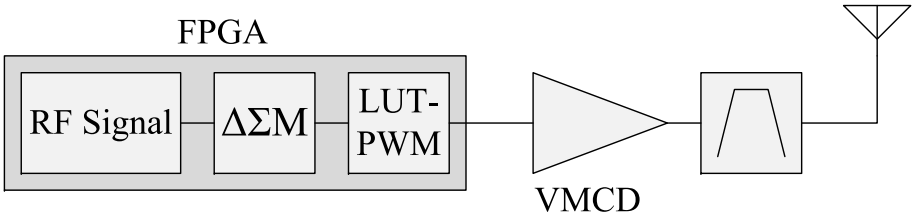


Figure 2.21: Multilevel ΔΣ modulator driving a LUT-based PWM and VMCD amplifier [47].

among the appropriate voltages. In [45], rather than switching the bias levels among discrete values, the power of each branch is adjusted using discrete PWM. This was shown to further enhance the efficiency compared to the original AMO tranmsitter and deliver more than twice the overall system efficiency of standard LINC (36.5% versus 17.1%). The presented results were at a centre frequency of 48 MHz.

As a final example of PWM in the context of SMPA, Podsiadlik et al. proposed using the output of a multilevel, bandpass ΔΣ modulator as an input to a lookup table- (LUT) based PWM [47]. The authors used a fourth-order ΔΣ modulator with 11 quantization levels and a 20 bit LUT to generate a two-level RF PWM signal at 741.4 MHz (a function of the chosen field programmable gate array [FPGA] testbed), which then drove a VMCD PA (Figure 2.21). They achieved a 10 dB improvement in dynamic range and 20 dB lower out-of-band noise floor compared to an equivalent upconverted 2-level ΔΣ modulator alone, in turn lowering the bandpass reconstruction filter requirements at the output. Additionally, the FPGA platform chosen for implementation is inherently reconfigurable.

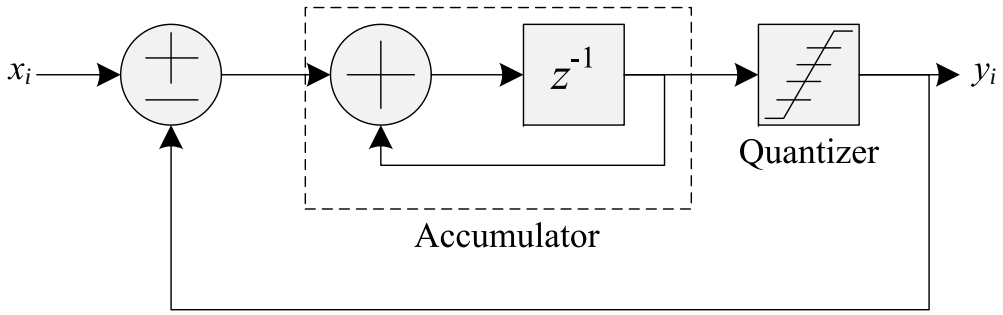


Figure 2.22: First-order ΔΣ modulator.

2.4.2 Delta-Sigma Modulation

When a sampled signal is quantized, the error between the quantized signal and the original signal is termed *quantization noise*. For a sufficient number and proper placement of the quantization levels according to the statistics of the input signal, the quantization noise present inside the signal band can be reduced to an acceptable level depending on the application. By using feedback in an attempt to cancel the quantization error, and oversampling the signal to a sufficient degree, the quantization noise power can be shaped away from the signal band of interest. This is the essence of ΔΣ modulation.

This behaviour can be explained by way of example. Figure 2.22 shows the topology of a first-order ΔΣ modulator. The input discrete-time signal is assumed to be low-pass and band-limited according to the oversampling ratio (OSR)

$$\text{OSR} = \frac{f_s}{2f_b} \tag{2.23}$$

where

$f_s =$ the sampling frequency in Hz, and
$f_b =$ the baseband bandwidth of the desired signal in Hz.

The quantized output value y_i is subtracted from the input value x_i and the result is accumulated. On the following clock, the value of the integrator is quantized and sent to the output.

The quantizer can be modeled as an addition of an error signal ε_i. This is reflected in Figure 2.23 [48]. The accumulator value w_i is equal to

$$w_i = w_{i-1} + x_{i-1} - y_{i-1} \tag{2.24}$$
$$= x_{i-1} - \varepsilon_{i-1}. \tag{2.25}$$

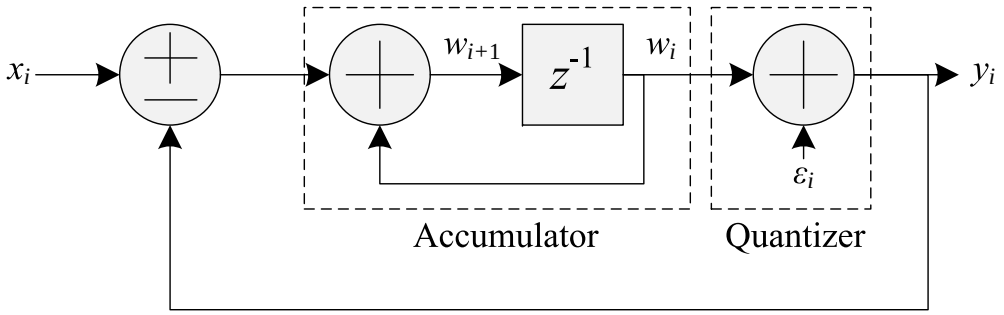


Figure 2.23: First-order ΔΣ modulator with the quantizer modeled as an addition of error.

This gives at the output

$$y_i = w_i + \varepsilon_i \tag{2.26}$$
$$= x_{i-1} + \varepsilon_i - \varepsilon_{i-1}. \tag{2.27}$$

The input signal experiences a delay to the output (x_{i-1}), with an added quantization noise component

$$n_i = \varepsilon_i - \varepsilon_{i-1} \tag{2.28}$$

which has a magnitude spectrum

$$N(f) = E(f)|1 - e^{-j2\pi f T_s}| \tag{2.29}$$
$$= 2\varepsilon_{rms}\sqrt{2T_s}\sin(\pi f T_s) \tag{2.30}$$

where T_s is the sampling period. This equation assumes an input signal which is sufficiently busy to apply the *white noise approximation* to ε_i. In this case the term $1 - e^{-j2\pi fT}$ is known as the *noise transfer function* (NTF) of the modulator. Whereas for the quantizer alone ε_i has a flat spectrum, the modulator overall has reduced quantization noise around the low frequencies where the desired signal resides as illustrated in Figure 2.24.

In general a ΔΣ modulator's behaviour in the z domain can be described by the following equation:

$$Y(z) = \mathrm{STF}(z)X(z) + \mathrm{NTF}(z)E(z) \tag{2.31}$$

where X, Y, and E represent the input, output and quantization error, respectively. $\mathrm{STF}(z)$ is the *signal transfer function*, which in the first-order modulator example described by Equation 2.27 is equal to $\mathrm{STF}(z) = z^{-1}$. That is, the full signal is passed from input to output with only a delay; however, it may be obscured by the quantization noise if it is not sufficiently band-limited.

By adding integrators, resonators, feedback and feedforward components, higher-order modulators can be realized. These give more degrees of freedom with which to adjust the NTF and

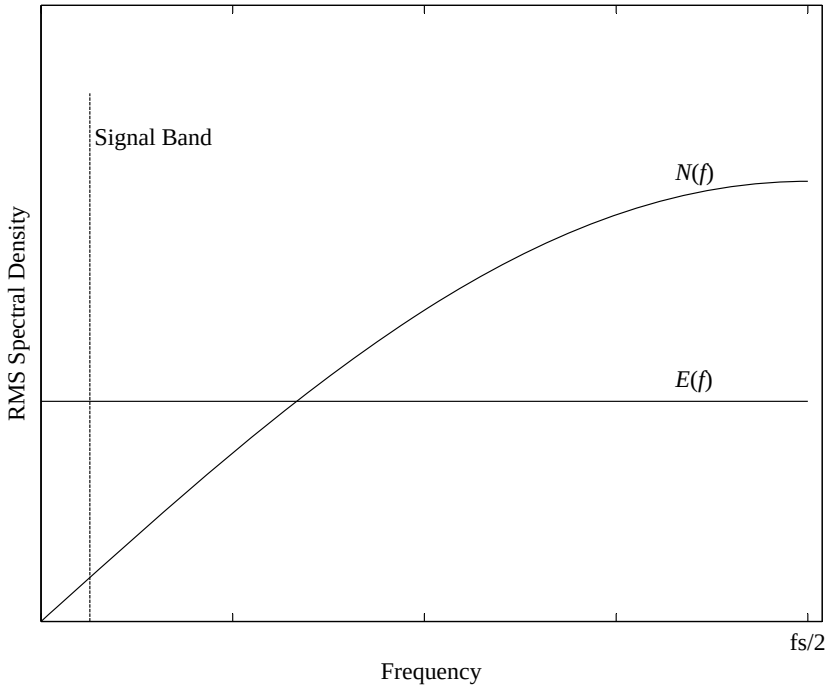
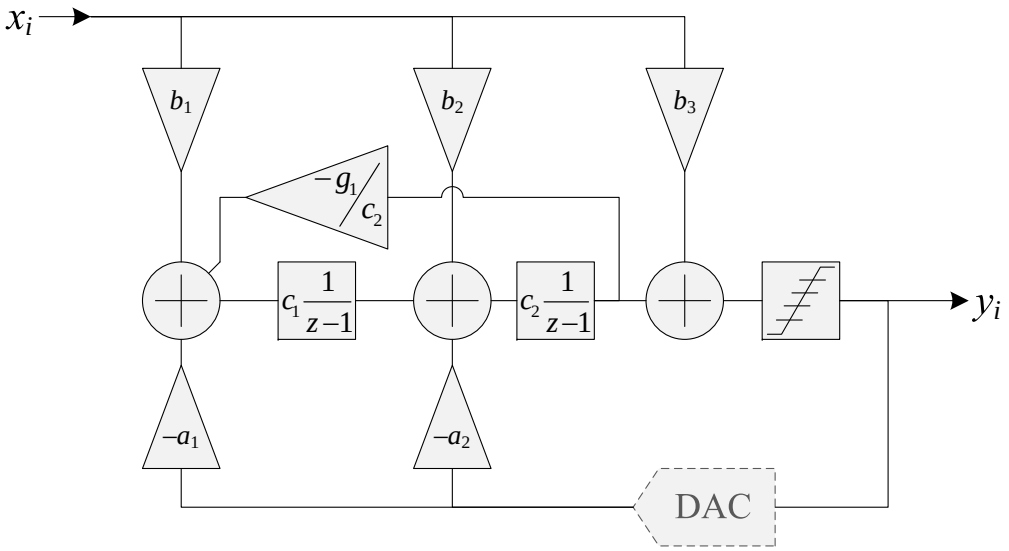


Figure 2.24: Noise spectrum shaping of first-order ΔΣ modulator [48].

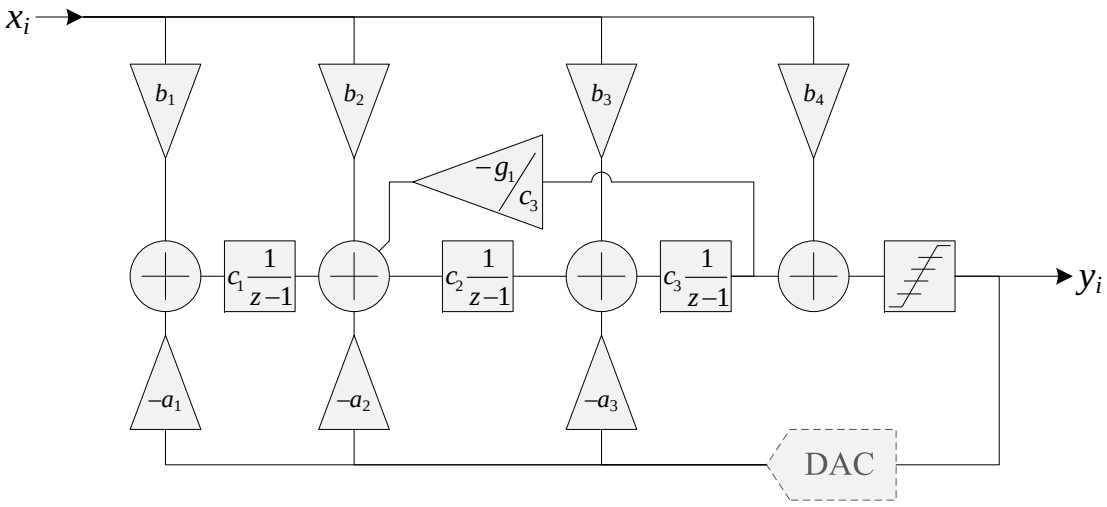
STF of the system. Several topologies have been collected by Schreier and used to implement a MATLAB toolbox which can be used to easily design ΔΣ modulators [49]. One such form is the cascade of integrators with feedback (CIFB), pictured in Figure 2.25.

The coefficients a_i, b_i, c_i and g_i can be adjusted to create the desired noise shaping behaviour. (The design of these coefficients is beyond the scope of this thesis.) The most important of these with respect to the noise shaping behaviour are the feedback terms a_i and g_i. They can especially be used to optmize the location of the zeros within the stopband of the NTF (i.e., the desired signal band) in order to minimize the in-band quantization noise and distortion, rather than placing all NTF zeros at DC or the centre of the signal band. Figure 2.26 illustrates this behaviour.

For ΔΣ modulation of baseband signals, the NTF should be a highpass function. The NTF can also be designed as a bandstop function for a signal centered at a frequency other than DC, creating a bandpass ΔΣ modulator. The previously mentioned standard topologies are all capable of implementing such an NTF (and corresponding bandpass STF), given the correct feedback and feedforward coefficients.

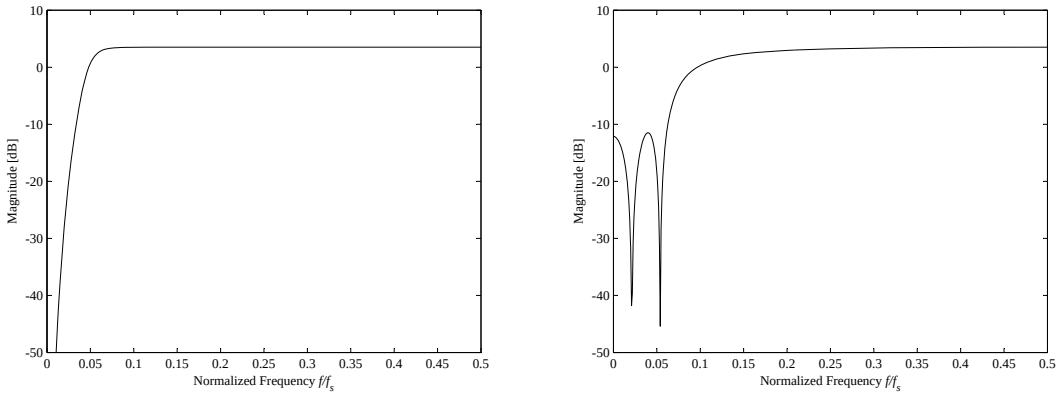


(a) Even order.



(b) Odd order.

Figure 2.25: CIFB form of ΔΣ modulator [49].



(a) Zeros at DC.

(b) Optimized zeros for OSR = 8.

Figure 2.26: Adjustment of zero locations in NTF to minimize in-band noise.

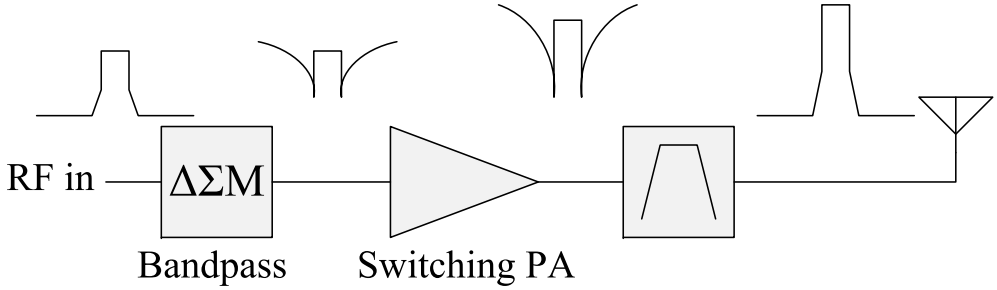


Figure 2.27: Class S amplifier system.

Class S Amplifier Systems

In a class S amplification system a $\Delta\Sigma$ modulator is used as a driver for a switching amplifier. This technique is quite popular for audio frequencies using a lowpass $\Delta\Sigma$ modulator. In the past decade, the increasing frequency capabilities of semiconductor processes and signal processing have led to increased interest in bandpass class S systems for RF application (Figure 2.27); for example, [28, 29, 50–52]. In one of the latest of these published results [29], Wentzel et al. used a 1.68 Gbps bandpass $\Delta\Sigma$ modulator to drive a gallium nitride (GaN) monolithic microwave IC (MMIC) containing a CMCD PA. The bit rate represented $4\times$ oversampling of a 420 MHz RF carrier tone. The authors used the modulator to achieve peak drain efficiency of 41% for the PA.

An RF class S system must also reconstruct the RF signal before transmission. Otherwise, the out of band quantization noise and sampling images would be broadcast, interfering with other channels and violating government regulations. A bandpass filter (BPF) performs this reconstruction. However, due to the proximity of the quantization noise to the signal band as

well as the magnitude of the noise power compared to the signal (recall Figure 2.26) the design specifications of such a filter are very strict in terms of relative bandwidth, rolloff and stopband attenuation. That is, the filter needs to have a very high quality factor Q. This is one of the principal limitations of RF class S systems today.

The PA itself (before the filter) in a class S system is a switching PA, inherently making it a high efficiency component of the system. In fact, the PA typically being most power-hungry component of the transmitter, the overall transmitter efficiency will be dominated by the PA efficiency. When driven by a $\Delta\Sigma$ modulator it amplifies not only the desired signal but also the shaped quantization noise of the modulator. It is this quantization noise which causes the PA to amplify efficiently. However, the quantization noise also represents a significant amount of power which is lost at the reconstruction filter. When referring to the power efficiency of a class S system, it is important to consider the total efficiency with respect to the *desired* signal.

Coding Efficiency

The total efficiency of a class S system is closely related to the modulator's *coding efficiency*, defined as

$$\eta_c = \frac{P_{sig}}{P_{total}} \tag{2.32}$$

where P_{sig} is the power within the signal band, and P_{total} is the total power of the modulated signal. For a discrete-time, lowpass $\Delta\Sigma$ modulator P_{total} is integrated from DC to the Nyquist frequency $f_s/2$. Therefore, the total drain efficiency of a class S system taking into account the desired signal bandwidth is

$$\eta'_D = \eta_c \eta_D \tag{2.33}$$

where η_D is the drain efficiency of the PA alone. This equation assumes an ideal "brick wall" reconstruction filter. In reality, the transmitted power will include a small portion of the out-of-band noise and the filter will possess insertion loss which decreases the efficiency further.

The coding efficiency depends strongly on the statistics of the signal, especially with respect to the output power of the $\Delta\Sigma$ modulator:

$$\eta_c = \frac{\sigma^2_{sig}}{P_{total}} \tag{2.34}$$

where σ^2_{sig} is the power variance of the input signal [52]. The upper limit of the coding efficiency depends not only on the input signal statistics but also on the quantizer limits, the quantizer resolution and the stability of the chosen modulator design [52].

Error Vector Magnitude

A high coding efficiency (and consequently high total efficiency) means little if the signal is not accurately transmitted. The fidelity of a transmitted RF signal is characterized by its EVM or equivalently its relative constellation error (RCE).

The EVM is defined as the magnitude of the error vector from the reference signal to the actual signal, normalized to the maximum reference signal level and expressed as a percentage. The average EVM is

$$\mathrm{EVM} = \sqrt{\frac{\overline{|g_i - g_{i,ref}|^2}}{\overline{|g_{i,ref}|^2}}} \times 100 \tag{2.35}$$

where $g_{i,ref}$ represents the reference vector sequence, and g_i represents the measured vector sequence. The overline denotes the average. The EVM can also be expressed as the RCE. The two are related by

$$\mathrm{RCE} = 20\log\left(\frac{\mathrm{EVM}}{100}\right) \tag{2.36}$$

where the EVM is expressed in % and the RCE is expressed in dB. The nonlinearity present in RF PAs operating in the saturated and efficient regime is typically the largest source of EVM degradation in a conventional transmitter. In a class S system the modulator contributes additional error to the signal depending on the modulator's characteristics. For the modulator alone the EVM is related to the in-band SNR, which in turn depends on the NTF design.

Part of the challenge of $\Delta\Sigma$ modulator design is the dependence on simulations in the design process. This is because closed-form expressions for many modulator figures of merit such as EVM and η_c simply do not exist. Third- and higher-order modulators have the additional parameter of stability to consider. It is important to test a $\Delta\Sigma$ modulator thoroughly with a realistic input signal to ensure stability and acceptable EVM performance.

Previous work examining the relationship between various $\Delta\Sigma$ modulator parameters and figures of merit has been undertaken principally by Johnson, Sobot and Stapleton [52–55]. The authors have demonstrated the importance of the coding efficiency's effect on the load power available from a class S system, furthermore accounting for the coding efficiency losses due to the DACs and PA switch losses. They also note that the coding efficiency depends on the input signal power, but the input power has an upper bound which depends on the modulator stability.

The work of Johnson et al. has focused primarily on the case of a two-level, bandpass $\Delta\Sigma$ pulse train for amplification by a class D amplifier. However, the quantizer in a $\Delta\Sigma$ modulator is not constrained to be two levels. The relationship between quantizer resolution, oversampling ratio, coding efficiency and signal quality is not very well understood in a multidimensional way. Chapter 4 presents a study of the effects of these parameters on the $\Delta\Sigma$ modulator performance.

Chapter 3

Push-Pull Inverse Class F Power Amplifier

Section 2.3 outlined the motivation for SMPAs and described several classes of SMPA. The classes presented were VMCD, CMCD, class F and inverse class F (F^{-1}). The CMCD was noted for its mitigation of the C_{DS} switching loss problem of VMCD, making it much more suitable for RF switching applications.

The class F^{-1} PA is similar to the CMCD in that the transistors experience the same drain current and voltage waveforms in each case. Therefore, the CMCD is often considered the push-pull configuration of the class F^{-1}. However, there is an important difference. The class F^{-1} achieves the desired waveform shaping through explicit termination of harmonic content generated by the transistor nonlinearity under high input drive, whereas in the CMCD the square current waveform is provided by the switching of the transistor and the half-rectified sinusoidal voltage is caused by the output resonant network.

In this chapter the design, implementation and measurement of a class F^{-1} PA in push-pull configuration is presented. This topology is chosen as a way to approximate CMCD operation without having to provide a switching signal to the intrinsic transistor gates. With packaged power devices, the parasitic inductance and losses caused by the packaging effects and bondwires make it difficult to provide the intrinsic gate with a proper switching waveform. Also, class F^{-1} warrants the use of distributed matching elements rather than a lumped element resonator, the former of which are generally more suitable at GHz frequencies anyway.

This chapter is organized as follows. Section 3.1 provides an overview of the design requirements and their motivation. A single-ended class F^{-1} design is carried out in Section 3.2, and its simulated performance is presented. Section 3.3 presents the balun transformer design. The experimental performance of the PA is presented in Section 3.4. Section 3.5 concludes the chapter with a discussion of the results.

The work in this chapter was previously presented in [56].

Table 3.1: Key parameters for the Rogers Corporation RT/duroid 5870 PCB substrate.

Parameter	**Symbol**	**Value**
Dielectric constant	ε_r	2.33
Loss tangent	$\tan\delta$	0.0005
Dielectric thickness		0.508 mm (0.020 in)
Conductor material		Electrodeposited copper
Conductor thickness		17 μm (0.5 oz/ft^2)
Conductivity	σ	59.6×10^6 S/m

3.1 Design Specifications

In recent years GaN high electron mobility transistors (HEMTs) have emerged as the device of choice for high power and high performance amplifiers. The main benefits of GaN HEMTs in PAs are their high breakdown voltage, high current density and good heat dissipation. On the other hand, the reliability of GaN and other III-V semiconductors remains somewhat in question and there is an active research effort investigating these issues [57]. Nevertheless, numerous recent papers have demonstrated high performance GaN PAs exploiting the advantages GaN has to offer (e.g., [23, 38, 42]). For this project the chosen transistor is a general purpose RF power GaN HEMT rated for 10 W saturated output power: the CGH40010F from Cree, Inc. [58]. Since the PA is to be a push-pull design, two such transistors are required. The chosen frequency of operation is 2.5 GHz.

The matching circuits are designed in microstrip to keep the design relatively simple. The chosen printed circuit board (PCB) substrate is the RT/duroid 5870 from Rogers Corporation, for which several key parameters are shown in Table 3.1.

The chosen balun structure (Section 3.3) transforms a 50 Ω unbalanced impedance into a 50 Ω balanced impedance, which is equivalent to an unbalanced impedance of 25 Ω at each of the two balanced ports. This must be accounted for by assuming a 25 Ω input and output impedance when designing the matching network for each single-ended class F^{-1} PA, two of which constitute the push-pull PA.

As described in the previous chapter the ideal harmonic impedances seen by the transistor drain for class F^{-1} operation are

$$Z_{L,2n} = \infty \text{ (open circuit) for even harmonics, and}$$
$$Z_{L,2n+1} = 0 \text{ (short circuit) for odd harmonics.}$$

As is common in harmonically tuned PAs, a compromise is made between the number of harmonic terminations satisfied and the complexity of the matching network. A more complex matching network can lead to additional loss which nullifies the efficiency gained by the additional harmonic termination(s) and the higher-order harmonic content generated by the intrinsic device will be attenuated by the package. In practice, high efficiency can be obtained by terminating only the second and third harmonic as demonstrated in [10, 42].

When the matching network presents close to ideal open/short for the second/third harmonics, the highest efficiency is not obtained. Again the package effects are to blame, effectively moving the impedances seen by the *intrinsic* device away from open/short. To counteract this, the angles of the second and third harmonic reflection coefficients $\Gamma_{L,2f_c}$ and $\Gamma_{L,3f_c}$ should be rotated away from open/short at the package output. Additional efficiency can be obtained by using a harmonic impedance matching network at the device gate with purely reactive harmonic impedances.

Since the transistor operates in a nonlinear regime, traditional RF amplifier design techniques using S-parameters do not suffice. Instead, the best combination of source and load impedances is determined using source and load pull simulation on a large signal model of the chosen transistor supplied by the manufacturer. This is performed for an input power $P_{in} = 28$ dBm, drain bias voltage $V_{DD} = 28$ V and quiescent current of $I_Q = 90$ mA. The fundamental impedances are tuned over entire Smith chart, and the harmonic impedances are tuned around the edges to ensure no harmonic content reaches the PA output. By iteratively tuning the fundamental and harmonic impedances, a set of impedances are eventually found that approximate class F^{-1} operation and provide high power-added efficiency (PAE). After several iterations the design impedances are chosen to be

$$Z_{L,f_c} = 14.2 + j19.3 \tag{3.1}$$
$$Z_{L,2f_c} = j169.2 \tag{3.2}$$
$$Z_{L,3f_c} = -j11.4 \tag{3.3}$$
$$Z_{S,f_c} = 15.3 - j3.9 \tag{3.4}$$
$$Z_{S,2f_c} = -j27.0. \tag{3.5}$$

These are summarized on the Smith chart in Figure 3.1. Note that $Z_{L,2f_c}$ and $Z_{L,3f_c}$ are rotated from the ideal open and short conditions as previously described. Note also that the third harmonic source impedance $Z_{S,3f_c}$ is not included. The PAE exhibits very little variation ($< 2\%$) with respect to $Z_{S,3f_c}$ over the entire Smith chart. It is therefore beneficial to omit the third harmonic tuning from the input matching network entirely, since it only adds complexity and potentially loss to the PA.

One point to note is the particularly high sensitivity of the PAE to the second harmonic source impedance $Z_{S,2f_c}$. The PAE contours from sweeping $Z_{S,3f_c}$ are shown in Figure 3.2, where each contour represents a 1% change in PAE. Near the optimum, the PAE contours are dense signifying a large drop for a small variation in $Z_{S,3f_c}$. However, one side of the optimum shows

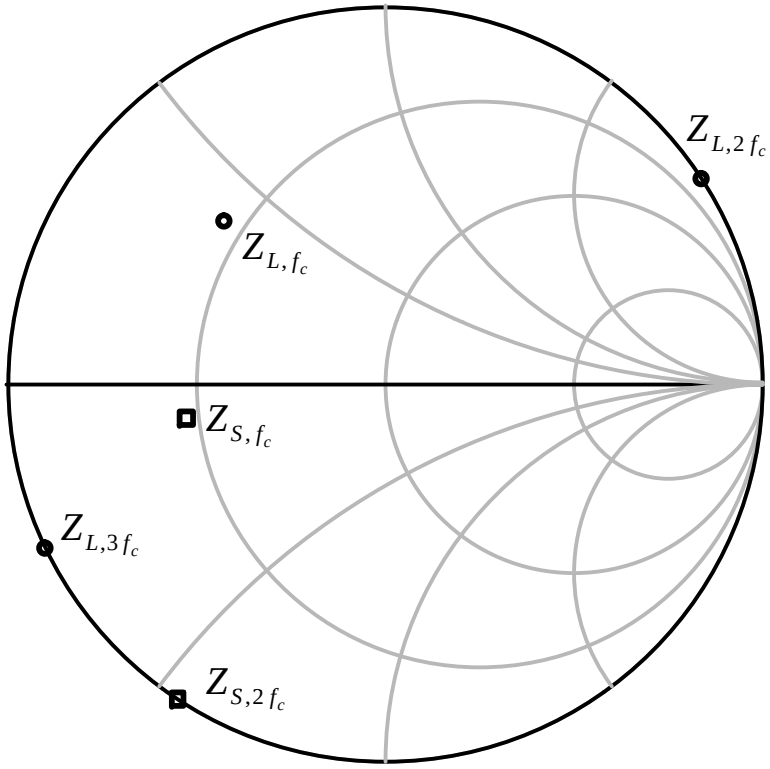


Figure 3.1: Design impedances found from source and load pull simulation. The reference impedance for the Smith chart is 50 Ω.

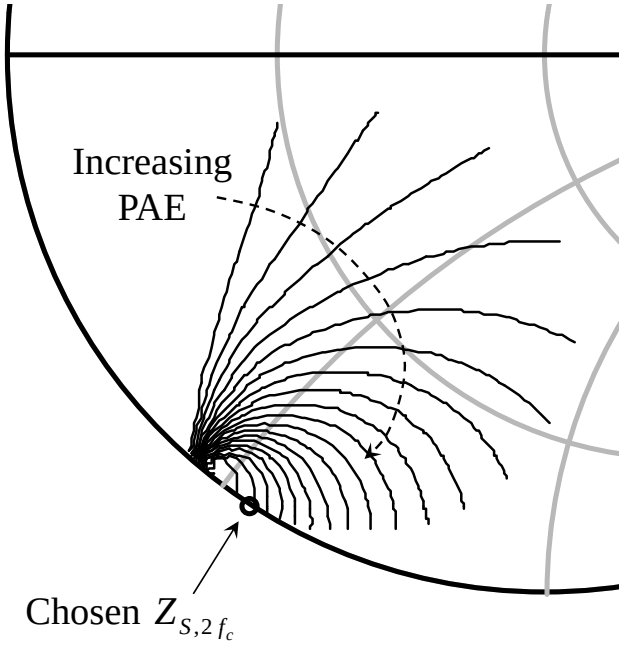


Figure 3.2: PAE contours from second harmonic source pull simulation indicating high sensitivity to $Z_{S,2f_c}$.

a steeper decline in PAE than the other so it is better to choose a design impedance on the less sensitive side of the optimum. This leaves some room for error in PCB fabrication as well as for variations in the active devices due to temperature, soldering and process variations.

3.2 Design of Single Class F^{-1} PA

3.2.1 Matching Network Design

The biasing lines are quarter-wavelength ($\lambda/4$), high-impedance microstrip lines terminated with capacitors. The first capacitor is an RF capacitor large enough to approximate a short-circuit at the design frequency. Additional capacitors are added in parallel to short circuit any low-frequency noise that may be generated by the DC power supply. The largest of these capacitors is 10 μF on the gate side and 33 μF on the drain side. The $\lambda/4$ line causes the capacitors to appear as an open circuit at the main signal path and so the biasing line does not affect the rest of the matching network design. They are placed close to the PA input, rather than the transistor gate, so that the harmonic matching section is also unaffected. For stabilization, the reference design in the transistor datasheet is used [58]. Stability at low frequencies is achieved with a

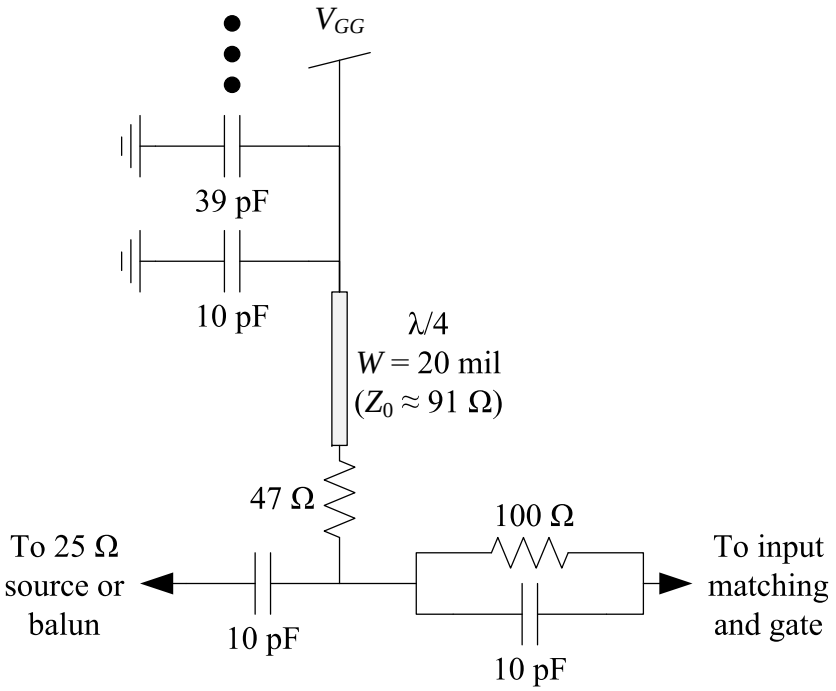


Figure 3.3: Input bias and stabilization network.

series resistor and a resistor on the DC bias line. A capacitor is placed in parallel with the first resistor to allow the RF signal to bypass it. The schematic and component values are displayed in Figure 3.3.

The system impedance for the matching network design is the standard 50 Ω and all microstrip transmission lines used have a 50 Ω characteristic impedance. However, as stated in Section 3.1 the balun causes the matching network design to constitute a transformation to Z_L or Z_S from 25 Ω instead. The matching technique employed is the same as that used in [23] where each section of the matching network corresponds to a single harmonic and the sections are isolated from each other.

The design of the input matching network begins with a shunt quarter-wavelength open stub at the second harmonic, which forms a short circuit. This isolates the harmonic matching section from the rest of the matching network. This short circuit is then rotated around the edge of the Smith chart using a transmission line, until the impedance looking into the transmission line at $2f_c$ is $-j27.0$ Ω. The impedance of a terminated, lossless transmission line is given by

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan\theta}{Z_L + jZ_0 \tan\theta} \tag{3.6}$$

where

$$\begin{aligned} Z_0 &= \text{ the characteristic impedance of the line,} \\ Z_L &= \text{ the terminating impedance, and} \\ \theta &= \text{ the electrical length of the line.} \end{aligned}$$

Substituting $Z_L = 0$ for the quarter-wavelength stub and the required $Z_{in} = Z_{S,2f_c}$, and rearranging

$$Z_{S,2f_c} = jZ_0 \tan\theta \tag{3.7}$$

$$\Rightarrow \theta = \tan^{-1} \frac{Z_{S,2f_c}}{jZ_0} \tag{3.8}$$

$$= \tan^{-1} \frac{-27}{50} \tag{3.9}$$

$$\approx -0.495 \text{ or } -28.3^\circ. \tag{3.10}$$

This is of course not realizable so we add π to get an equivalent length of

$$\theta = 2.647 \text{ or } 151.7^\circ. \tag{3.11}$$

Although the remainder of the matching network does not affect the second harmonic, the fundamental is affected by the second harmonic section. This is illustrated in Figure 3.4. In order to determine the required fundamental impedance seen past the second harmonic section Z_{S2,f_c}, note that the harmonic section transforms Z^*_{S,f_c} (where * denotes the complex conjugate) into

$$Y^*_{S2,f_c} = \frac{1}{Z_0}\left[\frac{Z_0 + jZ^*_{S,f_c}\tan\theta_{l1}}{Z^*_{S,f_c} + jZ_0\tan\theta_{l1}} + j\tan\theta_{s1}\right] \tag{3.12}$$

$$Z_{S2,f_c} = \left(\frac{1}{Y^*_{S2,f_c}}\right)^* \tag{3.13}$$

where

$$\begin{aligned} \theta_{l1} &= \text{ the electrical length of the first transmission line at } f_c, \\ \theta_{s1} &= \text{ the electrical length of the first stub at } f_c \end{aligned}$$

and $Y = 1/Z$ denotes the admittance rather than impedance.

Note also that the input stabilization elements add to the 25 Ω input impedance:

$$Z_{src} = 25 + \frac{1}{j\omega_c(10\text{ pF})} + \frac{1}{\frac{1}{100\Omega} + j\omega_c(10\text{ pF})} \tag{3.14}$$

$$= 25.4 - j12.7\ \Omega. \tag{3.15}$$

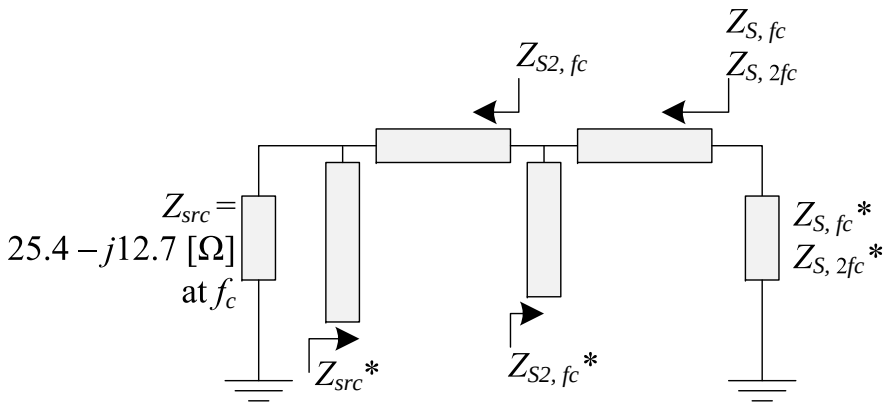


Figure 3.4: Input matching network structure including impedances used for calculation.

A simple single-stub network is used to transform Z_{src} into Z_{S2,f_c}.

The output matching network is designed in a similar way, except using three stubs: one for the fundamental, second harmonic and third harmonic. The second harmonic stub is placed closest to the transistor since during the load pull simulations it was found to have a larger influence on the performance. The second harmonic stub is designed and its effect on the third harmonic impedance is found. The third harmonic stub is then designed, and the effect of both harmonic matching sections on the fundamental is found. Finally, the fundamental matching network section is designed.

Using the Momentum electromagnetic (EM) simulator in Agilent Advanced Design System (ADS), the microstrip matching networks were simulated and tuned to provide the correct impedances at each frequency.

3.2.2 Simulated Performance of Single-Ended PA

The matching networks and large-signal model were used to simulate a single-ended class F^{-1} PA. EM models of the matching network were used, as well as S-parameter models for the critical surface-mount capacitors which were supplied by American Technical Ceramics.

Figure 3.5 displays the simulated output power and PAE versus input power for the single-ended PA. The simulated peak PAE is 78.5% at 2.5 GHz with 29 dBm input power and 40.6 dBm output, for a gain of 11.6 dB.

The simulated drain waveforms of the single-ended PA (at the package plane) are shown in Figure 3.6. The waveforms indicate a reasonable approximation of class F^{-1} behaviour.

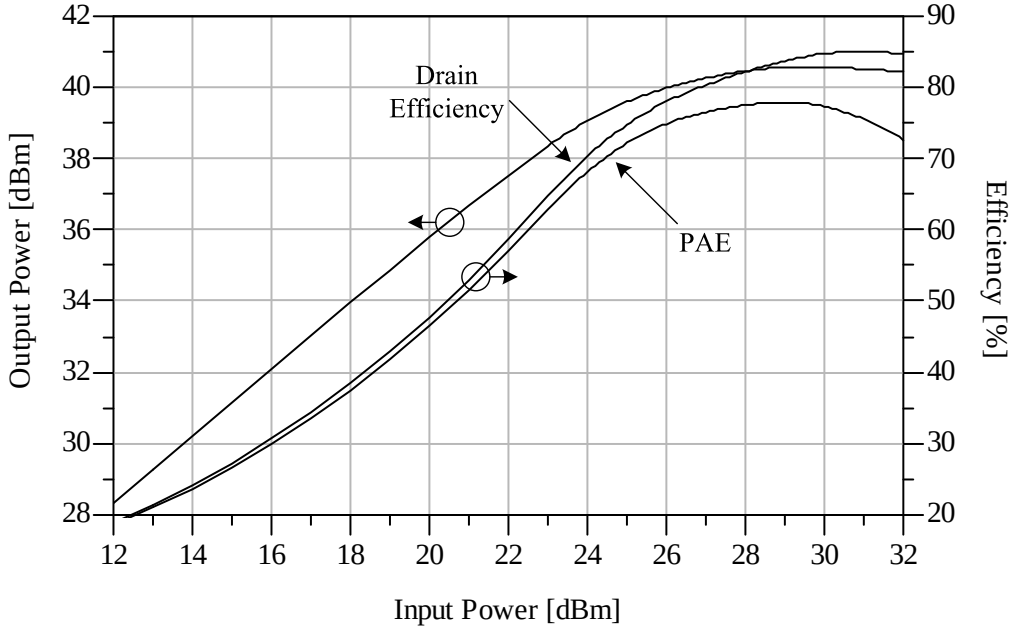


Figure 3.5: Simulated performance of the single-ended PA.

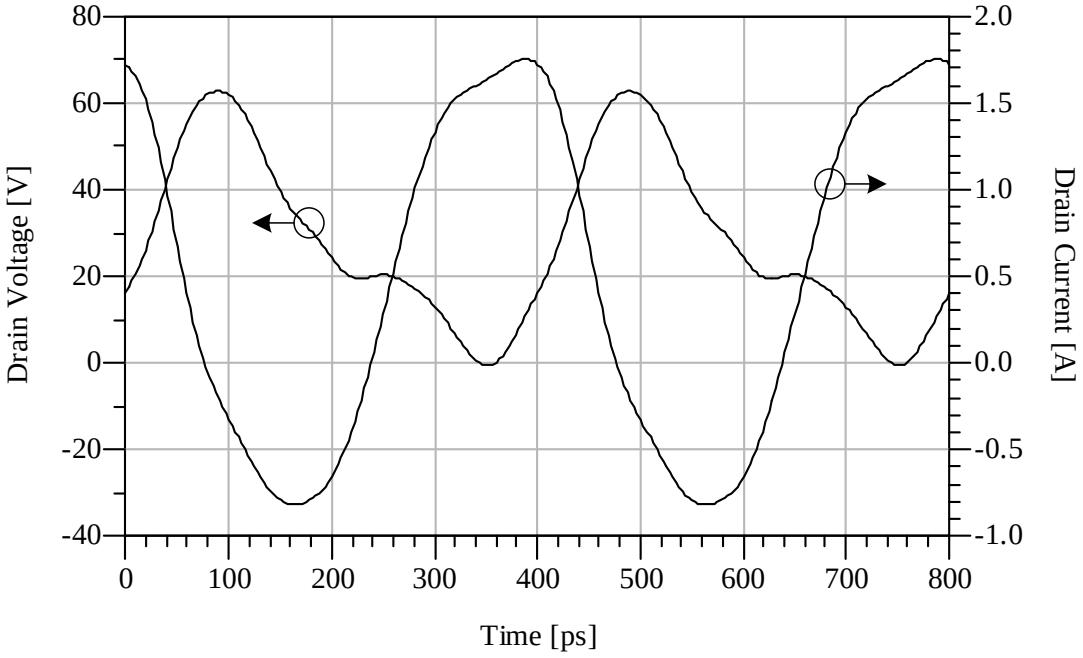


Figure 3.6: Simulated drain waveforms of the single-ended PA.

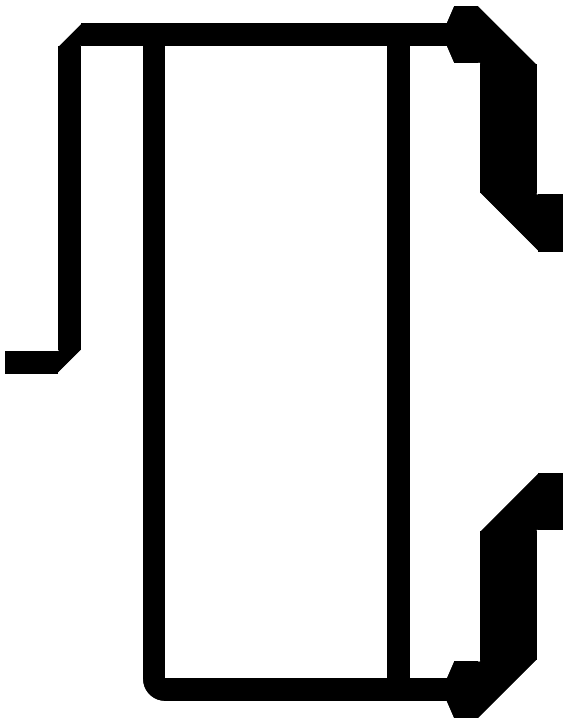


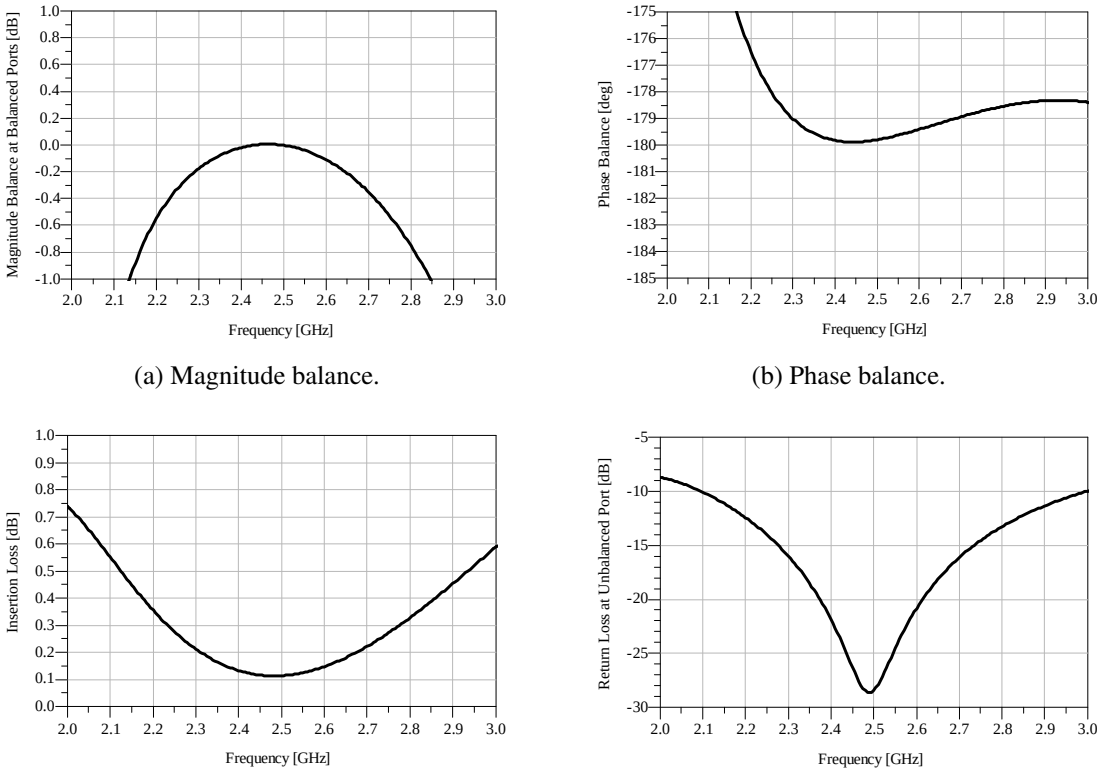
Figure 3.7: Layout of microstrip balun.

3.3 Balun Design and Simulation

With the single-ended PA complete, a balun is needed to perform the single-ended-to-differential conversion at the input and vice-versa at the output. A two-section half-wave topology [59] is chosen as a compromise between simplicity and size. By having the balun in microstrip rather than a discrete component, more control over the design is retained and precise modeling using an EM simulator is possible. In addition, by having the baluns integrated with the rest of the PCB, potential insertion loss from soldering a surface-mount balun is avoided.

The balun layout is shown in Figure 3.7. It consists of two (nominal) half-wave sections and two quarter-wave sections. The microstrip lines at the balanced ports are wider, corresponding to a 25 Ω characteristic impedance. The dimensions of all the sections are optimized in the Momentum simulator to provide as close to ideal balun behaviour as possible (i.e., 180° phase shift between the balanced ports, equal power division, minimal insertion loss and correct impedance match).

This balun is an approximately lossless, three-port network, therefore it is impossible to satisfy a matched condition at all three ports. The relevant optimization condition is chosen as a 50 Ω match at the unbalanced port, when the balanced ports are each terminated with 25 Ω.



(a) Magnitude balance.

(b) Phase balance.

(c) Insertion loss.

(d) Return loss at unbalanced port.

Figure 3.8: Simulated performance of balun.

After optimization, the balun provides a 180° phase shift between the balanced ports to within ±1°, equal power splitting within 0.2 dB, and less than 0.2 dB insertion loss between 2.4 and 2.6 GHz. Figure 3.8 displays the simulated performance metrics of the balun.

3.4 Experimental Results

The balun is used at the input and output to place two identical copies of the class F^{-1} PA into a balanced configuration. The fabricated PA is pictured in Figure 3.9.

Figure 3.10 displays the drain efficiency η_D and output power P_{RF} versus frequency. The input power is approximately 30 dBm, set based on measurements of the efficiency versus input power over the frequency range. η_D is over 70% across more than 80 MHz bandwidth (about 3% relative bandwidth). Notably, no tuning is performed on the PA after fabrication. This is partly responsible for the shift of the centre frequency from 2.5 GHz to approximately 2.46 GHz.

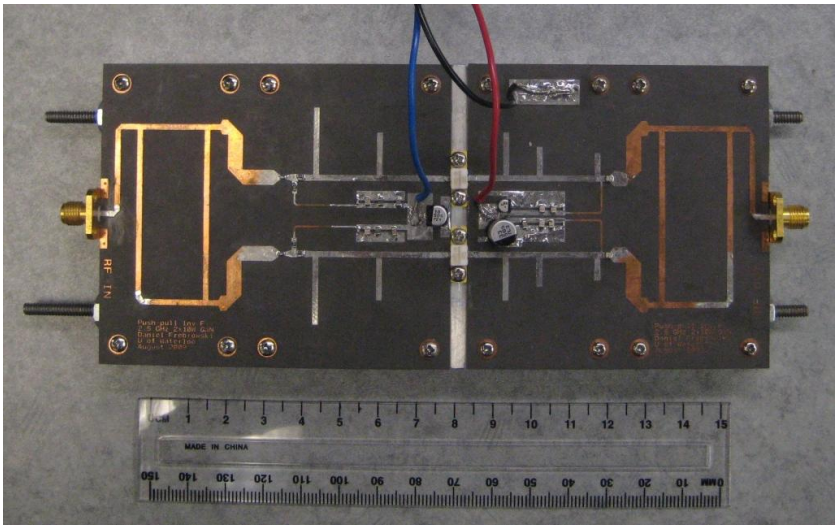


Figure 3.9: Photograph of completed push-pull class F^{-1} PA.

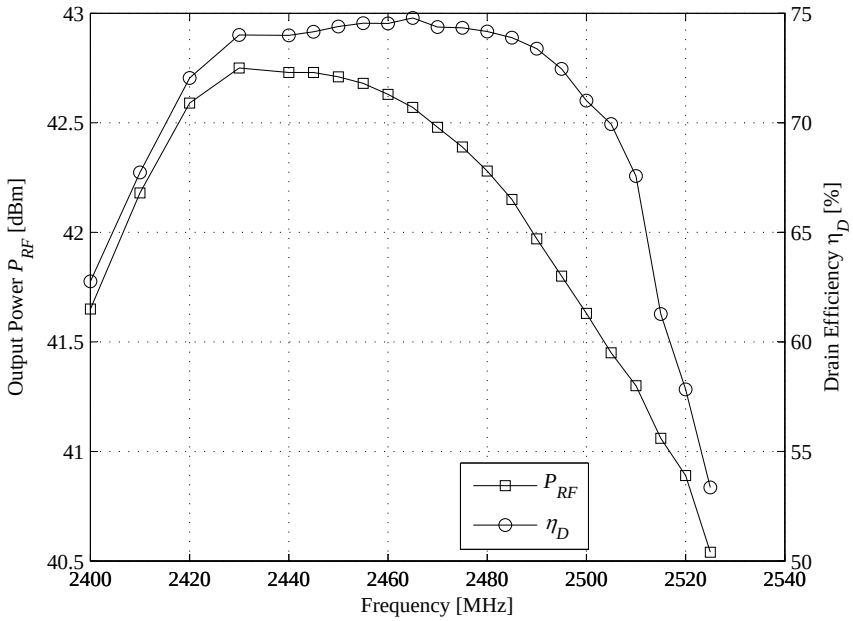


Figure 3.10: Performance of fabricated PA versus frequency for approximately 30 dBm input power.

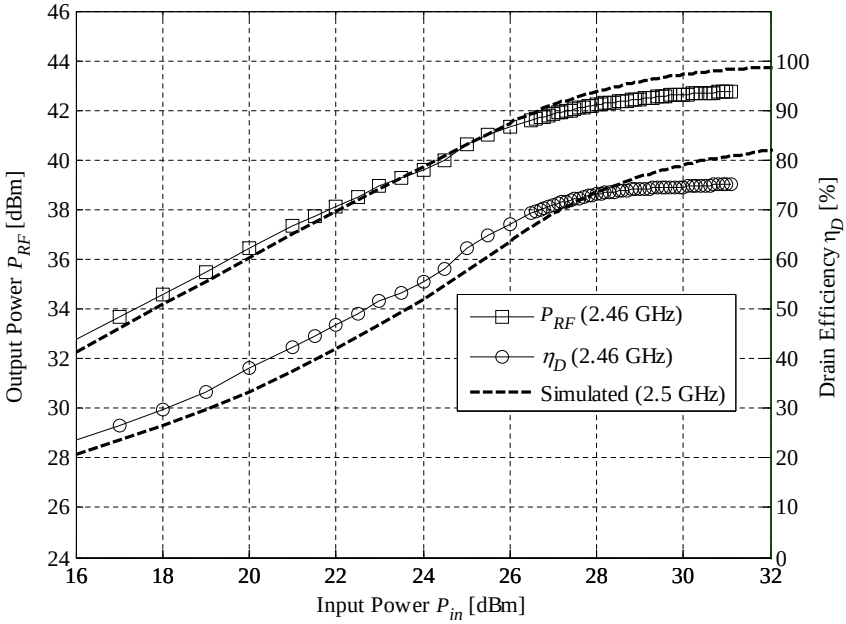


Figure 3.11: Performance of fabricated PA versus input power.

The measured and simulated η_D and P_{RF} versus input power are shown in Figure 3.11. The measured data is at the experimentally determined centre frequency of 2.46 GHz and the simulated data is at the designed centre frequency of 2.5 GHz, to account for the centre frequency shift. The maximum drain efficiency of 75.2% is measured for 31 dBm input power and 42.7 dBm output power. η_D is also shown versus P_{RF} in Figure 3.12.

It is important to note that the agreement between measurements and simulations is in the trend only. The measured η_D does not necessarily represent an improvement in efficiency over the simulation results. The main reason for this is that the centre frequency in terms of measured performance is different from the design frequency, due to variations in manufacturing of both the PCBs and the transistors.

3.5 Conclusion and Discussion

The CMCD configuration of PA is a good SMPA candidate for RF applications. It is often considered to be the push-pull configuration of the inverse class F PA with the caveat that the waveform shaping is provided by different mechanisms. In the case of the CMCD a switching input waveform causes the current through each switch to be a square wave, while in the class F^{-1} the waveform shaping is due to termination of harmonic content generated by the transistor's nonlinear operation.

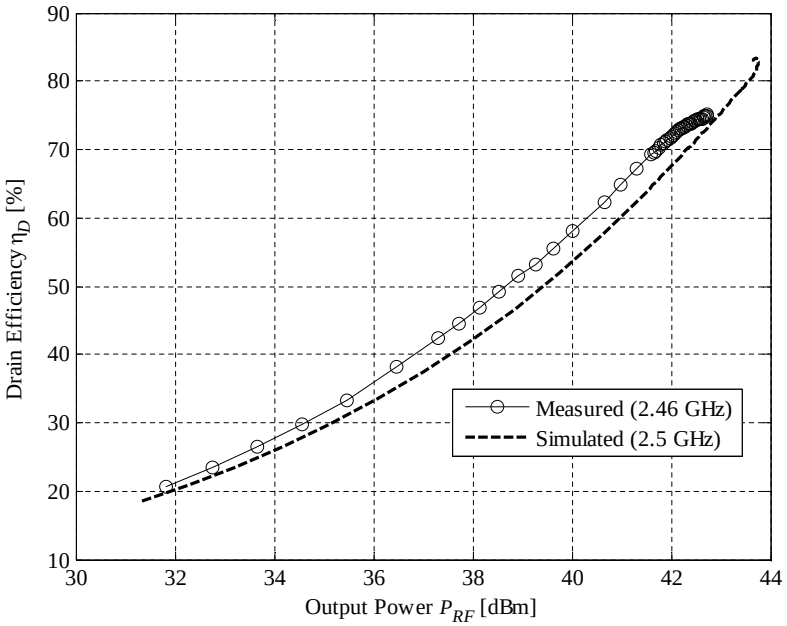


Figure 3.12: Drain efficiency of fabricated PA versus input power.

As a means to better understand the RF requirements of CMCD PAs, the analogous push-pull class F^{-1} PA is implemented, achieving maximum drain efficiency of over 75%, and over 70% drain efficiency across an 80 MHz bandwidth.

Figure 3.11 illustrates good agreement between the simulated results and the measured PA performance. This speaks to the importance of having an accurate large-signal model of the chosen device available for simulation. Combining this accurate transistor model with accurate EM modeling of the matching networks results in a fabricated PA which performs in good agreement with simulations without post-fabrication tuning as is typically required.

The input matching network of this PA includes a quarter-wavelength stub at the second harmonic. Besides improving the efficiency of the PA this stub causes the second harmonic content of the input signal to be reflected back to the signal source. For a switched signal there may be significant power located at the second harmonic (although not for a 50% duty cycle square wave containing power only at the odd harmonics) which does not reach the transistor gate. This is not an issue for class F^{-1} PAs; however, a CMCD PA treats the transistor as a switch and so the full switching signal should reach the intrinsic transistor gate. Furthermore, the package may not pass harmonic content to the transistor die. Therefore, the design of the input matching network for CMCD is complicated by the additional requirement that the intrinsic transistor gate must experience a fully switching signal, compared to the class F^{-1} requirement that the input simply be of sufficiently high power. This is not considered in this design but would be a consideration in a future implementation.

Chapter 4

Delta-Sigma Modulator Study

Delta-sigma ($\Delta\Sigma$) modulators have found several applications in wireless transmitters. Since they involve quantization of a signal into discrete states, they have been used to increase the digital portion of RF transmitters. This enhances the reconfigurability of the transmitter and makes it more suitable for SDR and CR applications. Section 2.2 provided several examples of such transmitters.

SMPAs also increase the reconfigurability of wireless transmitters by operating on a switching signal, providing compatibility with digital circuits. However, such a signal has a constant amplitude, a feature incompatible with wireless communication standards which are moving more towards increasing the PAPR in order to improve the spectral efficiency (i.e., the bits-per-second-per-Hz ratio). PWM and $\Delta\Sigma$ modulation are two ways of encoding amplitude and phase information into the timing of digital level transitions. The original signal can then be recovered or reconstructed with a BPF. The cascade of a $\Delta\Sigma$ modulator, SMPA and BPF is typically referred to as a class S system. Class S amplifier systems were briefly covered in Section 2.4.2.

SMPAs are attractive for their high efficiency as well as for their potential usefulness in SDR. However, when driven by a switching signal they amplify not only the desired signal but also the broadband content which shapes the pulses. An output BPF attenuates this extra content and so although the SMPA may amplify the digital signal very efficiently, the useful signal power is relatively small. The ratio of the useful signal power to total signal power is called the coding efficiency η_c and was outlined in Section 2.4.2 in the context of $\Delta\Sigma$ modulators.

With today's wireless standards the quality of the transmitted signal is arguably the single most important feature of a transmitter. This is affected enormously by the linearity of the PA. Highly efficient PAs operate in the nonlinear region, causing unacceptable degradation of the EVM and leakage of distortion into adjacent and far-out signal bands. SMPAs offer linear amplification only of constant envelope signals. When a varying power RF signal is encoded into a constant envelope signal for amplification by an SMPA (such as by a $\Delta\Sigma$ modulator), the encoder may introduce distortion into the signal band, lowering the SNR and raising the EVM.

Table 4.1: LTE signal parameters for simulation.

Parameter	**Value**
Signal type	3GPP LTE downlink
Bandwidth	3 MHz
Carrier frequency	2.140 GHz
Base sampling rate	3.84 MHz
Frame mode	Frequency division duplexing (FDD)
User equipment (UE) signals	1
UE signal mapping type	16 QAM
UE resource blocks (RB)	1 to 15 (all RBs)
Spectrum shaping	Tukey time windowing

The relationships between $\Delta\Sigma$ modulator performance figures (such as coding efficiency and SNR) and design parameters (such as oversampling and quantizer resolution) are not straightforward and closed-form equations for many of these relationships do not exist. The $\Delta\Sigma$ modulator design process must therefore include simulations with realistic input signals to ensure adequate coding efficiency, acceptable SNR/EVM and good stability.

This chapter presents a study of a few of these relationships and is organized as follows. Section 4.1 establishes the framework for the study including the signal characteristics; $\Delta\Sigma$ modulator structure, parameters and design methodology; and test transmitter architecture. Section 4.2 presents the results of the simulations and a discussion of the key findings. Section 4.3 presents the measured results for a representative $\Delta\Sigma$ modulator to validate the simulations. Finally, Section 4.4 concludes the chapter with a summary of the results and a discussion of future work.

4.1 Simulation Framework

4.1.1 Signal Characteristics

The chosen signal specification is the 3rd Generation Partnership Project's (3GPP) Long Term Evolution (LTE) specification. The downlink signal is based on orthogonal frequency division multiple access (OFDMA) with selectable channel bandwidth from 1.4 to 20 MHz. The chosen signal parameters for the simulation are listed in Table 4.1.

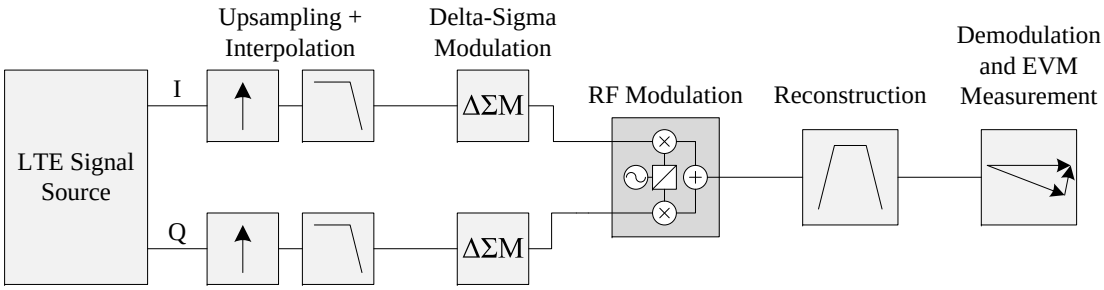


Figure 4.1: Schematic of ΔΣ modulator simulation.

Note that the base sampling rate of 3.84 MHz is the reference sample rate for all oversampling. That is, when an OSR of 4 is considered, the sample rate is 4×3.84 MHz $= 15.36$ MHz.

4.1.2 Simulation Setup

The simulation platform is the Ptolemy DSP simulator in Agilent ADS. Figure 4.1 illustrates the simulation schematic. The I and Q components are upsampled and interpolated depending on the OSR being examined. The oversampled signals are then quantized using lowpass ΔΣ modulators.

In order to capture the effect of the ΔΣ modulation accurately, the reconstruction filter must have very stringent specifications on passband ripple and stopband attenuation. Finite impulse response (FIR) filters are designed in MATLAB for this purpose using the equiripple method with passband ripple constrained to ≤ 0.02 dB and stopband attenuation set to 80 dB. The quantization noise begins very close to the signal band, so a filter with a very sharp rolloff is required to give good stopband attenuation while maintaining passband flatness.

The coding efficiency η_c is measured at the point immediately following the ΔΣ modulator and the signal quality is measured after RF modulation using the EVM measurement tool in the ADS LTE design kit. The quoted EVM in this study is that of the UE signal averaged across all resource blocks.

4.1.3 ΔΣ Modulator Design Methodology

Second- and third-order ΔΣ modulators are chosen for this study. The CIFB topology is used which was illustrated previously in Figure 2.25 on page 33. The MATLAB toolbox written by Schreier [49] is used for all ΔΣ modulator designs. First the NTF is designed for the given ΔΣ modulator with optimization of the NTF zeros enabled to minimize the in-band SNR. The STF is constrained to have the same poles as the NTF, and for simplicity the STF is designed with

one zero at $z = 0$. The coefficients are then calculated for the given modulator form (in this case CIFB). One set of coefficients is found for each tested OSR.

The chosen quantizer resolutions are 2 levels (1 bit), 4 levels (2 bits), 8 levels (3 bits) and 16 levels (4 bits), and 32 levels (5 bits). The tested OSRs are 4, 8, 16 and 32, relative to the base sampling rate of 3.84 MHz.

Careful control of the input signal amplitude is required in order to maximize the coding efficiency while ensuring that the modulator is stable. A gain is applied to the input signal and increased until a sharp increase in the EVM is observed. This is the point which indicates quantizer saturation or instability. The gain is then reset to the value which provides acceptable EVM.

4.2 Simulation Results

4.2.1 Second-Order Modulator

Figure 4.2(a) shows the simulated results for the second-order $\Delta\Sigma$ modulator, versus the number of bits in the output quantizer as explained in the previous section. Each line represents a different OSR. For all OSRs, the coding efficiency increases rapidly as the quantizer is changed from 1 to 3 bits. 4 bits provides less of an added benefit, and the 5-bit quantizer provides even less of a change since the coding efficiency is nearly saturated at this point. This is a useful observation since, in terms of hardware, the number of quantizer bits may reflect the complexity of the system which follows the $\Delta\Sigma$ modulator. For example, an extra bit can result in twice as many unit elements required for a PA. Therefore we can conclude that when considering the tradeoff between coding efficiency and system complexity, there is little to be gained by choosing a 5-bit quantizer over a 4-bit quantizer.

In the same plot, the EVM is expressed instead as the negative of the RCE (see Equation 2.36 on page 36), so that a higher value represents better signal quality analogous to the SNR. For low OSRs the benefit of having enhanced quantizer resolution is clear. For higher OSRs, this benefit is less apparent. The RCE appears to saturate around -50 dB. The reason for this is assumed to be a result of either the rounding precision of the simulator or the design of the FIR filters.

Figure 4.2(b) shows the same results, but with OSR on the horizontal axis and each line representing a different quantizer resolution. The OSR appears to negatively affect the coding efficiency, especially for low quantizer resolutions. On the other hand, for lower quantizer resolutions the OSR strongly affects the signal quality but the improvement saturates. For example, for the 3 bit quantizer, a 10 dB improvement is seen for an OSR of 16 over OSR of 8; however, doubling the OSR again barely yields an additional 2.5 dB. In a hardware context, choosing the lower OSR relaxes the frequency requirements for the modulator and RF components. In this

way a small tradeoff in signal quality may be acceptable for a simpler or more cost effective implementation.

4.2.2 Third-Order Modulator

Figure 4.3(a) shows the simulated results for the third-order ΔΣ modulator, versus the number of bits in the output quantizer. For the coding efficiency, a trend similar to the second-order case is observed: the benefit of a 5-bit quantizer over 4 bits is not as great as for the lower-resolution cases. Similarly, the benefit of higher quantizer resolution is greatest for the 3-bit case versus the 2-bit case.

Figure 4.3(b) displays the same data versus the OSR. Compared to the second-order modulator, there is a more pronounced effect of OSR on coding efficiency, especially for the lower quantizer resolutions and lower OSRs. The trends for the signal quality (i.e., RCE) are very similar to those of the second-order modulator. For low quantizer resolution, increasing the OSR can provide substantial benefits; however, for the 3-bit, 4-bit and 5-bit quantizers little improvement is observed beyond an OSR of 16.

4.3 Measurement Validation

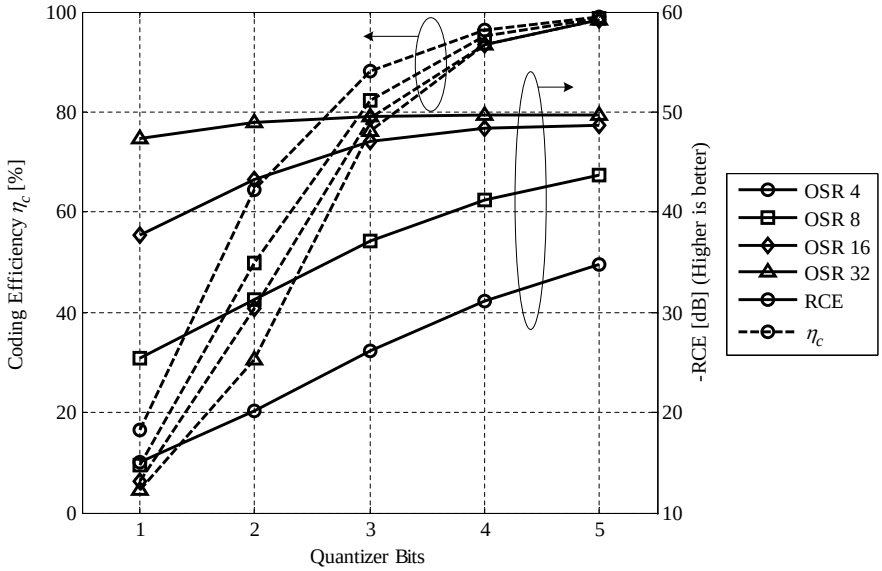
As a check of the validity of the simulations, a representative ΔΣ modulator (the second-order, 16× OSR, 3-bit quantizer case) is chosen for implementation in hardware using an Altera Stratix II FPGA platform. One frame of LTE data is stored in the FPGA and upsampled to 16× using FIR filters. The upsampled data is ΔΣ modulated and output to an RF DAC evaluation module (the DAC5688EVM from Texas Instruments Inc.). The coding efficiency is measured using a spectrum analyzer which also downconverts and captures the data for RCE calculation.

Figure 4.4 shows the measured spectrum of the signal. The relevant bandwidth is 61.44 MHz; that is, the sampling frequency of the ΔΣ modulation. The measured power in the 3 MHz signal band is -6.3 dBm, and the power across the 61.44 MHz (Nyquist) band is -5.1 dBm. This corresponds to a coding efficiency of

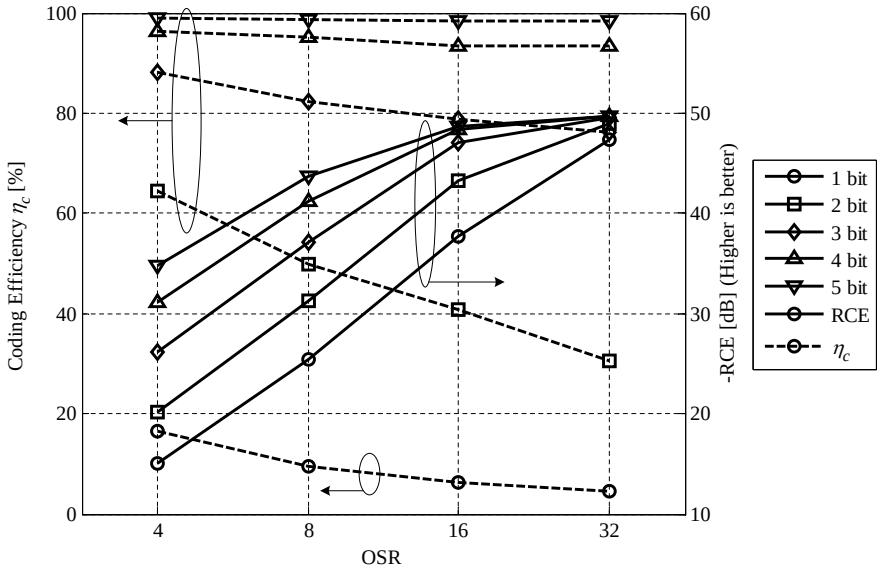
$$\eta_c = \frac{10^{-6.3/10}}{10^{-5.1/10}} \times 100 = 75.9\%. \tag{4.1}$$

This is in close agreement with the simulated coding efficiency for this ΔΣ modulator which was 78.9%.

Agilent ADS is used to demodulate the measured signal. The measured RCE of the system is -40.2 dB (0.9%). This is somewhat worse than the simulated result of -47.0 dB (0.5%) for

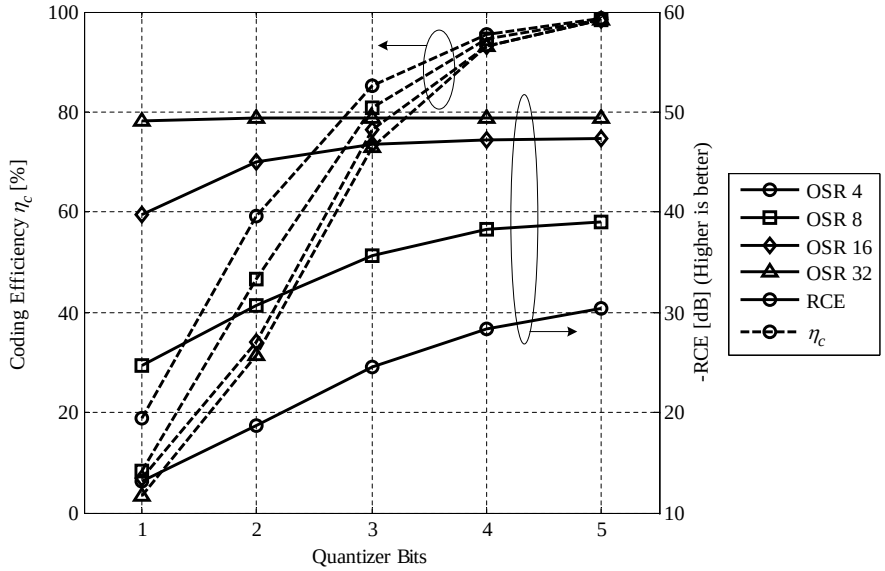


(a)

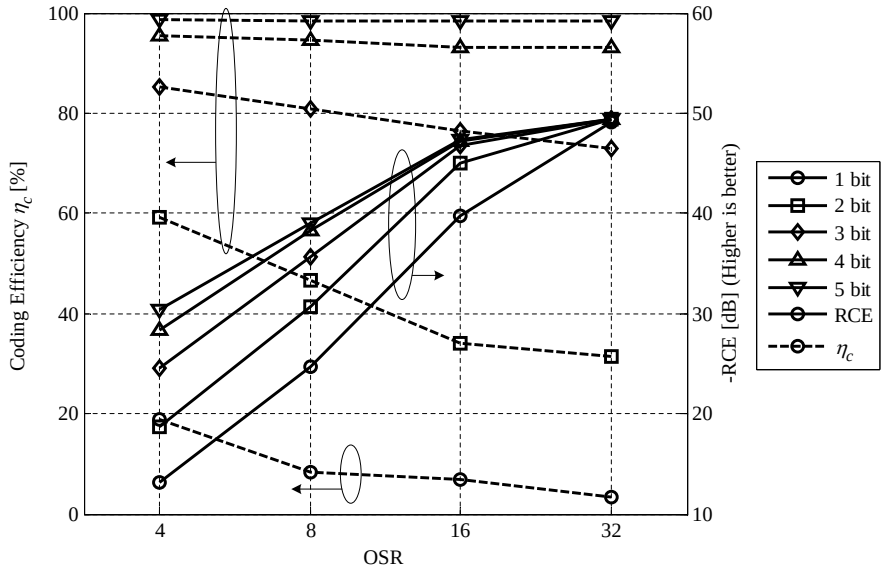


(b)

Figure 4.2: Performance of second-order ΔΣ modulator.



(a)



(b)

Figure 4.3: Performance of third-order ΔΣ modulator.

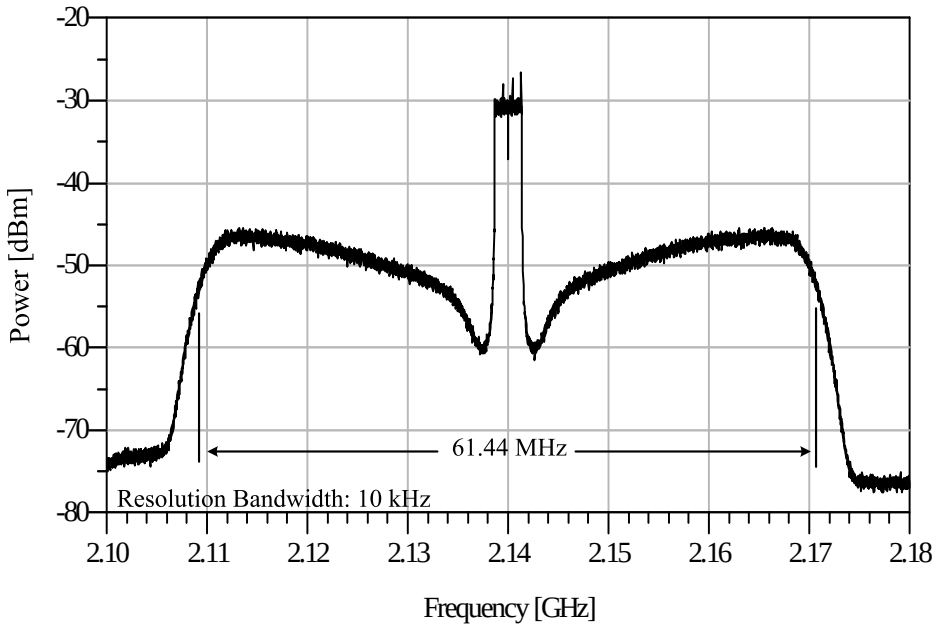


Figure 4.4: Measured spectrum of the ΔΣ modulated LTE signal.

this particular ΔΣ modulator configuration. The discrepancy can be attributed to noise and error in the hardware chain as well as the reduced bit precision of the hardware as compared to the floating point precision of the simulations. This is corroborated by the measured RCE of the 16× oversampled data without the ΔΣ modulator being only -42.8 dB (0.7%).

4.4 Conclusion

Interest in SMPA for SDR and reconfigurable radios is increasing due to SMPA's commonalities with inherently flexible digital circuits. With this interest has come a need to encode information into the time domain rather than the amplitude or power domain, due to the decreasing voltage headroom and improved timing resolution of modern digital IC processes. The way in which certain parameters concerning digital signal modulation techniques/circuits translate to the RF domain is not yet well-understood.

In order to better understand the tradeoffs between digital circuit complexity, digital performance and RF performance, a study of a set of ΔΣ modulators with adjustable parameters is undertaken. In this way the effect of each parameter on the RF performance can be observed. For both the second- and third-order modulators, it is clear that there are certain limits in terms of performance with respect to the coding efficiency and signal quality. For example, moving beyond 4 bits of quantizer resolution improves the coding efficiency very little. Similarly, 32×

oversampling provides only a modest improvement in signal quality over 16× oversampling, although this may also depend on other factors such as filter design and DSP precision. These observations allow the digital/RF transmitter designer to better decide on the implementation strategy from a cost/benefit point of view.

The reconstruction filter specifications resulting from a ΔΣ modulator design were not directly studied in this work. However, it is clear from Figure 4.4 that this aspect of the system-level design must be considered. The nature of ΔΣ modulation means that the quantization noise, although suppressed within the signal band, rises steeply just outside the signal band. This problem is even more prevalent in higher-order modulators which suppress in-band noise more effectively but result in steeper close-in noise shaping. This results in a requirement for reconstruction filtering with a very high quality factor (Q) to adequately suppress the close-in noise. If not adequately filtered, this noise can easily interfere with adjacent channels and/or violate spectral emission masks.

Now that a study of some of the tradeoffs of ΔΣ modulators is complete, a logical next step is to consider possible implementations of the ΔΣ modulator in a transmitter setting from a system level. Several such transmitter architectures appearing in the literature were explained in Chapter 2. Most of the presented transmitters and class S systems employ a 1-bit ΔΣ modulator and rely on oversampling to improve the signal quality. However, this approach neglects the coding efficiency which, as shown in this chapter, is strongly affected by the number of bits of quantizer resolution.

In order to have a high overall transmitter efficiency, the coding efficiency needs to be improved while maintaining signal quality. This work shows that signal quality and coding efficiency can be traded off through the quantizer resolution and the oversampling. This fact is already exploited in the extreme cases by class S PA systems and by ΔΣ data converters. In the case of class S systems, the resolution of the ΔΣ modulator is low to minimize the system complexity and high oversampling is used to retain signal quality. On the other hand, data converters often sample at a lower rate and quantize more finely. There exists a set of design choices between these two extremes which can be used in the context of RF transmitters. The potential impact of these tradeoffs can be seen in the following examples of ΔΣ modulator-based transmitter/PA topologies.

In the topology of Figure 4.5, the I and Q outputs of two multilevel baseband ΔΣ modulators drive a frequency conversion stage which modulates the signal to RF. The RF signal is then amplified, filtered and radiated. The quantizer resolution (N) affects both the coding efficiency and the signal quality. Increasing the resolution may increase the complexity of the frequency conversion stage compared to using 1-bit modulators; however, the performance requirements may be relaxed by reducing the OSR with a corresponding reduction in cost and complexity. The net effect on the signal is an improvement of coding efficiency without a reduction of signal quality. The frequency conversion could be implemented digitally (e.g., [8–10]) to increase transmitter reconfigurability. The drawback of this architecture is that it may be difficult to pro-

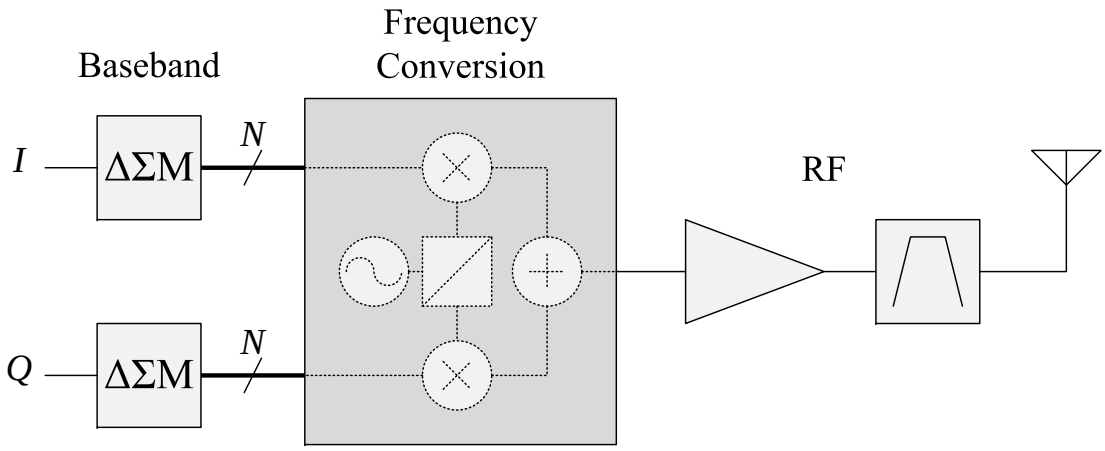
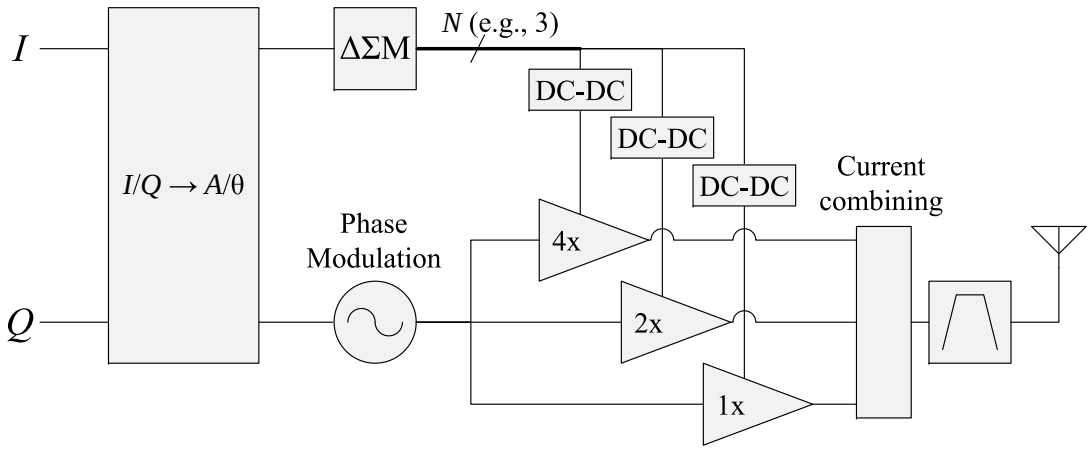


Figure 4.5: I/Q-based transmitter with baseband $\Delta\Sigma$ modulators.

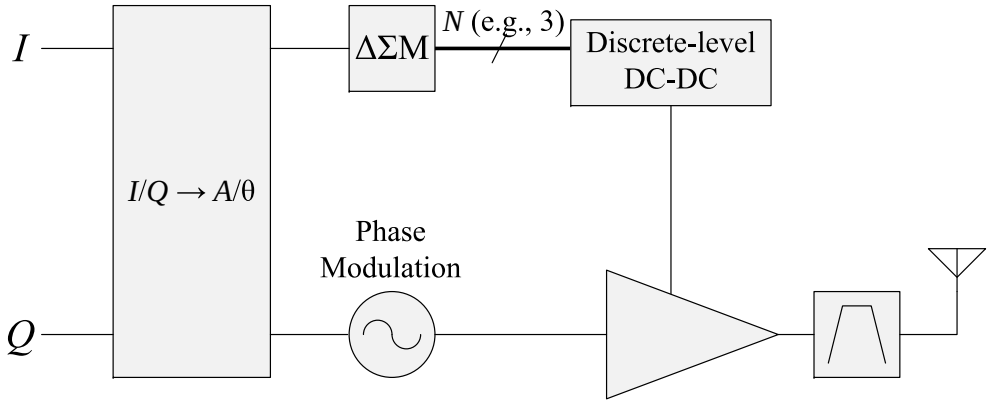
vide a constant-envelope or switched signal to the PA input when using multilevel $\Delta\Sigma$ modulators so that a high efficiency or switching-mode PA can be used.

Figure 4.6 illustrates the use of a $\Delta\Sigma$ modulator in a polar transmitter to modulate the amplitude component of the complex envelope, while the phase component is modulated onto the RF carrier. In Figure 4.6(a), the $\Delta\Sigma$ modulator output bits are then used to control a set of binary-weighted PAs which are summed using current combining. Using this technique allows each weighted PA to amplify a constant envelope input efficiently. However, as usual with polar transmitters, the expanded bandwidth of the amplitude and phase components is a drawback. An additional issue is the efficiency degradation arising from the current combining stage, mainly due to the effect of load modulation on each PA. Note that although this topology is similar to that of [16] (Figure 2.9 on page 14), this topology proposes the $\Delta\Sigma$ modulation for encoding of the signal envelope in a binary-weighted fashion whereas in [16] the $\Delta\Sigma$ modulation is used for dithering of unit amplifiers. Figure 4.6(b) illustrates a similar alternative topology in which a discrete-level DC-DC converter is used to control a single PA, eliminating the issue of load modulation due to current combining.

A hybrid solution combining the previous two ideas is illustrated in Figure 4.7. The I and Q components are each $\Delta\Sigma$ modulated and the output bits used to control a PA in each branch. This performs the upconversion with the LO. A quadrature hybrid then combines the two components for transmission. This approach has two main benefits: the DC-DC converter bandwidth is reduced compared to the polar approach and the PAs can be narrowband since their input is a single tone. However, the 50% combining efficiency of the quadrature hybrid is a significant issue. One possible way to get around this is to offset the LO to the Q PAs by 90° but the power combining may still be inefficient and complicated by potential load modulation in the case of a non-isolated combiner.



(a)



(b)

Figure 4.6: Polar transmitter with envelope ΔΣ modulation.

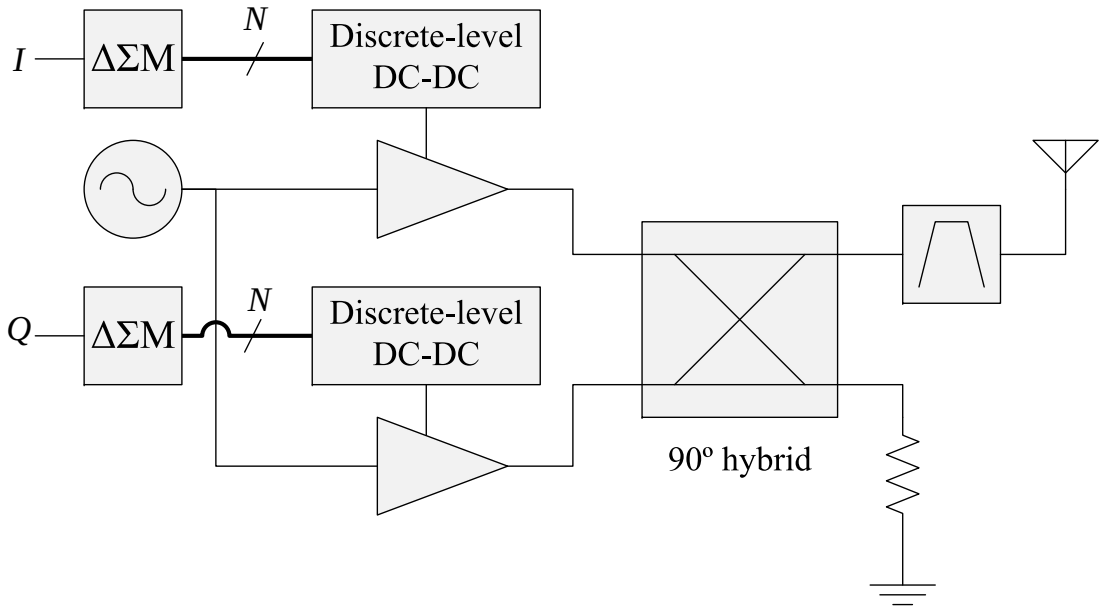


Figure 4.7: Transmitter combining ΔΣ modulated polar transmitter approach and quadrature multilevel ΔΣ modulator approach.

In all cases, the design of the ΔΣ modulator has a substantial effect on the specifications and design of the rest of the system. The resolution determines in part the complexity/area of the system, in turn affecting the power consumption, cost and device mobility. The oversampling sets the frequency specifications of the system, which also affects the power consumption as well as the cost through the choice of fabrication technology.

Chapter 5

Conclusion and Future Research Direction

This thesis studies two important innovations which are shaping the future of reconfigurable RF transmitter design: switching mode power amplifiers and time-domain signal modulation techniques. The PA presented here is part of an ongoing effort in the research community investigating high efficiency PAs. Since SMPAs share their switching operation with digital circuits it is important to investigate their performance and characteristics in such a context rather than under the typical single-tone input case. Some work is well underway in this area (e.g., [29]), but much remains to be improved and many issues to be resolved.

The class F^{-1} PA in Chapter 3 is designed and measured outside the context of digital circuits, with the aim of developing a strong foundation of insight and understanding of the RF requirements of SMPAs. Similarly, the study of $\Delta\Sigma$ modulators presented in Chapter 4 is undertaken mostly outside the PA context, although it was inspired and motivated by SMPAs. Now that this work is complete, the next step is to combine this knowledge into a full transmitter. This will provide a platform through which to investigate the interaction of time-domain modulation and SMPAs in the real world.

Several possible transmitter topologies taking advantage of this work are presented in Section 4.4, and the choice of topology to pursue in future research has yet to be decided. The choice will be influenced by a study of which architecture, combined with which IC technologies, will lend itself best to a fully reconfigurable system. In the case of the quadrature modulated system of Figure 4.5 (page 60), a good approach would be to implement the signal generation including the frequency conversion stage in an advanced digital CMOS process. This has already been demonstrated using digital techniques as in the DDRM architecture in Section 2.2.1 [5–8]. This would be followed by a power stage in a high-power technology such as GaN or gallium arsenide (GaAs). The whole system could then be integrated into a single package acting as a power RF DAC. A second approach would be to use the combined digital and RF capabilities of a process such as silicon germanium bipolar CMOS (SiGe BiCMOS).

Although this work emphasized $\Delta\Sigma$ modulation for the time-domain modulation, PWM is also worth exploring further. To this end a digitally-controlled PWM IC has been fabricated in 90 nm CMOS and is being tested at the time of this writing.

For a preliminary investigation of the performance of an integrated time-domain modulation and SMPA solution, silicon CMOS may be sufficient. A proof-of-concept IC and subsequent implementation incorporating higher-performance technologies such as GaN may be the subject of future research. Further enhancement of the transmitter reconfigurability should subsequently be explored.

As was demonstrated in Chapter 2, research in RF transmitters is moving towards reconfigurable transmitters implemented with as much digital hardware and design philosophy as possible. However, the relationships between digital performance and RF performance are not straightforward. Parameters and techniques common in the digital domain today must be transferred to the RF domain (and vice-versa) to enable designers of future SDR and CR circuits to bridge the gap between digital and RF electronics which exists today.

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