

Reconfigurable Impedance Matching Networks Based on RF-MEMS and CMOS-MEMS Technologies

by

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Siamak Fouladi Azarnaminy

Abstract

Reconfigurable impedance matching networks are an integral part of multiband radio-frequency (RF) transceivers. They are used to compensate for the input/output impedance variations between the different blocks caused by switching the frequency band of operation or by adjusting the output power level. Various tuning techniques have been developed to construct tunable impedance matching networks employing solid-state p-i-n diodes and varactors. At millimeter-wave frequencies, the increased loss due to the low quality factor of the solid-state devices becomes an important issue. Another drawback of the solid-state tuning elements is the increased nonlinearity and noise at higher RF power levels.

The objective of the research described in this thesis is to investigate the feasibility of using RF microelectromechanical systems (RF-MEMS) technology to develop reconfigurable impedance matching networks. Different types of tunable impedance matching networks with improved impedance tuning range, power handling capability, and lower insertion loss have been developed. Another objective is to investigate the realization of a fully integrated one-chip solution by integrating MEMS devices in standard processes used for RF integrated circuits (RFICs).

A new CMOS-MEMS post-processing technique has been developed that allows the integration of tunable RF MEMS devices with vertical actuation within a CMOS chip. Various types of CMOS-MEMS components used as tuning elements in reconfigurable RF transceivers have been developed. These include tunable parallel-plate capacitors that outperform the available CMOS solid-state varactors in terms of quality factor and linearity. A tunable microwave band-pass filter has been demonstrated by employing the proposed RF MEMS tunable capacitors. For the first time, CMOS-MEMS capacitive type switches for microwave and millimeter-wave applications have been developed using TSMC 0.35- μm CMOS process employing the proposed CMOS-MEMS integration technique. The switch demonstrates an excellent RF performance from 10-20 GHz.

Novel MEMS-based reconfigurable impedance matching networks integrated in standard CMOS technologies are also presented. An 8-bit reconfigurable impedance matching network based on the distributed MEMS transmission line (DMTL) concept operating at 13-24 GHz is presented. The network is implemented using standard 0.35- μm CMOS technology and employs a novel suspended slow-wave structure on a silicon substrate. To our knowledge, this is the first implementation of a DMTL tunable MEMS impedance matching network using a standard CMOS technology. A reconfigurable amplifier chip for WLAN applications operating at 5.2 GHz is also designed and implemented. The amplifier achieves maximum power gain under variable load and source impedance conditions by using the integrated RF-MEMS impedance matching networks. This is the first single-chip implementation of a reconfigurable amplifier using high-Q MEMS impedance matching networks. The monolithic CMOS implementation of the proposed RF MEMS impedance matching networks enables the development of future low-cost single-chip RF multiband transceivers with improved performance and functionality.

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Chapter 1

Introduction

1.1 Motivation

Multi-band RF front-ends based on reconfigurable integrated circuits have an important role in wireless communication systems. These systems are developed to support more than one frequency band of operation. In addition to multi-band functionality, they can dynamically adapt themselves to varying operational conditions such as temperature drift, and variations due to aging and manufacturing tolerances in active circuit elements.

Reconfigurable impedance matching networks are key components in any multi-band RF transceiver circuit. They are used to increase the overall system performance in terms of power efficiency and linearity by compensating for the input/output impedance variations between the different building blocks within an RF front-end such as power amplifiers (PAs), antennas and low noise amplifiers (LNAs) caused by switching the frequency band of operation or by adjusting the output power level. In today's wireless communication systems, the majority of tunable impedance matching networks are realized by solid-state varactors or switching p-i-n diodes. Ferroelectric barium strontium titanate (BST) varactor technology has also been utilized in the realization of tunable matching networks. Using

this technology a better RF linearity can be achieved compared to the solid-state varactors. However, at millimeter-wave frequencies, the increased loss of the matching networks due to the low quality factor of the solid-state devices and BST capacitors becomes an important issue. Another drawback of the solid-state tuning elements is the increased nonlinearity and noise at higher RF power levels.

microelectromechanical systems (MEMS) technology has the capability to provide a major impact on existing communication systems by reducing size, cost, weight and power dissipation. With the use of RF MEMS technology, reconfigurable matching networks with improved impedance tuning range, power handling capability, compact size and lower insertion loss suitable for high-frequency, high-power applications can be realized.

The current MEMS-based adaptive RF front-ends rely on multi-chip solutions where the active circuitry and the MEMS network are put together in a hybrid integration approach. The realization of a fully integrated one-chip solution would be possible by developing a process which enables the integration of the MEMS devices employing the standard processes used for RF integrated circuits (RFICs). Among the mainstream RFIC technologies, silicon-based CMOS processes have become the most favorable technology for the implementation of wireless communication systems due to their mature fabrication process, higher levels of integration and lower manufacturing cost.

1.2 Objectives

The purpose of this thesis is to investigate the feasibility of utilizing MEMS technology to design and implement innovative reconfigurable impedance matching networks with improved impedance coverage and higher power handling capability. Such matching networks would enable a new class of RF front-ends with unprecedented performance, agility and functionality. The realization of this class of networks will be possible due to advances in

the fields of MEMS technology and CMOS-MEMS integration techniques. The stages of this research include:

- **Development, modeling and fabrication of novel MEMS impedance matching networks:** Novel RF MEMS reconfigurable impedance matching networks are developed to meet several requirements such as wide tuning range, lower insertion loss, compact size and higher power handling capability. The first RF MEMS impedance matching network is based on dual-beam RF MEMS capacitive switches with 3 different states. The application of the proposed tri-state switch results in increasing the operational frequency band of the matching network with a wide impedance coverage. The second impedance matching network consists of MEMS series-contact switches and periodic defected-ground-structures (DGSs). The proposed structure achieves an improved insertion loss and power handling capability compared to the traditional RF MEMS impedance matching networks by utilizing MEMS switches placed on the ground planes. Both networks are fabricated using a seven-mask process developed at the University of Waterloo for the fabrication of RF MEMS devices.
- **Development of a novel CMOS-MEMS post-processing and integration technique:** A novel CMOS-MEMS post-processing technique is developed that can be used to integrate tunable RF MEMS devices within a chip fabricated using commercial standard CMOS processes. The MEMS structures are formed out of the metal and dielectric layers available in the CMOS process without any need to extra film deposition or lithographic patterning steps. Using the proposed technique, different types of RF MEMS tunable capacitors with parallel-plate structure and electrostatic actuation have been developed. These capacitors can achieve very high quality factor at millimeter wave frequencies. A tunable microwave band-pass filter with tunable center frequency and bandwidth is also designed and fabricated by

employing the proposed RF MEMS tunable capacitors.

- **Implementation of RF MEMS switches integrated in CMOS technology:** CMOS-MEMS capacitive type switches for microwave and millimeter-wave applications are investigated. The switches are fabricated using the 2P4M (double poly, four metal) TSMC 0.35- μm CMOS process. The mask-less CMOS-MEMS post-processing technique developed for the fabrication of parallel-plate electrostatically actuated microstructures at the University of Waterloo is utilized. An integrated monolithic CMOS implementation of these RF MEMS switches will result in low cost single chip RF multi-band systems with enhanced performance and functionality by eliminating the packaging parasitics present in the hybrid integration approaches.
- **Design and implementation of RF MEMS impedance matching networks using standard CMOS technology:** The integration of MEMS-based reconfigurable impedance matching networks in standard CMOS technologies is investigated. An 8-bit reconfigurable impedance matching network based on the distributed MEMS transmission line (DMTL) concept is presented. The network is fabricated in a standard 0.35- μm CMOS technology and using a CMOS-MEMS integration technique that is optimized for the fabrication of MEMS switched capacitors. The proposed network is optimized using a novel design procedure to improve the impedance coverage of the network on the Smith chart.
- **Development of reconfigurable amplifier using integrated CMOS-MEMS adaptive matching networks:** A reconfigurable amplifier is designed with tunable input and output matching networks which can be tuned to provide matching for variable source and load impedances and to yield an optimum operation of the amplifier. Design issues and circuit simulations for both the MEMS matching network and active circuitry are discussed. The amplifier is implemented using the standard TSMC 0.18- μm CMOS technology and the MEMS adaptive matching network is con-

structured using the proposed CMOS-MEMS integration technique on the same CMOS chip.

1.3 Thesis Outline

Following the motivation and objectives given in Chapter 1, Chapter 2 presents an overview of the different technologies available to realize tunable impedance matching networks with a focus on MEMS technology. Furthermore, the current advances related to the integration of MEMS devices using standard silicon-based CMOS technologies are addressed. In Chapter 3, two types of reconfigurable impedance matching networks that are fabricated using a conventional MEMS fabrication process are investigated. Chapter 4 presents the development of the CMOS-MEMS integration approach. Parallel-plate tunable capacitors with electrostatic actuation integrated on a CMOS chip are presented. The monolithic integration of a tunable band-pass filter with MEMS tunable capacitors as the tuning elements is investigated. A novel capacitive-type RF MEMS switch integrated in CMOS technology is also presented in this chapter. A reconfigurable DMTL impedance matching network utilizing switched MEMS capacitors implemented using standard CMOS technology is introduced in Chapter 5. The integration of tunable lumped-element impedance matching networks with an amplifier module on a single CMOS chip is presented in this chapter. Finally, a brief summary of the contributions of the thesis with an outline of the proposed future research are given in Chapter 6.

Chapter 2

Literature Survey

2.1 Reconfigurable Impedance Matching Networks

Reconfigurable impedance matching networks and impedance tuners are a critical component in many wireless communication systems, specially in multiband applications where there is a need to change the frequency band of operation, the output power level or the antenna patterns. Changing these parameters involves tuning of the impedance matching networks between different building blocks of the system in order to obtain an optimum power transfer and the highest system efficiency. In some other cases, there is an impedance change due to variable ambient conditions. These variations must be compensated for using adaptive impedance matching networks. Over the last few decades, tunable impedance matching networks have been realized using different technologies. With the development of micromachining techniques, tunable matching networks based on MEMS technology have attracted a great deal of interest during the last few years. Based on their tuning mechanisms, most tunable impedance matching networks presented in the literature fall into three basic types: MEMS tuning, electronic tuning, and tuning using ferroelectric materials. Tunable impedance matching networks, based on MEMS technology, are cat-

egorized as a separate category due not only to their multi-discipline tuning mechanism, but also to their potential use in the next generation multiband communication systems.

2.1.1 MEMS Tuning Method

Various MEMS components including tunable MEMS capacitors, MEMS capacitive switches, capacitor banks using MEMS switches, and distributed MEMS transmission line (DMTL), have been implemented in reconfigurable impedance matching networks and impedance tuners. The most straight forward approach to design reconfigurable impedance matching networks by employing MEMS technology is to replace the traditional varactors and inductors with their MEMS counterparts in lumped-element LC-networks. Lumped-element LC matching networks are the easiest to implement. In addition to their simplicity, the use of lumped elements in a lower frequency range results in a more compact circuit compared to distributed-element networks. Fig. 2.1 shows block diagram of an adaptive LC impedance matching module with a 5-bit MEMS capacitor array that can be used to compensate the

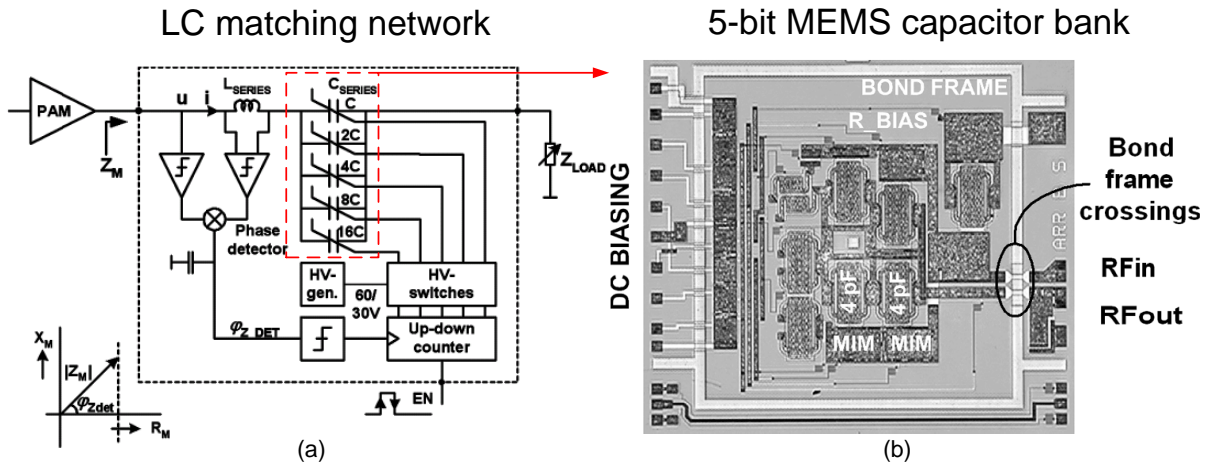


Figure 2.1: (a) Block diagram of an adaptive LC matching network and (b) die photograph of the MEMS capacitor bank [1].

imaginary part of the antenna impedance in a multi-standard mobile phone [1]. The measured MEMS array capacitance tuning ratio is almost a factor of 10. The module shows a maximum impedance correction of $-75j\Omega$ at 900 MHz and the measured insertion loss is approximately 0.5 dB at both low-band (900 MHz) and high-band (1800 MHz).

Impedance tuners using LC resonant unit-cells realized by MEMS tunable capacitors is presented in [2]. Since the capacitance variation of the MEMS capacitors is limited to 30%, resonant unit-cells operating near the resonance frequency are employed to extend the impedance tuning range needed for tuner operation as shown in Fig. 2.2. The large reactance change near the resonant frequency makes it possible to obtain a relatively large impedance variation. The tuner is capable of generating impedances in the second and third quadrants of the Smith chart from 25 GHz to 23.5 GHz with a maximum voltage standing wave ratio (VSWR) of 21.2 at 25 GHz.

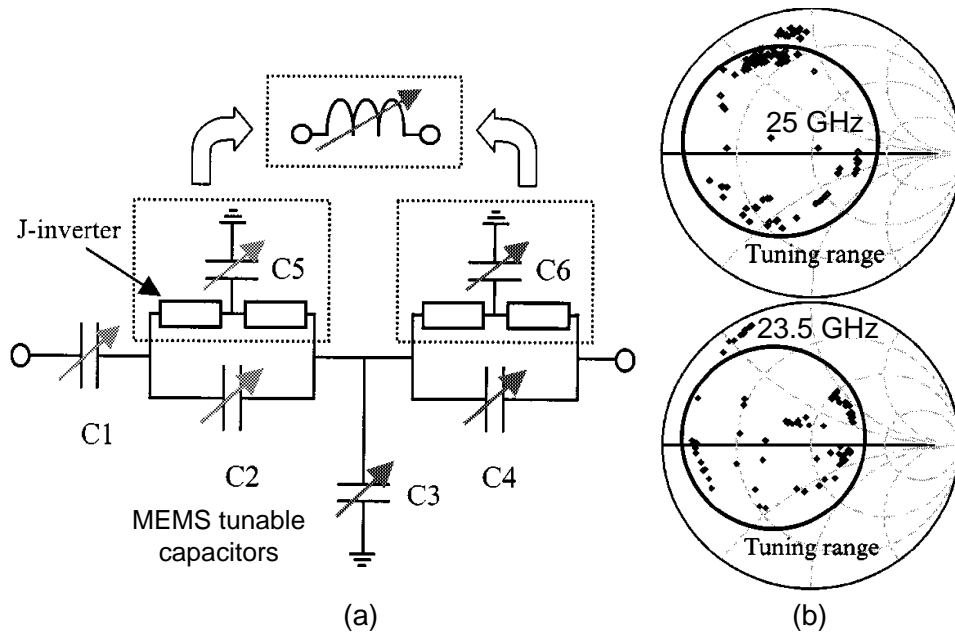


Figure 2.2: (a) Schematic circuit diagram and (b) measured impedance coverage of the analog impedance tuner in [2].

Although the LC-matching networks are easy to fabricate using MEMS devices, they have a narrow operating bandwidth and limited impedance coverage. Another most commonly used impedance matching technique, referred to as stub matching, employs short- or open-circuit transmission lines as stubs where both the effective electrical length and the distance between the stubs can be adjusted using MEMS tuning elements. The digital type impedance tuner in [2] consists of a $\lambda/4$ low-impedance line and two short-circuited stubs each one loaded with 6 MEMS capacitive switches as presented in Fig. 2.3. By actuating the MEMS capacitive switches, the loading capacitance and thus the effective electrical length of the lines are increased, resulting in subsequent impedance tuning. The measured results for this tuner shows an impedance coverage of the second quadrant of the Smith chart from 29-32 GHz with a maximum VSWR of 32.3 measured at 30 GHz. Single-, double- and triple-stub impedance tuners and matching networks using MEMS switches and switched capacitors have been reported by Papapolymerou *et al.* and Heikkila *et al.* [3, 4, 5, 6]. The switched capacitors were distributed at discrete points along the stubs as well as the sections between the stubs. This will generate more impedance points and a better coverage compared to the case where the switched capacitors are present only at

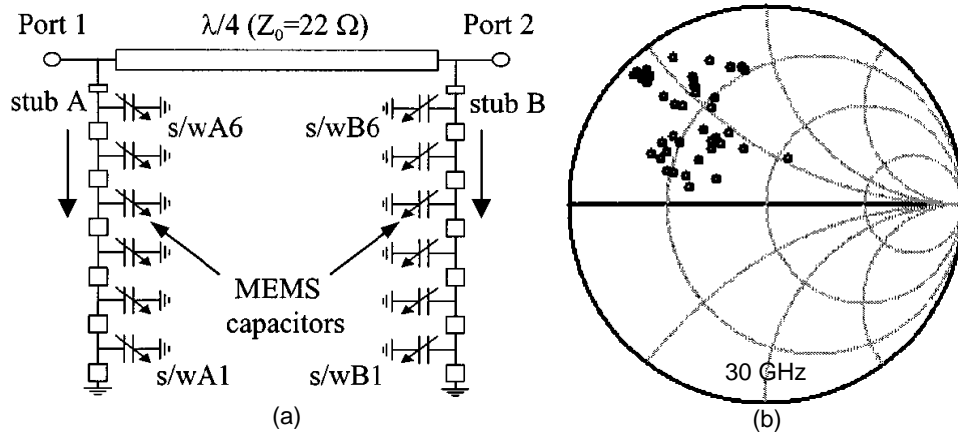


Figure 2.3: (a) Schematic circuit diagram and (b) measured impedance coverage of the digital impedance tuner in [2].

the end of the stubs. Fig. 2.4 illustrates the MEMS single-stub impedance tuner in [4] consisting of 10 switched MEMS capacitors and producing 1024 (2^{10}) different impedance states. Capacitively loaded lines were added before and after the stub in order to improve the impedance coverage and bandwidth. The tuner demonstrated good impedance coverage over a frequency band from 20 GHz to 50 GHz with a maximum VSWR of 32.3 at 40 GHz. Double- and triple-stub MEMS impedance tuners operating at W-band were also reported in [5]. Similar to the single-stub tuner, both the stubs and the connecting transmission lines are loaded and adjusted using switched MEMS capacitors located at discrete points. These tuners achieve a maximum VSWR of 24 at 100 GHz. Other configurations of broadband RF impedance tuners with four and ten stubs loaded with tuning varactors

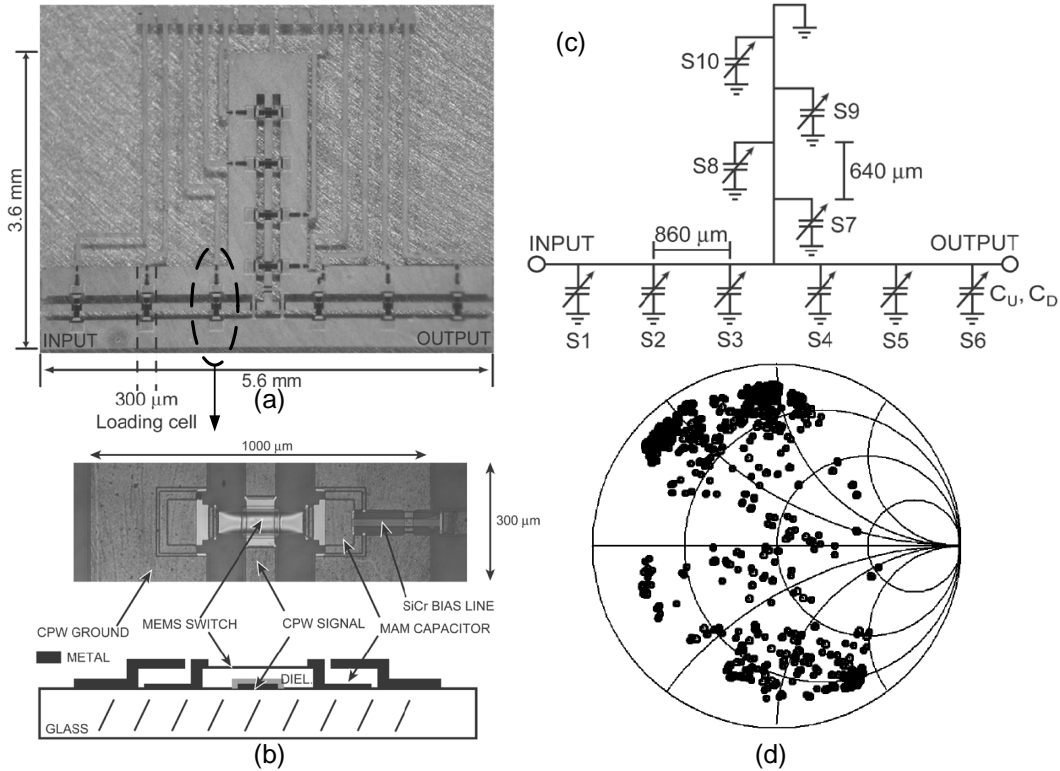


Figure 2.4: Photograph of (a) single-stub impedance tuner and (b) switched MEMS capacitor (c) circuit diagram and (d) impedance coverage at 40 GHz [4].

are presented in [7] and [8], respectively.

Besides the stub matching networks, switched MEMS capacitors can be used in distributed MEMS transmission line (DMTL) structures for impedance matching and tuning applications. Both the effective electrical length and characteristic impedance of such a transmission line is adjusted by switching the MEMS capacitors on and off. The advantage of DMTL networks over stub matching networks is their lower insertion loss and smaller size which makes them suitable for impedance matching applications. Reconfigurable RF MEMS impedance matching networks based on DMTL structure with $N = 4-8$ MEMS switched capacitors are reported by Heikkila *et al.* in [9, 10]. Fig. 2.5 illustrates the photograph and the impedance coverage of the reconfigurable matching network with 8 switched MEMS capacitors. The 8 element matching network produces 256 (2^8) different impedance states and is only $1 \times 2.5 \text{ mm}^2$ in size on a glass substrate. The matching network is capable of matching power amplifiers with $10-20 \Omega$ output impedance to 50Ω system reference impedance over a frequency band from 20 GHz to 50 GHz with an impedance matching

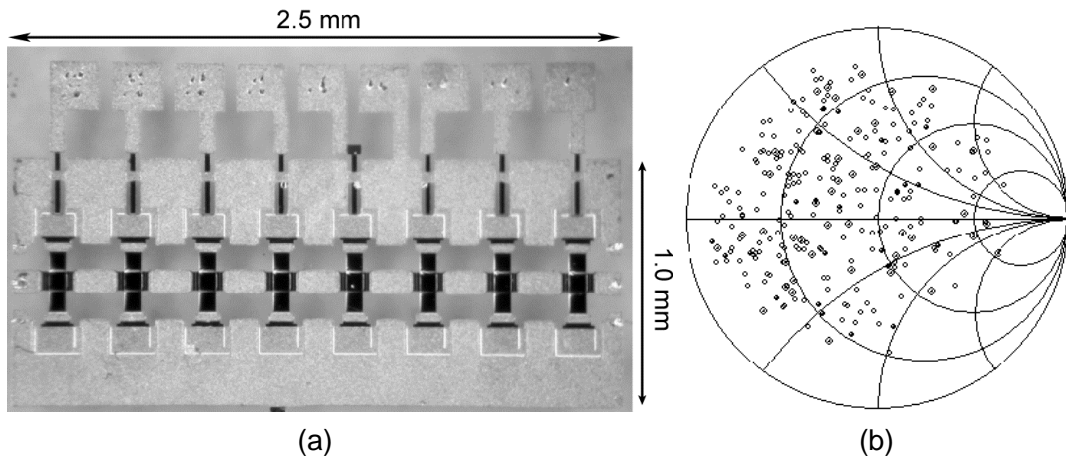


Figure 2.5: (a) Photograph and (b) impedance coverage of the reconfigurable impedance matching network based on DMTL structure with 8 switched MEMS capacitors at 40 GHz [9].

better than 10 dB. The measured insertion loss of the network when used to match a 10Ω load to 50Ω was better than 1.2 dB up to 40 GHz. An impedance tuner based on DMTL structure and optimized for both impedance coverage and power handling was reported in [11, 12]. Novel contact-less MEMS varactors were used instead of the switched MEMS capacitors. These capacitors can handle more than 3.5 W of RF power without self-actuation. The power handling capability of the tuner was further improved by optimum placement of the MEMS varactors along the transmission line so that the maximum voltage swing across all the varactors is equalized. Fig. 2.6 shows a picture and measured impedance coverage of the fabricated impedance tuner on a high-resistivity silicon substrate. The tuner occupies an area of $0.49 \times 0.12 \text{ mm}^2$ and demonstrates wide impedance tuning at 30 GHz.

Double-slug reconfigurable impedance matching networks based on a minimal-contact

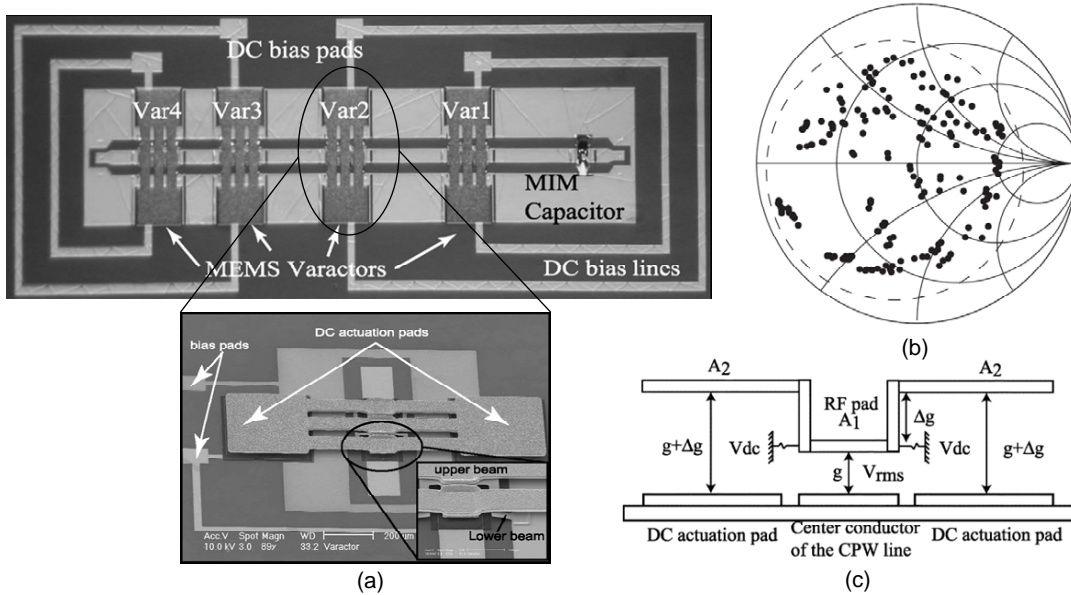


Figure 2.6: (a) SEM of the impedance tuner with high-power MEMS varactors, (b) the measured impedance coverage at 30 GHz, and (c) a cross section of the MEMS varactor [11, 12].

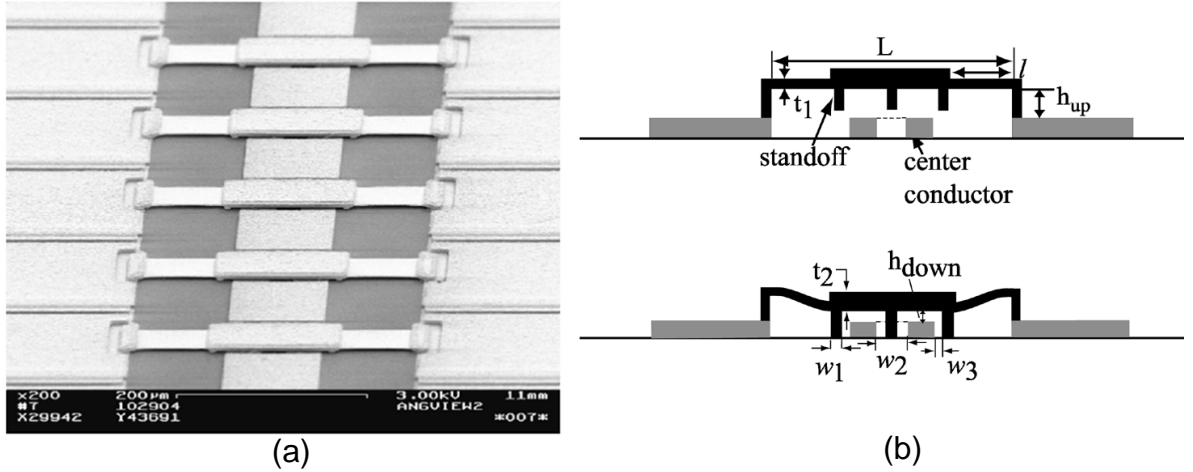


Figure 2.7: (a) SEM and (b) cross-section view of the minimal-contact varactor [13].

RF MEMS varactor was reported by Shen *et al.* [13, 14]. This varactor eliminates the dielectric charging, stiction, and low power handling capability of the conventional switched MEMS capacitors. Fig. 2.7 depicts the cross-sectional view of the minimal-contact varactors. Stand-offs on the bottom side of the bridge were used to limit its range of downward motion and avoid any contact with the signal line similar to the capacitive RF MEMS switches reported by Blondy *et al.* [15]. As shown in the schematic diagram of the double-slug tuner in Fig. 2.8, it consists of two quarter wavelength impedance tuner sections or slugs and two sections of transmission lines with a characteristic impedance Z_o and effective electrical length of Θ_1 and Θ_2 . The electrical length of the 90° slugs is used to tune the frequency of operation while Θ_1 and Θ_2 define the load impedance on the Smith chart that can be matched to the source impedance. The network is designed by loading a high-impedance coplanar waveguide (CPW) line with minimal-contact varactors, each having an individual biasing line. When the switches are in the up-state, the characteristic impedance of the loaded line section is designed to be 50Ω (Z_o) and when the switch is in its down-state position the local CPW line impedance is 25Ω (Z_m), and this section of the line will act as a 90° slug. By actuating a different number of switches, it is possible to

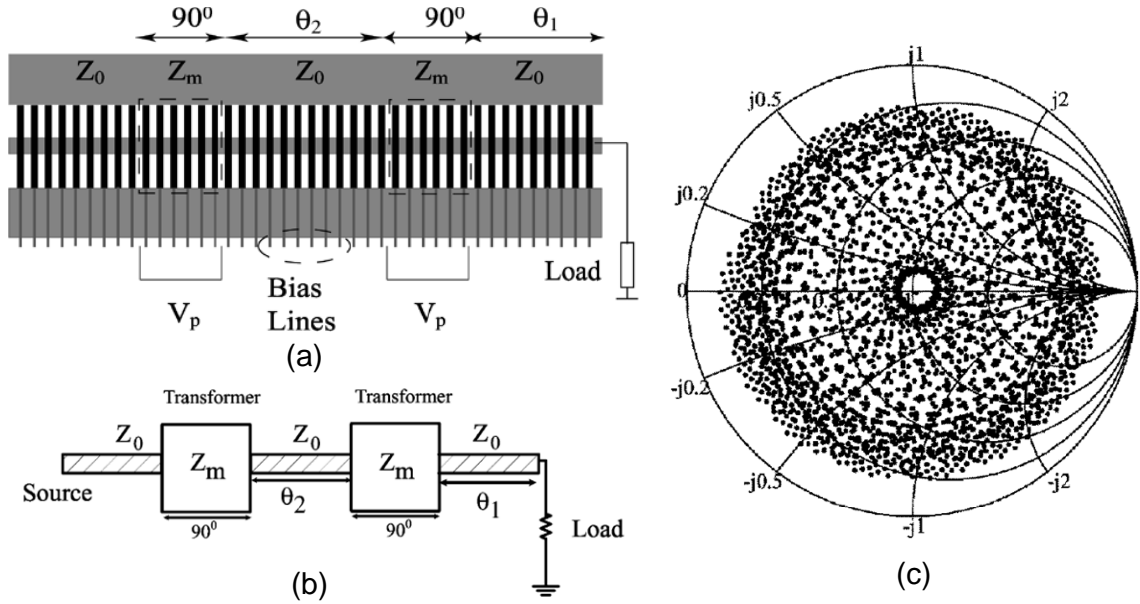


Figure 2.8: (a) Topology and (b) schematic diagram of the double-slug impedance tuner, (c) measured impedance coverage at 27.8 GHz [13].

change the length of the slugs and Θ_1 and Θ_2 . Measurement results demonstrate coverage of all four quadrants of the Smith chart from 10 to 30 GHz with a maximum VSWR of 12 and an insertion loss better than 3 dB.

2.1.2 Electronic Tuning Method

Electronic tuning of impedance matching networks is achieved by employing semiconductor varactors [16, 17, 18, 8] switches [19, 20] and p-i-n diodes [21]. This method offers a fast tuning speed, compact size, low cost and light weight. A reconfigurable impedance tuner in the 380-400 MHz frequency band and based on lumped and electronically tunable elements was reported by Mingo *et al.* [21]. The tuner is used to construct automatic matching system for antenna input impedance. The network is based on the generic low-pass Π matching network implemented using tunable capacitors. Each tunable capacitor consists

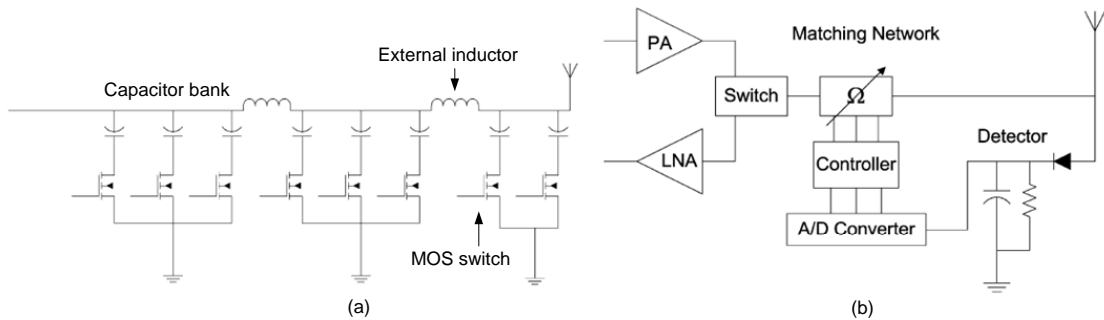


Figure 2.9: (a) Circuit diagram of the impedance tuner for ISM 2.4 GHz band and (b) system block diagram of the antenna tuning unit (ATU) [22].

of a set of fixed value capacitors that are selected by p-i-n diodes.

An adaptive impedance tuning unit implemented in 0.35- μm CMOS technology for the industrial-scientific-medical (ISM) 2.4 GHz band is reported in [22]. The circuit is based on shunt switched capacitor banks and external series inductors crating a ladder network as shown in Fig. 2.9. The switches used are CMOS transistors operating in the triode region. In total, there are 8 switches yielding $2^8=256$ different switch combinations for this impedance tuner. A controller unit can switch the matching network through all possible combinations in order to obtain the best performance to match the antenna input impedance.

Transmission lines loaded with active tuning elements similar to the DMTL structure can also be used as impedance matching and tuning networks. The first electronically reconfigurable impedance tuner for tuning of microwave monolithic integrated circuits (MMICs) was reported by Bishoff *et al.* [18]. The proposed tuner consists of a transmission line loaded with 4 capacitors each in series with a High Electron Mobility Transistor (HEMT) switch monolithically implemented on a GaAs substrate. The proposed tuner was applied to a narrow band amplifier operating at 27 GHz in order to compensate the process deviations. A reconfigurable CMOS tuner based on a transmission line periodi-

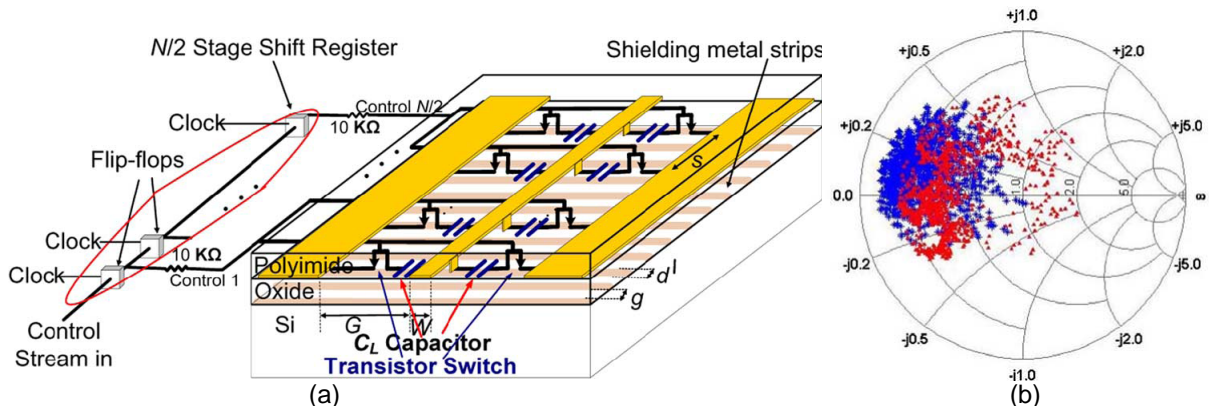


Figure 2.10: (a) Structure of the CMOS tuner based on switched capacitors and (b) measured impedance coverage at 10 GHz for tuners with a transmission line length of 1.6 mm (blue asterisks) and 3.6 mm (red triangles) [23].

cally loaded with CMOS transistor switches in series with capacitors is presented in [23]. The 5 to 16-GHz tuner is implemented in a standard 0.13- μm CMOS technology and can be configured to 2^{20} different impedances by an integrated 20-bit shift register. Although the proposed tuner has a relatively good impedance coverage as shown in Fig. 2.10, the high loss of the tuner impedes its application in high-performance programmable RF and microwave circuits.

2.1.3 Tuning Using Ferroelectric Varactors

The key drawbacks of electronic tuning using semiconductor devices are a relatively large insertion loss and a low power handling capability, which are attributed to the low quality factor and nonlinearity of the semiconductor switches and varactor diodes, respectively. A solution is to use thin-film ferroelectric varactors such as barium strontium titanate (BST) varactors. The capacitance of BST varactors can be varied by changing the dielectric constant of the ferroelectric material with the aid of an external DC bias voltage. BST varactors can be fabricated either in a parallel plate (metal-insulator-metal)

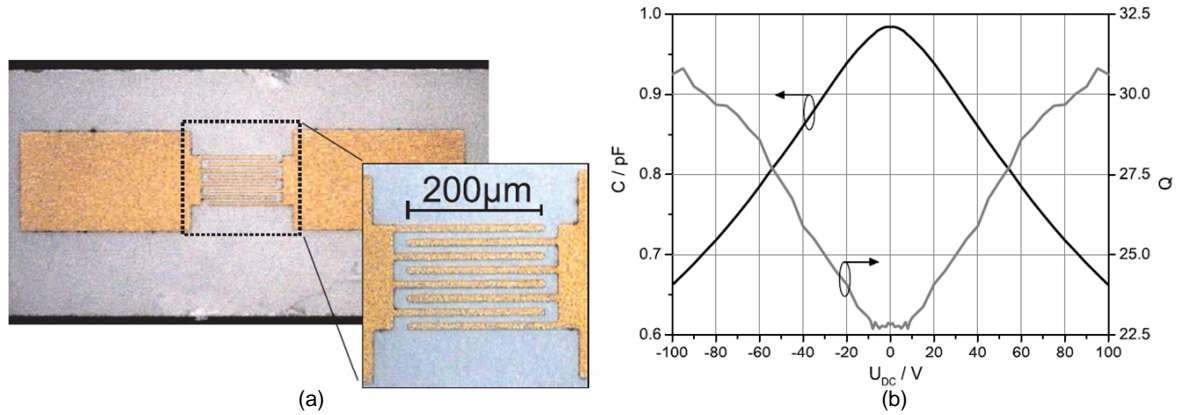


Figure 2.11: (a) A typical interdigitated BST varactor, (b) the measured C-V characteristic and Q -factor at 2 GHz [24].

fashion or an interdigitated configuration. Fig. 2.11 shows a typical interdigitated BST varactor fabricated on alumina (Al_2O_3) substrate and its characteristics at 2 GHz [24]. Typically, tunable impedance matching networks based on BST varactors fabricated on RF substrates, achieve an insertion loss from 0.3 dB to 6 dB with a centre frequency from 850 MHz to 1.95 GHz [25, 24, 26, 27, 28]. The linearity characterization of the impedance matching network in [24], reveals a third-order intercept point (IP3) of 52.8 dBm under the conventional two-tone intermodulation test with a maximum input power of 33 dBm at 1.95 GHz with 1 MHz of offset between the two inputs. Due to the compatibility of the fabrication process of BST varactors with traditional semiconductor processes, the size of the complete tunable impedance matching networks using this technology is near that of semiconductor-based matching networks. One disadvantage is the higher bias voltage used for BST varactors, such as 30 V in [25] and 100 V in [24]. Another drawback is the frequency limitation due to low quality factors beyond 2 GHz.

2.2 Adaptive Amplifiers and Automatic Matching Systems

A compact implementation of adaptive amplifiers and automatic matching systems used in multiband RF front-ends is possible by integrating high efficiency microwave circuits with tunable RF MEMS impedance matching networks and tuners [29, 21, 16, 8, 30, 1]. A reconfigurable amplifier with an adaptive matching network based on RF MEMS shunt capacitive switches was reported by Lu *et al.* [29]. Double-stub tunable input and output impedance matching networks were used to provide matching at two different frequency bands (6 and 8 GHz) for optimum power added efficiency (PAE) and power gain. Fig. 2.12 shows the circuit diagram for the matching networks and the photograph of the fabricated tunable amplifier circuit. A pseudomorphic high electron mobility transistor (pHEMT) was mounted onto the silicon wafer and the matching circuits were connected to the transistor in a hybrid integration fashion. The amplifier demonstrated 7.2 dB gain with 26.4% PAE at 6 GHz and 6.1 dB gain with 16.7% PAE at 8 GHz.

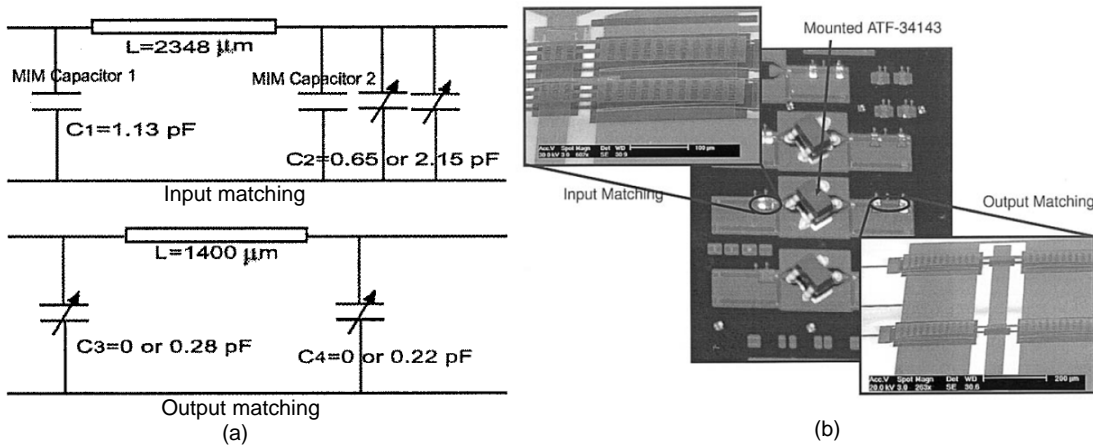


Figure 2.12: (a) Circuit diagram of the double stub matching networks and the photograph of the adaptive amplifier [29].

An intelligent RF power amplifier with a reconfigurable output matching network is reported in [30]. The MEMS output matching network is based on a double-stub topology and consists of 4 MEMS switches, fixed capacitors and a varactor diode. The gain of the amplifier was optimized over a 4-GHz bandwidth at X-band by intelligently switching the MEMS switches and changing the bias voltage of the varactor. Each MEMS switch provides a capacitance ratio of 43:1 and can be used to tune the load impedance in a discrete manner with a total of 16 (2^4) different states. For each state, the output impedance can also be fine tuned using the varactor diode. Fig. 2.13 shows the block diagram of the intelligent power amplifier consisting of GaAs pHEMT transistors, narrow-band filters used as the input matching, A/D converters, power sensors, and the MEMS output matching network. The system was fabricated in a hybrid configuration. Using intelligent control algorithms, the output power was maintained close to an optimum value for the frequency band from 7-11 GHz while the input power varied from 10 to 21 dBm. The system can also detect malfunctioning MEMS switches and reconfigure itself for this situation.

The adaptive multiband multimode power amplifier (PA) in [16] is continuously tunable

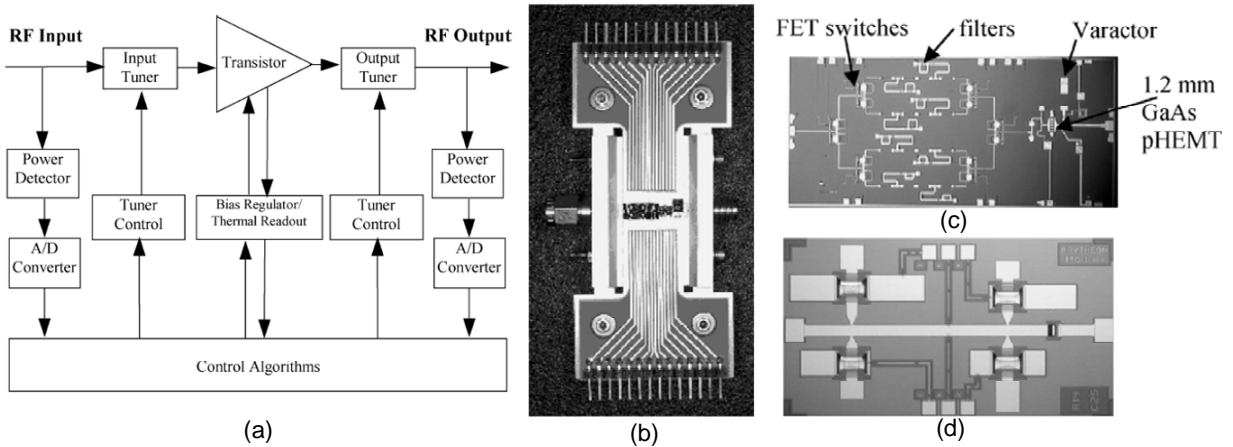


Figure 2.13: (a) Block diagram of the intelligent power amplifier, (b) picture of the overall system, (c) transistors and active circuitry (d) output MEMS matching network [30].

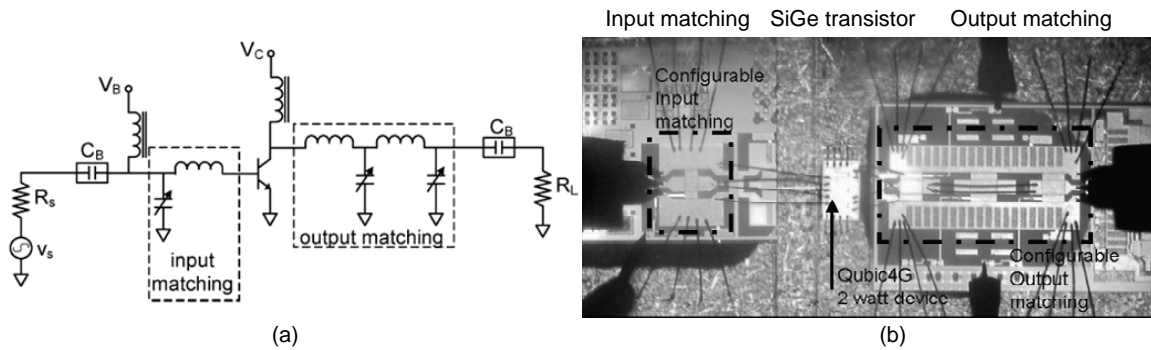


Figure 2.14: (a) Block diagram and (b) microphotograph of the multiband power amplifier in [16].

in operating frequency and output power level. The amplifier utilizes reconfigurable input and output impedance matching networks based on high- Q varactors ($Q > 100$ at 2 GHz) and a SiGe transistor as active device. It demonstrates an output power of 27-28 dBm at the 900, 1800, 1900, and 2100 MHz bands with reasonable efficiencies. Fig. 2.14 shows a microphotograph of the final implemented PA module where the active device and the matching networks are put together in a hybrid integration approach.

Reconfigurable impedance matching networks are also employed in intelligent automatic impedance matching systems that can be used for a wide variety of wireless applications such as antenna matching [21, 8]. Although good results in terms of band switching, efficiency and power control range, have been achieved for the adaptive amplifiers and automatic matching systems described in this section, there is still significant room for improvements at the technology level and integration of the active circuitry with the tunable matching networks. Consequently, even higher performance can be obtained for the future fully-integrated implementations.

2.3 Integrated CMOS-MEMS Devices

There has been an intensive research on RF-MEMS and RF-CMOS technologies in order to develop multiband RF transceivers. A single-chip implementation of these multiband RF transceivers will be possible by fusion of these two technologies. From this perspective, several researchers have studied the integration of MEMS devices with standard CMOS technologies. The main advantage of this integration process will be the low-cost fabrication of MEMS-based RF transceivers using a standard CMOS process and easy and rapid transfer to industry.

A low-temperature (below 310°C) CMOS-compatible fabrication process for the RF CMOS-MEMS switches is presented in [31]. The process features multilevel gold layers and formation of a capsule sealing the MEMS devices to ensure their stable operation, as depicted in Fig. 2.15. A single-pole 8-through (SP8T) contact-type RF MEMS switch stacked on a CMOS chip is fabricated using the proposed process. The switch is controlled directly by the underlying CMOS control circuitry operating at 3.3 V CMOS

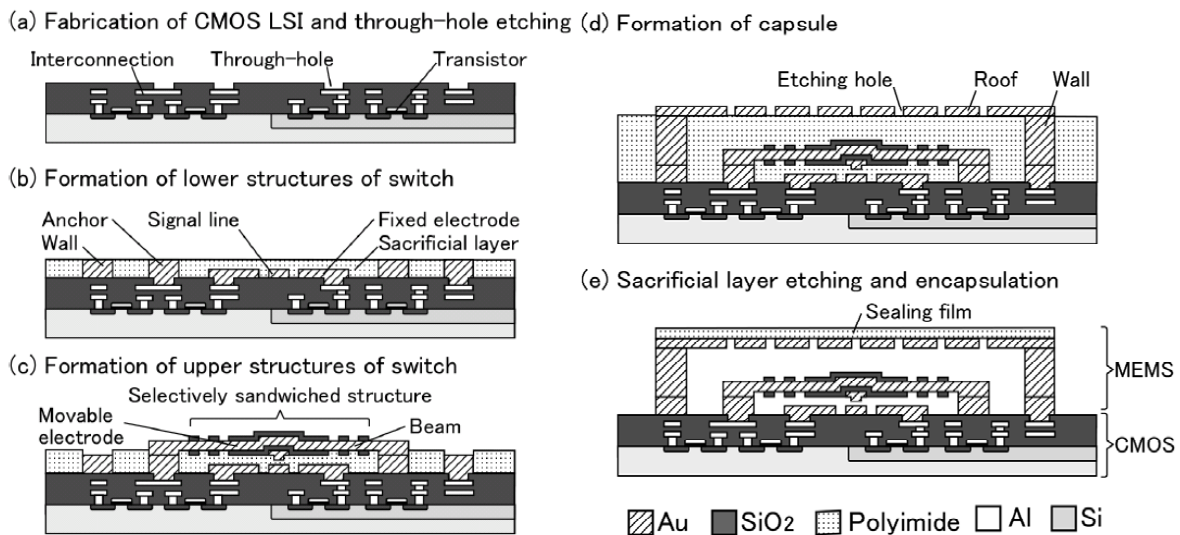


Figure 2.15: Process flow for the CMOS-compatible MEMS process in [31].

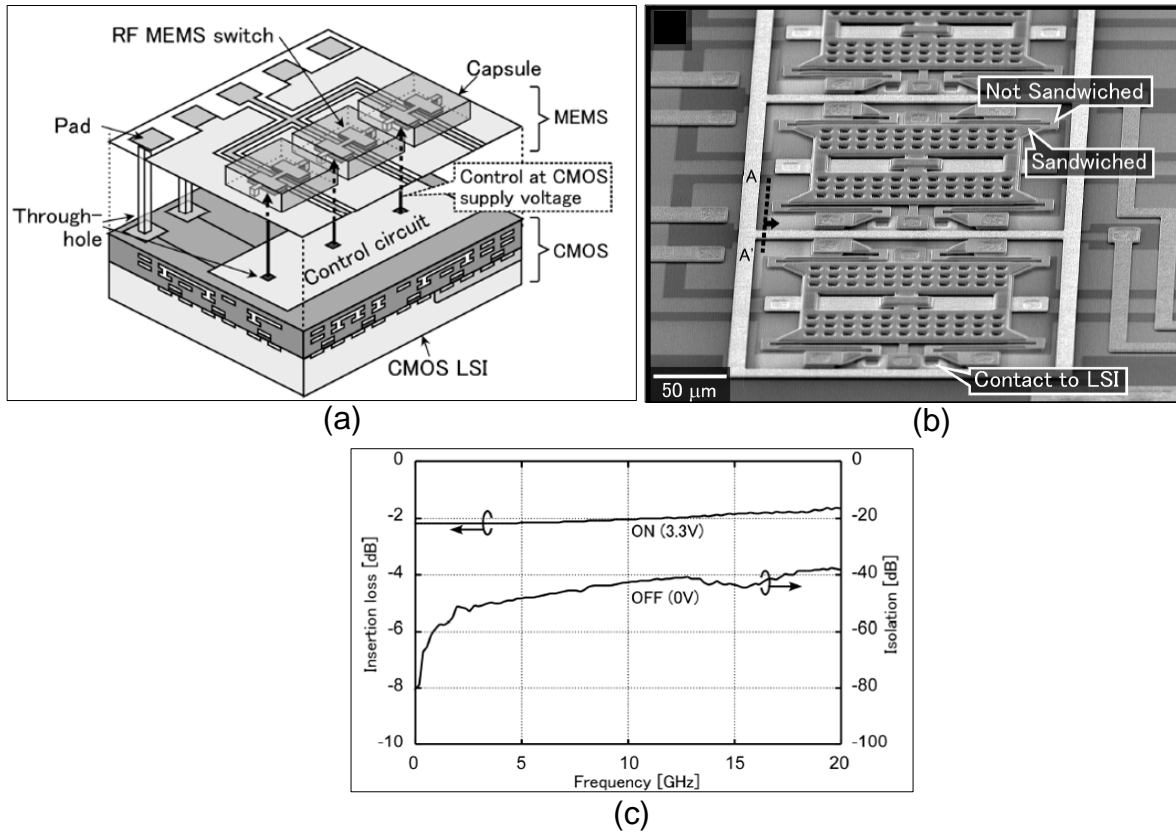


Figure 2.16: (a) Schematic view, (b) SEM image and (c) measured S-parameters of the CMOS-MEMS switch [31].

supply voltage. The switch offers single-chip integration capability and an RF performance higher than that of conventional p-i-n diode and transistor switches. Fig. 2.16 shows the schematic diagram and SEM image of the switch implemented on a 0.6- μm CMOS chip, which contains a 3-bit address decoder circuit and an IO circuit for switch actuation. The switch is actuated by a 3.3 V DC external voltage source. The insertion loss and the isolation of the switch are 2 dB and higher than 40 dB from DC to 10 GHz, respectively, as shown in Fig. 2.16(c).

A CMOS-MEMS processing for the fabrication of electrostatically actuated microstructures with lateral motion was pioneered by Fedder *et al.* at Carnegie Mellon University

(CMU) [32]. The proposed process consists of a sequence of maskless dry etching steps as depicted in Fig. 2.17. The processing starts with a CMOS chip fabricated using a standard CMOS technology. Then one or multiples of CMOS metallization layers is used as an etch resistant mask to define the microstructures. The microstructures are released by removing the CMOS dielectric layer and the silicon substrate underneath using dry etching steps. Several RF-MEMS devices including high- Q micromachined inductors [33], RF-MEMS tunable capacitors [34, 35] and micromechanical resonators [36, 37] have been fabricated using this process.

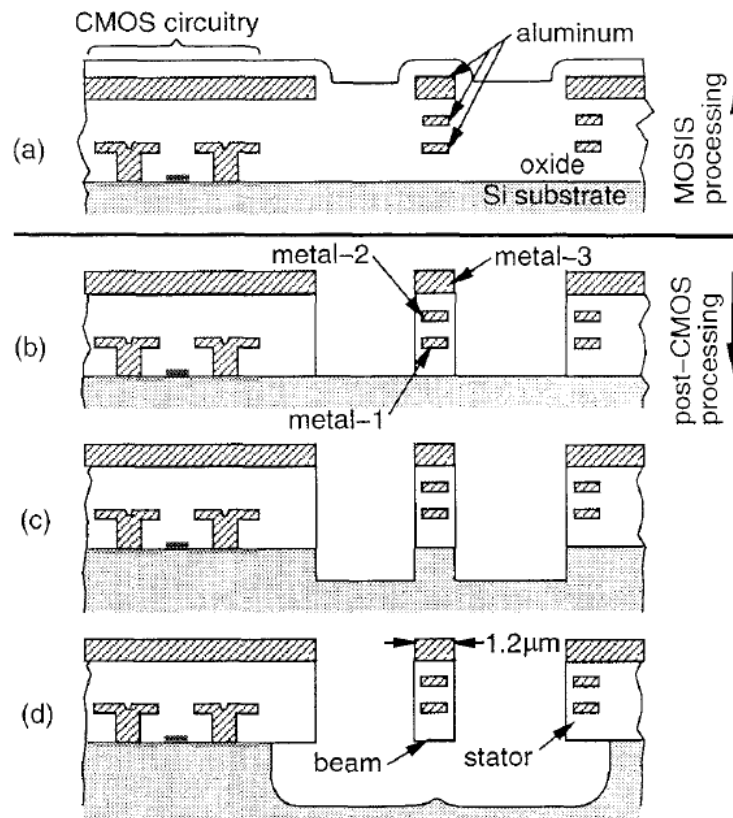


Figure 2.17: Process flow for CMOS-MEMS processing at CMU (a) before applying the processing (b) after anisotropic oxide etching (c) after anisotropic silicon etching and (d) after isotropic etching of the silicon substrate and release [32].

A CMOS-MEMS variable capacitor with a tuning ratio of 6.9:1, a Q -factor of 28 at 3 GHz, and a self-resonant frequency of 11 GHz is reported in [35]. The capacitor was fabricated in a standard 0.35- μm BiCMOS and micro-machined using the CMU CMOS-MEMS processing. The capacitor consists of two sets of interdigitated capacitance beams; one fixed and the other is movable as shown in Fig. 2.18. Electrothermal actuators are used to control the lateral (in-plane) gap, and hence capacitance of the device. A mechanical latching mechanism is also utilized to hold the movable beams at six different positions without consuming DC power.

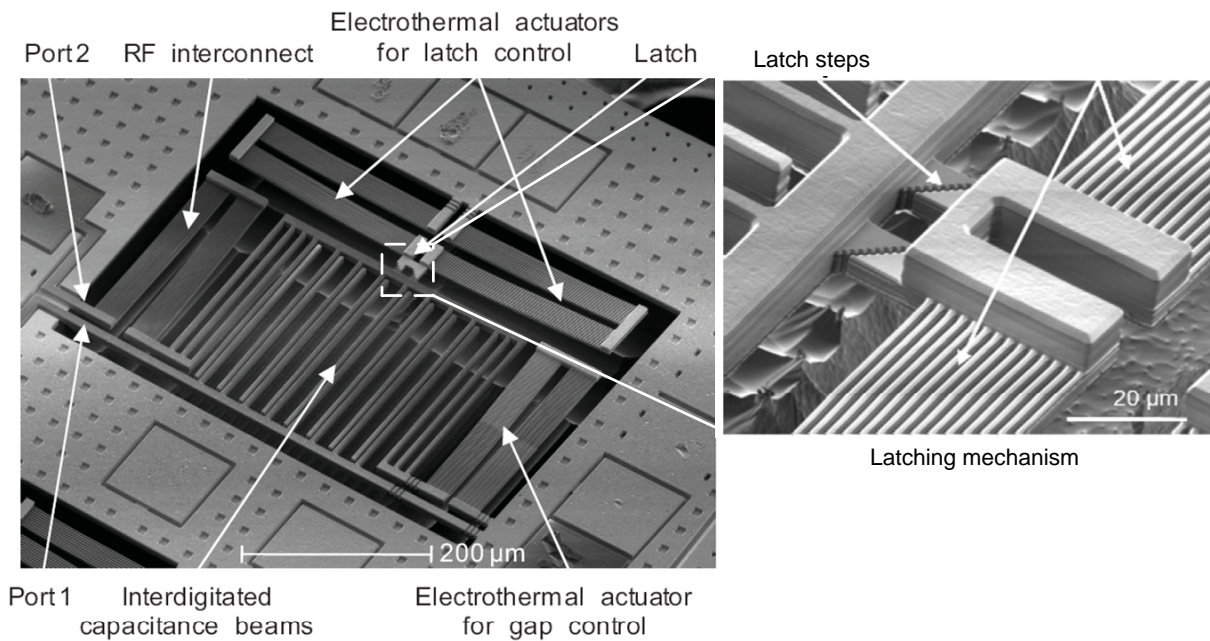


Figure 2.18: SEM image of the CMOS-MEMS tunable capacitor [35].

CMOS-MEMS tunable filters are reported in [38] using CMOS-MEMS tunable capacitors and micromachined inductors implemented by the CMU CMOS-MEMS processing. Fig. 2.19 shows the SEM image and the S-parameters of the tunable bandpass filter fabricated using foundry Jazz Semiconductor 0.35- μm BiCMOS process. The tuning range of the filter is from 1.67 GHz to 2.13 GHz (24%). The measured insertion loss varies from

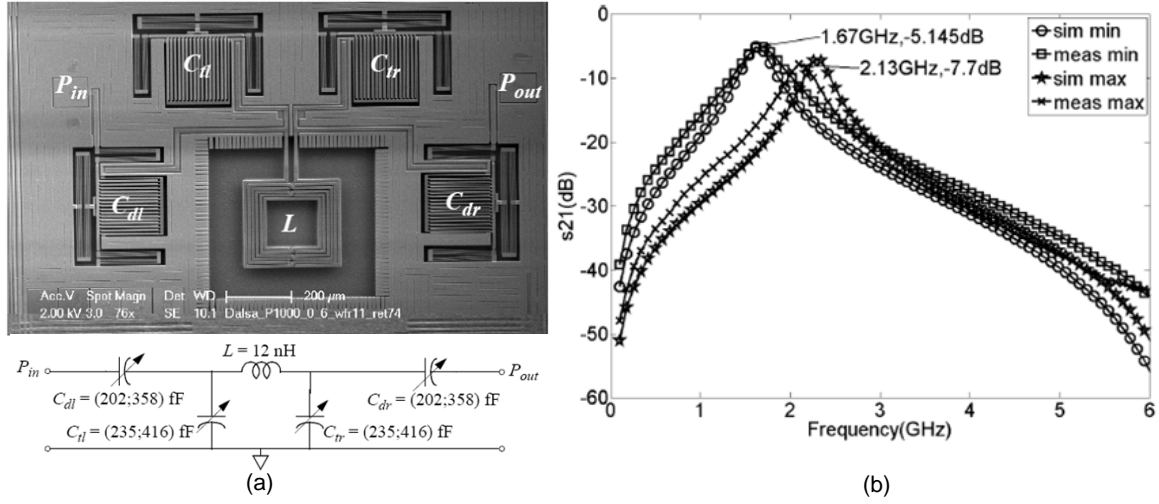


Figure 2.19: (a) SEM image and circuit diagram of the tunable bandpass filter (b) S-parameters [38].

5.1 dB to 7.7 dB and the measured filter bandwidth is 450 MHz ($Q = 3.7$) and 350 MHz ($Q = 6$) across the tuning range.

Micromechanical resonators, filters, and mixers were also made by micromachining composite metal and dielectric interconnect layers within foundry CMOS processes [37, 39, 40]. Fig. 2.20(a) shows a cantilever beam CMOS-MEMS resonator. The measured response at 10 mTorr vacuum shows that the cantilever has a primary resonance at $f_o = 435$ kHz with a Q around 1400. Mixing at RF frequencies can be achieved using the proposed micromechanical resonator over a wide local oscillator (LO) frequency range from 10 MHz to 3.2 GHz. A differential square frame resonator operating at 6.184 MHz and 17.63 MHz for the fundamental and 2nd harmonic modes, respectively fabricated using CMOS-MEMS technology is also presented in Fig. 2.20(b). The resonator exhibits a quality factor of 996 in vacuum at the fundamental resonant frequency.

An RF-MEMS capacitive-type switch integrated in CMOS was reported by Zhang *et al.* [41]. The switch consists of two sets of interdigitated beams for capacitive coupling between

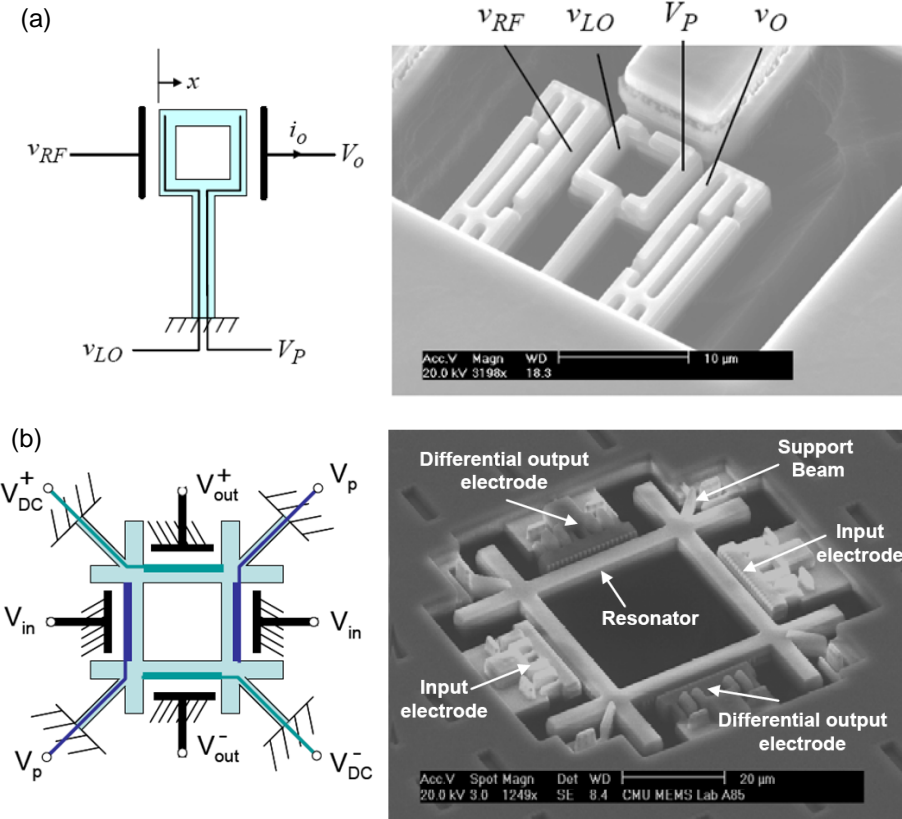


Figure 2.20: (a) Cantilever micromechanical resonator and (b) square frame resonators fabricated by CMOS-MEMS technology [37, 39].

the RF ports in a CPW configuration as shown in Fig. 2.21. A thermal actuator with polysilicon heater is used for switch actuation. The switch is integrated in a commercial CMOS AMI 0.6- μm process using a CMOS-MEMS processing similar to CMU’s process. Measurement results reveal an insertion loss of 1.6 dB and an isolation of 33 dB at 5.4 GHz as shown in Fig. 2.21(c). However, the size of the switch is too big due to the interdigitated beam structure, also the use of thermal actuators results in high DC power consumption if a suitable latching mechanism is not utilized for the proposed switch.

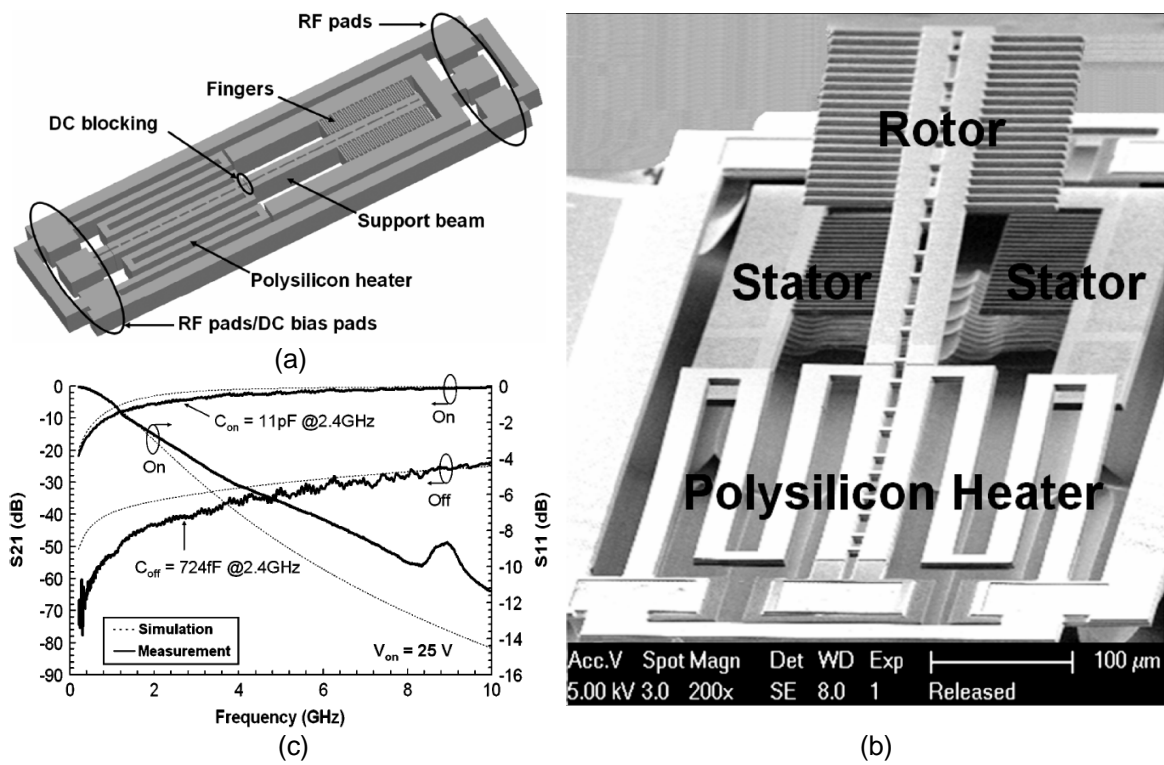


Figure 2.21: (a) 3-D view, (b) SEM image and (c) S-parameters of the CMOS RF MEMS switch [41].

Chapter 3

RF MEMS Tunable Impedance Matching Networks

3.1 Introduction

Intelligent RF front-ends with multi-band functionality that can support different wireless standards have an important role in communication systems. In these systems, there is often an impedance mismatch between the different building blocks such as the antenna and the power amplifier due to the operation in different frequency bands or due to the varying operational conditions. A tunable impedance matching network with a wide impedance coverage, bandwidth and low insertion loss is required within these RF front-ends to ensure an optimum power transfer between the blocks and to increase the battery life time. In addition to tunable impedance matching in multi-band RF front-ends, reconfigurable matching networks capable of producing a multitude of impedance points are necessary for use in characterization of active semiconductor devices such as load-pull and noise parameter measurement setups [5]. In this case the matching network is used as an impedance tuner to manipulate the impedance conditions under which the device under test (DUT)

or transistor is tested.

A number of reconfigurable impedance matching networks and impedance tuners have been demonstrated using solid-state tuning elements at lower frequencies up to 2.4 GHz [21, 16, 42, 43, 44]. Ferroelectric materials such as barium strontium titanate (BST) varactor technology has also been utilized in the realization of tunable impedance matching networks [28, 25, 45]. Using BST varactors a better RF linearity can be achieved compared to the solid-state varactors. At higher millimeter-wave frequencies, the increased loss of the matching networks due to the low quality factor of the solid-state varactors and BST capacitors becomes an important issue. Another drawback of the solid-state tuning elements is the increased nonlinearity and noise at higher RF power levels. Recently, reconfigurable impedance matching networks based on MEMS technology have been successfully demonstrated, e.g., [6, 9, 12, 13]. MEMS-based impedance matching networks are compact and electronically tunable, providing lower insertion loss, lower power consumption and higher linearity compared to the solid-state and BST varactors. Although the previously reported RF MEMS tuners have achieved wide impedance coverage and can handle relatively high RF power levels, still they have a limited performance in terms of power handling capability due to the use of MEMS capacitive bridges or switched capacitors on the signal line which suffer from self-actuation under high RF power levels. Additionally, the insertion loss of these networks deteriorates when a large number of tuning elements are used to achieve wider impedance coverage.

In this chapter, new types of RF MEMS impedance matching networks are presented. The first type of RF-MEMS distributed matching network is based on dual-beam MEMS switches which achieves an extended frequency band of operation. In order to increase the operating frequency range while reducing the total size of the network, a tri-state MEMS switch is employed along with a slow-wave structure. A second type of RF MEMS impedance matching network is presented that employs periodic defected-ground-

structures (DGSs). Unlike the conventional MEMS matching networks, the proposed structure employs MEMS series-contact type switches on the coplanar waveguide (CPW) ground planes which do not suffer from self-actuation. Furthermore, the insertion loss of the tuner is only limited by the loss of the transmission line and not the number of MEMS switches used for the maximum impedance coverage. Both types of the impedance matching networks are fabricated using the UW-MEMS process developed at the University of Waterloo in the CIRFE lab. The experimental results demonstrate the improved impedance coverage, loss and power handling capability compared to the conventional RF MEMS impedance matching networks.

3.2 Impedance Matching Network Using Dual-Beam MEMS Switches

In this section a reconfigurable impedance matching network using dual-beam MEMS switches is presented. The use of dual-beam MEMS switches with 3 separate states compared to the conventional MEMS switches with only 2 states, improves the maximum operating frequency of the matching network. A slow-wave structure is also applied in order to reduce the total size of the network.

3.2.1 Design and Analysis

One of the well known methods used to construct reconfigurable impedance matching networks using MEMS technology is the Distributed MEMS Transmission Line (DMTL) method. The DMTL structure consists of a transmission line with a high characteristic impedance (Z_o) which is periodically loaded with capacitive MEMS switches as shown in Fig. 3.1. This method have been previously applied to MEMS phase shifters [46], tunable

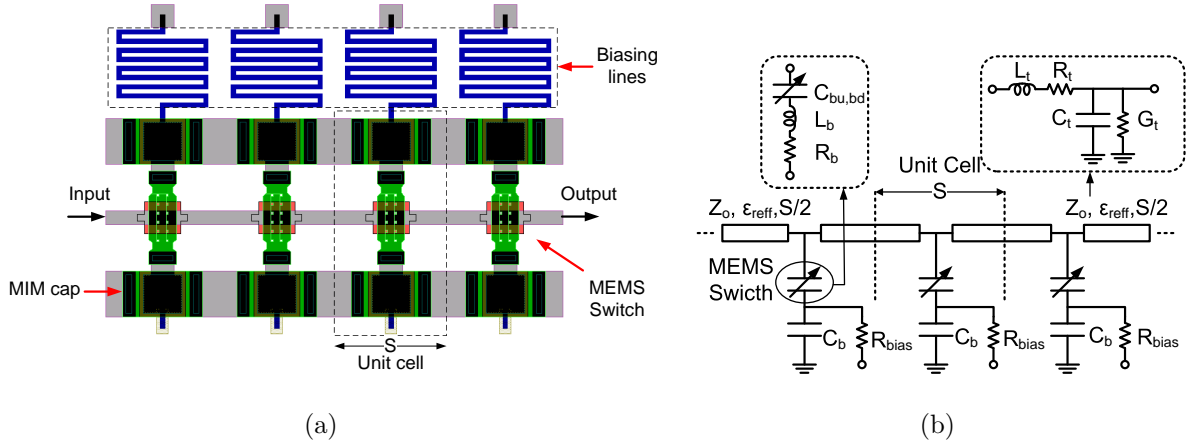


Figure 3.1: (a) Schematic view of the conventional DMTL structure with MEMS switches and (b) equivalent circuit diagram.

filters [47], [48], impedance matching networks [13], [49] and impedance tuners [6].

Fig. 3.1 shows the lumped-element equivalent circuit diagram of the DMTL structure. The local characteristic impedance and the effective dielectric constant of the transmission line loaded with MEMS switches depend on the state of the switch, up- or down-state, according to the DMTL equations in [50].

$$\begin{aligned}
 Z_{u,d} &= Z_o / \sqrt{K} \\
 \epsilon_{ref-u,d} &= \epsilon_{ref} K \\
 K &= 1 + \frac{c Z_o C_{bu,bd}}{S \sqrt{\epsilon_{ref}}} \quad (3.1)
 \end{aligned}$$

where, Z_o and ϵ_{ref} are the characteristic impedance and the effective dielectric constant of the unloaded line, respectively, c is the speed of light, S is the spacing between two consecutive MEMS switches, C_{bu} and C_{bd} are the capacitance of the MEMS switch in the up-state and down-state positions, respectively. The objective is to change both the characteristic impedance and effective dielectric constant of the transmission line by switching the MEMS switches 'on' and 'off'. A DMTL structure with N MEMS switches can achieve 2^N different states by individually actuating each MEMS switch. When the DMTL struc-

ture is used as an impedance matching network, each state of the network corresponds to a load impedance at the output port that can be matched to the source impedance present at the input port. The design goal is to uniformly distribute all these impedance matched points on the Smith chart in order to obtain a wide impedance coverage using the designed DMTL network.

For the uniformity of the Smith chart coverage we have used a uniformity factor, χ^2 , introduced in [51]

$$\chi^2 = \sum_{i=1}^{N_i} \sum_{j=1}^{N_j} \frac{(N(i, j) - \frac{N_{total}}{N_i N_j})^2}{\frac{N_{total}}{N_i N_j}} \quad (3.2)$$

where $N_i \times N_j$ is the number of pie shaped sub-sections dividing the Γ -plane and $N(i, j)$ is the number of impedance matched points inside each sub-section, as shown in Fig. 3.2.

A conventional DMTL matching network is optimized in terms of the uniformity of the Smith chart coverage and by using the design methodology reported in [51] through the proper choice of the design parameters for the unit cell shown in Fig. 3.1. Assuming the characteristic impedance of the loaded line when all the switches are in their up-state position is $Z_u = Z_{ref}$, where $Z_{ref} = 50 \Omega$ is the system reference impedance, there are three main design parameters that can be used to optimize the performance of the network. The

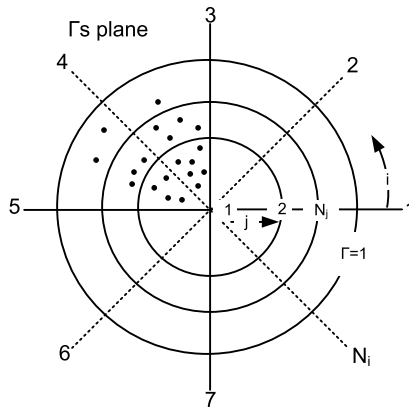


Figure 3.2: Pie shaped sub-sections used to estimate the uniformity factor.

design parameters are: (i) the characteristic impedance of the unloaded line (Z_o), (ii) the electrical length of each DMTL unit cell ($\Phi_{u,d}$) obtained for each state of the MEMS switch using (3.6) and (iii) the down-state MEMS switch capacitance (C_{bd}) or equivalently the capacitance ratio $C_r = C_{bd}/C_{bu}$. All the other parameters of the unit cell are related to these three as follows:

$$Z_u = Z_{ref}, Z_d = \frac{Z_{ref}Z_o}{\sqrt{Z_o^2C_r - Z_{ref}^2(C_r - 1)}} \quad (3.3)$$

$$\varepsilon_{reff-u} = \varepsilon_{reff} \frac{Z_o^2}{Z_{ref}^2} \quad (3.4)$$

$$\varepsilon_{reff-d} = \frac{\varepsilon_{reff}}{Z_{ref}^2} (Z_o^2C_r - Z_{ref}^2(C_r - 1)) \quad (3.5)$$

$$\Phi_{u,d} = \frac{360^\circ S}{c} f \sqrt{\varepsilon_{reff-u,d}} \quad (3.6)$$

The minimum required total electrical length of the network in the up-state position $N \times \Phi_u$ is set by the frequency band of operation. As given in (3.6), the physical length of the unit cell S and consequently the total size of the network is minimized by increasing ε_{reff-u} which is a function of both Z_o and ε_{reff} . ε_{reff} can be increased by utilizing slow-wave structures as will be explained later, but there is a maximum limit for Z_o which is set by the required uniformity of the impedance coverage. To improve the impedance coverage of the network, the down-state characteristic impedance of the loaded line Z_d needs to be lowered while the electrical length of the cell in the down-state position Φ_d must be increased. Hence, for a specific frequency band, in order to achieve a wide impedance coverage while maintaining the total size of the network as small as possible, a proper value of Z_o is selected and ε_{reff-u} is maximized through the proper choice of the dimensions of the MEMS switch and also the geometries of the slow-wave transmission line.

When the proposed optimization technique is applied to conventional DMTL matching network with 2-state MEMS switches, the maximum operating frequency is extremely reduced due to the increased effective electrical length of the unit cell and reduced down-state

characteristic impedance. To decrease the minimum operating frequency while maintaining a maximum operating frequency, the DMTL unit cell should present additional states with a smaller electrical length properly selected for the maximum frequency of operation.

The basic idea here is to use a tri-state capacitive MEMS switch with two cantilever beams along with a slow-wave CPW transmission line as shown in Fig. 3.3. Using the slow-wave structure, the impedance matching coverage is improved at lower frequencies while reducing the total size of the network. In addition, the tri-state MEMS switch presents three different capacitance values in order to have an improved impedance coverage over a wider frequency range. The first state of the MEMS switch when both beams are in the up-state position presents the capacitance value, $C_{b,1}$, required to have a loaded characteristic impedance, $Z_{DMTL,1}$, around the 50Ω reference impedance, Z_{ref} . For the second state, when only one of the cantilever beams is actuated to the down-state, an intermediate capacitance value, $C_{b,2}$, is achieved which accommodates a wide impedance coverage for the higher frequency band of operation while the third state, with both beams actuated, provides a high down-state capacitance value, $C_{b,3}$, necessary for the lower band of the

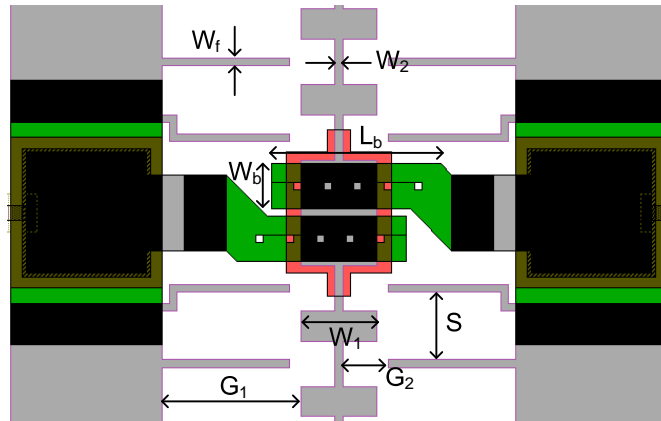


Figure 3.3: Layout of the proposed unit cell, $G_1=185\mu\text{m}$, $G_2=60\mu\text{m}$, $W_1=100\mu\text{m}$, $W_2=10\mu\text{m}$, $W_f=10\mu\text{m}$, $S=90\mu\text{m}$, $w_b=60\mu\text{m}$, $L_b=240\mu\text{m}$.

frequency range of operation.

The designed slow-wave transmission line on a 25 mil alumina substrate ($\epsilon_r = 9.8$) has an unloaded characteristic impedance of $Z_o = 65 \Omega$ and an effective dielectric constant of $\epsilon_{reff} = 14.5$. The network consists of 8 tri-state MEMS switches and the spacing between each consecutive switch is selected to be 500 μm . The dimensions of the switch are selected to obtain the design parameters listed in Table 3.1.

Table 3.1: tri-state MEMS switch and DMTL line parameters

Symbol	Parameter	Value
C_b ($1^{st}/2^{nd}/3^{rd}$)	capacitance (fF)	48/180/328
Z_{DMTL} ($1^{st}/2^{nd}/3^{rd}$)	characteristic impedance (Ω)	50/40/30
ϵ_{reff} ($1^{st}/2^{nd}/3^{rd}$)	effective dielectric constant	23/40/60

3.2.2 Fabrication Process

The impedance matching network is fabricated at the University of Waterloo using the UW-MEMS seven-mask process [52]. Fig. 3.4 shows the processing steps. First, a 70 nm layer of Cr deposited on a 25 mil alumina substrate and patterned to form the biasing lines. Then, a 0.5 μm thick layer of oxide is deposited and patterned to cover the biasing lines followed by the deposition of a 40/50 nm seed layer of evaporated Cr/Au layer. Then the first gold layer was electroplated to a thickness of 1.5 μm . Next, a 30 nm Cr adhesion layer and a 0.5 μm PECVD silicon oxide layer were deposited and dry-etched in a reactive ion etching (RIE) chamber in the forth photolithography step. This oxide layer is used as the capacitive switch dielectric layer. Subsequently, the 2.5 μm polyimide sacrificial layer was spin-coated and baked. The fifth mask was then used to create the anchors by RIE

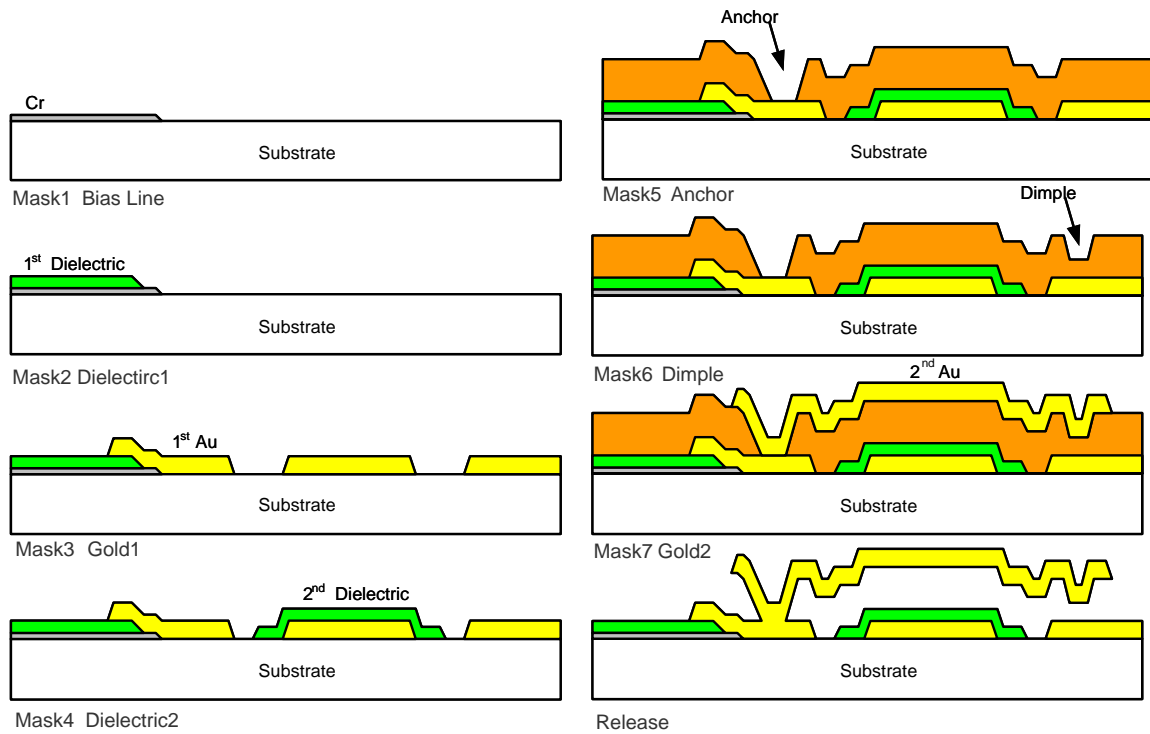


Figure 3.4: UW-MEMS fabrication process steps.

etching employing a thin aluminum masking layer. The sixth mask was used to partially etch the polyimide in order to make the dimples (not used in this design). During the

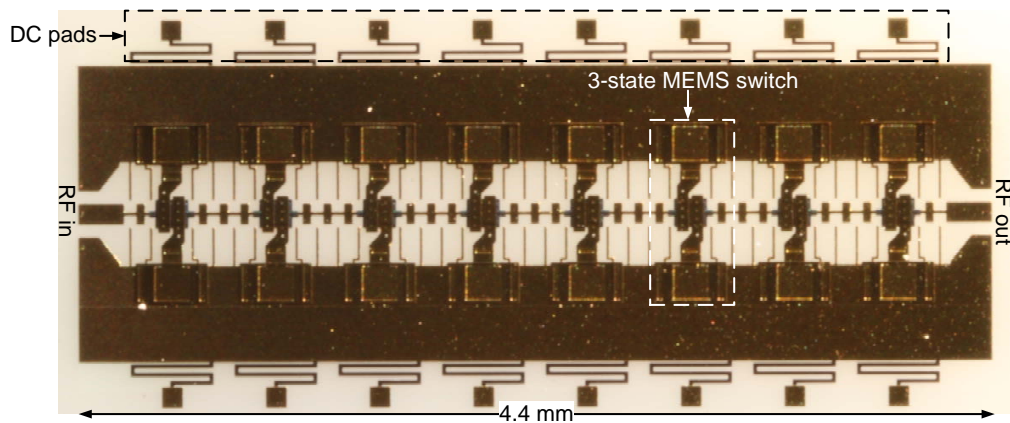


Figure 3.5: Photograph of the fabricated impedance matching network.

next step, the structural layers were formed using a 1.25 μm thick electroplated gold on a 100 nm Au seed layer. Finally, the devices were released in an oxygen plasma. Fig. 3.5 shows a picture of the fabricated slow-wave DMTL network measuring 4.4 mm long. A close-up SEM image of the dual-beam MEMS switches is shown in Fig. 3.6.

3.2.3 Experimental Results

The S-parameters of the fabricated network is measured for a number of different states of the MEMS switches and compared with the simulation results. The RF measurements were performed on-wafer using a vector network analyzer with SOLT calibration. The DC actuation voltage of the MEMS switches is measured to be $V_{pi} = 45$ Volts. As seen in Fig. 3.7 there is a good agreement between the simulated and measured S-parameters for both states; when all the MEMS switches are in their up-state position and when all the switches are actuated to the down state position. The measured S-parameters are fitted to the

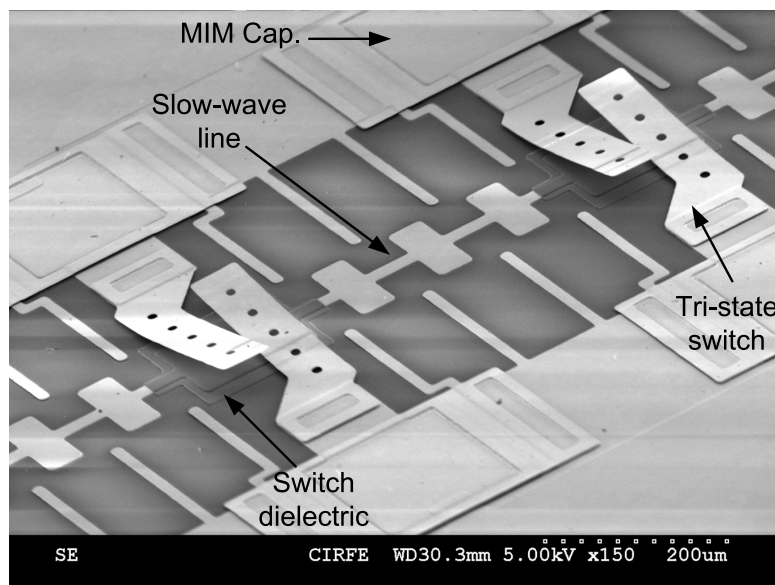


Figure 3.6: SEM image of the tri-state MEMS switch.

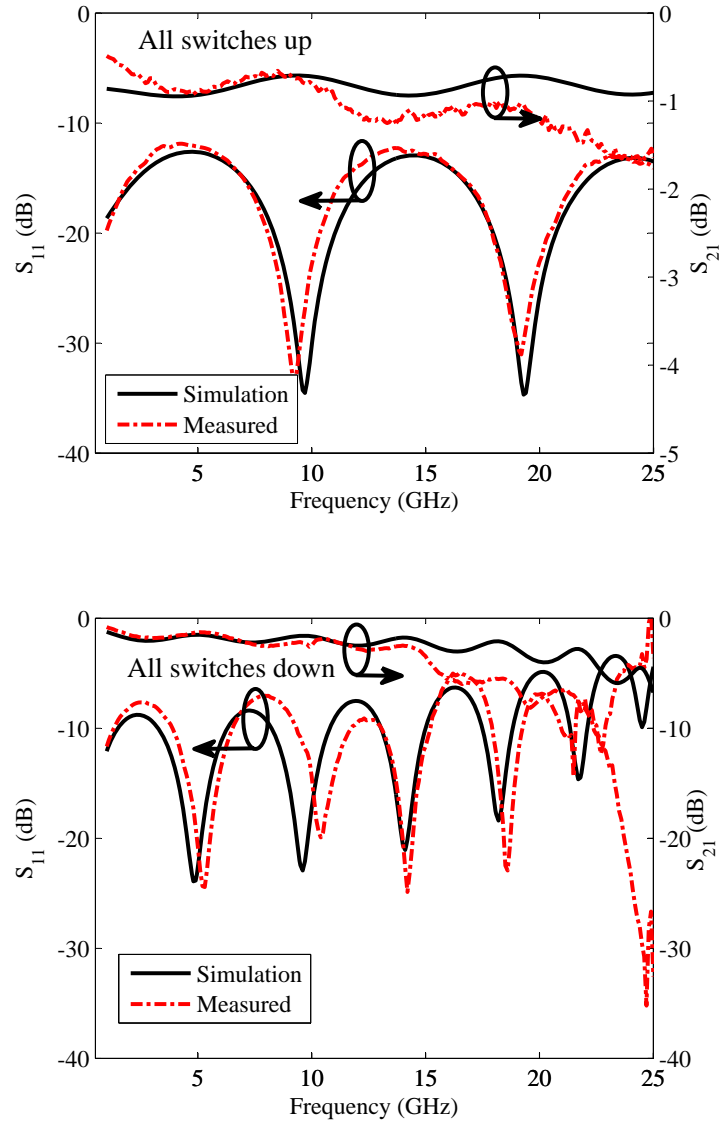


Figure 3.7: Measured v.s. simulated S-parameters of the fabricated impedance matching network for two different states of the MEMS switches.

equivalent circuit model of Fig. 3.8 in order to extract the parameters as summarized in Table 3.2.

The measured impedance coverage of the fabricated network on the Smith chart is

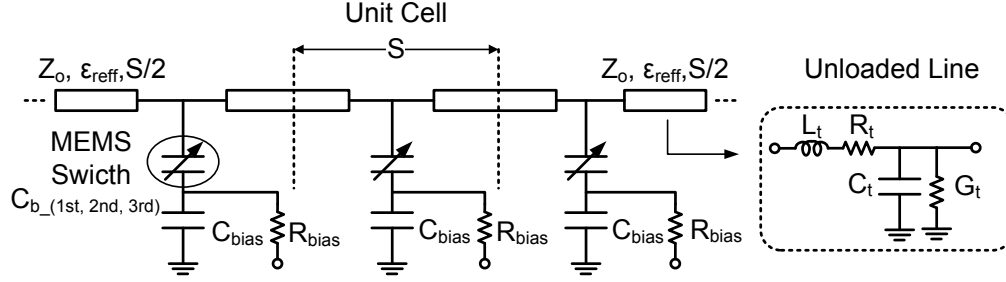


Figure 3.8: Equivalent circuit model of the matching network with 3-state MEMS switches.

obtained using the equivalent circuit model of Fig. 3.8 and the parameters listed in Table 3.2. Fig. 3.9 shows all the impedance points on the Smith chart that can be matched to 50 Ω source impedance using the fabricated matching network at four different frequencies from 5 GHz to 20 GHz. The computed uniformity factor, χ^2 , using (3.2) and for $N_i=25$, $N_j=10$, over a frequency band from 1 to 22 GHz is also presented in Fig. 3.10. The uniformity factor is less than 1000 from 9 GHz to 21 GHz which corresponds to an acceptable uniform coverage of the Smith chart [51]. The maximum frequency of operation was improved from

Table 3.2: Equivalent circuit model parameters of the DMTL unit-cell extracted from the measured S-parameters

Symbol	Parameter	Value
C_b (1 st /2 nd /3 rd)	capacitance (fF)	11/158/306
$R_t/L_t/G_t/C_t$	RLGC parameters (Ω /pH/S/fF)	0.64/207/2 $\times 10^{-9}$ /45
Z_o	unloaded characteristic impedance (Ω)	68
ϵ_{reff}	unloaded effective dielectric constant	13.6
Z_{DMTL} (1 st /2 nd /3 rd)	characteristic impedance (Ω)	63/40.8/32.3
ϵ_{reff} (1 st /2 nd /3 rd)	effective dielectric constant	15.2/37.1/59.3

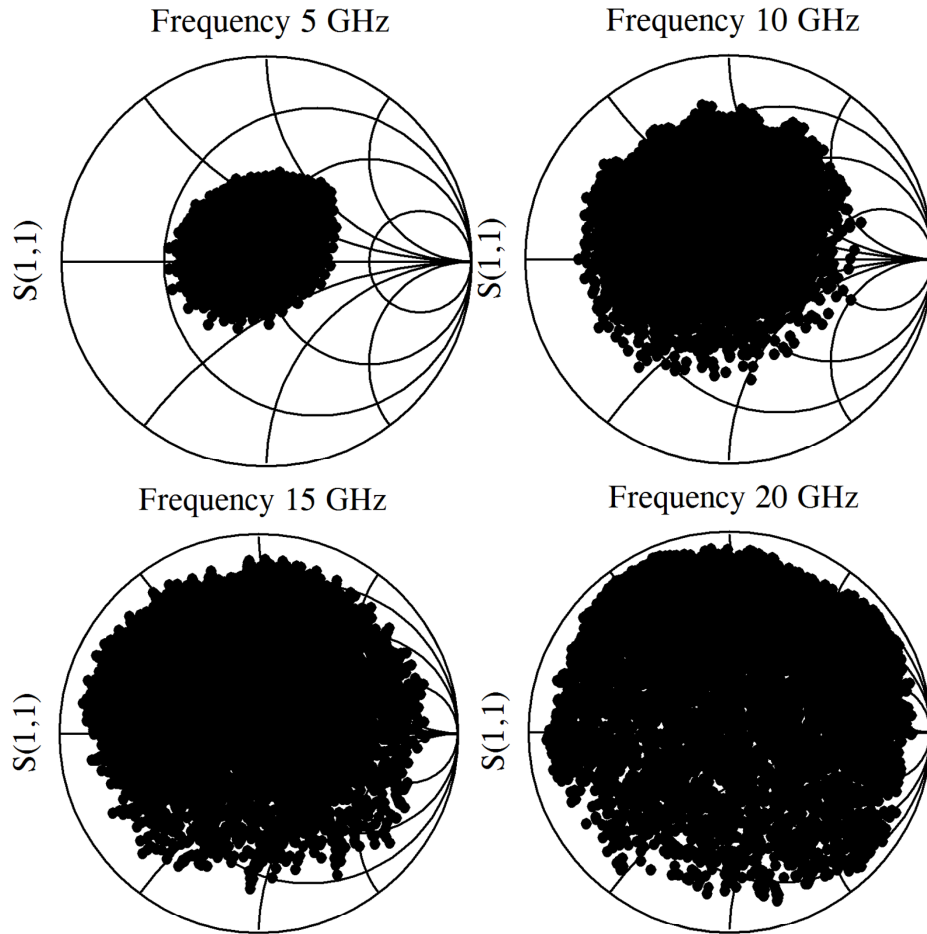


Figure 3.9: Measured impedance coverage of the matching network.

17 for the conventional DMTL matching network to 21 GHz for the proposed impedance matching network based on tri-state MEMS switches.

The Smith chart coverage, presented in Fig. 3.9, represents only a finite number of impedance points on the Smith chart that can be perfectly matched to 50Ω . On the other hand, impedance matching is usually evaluated in terms of a given level of return loss. The return loss performance of the network when used to match different source impedances to 50Ω load at different frequencies is shown in Fig. 3.11. As seen in this figure, using the fabricated network, a wide range of impedance values can be matched to 50Ω with a return

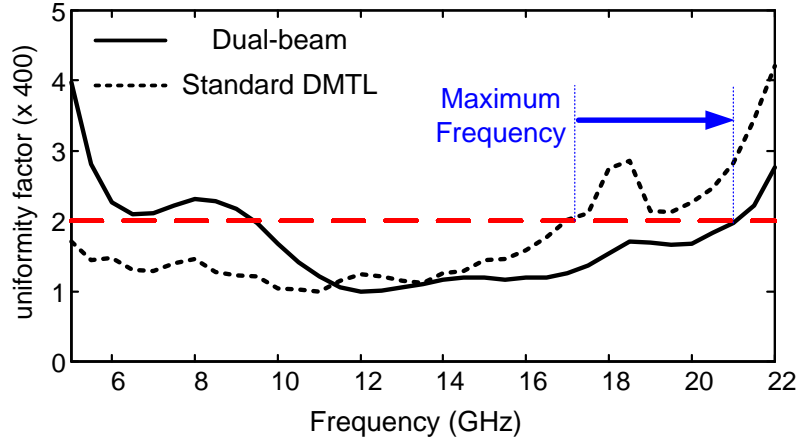


Figure 3.10: Measured uniformity factor of the matching network with tri-state MEMS switches compared to a standard DMTL network.

loss better than 10 dB. The maximum measured voltage standing wave ratio (VSWR) for an impedance matching with a return loss better than 10 dB is 3.56, 8.1, 15.7 and 24 at 5 GHz, 10 GHz, 15 GHz and 20 GHz respectively.

The performance of the matching network in terms of loss can be analyzed by using the power transfer ratio (G_T) when the matching network is used to transfer power between a source with 50Ω impedance and a load with variable impedance. The power transfer ratio includes both the loss from the matching network itself as well as the loss caused by the impedance mismatch between the ports and is obtained using the following equation:

$$G_T = \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} |S_{21}|^2 \quad (3.7)$$

Fig. 3.12 shows the worst case power transfer ration as a function of VSWR at different frequencies computed using the measured S-parameters for all the possible combinations of the MEMS switches states. Based on these results, the fabricated impedance matching network can be used to match different load impedances out to a maximum VSWR of 24:1

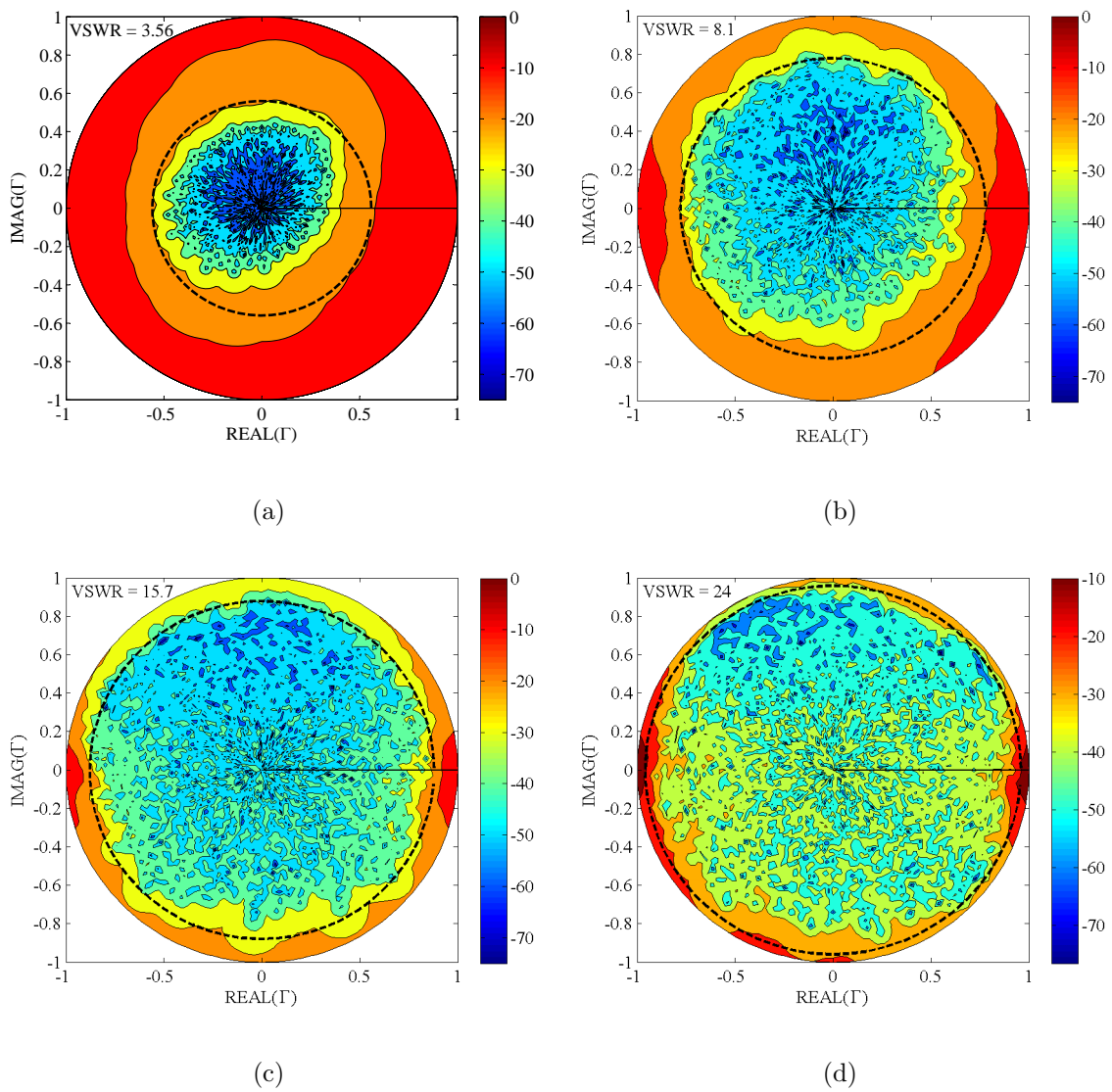


Figure 3.11: Measured return loss performance of the network at (a) 5 GHz, (b) 10 GHz, (c) 15 GHz and (d) 20 GHz.

at 20 GHz with a power transfer ratio of better than 4.3 dB and an impedance matching better than 10 dB.

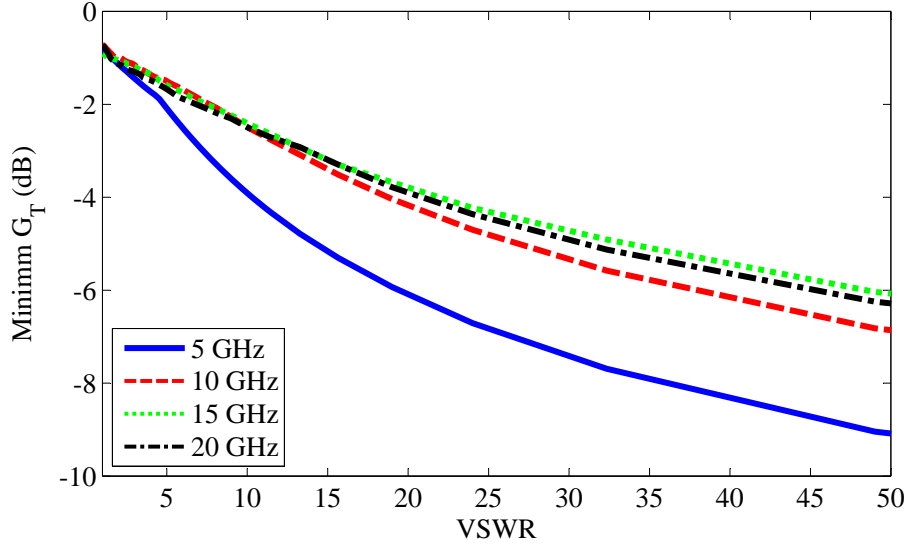


Figure 3.12: Measured minimum power transfer ratio of the fabricated network versus VSWR at different frequencies.

3.3 Matching Network Using DGS structure

The previously reported MEMS impedance matching networks based on DMTL structure where the signal line is periodically loaded with capacitive MEMS switches have achieved wide impedance coverage, lower insertion loss and better performance in terms of linearity and power handling compared to the other semiconductor impedance matching networks. Still these MEMS impedance matching networks have a limited performance in terms of power handling capability. This is due to the use of MEMS capacitive switches on the signal line which suffer from self-actuation under high RF power levels [53]. Additionally, the insertion loss of these networks deteriorates when a large number of MEMS switches are used to achieve higher number of impedance matched points on Smith chart and wider impedance coverage.

For the MEMS impedance matching network presented in this section, instead of using

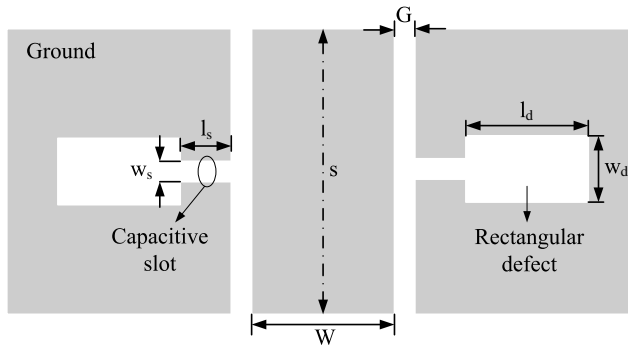


Figure 3.13: Layout of the DGS unit cell, l_s and w_s are the slot dimensions, l_d and w_d are the rectangular defect dimensions and W and G are the CPW transmission line dimensions.

MEMS switches as a capacitive loading between the signal line and ground planes of the transmission line, we have employed MEMS switches on only the ground planes of the transmission line section. This will improve the power handling capability and also the insertion loss of the matching network as will be demonstrated through the measurement results.

3.3.1 Design and Analysis

Transmission lines with periodic defected ground structures (DGSs) have been previously applied to microwave filters [54], RFICs and amplifiers [55, 56] and many other microwave circuits such as couplers, antennas and power dividers [57, 58, 59]. They provide increased slow-wave factor and higher characteristic impedance which can be used to realize microwave circuits with smaller size and better performance.

The transmission line with DGS consists of rectangular defects and a narrow capacitive slots etched on the ground planes of the CPW line as shown in Fig. 3.13. Both the characteristic impedance and the effective dielectric constant of the transmission line can be adjusted by employing the slow-wave characteristic of the DGS cells. Each DGS unit

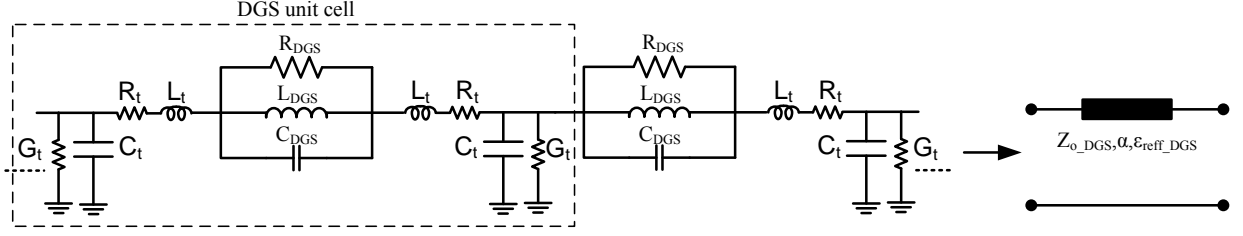


Figure 3.14: Equivalent circuit model of the DGS structure.

cell is modeled by two sections of transmission line and a series RLC circuit as shown in the equivalent circuit diagram of Fig. 3.14. L_t , C_t , G_t and R_t are the parameters for the equivalent $RLGC$ network of the original CPW line without defects which can be obtained from the S-parameters [60]. The rectangular defect is represented by an inductance (L_{DGS}) while the connecting slot is equivalent to a capacitance (C_{DGS}). The resonance characteristic of the DGS unit cell is used to extract R_{DGS} , C_{DGS} and L_{DGS} values according to the following equations [61]

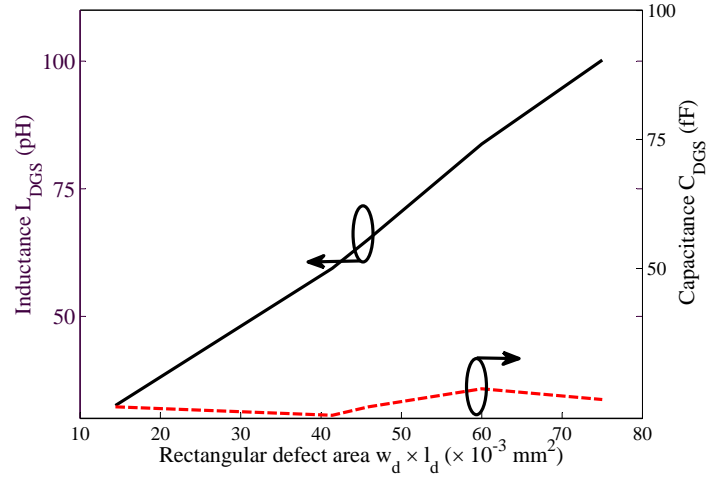
$$R_{DGS} = 2Z_o \left(\frac{1}{|S_{21}|} - 1 \right) \Bigg|_{\omega=\omega_o} \quad (3.8)$$

$$C_{DGS} = \frac{\sqrt{0.316^2(R + 2Z_o)^2 - 4Z_o^2}}{1.9Z_oR(\omega_2 - \omega_1)} \quad (3.9)$$

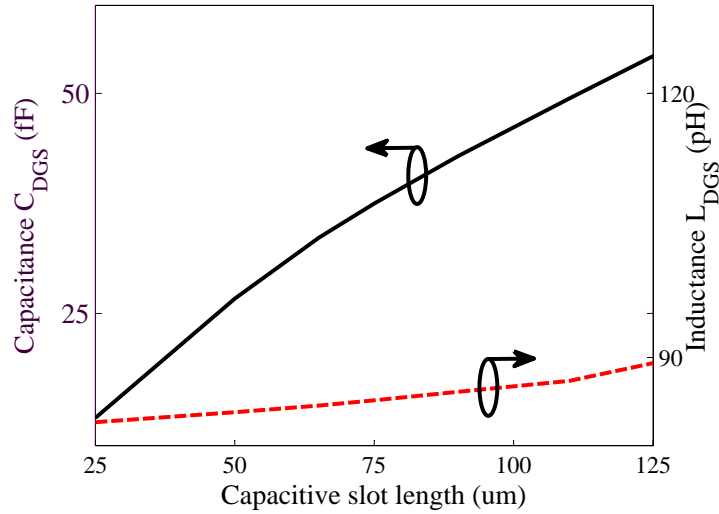
$$L_{DGS} = (\omega_o^2 C_{DGS})^{-1} \quad (3.10)$$

where Z_o is the characteristic impedance of the CPW line without the defects and $\omega_2 - \omega_1$ is the -10 dB bandwidth. Fig. 3.15 shows the simulation results for various dimensions of the rectangular defect, where the inductance L_{DGS} and capacitance C_{DGS} are plotted as a function of the rectangular defect area $w_d \times l_d$ and the length of the capacitive slot l_s . As seen in this figure, the area of the rectangular defect, $w_d \times l_d$, determines the inductance value, L_{DGS} , while the length of the capacitive slot, l_s , mainly affects the capacitance value, C_{DGS} .

The periodic placement of the DGS unit cells along the CPW line will increase the effective dielectric constant of the line (ϵ_{reff_DGS}) due to its slow-wave effect and also the



(a)



(b)

Figure 3.15: L_{DGS} and C_{DGS} as a function of the (a) rectangular defect area $w_d \times l_d$, $l_s = 50 \mu\text{m}$ and (b) the capacitive slot length l_s , $w_d = 200 \mu\text{m}$ and $l_d = 300 \mu\text{m}$.

characteristic impedance of the line (Z_{o_DGS}) according to the following equations:

$$Z_{o_DGS} = \sqrt{\frac{SL_t + L_{DGS}}{SC_t}} \quad (3.11)$$

$$Z_{o_DGS} = Z_o\sqrt{K} \quad (3.12)$$

$$\varepsilon_{reff_DGS} = \varepsilon_{reff}K \quad (3.13)$$

where S is the spacing between two consecutive rectangular defects, Z_o and ε_{reff} represent the characteristic impedance and the effective dielectric constant of the original CPW line without the ground defects, respectively, and K is a scaling factor obtained by

$$K = 1 + \frac{L_{DGS}}{SL_t} \quad (3.14)$$

Fig. 3.16 shows the schematic of the proposed impedance matching network which has 12 sets of DGSs etched on each side of the CPW ground plane with the MEMS series switches with metal-to-metal contact placed across the capacitive slots. When the MEMS switch is in the up state position or 'off' state, the slow-wave effect of the DGS results in a localized high impedance Z_{o_DGS} and a high effective dielectric constant ε_{reff_DGS} region. While, when the switch is actuated to its down-state position, 'on' state, a short bridge is realized across the capacitive slot eliminating the DGS effect and the CPW line characteristic impedance and effective dielectric constant becomes Z_o and ε_{reff} , respectively.

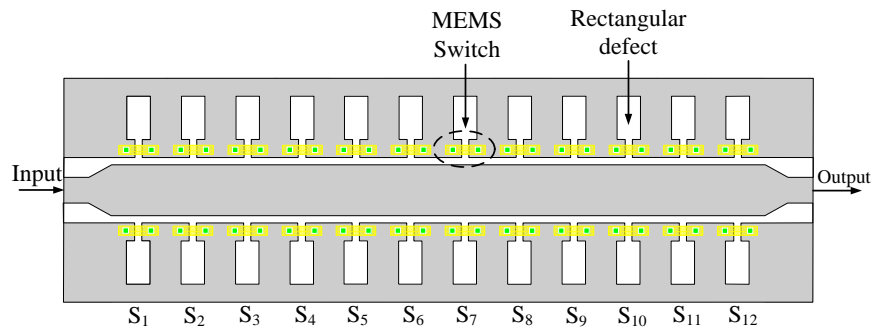


Figure 3.16: Schematic of the reconfigurable impedance matching network with DGS and MEMS contact switches.

The proposed DGS structure with N sets of MEMS switches and rectangular defects can be used to match 2^N different load impedance points at the output port to the source impedance at the input port by individually actuating each set of the MEMS switches. The design goal is to uniformly distribute all these impedance matched points on the Smith chart in order to obtain a wide impedance coverage using the designed network. Assuming the system reference characteristic impedance is Z_{ref} which is commonly 50Ω , there are three main parameters that can be used to optimize the design in terms of impedance coverage. These parameters are: (i) the characteristic impedance of the CPW line without defects Z_o , (ii) the characteristic impedance of the DGS line Z_{o_DGS} and (iii) the electrical length of each DGS unit cell (Φ and Φ_{DGS}) according to the state of the MEMS switch obtained by

$$\Phi = \frac{360^\circ S}{c} f \sqrt{\varepsilon_{ref}} \quad (3.15)$$

$$\Phi_{DGS} = \frac{360^\circ S}{c} f \sqrt{\varepsilon_{ref_DGS}} \quad (3.16)$$

These parameters depend on the geometrical dimensions of the rectangular defect and also the spacing between the DGS unit cells shown in Fig. 3.13. When the output port of the matching network is terminated by the system reference impedance, Z_{ref} , the input impedance Z_k seen from the input port of each DGS unit cell and starting from the load ($k = 0$) to the input port ($k = N$) is computed using the following iterative equation

$$Z_k = \frac{1 + \left(\frac{Z_{k-1} - Z_{DGS,k}}{Z_{k-1} + Z_{DGS,k}} \right) e^{-2j\Phi_k}}{1 - \left(\frac{Z_{k-1} - Z_{DGS,k}}{Z_{k-1} + Z_{DGS,k}} \right) e^{-2j\Phi_k}} Z_{DGS,k} \quad (3.17)$$

for $k = 1$ to N where $Z_{k=0} = Z_{ref}$, $Z_{DGS,k} = Z_o$ or Z_{o_DGS} , and $\Phi_k = \Phi$ or Φ_{DGS} , according to the state of the MEMS switch for the k^{th} DGS unit cell. Then the reflection coefficient at the input port Γ_{in} will be

$$\Gamma_{in} = \frac{Z_N - Z_{ref}}{Z_N + Z_{ref}} \quad (3.18)$$

For a specific frequency band of operation, using the design parameters mentioned earlier and equations (3.17) and (3.18), all the impedance points on the Smith chart that can be

matched to a 50Ω source impedance and using the designed DGS impedance matching network can be obtained. The design parameters can be optimized using a mathematical software such as MATLAB and based on the uniformity of the Smith chart coverage. The uniformity of Smith chart coverage is assessed based on the uniformity factor, χ^2 , previously defined by equation (3.2).

The geometrical dimensions of the designed DGS impedance matching network are listed in Table 3.3. The finite ground CPW line with dimensions $20/150/20 \mu\text{m}$ ($G/W/G$) on a 25 mil thick alumina substrate ($\epsilon_r = 9.8$) results in a characteristic impedance of $Z_o = 35 \Omega$, and an effective dielectric constant of $\epsilon_{reff} = 5.4$. The impedance and the effective dielectric constant of the DGS structure are Z_{o_DGS} close to 50Ω and $\epsilon_{reff_DGS} = 8.9$. The equivalent circuit model parameters of the DGS unit cell are also listed in Table 3.3. Fig. 3.17 shows the impedance coverage of the designed network obtained using equations (3.17-18) and the design parameters listed in Table 3.3. As seen in this figure, the network achieves a wide coverage of the Smith chart for a frequency band from 24 GHz to 60 GHz.

The maximum frequency of operation of the proposed impedance matching network is limited by the self-resonance frequency of the DGS unit cell and also the Bragg frequency

Table 3.3: Geometrical parameters and the equivalent circuit model parameters

<i>Geometrical Parameters (μm)</i>						
l_s	w_s	l_d	w_d	W	G	S
50	30	180	80	150	20	280
<i>Equivalent Circuit Parameters</i>						
R_{DGS}	L_{DGS}	C_{DGS}	Z_o	Z_{o_DGS}	ϵ_{reff}	ϵ_{reff_DGS}
1.067 k Ω	73.87 pH	21.56 fF	35 Ω	50 Ω	5.4	8.9

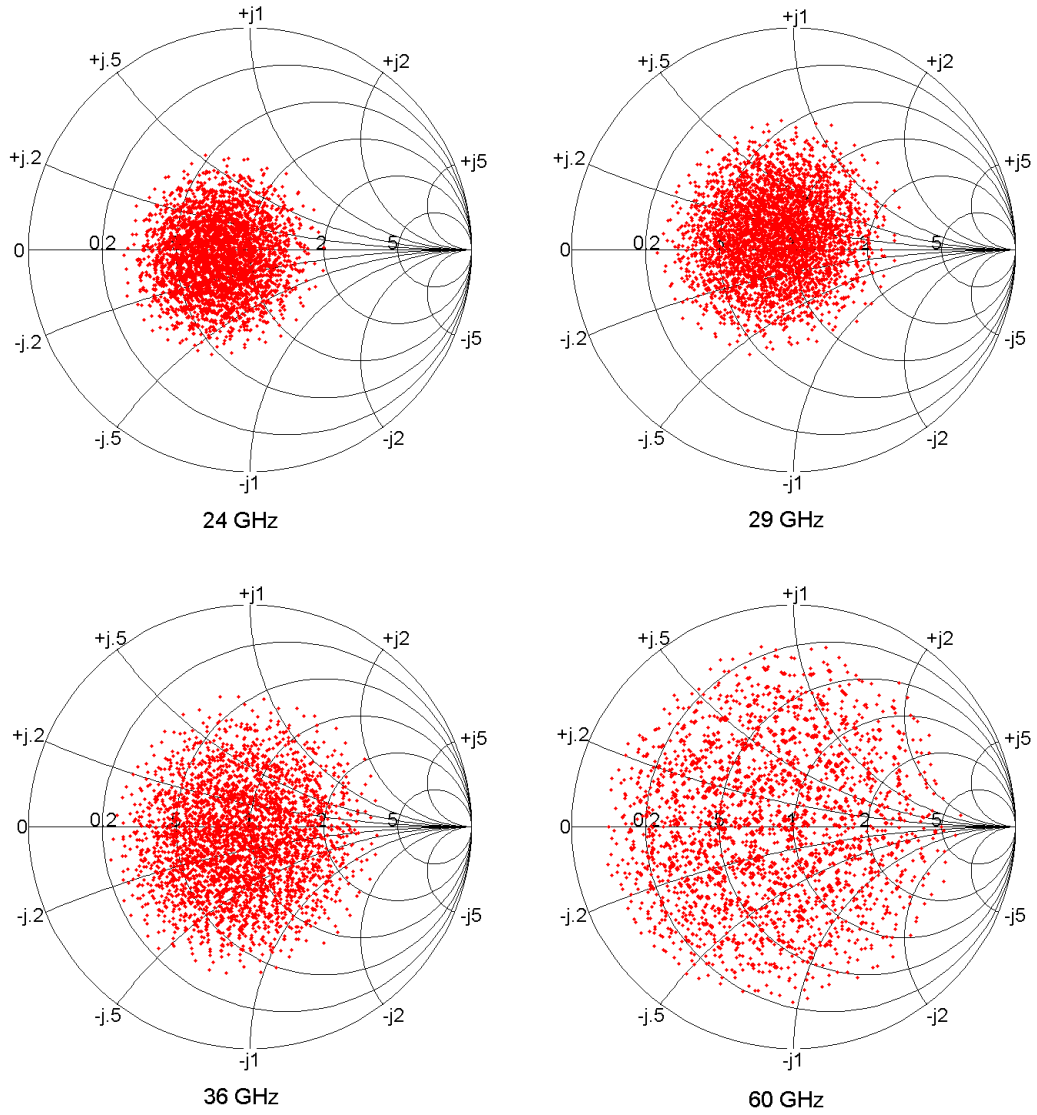


Figure 3.17: Calculated impedance coverage of the DGS impedance matching network at different frequencies from 24 to 60 GHz.

of the periodic DGS structure. The simulated self-resonance frequency of the DGS unit cell with the dimensions listed in Table 3.3 is obtained to be 126 GHz. The Bragg frequency f_B of the periodic DGS structure when all the MEMS switches are in the up-state position

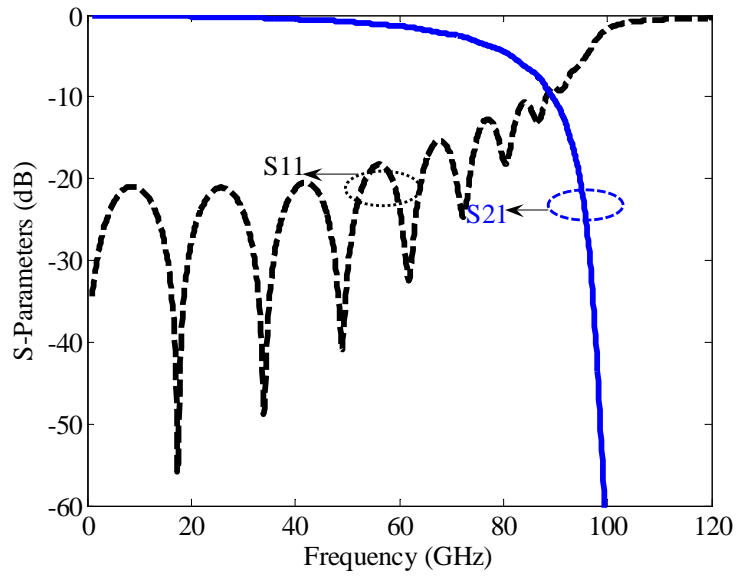
is calculated using (3.19) and is obtained to be 87 GHz.

$$\begin{aligned}\omega_B &= \sqrt{\frac{b - \sqrt{b^2 - 4ac}}{2a}} \\ a &= S^2 L_t C_t L_{DGS} C_{DGS} \\ b &= S^2 L_t C_t + S L_{DGS} C_t + 4 L_{DGS} C_{DGS} \\ c &= 4\end{aligned}\tag{3.19}$$

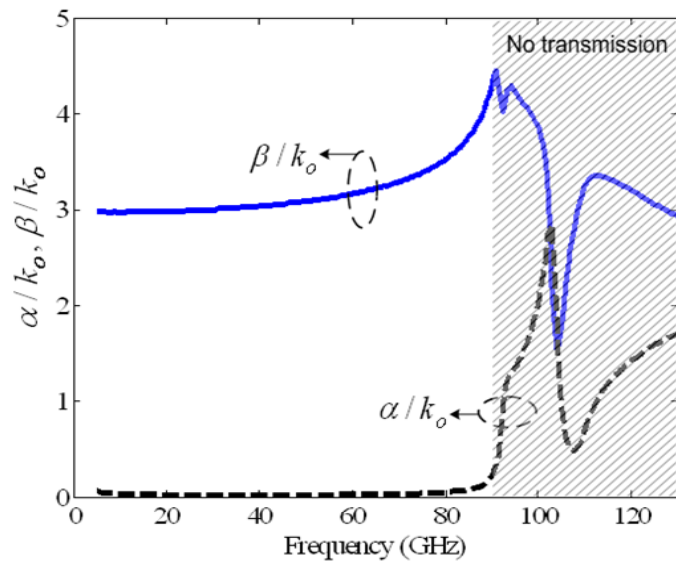
Fig. 3.18(a) shows the simulated S-parameters of the DGS structure with 12 unit cells when all the MEMS switches are in their up state position. The dispersion characteristic is also presented in Fig. 3.18(b). When the frequency of operation is approaching the Bragg condition, there is a significant rise in the attenuation constant and the signal is attenuating. This defines the stop-band of the periodic structure. The Bragg frequency obtained from the dispersion characteristic agrees with the theoretical value using (3.19).

3.3.2 Fabrication Process

Fabrication of the reconfigurable impedance matching network was performed at the University of Waterloo in the CIRFE lab. As shown in Fig. 3.19, it begins with e-beam evaporation of a 50 nm Chromium (Cr) layer to form the biasing lines and actuation electrodes. These patterns are encapsulated by a 300 nm PECVD deposited silicon nitride (Si_xN_y) film except where the bias pads are located. Next, 2 μm gold (Au) is electroplated on a 30/50 nm TiW/Au bilayer and patterned to form the CPW lines. Consecutively, a 3 μm of sacrificial photoresist layer is employed and patterned for the anchors, and dimples on the switch contact points. A 1.3 μm electroplated Au layer on top of a 0.2 μm evaporated Au seed layer is used for the cantilevers. Finally, the sacrificial layer is removed using wet release and critical-point-drying (CPD) is used to release the MEMS switches.



(a)



(b)

Figure 3.18: (a) simulated S-parameters and (b) the dispersion characteristic of the periodic DGS structure.

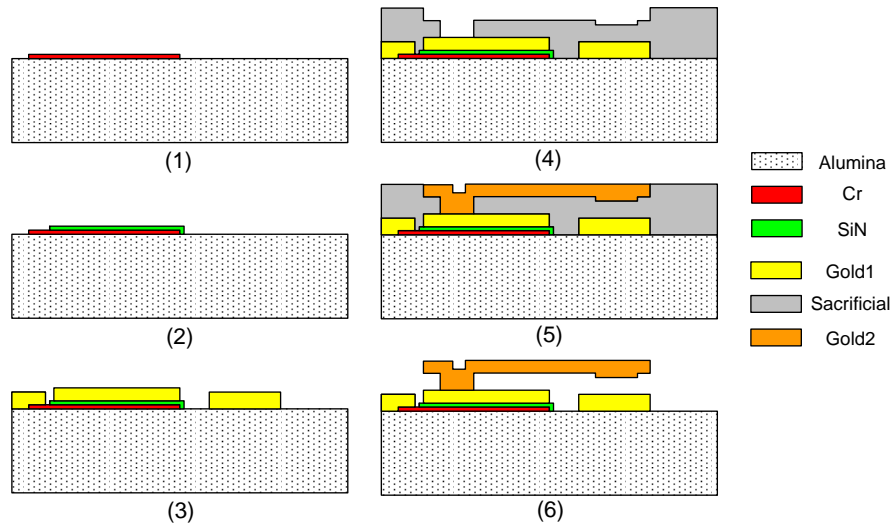


Figure 3.19: The fabrication process for the DGS impedance matching network.

Fig. 3.20 shows the photograph of the fabricated matching network. The size of the device is only $1.3 \times 3.6 \text{ mm}^2$. An SEM image of the MEMS series-contact switch is also presented in Fig. 3.21. The MEMS switch is based on a cantilever structure which does

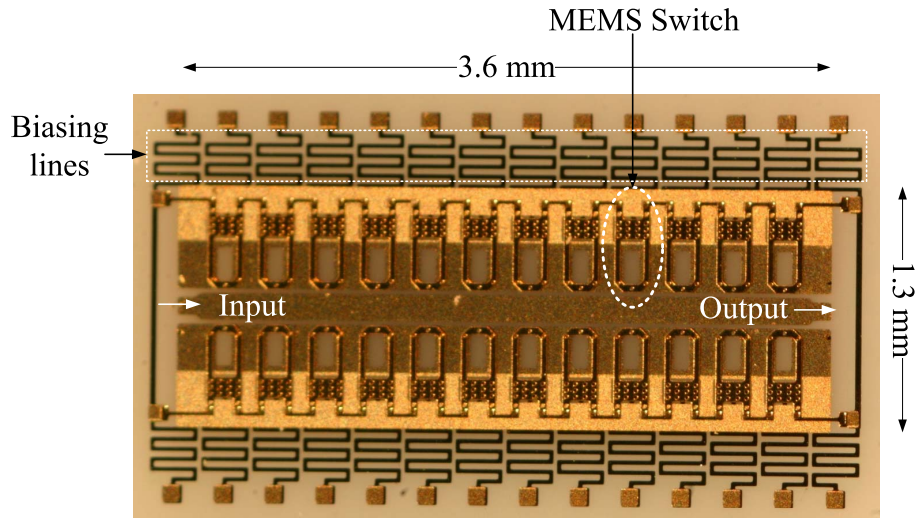


Figure 3.20: Picture of the fabricated reconfigurable impedance matching network using DGS structure.

not require a high DC actuation voltage (measured $V_{pi} = 21$ V). Despite the low actuation voltage, the power handling of the network is not limited by self actuation under high RF power levels. Additionally, the loss of the switch does not have any significant impact on the insertion loss of the structure. Hence wider impedance coverage can be achieved by increasing the number of MEMS switches.

3.3.3 Experimental Results

The fabricated network can produce 4096 (2^{12}) different impedance points covering the Smith chart. The equivalent circuit model of the DGS unit cell presented in Fig. 3.14 is used to simulate all the possible impedance match points at different frequencies. The validity of the equivalent circuit model is demonstrated by comparison with the measurement results. Fig. 3.22 shows the comparison between the S-parameters using the circuit model and measured results when all the switches are in the up state and down state posi-

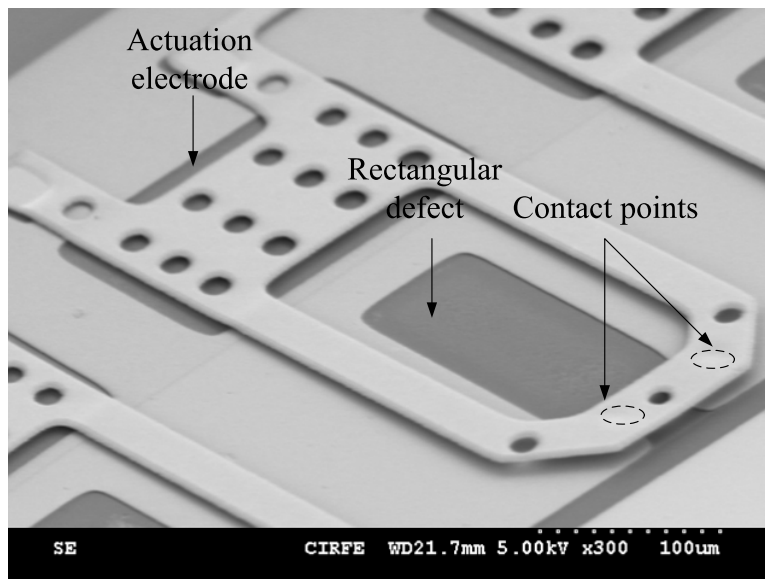
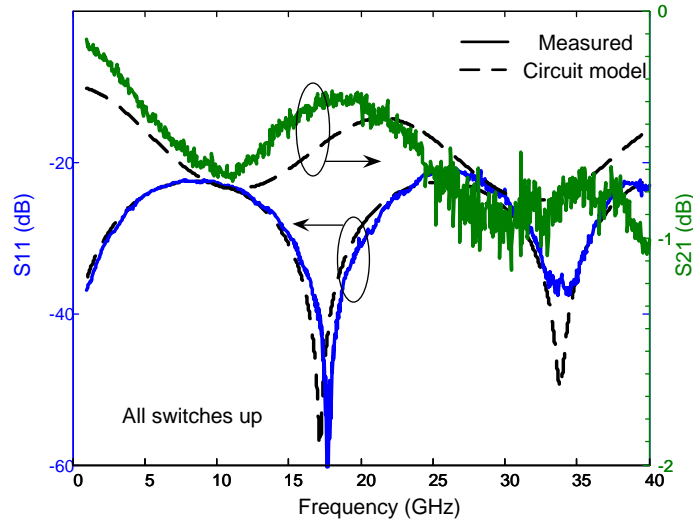
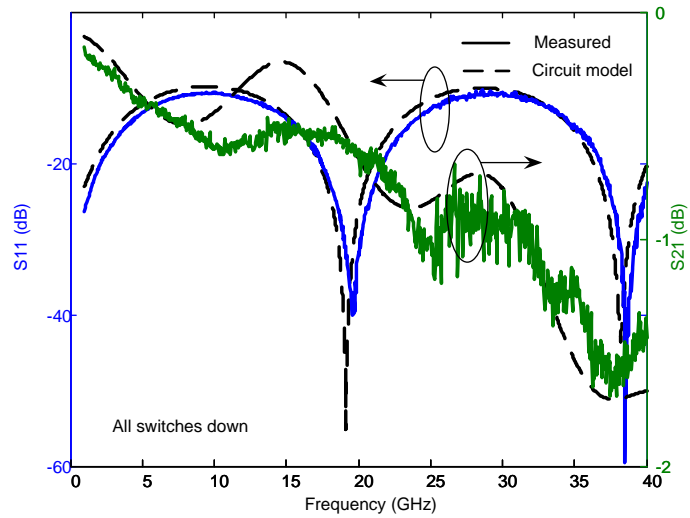


Figure 3.21: SEM image of the fabricated MEMS series-contact switch.

tions, respectively. The simulated 4096 and measured 20 impedance points on the Smith



(a)



(b)

Figure 3.22: Simulated v.s. measured S-parameters when all the switches are in their (a) up-state position 'off' and (b) down state position 'on'.

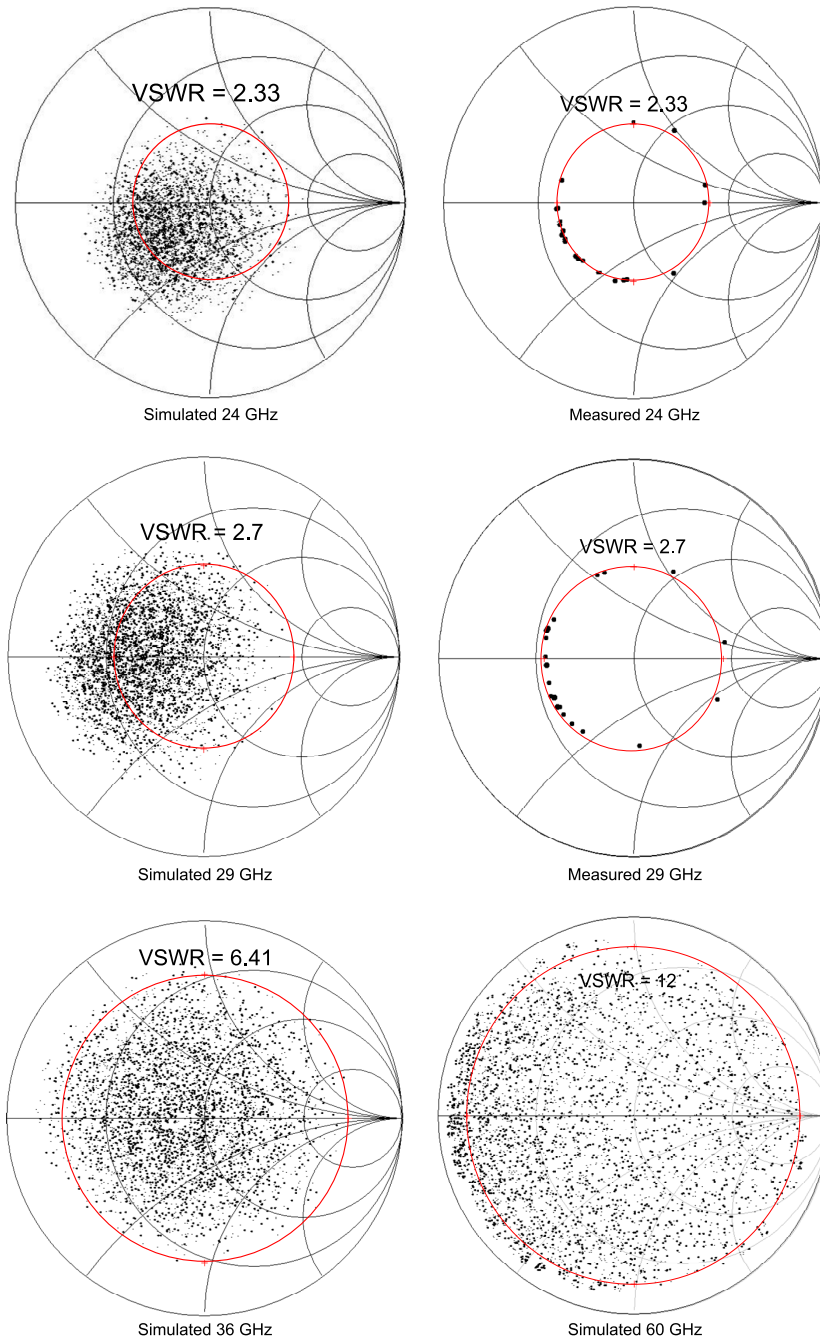
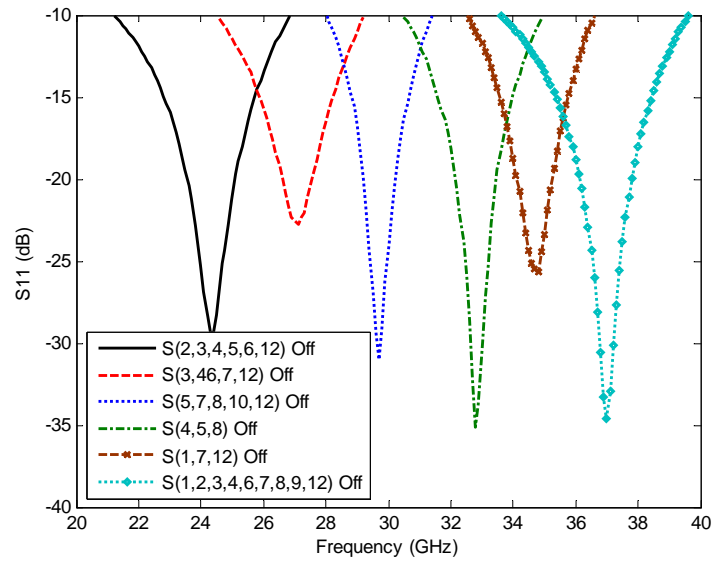
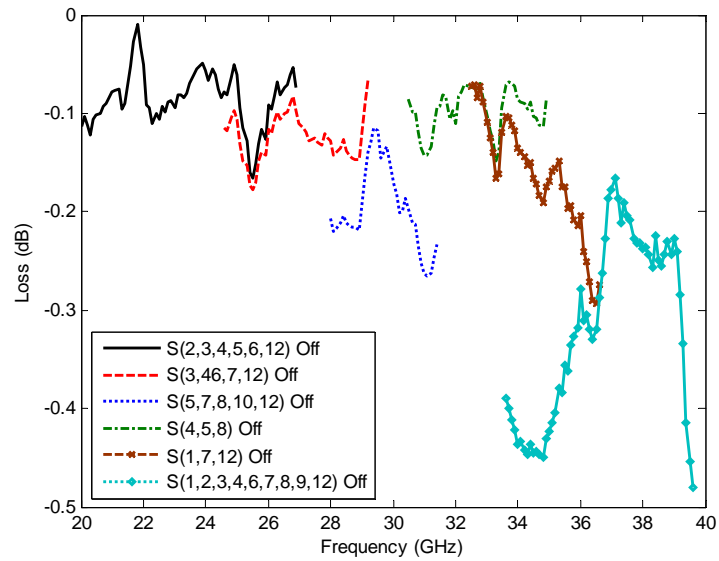


Figure 3.23: Simulated (4096) and measured (20) impedance points of the fabricated re-configurable impedance matching network at different frequencies.



(a)



(b)

Figure 3.24: Measured S_{11} and loss of the matching network when used to match a 10Ω load to 50Ω .

chart at different center frequencies are shown in Fig. 3.23. Measurements are performed by terminating the input port by a 50Ω load and calculating the reflection coefficient at the output port in ADS. The switch combinations for impedance point measurements are chosen to obtain the maximum VSWR circles. There is a good agreement between the simulated and measured achievable maximum VSWR using the developed impedance matching network. The network can be used to match loads up to a maximum VSWR of 6.41:1 and 12:1 at 36 GHz and 60 GHz, respectively.

The impedance matching performance is demonstrated by terminating the output port with a 10Ω load and matching it to 50Ω reference impedance at different center frequencies using different settings of MEMS switches. The measured return loss and also the loss of the network is presented in Fig. 3.24. Since the ports are mismatched in this case, the loss of the network is more accurately defined as the ratio between the power transferred to the load and the power delivered into the network [13]

$$\alpha = \frac{|S_{21}|^2}{1 - |S_{11}|^2} \quad (3.20)$$

The network is capable of matching a 10Ω load to 50Ω with a return loss better than 12 dB from 22 GHz up to 40 GHz while the measured loss is better than 0.5 dB all over the frequency band.

The power handling of the impedance matching networks becomes an important issue when they are used for output matching of power amplifiers in RF front-ends or when they are used as impedance tuners in load-pull measurement setups. To measure the power handling capability of the fabricated DGS impedance matching network, the test setup shown in Fig. 3.25 is used. Using a 25 dBm RF signal at 10 GHz from the synthesizer and a 20 W X-band amplifier, a maximum RF power level of 41 dBm (12 W) can be transferred to the matching network. The test is performed by varying the input power to the matching network and measuring the output power for several settings of MEMS switches as shown in Fig. 3.26. The results illustrate a linear increase in the output power level proportional

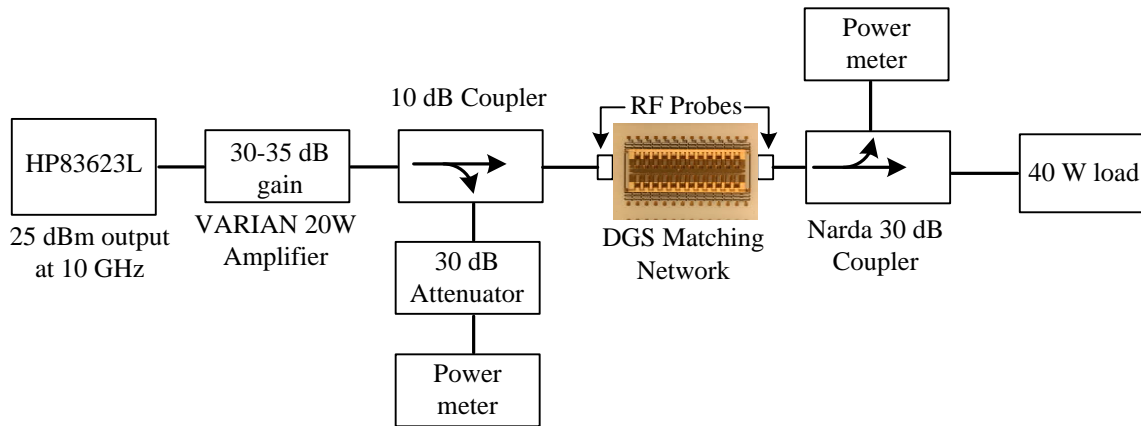


Figure 3.25: High power measurement setup.

to the input power without any sign of self-actuation of the MEMS switches for an input power level up to 41 dBm (12 W). This power handling level is considered to be the highest reported power handling capability among the existing RF MEMS impedance matching networks [12].

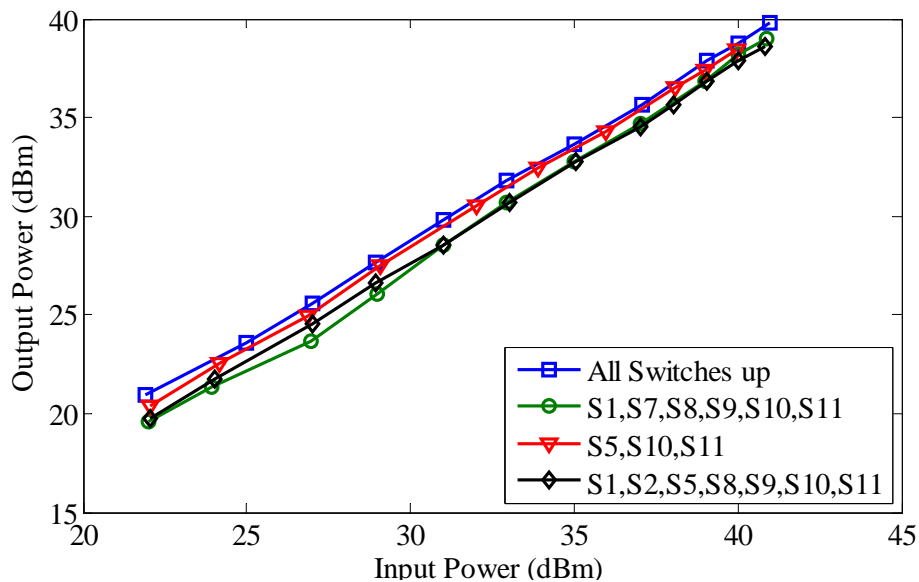


Figure 3.26: Measured power handling of the matching network.

The use of tunable MEMS devices for RF applications is beneficial in terms of generating very low intermodulation products and it makes them attractive for tunable filter, phase shifters or matching networks for communication applications [62]. The performance of the fabricated DGS impedance matching network in terms of nonlinearities is demonstrated through the intermodulation distortion analysis of the network using the two-tone third-order intermodulation intercept point (IIP3) measurement setup as shown in Fig. 3.27. The output spectrum of the impedance matching network for $f = 20$ GHz and an offset frequency of $\Delta f = 10$ kHz when all the MEMS switches are in their up-state position and the input/output ports are terminated with 50Ω RF probes is presented in Fig. 3.28. The simulated mechanical self-resonance frequency of the cantilever MEMS switch for the first transverse modal shape using ANSYS is $f_o = 10.81$ kHz as shown in Fig. 3.29. The nonlinearities of the MEMS switch will be prominent when $\Delta f \leq f_o$. As seen in Fig. 3.28, the measured 3^{rd} order intercept point (TOI) is 42 dBm and is expected to be even higher for higher Δf values which can not be measured due to the noise limitations of the test setup in Fig. 3.27.

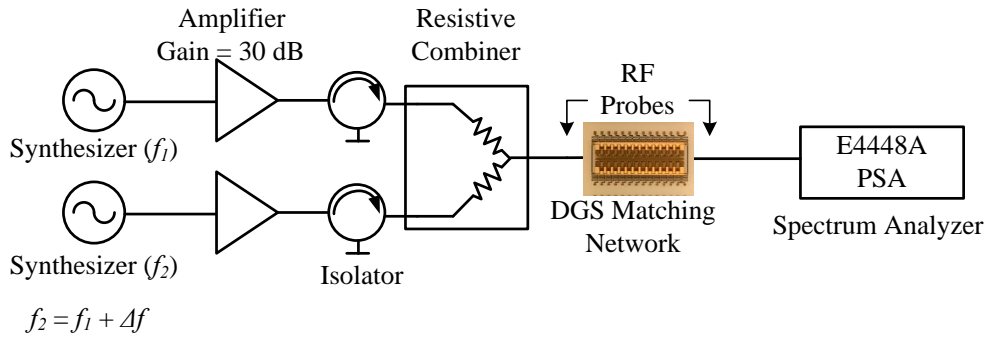


Figure 3.27: Intermodulation test setup.

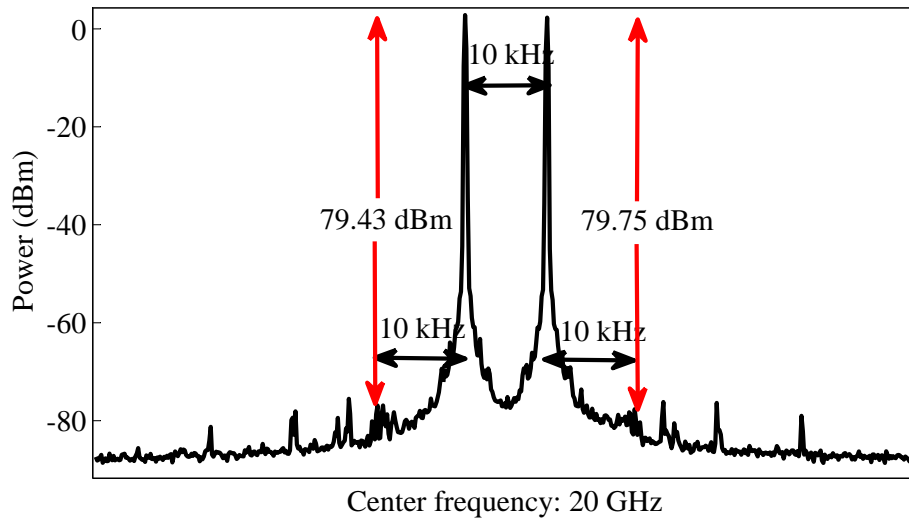


Figure 3.28: Measured output spectrum for $f = 20$ GHz and $\Delta f = 10$ kHz.

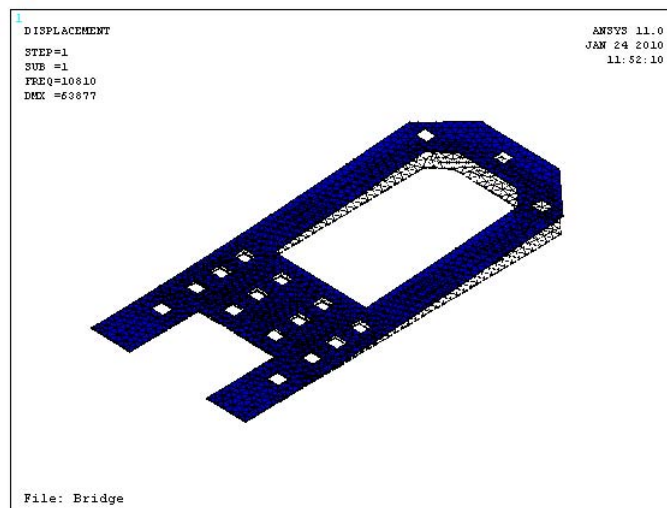


Figure 3.29: Simulated mechanical self-resonance frequency of the cantilever MEMS switch.

3.4 Summary

In this chapter, two novel structures for RF MEMS tunable impedance matching networks are presented. A reconfigurable impedance matching network based on a slow-wave DMTL structure loaded with tri-state MEMS capacitive switches is proposed with an extended operating frequency range both for the lower and upper bands. The size of the network fabricated on an alumina substrate is very compact ($4.4 \times 1.9 \text{ mm}^2$). The fabricated network achieves an improved impedance coverage between 5 GHz and 20 GHz and the measured power transfer ratio is better than 4.3 dB for a wide range of input impedances. A reconfigurable impedance matching network using MEMS series-contact switches and periodic defected ground structures is presented. The application of DGSs results in an improved insertion loss and power handling capability. Measurement results demonstrate wide coverage of the Smith chart. The measured loss of the network when used to match a 10Ω load to 50Ω from 22 GHz up to 40 GHz is only 0.5 dB.

Chapter 4

CMOS-MEMS Integration and RF-MEMS Devices Fabricated using This Process

4.1 Introduction

Silicon-based standard complementary metal-oxide-semiconductor (CMOS) technologies have always been of great interest for the implementation of wireless communication systems due to their mature fabrication process, higher level of integration with other analog and digital signal processing circuits and also low fabrication cost. During the past few years, the need for a wider frequency bandwidth has been a main reason to extend the applicability of silicon-based CMOS technologies for microwave and millimeter-wave applications. Millimeter-wave CMOS circuits with superior RF performance such as CMOS oscillators [63], mixers [64], amplifiers [65] and microwave passive components [66], [67], have been previously demonstrated. In addition to a higher frequency of operation, another key requirement in the current wireless communication industry is the multi-band function-

ality enabling the integration of several wireless standards into a single RF front-end that can operate in different frequency bands. Most recent solutions for the implementation of these multi-band RF front-ends employ RF MEMS devices [30, 68, 69, 70]. RF MEMS devices offer an excellent RF performance, low DC power consumption, light weight, better linearity and low intermodulation products at millimeter-wave frequencies [50]. However, the MEMS-based multi-band RF front-ends incorporate off-chip MEMS devices and have not led to a fully integrated silicon solution using a mainstream CMOS process. An integrated monolithic CMOS implementation of the RF MEMS devices will result in low cost single chip RF multi-band systems with enhanced performance and functionality by eliminating the packaging parasitics present in the hybrid integration approaches.

Monolithic integration of RF MEMS switches with active CMOS circuitry based on a CMOS-compatible MEMS fabrication process was reported in [31] where the RF MEMS switches were stacked on a CMOS chip and controlled by the underlying CMOS control circuitry. The fabrication of the proposed monolithically integrated RF MEMS switches requires development of a low temperature ($T < 350^\circ\text{C}$) MEMS fabrication process that does not damage the underlying CMOS active circuits. An alternative CMOS-MEMS integration approach was pioneered by Fedder *et al.* [32], [71] to create electrostatically actuated micro-structures with high aspect ratio composite beam structures. RF MEMS devices like tunable capacitors [72] and micromachined inductors [33] using this post-CMOS maskless micromachining process have been developed. A capacitive series-type RF MEMS switch using the same integration approach was reported in [41]. The switch is thermally actuated and has a comb-finger structure for the capacitive coupling between the input/output RF ports. The maximum reported capacitance ratio of the switch is limited to 15:1. Moreover, thermal actuators consume high DC power for actuation; therefore, they require latching mechanisms adding to the complexity of the RF MEMS switch design and increasing the chip real state.

The CMOS-MEMS post-processing in [32] can be used for the integration of microstructures with only lateral motion such as interdigital MEMS tunable capacitors. In this chapter, we introduce a maskless CMOS-MEMS integration approach developed at the University of Waterloo that allows the integration of MEMS structures with vertical motion in CMOS technology for the first time [73]. The advantage of RF MEMS structures with electrostatic actuation and vertical motion such as parallel-plate MEMS tunable capacitors compared to interdigital structures are higher quality factor, smaller size and also higher self-resonance frequency. Several RF MEMS devices are fabricated using the proposed processing technique. These devices include parallel-plate MEMS varactors which are compact and exhibit a high quality factor and an acceptable tuning range, a tunable bandpass filter operating at 10 GHz, and novel CMOS-MEMS capacitive shunt-type switches for microwave and millimeter-wave applications. The proposed RF MEMS devices can be used in future reconfigurable CMOS RF front-ends.

4.2 CMOS-MEMS Integration

There are three different approaches to fabricate and integrate tunable RF MEMS devices within CMOS, GaAs, SiGe or any other IC compatible technology. The first two approaches, referred to as modular integration, allow the separate development and optimization of electronics and MEMS processes [74]. The Pre-CMOS integration scheme involves the fabrication of the CMOS electronics on top of the MEMS structures and was first demonstrated by Sandia National Laboratories [75]. The second scheme introduced by Texas Instruments Inc. [76] requires the fabrication of MEMS structures on top of VLSI-CMOS electronics without damaging the underlying circuitry. In order to achieve high performance and reliable integrated MEMS technology using this technique, low-temperature CMOS compatible micromachining processes are needed to be developed. The third approach to CMOS-MEMS integration is by using post-processing techniques in

order to fabricate MEMS structures using the existing metal interconnect layers available in a standard CMOS process. This approach will be considered as the main CMOS-MEMS integration technique in this chapter.

The proposed CMOS-MEMS processing technique is applicable to any standard and commercially available CMOS technology with more than four metallic layers such as 0.35- μm CMOS or 0.18- μm CMOS technologies from TSMC, Taipei, Taiwan. The 2P4M 0.35- μm CMOS technology consists of two poly-silicon layers and four metal (Aluminum) layers as shown in Fig. 4.1. The metal layers are a composite layer of TiN/Al/Ti and the inter-metal dielectric (IMD) layer between the interconnect metal layers is borophosphosilicate glass (BPSG). The passivation layer on top of the chip is $\text{Si}_x\text{N}_y/\text{SiO}_2$. Fig. 4.1 shows the cross-section view and the thickness of each metal and IMD layers. MEMS devices are constructed using composite metal-dielectric layers as the structural layers and by using one or more metal layers as the sacrificial layers as will be explained in a later section.

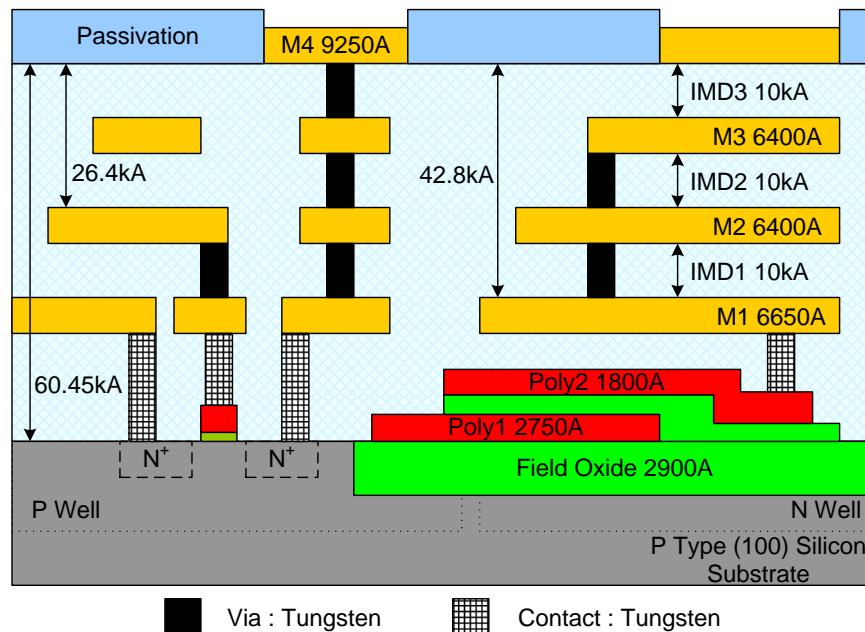


Figure 4.1: 2P4M 0.35- μm CMOS process from TSMC.

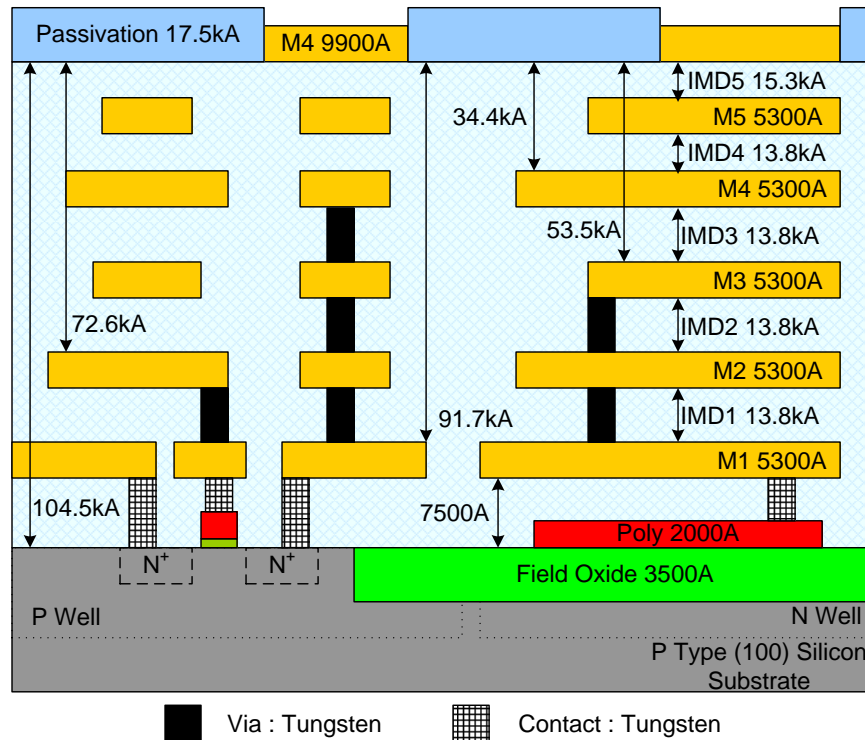


Figure 4.2: 1P6M 0.18- μm CMOS process from TSMC.

The other CMOS technology which is utilized for CMOS-MEMS integration is the TSMC 1P6M 0.18- μm CMOS process that consists of six metallization layers plus one polysilicon layer with two different resistivity values. The cross-section view of this process is shown in Fig. 4.2.

The CMOS-MEMS processing starts with a chip fabricated using one of the standard CMOS processes mentioned earlier. Fig. 4.3 shows the chip after the standard CMOS processing. The CMOS die may include CMOS active circuitries, MEMS structures and pads formed using the conventional CMOS processing. The MEMS structures are created using the metal and dielectric layers and released by removing the silicon substrate or by etching one or more metal layers as the sacrificial layer. One advantageous feature of the developed process is that it does not require any extra film deposition or lithographic

patterning steps as opposed to the known MEMS fabrication processes. The first processing step is similar to the CMOS-MEMS processing reported in [32], [71]. It includes anisotropic reactive ion etching (RIE) of the CMOS dielectric layer (e.g. silicon dioxide). One of the multiple metal layers of the CMOS layer stack (e.g. M_4) is used as etch resistant mask and portions of the CMOS dielectric layer which is not covered by the metal mask will be removed during this stage. This step is required in order to expose the sacrificial metal layer (e.g. M_2) and also the silicon substrate in some specific areas on the chip.

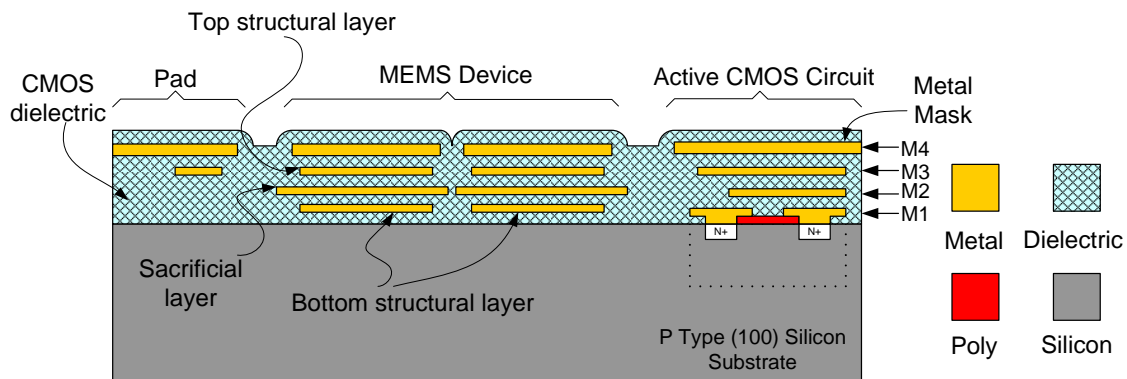


Figure 4.3: CMOS chip after standard processing. M_4 is used as RIE mask, M_3 and M_1 are the MEMS structural layers, and M_2 is the sacrificial layer.

Fig. 4.4 shows the chip after anisotropic RIE removal of portions of the CMOS dielectric layer. Open windows in the dielectric layer are used to access the silicon substrate and also the sacrificial metal layer. Release holes are also included on the MEMS structures in order to facilitate the access to the sacrificial layer between the two parallel-plates of the MEMS structure. The etching recipe used for this step is optimized for the best etch profile and to obtain the maximum possible anisotropy and aspect ratio. The etching rate was another parameter during the recipe optimization. The CF_4/H_2 RIE etch parameters for this step, using the Trion RIE system with inductively coupled plasma (ICP) capability, are listed in Table 4.1.

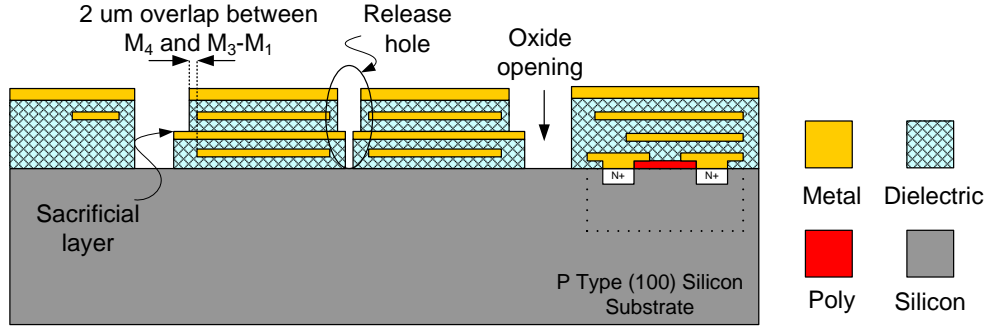


Figure 4.4: First RIE removal of CMOS dielectric layer.

Table 4.1: RIE etch parameters for the first CMOS-MEMS processing step

Target	Pressure	ICP	RF	Gas	Flow	Etch
Material	(mTorr)	Power	Power	Content	(sccm)	rate
Oxide	11	240 W	55 W	CF ₄ :H ₂	39:5	408 A/min

Fig. 4.5 shows the SEM image of the CMOS chip after the 1st RIE of the CMOS dielectric layer. The total thickness of the silicon dioxide (SiO₂) etched during this step is 6 μm and 10.5 μm for the 0.35- and 0.18- μm CMOS technologies, respectively. An issue faced during the RIE removal of the CMOS dielectric is the creation of RIE polymer. This polymer build up will reduce the etching rate or even it can stop further etching of the dielectric layer. For this reason it is recommended to remove this polymer during the RIE of the dielectric layer or at the end of the first processing stage. The RIE polymer can be removed using the post-etch residue remover EKC265TM from EKC Technology, Hayward, CA. As shown in Fig. 4.5, after this step both the sacrificial metal layer and silicon substrate around the MEMS devices are exposed for subsequent etching.

The next processing step is a time-controlled isotropic etching of the silicon substrate in an SF₆/O₂ plasma as presented in Fig. 4.6. This stage is optional and is used to create an air trench under the MEMS structures. This trench is used to improve the RF performance

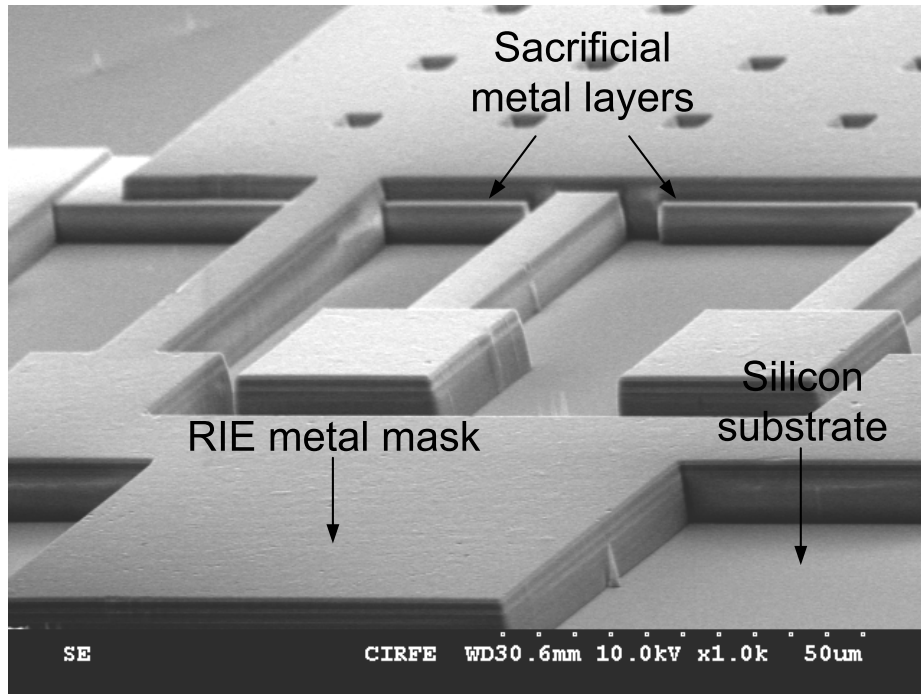


Figure 4.5: First RIE removal of CMOS dielectric layer.

of the MEMS device by removing the parasitic effects of the lossy silicon substrate at higher microwave frequencies. The depth of the trench is in the range of 60 μm to 100 μm with a maximum under-etch of 30 μm . The reactive ion etching parameters used for this step are listed in Table 4.2. Fig. 4.7 shows an SEM image of the CMOS chip after this step.

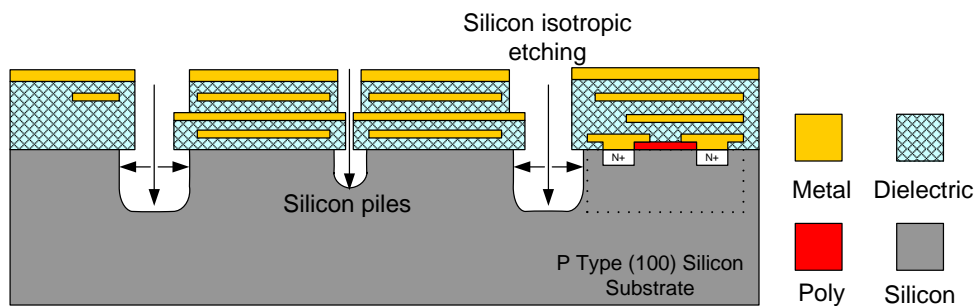


Figure 4.6: Isotropic RIE of silicon substrate under the MEMS structures

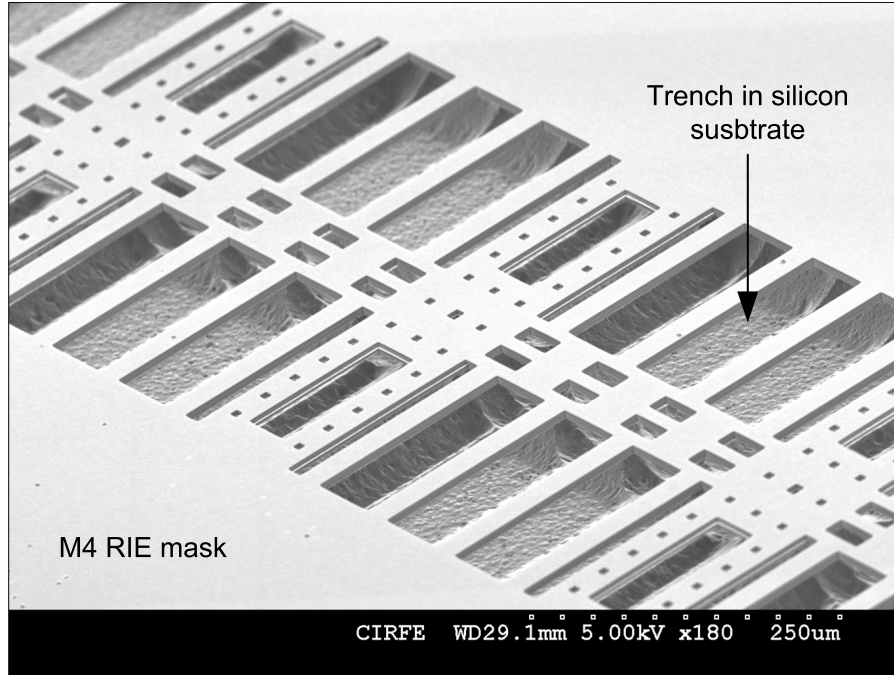


Figure 4.7: SEM image of the CMOS chip after the isotropic RIE of silicon substrate.

Table 4.2: RIE etch parameters for the isotropic silicon etching

Target	Pressure	ICP	RF	Gas	Flow	Etch
Material	(mTorr)	Power	Power	Content	(sccm)	rate
Silicon	50	192 W	0 W	SF ₆ :O ₂	24:5	17 × 10 ³ Å/min

Following the RIE of the CMOS dielectric layer and the silicon substrate, the next step will be the wet isotropic and anisotropic etching of the exposed sacrificial metal layer and the CMOS substrate for a controlled amount of time, respectively, as shown in Fig. 4.8. By removing the sacrificial metal layer, an air gap is created between the plates of the MEMS structure. The metal mask that is used during the first RIE of the CMOS dielectric layer will also be removed during this step. Release holes on the top plate of the MEMS structure are required in order to facilitate the wet etching of the sacrificial aluminum layer. For the wet etching, solutions of (16:1:1) phosphoric-acetic-nitric (PAN) etch and

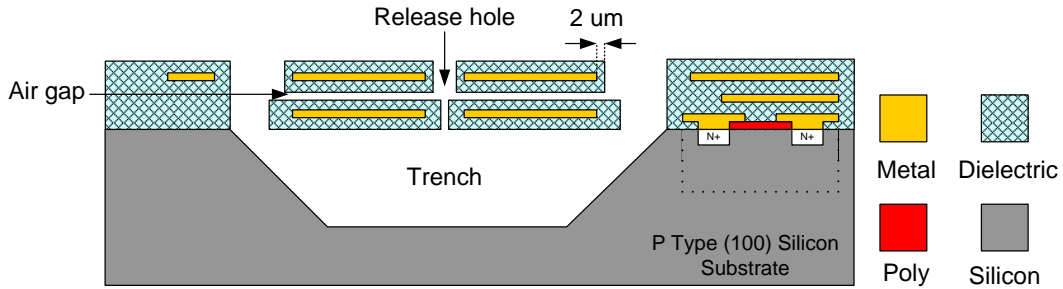


Figure 4.8: Wet etching of the sacrificial layer and the silicon substrate.

60% diluted potassium hydroxide (KOH) at 40°C for 15 min and 30% hydrogen peroxide (H₂O₂) at 60°C for 30 min were applied. The KOH solution is used in order to remove the remaining piles of silicon inside the trench, left after the RIE of the silicon substrate and also to increase the depth of the trench under the MEMS structure. Alternatively, diluted 5% electronic grade tetra methyl ammonium hydroxide (TMAH) at 80-85°C can be used instead of KOH. During the wet etching of the sacrificial layer, the structural metal layers (e.g. M₃ and M₁) are protected from being etched by the wet etchant using a dielectric layer surrounding these layers. This is accomplished by extending the RIE metal mask (e.g. M₄) over the top of the structural metal layers by at least 2 μm as shown in Fig. 4.4. On the other hand, wherever an air gap is required, the sacrificial layer is extended beyond the RIE mask and exposed after the RIE of the CMOS dielectric layer. After the wet etching step, the CMOS dies are placed in a CO₂ critical point dryer (CPD) system to avoid any stiction problem of the released MEMS structures.

The final post-processing step is the second RIE of the oxide layer on top of the pads for electrical contact and also on top of the plates of the MEMS structure to reduce the stiffness and the required DC actuation voltage. The same oxide RIE recipe as in Table 4.1 was used for this step. Fig. 4.9 shows the CMOS die after this processing step. An SEM image of a MEMS structure fabricated using the developed CMOS-MEMS processing is presented in Fig. 4.10.

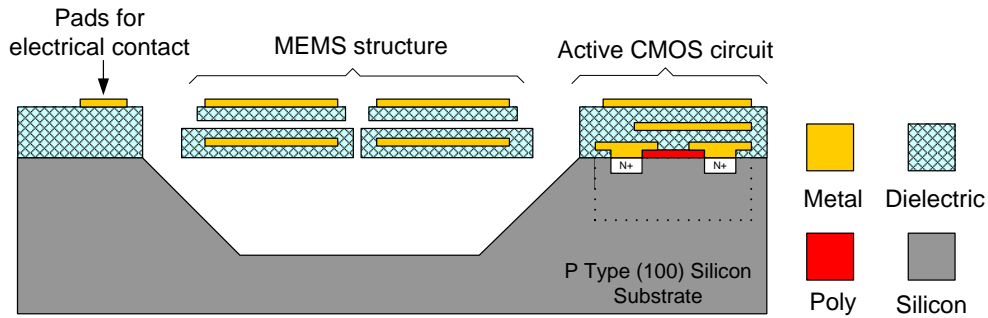


Figure 4.9: CMOS chip after the second RIE of the CMOS dielectric layer.

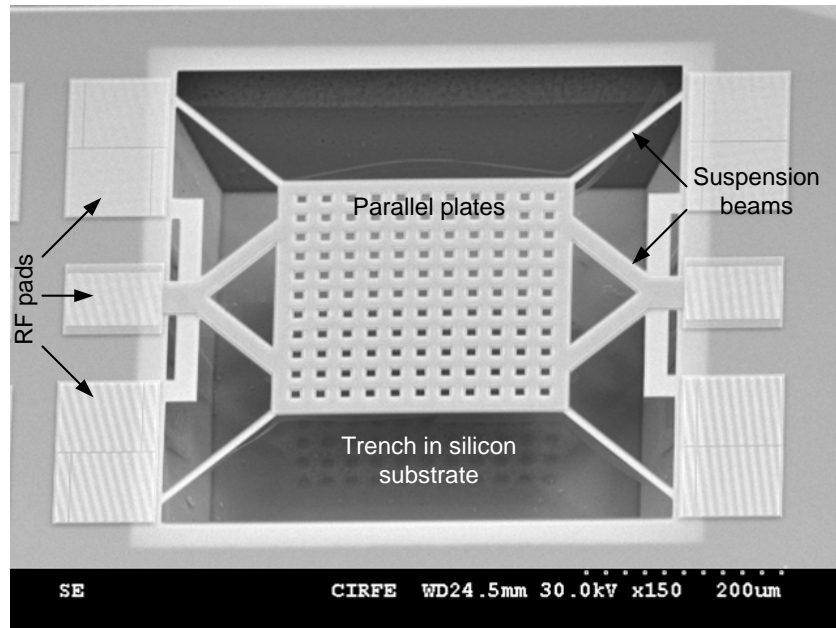


Figure 4.10: SEM image of a MEMS tunable capacitor with parallel-plate structure fabricated using the CMOS-MEMS processing.

4.3 CMOS-MEMS Tunable Capacitors

CMOS-MEMS tunable capacitors were fabricated using the developed CMOS-MEMS processing [77], [78]. These capacitors have an excellent quality factor compared to the semiconductor varactors at high RF frequencies and have a small area and can be utilized in

fully integrated multi-band RF front-ends. The fabricated tunable capacitors are used as the tuning elements within an integrated tunable bandpass filter which is presented in section 4.4. Both the RF simulation and measurement results are presented in this section. Figure 4.11 presents the layout of the tunable MEMS capacitor fabricated using the 2P4M TSMC 0.35- μm CMOS technology and by employing the CMOS-MEMS processing at the University of Waterloo.

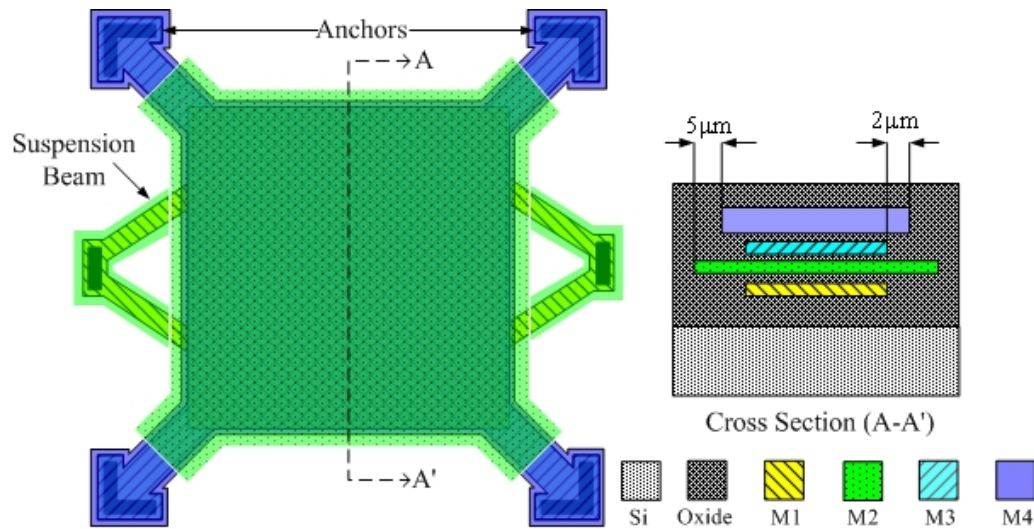
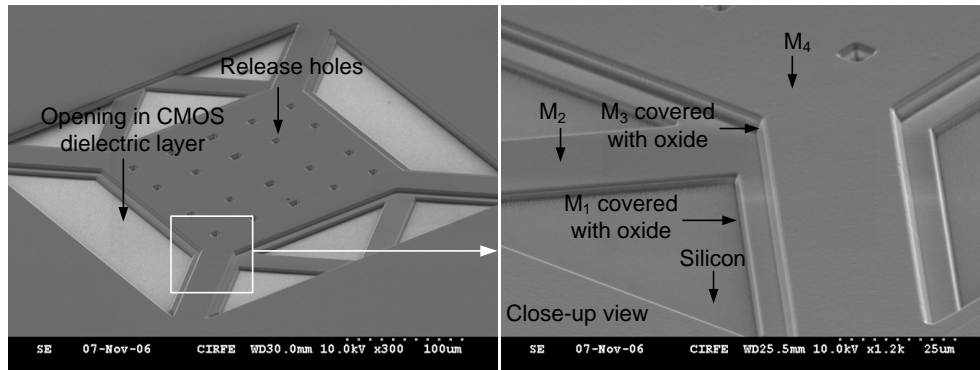


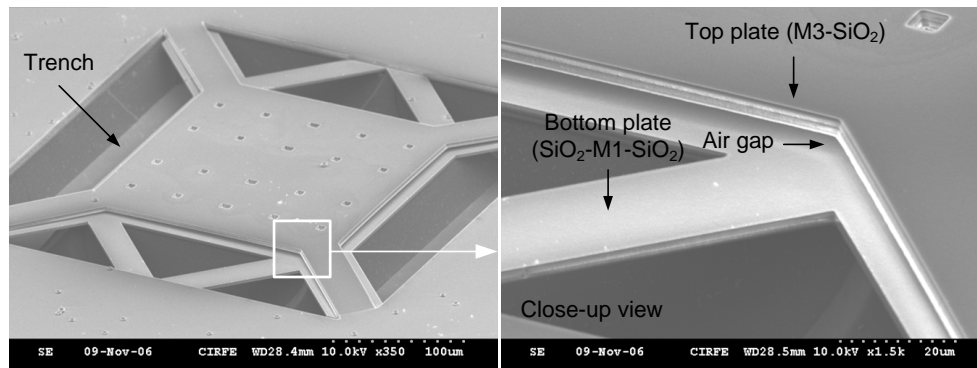
Figure 4.11: Layout and cross-section view of the parallel-plate MEMS capacitor fabricated using the 2P4M 0.35- μm CMOS process.

The top and bottom plates of the capacitor are made of M_3 and M_1 layers respectively, and the second metal layer M_2 that is 0.6 μm thick is used as the sacrificial layer. This metal layer will be removed after the CMOS-MEMS processing to create the air gap between the plates. The total gap between the plates, after release, consists of two SiO_2 layers with a thickness of 1 μm and a 0.6 μm air gap. The oxide dielectric layer prevents the occurrence of a short circuit when the DC actuation voltage exceeds the pull-in voltage of the MEMS capacitor. Fig. 4.12 shows SEM images of the fabricated CMOS-MEMS tunable capacitor. As shown in this figure, the capacitor includes a 100 μm air trench in the silicon substrate

and under the bottom plate. This trench will improve the RF performance and the quality factor Q of the capacitor by removing the parasitic effects of the low-resistivity (8-12 Ωcm) silicon substrate commonly used in standard CMOS process. The substrate loss is mainly due to the eddy currents present at high frequencies inside the silicon substrate.



(a)



(b)

Figure 4.12: SEM image of the MEMS capacitor (a) after removing the CMOS dielectric layer and (b) after all the CMOS-MEMS processing steps.

RF simulations of the capacitor were performed in HFSS. Fig. 4.13 shows the extracted capacitance value over a frequency range from 1-15 GHz for the the CMOS-MEMS tunable capacitor shown in Fig. 4.12. The area of the plate is $200 \times 200 \mu\text{m}^2$. The capacitance value for the up-state, C_u , when the DC actuation voltage is zero, is 0.377 pF. The maximum

capacitance value after the top plate is pulled down on the bottom plate, by applying a DC actuation voltage higher than the pull-in voltage, is $C_d = 0.944$ pF at 10 GHz. The simulated quality factor Q of the capacitor is above 20 from 5 GHz up to 10 GHz.

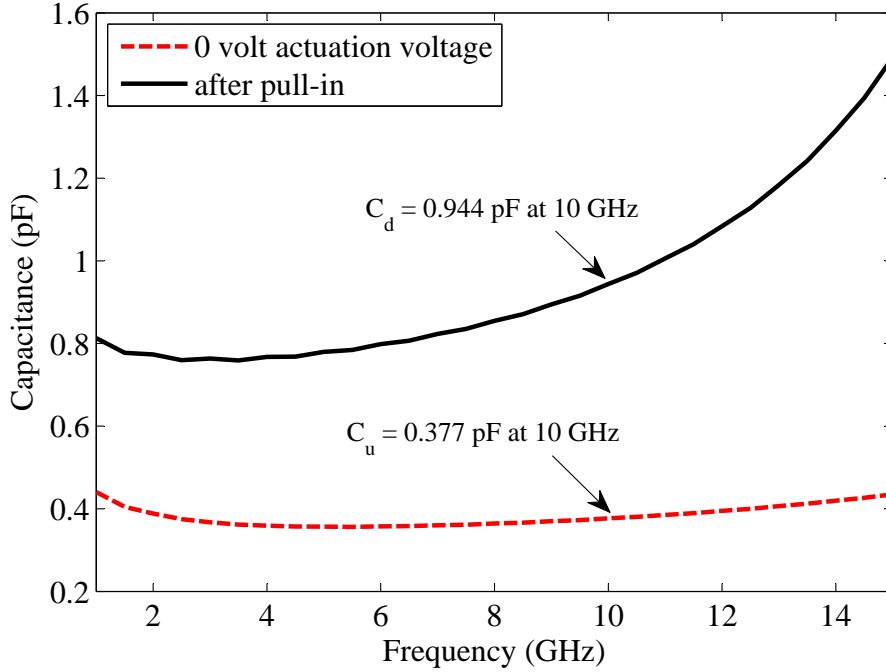


Figure 4.13: Simulated capacitance value of the CMOS-MEMS capacitor.

One port on-wafer measurement of the tunable capacitor is performed using an HP8722ES vector network analyzer and Cascade RF probe station. The capacitance value is extracted by fitting the measured S_{11} parameter of the device to an equivalent series RC circuit in ADS for different DC actuation voltages. Fig. 4.14 shows the extracted capacitance value over a frequency range from 1 to 15 GHz. At 10 GHz, the measured capacitance value is found to be 0.23 pF. The simulated capacitance value as shown in Fig. 4.13 is 0.377 pF. The difference between the HFSS simulation and the measured result is attributed to the deflection of the top plate after CMOS-MEME processing. This is due to the residual stress gradient present in the composite Al/SiO₂ layer forming the top plate of the capaci-

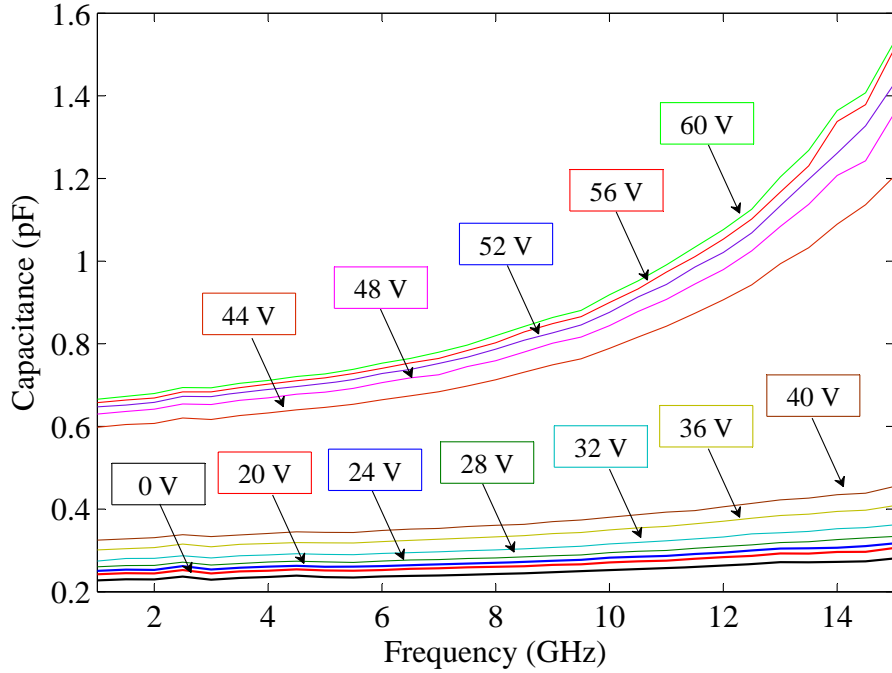


Figure 4.14: Measured capacitance value of the CMOS-MEMS capacitor for different DC actuation voltages.

tor. Characterization of the residual stress values in the aluminum and oxide layers of the 0.35- μm CMOS process will be explained in Section 4.5. Fig. 4.15 shows the simulated deflection of the top plate of the capacitor using CoventorWare software. A stress gradient value of $\sigma_{mis} = 145$ MPa inside the composite Al/SiO₂ layer is used for simulation. The deflection profile of the fabricated capacitor is also measured using an optical interferometer WYKOTM. A maximum deformation of 1.9 μm is measured which is in a close agreement with the CoventorWare simulation result. This explains the difference between the measured and simulated capacitance values.

The measured capacitance versus the DC actuation voltage at 10 GHz is presented in Fig. 4.16. As seen in this figure, the measured pull-in voltage, V_{pi} , for this capacitor is 43 Volts. The maximum capacitance before pull-in is 0.38 pF, and the capacitor demon-

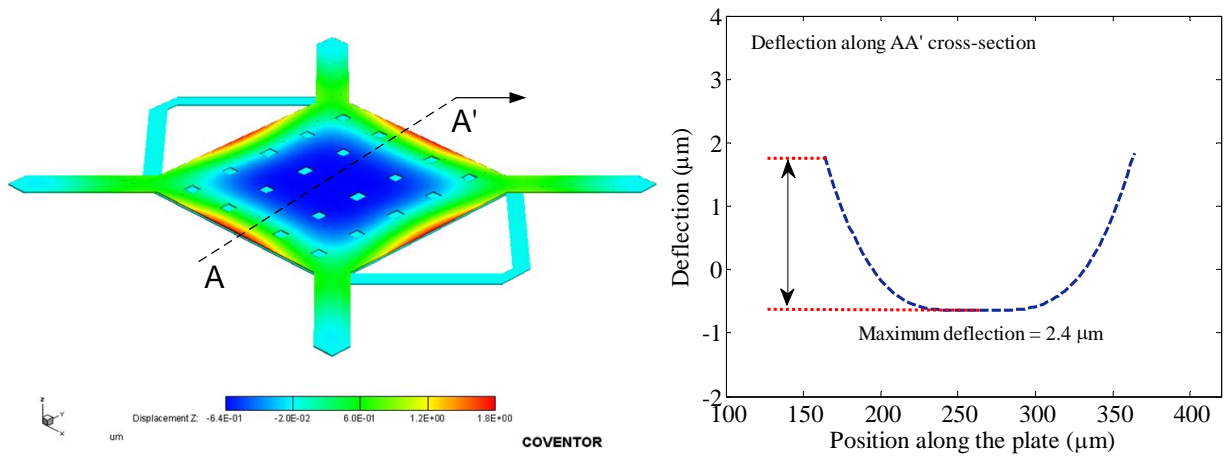


Figure 4.15: Simulated deflection profile of the top plate of the CMOS-MEMS capacitor due to the residual stress gradient in the Al/SiO₂ layer.

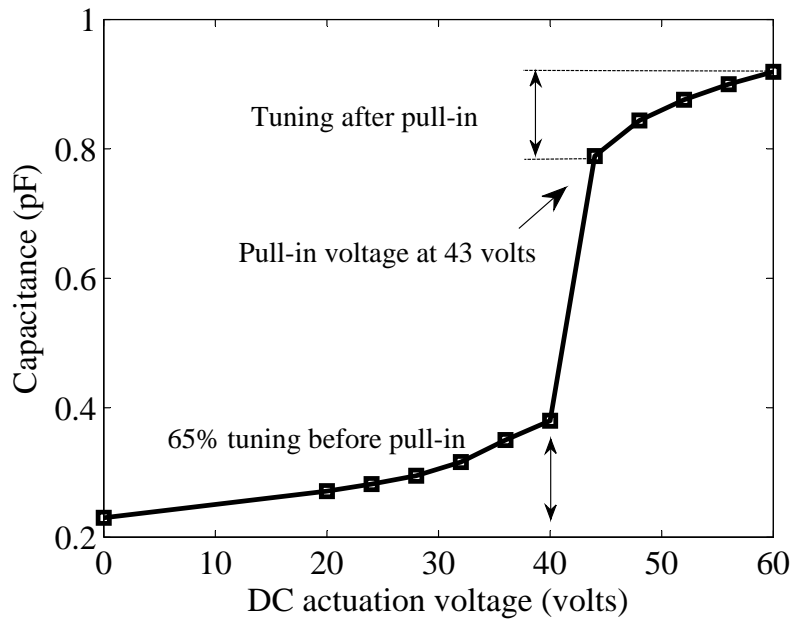


Figure 4.16: Extracted capacitance versus DC actuation voltage at 10 GHz.

strates a linear tuning range of approximately 65% before pull-in happens. The measured capacitance right after pull-in is 0.79 pF. The capacitance still increases with increasing the actuation voltage beyond 43 Volts, and this extends the tuning range of the capacitor beyond the 50% tuning limit of a conventional parallel-plate capacitor. This is due to the fact that both the top and bottom plates are movable. The existence of a second movable plate will increase the tuning range as reported in [79]. The maximum tuning range of the proposed capacitor is measured to be 296% at 10 GHz for a DC actuation voltage of 60 Volts.

The quality factor of the capacitor is determined from the measured S_{11} parameter and using the real and imaginary components of the extracted input impedance. As shown in Fig. 4.17, the measured quality factor is above 18 for a frequency range from 1 GHz up to 10 GHz which is considered to be higher than the previously reported CMOS-MEMS

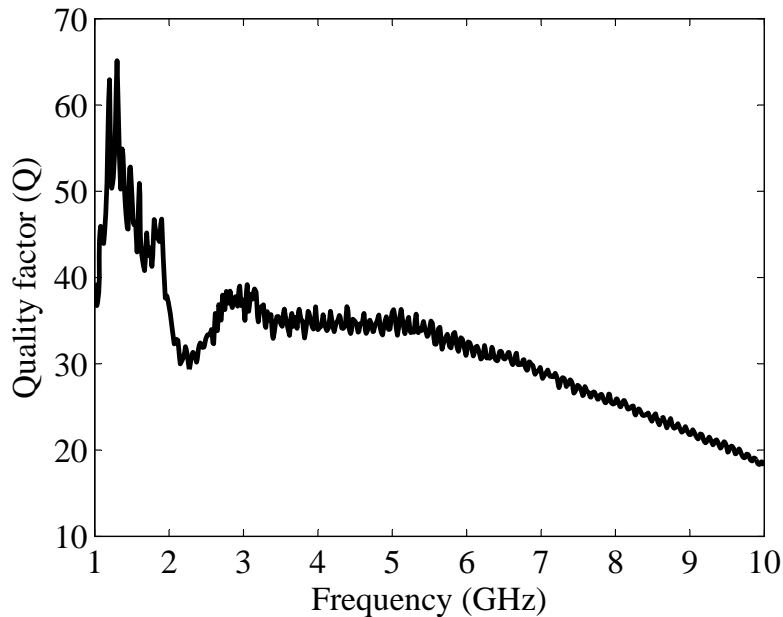


Figure 4.17: Measured quality factor of the CMOS-MEMS tunable capacitor.

tunable capacitors with comb-finger structure [34]. This high quality factor is due to the cancelation of the substrate loss and its parasitic effects at higher RF frequencies. Another important effect of removing the silicon substrate is the improved self-resonance frequency. The measured self resonance frequency is higher than 15 GHz.

Other types of CMOS-MEMS tunable capacitors including a tri-state capacitor with digital-type tuning and also an analog-type tunable capacitor with a continuously linear tuning characteristic were also fabricated using the developed CMOS-MEMS processing [77]. A comparison of the developed CMOS-MEMS tunable capacitors with the state of the art semiconductor MOS varactors is presented in Table 4.3. The only other MEMS tunable capacitor integrated in a standard CMOS technology, reported by Oz et. al. [34], [84], is based on a comb finger beam structure and electro-thermal actuators were used for tuning. The parallel-plate CMOS-MEMS tunable capacitor presented in this section have

Table 4.3: Comparison between the developed CMOS-MEMS tunable capacitors and MOS varactors in CMOS technology.

publication	C_{min}	Tuning ratio	Quality factor Q	$V_{tune}/power$	Technology
Ref. [80]	0.1 pF	12	<20 @ 5.8GHz	-1.5 to +1.5V	65-nm CMOS
Ref. [81]	NA	6.2	7.7 @ 10GHz	-1 to +1V	0.13- μ m CMOS
Ref. [82]	NA	2.7~ 3.4	30~40@ 2.4GHz	NA	90-nm CMOS
Ref. [83]	20 fF	5.2	~20@ 10GHz	-1 to 1V	90-nm CMOS
Ref. [34]	42 fF	3.52	52 @ 1.5GHz	12V/34mW	0.35- μ m CMOS-MEMS
this work [78]	0.23 pF	3.96	18 @ 10GHz	60V/0W	0.35- μ m CMOS-MEMS
this work [77] (digital-type)	0.3 pF	5.6	300 @ 1.5GHz	70V/0W	0.35- μ m CMOS-MEMS
this work [77] (analog-type)	0.8 pF	2.15	300 @ 1.5GHz	52V/0W	0.35- μ m CMOS-MEMS

a higher capacitance value with better Q factor, smaller size and near to zero DC power consumption using electrostatic actuation instead of thermal actuators compared to the tunable capacitor in [34].

4.4 Microwave Tunable Bandpass Filter Integrated in CMOS Technology

Tunable filters are among the reconfigurable blocks that if integrated with RF CMOS electronics can reduce the overall system size, weight and cost. A number of integrated tunable filters have been demonstrated using solid-state tuning elements [85]. Despite the small area and high switching speed of the active tuning elements, the major disadvantage is their susceptibility to noise and lower power handling due to nonlinearities in the active semiconductor devices. Using CMOS-MEMS technology, it is possible to replace these active components with passive RF MEMS tuning elements possessing superior RF

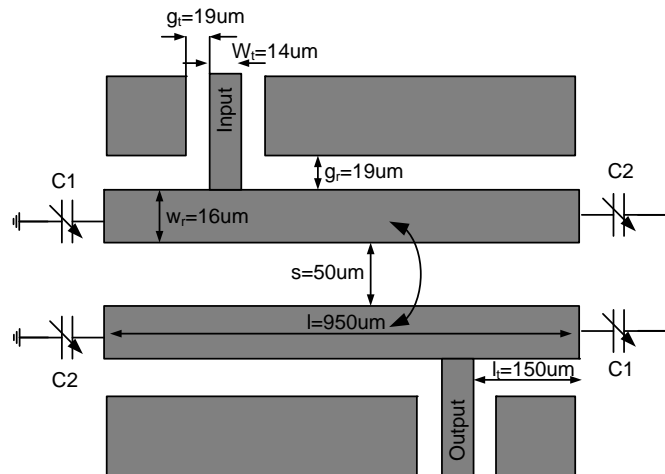


Figure 4.18: Layout of the 2-pole interdigital bandpass filter with CMOS-MEMS tunable capacitors.

performance in terms of linearity, tuning range, loss, and power handling.

The design and fabrication of an integrated tunable bandpass filter is presented in this section. This filter is designed with the benefit of novel parallel-plate tunable CMOS-MEMS capacitors presented in the previous section. The filter is realized as a 2-pole capacitively loaded interdigital filter with tapped line input and output coupling as shown in Fig. 4.18. The effective electrical length of each resonator and also the length l_t measured from the resonator ground to the tap point can be tuned using the CMOS-MEMS tunable capacitors. This enables the tuning of the filter's center frequency and bandwidth together. Interdigital bandpass filter design techniques [86], [87] are used to design a 2-pole Tchebychev filter with a center frequency of 10 GHz, a fractional bandwidth of 10%, and 0.1 dB ripple in the pass-band. HFSS 3D finite element EM simulator was used to find the dimensions of the filter as shown in Fig. 4.18. The characteristic impedance of the input and output CPW feed-lines is set to 50Ω . The coupled resonator sections are $950 \mu\text{m}$ long and separated by $50 \mu\text{m}$ producing even and odd mode characteristic impedances of 54Ω and 46Ω , respectively. The effective electrical length of each resonator section

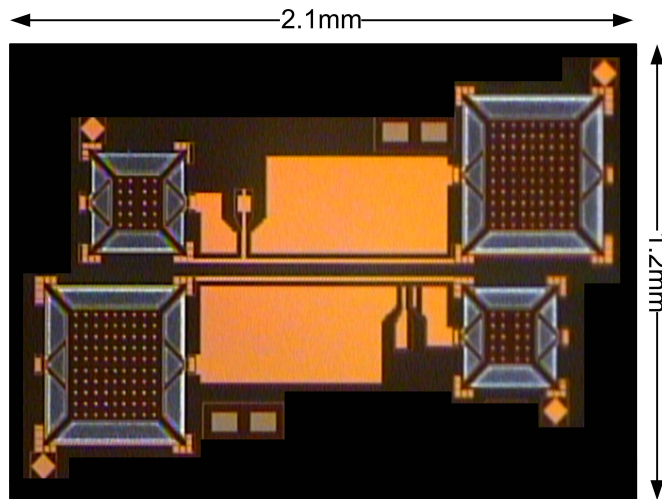


Figure 4.19: Optical photograph of the integrated tunable bandpass filter.

loaded with two capacitors is 45° at the filter's center frequency. The capacitance values were determined using optimization tools in Agilent ADS. The capacitance values for C_1 and C_2 at zero DC actuation voltage are 0.23 pF and 1.8 pF, respectively. Knowing the initial gap between the plates and a capacitance value of 1.8 pF, the area of the capacitor is calculated to be only $367 \times 400 \mu\text{m}^2$ leading to the compact implementation of the proposed tunable band-pass filter. An optical micro-photograph of the fabricated filter is shown in Fig. 4.19. The size of the fabricated filter is only $1.2 \times 2.1 \text{ mm}^2$ including all the tuning elements, RF pads, and the dc bias pads for tunable capacitors.

A DC actuation voltage ranging from 0 to 60 volts is applied through the bias pads to tune the filter. Fig. 4.20 shows the simulated and measured insertion and return loss of the filter at 0 volts. There is a good agreement between the measurement and simulation results. At 0 volts, the minimum insertion loss is measured to be 5.66 dB with a bandwidth

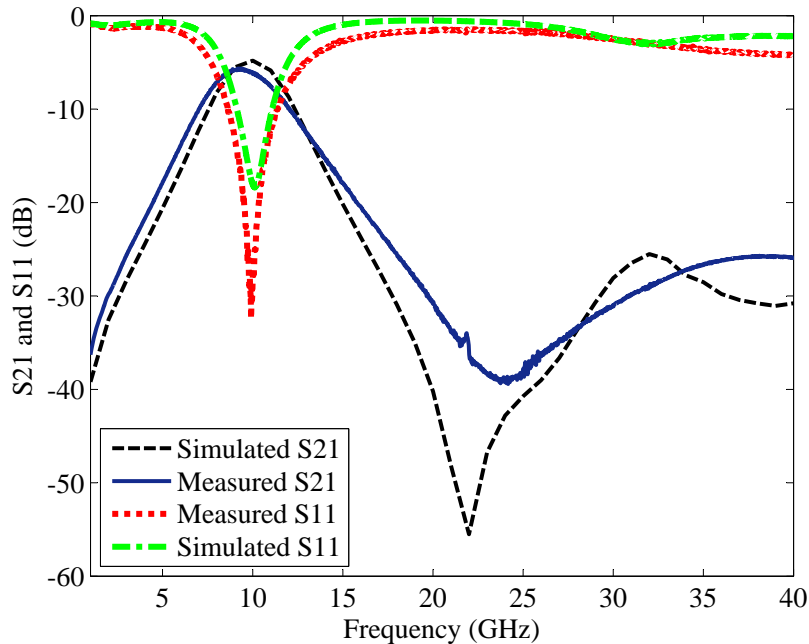


Figure 4.20: Simulated and measured insertion and return loss at 0 volt.

of 0.86 GHz (9%) and a return loss better than 20 dB.

The capacitor set C_2 shown in Fig. 4.18 is used to change the center frequency by varying the effective electrical length of each resonator section, whereas the second set C_1 tunes the input/output coupling by changing the tapping location. Using these two sets of tunable capacitors it is possible to tune the filter center frequency while maintaining a constant bandwidth. As shown in Fig. 4.21, when only C_2 is used for tuning, the bandwidth is reduced from 955 MHz to 764 MHz after tuning while using both sets of capacitors the bandwidth remains almost the same.

Measured insertion loss and return loss for different bias voltages ranging from 0 to 40 volts are shown in Fig. 4.22. The mid-band insertion loss ranges from 5.66 dB to 5.95 dB

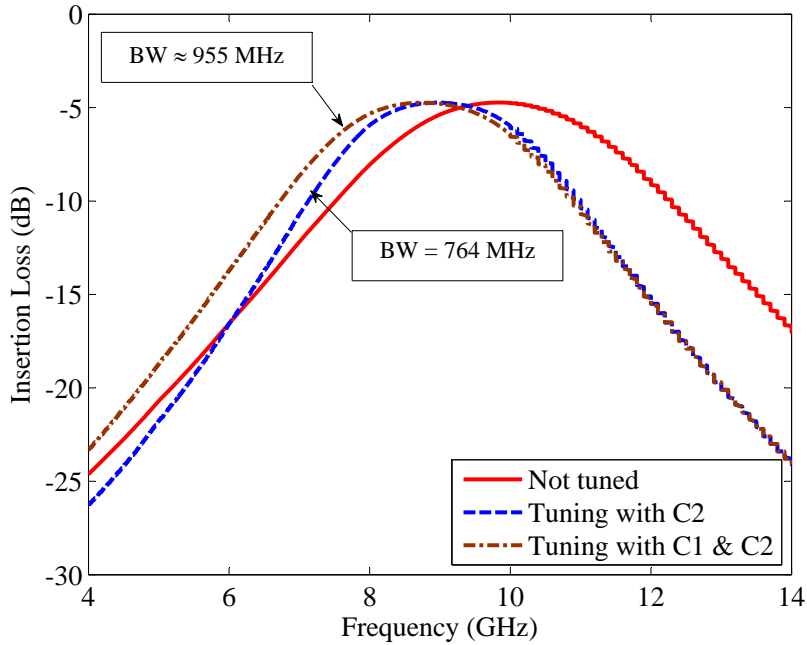
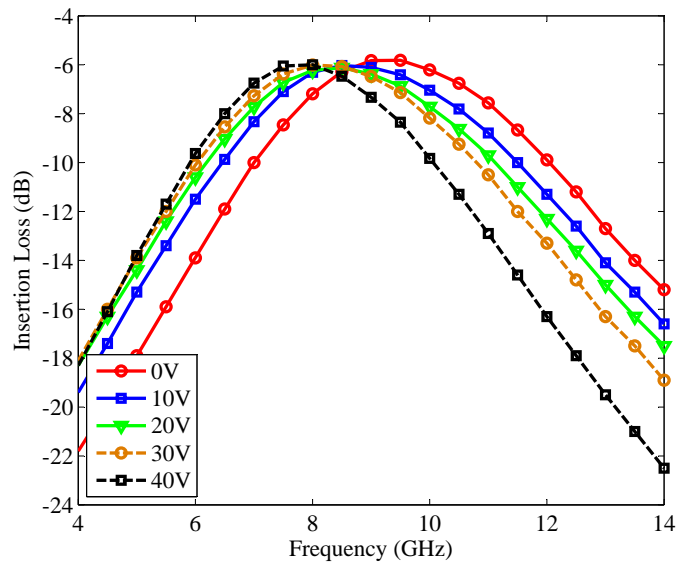
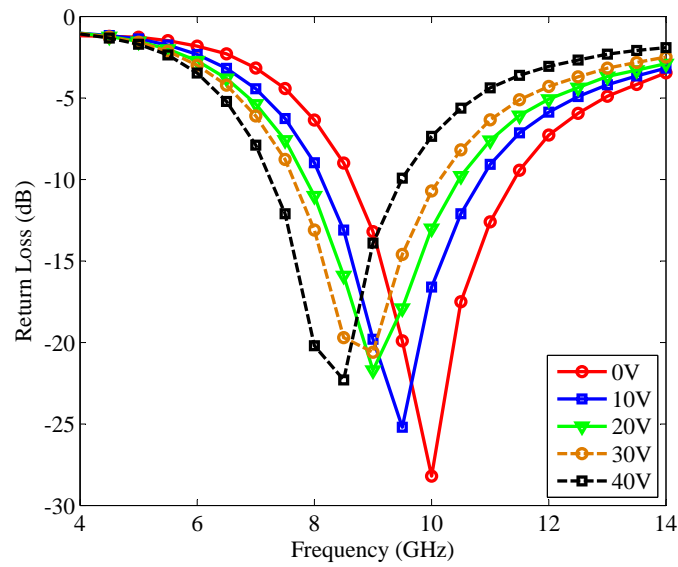


Figure 4.21: Simulation results for tuning the filter center frequency which illustrates the need to use both sets of capacitors to maintain a constant bandwidth.



(a)



(b)

Figure 4.22: Measured (a) insertion loss and (b) return loss of the tunable filter for different DC actuation voltages.

and the tuning range is measured to be 1.6 GHz (17%) with a constant bandwidth of 855 MHz.

4.5 Capacitive RF MEMS Switches Fabricated using Standard CMOS Technology

4.5.1 Introduction

RF MEMS switches offer a good RF performance, low DC power consumption, light weight, better linearity and low intermodulation products at millimeter-wave frequencies [88] and can be used in multiband RF transceivers. However, the existing MEMS-based multiband RF transceivers incorporate off-chip MEMS switches and have not led to a fully integrated silicon solution using a commercially available low cost standard CMOS process.

There has been efforts to monolithically integrate RF MEMS switches with active CMOS circuitry by several researchers. RF MEMS switches fabricated using a CMOS-compatible MEMS fabrication process and stacked on a CMOS chip was reported in [31]. An alternative CMOS-MEMS integration approach was pioneered by Fedder et. al. to create electrostatically actuated microstructures with high aspect ratio composite beam structures [32], [71]. A capacitive series type RF MEMS switch using this integration approach was reported in [41]. The switch is thermally actuated and has a comb-finger structure for the capacitive coupling between the input/output RF ports. The maximum reported capacitance ratio of the switch is limited to 15:1. Moreover, thermal actuators consume high DC power for actuation; therefore, they require latching mechanisms adding to the complexity of the RF MEMS switch design and increasing the chip real state.

In this section, novel CMOS-MEMS capacitive shunt-type switches for microwave and millimeter-wave applications are demonstrated [89]. The switches are based on a warped-

plate structure increasing the capacitance ratio. Electrostatic actuation is utilized to reduce the DC power consumption. The switch is implemented using the standard 0.35- μm CMOS process and the mask-less CMOS-MEMS processing developed for the fabrication of parallel-plate electrostatically actuated microstructures at the University of Waterloo. A capacitance ratio of 91:1 is achieved for the fabricated switches. An insertion loss better than 1.41 dB and an isolation of 19-40 dB from 10 to 20 GHz is demonstrated. The proposed switches can be used in reconfigurable CMOS RF front-ends.

4.5.2 Switch Design

Fig. 4.23 shows the top view and the cross-sectional view of the shunt capacitive RF MEMS switch implemented using the standard 0.35- μm CMOS process. The switch consists of a coplanar waveguide (CPW) transmission line section and two warped plates anchored on the center conductor and suspended on top of the ground conductors of the CPW line. As shown in the cross-sectional view of Fig. 4.23(b), the warped plates consist of a composite Al/SiO₂ layer. The warping of the plates after releasing the MEMS switch is due to the difference in the residual stress of the constituent metal and dielectric layers. The warped plates form an RF capacitance between signal and ground; C_u when the plates are up and C_d when the plates are pulled down on the ground conductors. The warped plate structure is used in order to decrease the up-state capacitance while enhancing the down-state capacitance. This will increase the capacitance ratio

$$C_r = C_d/C_u \quad (4.1)$$

The actuation electrodes are placed inside the gap between the CPW signal and ground conductors and separated from the RF ports. To actuate the switch a DC bias voltage, V_b , is applied between the actuation electrodes and the warped plates. The bias voltage

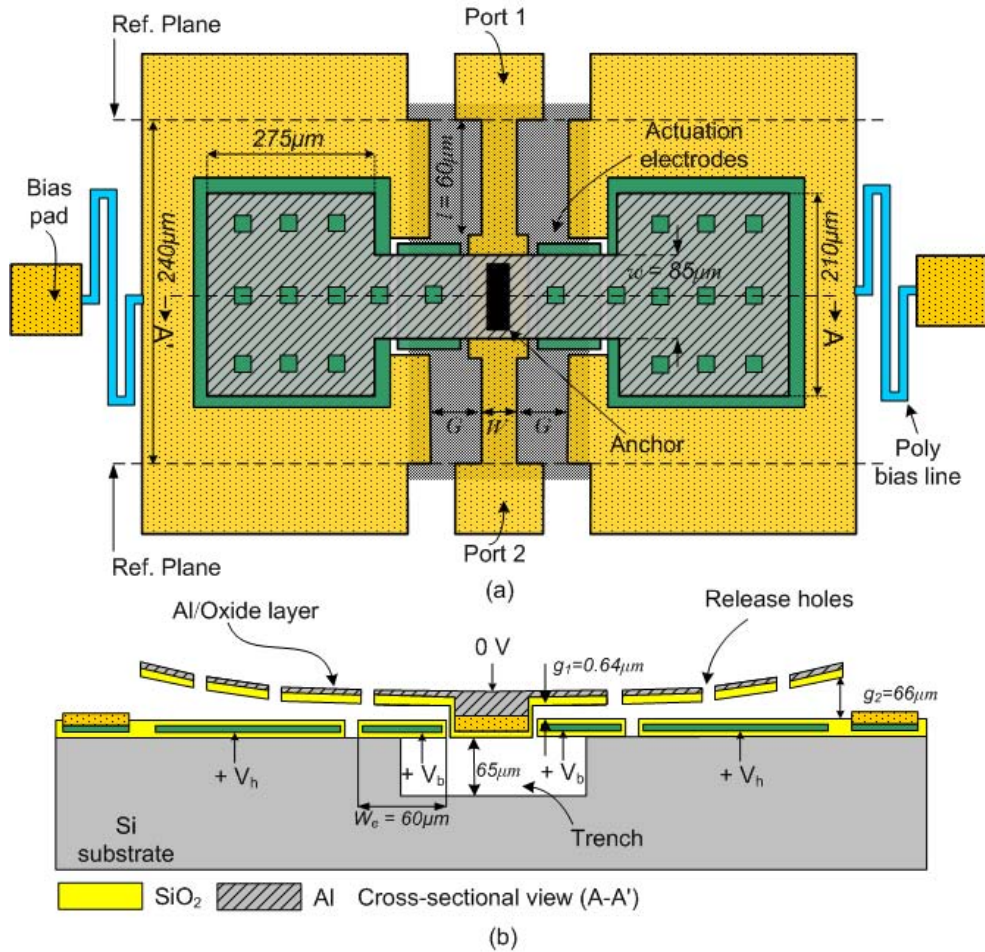


Figure 4.23: (a) Top view and (b) cross-sectional view of the shunt capacitive CMOS RF MEMS switch.

is provided through high-resistivity polysilicon lines. The air gap between the actuation electrodes and the warped plates is maintained as small as possible to decrease the actuation voltage V_b . A second lower DC bias voltage V_h is applied between the signal and ground conductors and through the RF ports to bring the switch to the down-state position. The switch also includes a $65 \mu\text{m}$ air trench in the silicon substrate and under the signal conductor. This trench will improve the RF performance and the insertion loss of the switch by removing the parasitic effects of the low-resistivity ($8\text{-}12 \Omega\text{cm}$) silicon substrate

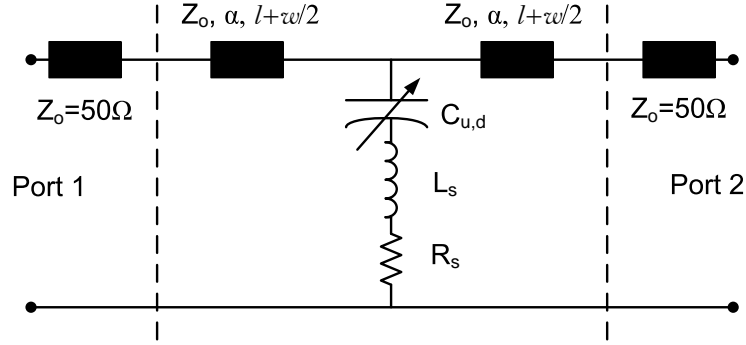
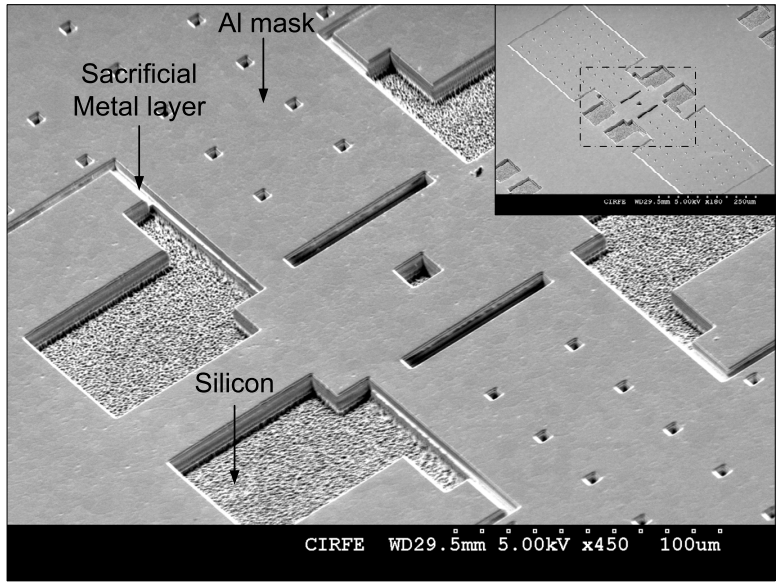


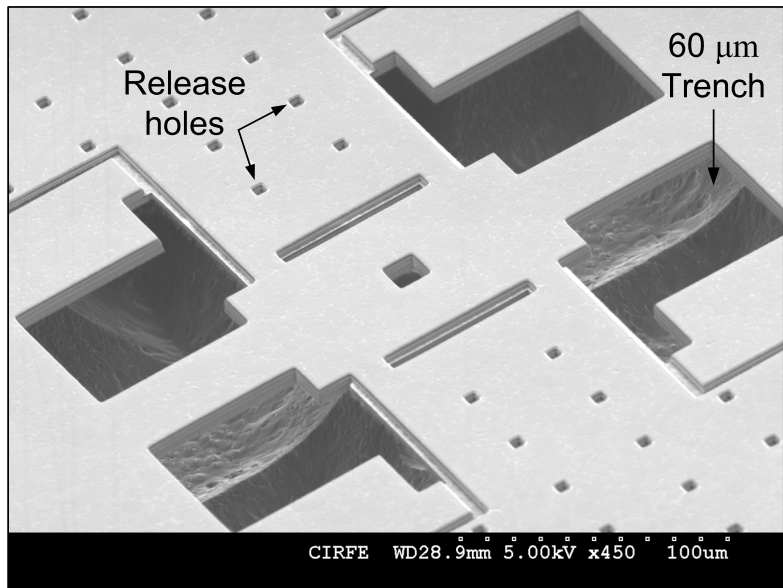
Figure 4.24: Equivalent circuit diagram of the shunt capacitive CMOS RF MEMS switch.

commonly used in standard CMOS processes. The substrate loss is mainly due to the eddy currents present at higher frequencies inside the silicon substrate.

The switch consists of two $210 \mu\text{m} \times 275 \mu\text{m}$ warped plates suspended over a CPW line with dimensions of $G/W/G = 60/30/60 \mu\text{m}$ and a characteristic impedance $Z_o = 102 \Omega$. As shown in the equivalent circuit model of Fig. 4.24, the warped plates are presented by a series capacitor-inductor-resistor (CLR) model terminated by two sections of transmission lines with a length of $l + w/2$ where $l=60 \mu\text{m}$ is the distance from the edge of the warped plates to the reference lines and $w=85 \mu\text{m}$ is the width of the warped plates at the anchor point. For the up-state, the impedance of the switch is approximated by the small shunt capacitance of the switch, C_u . The characteristic impedance of the loaded CPW line in the up-state position of the switch is close to 50Ω . When the switch is actuated, the shunt capacitance is increased to C_d , creating an RF short between the signal and ground. The equivalent circuit model parameters can be obtained using the electromagnetic simulations and also by fitting measured S-parameters of the switch using the modeling approach presented in [90] and will be discussed in a later section.



(a)



(b)

Figure 4.25: SEM image of the switch after (a) removing the CMOS dielectric layer using RIE and (b) the isotropic RIE of the Si substrate.

4.5.3 Fabrication

The proposed CMOS RF MEMS switches are fabricated using the standard 2P4M 0.35- μm CMOS process from TSMC (Taipei, Taiwan) and then processed by optimizing the CMOS-MEMS process previously used for the fabrication of RF MEMS tunable capacitors. Fig. 4.25(a) presents the switch after removing the CMOS dielectric layer around the MEMS structure using a CF_4/H_2 plasma etch recipe. After this step both the sacrificial metal layer and the silicon substrate around the MEMS devices will be exposed for subsequent etching. Fig. 4.25(b) shows the switch after isotropic RIE of silicon in an SF_6/O_2 plasma to create the 60 μm trench under the signal lines. This is followed by the wet etching of the sacrificial layer and release of the warped plates and the second oxide RIE to open the pads and remove the oxide on top of the warped plates. Fig. 4.26 shows an SEM image of the final fabricated CMOS RF MEMS switch after all the CMOS-MEMS processing steps.

4.5.4 Mechanical Simulation Results

Residual stresses present in the constituent metal and dielectric layers of the CMOS process which are induced by thermal mismatch cause warping of the plates of the proposed RF MEMS switch. This property is used to increase the capacitance ratio of the switch. To illustrate this concept, finite element analysis with CoventorWare was performed to simulate the warpage of the switch's top plates. The RF performance of the switch was also simulated using Ansoft HFSS software.

As shown in the cross-sectional view of the composite metal-dielectric layer in Fig. 4.27, the bilayer warped plates of the switch are subjected to residual stresses generated from the fabrication process. The biaxial residual stress in the top Al layer is assumed to be tensile while that in the bottom oxide layer is compressive throughout the thickness of the oxide layer.

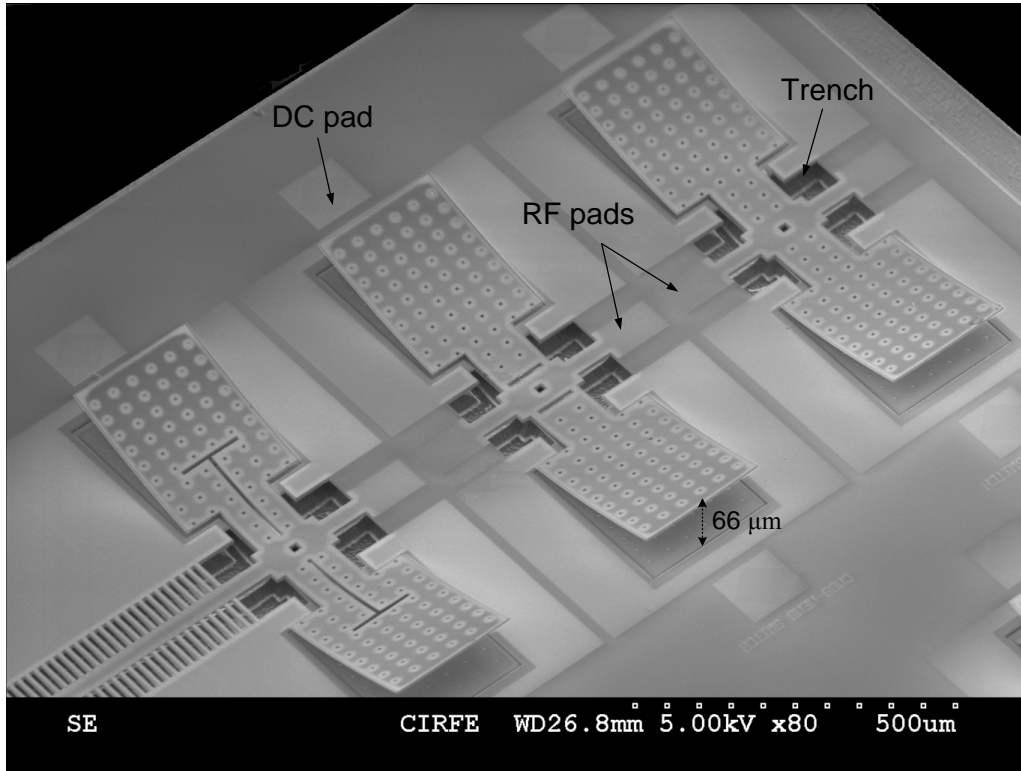


Figure 4.26: SEM image of the fabricated CMOS RF MEMS switches.

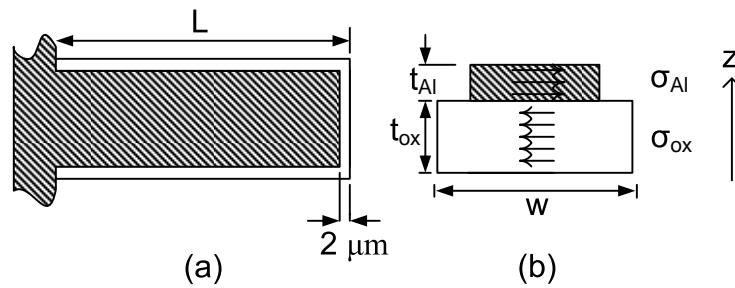


Figure 4.27: (a) Top view and (b) cross-section of the composite Al/SiO₂ cantilever beams used to extract residual stress components of each layer.

The accurate characterization and control of the stress-induced warpage is essential for the design and implementation of the proposed switch. The residual stress values of each layer is determined by conducting experiments on the stress-induced bending of bilayer

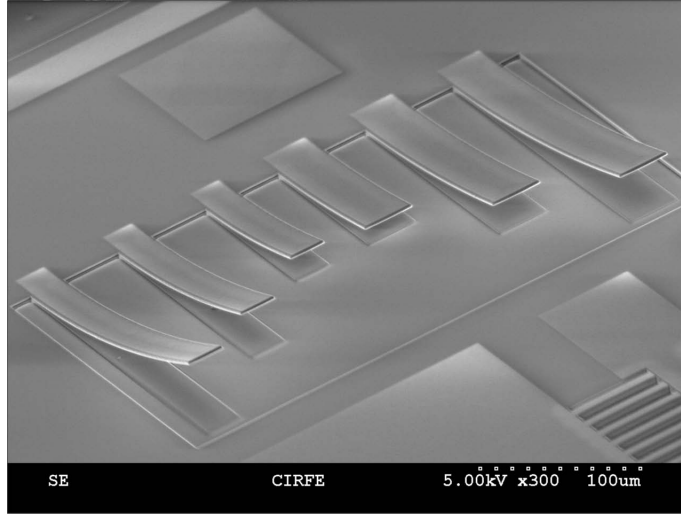


Figure 4.28: SEM image of the cantilever beams used as test structures for stress analysis.

cantilever beams. Fig. 4.28 shows the SEM image of an array of released cantilever beams with lengths from 100 μm to 200 μm used as test structures for stress analysis. The curvature-based approach presented in [91], [92], [93] is used to derive the residual stress values present in the oxide and aluminum layers of the CMOS process.

The warped plates of the proposed CMOS-MEMS switch consist of the same composite Al/SiO₂ layer as the cantilever beams shown in Fig. 4.27. The bending curvature of this bilayer structure is related to the residual stress values by [91]

$$\kappa = \frac{1}{E_{ox}t_{ox}} \frac{6r(1+r)\sigma_{mis}}{1 + 4\gamma r + 6\gamma r^2 + 4\gamma r^3 + \gamma^2 r^4} \quad (4.2)$$

where E denotes Young's modulus, $\gamma = E_{Al}/E_{ox}$ is the modulus ratio, $r = t_{Al}/t_{ox}$ is the thickness ratio, and $\sigma_{mis} = \sigma_{Al} - \gamma\sigma_{ox}$ represents the difference in the residual stress values for the aluminum and oxide layers.

The measured deflection profile of a 156 μm long and 30 μm wide Al/SiO₂ cantilever beam using an optical interferometer WYKOTM is shown in Fig. 4.29. The measured deflection profile d is then decomposed into *tilt* and *curl* components induced from the

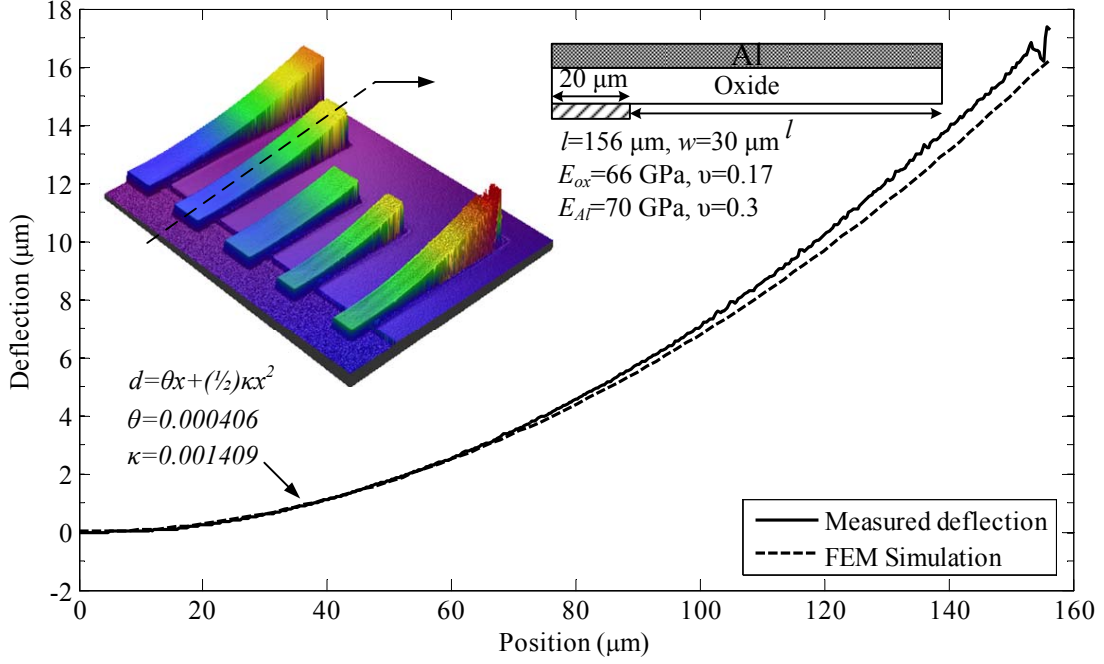


Figure 4.29: Measured deflection profile of the bilayer cantilever beam and FEM simulation result for $\sigma_{mis}=144.74$ MPa.

mean and stress gradient components, respectively [93].

$$d = \theta x + \frac{\kappa}{2} x^2 \quad (4.3)$$

where x is the position along the beam, θ represents the angular tilt and κ is the bending curvature which are determined by curve fitting of the measured deflection profile. The stress gradient obtained from different cantilevers is averaged to be $\sigma_{mis} = 144.74$ MPa and the standard deviation is calculated to be 2.1 MPa. As illustrated in Fig. 4.29, the measured deflection profile agrees with the simulation results using CoventorWare and the determined residual stress gradient in the FEM model.

Fig. 4.30 shows the final FEM simulation result for the warpage of the proposed CMOS-MEMS switch. The maximum simulated tip deflection of the warped plates is $59 \mu\text{m}$. By comparison between the maximum deflection of the top plate using the FEM simulation

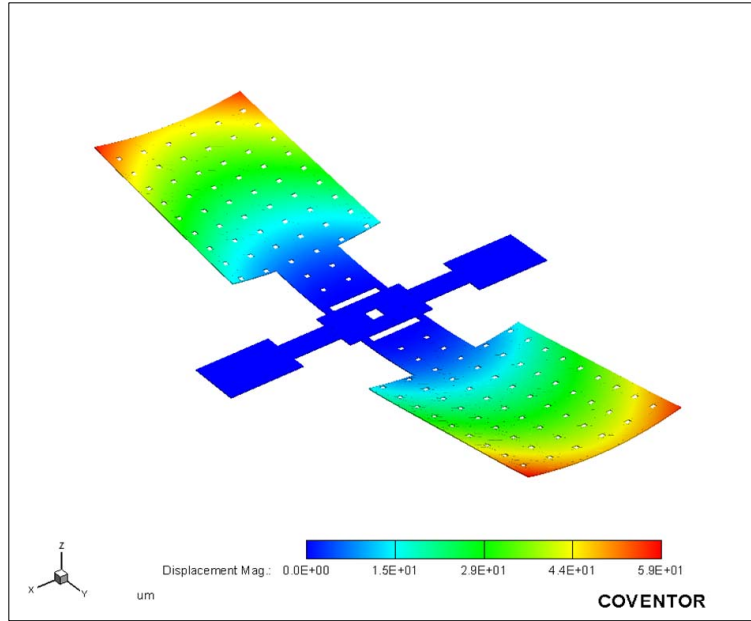


Figure 4.30: FEM simulation result for the fabricated CMOS-MEMS switch with warped plates using the determined residual stress values, the maximum deflection of the top plate is simulated to be 59 μm .

result and the measured maximum deflection of 66 μm as shown in the SEM image of Fig. 4.26, we can see that by using the extracted residual stress values present in the oxide and aluminum layers we are able to closely predict the warpage of the fabricated device.

Coupled-field electro-mechanical simulation was also performed with CoventorWare to evaluate the actuation voltage of the switch. In order to actuate the switch first a DC bias voltage, V_b , is applied between the warped plates and the actuation electrodes. The simulated pull-down voltage between the warped plates and the actuation electrodes is predicted to be $V_b=68$ V. As shown in Fig. 10(a), after the warped plate comes into contact with the actuation electrode, the air gap between the warped plate and the ground plane is significantly reduced. This will result in lowering the second required actuation voltage, V_h , applied to the RF port and between the signal and ground plane. The second

electrostatic force produced by V_h pulls down the warped plate into complete contact with the ground plane in a rolling motion. As shown in Fig. 10(b), the switch is actuated to the down-state position with $V_b = 68$ V and $V_h = 30$ V. The simulated hold-down voltage is obtained to be 12 V.

4.5.5 EM Simulation Results

Electromagnetic simulations of the proposed switch are performed using Ansoft HFSS tools. The deformed mesh structure obtained from the FEM stress analysis is transferred from CoventorWare to HFSS to simulate the RF response of the switch in the up-state. Fig. 4.32(a) shows the simulated S-parameters of the switch from 1 to 20 GHz for the up-state. The maximum insertion loss at 20 GHz is simulated to be 0.81 dB and the return loss is better than 15 dB for the frequency range up to 20 GHz. The equivalent circuit model parameters of the switch shown in Fig. 4.24 are extracted from the simulated S-parameters. The switch is predicted to demonstrate an up-state capacitance of $C_u=24$ fF between signal and ground. For the up-state position the impedance of the shunt capacitive switch is given by

$$Z_{s,up} = R_s + j\omega L_s + \frac{1}{j\omega C_u} \quad (4.4)$$

Since the impedance is mainly determined by C_u , the inductance L_s and resistance R_s are not fitted. The simulated return loss and isolation for the down-state position are presented in Fig. 4.32(b). The maximum isolation in this state is simulated to be 12.9 dB at 10 GHz and 20.2 dB at 20 GHz. The switch down-state capacitance C_d , inductance L_s and resistance R_s are determined from fitting the S-parameters to the equivalent CLR model in Fig. 4.24. The down-state capacitance is simulated to be $C_d = 2.6$ pF resulting in a down-state/up-state capacitance ratio C_r of 108:1. The equivalent inductance $L_s = 4.72$ pH is mainly associated to the width of the warped plates over the CPW gap $w = 85$ μm as shown in Fig. 4.23(a). The series resistance R_s does not have any significant effect

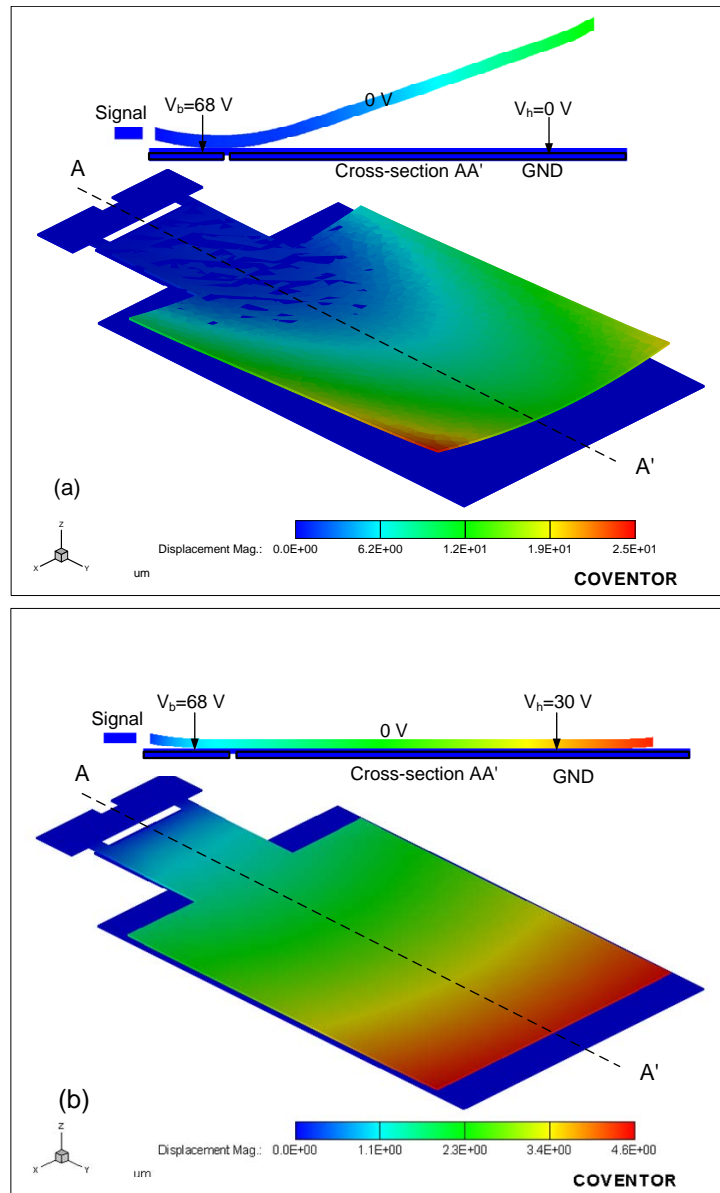


Figure 4.31: FEM simulation results for the actuation voltage of the switch (a) when the first bias voltage V_b is applied between the signal and the actuation electrode and (b) when the warped plates are pulled down by applying the second bias voltage V_h between signal and ground conductors.

on the S-parameters below the self-resonance frequency of the series CLR circuit $f_o = 45$ GHz and it can only be fitted around this frequency. The equivalent series resistance is determined to be $R_s = 0.01 \Omega$.

4.5.6 Measurement Results

The RF performance of the switch is measured using two-port on-wafer measurements up to 20 GHz using an HP8722ES vector network analyzer. The measured S-parameters of the switch for the up-state are presented in Fig. 4.32(a) along with the simulation results. The maximum insertion loss at 20 GHz is measured to be 0.98 dB and the return loss is better than 18 dB at 10 GHz and 13 dB at 20 GHz. There is a good agreement between the simulation and measurement results as shown in this figure. Using the same procedure as explained earlier for the EM simulation results, the value of the up-state capacitance is extracted to be $C_u = 23$ fF from the measured results. The switch is actuated to the down-state position by applying the actuation voltages $V_b = 82$ V on the actuation electrodes and $V_h = 25$ V applied to the RF port through a bias-tee connected to the ports of the network analyzer. The measured S-parameters of the switch in the down-state position are presented in Fig. 4.32(b). The maximum isolation in this state is obtained to be 12.4 dB at 10 GHz and 17.9 dB at 20 GHz. The measured down-state capacitance is extracted to be $C_d = 2.1$ pF resulting in a measured capacitance ratio, C_r of 91:1. The reduction in the down-state capacitance compared to the simulation result is attributed to the surface roughness of the oxide dielectric layer between the warped plates and the ground plane. Assuming a perfectly flat oxide layer with a dielectric constant of $\epsilon_r = 3.9$ and a thickness of $t_{ox} = 0.73 \mu\text{m}$ for the simulations, a capacitance degradation of 19% occurs due to the surface roughness.

The dynamic response of the fabricated switch is also evaluated by measuring the switching time, using the test setup shown in Fig. 4.33. The dynamic transient response is

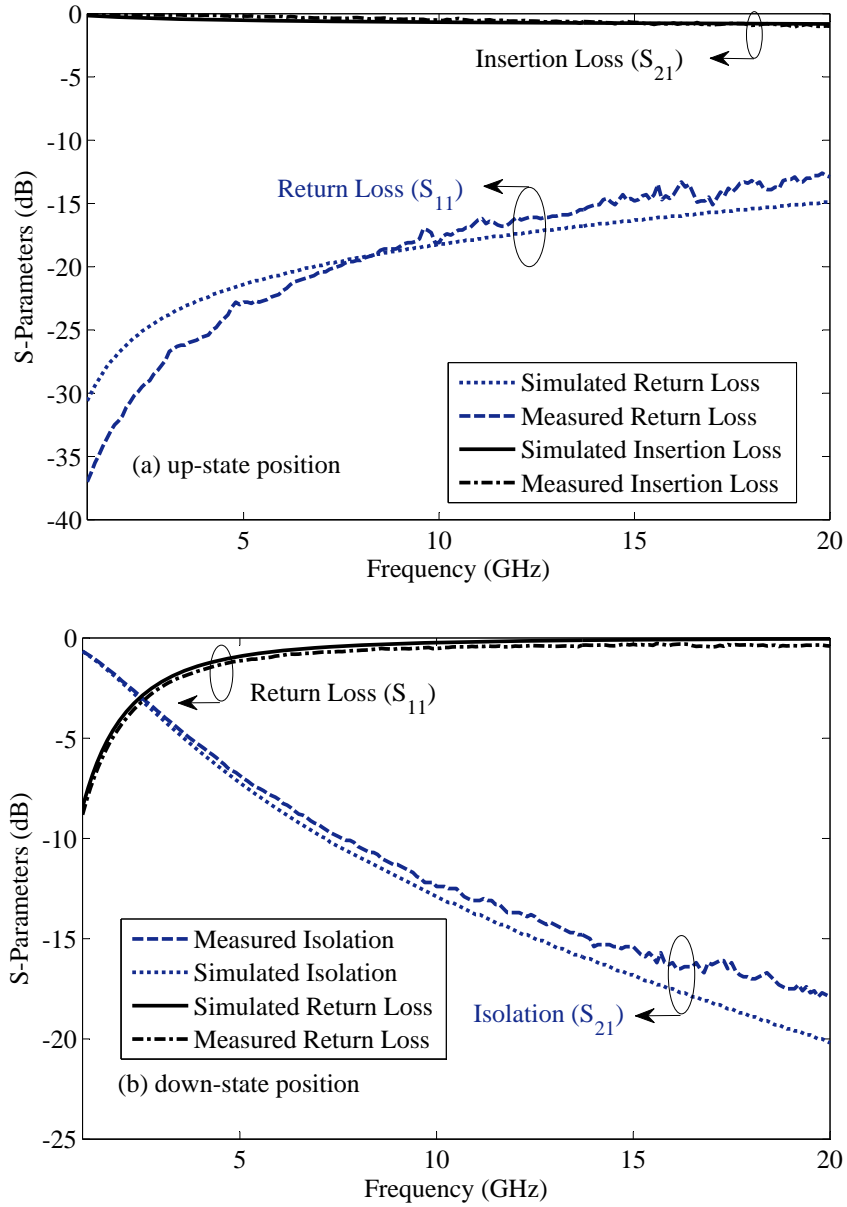


Figure 4.32: Simulated and measured S-parameters of the fabricated capacitive switch for (a) up-state and (b) down-state positions.

measured with a square wave signal used to actuate the switch. The switch is actuated at a rate of 1 kHz with a 0-85 V unipolar voltage and 25 dBm of input RF power at 10 GHz.

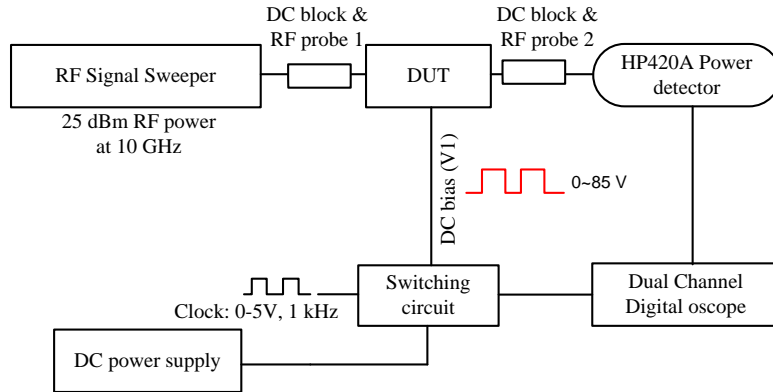


Figure 4.33: Switching time measurement setup.

A high-speed RF power detector is used at the output port to record the transmitted RF power through the switch. Fig. 4.34(a) shows both the actuation voltage and the output signal of the power detector when the switch changes its state from up-state to down-state. The switching time is estimated to be 96 μsec for the up-to-down state transition. The squeeze film damping coefficient plays an important role for this transition. The measured switching time for the down-to-up state transition is 49 μsec as shown in Fig. 4.34(b).

4.5.7 Cascaded Switch

The maximum isolation and the return loss performance of the capacitive type RF MEMS switches are limited by the capacitance ratio of the switch. The maximum achievable capacitance ratio itself is set by the limitations of the fabrication process. By using cascaded switch structures one can achieve a higher isolation and better return loss compared to a single element switch with limited capacitance ratio [50], [94].

A second capacitive type shunt RF MEMS switch integrated in CMOS technology and with higher isolation and better return loss performance is designed and fabricated. The cascaded switch consists of a π -match circuit as shown in the equivalent circuit diagram of Fig. 4.35 where a transmission line section with a high characteristic impedance of Z_h is

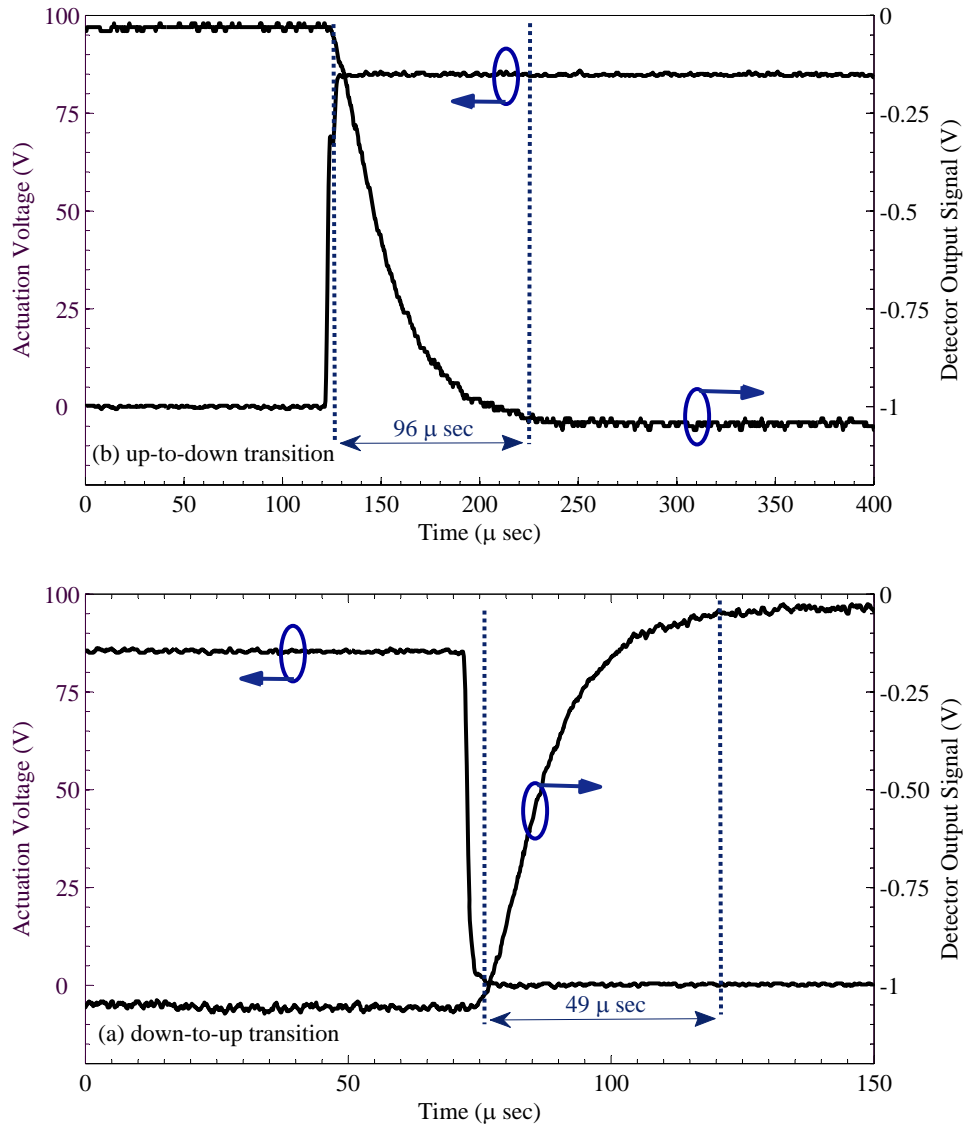


Figure 4.34: Switching time measurement results of the fabricated switch for (a) up-to-down state and (b) down-to-up state transitions.

used between two shunt capacitive MEMS switches with a maximum measured capacitance ratio of 91:1. The extracted CLR model of the single switch is used to design the cascaded switch. The characteristic impedance, Z_h , and the length of the transmission line section,

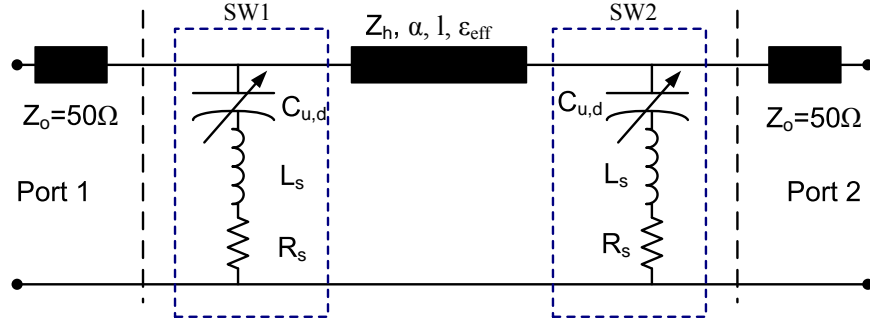


Figure 4.35: Equivalent circuit diagram of the cascaded switch with π -match circuit.

l , is determined following the design procedure in [94]. The switch is optimized for an isolation better than 20 dB at 10 GHz.

Since the CMOS silicon substrate has a very low resistivity ($8 \Omega cm$), it is not suitable for microwave applications. Hence, a deep trench in the silicon substrate and under the signal path of the transmission line section is crucial in order to eliminate the parasitic effects of the lossy silicon substrate and obtain a reasonable RF performance for the fabricated switch. Although the air trench improves the RF performance, it also results in a very low effective dielectric constant ϵ_{eff} for the suspended transmission line, increasing the total required footprint of the fabricated switch on the CMOS chip. Therefore, a slow-wave structure as the one shown in Fig. 4.36 is utilized to reduce the length of the CPW transmission line and the size of the fabricated switch. The proposed slow-wave structure consists of multiple ground fingers attached to the signal line through an oxide bridge. The $1.4 \mu m$ wide oxide layer is used to increase the capacitive loading on the signal line and to increase its effective dielectric constant. It also mechanically connects the fingers to the signal line and prevents them from warping due to the residual stress after release from the silicon substrate. Fig. 4.37 shows the attenuation constant and the effective dielectric constant of the proposed slow-wave, suspended CPW transmission line compared to a standard CPW line on a lossy silicon substrate and also a conventional suspended

CPW line with an air trench. The slow-wave suspended transmission line section used for the cascaded switch design has a characteristic impedance of $Z_h = 61 \Omega$, an effective dielectric constant of $\epsilon_{eff} = 6.8$, and an attenuation constant of 0.83 dB/cm at 10 GHz. An optical micrograph of the fabricated cascaded switch is presented in Fig. 4.38.

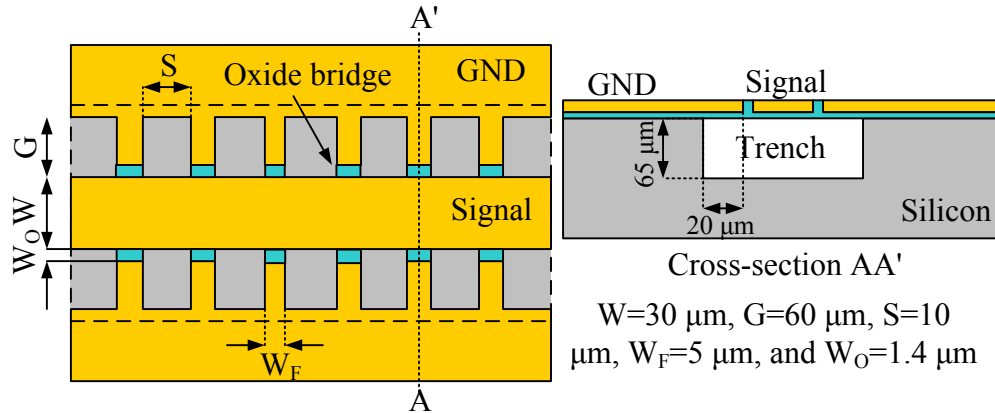


Figure 4.36: Top view and the cross-sectional view of the CPW slow-wave structure.

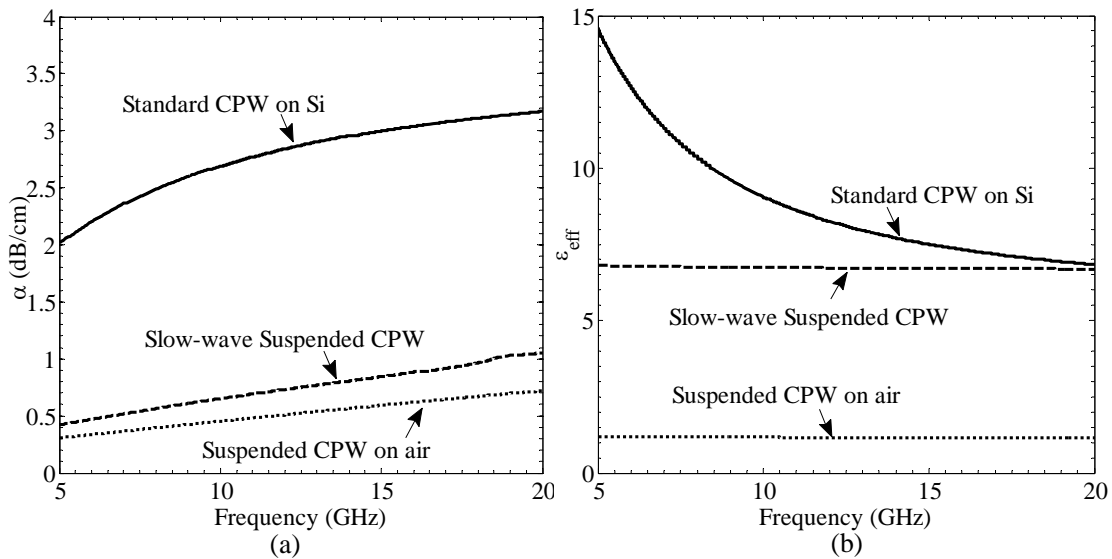


Figure 4.37: (a) Attenuation constant and (b) effective dielectric constant of three different CPW transmission lines on CMOS silicon substrate.

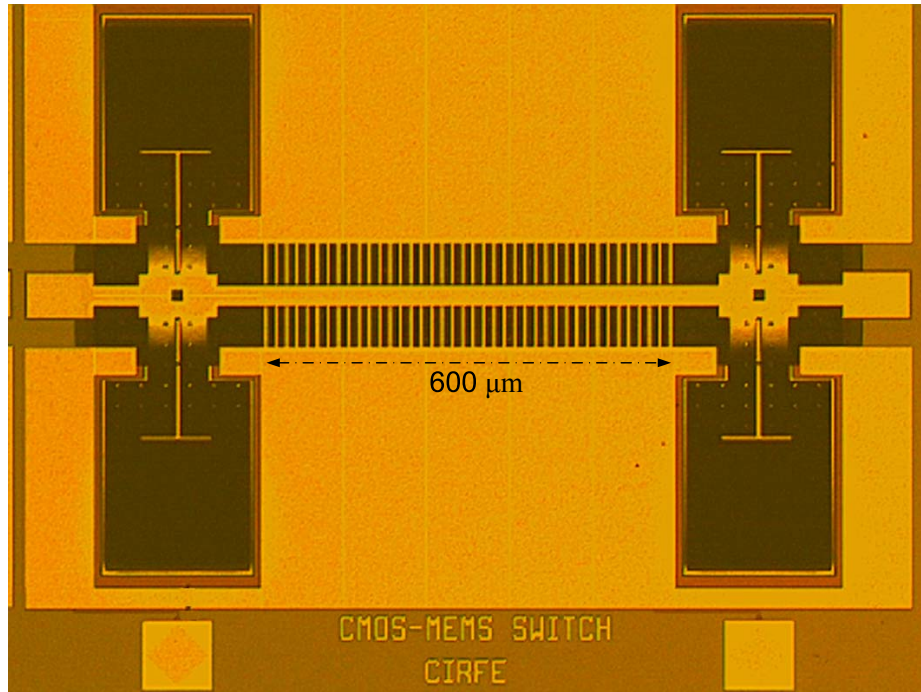


Figure 4.38: Optical micrograph of the cascaded switch with improved isolation and return loss.

Fig. 4.39 shows the measured S-parameters of the cascaded capacitive shunt RF MEMS switch with π -match circuit. The measured return loss is obtained to be better than 19 dB across the frequency band from 1 GHz up to 20 GHz. The insertion loss is measured to be 0.58 dB at 10 GHz and 1.41 dB at 20 GHz. The isolation of the switch is significantly improved compared to the single switch. Using the π -match circuit, the isolation is obtained to be higher than 19 dB for the frequency band from 10-20 GHz.

4.6 Summary

The fabrication of RF MEMS devices using standard CMOS technologies can push MEMS technology to higher levels of integration and improve the performance of RF integrated cir-

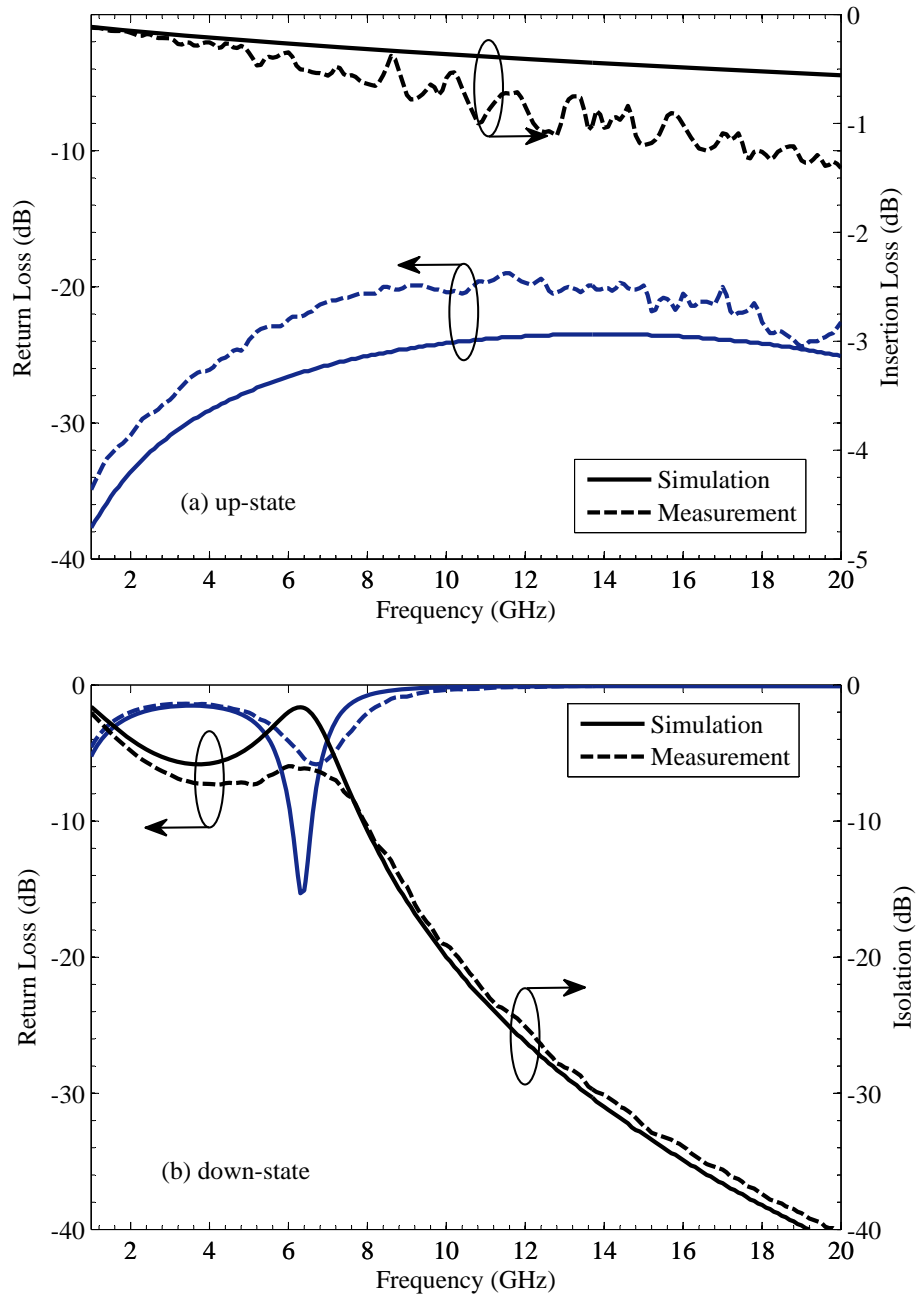


Figure 4.39: Measured S-parameters of the fabricated cascaded switch with π -match circuit integrated in CMOS technology for (a) up-state and (b) down-state.

cuits by eliminating the use of bulky off-chip components. In this chapter, the integration of RF MEMS devices with electrostatic actuation in commercially available CMOS technologies is presented. The developed CMOS-MEMS process allows the fabrication of RF MEMS devices such as tunable capacitors with high quality factor and compact size. An integrated tunable band-pass filter with parallel-plate CMOS-MEMS capacitors is reported which achieves a tuning range of 17% at 9.5 GHz center frequency. Capacitive shunt-type RF MEMS switches implemented using a standard CMOS process are presented for the first time. The switches are fabricated using the 2P4M TSMC 0.35- μm CMOS process and by employing the available dielectric and interconnect metal layers of the CMOS process. The capacitance ratio is improved by using a warped-plate structure. A capacitance ratio of 91:1 is achieved for the fabricated switches. The switch demonstrates an insertion loss less than 1.41 dB, a return loss better than 19 dB and an isolation of more than 19 dB all over the frequency band from 10-20 GHz. The proposed integrated RF MEMS devices can be used to implement multiband and reconfigurable RF front-ends. The fabrication of the proposed RF MEMS devices in a standard CMOS process enables the fully integrated silicon solution for these RF front-ends.

Chapter 5

Reconfigurable MEMS Impedance Matching Networks Fabricated by Standard CMOS Technologies

5.1 Introduction

Reconfigurable impedance matching networks capable of electronically tuning are the key components in the development of adaptive RF transceivers. Several reconfigurable impedance matching networks employing RF MEMS technology have been previously reported. The use of MEMS technology improves the overall performance of these matching network in terms of impedance coverage, loss, power handling and linearity as explained earlier in chapter 3. However, all the previously reported MEMS-based reconfigurable impedance matching networks require a MEMS fabrication process which is not fully compatible with standard CMOS technologies and the implementation of reconfigurable RF front-ends based on these MEMS impedance matching networks rely on a hybrid integration of the matching network with the rest of the RFIC electronics not leading to a

single-chip solution. For example, the reconfigurable amplifier with adaptive matching network in [29] incorporates off-chip MEMS switches used as capacitive stubs in a double-stub matching network. Another dual-band receiver front-end which covers the 1.8 GHz and 5-6 GHz frequency bands was reported in [69] where packaged series contact type MEMS switches are employed to switch between two narrow-band impedance matching networks for each frequency band. The power amplifier in [30] can be tuned over a frequency range from 8-12 GHz by using a reconfigurable output tuner using MEMS switches and a semiconductor-based varactor put together in a hybrid configuration.

In this chapter, we investigate the integration of MEMS-based reconfigurable impedance matching networks in standard CMOS technologies. An 8-bit reconfigurable impedance matching network based on the distributed MEMS transmission line (DMTL) concept is presented that operates at a 13-24 GHz frequency band. Using the proposed network, a wide impedance coverage on the Smith chart is obtained. Design, modeling, fabrication and measurement results of the network are presented. The network is fabricated in a standard 0.35- μm CMOS technology using the CMOS-MEMS processing at the University of Waterloo. A reconfigurable amplifier with tunable lumped-element input and output impedance matching networks using CMOS-MEMS on-chip tunable capacitors and high-Q inductors is also presented. The reconfigurable MEMS impedance matching networks enable the amplifier to operate with the optimum power gain under variable load and source impedance conditions. The amplifier with the tunable input and output impedance matching networks is implemented in 0.18- μm CMOS technology. The monolithic CMOS implementation of these RF MEMS impedance matching networks enables the development of future low-cost single-chip RF multiband transceivers with improved performance and functionality.

5.2 Distributed MEMS Tunable Impedance Matching Network Based on Suspended Slow-Wave Structure Fabricated in 0.35- μm CMOS Technology

5.2.1 Design and Optimization

Fig. 5.1 shows the layout of the DMTL MEMS impedance matching network implemented in 0.35- μm CMOS technology. The network consists of a novel suspended slow-wave transmission line on a silicon substrate loaded with 8 capacitive RF MEMS switches producing 256 (2^8) different impedance matched points on the Smith chart. The use of the slow-wave structure results in a reduced total footprint and enhanced impedance coverage of the network. The design of the proposed impedance matching network follows a similar design procedure previously explained for the matching network with dual-beam MEMS switches in section 3.2 with the difference that the CMOS-MEMS switches used here have only two states similar to the MEMS switches used in conventional DMTL structures.

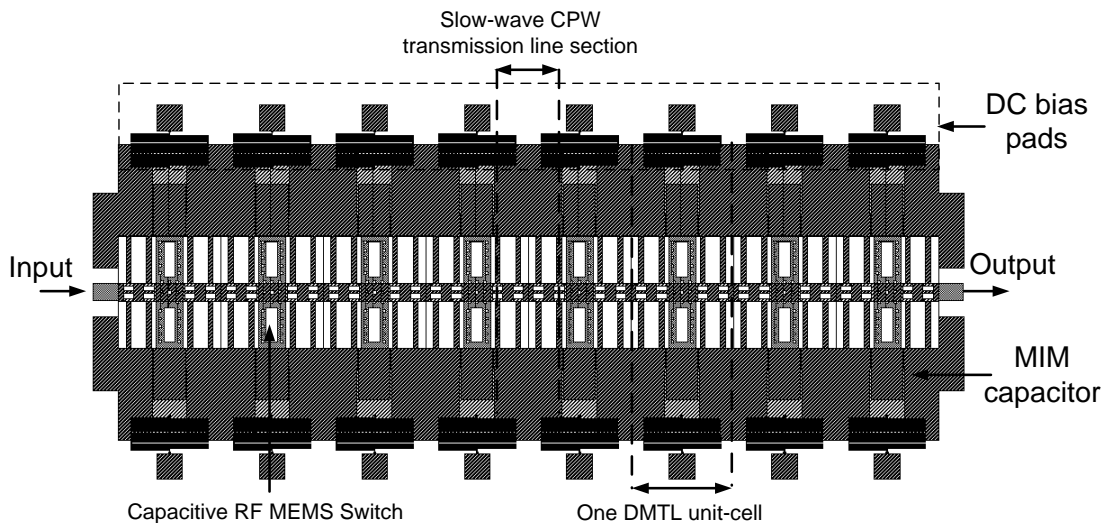


Figure 5.1: Layout of the MEMS DMTL impedance matching network in 0.35- μm CMOS.

The performance of the designed impedance matching network is optimized in terms of the uniformity of the Smith chart coverage obtained using a uniformity factor (χ^2) as in equation (3.2) and by using the design algorithm presented in [51]. The main design parameters include the characteristic impedance of the unloaded transmission line section without the loading effect of the MEMS switches (Z_o), the electrical length of the DMTL unit cell ($\Phi_{u,d}$) for the up-state and down-state of the MEMS switch, and the capacitance ratio of the MEMS switch ($C_r = C_{bd}/C_{bu}$). All the other parameters of the DMTL unit cell and its equivalent circuit model as shown in Fig. 5.2 are related to these three parameters as in equations (3.3-6). Table 5.1 lists the design parameters of the proposed DMTL impedance matching network that is designed to operate at a frequency band from 13 to 24 GHz.

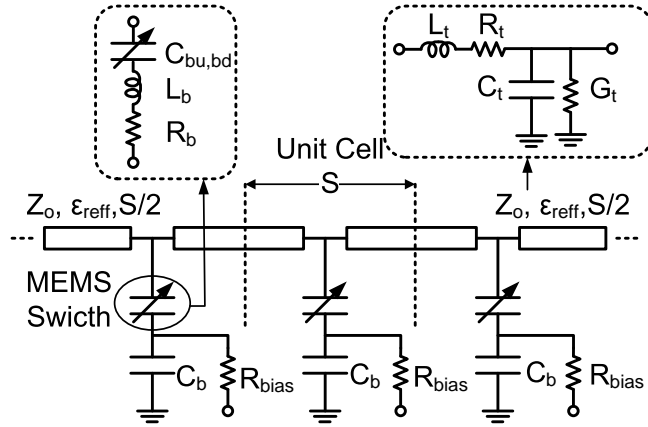


Figure 5.2: Equivalent circuit diagram of a DMTL structure.

Table 5.1: Design parameters for the DMTL matching network operating from 13-24 GHz

Z_{ref} (Ω)	50	Z_u (Ω)	50	N	8	Z_d (Ω)	30	S (μm)	400
ϵ_{reff-u}	20	Z_o (Ω)	102	ϵ_{reff-d}	55	ϵ_{reff}	4.83	C_r	3.3

5.2.2 CMOS Implementation

The network is implemented in a standard two-poly four-metal (2P4M) 0.35- μm CMOS process and then post-processed to integrate the capacitive MEMS switches by an optimized version of the CMOS-MEMS processing technique used for the fabrication of MEMS tunable capacitors as explained in section 4.2. Fig. 5.3 shows the top view and the cross-section view of the DMTL unit cell. A novel suspended slow-wave coplanar waveguide (CPW) structure is utilized in order to reduce the loss caused by the low-resistivity silicon substrate (8-12 Ωcm), enhance the effective dielectric constant of the line, and reduce the total footprint of the network. The MEMS bridge consists of a composite aluminum-oxide (Al/SiO₂) stack that is suspended 1.15 μm above the signal line. As shown in the cross-sectional view of Fig. 5.3, there is a 100 μm deep trench under the signal line that isolates

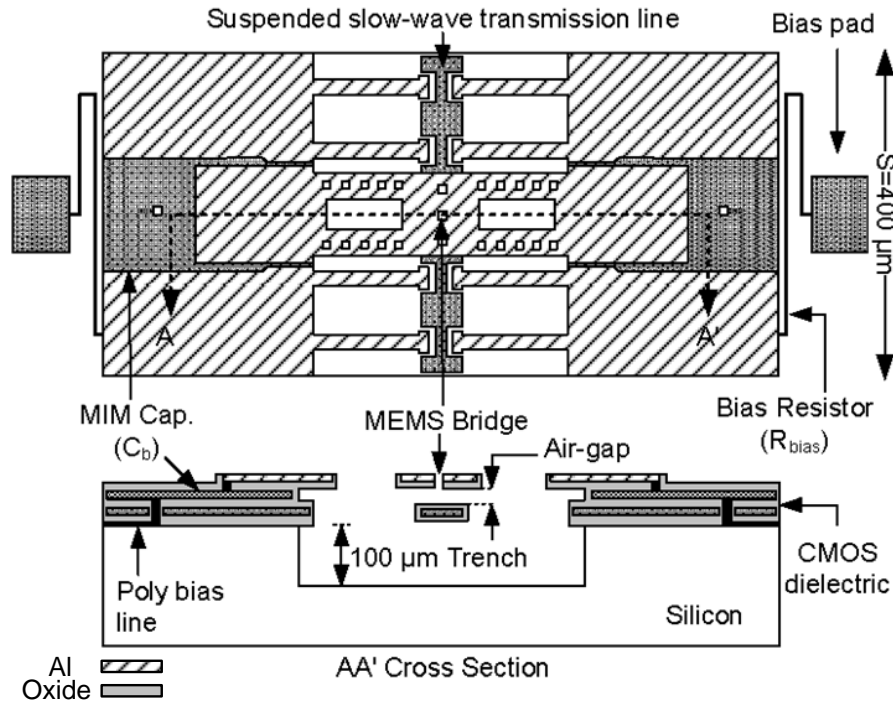


Figure 5.3: Top view and the cross sectional view of the DMTL unit cell.

it from the substrate. The actuation voltage is applied to the MEMS bridge through a bias resistor (R_{bias}) made of polysilicon with a DC resistance of $50 \Omega/\text{square}$. There is a metal-insulator-metal (MIM) capacitor between the MEMS bridge and the ground plane (C_b) that provides DC isolation between the MEMS bridges and makes it possible to separately actuate each switch by applying a DC bias voltage between the signal line and each MEMS bridge independently. Since $C_b \gg C_{bu}$ and C_{bd} , the total shunt capacitance between the signal line and ground for the up- and down-state positions is dominated by C_{bu} and C_{bd} , respectively.

Fig. 5.4 shows the schematic diagram of the CMOS-MEMS processing steps. Fig 5.4(a) shows the CMOS die after standard processing. During the first step, as presented in Fig. 5.4(b), the CMOS dielectric layer is removed using reactive ion etching (RIE) of oxide and using the topmost metal layer (M_4) as a mask which is similar to the post-processing reported in [32], [71]. After this step both the silicon substrate and the sacrificial metal layers are exposed for subsequent etching and release of the MEMS capacitive switches as shown in the SEM image of Fig. 5.5. The second step involves the RIE of the silicon

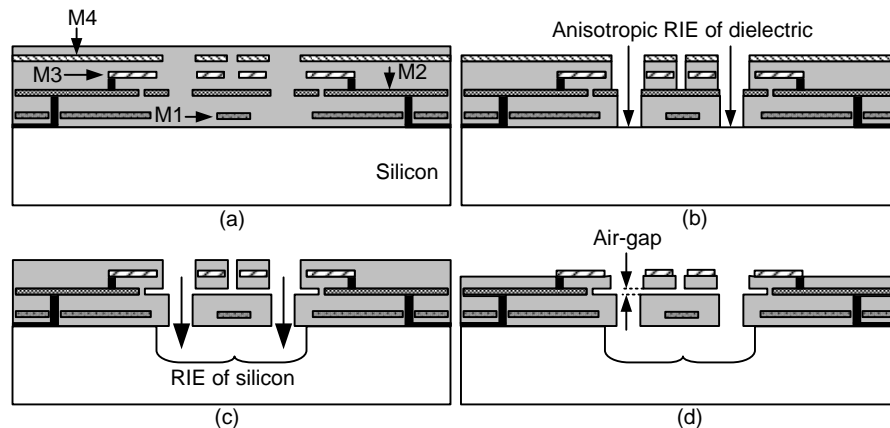


Figure 5.4: CMOS-MEMS processing steps required to integrate the MEMS capacitive switches in the $0.35\text{-}\mu\text{m}$ CMOS technology.

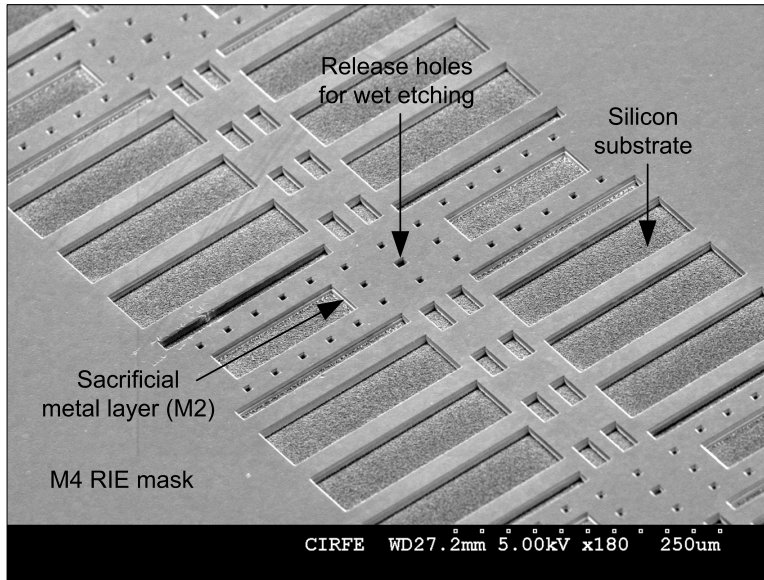


Figure 5.5: RIE of the CMOS dielectric layer to expose the silicon substrate and M2 sacrificial layer.

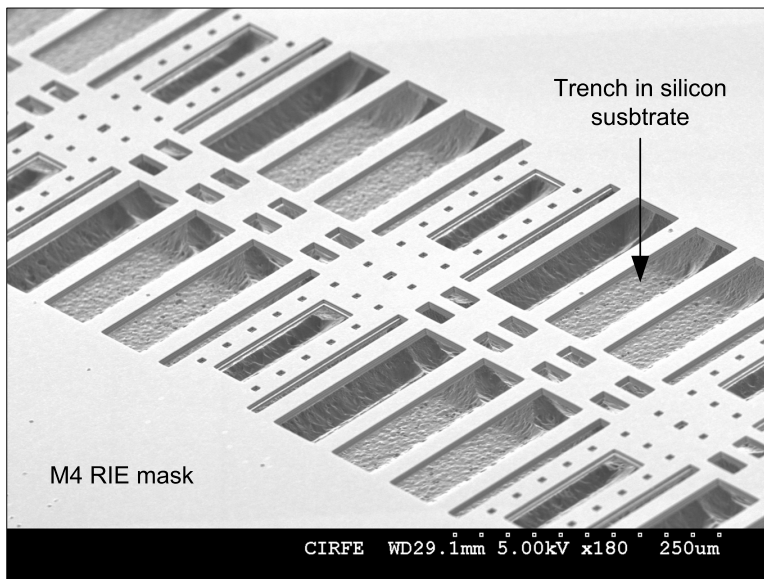


Figure 5.6: RIE of the silicon substrate to create a trench under the signal line.

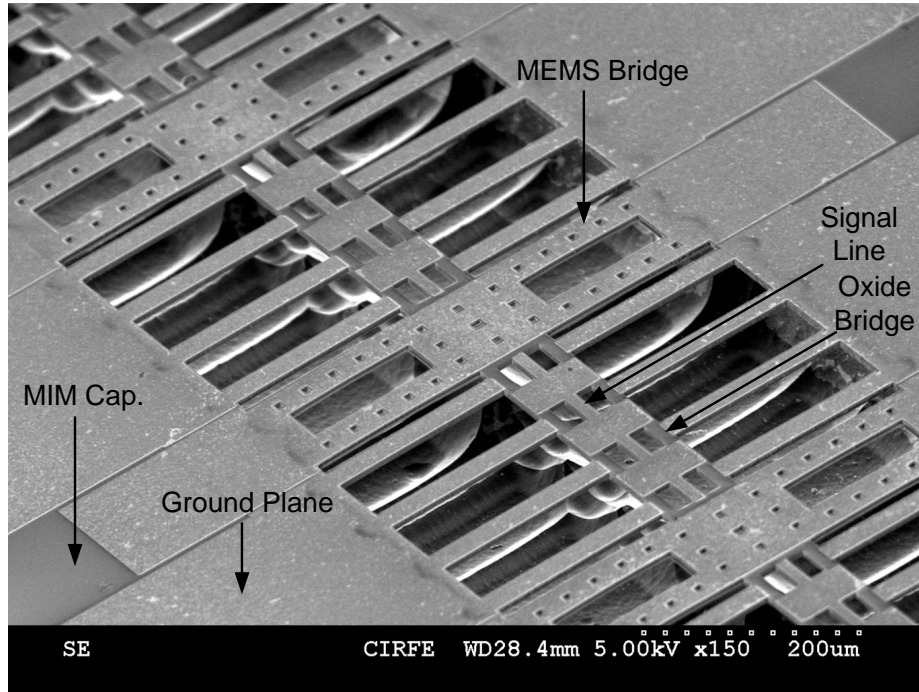


Figure 5.7: SEM image of the CMOS-MEMS capacitive switch.

substrate in order to create the trench under the signal line, as shown in Fig. 5.6, and also wet etching of the sacrificial metal layer (M_2). By removing M_2 , an air gap is created between the MEMS bridge (M_3) and the signal line (M_1) [as in Fig. 5.4(c)]. The final post-processing step is the critical point drying of the dies after wet etching of the sacrificial layer and a second oxide RIE to remove the oxide on top of the pads for electrical contact and also to etch the oxide layer on top of the MEMS bridges to reduce the required actuation voltage of the MEMS device [see Fig. 5.4(d)]. An SEM image of the MEMS capacitive switch after all the post-CMOS processing steps is presented in Fig. 5.7. A photograph and diagram of the fabricated DMTL impedance matching network with 8 MEMS capacitive switches is shown in Fig. 5.8. The MEMS bridges are connected to the bias pads through bias resistors ($R_{bias} > 10 \text{ k}\Omega$) and the CPW center conductor is DC grounded in the test setup using bias tees.

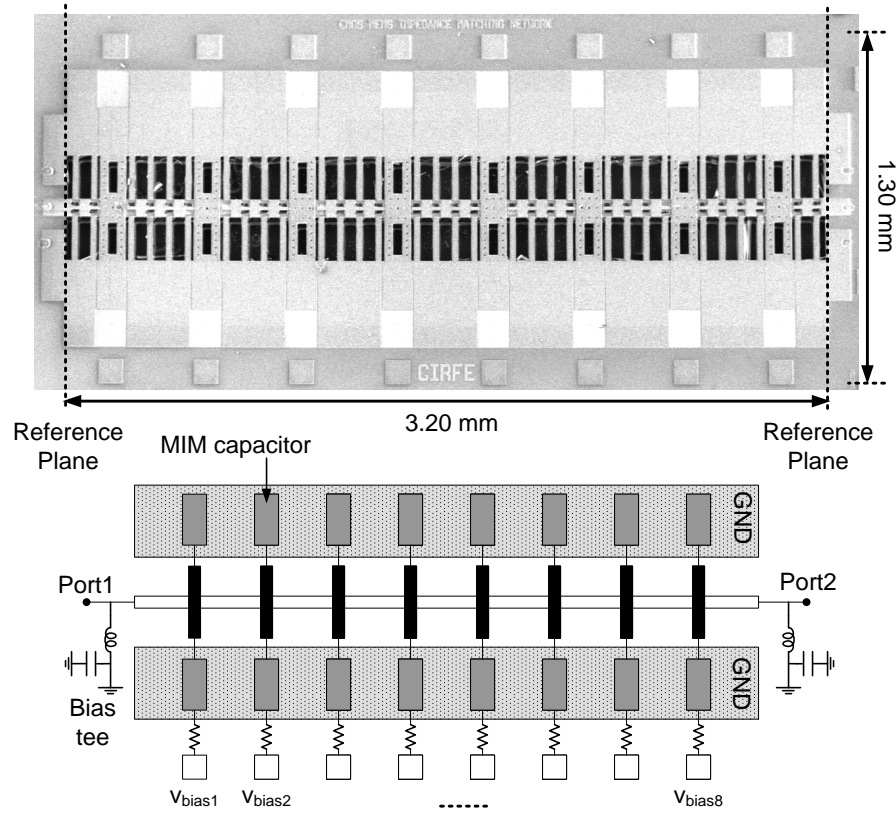


Figure 5.8: (a) Photograph and (b) diagram of the DMTL impedance matching network with 8 MEMS switches built in 0.35- μm CMOS technology.

5.2.3 Suspended Slow-Wave Transmission Line

The CPW transmission line is a suitable topology for the implementation of on-chip millimeter-wave circuits and interconnects using the silicon-based technologies. This is due to the unavailability of substrate via holes in these technologies. For the microstrip transmission lines in silicon-based monolithic microwave integrated circuits (MMICs), the signal and ground conductors are separated only by a few microns of inter-metal dielectric layer and this will impose several difficulties such as increased capacitance between signal and ground. Hence, a transmission line with a high characteristic impedance ($Z_o = 102 \Omega$), requires a narrower signal line increasing the ohmic resistance and loss of the trans-

mission line. In contrast, using the CPW topology, a wider signal path can be used since the spacing between the signal and ground conductors is not limited by the thickness of the inter-metal dielectric layer. In the conventional silicon-based CPW transmission lines, there is a strong penetration of the electromagnetic field into the low resistivity silicon substrate which increases the loss at millimeter-wave frequencies. This can be addressed by adding floating metal shield strips between the CPW line and the lossy silicon substrate using the lower interconnect metal layers [95, 96, 97]. A micromachined coplanar waveguide transmission line fabricated in a standard CMOS process is reported in [98] where the lossy silicon substrate was removed in the vicinity of the transmission line. Although the insertion loss characteristic was improved, the line has a low relative dielectric constant which results in a larger on-chip wavelength increasing the chip real state. In this section, a novel suspended slow-wave CPW transmission line structure is presented which enables the fabrication of a transmission line with a high characteristic impedance, lower insertion loss and compact size using the standard silicon-based CMOS technologies.

Fig. 5.9 illustrates the schematic of the proposed suspended slow-wave (SSW) structure. The slow-wave effect is achieved by extending T-shaped metal patterns from the ground planes to the signal line to increase the line capacitance value and also by periodically reducing the width of the central conductor to increase the line inductance [99]. The 1- μm wide oxide bridge, mechanically connects the T-shaped ground pattern to the signal line which is used to suspend the signal conductor after removing the silicon substrate. Three types of CPW transmission lines are compared, including the CPW on silicon substrate, suspended CPW (S-CPW) and suspended slow-wave CPW (SSW-CPW). Using 3D full-wave simulations with HFSS, the performance of each transmission line is characterized by the attenuation per millimeter length (α in dB/mm), relative dielectric constant (ϵ_r), and quality factor (Q). For a fair comparison, all the transmission lines are designed to have the same characteristic impedance $Z_o = 102 \Omega$.

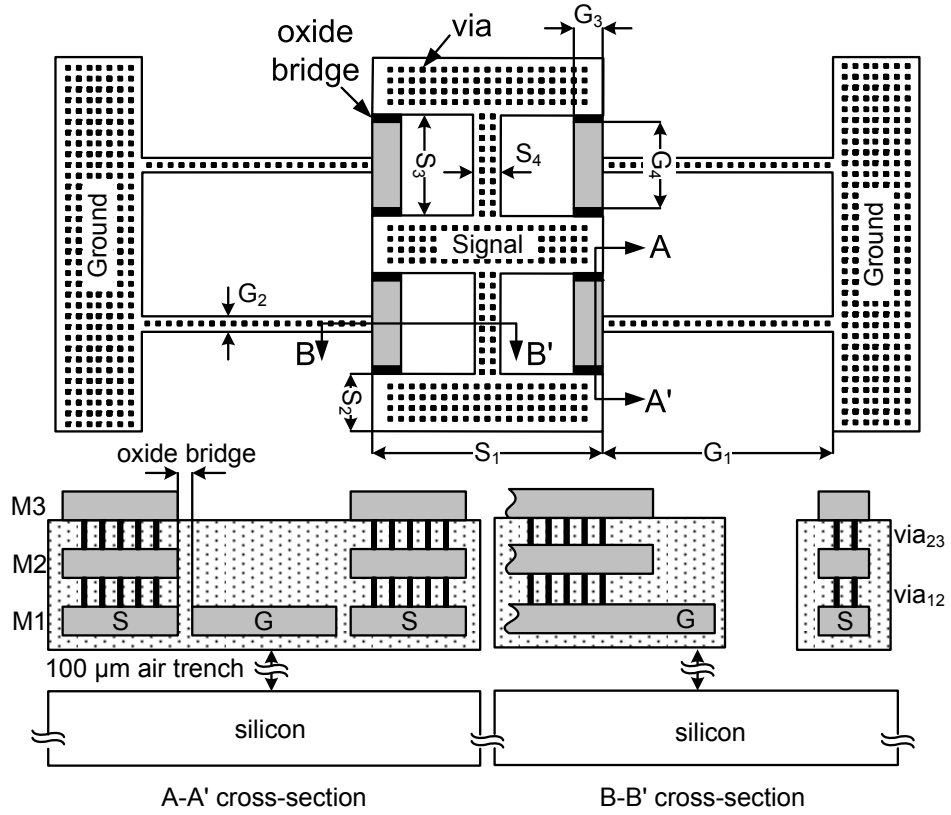


Figure 5.9: Top view and the cross-sectional view of the suspended slow-wave CPW transmission line, S and G parameters mark the signal line and ground plane dimensions, respectively.

Table 5.2: Geometrical parameters of the CPW, S-CPW, and SSW-CPW lines

SSW-CPW			
$S_1 : 70 \mu\text{m}$	$S_2 : 20 \mu\text{m}$	$S_3 : 40 \mu\text{m}$	$S_4 : 10 \mu\text{m}$
$G_1 : 185 \mu\text{m}$	$G_2 : 20 \mu\text{m}$	$G_3 : 10 \mu\text{m}$	$G_4 : 38 \mu\text{m}$
S-CPW		CPW	
$G : 33 \mu\text{m}$	$S : 70 \mu\text{m}$	$G : 220 \mu\text{m}$	$S : 12 \mu\text{m}$

Table 5.2 summarizes the geometrical parameters of the transmission lines studied in this section. Fig. 5.10 shows the simulated relative dielectric constant of the conventional CPW line on low resistivity ($8 \Omega\text{cm}$) silicon substrate, suspended CPW (S-CPW), and suspended slow-wave (SSW-CPW) lines extracted from the S-parameters using [60]. The ϵ_r of the conventional CPW is about 6.5 and is set by the relative dielectric constant of the silicon substrate ($\epsilon_r = 11.9$) and the surrounding air ($\epsilon_r = 1$). The suspended CPW line in air with $S = 70 \mu\text{m}$ and $G = 33 \mu\text{m}$ has a relative dielectric constant $\epsilon_r = 1.1$. Since the wavelength is inversely proportional to $\sqrt{\epsilon_r}$, the S-CPW structure will not lead to a compact implementation of the proposed network. This issue is addressed by employing the proposed SSW-CPW structure. The SSW-CPW structure has a relative dielectric constant of $\epsilon_r = 4.8$ resulting in a size reduction factor of 2.1 compared to the S-CPW structure. The attenuation and quality factor of the lines are shown in Fig. 5.11 and Fig. 5.12, respectively. The attenuation of the CPW on silicon is 3.8 dB/mm at 20 GHz. By removing the silicon substrate under the signal line, the attenuation is reduced to less than

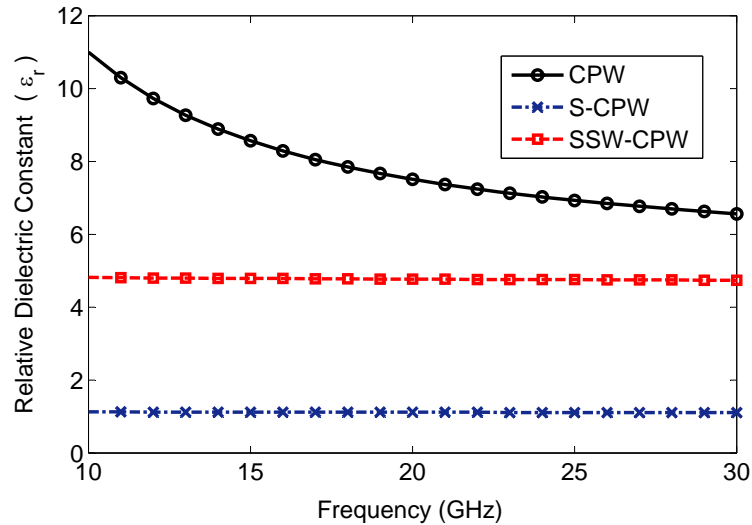


Figure 5.10: Simulated relative dielectric constant (ϵ_r) of the CPW, S-CPW, and SSW-CPW transmission lines.

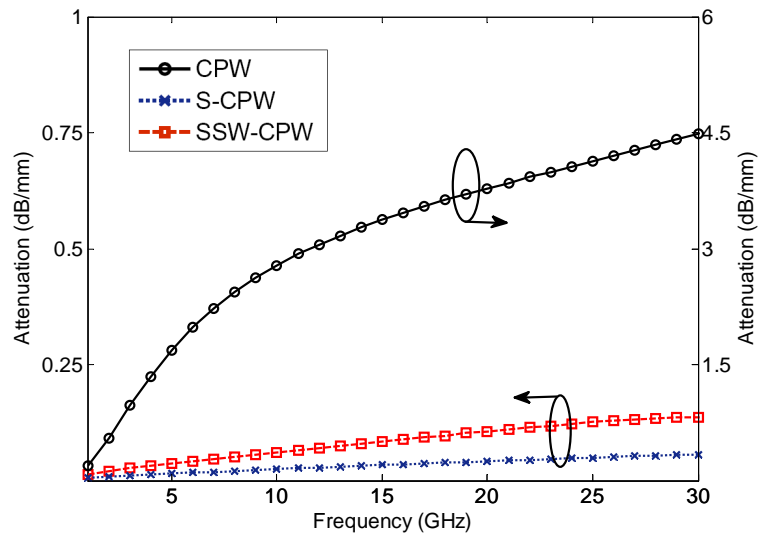


Figure 5.11: Simulated attenuation (α) per millimeter length of the CPW on silicon substrate, S-CPW, and SSW-CPW transmission lines.

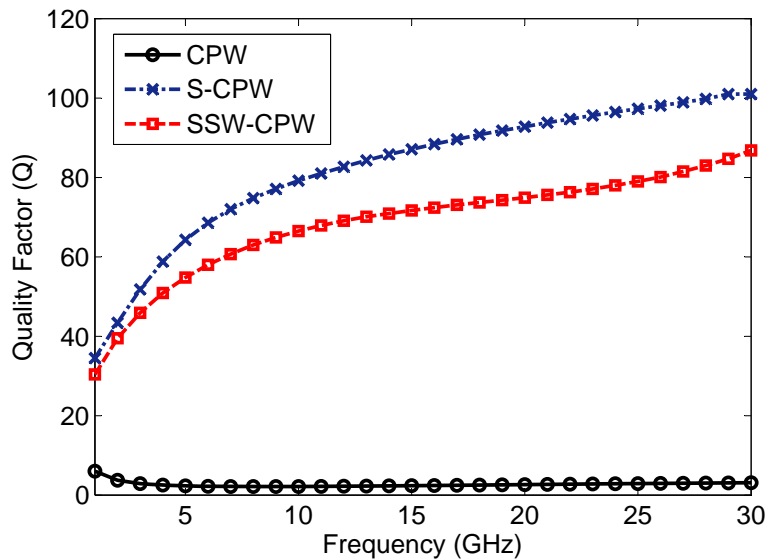


Figure 5.12: Simulated quality factor (Q) of the CPW on silicon substrate, S-CPW, and SSW-CPW transmission lines.

0.1 dB/mm and 0.14 dB/mm for the S-CPW and SSW-CPW lines, respectively. Fig. 5.12 compares the quality factor of the lines. At 20 GHz, the CPW line on silicon has a quality factor of less than 5 while the SSW-CPW line achieves a quality factor of 75. The Q factor of the SSW-CPW line is comparable to the quality factor of the S-CPW line with a Q of 93 at 20 GHz. According to these results, the use of the SSW-CPW line permits the compact implementation of the proposed impedance matching network with a lower insertion loss.

5.2.4 DMTL Unit Cell

The DMTL unit cell consists of a 400- μm long SSW-CPW line section that is loaded with a MEMS switch as shown in the schematic diagram of Fig. 5.3. The SSW-CPW line section has an unloaded characteristic impedance of 102 Ω and a relative dielectric constant of 4.83. The dimensions of the MEMS switch are 120 μm by 70 μm on the signal line and are selected in order to obtain the design parameters listed in Table 5.1. Electromagnetic simulations with HFSS are performed to find the S-parameters of the DMTL unit cell for the up- and down-state positions and also for the unloaded slow-wave transmission line. As shown in the equivalent circuit diagram of the DMTL unit cell in Fig. 5.2, the MEMS switch is represented by a series RLC network with a capacitance value C equal to C_{bu} and C_{bd} for the up- and down-state positions, respectively. The suspended slow-wave transmission line section is modeled using the equivalent $RLGC$ network extracted from the S-parameters, [60]. The equivalent circuit model of Fig. 5.2 is used in ADS to fit the simulated S-parameters of the DMTL unit cell in the up- and down-state positions and the extracted parameters are summarized in Table 5.3.

Table 5.3: The equivalent circuit model parameters of the DMTL unit-cell extracted from EM simulation results

MEMS switch parameters			
C_{bu} (fF)	74.8	L_b (pH)	7.8
C_{bd} (fF)	252	R_b (Ω)	0.247
C_r	3.37	S (μm)	400
C_b (pF)	2.6	R_{bias} (K Ω)	>10
unloaded line parameters			
C_t (fF)	14.37	L_t (pH)	149
R_t (Ω)	0.52	G_t (S)	7×10^{-8}
ε_{reff}	4.83	Z_o (Ω)	102
loaded line parameters			
Z_u (Ω)	53	Z_d (Ω)	32
ε_{reff-u}	17	ε_{reff-d}	51

5.2.5 Impedance Coverage

The equivalent circuit model of the DMTL unit-cell with the extracted parameters listed in Table 5.3 is used to simulate the impedance coverage of the matching network for all the possible combinations of the MEMS switch states. Fig. 5.13 shows the simulated impedance coverage of the network at six different frequencies from 14 GHz to 24 GHz suitable for applications such as vehicular radar at a 24 GHz industrial-scientific-medical (ISM) band. As shown in this figure, the proposed impedance matching network results in a uniform coverage of the Smith chart. The uniformity of the Smith chart coverage is evaluated based on a uniformity factor χ^2 given in equation (3.2) and repeated here for clarity:

$$\chi^2 = \sum_{i=1}^{N_i} \sum_{j=1}^{N_j} \frac{(N(i, j) - \frac{N_{total}}{N_i N_j})^2}{\frac{N_{total}}{N_i N_j}} \quad (5.1)$$

where $N_i \times N_j$ is the number of pie shaped sub-sections dividing the Smith chart and $N(i, j)$ is the number of impedance points inside each sub-section. The estimated uniformity factor

over a frequency band from 10 to 30 GHz and for $N_i = 10$, $N_j = 25$, is presented in Fig. 5.14. The designed impedance matching network achieves a χ^2 factor of less than 500 for the

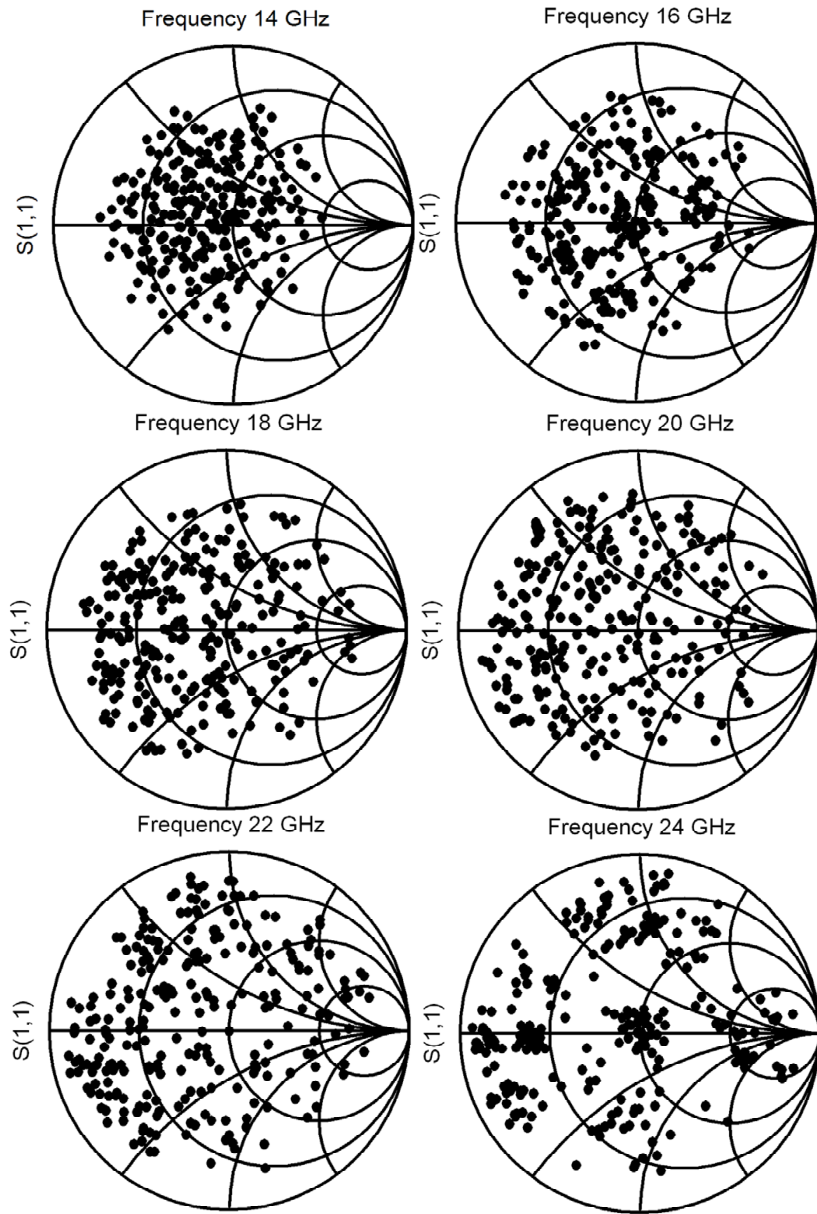


Figure 5.13: Simulated impedance coverage of the designed DMTL impedance matching network at different frequencies.

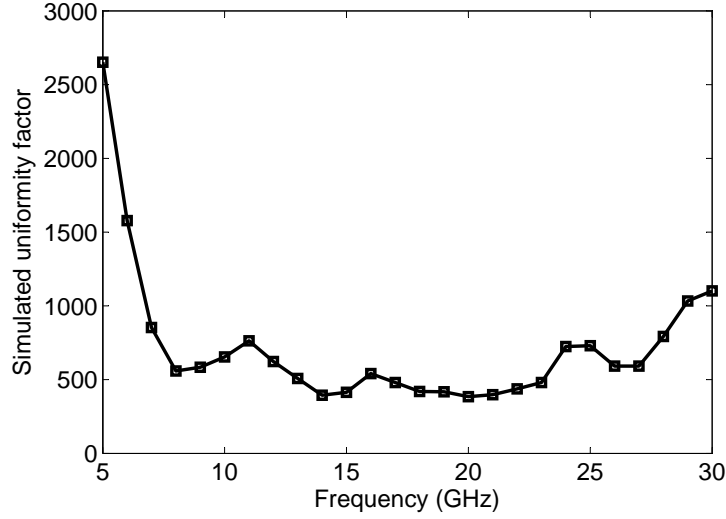


Figure 5.14: Estimated uniformity factor of the designed DMTL impedance matching network.

frequency band from 13 to 23 GHz. A χ^2 factor of less than 500 corresponds to a fairly wide coverage of the Smith chart with a return loss better than 10 dB as will be explained using the experimental results. The maximum frequency of operation for the proposed DMTL impedance matching network is determined by the Bragg frequency (f_B) of the periodic DMTL structure when all the MEMS switches are actuated to the down-state position [46]

$$\omega_B = \sqrt{\frac{b - \sqrt{b^2 - 4ac}}{2a}}$$

$$a = s^2 L_t C_t L_b C_{bd}$$

$$b = s^2 L_t C_t + s L_t C_{bd} + 4 L_b C_{bd}$$

$$c = 4 \tag{5.2}$$

and is $f_B = 33$ GHz using the equivalent circuit model parameters listed in Table 5.3.

5.2.6 Experimental Results

On-chip S-parameter measurements of the fabricated DMTL impedance matching network were performed using an RF probe station with SOLT calibration over a frequency range from 1 to 26 GHz. Fig. 5.15 compares the measured and simulated S-parameters of the matching network for two different states of the MEMS switches, i.e., when all the switches are in their up-state position and when all the switches are actuated to the down-state position. As shown in this figure, there is a fairly good correlation between the measured S-parameters and the EM simulation results for both states. The measured S-parameters of the matching network with all the switches in the up-state and down-state positions were fitted to the equivalent circuit model of the impedance matching network in ADS. The extracted equivalent circuit model parameters from the measurement results are listed in Table 5.4.

The MEMS bridge as shown in the cross-sectional view of Fig. 5.3 consists of a composite metal-dielectric layer of Al/SiO₂ with a thickness of $t_{Al} = 0.64 \mu\text{m}$ and $t_{ox} = 1 \mu\text{m}$, respectively. This composite bridge is subjected to a residual stress gradient generated from the fabrication process and causes an upward deformation of the MEMS bridge. The accurate characterization of the stress-induced bending is essential for the design of the

Table 5.4: The equivalent circuit model parameters of the DMTL unit-cell extracted from the measured S-parameters

C_{bu} (fF)	72	L_b (pH)	12
C_{bd} (fF)	246	R_b (Ω)	0.1
C_t (fF)	12	L_t (pH)	143
R_t (Ω)	0.251	G_t (S)	2.4×10^{-7}
ε_{reff}	3.86	Z_o (Ω)	109
Z_u (Ω)	54	Z_d (Ω)	32.5
ε_{reff-u}	15.6	ε_{reff-d}	44

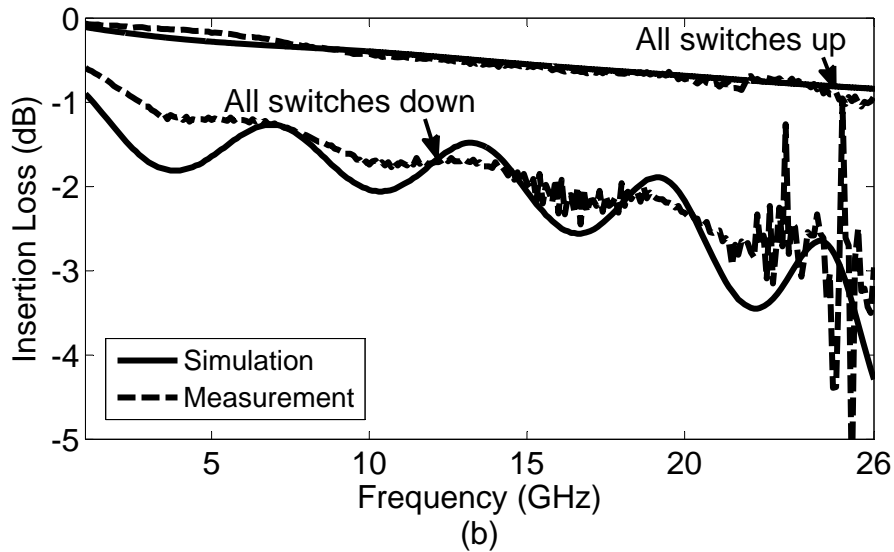
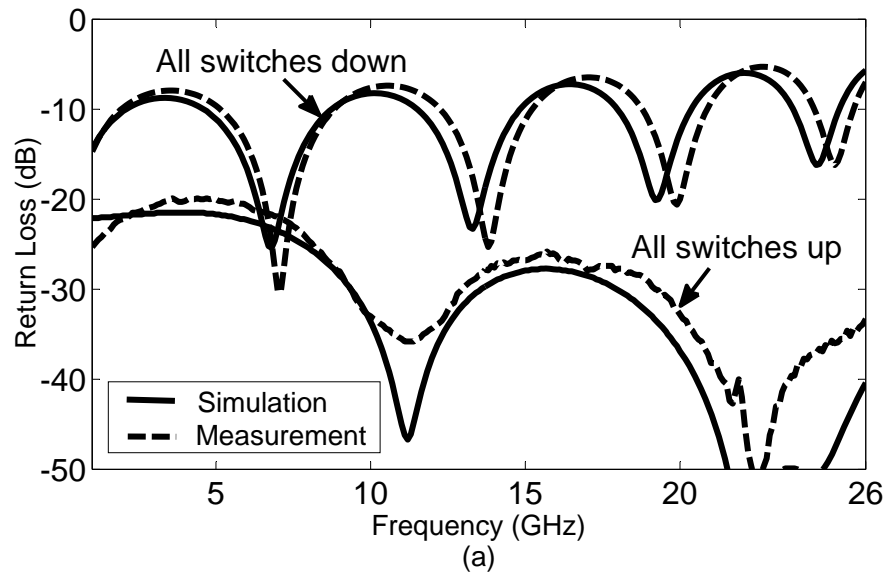


Figure 5.15: Measurement and simulation results of the CMOS DMTL impedance matching network (a) return loss for two different combinations of MEMS switches and (b) the insertion loss.

MEMS bridge up-state capacitance C_{bu} . The stress gradient is determined by characterizing the stress-induced bending of bilayer cantilever beams and is obtained to be $\sigma_{mis} =$

145 MPa as explained in section 4.5. The measured height of the MEMS bridges after release is 1.15 μm using an optical interferometer from WYKOTM. The measured up- and down-state MEMS bridge capacitance values are found to be $C_{bu} = 72$ fF and $C_{bd} = 246$ fF, respectively, resulting in a measured capacitance ratio of $C_r = 3.42$ which is very close to the simulation results summarized in Table 5.3. The measured actuation voltage, V_p , of the MEMS switches is 65 V.

5.2.7 Loss Analysis

Since, in real-world applications, the impedance matching network is used as a mismatched two-port network, the loss of the network is more accurately defined as the ratio between the power transferred to the load and the power available at the input of the network [13]

$$\alpha = \frac{|S_{21}|^2}{1 - |S_{11}|^2}. \quad (5.3)$$

Fig. 5.16 shows the measured loss when all the switches are in the up- and down-state positions and also the average loss of all the possible combinations of switch states. The equivalent ADS circuit model of the matching network with both input and output ports terminated with 50 Ω loads was used to find the minimum, maximum and average loss of the network at each frequency and for all the possible states. The average loss of the network is between 0.4-2.1 dB from 1 to 26 GHz. The maximum loss was obtained to be 7.55 dB at 26 GHz for the $(S_8 \dots S_1) = (10100101)$ state of the matching network where '1' and '0' correspond to the down- and up-state of the MEMS switches, respectively.

5.2.8 Impedance Coverage and Power Transfer

Fig. 5.17 shows the measured impedance coverage of the network at different frequencies from 14 to 24 GHz which are in close agreement with the simulated impedance coverage

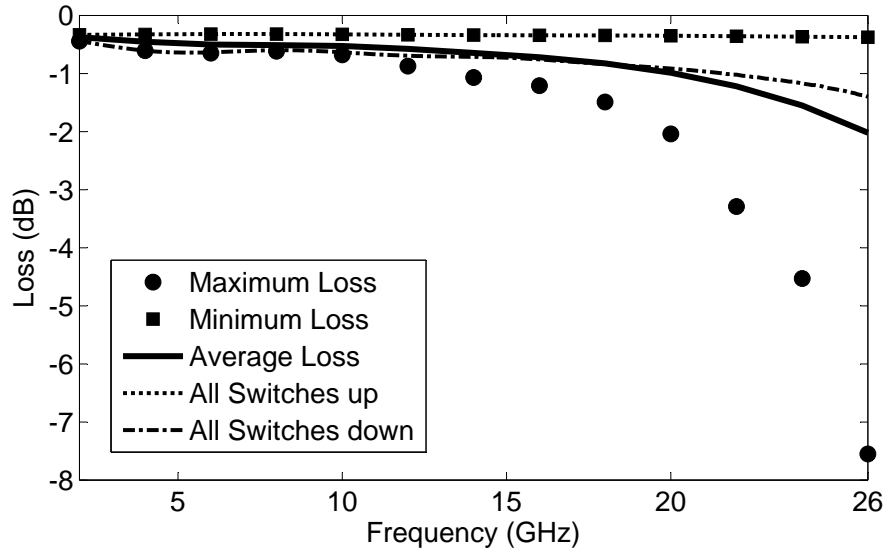


Figure 5.16: Estimated loss of the fabricated DMTL impedance matching network when all the switches are in the up- and down-state positions, the minimum, maximum, and average loss for all the possible states.

as presented in Fig. 5.13. The performance of the fabricated impedance matching network in terms of the return loss is presented in Fig. 5.18. As shown in this figure, using the fabricated matching network at 14 GHz, all the source impedances out to a maximum voltage standing-wave ratio (VSWR) of 4.56:1 can be matched to 50Ω with a return loss better than 10 dB. The measured data at 24 GHz demonstrates a wide coverage of the Smith chart with a return loss better than 10 dB and a maximum VSWR of 11.5:1. The measured uniformity factor of the Smith chart coverage is also presented in Fig. 5.19 and is around 500 from 13 to 24 GHz.

The power transfer ratio G_T (in dB) when the matching network is used to transfer power between a source with variable source impedance and a 50Ω load is computed using the measured S-parameters for all the possible combinations of the MEMS switch states

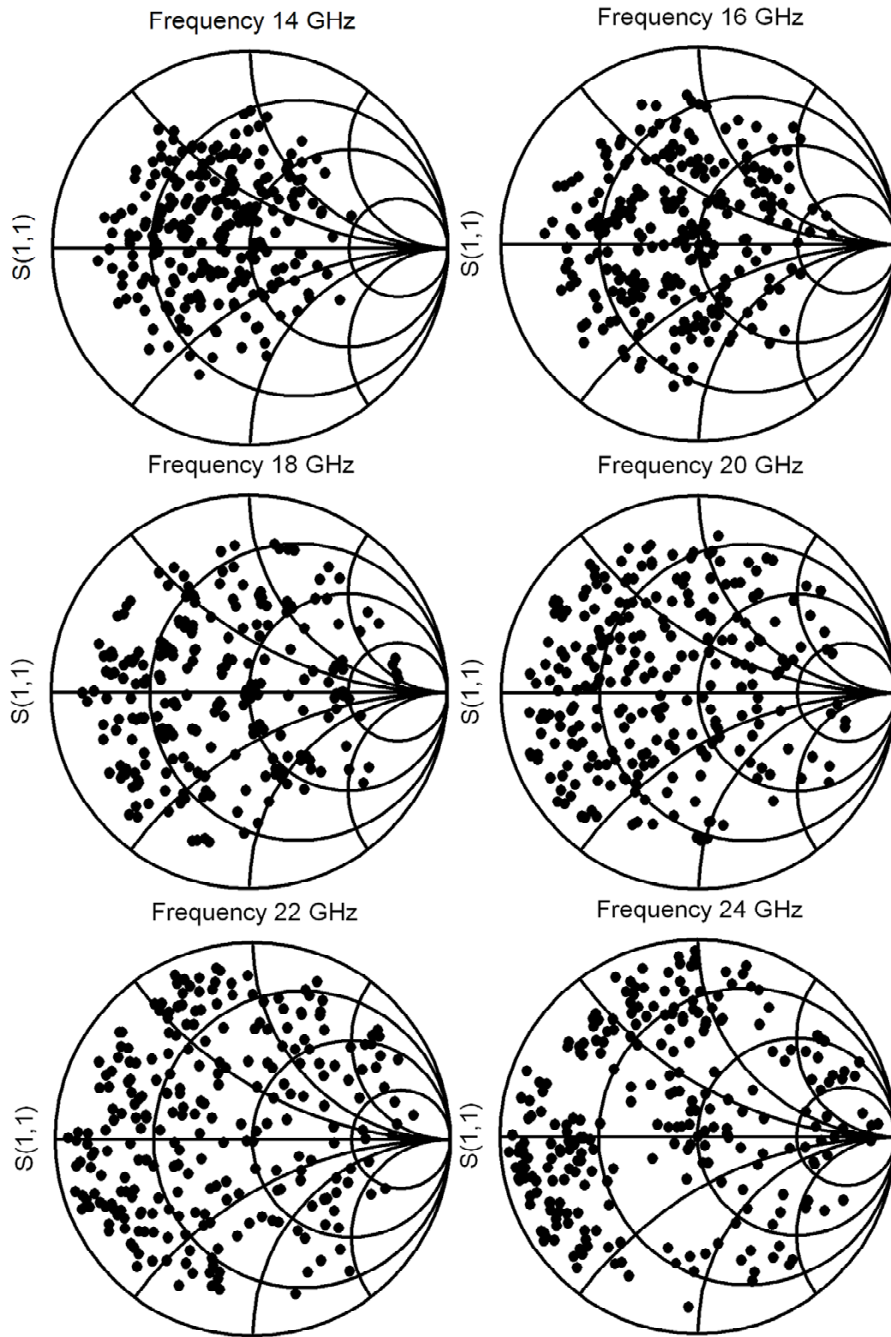


Figure 5.17: Measured impedance coverage of the fabricated DMTL impedance matching network from 16 to 26 GHz.

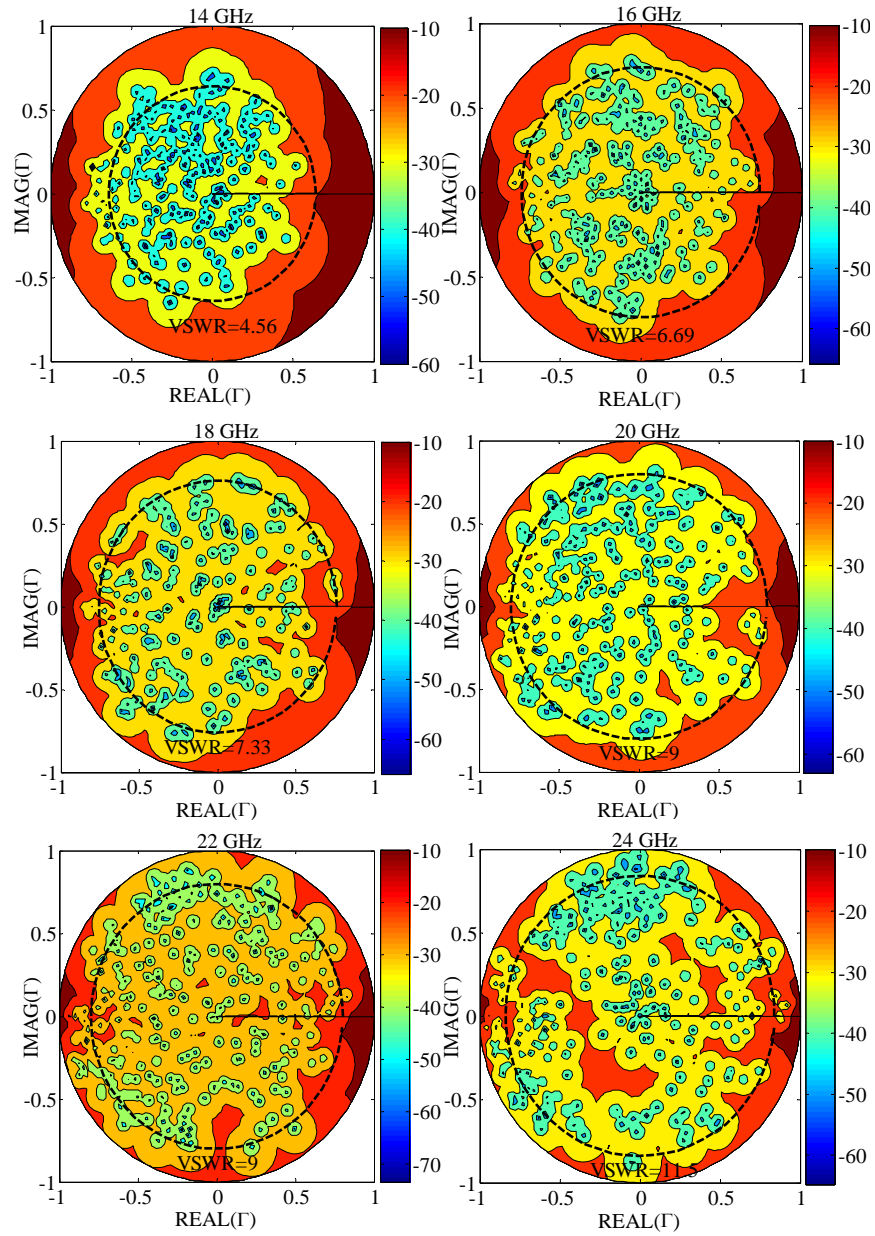


Figure 5.18: Measured return loss performance of the fabricated network. The maximum VSWR with an impedance match better than 10 dB is 4.56, 6.69, 7.33, 9, 9, and 11.5 at 14, 16, 18, 20, 22, and 24 GHz respectively.

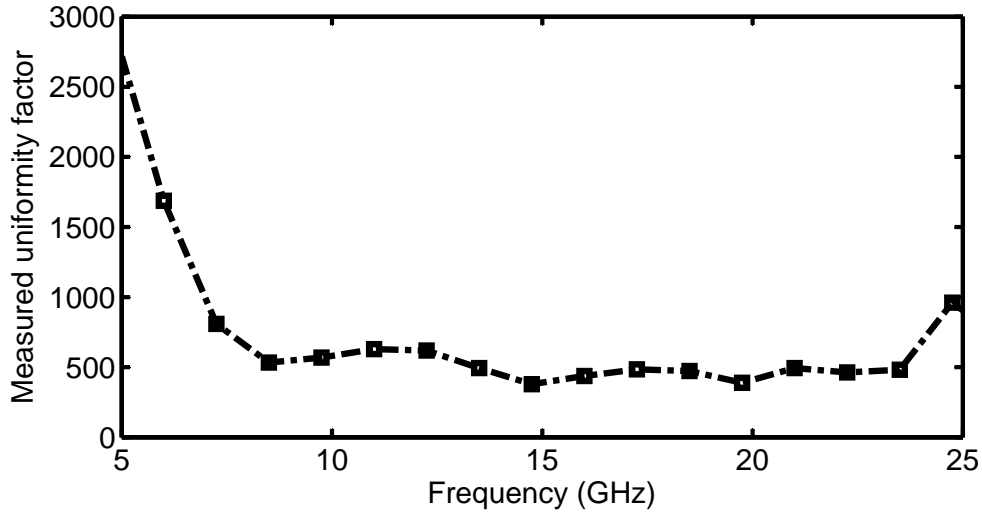


Figure 5.19: Measured uniformity factor of the fabricated DMTL impedance matching network.

and over the entire Γ_S plane using the following equation:

$$G_T = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} |S_{21}|^2 \quad (5.4)$$

Equation (5.4) includes both the effects of dissipation in the matching network itself and loss due to impedance mismatch. Fig. 5.20 shows the minimum power transfer ratio in dB for different VSWR values at different frequencies. Based on these results, the fabricated impedance matching network can be used to match different source impedances out to a maximum VSWR of 11.5:1 at 24 GHz with a power transfer ratio of better than 2.84 dB and with return loss better than 10 dB.

5.2.9 Intermodulation Distortion

In order to demonstrate the linearity performance of the fabricated CMOS-MEMS tunable impedance matching network, the intermodulation distortion analysis of the network was

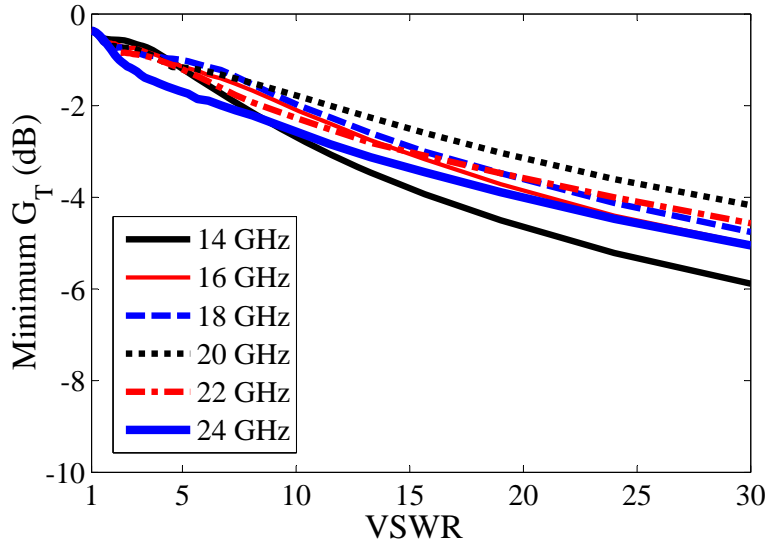


Figure 5.20: Minimum measured power transfer ratio G_T of the network versus VSWR at different frequencies.

performed using a two-tone measurement setup as shown in Fig. 5.21. The output spectrum of the impedance matching network for $f = 20$ GHz and $\Delta f = 1$ kHz when both the input and output ports are terminated by 50Ω RF probes is presented in Fig. 5.22(a). The measured third order intermodulation products (IM3) versus the input power at $\Delta f = 1$ and 10 kHz at $f_o = 20$ GHz without any DC bias voltage applied to the MEMS switches

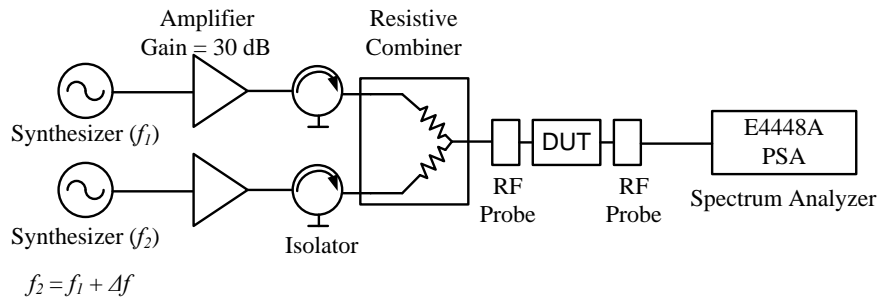


Figure 5.21: Two-tone intermodulation distortion measurement setup.

are also presented in Fig. 5.22(b). From these results, the measured third order intercept point (TOI) is 33 dBm and 39 dBm for $\Delta f = 1$ kHz and $\Delta f = 10$ kHz, respectively. For higher Δf values, the third order intercept point is expected to be even higher and cannot be measured due to limitations of the test setup in Fig. 5.21.

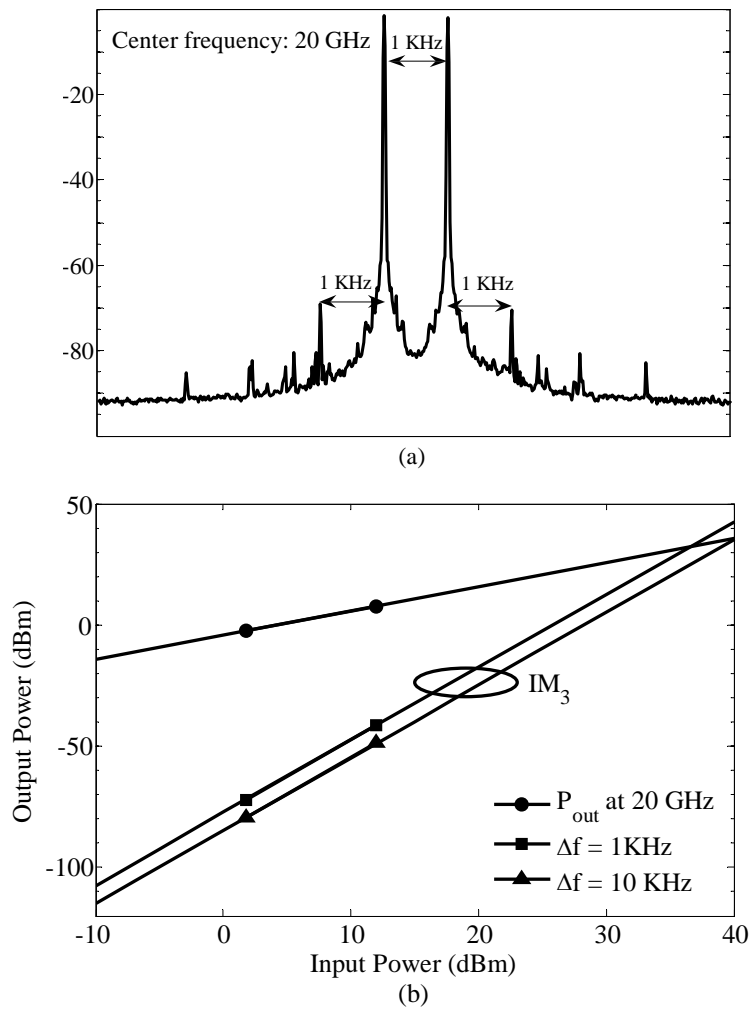


Figure 5.22: (a) Measured output spectrum for $f = 20$ GHz and $\Delta f = 1$ kHz, (b) IM3 products versus the input power and Δf .

5.3 Reconfigurable Amplifier with Tunable Matching Networks in 0.18- μm CMOS Technology

In this section, a reconfigurable CMOS amplifier operating at 5.2 GHz for WLAN applications is designed and fabricated in TSMC 0.18- μm CMOS technology. The amplifier utilizes lumped-element tunable MEMS impedance matching networks implemented using integrated CMOS-MEMS tunable capacitors and micromachined inductors with high quality factor and low loss. At the operating frequency of the amplifier, the lumped-element approach is superior to the transmission line based impedance matching networks due to the large on-chip wavelength increasing the chip real state. The reconfigurable MEMS impedance matching networks enable the amplifier to operate with an optimum power gain under variable load and source impedance conditions. The integration of MEMS in a standard CMOS technology allows the single-chip implementation of this amplifier.

5.3.1 CMOS-MEMS Process for the 0.18- μm CMOS Technology

Fig. 5.23 presents the CMOS-MEMS processing steps developed for TSMC 0.18- μm one-poly six-metal 1P6M RF-CMOS technology. The CMOS-MEMS processing is similar to the processing previously described in Chapter 4 for the implementation of parallel-plate MEMS tunable capacitors and capacitive RF MEMS switches using the 0.35- μm CMOS technology with the difference that for the 0.18- μm technology there are more metal layers available that can be used as MEMS structural layers. As shown in Fig. 5.23, M_5 and M_3 aluminum layers are used as the structural layers for the top and bottom plates of the MEMS tunable capacitor, respectively, while top-most metal layer M_6 is used as the RIE mask and M_4 is used as the sacrificial layer for MEMS release. Besides the ability to integrate MEMS tunable capacitors in a CMOS chip using the proposed processing, it also allows the integration of micromachined inductors with high quality factor. This is

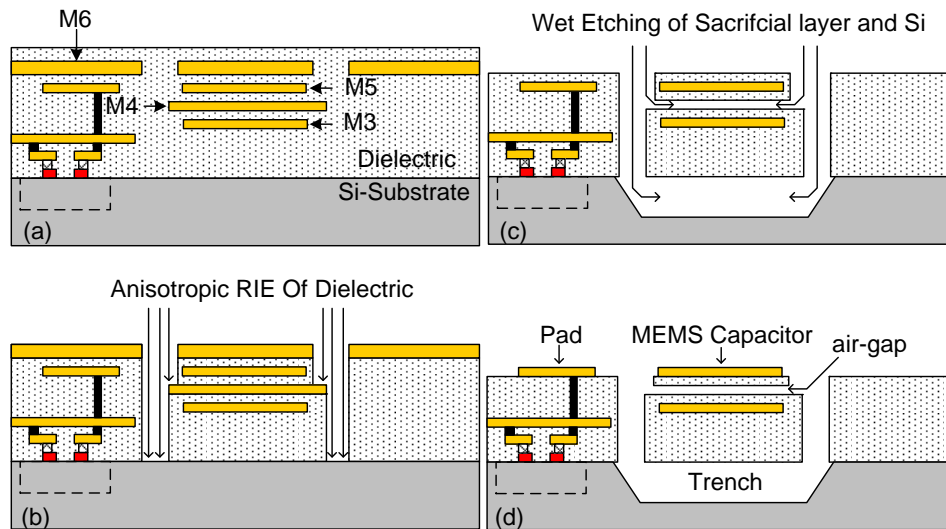


Figure 5.23: CMOS-MEMS processing steps required to integrate the MEMS parallel-plate capacitors in the 0.18- μm CMOS technology.

possible by removing the CMOS dielectric layer in the vicinity of the the inductors and by subsequently removing the low-resistivity silicon substrate underneath.

5.3.2 Reconfigurable Amplifier Design

The circuit schematic of the CMOS amplifier with reconfigurable input/output impedance matching networks using MEMS tunable capacitors is presented in Fig. 5.24. A cascode configuration is used to increase the stability of the N-MOS RF transistors. The size of the transistors was selected in order to maximize the maximum frequency of oscillation ($W/L = 32 \times 2.5 \mu\text{m} / 0.18 \mu\text{m}$). The cascode transistors are biased at $V_{DD} = 1.8 \text{ V}$ and $V_{G1} = 1 \text{ V}$. A load-pull simulation is performed in ADS using the available transistor models to obtain the optimum input and output matching conditions for the maximum available power gain and the minimum noise figure. Table 5.5 summarizes these simulation results.

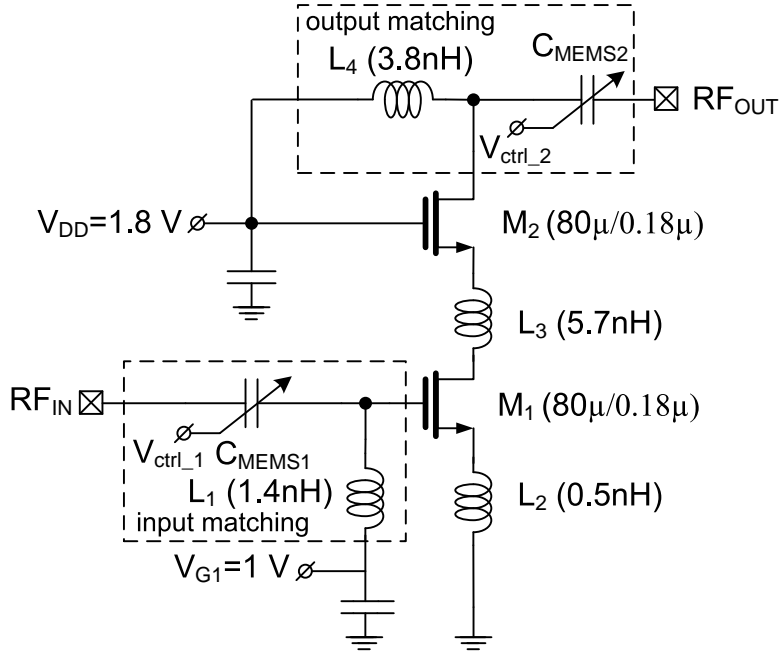


Figure 5.24: Schematic of the 5.2 GHz single-stage cascode amplifier.

Table 5.5: Optimum Source and Load Impedances

Condition	Optimum Z_{source}	Optimum Z_{load}
$MAG^a = 22 \text{ dB}$	$20.6 + j92.8 \text{ ohm}$	$135.6 + j30.8 \text{ ohm}$
$NF_{min}^b = 0.57 \text{ dB}$	$93.1 + j340 \text{ ohm}$	$86.8 + j340 \text{ ohm}$

^a Maximum Available Gain.

^b Minimum Noise Figure.

It is not possible to obtain both minimum noise figure and maximum power gain at the same time therefore a compromise has been made between the two. The input and output matching networks are designed so that at 0 V DC bias voltage for the CMOS-MEMS tunable capacitors the simulated maximum gain of the amplifier is 12.8 dB and the noise figure is 2.3 dB, respectively. The required source and load impedances to satisfy these conditions are $Z_{source} = (22 + j67) \Omega$ and $Z_{load} = (52 + j239) \Omega$, respectively. By adjusting

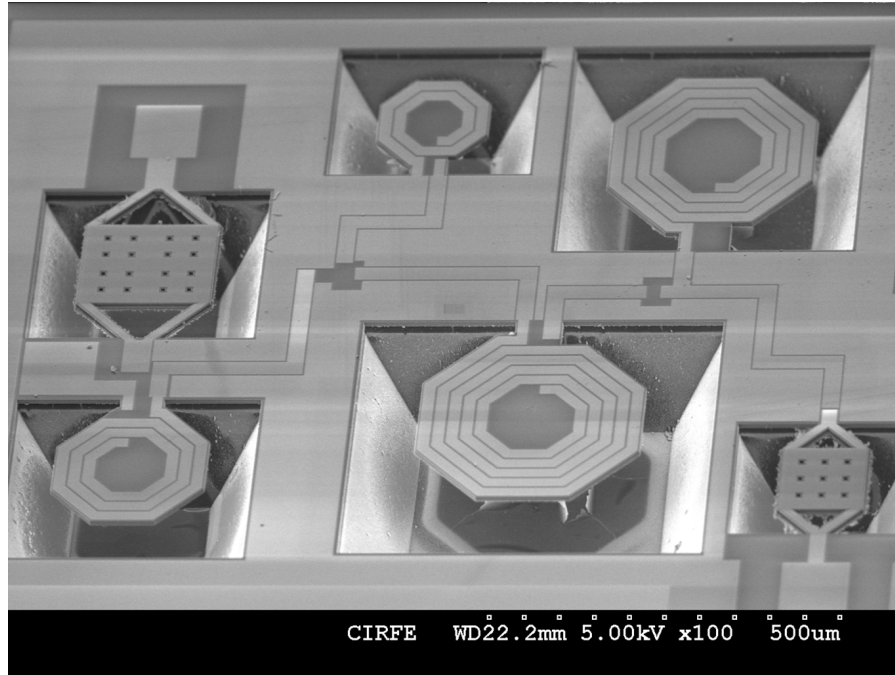


Figure 5.25: SEM image of the amplifier circuit with integrated CMOS-MEMS capacitors and inductors.

the two DC bias voltages $V_{ctrl,1}$ and $V_{ctrl,2}$ it is possible to maintain the gain of the amplifier under variable source and load impedances as will be explained through the measurement results in a later section. Fig. 5.25 shows the SEM image of the fabricated amplifier circuit with integrated CMOS-MEMS tunable capacitors and micromachined inductors. The total chip area is $1.1 \times 1.4 \text{ mm}^2$ including both the RF and the DC bias pads. The deep trench in the silicon substrate and under the capacitors and inductors completely isolates these passive components from the low-resistivity silicon substrate improving the Q -factor and reducing the insertion loss caused by the passive elements.

5.3.3 Experimental Results

The performance of the proposed reconfigurable amplifier is characterized through on-wafer S-parameter measurements while the effects of the probes and the connecting cables were de-embedded by standard SOLT calibration. Operated at a 1.8 V supply voltage, the fabricated amplifier consumes 14.5 mA of DC current. Fig. 5.26 shows the measured and simulated gain (S_{21}) and input/output reflection coefficient of the amplifier for $P_{in} = -10$ dBm and when the input/output ports of the amplifier are terminated with 50Ω loads. The measured gain of the amplifier is above 10 dB between 5-5.9 GHz and the amplifier maintains an input/output return loss better than 10 dB within the band. A maximum measured gain of 14.3 dB is obtained at 5.4 GHz.

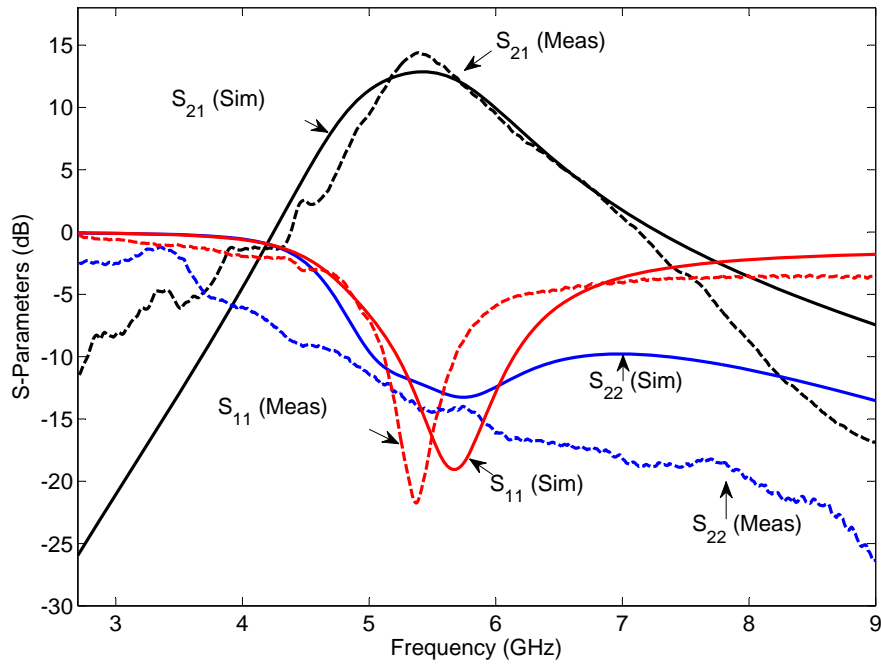


Figure 5.26: Measured and simulated S-parameters of the reconfigurable amplifier when the load/source impedance is 50Ω .

The theoretical maximum tuning range of the parallel-plate CMOS-MEMS tunable capacitors used in the input/output matching networks is 77%. The top and bottom plates of these capacitors consists of a composite Al/SiO₂ and SiO₂/Al/SiO₂ layers, respectively. By employing the difference in the residual stress values between the metal and dielectric layers of the CMOS process a curled-plate structure can be achieved. This curled-plate structure will enhance the maximum tuning range of the proposed CMOS-MEMS variable capacitors as reported in [77]. The measured tuning range of the MEMS capacitor in the input matching circuit is from 0.33 pF to 0.74 pF or 124% for a DC bias voltage $V_{ctrl,1}$ between 0 to 60 V. The maximum tuning for the second MEMS capacitor in the output matching network is between 0.13 pF and 0.34 pF or 162% with an actuation voltage up to 60 V. The reconfigurable input/output impedance matching networks can compensate for the variations in the source/load impedances. Fig. 5.27 shows the performance of the input matching network when it is used to match different source impedances on the Γ_S plane to $Z_{source} = (22+j67) \Omega$. As seen in this figure a fairly wide area of the Smith chart is covered with an impedance matching better than 10 dB which corresponds to maximum variation of $\pm 2\%$ in the gain of the amplifier. The load impedance can also change due to the variable operating conditions. The measured Smith chart coverage of the output impedance matching network is presented in Fig. 5.28. Measurement results for the amplifier when the output port is terminated with a non-50 Ω load are presented in Fig. 5.29. The maximum gain of the amplifier is improved from 11.2 dB to 14.4 dB by tuning the CMOS-MEMS variable capacitor in the output impedance matching network while an output reflection coefficient better than 10 dB is achieved within 4.6 to 5.9 GHz for the tuned state.

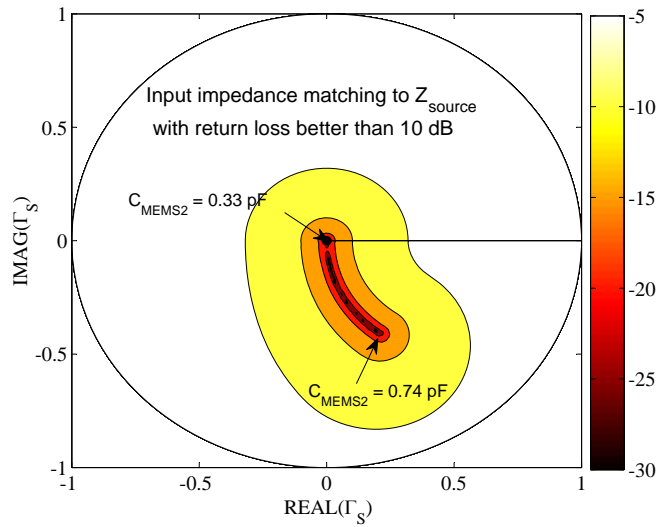


Figure 5.27: Measured Smith chart coverage of the input impedance matching network when used to match non-50 Ω source impedances to $Z_{source} = (22+j67) \Omega$.

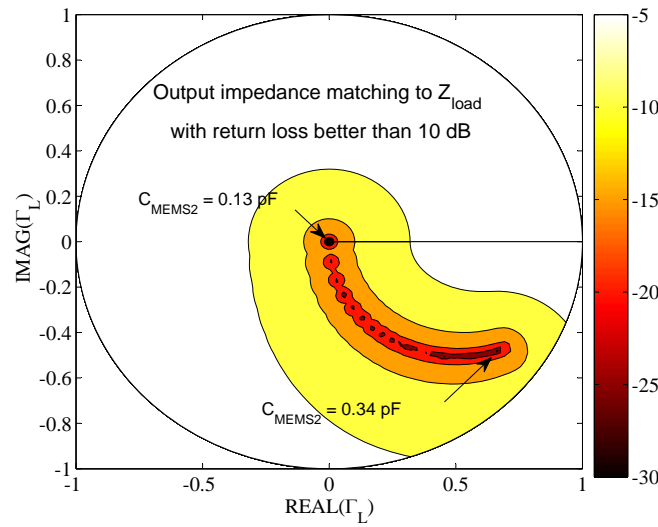


Figure 5.28: Measured Smith chart coverage of the output impedance matching network when used to match non-50 Ω load impedances to $Z_{load} = (52+j239) \Omega$.

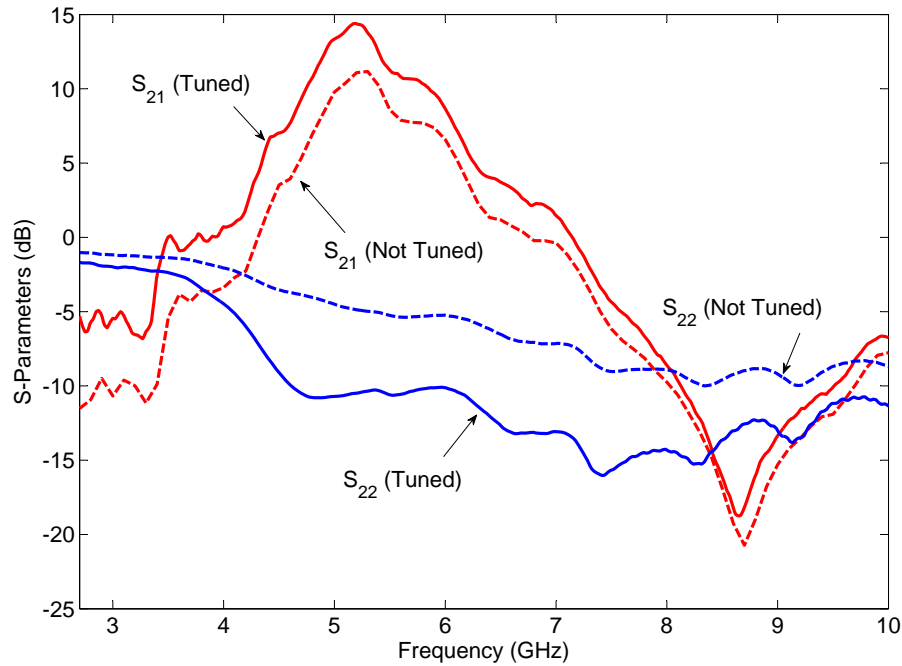


Figure 5.29: Measured gain and output reflection coefficient of the reconfigurable amplifier when the output port is terminated with a non-50 Ω load for both tuned and un-tuned states.

5.4 Summary

Tunable MEMS impedance matching networks integrated in standard CMOS technologies are presented for the first time. The first impedance matching network is based on a DMTL structure utilizing a novel slow-wave CPW structure with 8 capacitive MEMS switches fabricated in a standard 0.35- μm CMOS process. Measurement results demonstrate that the network can be used to match impedances on the Smith chart with a maximum VSWR of 11.5:1 with a return loss better than 10 dB and a power transfer ratio of better than 2.84 dB at 24 GHz. For the first time, a single-chip reconfigurable amplifier with MEMS impedance matching networks integrated in a standard 0.18- μm CMOS process is demonstrated. The amplifier achieves a maximum gain of 14.3 dB at 5.4 GHz when the input/output ports are

terminated by 50Ω loads. With the use of tunable MEMS impedance matching networks, a constant gain of the amplifier is achieved for variable source and load impedances. The proposed integrated impedance matching networks can also be used to tune the center frequency of the amplifier or compensate for variations in the active device parameters due to temperature drift or fabrication tolerances. The implementation of the tunable MEMS impedance matching network with CMOS circuits on the same chip allows for fully integrated silicon solutions for future multiband reconfigurable RF front-ends.

Chapter 6

Conclusions

The main focus of this thesis is on the development of high performance reconfigurable impedance matching networks using MEMS technology and on the development of a CMOS-MEMS processing that allows the implementation of varactors, switches and impedance matching networks using commercially available standard CMOS technologies. The major contributions of the research are summarized below. Some of the research problems and issues that can be addressed as a future work are also listed in this chapter.

6.1 Contributions

The major contributions of this thesis are outlined as follows:

- Two novel structures are proposed for the implementation of MEMS tunable impedance matching networks. The first structure is based on a slow-wave distributed MEMS transmission line structure loaded with tri-state MEMS capacitive switches and optimized for an extended frequency band of operation. The proposed design consists of 8 tri-state RF-MEMS switches producing 6561 (3^8) impedance states. The size

of the tunable matching network fabricated on an alumina substrate is compact ($4.4 \times 1.9 \text{ mm}^2$). The measured results demonstrate a wide coverage of the Smith chart between 5 GHz to 20 GHz. The power transfer ratio of the network is better than 4.3 dB for a wide range of impedances. The second structure presents a novel approach to construct low-loss reconfigurable impedance matching networks and tuners using MEMS series-contact switches and periodic defected-ground-structures (DGSs) implemented on coplanar waveguide transmission lines. The proposed DGS structure results in an improved insertion loss and power handling capability in comparison with the conventional RF MEMS impedance matching networks. The network consists of 12 DGSs and RF MEMS series-contact switches producing 4096 (2^{12}) impedance states. The tunable matching network was fabricated on an alumina substrate and is only $1.3 \times 3.6 \text{ mm}^2$ in size. The measured results demonstrate a wide coverage of the Smith chart with a maximum VSWR of 12:1 at 60 GHz. The measured loss of the network when used to match a 10Ω load to 50Ω from 22 GHz up to 40 GHz is only 0.5 dB.

- A new CMOS-MEMS processing and integration technique is developed at the Centre for Integrated RF Engineering (CIRFE) at the University of Waterloo that allows for the first time the integration of tunable or reconfigurable RF MEMS devices with vertical motion in a CMOS chip as opposed to the previously reported CMOS-MEMS post-processing techniques. The process is applicable to any standard CMOS process such as TSMC 0.35- μm or 0.18- μm CMOS technologies. The MEMS structures are formed out of the available metal and dielectric layers and released by removing the silicon substrate or by etching one or more metal layers as the sacrificial layer. One advantageous feature of the developed CMOS-MEMS processing is that it does not require any extra film deposition or lithographic patterning steps as opposed to the known MEMS fabrication processes. The proposed CMOS-MEMS integration

process is optimized for general RF applications. Nevertheless, the process is also applicable to many other MEMS devices.

- RF MEMS tunable parallel-plate capacitors with electrostatic actuation and parallel-plate structure are developed using the proposed CMOS-MEMS processing. The capacitors are built in 0.35- μm CMOS technology and have a quality factor that exceeds the quality factor of the semiconductor varactors available in CMOS technologies. A 2-pole coupled line tunable bandpass filter with a center frequency of 9.5 GHz and a 9% relative bandwidth is designed and fabricated using the proposed CMOS-MEMS tunable capacitors. A tuning range of 17% is achieved. The filter has an insertion loss of 5.66 dB and occupies a chip area of $1.2 \times 2.1 \text{ mm}^2$.
- Novel CMOS-MEMS capacitive type switches for microwave and millimeter-wave applications are demonstrated. The switches are fabricated using the 0.35- μm CMOS process and consist of composite metal-dielectric warped membranes. The warped-plate structure is used to increase the capacitance ratio of the switch. The switch demonstrates a measured capacitance ratio of 91:1 and a good RF performance from 10-20 GHz with an insertion loss less than 1.41 dB, return loss below 19 dB and an isolation between 19-40 dB. The proposed RF MEMS switches can be used in millimeter-wave CMOS RF front-ends where multiband functionality and reconfigurability is required.
- Integration of MEMS-based reconfigurable impedance matching networks in standard CMOS technologies is investigated. A novel 8-bit reconfigurable impedance matching network based on the distributed MEMS transmission line (DMTL) concept is presented that operates at 13-24 GHz frequency band. The network was extensively characterized in terms of the RF performance and intermodulation products for high-power millimeter-wave applications. The network is implemented using a standard 0.35- μm CMOS technology and employs a novel suspended slow-wave structure on

a silicon substrate. The suspended slow-wave structure results in a reduced total footprint and enhanced impedance coverage. The network demonstrates a wide coverage of the Smith chart up to a maximum VSWR of 11.5:1 with an impedance matching better than 10 dB and a power transfer ratio of better than 2.84 dB at 24 GHz. To our knowledge, this is the first implementation of a DMTL tunable MEMS impedance matching network using a standard CMOS technology. A reconfigurable amplifier chip for WLAN applications operating at 5.2 GHz is also designed and implemented. The amplifier can achieve maximum power gain under variable load and source impedance conditions by using the proposed integrated RF-MEMS impedance matching networks. The amplifier and the matching network were fabricated in standard 0.18- μm RF-CMOS technology. This is the first single-chip implementation of a reconfigurable amplifier using high-Q MEMS impedance matching networks.

In summary, the focus of this research has been on the development of reconfigurable impedance matching networks using MEMS technology. Table 6.1 compares the performance of the proposed MEMS impedance matching networks in this research with the previously reported matching networks implemented using other technologies such as semiconductor switches and varactors, BST capacitors and also MEMS technology. The MEMS technology and the integration with standard CMOS technologies enables the low-cost implementation of these impedance matching networks with improved performance and functionality and higher level of integration. However, there are still several unexplored issues such as packaging and reliability which need to be addressed under future work.

6.2 Future Work

There has been an extensive research and investigation of a wide range of topics in this thesis to advance the development of reconfigurable impedance matching networks using

Table 6.1: Comparison between the developed MEMS tunable impedance matching networks and other reported technologies.

publication	Frequency range	Max. VSWR	Max. loss	Return loss	IIP3/ Power handling	Technology
Ref. [22]	2.4 GHz ISM band	5	1 dB ($50\Omega \rightarrow 50\Omega$)	10 dB	22 dBm ($\Delta f=40$ MHz)	0.35- μ m CMOS semiconductor switches & off-chip inductors
Ref. [100]	16-20 GHz	12.33	3 dB at 18 GHz ($50\Omega \rightarrow 50\Omega$)	15 dB	NA	GaAs pHEMT switches
Ref. [23]	5-16 GHz	< 5	5-10 dB	NA	-1 dBm ($P_{out-1dB}$)	0.13- μ m CMOS semiconductor switches
Ref. [24]	1.95 GHz	< 5	1.15 dB at 1.95 GHz ($50\Omega \rightarrow 50\Omega$)	10 dB	46.3 dBm ($\Delta f=1$ MHz)	BST on Al_2O_3 ($Q = 23$ at 2GHz, 0V)
Ref. [28]	1.5-2 GHz	4 at 2 GHz	5.5 dB (all states)	NA	NA	BST on sapphire ($Q = 33$ at 2GHz, 0V)
Ref. [13]	10-30 GHz	12	3 dB (all states)	15 dB	NA	RF MEMS DMTL on quartz
Ref. [10]	4-18 GHz	NA (10 – 20 Ω to 50 Ω)	1.5 dB at 18 GHz (10 $\Omega \rightarrow$ 50 Ω)	16.5 dB	>30dBm ($\Delta f=10$ kHz)	RF MEMS DMTL on glass
Ref. [9]	20-50 GHz	NA (10 – 20 Ω to 50 Ω)	1-1.5 dB at 40 GHz (10 – 20 $\Omega \rightarrow$ 50 Ω)	10 dB	NA	RF MEMS DMTL on glass
This research [101]	5-20 GHz	24 at 20 GHz	4.3 dB (all states at 20GHz)	10 dB	NA	RF MEMS DMTL on alumina dual-beam switch
This research [102]	22-60 GHz	6.41 at 36 GHz	0.5 dB at 22-40 GHz (10 $\Omega \rightarrow$ 50 Ω)	12 dB	42 dBm ($\Delta f=10$ kHz)/ 12W	RF MEMS on alumina DGS structure
This research [103]	13-24 GHz	11.5 at 24 GHz	2.84 dB at 24 GHz (all states)	10 dB	39 dBm ($\Delta f=10$ kHz)	0.35- μ m CMOS CMOS-MEMS switches

MEMS technology and integration with CMOS technologies. There are several related research problems in this area that can be possibly explored in the future.

- An investigation of the proposed CMOS-MEMS devices is required in terms of life time and reliability characterization which plays an important role in the manufacturing and commercialization of the proposed CMOS-MEMS processing and fabricated devices. Environmental effects such as ambient temperature can influence the performance of these devices. For this reason, compensation techniques using closed-loop control systems, that can be integrated on the same CMOS chip, are required.
- The introduced CMOS-MEMS processing can be applied to other commercially available RF integrated circuit (RFIC) foundry processes such as GaAs microwave monolithic integrated circuits (MMIC), SiGe, sub-100 nm RF-CMOS, Integrated Passive Device (IPD) and many other technologies suitable for RF applications.
- The implementation of an intelligent adaptive impedance matching module on a single CMOS chip will be possible based on the developed CMOS-MEMS processing. This also requires design and fabrication of several novel components including RF power sensors, couplers, control units and MEMS driving circuitry. The realization of such an intelligent matching module will demonstrate more innovative aspects and possibilities for commercial exploitation of the research in this thesis.

APPENDICES

Appendix A

List of Acronyms

RF	Radio Frequency
PA	Power Amplifier
LNA	Low Noise Amplifier
BST	Barium Strontium Titanate
MEMS	Microelectromechanical Systems
RFIC	Radio-frequency Integrated Circuit
CMOS	Complementary Metal-Oxide-Semiconductor
DGS	Defected Ground Structure
TSMC	Taiwan Semiconductor Manufacturing Company
DMTL	Distributed MEMS Transmission Line
VSWR	Voltage Standing Wave Ratio
ISM	Industrial, Scientific and Medical
MMIC	Monolithic Microwave Integrated Circuits
HEMT	High Electron Mobility Transistor
GaAs	Gallium-Arsenide

PAE	Power Added Efficiency
pHEMT	pseudomorphic High Electron Mobility Transistor
SiGe	Silicon-Germanium
BiCMOS	Bipolar-CMOS
CMU	Carnegie Mellon University
LO	Local Oscillator
DUT	Device Under Test
CIRFE	Centre for Integrated RF Engineering
RIE	Reactive Ion Etching
PECVD	Plasma Enhanced Chemical Vapor Deposition
SOLT	Short-Open-Load-Transmission
IIP3	Third-Order Intermodulation Intercept Point
TOI	Third-Order Intercept
VLSI	Very Large Scale Integration
IMD	Intermodulation Distortion
BPSG	Borophosphosilicate Glass
ICP	Inductively Coupled Plasma
PAN	Phosphoric-Acetic-Nitric
KOH	Potassium Hydroxide
CPD	Critical Point Drying
CPW	Coplanar Waveguide
SSW	Suspended Slow Wave
S-CPW	Suspended Coplanar Waveguide
SSW-CPW	Suspended Slow Wave Coplanar Waveguide
HFSS	High Frequency Structure Simulator
ADS	Advance Design System
WLAN	Wireless Local Area Network

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