CDM Robust & Low Noise ESD protection circuits

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Sumanjit Singh Lubana

Abstract

In spite of significant progress during last couple of decades, ESD still affects production yields, manufacturing costs, product quality, product reliability and profitability. The objective of an ESD protection circuit is to create a harmless shunting path for the static electricity before it damages the sensitive electronic circuits. As the devices are scaling down, while ESD energy remains the same, VLSIs are becoming more vulnerable to ESD stress. This higher susceptibility to ESD damage is due to thinner gate oxides and shallower junctions. Furthermore, higher operating frequency of the scaled technologies enforces lower parasitic capacitance of the ESD protection circuits. Hence, increasing the robustness of the ESD protection circuits with minimum additional parasitic capacitance is the main challenge in state of the art CMOS processes. Furthermore with scaling, the integration of analog blocks such as ADC, PLL's, DLL's, oscillator etc. on digital chips has provided cheap system on chip (SOC) solutions. However, when analog and digital chip are combined into single mixed-signal chip, on-chip noise coupling from the digital to the analog circuitry through ESD protection circuits becomes a big concern. Thus, increasing supply noise isolation while ensuring the ESD protection robustness is also a big challenge.

In this thesis, several ESD protection circuits and devices have been proposed to address the critical issues like increased leakage current, slower turn-on time of devices, increased susceptibility to power supply isolation etc. The proposed ESD protection circuits/devices have been classified into two categories: Pad based ESD protection in which the ESD protection circuits are placed in the I/O pads, and Rail based ESD in which ESD protection

circuit is placed between power supplies. In our research, both these aspects have been investigated. The Silicon Controlled Rectifier (SCR) based devices have been used for Pad ESD protection as they have highest ESD protection level per unit area. Two novel devices Darlington based SCR (DSCR) and NMOS Darlington based SCR (NMOS-DSCR) having faster turn-on time, lower first breakdown voltage and low capacitance have been proposed.

The transient clamps have been investigated and optimized for Rail based ESD protection. In this research, we have addressed the issue of leakage current in transient clamps. A methodology has been purposed to reduce the leakage current by more than 200,000 times without having major impact on the ESD performance. Also, the issue of noise coupling from digital supply to analog supply through the ESD protection circuits has been addressed. A new transient clamp has been proposed to increase the power supply noise isolation. Finally, a new methodology of placement of analog circuit with respect to transient clamp has been proposed to further increase the power supply noise isolation.

Acknowledgements

I would like to express my deepest gratitude to my supervisor Prof. Manoj Sachdev for his technical guidance, moral support and encouragement. During my tough times, he was always there to guide, cooperate and help me in the best possible way. This thesis wouldn't have been possible without his support and guidance. I am really grateful to have him as my research supervisor. Moreover, I would like to thank Prof. David Nairn and Prof. Ajoy Opal for taking out their invaluable time to become my thesis reader.

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My special thanks to my family for their constant support, love and encouragement. Without their support I would have never completed my thesis.

Dedication

I would like to dedicate this thesis to my beloved mother. She made several sacrifices so I can be what I am today.

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Chapter 1
Introduction

It is very common to observe the effects of Electrostatic discharge (ESD) in our day to day life. The thunder lightning, standing of hair after touching the Van de Graaf generator or a shock felt when we touch each other or door knobs in a cold and dry winter day are all well known effects of ESD. The ESD phenomenon is a charge re-balancing act between two objects which have accumulated static electricity.

Static electricity is generated by the imbalance of the electrons on the surface of material by process known as tribo-electrification. The tribo-electric charge is accumulated on an insulator when it is rubbed against another insulator. The rubbing of the two insulators lead to one insulator gaining electrons and other losing electrons as shown in Figure 1-1. The insulator which gains electrons will accumulates a net negative charge and vice-versa. The amount of static charge accumulated on an object depends on the environmental factors such as relative humidity, electron affinity of the object, rate of separation of objects, contact area, pressure, and friction between the two materials [1].

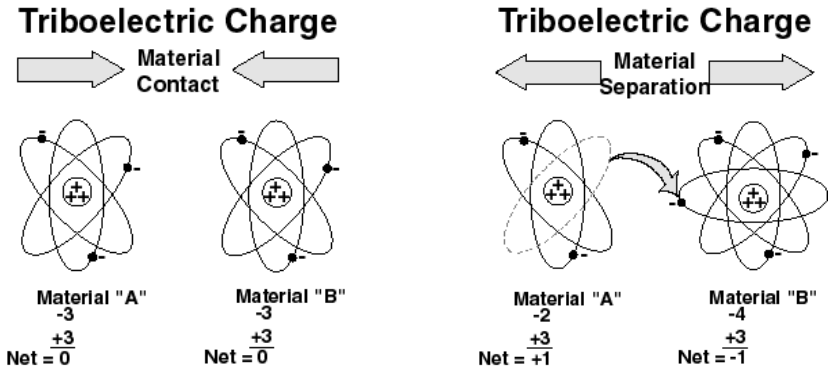


Figure 1-1: Tribo-electric Charging [2]

Table 1-1: Electrostatic potential & Humidity

Means of static generation	Electrostatic potential (V)	
	10-20 % Relative humidity	65-90% Relative humidity
Walking across a carpet	35,000	1,500
Walking on a vinyl floor	12,000	250
Picking up a polythene bag	20,000	1,200
Getting up from a polyurethane foam chair	18,000	1,500

The electrostatic voltage developed can be as high as a few kilo-volts. Table 1-1 [3] shows the typical electrostatic potential for both high and low humidity environments. High humidity environments produce lower electrostatic potential than low humidity environment. The high humidity environment has high moisture content, therefore more charge is conducted away in the environment through the material decreasing the electrostatic potential. As the potential created during ESD event is very high (in the order of 3 -35 kV), a discharge through a semiconductor device can result in device failure.

1.1 Motivation

The electrostatic discharge resulting from touching, rubbing and sliding during the Integrated circuit(IC) manufacturing can damage the IC [4, 6]. Figure 1-2 [7] shows a chart of the semiconductor failure causes for all the field returns analyzed the ESD account for 17% of

these failures. It was also reported by Wagner et al. [8] that ESD is responsible for more than 25% of the failures encountered. Thus the ESD has significant impact on reducing the yield of the semiconductor devices.

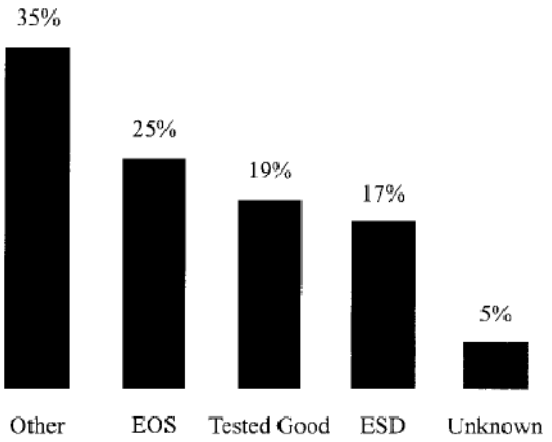


Figure 1-2: Field Return Failure Causes

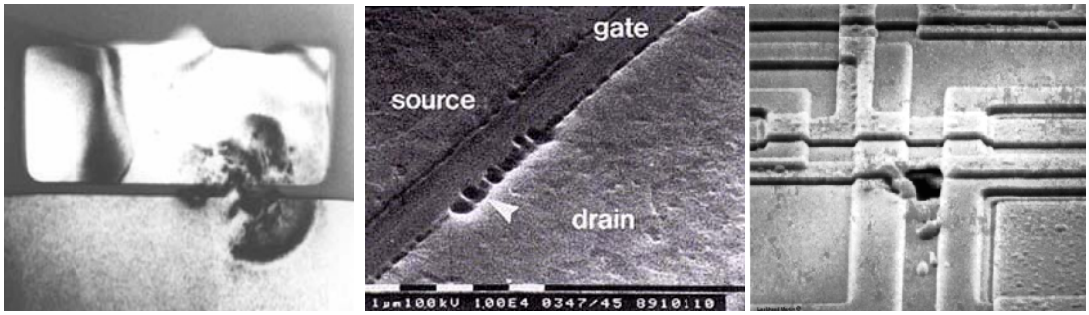
The ESD event affects an IC throughout a product's life. During the wafer-fabrication process clean rooms can generate charge over 20,000V. The electrostatic charge is generated due to the extensive use of synthetic materials in containers and tools used for transportation of wafers [9]. The electrostatic charge attracts airborne particles, these particles stick on wafer and alter the pattern produced on the circuit and hence lower the yield. Also, in wafer-fabrication the electrostatic charge accumulation erodes the pattern defined on the mask during photolithography process. Thus each circuit that is printed with this damaged mask will now be damaged [10][11]. There can be also direct ESD discharge on the wafer which can rupture thin gate oxide and damage junctions [10]. The ESD Hazards are also present during the assembly operation of the IC's. In the assembly operation, the wafers are sliced to separate the individual dies. The films used during the sawing of the wafer charges the dies

to a electrostatic voltage of 10000V. The dies are then transported and placed in the packages. The wires are then attached to the die to interface with the outer world and then lastly a package is formed around the die. During all these operations ESD events can occur [12].

The ESD event related failures can be mitigated in two ways:

1. By proper handling and grounding of the personnel and equipment during manufacturing and usage of chips.
2. By adding an on-chip ESD protection circuit. During an ESD event the ESD protection circuit triggers, and carries the high current away from the internal circuitry thus protecting the sensitive semiconductor device.

The IC manufacturers cannot guarantee how the customers are going to handle the products, so all the IC manufacturers use on-chip ESD protection circuits to reduce the ESD related damages.



(a) (b) (c)

Figure 1-3: (a) Gate oxide damage (b) Drain junction filamentation (c) Interconnects damage [13]

Figure 1-3 shows the effects of the ESD stress on the semiconductor device. As discussed previously the amount of electrostatic charge deposited can easily exceed several kilo-volts. These high voltages create high electric field and electric current in semiconductors that can easily rupture thin gate oxide in semiconductor devices. Consider a 90nm technology, the gate oxide thickness is 18Å and the dielectric breakdown electric field is of the order of 10-15MV/cm. A maximum DC voltage of 2.7 V ($V_{MAX} = E_{MAX} * t_{OX}$) can easily damage a semiconductor device. In a typical CMOS technology, the thin oxide gate transistors of input buffers are directly tied to the inputs of the pin. Thus nano-metric technologies are easily vulnerable to gate oxide breakdown (Figure 1-3(a)).

The high current density can also cause melting of semiconductor devices due to Joule's heating. The Joule's heating is the resistive heat generated by electric current moving through electric field. If this high current is localized in an area of high electric field thermal runaway can occur leading to short circuit or open circuit or modifying characteristics of device like increase in leakage current, shift in threshold voltage etc. Thermal runaway is a positive-feedback process as silicon has a negative thermal resistance coefficient. An increase in lattice temperature lowers the resistance of silicon, increasing the current which further increases the lattice temperature until the semiconductor device melts. Figure 1-3(b) and Figure 1-3(c) shows the effects of high current density on the semiconductor devices.

Thus the ESD damages can be classified into soft and hard failures. In the soft failures the device has a partial damage such as increase in the leakage current, shift in threshold voltage. The basic functionality of the circuit works fine, but it may fail certain corner cases. On the

other hand, in the hard failures the semiconductor device is completely destroyed and the basic functionality is lost.

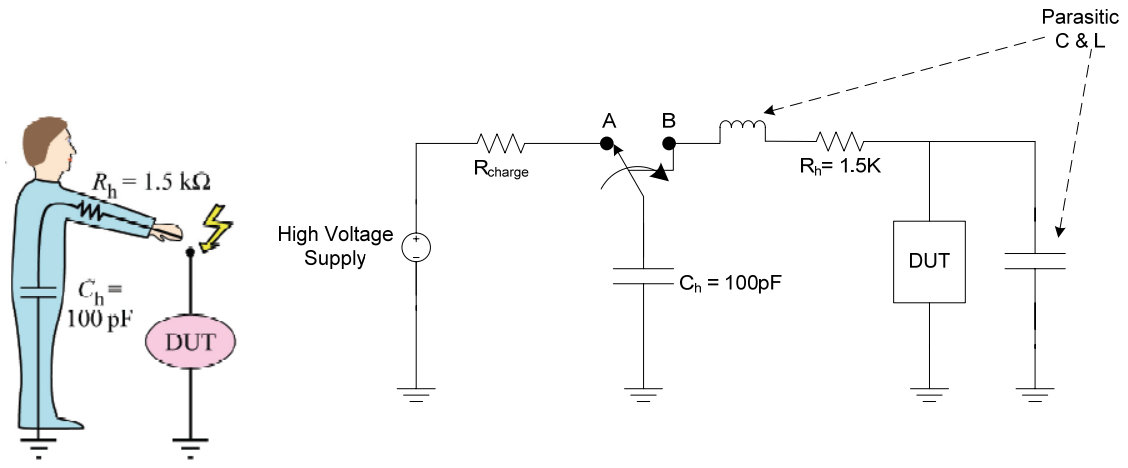
1.2 ESD test models and test methods

In order to fully characterize the susceptibility of Device under Test (DUT) to ESD damage and for purposes of reproduction of ESD event, there should be ESD models which accurately simulate the behavior of real ESD events. The models should be standardized for consistent and reliable parameters which can help in designing ESD protection circuits. The ESD test models can be classified into three categories:

1.2.1 Human Body Model (HBM)

Human Body Model (HBM) simulates the impact of charged human touching a grounded DUT. The human body can accumulate charge to high voltage by walking across a carpet. The amount of charge accumulated may vary from human to human depending on selection of footwear, posture (standing or sitting) etc. The large variability in the Human Body Model (HBM) makes it clear that a standard model should be developed for consistency. Figure 1-4 shows the standard model used to simulate the HBM stress.

In this model, $C_{h\ and}$ R_h represent body capacitance and resistance and their values have been standardized in [15] standard. To test the DUT for a certain HBM ESD stress, the capacitor (C_b) is charged to specified ESD stress level and then it is discharged through the DUT by changing the position of switch to B.



(a) (b)

Figure 1-4: HBM (a) Illustration (b) Model

1.2.2 Machine Model (MM)

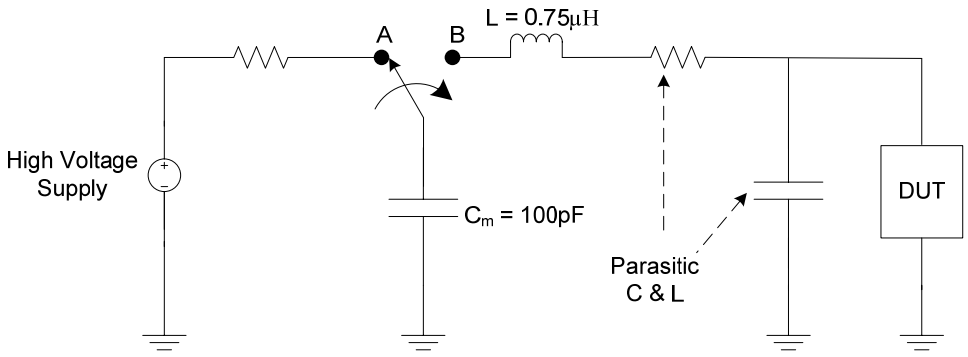


Figure 1-5: Machine Model

Machine Model (MM) simulates the discharge of charged machines through the grounded DUT. Thus, it models the handling of semiconductor devices by automated assembly machines. The model is implemented by replacing impedance in the HBM by impedance of machines. As different machines have different impedances so standard values of impedance

(C_m = 100pF and L = 0.75μH) has been defined in [16] standard. The MM is shown in Figure 1-5.

1.2.3 Charged Device Model (CDM)

The Charged Device Model (CDM) models the electrostatic discharge occurring between the charged chip and grounded surface. The grounded surface can be a hard grounded surface or a large charge sink like a metal work table or pool. The CDM stress is most difficult to

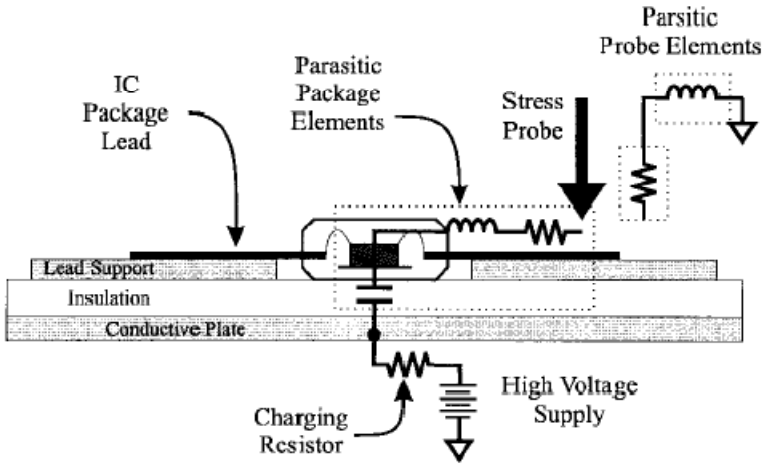


Figure 1-6: CDM ESD with parasitic [7]

reproduce and is increasingly becoming a concern for nano-metric technologies. The CDM stress can occur during the packaging of the chip die or during testing of the chip. The die can get charged tribo-electrically by assembly lines or manufacturing machines. When the die is placed in the package, electrostatic charge can discharge through grounded package through a low impedance path. Similarly, the CDM stress can occur during the testing of the chip where a part can get charged during handling of the chip. When the part comes in contact with the tester's pin, it discharges. The amount of discharge current depends on

capacitance of the total chip. So, the package size and design of the circuit have a strong influence on the peak amplitude current.

1.2.4 Comparison between HBM/MM/CDM

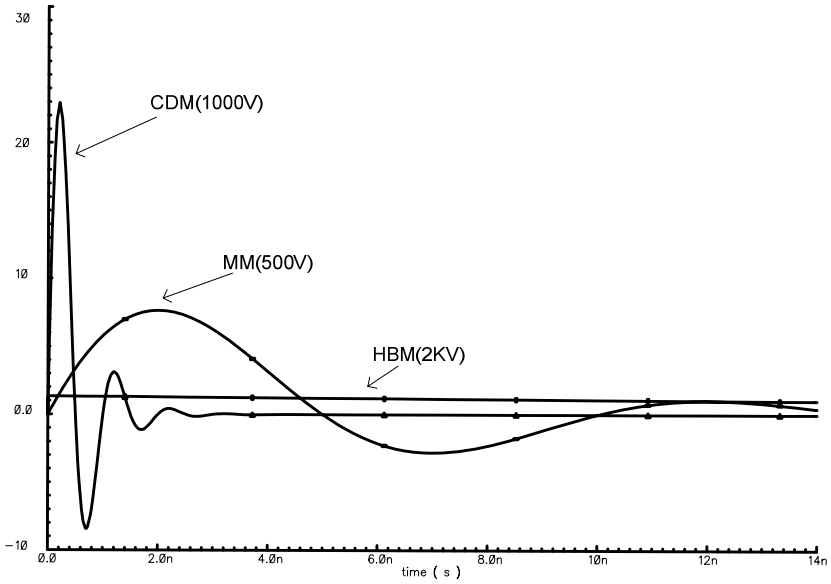


Figure 1-7: HBM, MM & CDM Currents

Figure 1-7 shows the current waveform when HBM, MM and CDM stress is applied to DUT. It is can be observed that the CDM stress current has highest peak current and smallest rise time (300-500 ps) as compared to MM and HBM. The HBM stress current has smallest peak current (1.20-1.48 A), large rise time (2.0-10 ns) and large decay time (130-170 ns). The MM has higher peak current (~10.4 A) and smaller rise time (1-2 ns) than HBM. The MM has higher peak current due to higher capacitance and hence lower overall impedance of the path which results in higher current densities during the MM discharge. Therefore, even though MM damages are similar to that of HBM, the MM related ESD failures occur at much lower threshold levels.

1.2.5 TLP/ Vf-TLP testing

A single characterization model is not sufficient to guarantee the robustness against all the ESD failures. It is possible a circuit passes test for one model for example HBM and fails for another model like CDM. Also, the characterization models only give the result whether a circuit passes or fails a test, they don't give an insight on how the protection circuit is working and how and where they fail or pass.

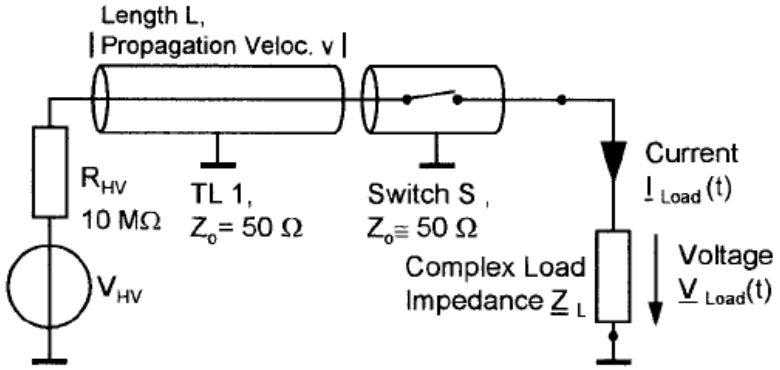


Figure 1-8: TLP basic set up [18]

Tim Maloney [17] introduced the use of Transmission-line Pulse (TLP) in order to characterize and design ESD protection circuits. A schematic of basic TLP set up is shown in Figure 1-8. The basic principle is to charge a 50 Ω coaxial cable using a high voltage source and then discharging it through a 50 Ω resistor into ESD protection circuit. The resultant output waveform is a rectangular voltage pulse, whose pulse width is directly proportional to the length of the transmission line cable and amplitude directly proportional to the amplitude of the pre-charged level.

This constant rectangular or square pulse current is driven into the DUT and the voltage across the DUT is observed. Thus the behavior of device (DUT) for a given current stress is

studied. The peak amplitude of the constant current source is increased in specified steps until the device fails. The device failure is observed by studying the leakage current of the device under normal operating conditions after each current stress. A large increase in leakage current indicates the failure of a device. Thus the IV characteristics of the devices can be extracted for high current and voltages. It has been shown by several researchers [19-20] that there is strong correlation between TLP failure levels and HBM/MM protection levels. Thus the TLP measurement is used extensively for the characterization of semiconductor devices and to qualify them for HBM/MM immunity.

The researchers have also tried to correlate the TLP measurement data with the CDM stress. In order to emulate high-current conditions similar to CDM, a large current pulse of rise time closer to CDM rise time is required. It is very difficult to obtain a fast transient pulse (1-3ns) with a rise time of 300-500ps with a normal TLP setup. Also, CDM stress is a one pin test while the TLP set up requires a set of two pins. Therefore to measure the device dynamics such as trigger speed of a device, transient current under CDM stress conditions etc. , Horst Geiser [18] modified the basic TLP set up to realize a Vf-TLP. In this setup, a square pulse of short duration and small rise time is applied to the DUT by discharging a pre-charged transmission line into the DUT. The incident pulse is reflected from the DUT and the average current and voltage over the time interval between 65% and 95% of pulse width is recorded. Thus the IV characteristics of the devices can be extracted for all the current and voltages. The difference between the conventional TLP and Vf-TLP is that Vf-TLP doesn't wait for voltage across the DUT to reach the equilibrium value.

1.3 Challenges in the nano-metric technology

The designing of ESD protection circuit is becoming more and more challenging with the scaling down of the CMOS technology. The ICs are becoming more and more susceptible to ESD damage as they are becoming smaller and faster due to higher current density and lower oxide breakdown voltage. In addition, the ESD protection circuits can't be scaled with the technology for example an ESD protection circuit in 180nm technology is not guaranteed to provide same protection level in 130nm technology. In this section we will discuss some of the challenges in designing ESD protection circuits.

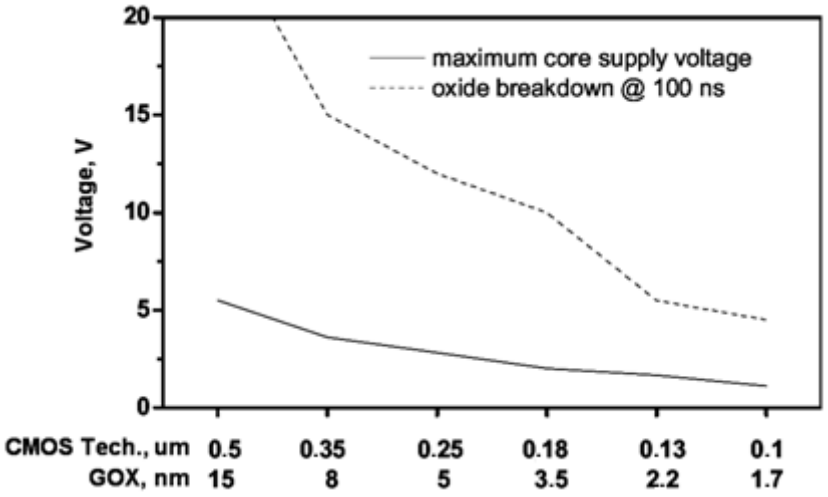


Figure 1-9: Breakdown voltage of gate oxide for 100 ns duration stress pulses and supply voltage as a function of CMOS technology generation [21]

1. **Oxide Breakdown Voltage**: Figure 1-9 shows the oxide breakdown voltage when a 100ns pulse (similar to HBM event) is applied to minimum gate length transistor as a function of CMOS technology. It is evident that as we are scaling down the technology the oxide breakdown voltage is decreasing for example in 0.18 μm technology, oxide failure occurs at

~10 V and in 0.09 μm technology it occurs at ~5V. Hence, ESD failures occur at a much lower voltage.

2.**CDM failures:** Unfortunately, traditional ESD protection strategies which are effective against HBM and MM stresses are not effective against CDM stresses in nano-metric regime. The reason is that in nano-metric technologies the damages (gate oxide, junction breakdown) occur at lower voltages. Secondly, relatively slow ESD protection circuits are not able to trigger quickly enough to dissipate the ESD energy associated with CDM stress. Thirdly, the scaling down of CMOS technology has resulted in an increase in complexity of system on chip (SOC) because more and more components can now be packaged into the same area. Hence the number of pin count has increased, so we require bigger packages to pack the dies. The bigger complex packages require higher decoupling capacitances for high speed which result in higher CDM discharge currents through the device. Finally, the advancement in the processing and automated manufacturing has resulted in higher chips failing due to CDM stress [21]-[24]. Also, with advancement in CMOS manufacturing and with evolution of more efficient production control methods, the HBM/MM standards can be lowered [25] without affecting the yield. Thus the failures in chip due to CDM stress are increasing.

3.**Noise coupling from digital supply to analog supply:** The scaling down of CMOS process technology has increased degree of integration, enabling growth of mixed-signal circuits. The integration of analog blocks such as ADC, PLL's, DLL's, oscillator etc. on digital chips has provided cheap system on chip (SOC) solutions. However, when analog and

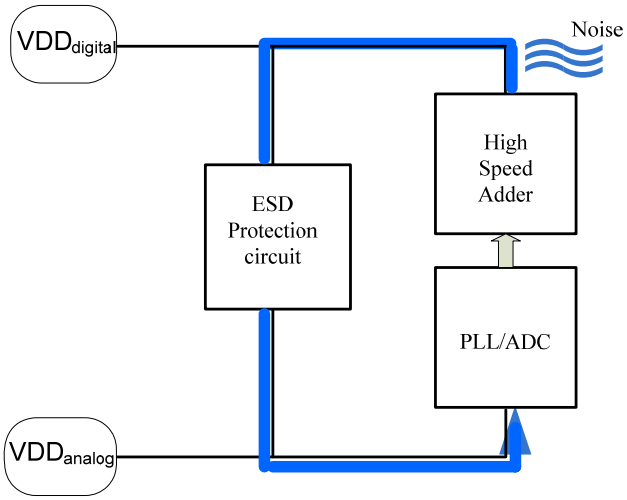


Figure 1-10: Noise Coupling from Digital Supply to Analog Supply

digital chips are combined into one single mixed-signal chip, on-chip noise coupling from the digital to the analog circuitry becomes a big concern. This problem can be solved by separating the on-chip power distribution networks for the analog and digital circuits. For noise immunity these power distribution networks should be isolated, however for ESD robustness of I/O pads there should be ESD protection circuits between the analog and digital supplies. The noise coupled through ESD networks significantly degrades the performance of mixed-signal circuits. Figure 1-10 shows a block diagram of such a system where noise generated from digital block (High speed adder) propagates to the analog block (PLL/ADC) through ESD protection circuit degrading the performance and hence increasing the jitter of PLL. This coupling noise cannot be suppressed easily because reducing the noise usually leads to the degradation of the ESD performance. Therefore, clamps should be optimized not only for ESD performance, but also for noise cancellation.

4. Other effects:

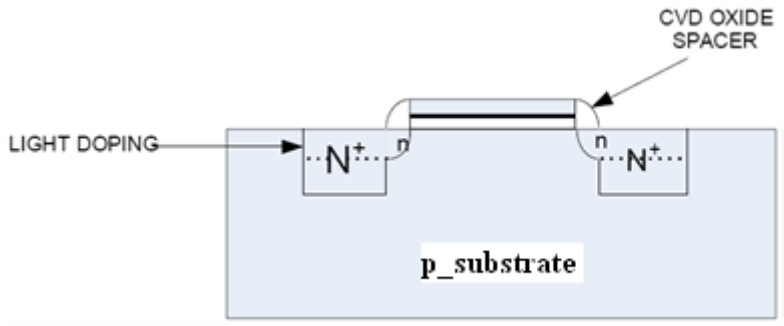


Figure 1-11: LDD in NMOS transistors [26]

The nano-metric technologies have several process enhancements to counteract the effects of the scaling like LDD, silicidation, scaling of interconnects etc. In the LDD structure, narrow, self aligned, n-regions are introduced between the n^+ source drain diffusions in the p-substrate as shown in Figure 1-11. This spreads the high electron field at drain pinch off region, increasing the breakdown voltage and reducing the impact ionization effect and hence the hot-electron effect. However, the introduction of LDD structures exacerbates the constraints for designing the ESD protection circuits. The shallower LDD diffusion regions have a greater current density for a given current level. There is more localized heating, and hence the device will fail at a lower ESD stress [27-30]. Also, the introduction of silicidation to reduce the ballast resistance of the transistor has an adverse effect on ESD performance. The decrease in the ballast resistance leads to current localization by concentrating current flow at the surface of device. Also scaling of interconnects has an adverse effect on scaling. Each technology scaling usually reduces thickness and pitch as compared to previous technology, while maintaining the aspect ratio. Thus the sheet resistance increases, line capacitance decreases and hence it lowers the maximum current carrying capacity [31].

1.4 Summary and Thesis Outline

In this chapter, an insight into how electrostatic discharge takes place has been given. The failure mechanisms associated with electrostatic discharge in semiconductor devices has also been discussed. The three test models HBM, MM, CDM and test methods TLP/Vf-TLP used in the semiconductor industries to qualify the devices have also been presented. Finally, the challenges associated with designing of ESD protection circuits as we are scaling down the semiconductor technology have also been discussed.

The rest of thesis is partitioned into three parts. The Chapter 2 focuses on ESD protection methodologies adopted in the semiconductor chips. It discusses the two different types of ESD protection devices: snapback devices and non-snapback devices. The Chapter 3 discusses the snapback devices. Two novel snapback ESD protection devices with superior CDM stress handling capability, lower triggering voltage have been discussed. In Chapter 4 non-snapback devices have been discussed. A new ESD protection clamp with better stability and performance has been presented. Also, ESD protection circuits have been presented to address the critical issues like leakage current and noise coupling from digital to analog supply. Finally, conclusion and future work is presented in Chapter 5.

Chapter 2
ESD Protection methodologies and devices

2.1 ESD zapping modes

The ESD stress can occur between any two arbitrary pins. The stress voltage can be positive or negative depending on the direction of applied stress. In general, the device pins are stressed with respect to power and ground supplies. So, depending on direction of the applied stress and discharge path, there can be four possible zapping modes. These modes are shown in Figure 2.1 PS-mode, NS-mode, PD-mode and ND-mode [32].

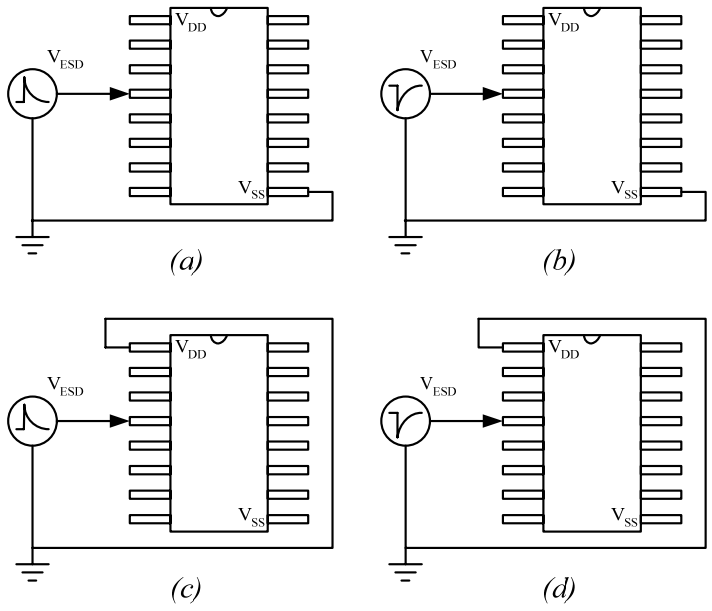


Figure 2-1: ESD zapping modes (a) PS-mode (b) NS-mode (c) PD-mode (d) ND-mode.[25]

The PS-mode (Figure 2.1(a)) (NS-mode (Figure 2.1(b))) refers to situation when a positive (negative) ESD stress voltage is applied to the pin and it discharges through the V_{SS}

(ground) pin Similarly the PD-mode (Figure 2.1(c)) (ND-mode(Figure 2.1(d))) refers to situation when a positive (negative) ESD stress voltage is applied to the pin and it discharges through V_{DD} (power) pin.

The ESD protection circuits in nano-metric technologies should be able to provide effective discharge path for all the four ESD zapping modes. The failure threshold is defined as minimum of the sustaining voltages of ESD stress for all the four zapping modes. For example a particular pin is passing 2kV ESD stress for PS-mode, NS-mode and PD-mode, but only passes 1kV ESD stress for ND-mode. Then the ESD failure threshold for this pin is only 1kV.

2.2 On-chip design methodologies

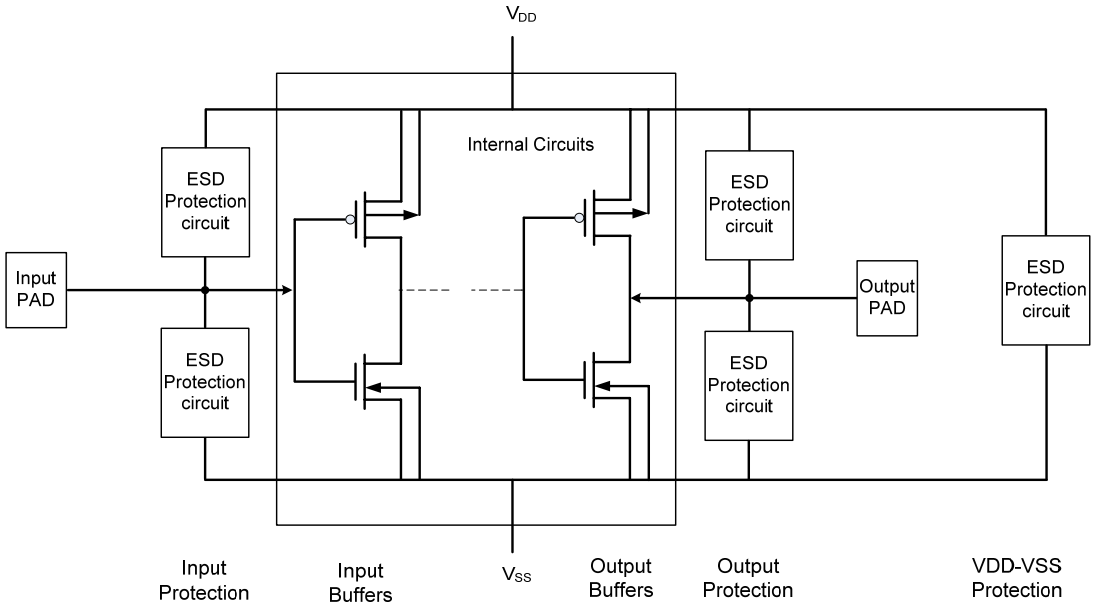


Figure 2-2 : Schematic of on-chip ESD Protection System

The function of ESD protection circuits is to limit the I/O pad voltage below the threshold voltage failure of the gate oxide by bypassing most of the ESD stress current. The Figure 2-2 shows the schematic of on-chip ESD protection methodology which provides protection against all the zapping modes. The ESD stress current can be bypassed from the internal circuitry either directly from the input (output) pad to power supply (V_{DD} or V_{SS}) or by passing the ESD stress current from the input (output) pad through the power rail ($V_{DD} - V_{SS}$ rail). So, based on how ESD stress current is shunted there are two general categories for ESD circuit protection.

2.2.1 Pad based ESD protection

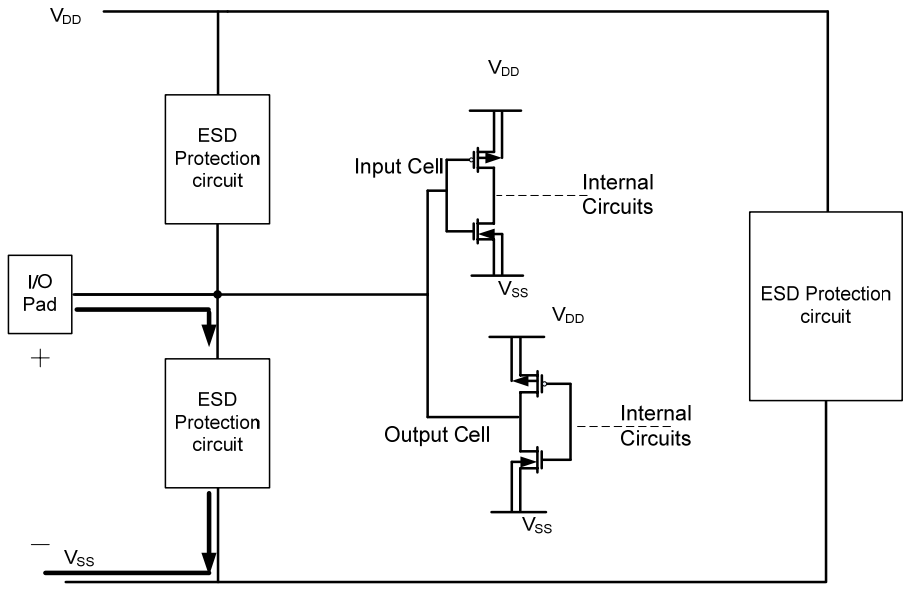
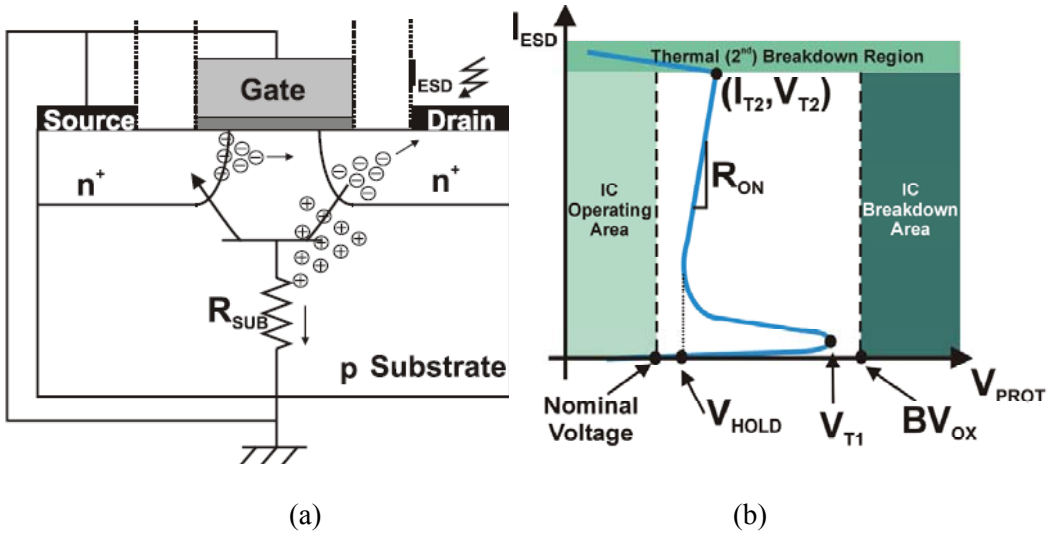


Figure 2-3: Pad based ESD protection

In the pad based protection, an ESD protection device exits between every pad- ground and pad-power pins. The Figure 2-3 shows a schematic of pad based ESD protection. A positive ESD discharge from I/O pad to the ground terminal is also shown in the figure. The ESD

stress current directly flows from the I/O pad to the ground through ESD protection circuit, hence it is called Pad based ESD protection. The ESD protection circuit must ensure that voltage across the internal circuitry is well below the failure threshold level of CMOS devices. In this protection scheme, we ensure that between any two pins there is a low impedance path designed to carry ESD discharge current for both polarities of ESD stress.



(a) (b)

Figure 2-4 : (a) Grounded gate NMOS (GGNMOS) (b) Typical Snapback device behavior [33]

The protection devices used in the pad based protection are generally snapback devices. In snapback devices, by increasing the voltage across the device, the device goes into avalanche breakdown and in this region it carries the ESD stress current. The first breakdown voltage (V_{T1}) is designed to be less than oxide breakdown voltage. Once the device get's triggered, due to the inherent feedback mechanism in the device, the voltage across the device drops to a holding voltage (V_{HOLD}). The holding voltage is designed to be greater than nominal voltage to avoid accidental trigger of the device under normal operating conditions.

Grounded Gate MOSFET [35] and silicon controlled rectifier (SCR) are most commonly used snapback devices in the CMOS technology.

2.2.2 Rail based ESD protection

In the rail based protection, ESD protection circuit is placed between the power supply rails (V_{DD} and $V_{SS)}$. Figure 2-5 shows the schematic of rail based ESD protection method. A positive discharge from the I/O pad to ground terminal is also shown. The ESD stress current directly flows from the forward biased diode D1 (parasitic diode of the input cell and output cell) through the power supply rail (V_{DD}) through the ESD protection circuit to the ground terminal (V_{SS}). Therefore the two devices in series (Diode D1 and ESD protection circuit) must meet the voltage-limiting criterion to protect the internal circuits. For a NS-mode stress the ESD stress current will pass directly through the parasitic diode D2. Therefore the size of the parasitic diode which depends on the sizing of the input and output buffer determine the current carrying capability. The size of input and output buffer is very large and hence we don't have to worry about the current carrying capability of the diodes.

The I/O protection in rail based ESD protection is very sensitive to the placement of the ESD protection circuit as bus resistance from the I/O pad to ESD protection circuit varies as how we place the clamps. Therefore the resistance between I/O pad and ESD protection circuit should be carefully estimated.

The protection circuits used in the rail based protection are non-snapback devices. In non-snapback devices, by increasing the voltage across the device, the current starts to increase. Unlike the snapback device, the non-snapback devices don't go into the breakdown region

under the high current regime. The most commonly used non-snapback devices are diodes and MOSFET's based circuits.

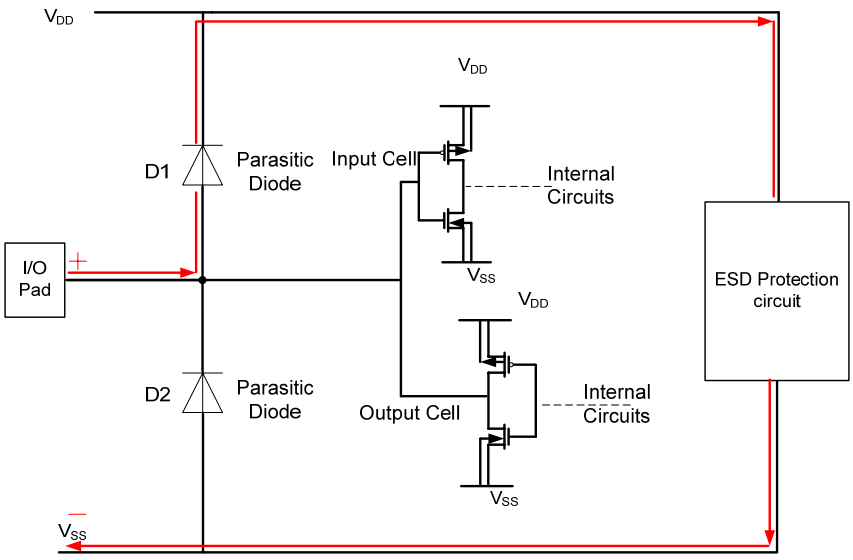


Figure 2-5:Rail based ESD Protection

2.2.3 Comparison between Pad and Rail based ESD protection

Designers often have to make a decision whether to opt for Pad based protection with snapback devices or Rail based protection scheme with non-snapback devices. The pad based ESD protection scheme has a very easy implementation, as ESD protection circuits are only placed in pads .For compact designs the ESD protection circuits can be contained in I/O pads only. By optimization, the snapback devices can be made very robust and immune to false-triggering. On the contrary, the pad-based ESD protection also has several disadvantages. Firstly, it cannot be ported from one technology to another technology and even from one fab to another fab as the parameters in snapback devices are very sensitive to the process variations. Secondly, with the advances in the process technologies and introduction of silicidation has dramatically affected the robustness of snapback devices. The silicidation

reduces the ballast resistance which results in non-uniform conduction between different fingers and within finger in MOSFET [36] and SCR based devices. Thus, the I_{T2} or maximum current carrying capability is reduced. Finally, there are few compact circuit models available to design the snapback protection devices. Hence, we have to rely on device level simulators like Medici, Sequoia to design these protection circuits. Thus it becomes very difficult to verify the functionality of the circuits along with the ESD protection devices.

The rail-based ESD protection is far less susceptible to the process variations and can be imported from one fab to another fab. Moreover the rail based ESD protection circuits use non-snapback based protection devices like diodes and MOSFET based circuits (clamps) and hence can be easily simulated in circuit simulators along with internal circuits to verify the functionality of the circuit. However, the non-snapback circuits are generally susceptible to false triggering especially for hot plug applications and fail-safe applications. Secondly, the non-snapback circuits are prone to oscillations during normal conditions and power up sequences. Thirdly, with the increase of the die size and interconnect resistance with scaling, the resistance of the supply path is becoming very important. With ultra-thin oxide transistors, even a small voltage build-up due to parasitic resistance can cause failure. Finally, with the scaling of technology and addition of more and more components on SOC chips has increased the number of power supply islands on chip . Hence the number of power clamps will increase because we will need extra ESD protection circuit between each power supply island. Therefore, the leakage current of the rail-based protection schemes becomes critical in multiple power supply chips.

Chapter 3
Snapback Devices

As discussed in the previous section, snapback devices are devices that go into avalanche breakdown during an ESD event. The most commonly used snapback devices in CMOS technology are variants of MOSFET's and SCR's. This chapter will cover different aspects of snapback based ESD protection circuits. The section 3.1 will explain most commonly used snapback devices- MOSFET and SCR. The section 3.2 will discuss the state of art based SCR devices already in use to address the challenges of technology scaling, particularly CDM stress and lower first triggering voltage (V_{t1}). The section 3.3 and section 3.4 will describe the new devices implemented in this research to address the issues of scaling.

3.1 Introduction

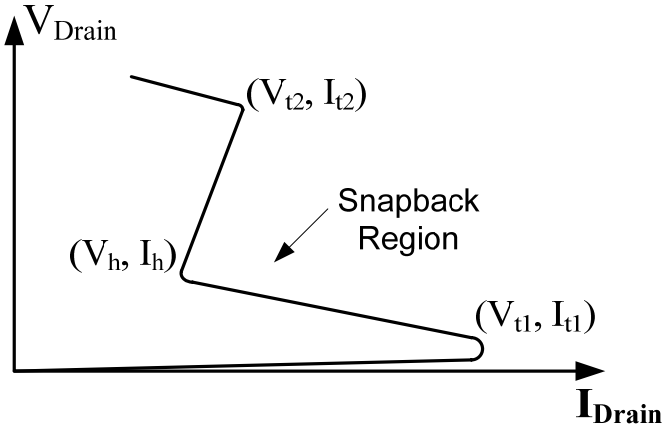


Figure 3-1: Typical IV Characteristics of Snapback Devices

The typical IV characteristic of any generic snapback device is shown in Figure 3-1. The device triggers only when the voltage goes beyond triggering voltage (V_{t1}). After the device triggers the voltage drops to a holding voltage (V_h), and in this region, the device carries the

ESD stress current. The thermal run-away occurs at second breakdown point (breakdown voltage V_{t2}, breakdown current I_{t2}). I_{t2} is measure of the robustness of a protection device, so it should be as high as possible. In the following section basic snapback based ESD protection circuits will be discussed.

3.1.1 Grounded Gate MOSFET (GGNMOS)

The Grounded Gate MOSFET (GGNMOS) is the simplest form of the snapback based ESD protection circuit. As the name implies, the gate of NMOS is shorted together with substrate and source to ground. Figure 3-2(b) shows the cross-section of the MOSFET along with the parasitic bipolar transistor [37]. As we increase the voltage across the drain, the drain-substrate junction becomes more and more reverse biased, until it reaches the avalanche breakdown. The hole-electron pairs are generated in avalanche breakdown. The hole current flows into the substrate and build a positive potential across the base-emitter junction (V_{be}) of the parasitic bipolar transistor. As the hole current is increased, the V_{be} increases until the parasitic npn-transistor turns on. The drain voltage (V_{DRAIN}) at this point is called triggering voltage (V_{t1}). At this point there is no need to keep the $V_{DRAIN} = V_{t1}$ to maintain the same drain current, so the voltage across the drain starts decreasing to holding voltage (V_h) and a snapback behavior is observed. Further increasing the drain voltage increases the drain current until the thermal device failure occurs. The voltage at this point is called second breakdown voltage (V_{t2}) and the corresponding current is called second breakdown current (I_{t2}).

The GGNMOS is not suitable for providing ESD protection in nano-metric technologies. The NMOS trigger voltage (V_{t1}) is very high and is not sufficient to provide protection for thin gate oxides (technologies node beyond 180nm). Also, GGNMOS is not suitable for digital I/O pads which are sensitive to a leakage current as with scaling of technology, the leakage current of the NMOS is increasing exponentially.

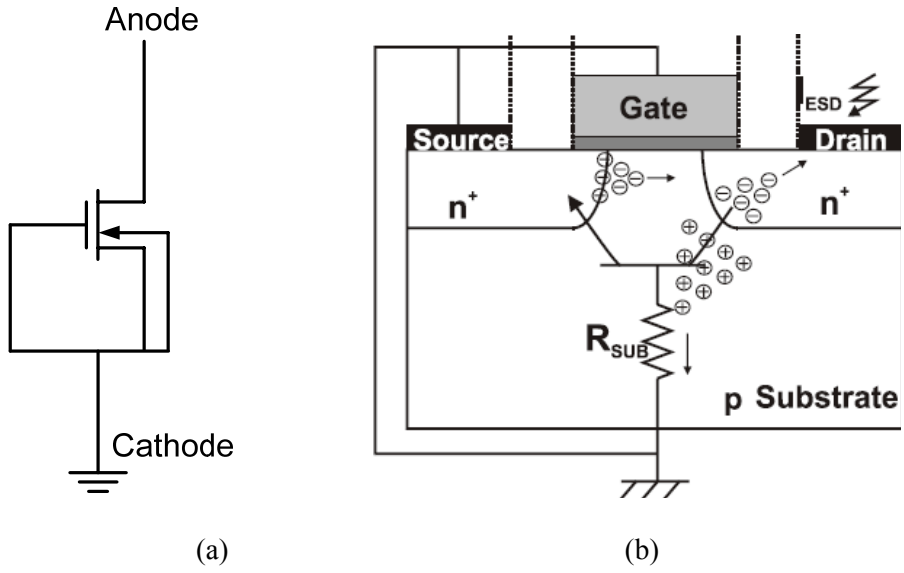


Figure 3-2: Grounded gate NMOS (GGNMOS) (a) Schematic (b) Cross-section

3.1.2 Silicon Controlled Rectifier (SCR)

Silicon controlled Rectifier (SCR) based devices are the most commonly used snapback based devices for ESD protection. Figure 3-3(a) shows the cross-section of a SCR device in the CMOS technology which consists of a sandwich of pnpn structure. The p^+, n^+ diffusion in the n-well are connected to anode and p^+, n^+ diffusion in the substrate are connected to the cathode. As an ESD protection circuit in an I/O pad, the anode is connected to the I/O pad

and cathode is grounded. Figure 3-3(b) shows the equivalent schematic of an SCR which consists of a parasitic lateral npn transistor and a vertical pnp transistor.

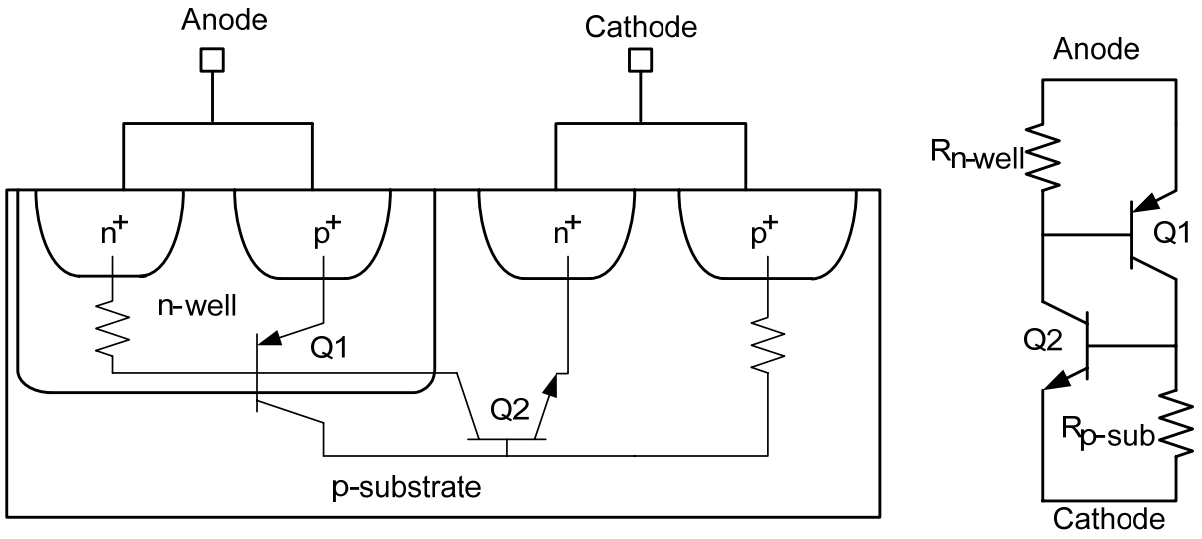


Figure 3-3: Silicon Controlled Rectifier (a) Cross Section (b) Equivalent Schematic

The SCR can provide ESD protection under both forward and reverse biased conditions. During the forward bias conditions, the anode voltage rises and reverse biases the n-well to p-substrate junction until it goes in avalanche breakdown region. The high injection of current can turn on either of two parasitic transistors (Q1, Q2). Typically Q2 turns on faster than Q1 due to higher gain of npn transistor as compared to pnp transistor. When the Q2 turns on, due to regenerative feedback Q1 will also turn on. When both transistors Q1 and Q2 are "ON", there is no need to keep the V_{ANODE}= V_{t1} to maintain the same current and hence the voltage across the anode will be reduced to V_H. Thus snapback characteristics are observed.

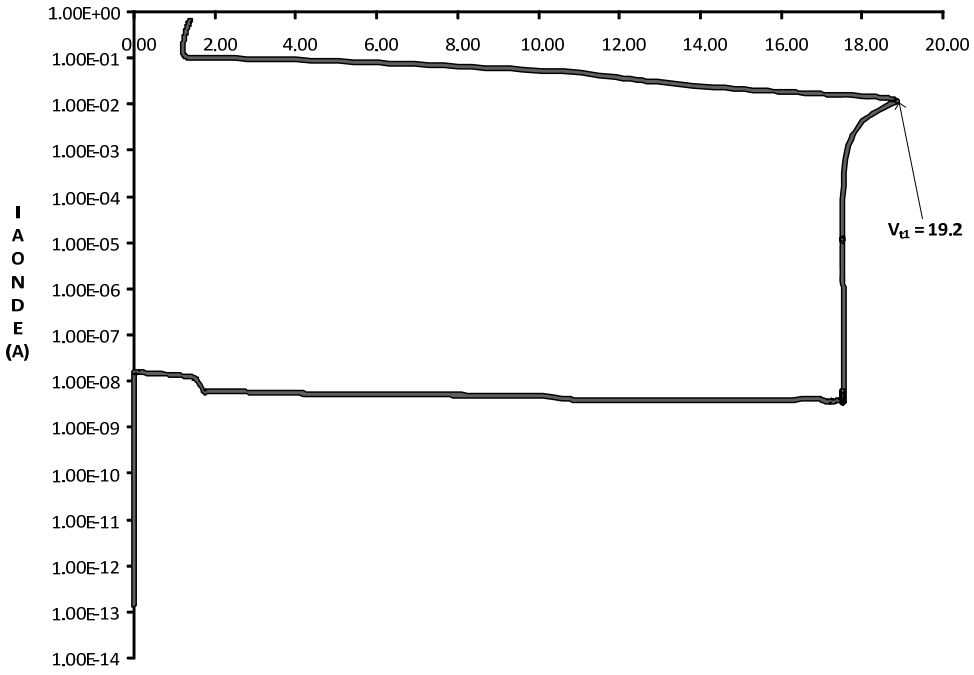
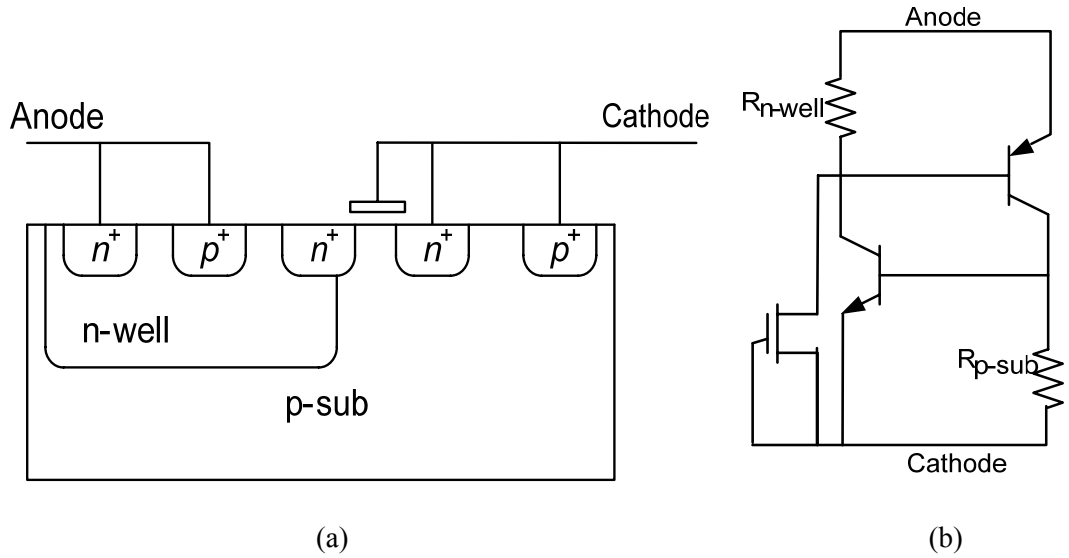


Figure 3-4: IV Characteristics of SCR in 180nm technology

Figure 3-4 shows the IV characteristics of the SCR device simulated in Medici in 180nm technology. The triggering voltage of the SCR device is 19.2 V and is not sufficient to protect the thin gate oxide of CMOS technology. The SCR device has a high triggering voltage (19.2V) and low holding voltage (1.2V) which makes it unsuitable for nano-metric technology, but it offers the highest ESD robustness per unit area. The current density in SCR is uniformly distributed, which permits better heat dissipation and hence highest ESD protection per unit area. The highest ESD protection per unit area makes SCR devices suitable for high speed applications where parasitic capacitance of ESD protection circuit should be minimized.

3.1.3 Low Voltage Triggered SCR (LVTSCR)

As discussed in the previous section, SCR has a high first breakdown voltage. The first breakdown voltage in an SCR device is due to high avalanche breakdown voltage of n-well and p-substrate. The V_{t1} can be lowered by insertion of a n+ region between the boundary of n-well and p-sub junction. It can be further lowered by inserting a gate electrode between the added n+ region and cathode n+ as shown in Figure 3-5(a). This structure is called low voltage triggered silicon controlled rectifier (LVTSCR) [38][39]. The breakdown voltage of LVTSCR is almost equal to the breakdown voltage of GGNMOS, which is still high to protect the thin-oxide gate devices in the nano-metric technology.



(a) (b)

Figure 3-5: LVTSCR (a) Cross section (b) Circuit Schematic

3.2 State of the art SCR based devices

The SCR device has a high trigger voltage and low holding voltage. The low holding voltage is becoming less of a constraint as the power supply voltage is also reducing with scaling of

technology but high trigger voltage is a major concern. As discussed in the chapter 1, the gate oxide breakdown voltage is decreasing and ESD related CDM failures are rising with scaling of technology. Thus, it is imperative to reduce the triggering voltage, and decrease the turn-on speed of SCR devices to provide protection against CDM ESD failures. The following section discusses the state of the art SCR based devices available to reduce the triggering voltage and turn-on time of SCR device.

3.2.1 Native-NMOS- Triggered SCR device (NANSCR)

The Native-NMOS SCR (NANSCR) [40] reduces the triggering voltage and increases the turn-on speed of device by introduction of low threshold voltage NMOS in parallel with the SCR device. The native NMOS is directly built in the lightly doped p-type substrate in a twin tub process, so the threshold voltage is almost zero. The drain of the native NMOS is directly connected to the anode of the SCR. The gate of native NMOS is connected to negative bias circuit (NBC) to reverse bias the transistor under normal operating conditions to reduce the leakage current. A p^+ diffusion is inserted in p-well between n-well edge and n^+ diffusion and is connected to the source of the native NMOS. Figure 3-6(a) shows the cross section and Figure 3-6(b) shows the equivalent circuit schematic of the hybrid NANSCR structure.

During an ESD event, the NBC node is floating, so the native NMOS is “ON” and pumps current from the pad of the anode to base of the parasitic NPN transistor of SCR device. The trigger current raises the voltage across the base of NPN transistor, when the base voltage is greater than 0.7 V the NPN transistor becomes active. The positive feedback regeneration turns on the PNP transistor and hence turns on the SCR device to discharge the ESD current.

Thus native- NMOS helps in turning “ON” the SCR by lowering the trigger voltage and turn-on time of the SCR.

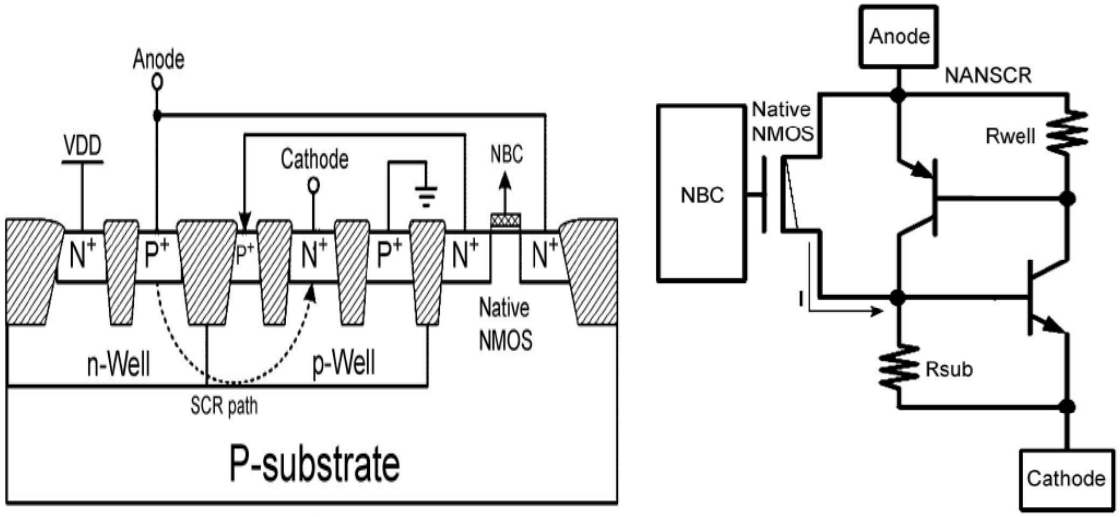
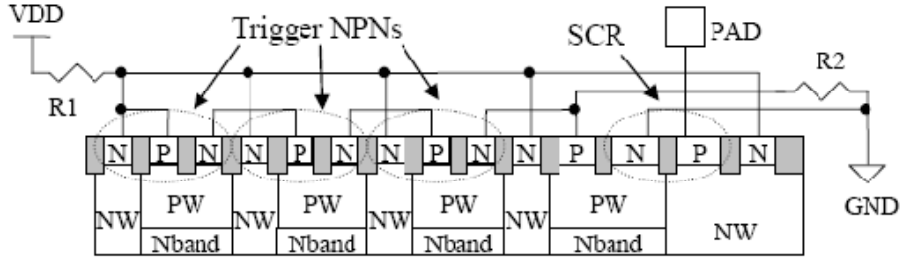


Figure 3-6: NANSCR (a) Cross Section (b) Circuit Schematic

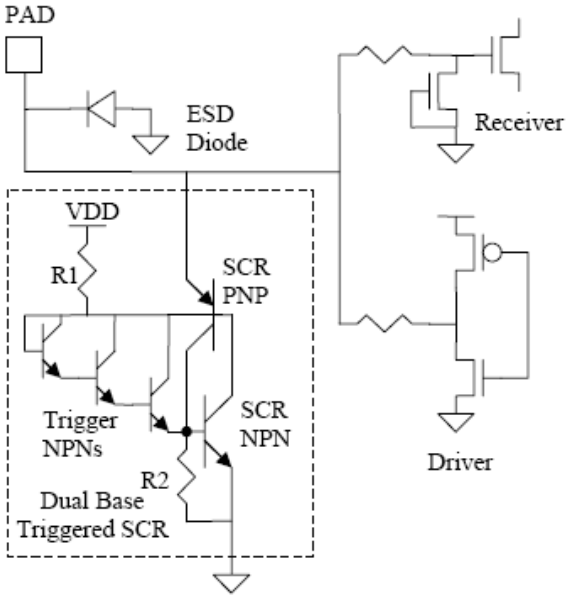
3.2.2 IBM’s Bipolar-Triggered SCR device (DbtSCR)

The Darlington bipolar triggered SCR (DbtSCR) [41] reduces the triggering voltage and increases the turn-on speed of SCR by introduction of string of small NPN bipolar transistors between the bases of the parasitic NPN transistors and PNP transistors forming the SCR. The NPN transistors are connected in the Darlington configuration (emitter of transistor connected to base of other transistor) to increase the gain of the transistor, and hence reduce the turn-on time of SCR device. Figure 3-6 (a) shows the cross-section of DbtSCR with three NPN transistors connected in the Darlington configuration and Figure 3-6(b) shows the equivalent schematic. The resistors R1 and R2 are connected in circuit to modify the turn-on characteristics of the SCR based device. The resistor R2 shunts the SCR NPN and keeps the transistor off for small values of the current. The resistor R1 biases the N-well at a positive

potential, so under normal operating conditions the N-well capacitance to the substrate doesn't load the pad.



(a)



(b)

Figure 3-7: Dual base DbtSCR (a) Cross Section (b) Schematic

3.2.3 Gate Triggered or Substrate triggered LVTSCR (GT-LVTSCR, ST-LVTSCR)

The Gate coupling and substrate triggering mechanism reduces the first breakdown voltage by applying trigger voltages to gate [42] and substrate [43] of LVTSCR. In gate coupling a positive voltage is applied to the gate. The voltage applied to the gate increases the current in

the channel, which helps to forward bias the parasitic npn transistor and hence lowers first breakdown voltage. Similarly in substrate triggering, a positive voltage is applied to the substrate. This voltage forward biases the source-substrate junction of the NMOS reducing the threshold voltage (V_{TH}) of NMOS transistor in LVTSCR and hence first breakdown voltage. Also, this external voltage increases the base voltage of the parasitic NPN transistor and hence smaller voltage will be required to turn-on the LVTSCR.

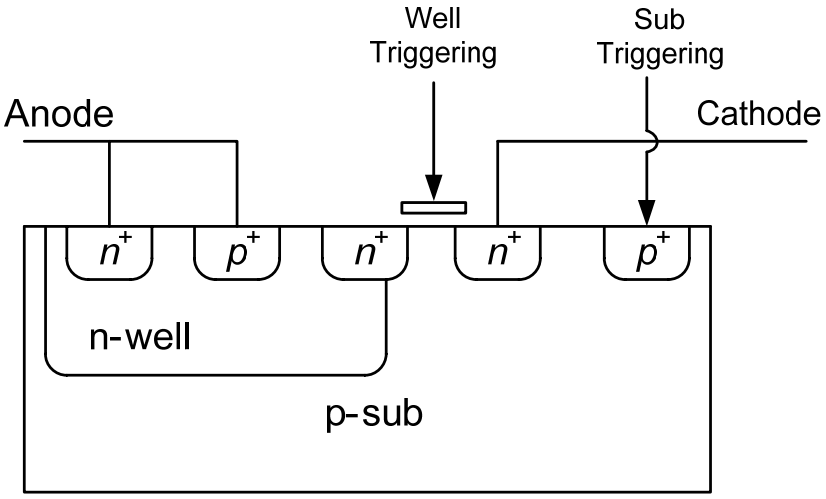


Figure 3-8: Cross Section of Gate triggered and substrate triggered SCR

3.3 Proposed Snapback devices

The state of the art devices discussed in the previous section to counteract the effects of scaling technology use the triple well technologies (NANSCR,DbtSCR) to fabricate these special devices. The triple well process technology requires extra fabrication steps and are more expensive than the standard fabrication. Also, the extra triggering mechanisms (NANSCR,GG-LVTSCR, ST-LVTSCR) designed to reduce the first breakdown voltage increase the parasitic capacitance of the device. Thus these devices are unsuitable for high

speed applications. A novel low capacitance Darlington based SCR (DSCR) device with a tunable triggering voltage is proposed in section 3.3.1. Also, in order to mitigate the effects of CDM stress, a NMOS based Darlington based SCR device (NMOS-DSCR) is proposed in section 3.3.2.

3.3.1 Darlington based SCR device (DSCR)

The Darlington based SCR (DSCR) reduces the first breakdown voltage of an SCR device without addition of any extra triggering devices such as substrate triggering in ST-LVTSCR[43], gate-triggering in GT-LVTSCR[42], NMOS in NANSCR etc. Hence, the parasitic capacitance of DSCR is very low (comparable to original SCR device) and can be used in high speed applications. The structure of original SCR is modified to reduce the first breakdown voltage (V_{t1}). An extra n-well is inserted between the boundary of n^+ and p^+ diffusions of the cathode. A p^+ diffusion is added to the n- well and it is connected externally to the n^+ diffusion inserted at the boundary of the n-well and p-substrate as shown in Figure 3-9 (a). The equivalent circuit of resultant DSCR is shown in Figure 3-9(b). The insertion of extra p^+ diffusion in n-well adds an extra parasitic PNP transistor (Q3) to NPN transistor (Q2). The transistors Q2 and Q3 are connected in the Darlington configuration, which increases the current gain and helps in turning-on DSCR faster and hence lowering first breakdown voltage. The gain of the additional transistor is a function of distance between n^+ diffusion of cathode and the n-well ("D" as shown in Figure 3-9(a)).

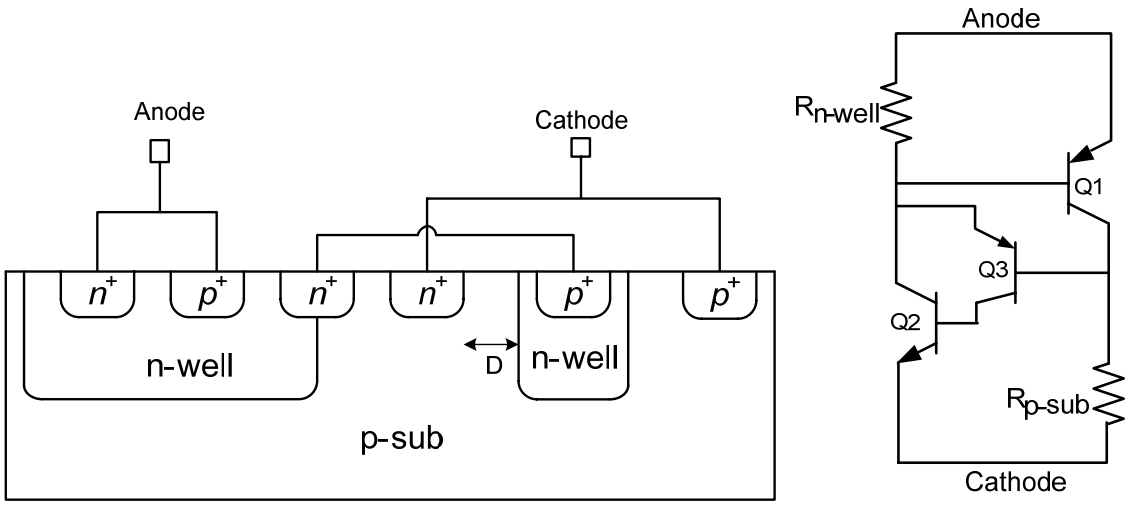


Figure 3-9: Darlington based SCR(DSCR) (a) Cross Section (b) Circuit Schematic

The DSCR was simulated in MEDICI (device simulator) using the process parameters of the CMOS 180nm technology. The quasi-dc simulations were done for 100 µm width and various values of "D" and IV characteristics were plotted. Fig3-10 shows the IV characteristics of DSCR (width = 100 µm) simulated for D=0.7 µm, D =1 µm and compares it with SCR device (width = 100 µm). It is evident from the simulations that the first breakdown voltage has been reduced from 22 V (SCR device) to 3.2 V (D=0.7 µm). The first breakdown voltage can be further reduced to 1.5 V by setting D=0.5 µm.

Iin order to verify the simulation results, the DSCR was fabricated in the 180nm technology. A 100µm wide DSCR was fabricated in 180nm technology with D=0.7 µm. Figure 3-11 shows the TLP measurements results for this device. It can be observed that the first breakdown voltage of the DSCR is 3V, which is in accordance with our simulation results (Figure 3-10). The leakage current of DSCR ($I_{LEAKAGE}$ ~ 50 pA) is also very low. Also, the second breakdown current (the complete waveform is not shown in Figure 3-11 for

clarity purposes) was over 4A. The HBM measurements were also carried out on the device and as expected it passed ± 6 kV ($V_{ESD} = I_{t2} * 1.5$ kV).

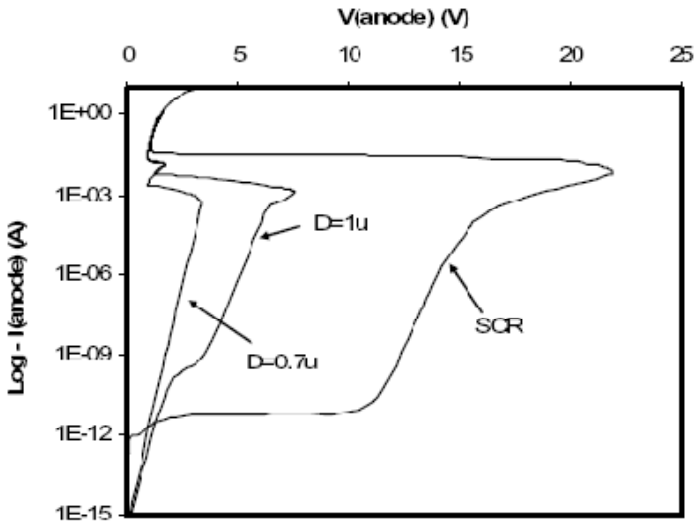


Figure 3-10: IV Characteristics of DSCR and SCR device in CMOS 180nm technology

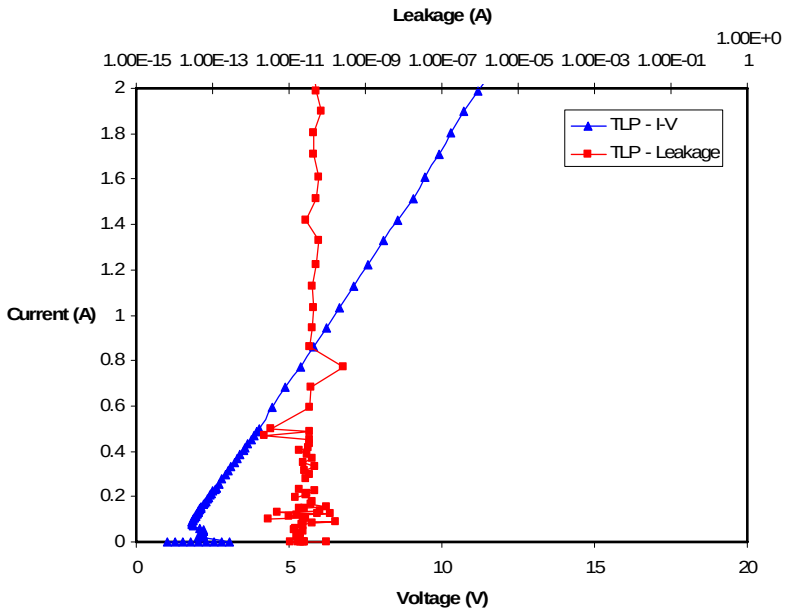


Figure 3-11: TLP measurement results for DSCR in CMOS 180nm technology

3.3.1.1 Parasitic Capacitance of DSCR

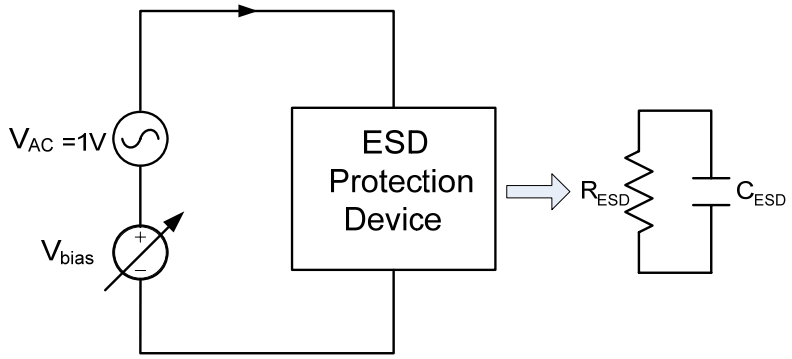


Figure 3-12: Circuit to simulate the parasitic capacitance of ESD protection device

As discussed in the previous section, the DSCR structure has a low parasitic capacitance as compared to other devices because it doesn't have any extra triggering devices to lower its first breakdown voltage. In order to verify this claim, the parasitic capacitance of ESD protection devices must be simulated. The ESD protection device can be modeled by equivalent resistance (R_{ESD}) and capacitance (C_{ESD}) [44]. Figure 3-12 shows the circuit to simulate the parasitic capacitance in Medici (device simulator). An AC simulation is done for various bias voltages varying from 0 to 1.8V. The value of R_{ESD} is calculated at a very low frequency as V_{DD}/I_{IN} and then the value of C_{ESD} is extracted from the input impedance calculated at a high frequency (shown in the formula).

$$@\ f = 1\,Hz : R_{ESD} \cong Z_{in} = \frac{V_{AC}}{I_{in}}$$

$$@\ f = f_0 : Z_{in} = \frac{R_{ESD}}{1 + 2\pi f_0 R_{ESD} C_{ESD}} = \frac{V_{AC}}{I_{in}}$$

$$\Rightarrow C_{ESD} = \sqrt{\frac{\left(R_{ESD} / Z_{in}\right)^2 - 1}{R_{ESD}^2 \omega_0^2}}$$

Figure 3-13 shows the parasitic capacitance voltage(C-V) characteristics of DSCR at 1 GHz and compares it with GST-LVTSCR and LVTSCR. All the devices are 100 µm wide and GST-LVTSCR, DSCR are designed to have the same first breakdown voltage of 5V. It is evident from the graph that for the same or similar breakdown voltage the parasitic capacitance of DSCR is reduced from 125fF to 85fF.

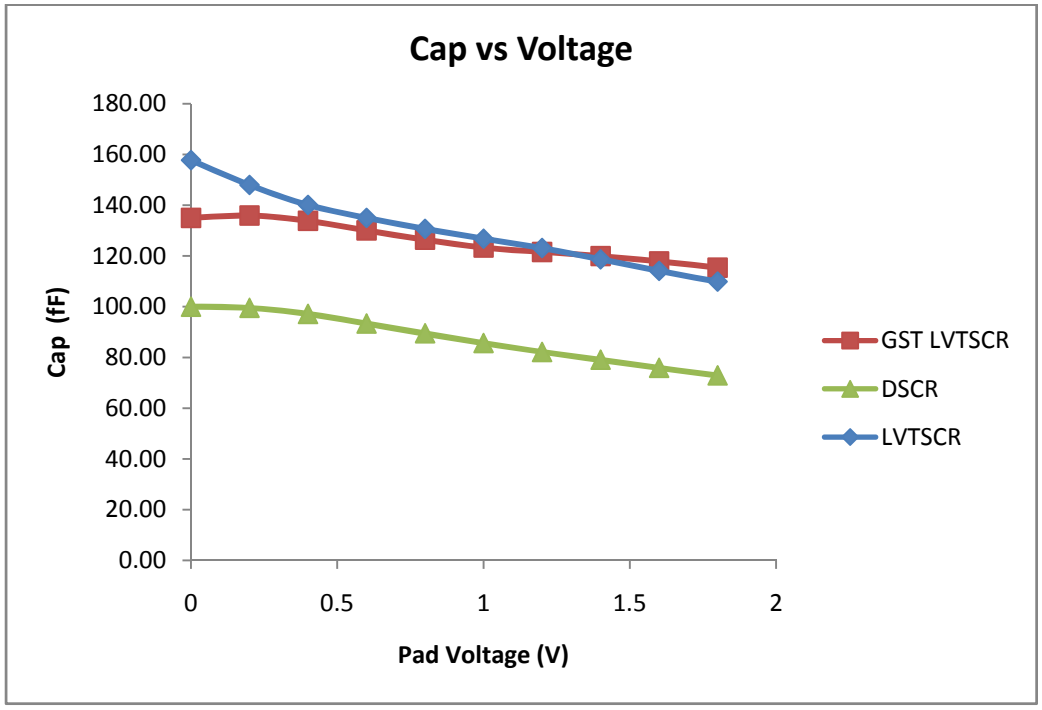
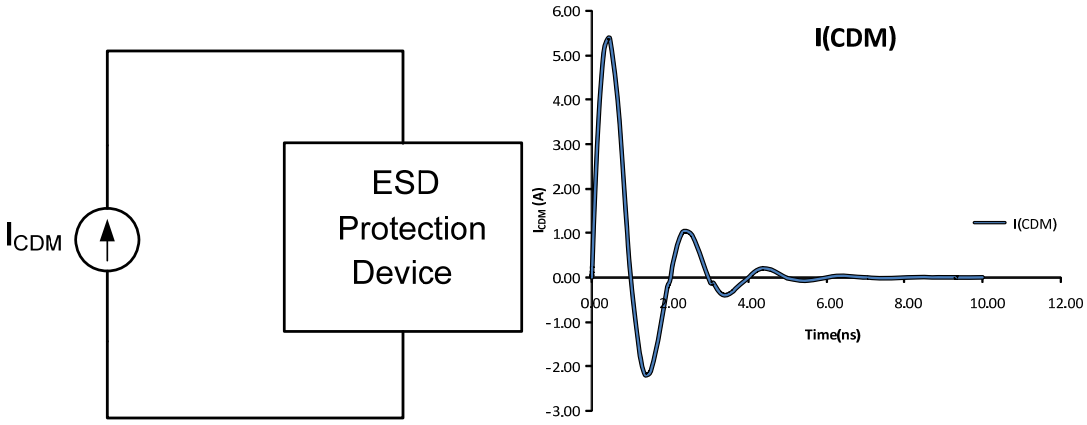


Figure 3-13: Simulating capacitance for various pad voltage

3.3.1.2 CDM Performance of DSCR

The Darlington NPN transistor in DSCR helps in turning-on the SCR device very quickly, and makes it suitable for handling CDM Stress. To test the effectiveness of the DSCR, the devices must be simulated under CDM Stress conditions. Figure 3-14(a) shows the circuit to simulate the CDM stress. A constant current source, which models the CDM stress current

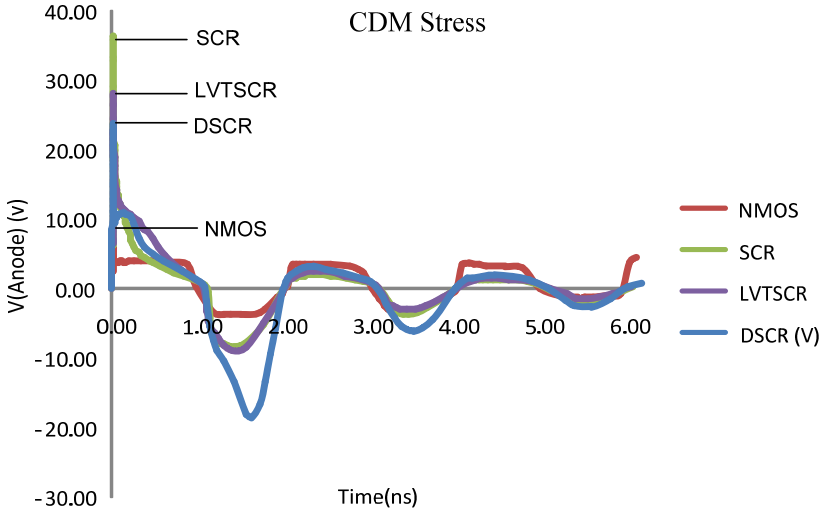
(shown in Figure 3-14 (b) [46], is pumped into the ESD protection device and the corresponding peak voltage is observed. Smaller the peak voltage, the faster will be turn-on time of device and higher CDM robustness.



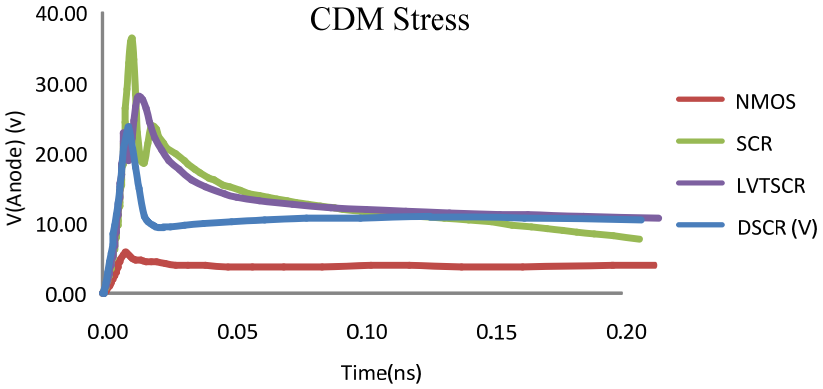
(a) (b)

Figure 3-14: (a) Circuit to simulate CDM Stress (b) CDM current waveform

Figure 3-15 shows the voltage across the pad, when a 500V CDM stress is applied to DSCR and compares it with SCR, LVTSCR and GGNMOS. All the devices are 100µm wide and the same CDM Stress current is applied. It can be observed that the peak voltage for GGNMOS is 5.73V, DSCR is 23.6V, LVTSCR is 28.1V and SCR is 36.3 V. Thus the CDM performance of the GGNMOS is the best, but it is unsuitable for nano-metric technology as it has a very high first breakdown voltage. Also, it can be observed that the CDM performance of the DSCR is better than the LVTSCR and SCR device.



(a)



(b)

Figure 3-15 : CDM Stress Voltage (a) Time range 6ns (b) Time Range 200ps

3.3.2 NMOS-Darlington based SCR device (NMOS-DSCR)

The DSCR structure has a low triggering voltage and capacitance which makes it suitable for nano-metric technology, but the CDM stress performance of the GGNMOS structure is better than DSCR. The NMOS-Darlington based SCR device (NMOS-DSCR) integrates the DSCR structures and GGNMOS transistor into one hybrid structure. The hybrid structure has a low triggering voltage and superior CDM Stress performance. Figure 3-16 shows the cross-

section of the NMOS-DSCR structure. The DSCR structure is modified and the n^+ diffusion connected to the anode is moved to the edge of n-well and p-substrate. An extra n^+ diffusion and thin gate oxide is inserted in p-substrate and connected to the p-substrate as shown in Figure 3-16.

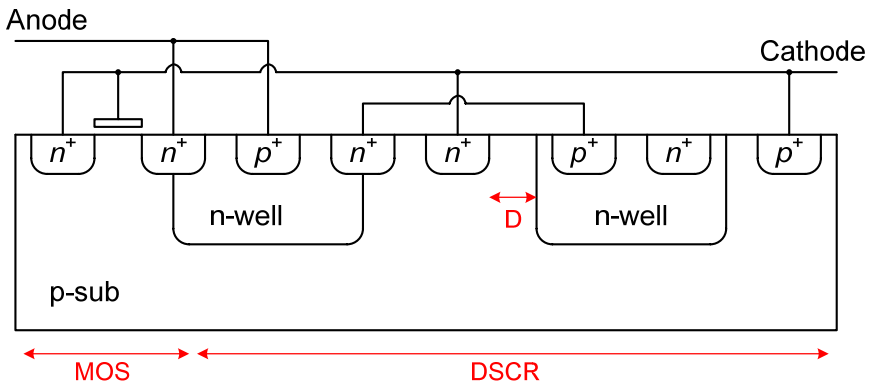


Figure 3-16: Cross Section of NMOS – DSCR

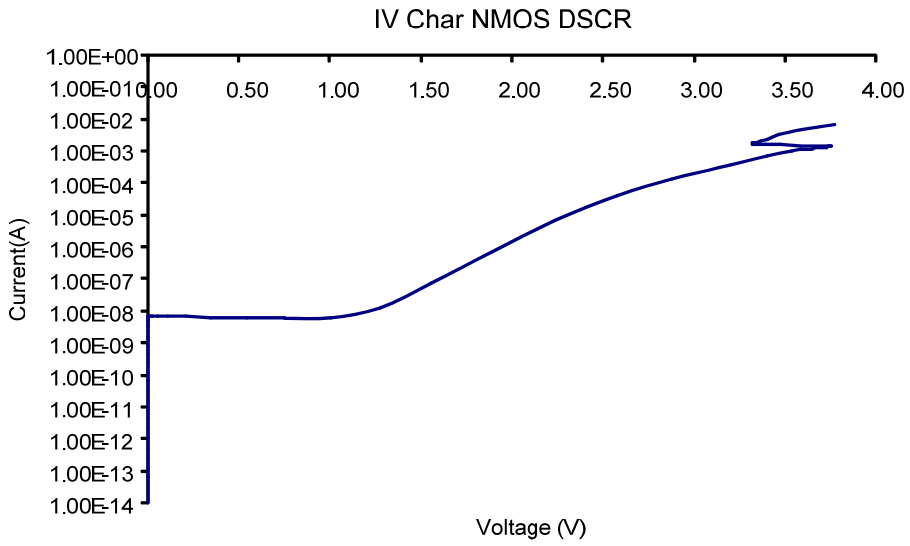


Figure 3-17: IV Characteristics of NMOS-DSCR

The NMOS-DSCR structure was simulated in MEDICI (device simulator) using the process parameters of the CMOS 180nm technology. The quasi-dc simulations were done for

100 µm width and IV characteristics were plotted. Figure 3-17 shows the IV characteristics of NMOS-DSCR simulated for D=0.7 µm. The first breakdown voltage is 3.6 V and the holding voltage is 3.3 V, similar to the IV characteristics of the DSCR.

3.3.2.1 CDM Performance of NMOS-DSCR

As discussed in previous section, the GGNMOS offers superior ESD CDM stress performance as compared to other devices. So, the hybrid NMOS-DSCR structure should also have superior ESD CDM Stress performance. A 500 V CDM stress was applied on the NMOS-DSCR and DSCR devices which are 100µm wide. The simulations are done in the device level simulator MEDICI. Figure 3-18 shows the voltage across the pad, and it can be observed peak voltage has been decreased from 23.6 V in DSCR to 14.8 V in NMOS-DSCR voltage. Thus the CDM stress performance of the hybrid structure is better than DSCR, LVTSCR, SCR etc.

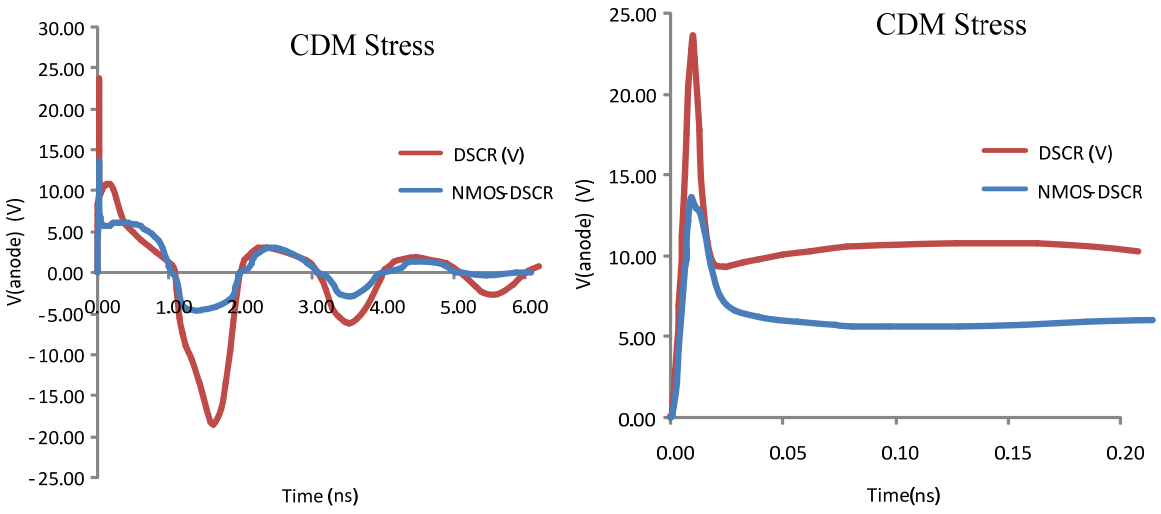


Figure 3-18 : CDM Stress Voltage (a) Time range 6ns (b) Time Range 200ps

3.3.2.2 Parasitic Capacitance of NMOS-DSCR

The superior CDM stress performance of the hybrid ESD protection circuit comes at the added cost of parasitic capacitance. Figure 3-19 shows the capacitance voltage (CV) characteristics of NMOS-DSCR at 1 GHz and compares it GST-LVTSCR and DSCR. All the devices are 100 µm wide and are designed to have the same first breakdown voltage of ~5V. It is evident from the graph that for the same or similar breakdown voltage the parasitic capacitance of NMOS-DSCR is similar to the parasitic capacitance of GST-LVTSCR and greater than parasitic capacitance of DSCR.

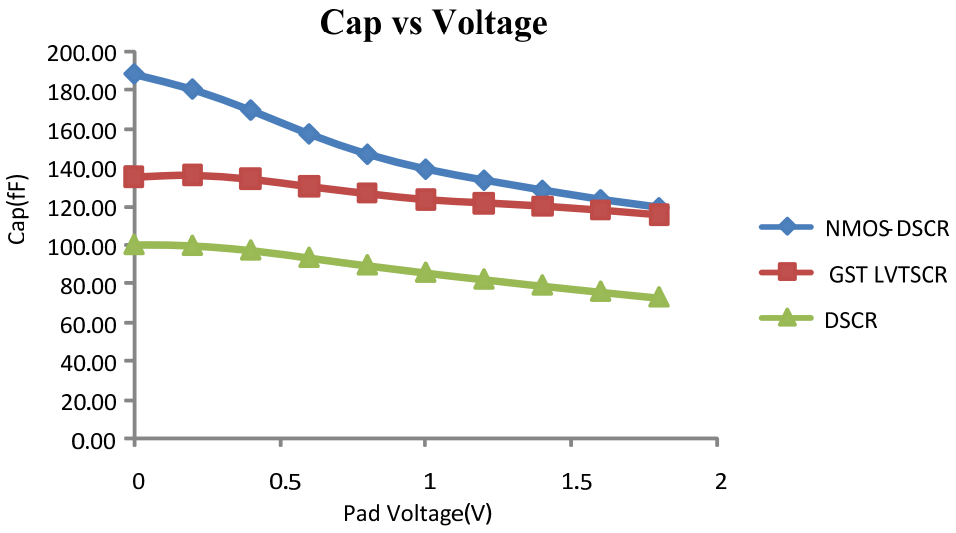


Figure 3-189: Simulating capacitance for various pad voltage

3.4 Summary

This chapter presented a background on different snapback devices. The traditional snapback devices likes MOSFET, SCR and LVTSCR were discussed. The traditional snapback devices have either low holding voltage or high triggering voltage. Also the turn-on time of these devices is very high, making them unsuitable for the handling CDM stress. Some of the state

of the art snapback devices like DbtSCR, NANSCR, GT- LVTSCR and ST-LVTSCR have been discussed to counteract the above mentioned problems. In this research we have purposed two novel snapback devices – DSCR, NMOS-DSCR. The table 3-1 gives the summary of performance of different snapback devices. The CDM robustness of DT-SCR, NAN-SCR has not been reported as these devices can only be fabricated in twin-tub process technology. The twin-tub process technology is not supported by the university technology library provider (CMC). So, it's impossible to model/simulate these devices. The values reported in table3-1 for NAN-SCR, DT-SCR are the measurement results.

Table 3-1: Summary of performance of different snapback devices

	Technology	HBM (kV)	V_{t1}(V)	Cap (fF)	CDM Stress
SCR	0.18µm	-	19.2	-	36.3
NMOS	0.18µm	-	7.4	-	5.73
DT-SCR [69]	0.25µm	> 6	7	160	-
NAN-SCR [40]	0.13µm	3	4	130	-
GST-LVTSCR [43]	0.18µm	6	5	115.6	28.1V
DSCR	0.18µm	>6	3	72.9	23.1V
NMOS- DSCR	0.18µm	>6	3.45	119.5	14.8V

It is clear from the table that the GGNMOS offers the superior CDM robustness but is having very high first breakdown voltage making them unsuitable for the nano-metric technology. The NMOS-DSCR offers excellent CDM robustness, without compromising the first breakdown voltage. The only disadvantage of NMOS-DSCR structure is higher capacitance than DSCR. The DSCR offers lowest capacitance, lowest first triggering voltage solution making them suitable for high speed applications.

Chapter 4
Non-Snapback Devices

As discussed in chapter 2, non-snapback devices are the devices that don't go into the avalanche breakdown region under the high current regime. The most commonly used non-snapback devices are diodes and MOSFET's based clamps. This chapter will cover different aspects of the MOSFET based clamps and will introduce newer enhanced clamps to counteract the effects of scaling down the technology. The section 4.1 will give an overview of different types of clamps (static, transient clamps). In section 4.2, state of the art clamps will be presented. The section 4.3 will discuss a method to reduce the leakage current of MOSFET based clamps. The section 4.4 will present a robust novel transient clamp. Finally, the section 4.5 will address the noise coupling issue in the mixed-signal design, and will discuss methods to reduce the noise coupling from digital supply to analog supply through clamps .

4.1 Introduction

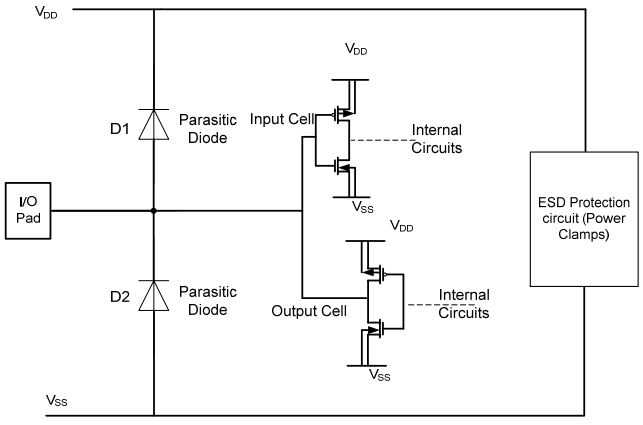


Figure 4-1: Power Clamps in Rail based ESD protection circuit

Non-snapback devices have non-avalanching junctions, that don't go into the avalanche breakdown during the ESD stress. They can be designed and simulated using circuit simulators like Cadence and are portable from one fab to another fab and also into different technology nodes. As already discussed in chapter 2, non-snapback devices are used in Rail based ESD protection methodology. The non-snapback devices are mostly used between the power supplies, hence they are also called Power clamps. Figure 4-1 shows a block diagram of a Power Clamp in Rail based ESD protection methodology.

Power clamps can be grouped into two categories: static clamps and transient ordynamic clamps. Static clamps provide a steady-state current and voltage response. They limit the supply voltage by carrying a large current through a low impedance load when the voltage exceeds a threshold value. Diodes, GGNMOS and SCR based devices fall into this category. On the contrary, transient clamps sense the rapid changes in the voltage or current to recognize an ESD event and trigger accordingly to discharge the ESD current. These clamps trigger for a short duration of time, only for time till the ESD stress current gets discharged completely. RC network with a big MOS transistor to discharge the ESD stress current fall into this category.

Static and transient clamps have their own advantages and disadvantages. Static clamps (Diodes, GGNMOS etc) are smaller in size and occupy less area on the chip, but they have long turn-on time and don't react quickly under the CDM stress conditions. On the contrary, transient clamps trigger faster and carry large transient currents under an ESD event. Also they can be simulated in circuit simulators like Cadence, PSPICE etc. Their disadvantage is

that they are susceptible to trigger under fast-rise time events like Noise, power-up of chip etc. In the following sections static clamps and transient clamps will be discussed in detail.

4.1.1 Static Clamps

Static clamps trigger when the voltage across the circuit becomes greater than a threshold voltage called trigger voltage. The trigger voltage should be designed to be less than the oxide breakdown voltage. The diode string, GGNMOS and SCR based devices are the commonly used static power clamps. The criteria of selection of the what type of static clamp to use depends on numerous factors like current handling capability of device, leakage current, turn-on time of the devices etc.

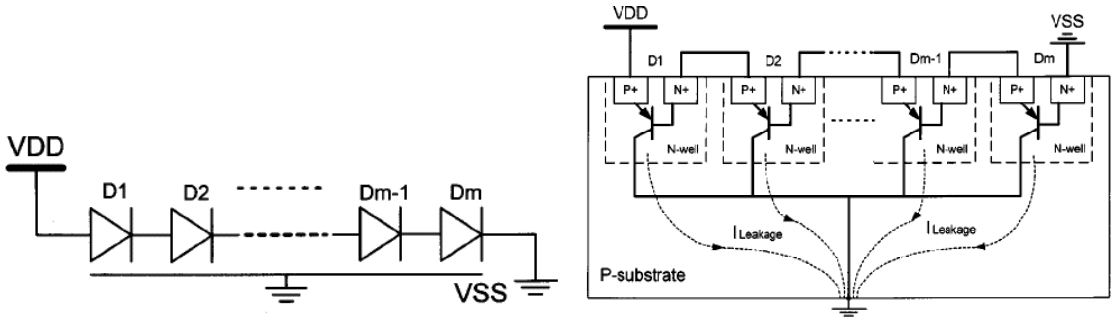


Figure 4-2: Diode Strings (a) Schematic (b) Cross section [46]

Diodes in their forward-biased conditions can carry much larger currents, but their turn-on voltage is very small. Therefore, a stack of diodes can be used to increase the triggering voltage. Figure 4-2 shows the schematic and cross section of the diode strings used as the static clamp between power supply and ground or between different power supplies. The stacking increases the leakage current [47] due to the current amplification of the parasitic NPN bipolar transistor. The Darlington configuration of bipolar NPN transistors also leads to

the reduction in the turn-on voltage or trigger voltage at higher temperatures [48][49]. In order to overcome these limitations several structures like zener diodes [67], cantilever diodes [49] etc. have been proposed.

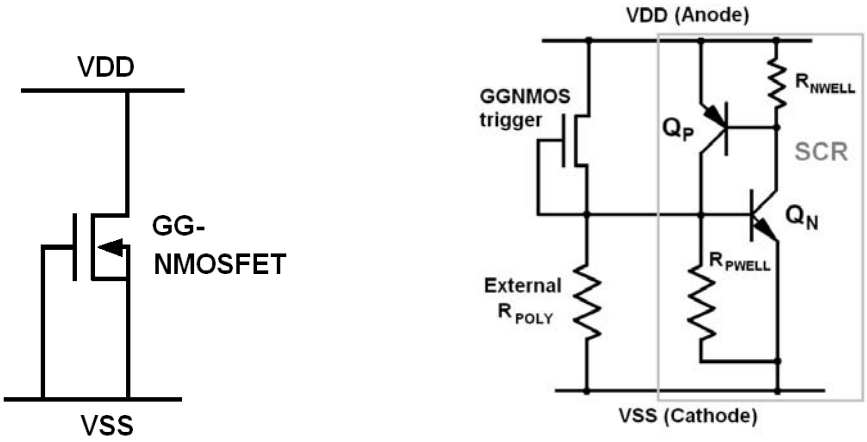


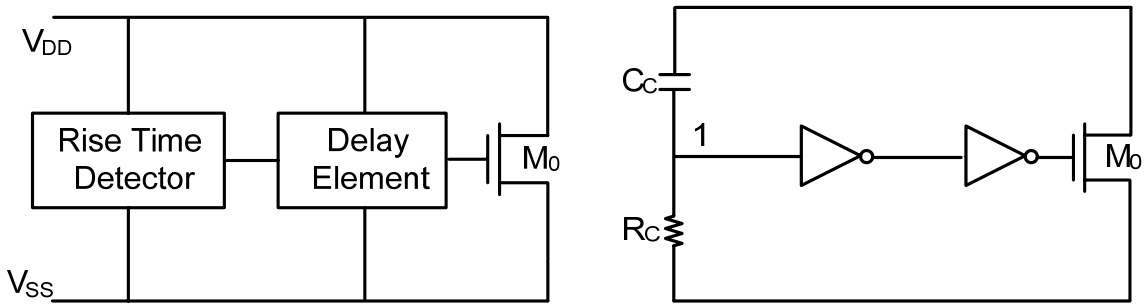
Figure 4-3: Schematic (a) Grounded Gate NMOS (b) High holding voltage LVTSCR[53]

GGNMOS and SCR based devices are also used as static clamps. The main limitations of these devices is relatively high triggering voltage which is not sufficient to protect the thin gate oxides in nano-metric technologies and also low holding voltage which can lead to latch up issues under normal operating conditions. Figure 4-3 shows the schematic of GGNMOS and High holding voltage LVTSCR[8] which can be used as static clamps.

4.1.2 Transient Clamps

Transient clamps sense the rapid changes in the voltage or current to recognize an ESD event and trigger accordingly to discharge the ESD current. During the ESD event, transient clamps turn-on quickly and turn-off slowly until all the ESD stress current has been discharged. Figure 4-4 (a) shows the schematic of a generic MOS based transient clamp. It consists of a rise time detector to detect an ESD event, a delay element to control the time for

which clamp stays on and a big transistor M_0 to discharge the ESD current. The advantage of using transient clamps is their ability to provide protection at low voltages(suitable for thin-oxide technology devices), no extra fabrication processing steps required, possibility of circuit level simulation with Cadence, Spice etc. and low turn-on time (CDM stress robustness). On the contrary, transient clamps are vulnerable to false triggering due to the circuit noise or during power-up event.



(a) (b)

Figure 4-4 : (a) Generic Schematic of transient clamp (b) Inverter based transient clamp [54]

Figure 4-4(b) shows a schematic of simplest transient clamp, an inverter based transient clamp [54]. The RC-circuit senses the ESD event, and drives the big transistor M_0 through a cascade of inverters. The RC timer is responsible for making a decision between an ESD event and normal power-up event. The clamp will trigger falsely if RC timer circuit is unable to make a distinction between them. The inverters are added to drive the big NMOS transistor (M_0) and to improve the noise immunity. Under the normal operating conditions, the output of the first inverter is "1", and it is difficult to flip the value of this inverter. Hence, it provides improved noise immunity.

The RC-circuit can be designed to distinguish between the ESD event and the normal power-up event. An ESD event lasts for hundreds of nano-seconds, while a normal power-up event is in the order of milliseconds. Thus, it is possible to distinguish between a normal power-up event and an ESD event. The RC time constant should be designed to be greater than the time required to completely discharge the ESD event and less than the rise-time of the power-up event. Typically the RC time constant chosen is between 600ns – 1μs, therefore the value of resistors range from 80-90K and capacitor from 18-20pF. Hence it requires huge capacitor and resistor to implement the inverter based transient clamp. Also, careful consideration should be given to design the inverter based clamp as it have been found that the circuit may oscillate during an HBM ESD event and power-up conditions [55].

4.2 State of the art transient clamps

The traditional inverter based clamp needs a large RC network (large die area required) to keep it in conductive state for whole duration of the ESD stress. The large RC time constant can lead to false triggering in hot power plug applications and increased susceptibly to power bus noise. Another concern in transient clamps is the possibility of the oscillation during the power-up and ESD conditions [55]. In this section, state of the art transient clamps will be discussed to address these issues.

The feedback enhanced triggering clamp [57] uses a feedback circuitry to enhance the ESD circuit operation and reduce the RC time constant of the rise time detector. The feedback enhanced triggered transient clamp is shown in the Figure 4-5. When the ESD stress is applied on the V_{DD} rail, the voltage at node “1” rises. Thus the voltage at node “2”

goes to V_{SS} voltage, while the voltage at node "3" rises to V_{DD} and turns the main transistor M_0. The positive feedback mechanism discharges the node 2 to V_{SS} voltage and helps in further charging node "3" to V_{DD} voltage. Once the transistor M_0 is turned on, it is latched on

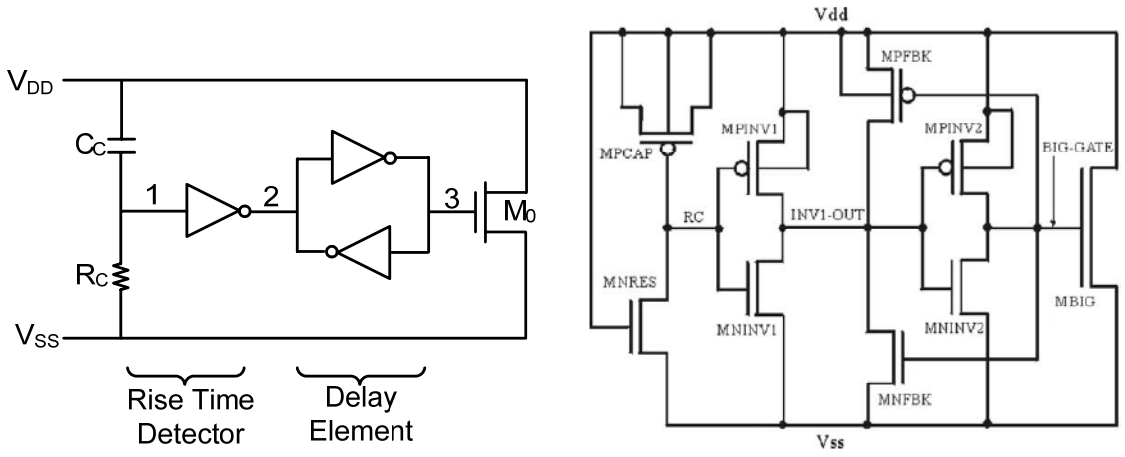


Figure 4-5: Feedback enhanced triggering clamp (a) Block Diagram[56] (b) Schematic [57]

to its conductive state by the latch mechanism and keeps the main transistor M_0 "on" for 700ns [57]. Further, it was reported that clamps is immune to the false triggering and doesn't trigger for a very fast power-up sequence of 1µs. The only limitation of this clamp is the possibility of oscillations during power-up and/or under ESD operation [56].

The thyristor based clamp [56] uses CMOS thyristor as a delay element to reduce the RC time constant and enhance the ESD circuit operation. It was reported in the paper that the CMOS thyristor can generate delay from a few nano-seconds to milliseconds range with low static leakage current. Figure 4-6 shows the schematic of a CMOS thyristor based clamp. The resistance "R_1" is used to pull down the node 3 under the normal operating conditions when the transistor M_4 is "off". A high value of "R_1" increases the time for which ESD clamp stays "on" , but it is unable to turn-off the transistor M_0 under normal operating conditions.

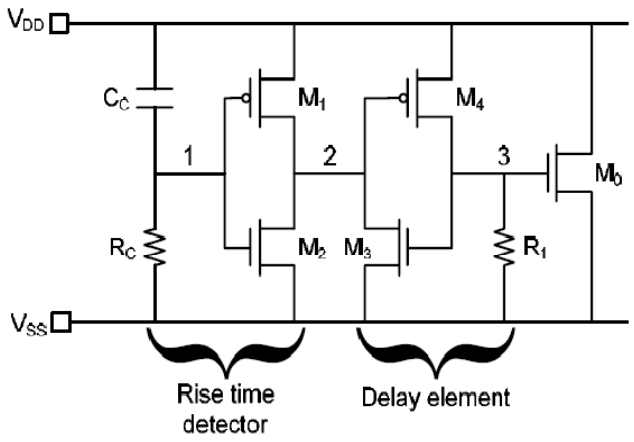


Figure 4-6 :Thyristor based Clamp [56]

On the contrary a low value of "R_1" turns-off the transistor M_0 under normal operating condition but reduces the time for which ESD clamp turns "on" during ESD event. Therefore, the value of R_1 should be optimized for the ESD performance and turning-off of transistor M_0 under normal operating conditions. Further, it was reported that this clamp is immune to the false triggering and doesn't trigger for a very fast power-up sequence of 1µs. Also, it was reported by the authors that the clamp is robust against oscillation under power-up and/or ESD operation.

Another type of clamp to reduce the RC time constant, avoid false triggering during power-up and reduce the possibility of oscillation is the Flip-Flop based clamp [58]. The Flip-Flop based Clamp uses a rising edge triggered D-type flip-flop to latch the transistor M_0 into conductive stage for theoretically infinite time. Figure 4-7(a) shows the block diagram of the Flip-Flop based Clamp. When an ESD event occurs, a rising edge is detected at the clock input of the Flip-Flop. The value of "D=0" is sampled and latched by the Flip-Flop. The

output value “Q” turns on the main transistor M_0 into conductive stage through an inverter for whole ESD event.

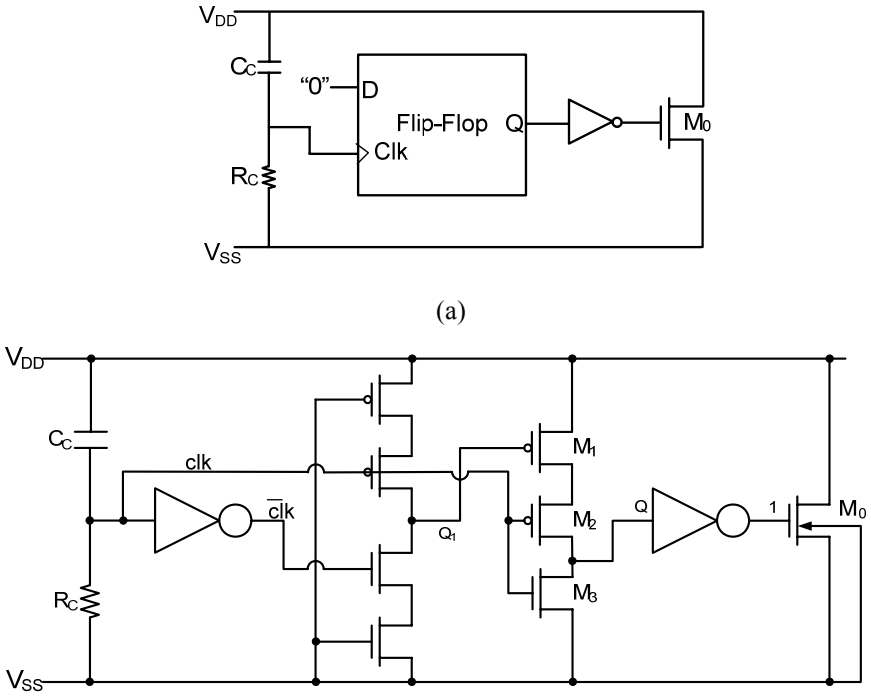


Figure 4-7:Flip-Flop based Clamp (a) Block Diagram (b) Schematic [58]

The Flip-Flop based Clamp (FF Clamp) can be designed to turn-off the clamp under normal operating conditions. Figure 4-7(b) shows the schematic of the Flip Flop based Clamp. Further, it was reported in the paper [58] that the clamp was immune to false triggering for fast power-up sequence of 200ns. It is also immune to oscillations and provides excellent power supply noise immunity.

4.3 Low Leakage Clamp

The scaling down of CMOS process technology has increased degree of integration, enabling growth of mixed-signal circuits. The integration of analog blocks such as ADC, PLL's, DLL's, oscillator etc. on digital chips has provided cheap system on chip (SOC) solutions. However, at the same time the number of power islands is increasing due to separate power supplies for different blocks to increase power supply isolations. Thus the number of power clamps or transient clamps is also increasing in an SOC. The increase in power clamps and reduction of threshold voltage (V_{TH}) with scaling of technology has increased the leakage current of ESD protection network. In this research, a new method has been proposed to reduce the leakage current of the transient clamp with minimum impact on the ESD robustness.

Figure 4-8(a) shows a generic block diagram of conventional transient clamp. Most of the leakage current of the transient clamp is through the main transistor M_0. The leakage current of M_0 can be reduced by adding source impedance i.e. reverse biasing the main transistor M_0. The source impedance should satisfy following the criteria:

1. Under normal operating conditions it should reverse bias the main transistor M_0 to reduce leakage current.

2. Under ESD stress, the ESD performance should almost remain unaffected by addition of source impedance.

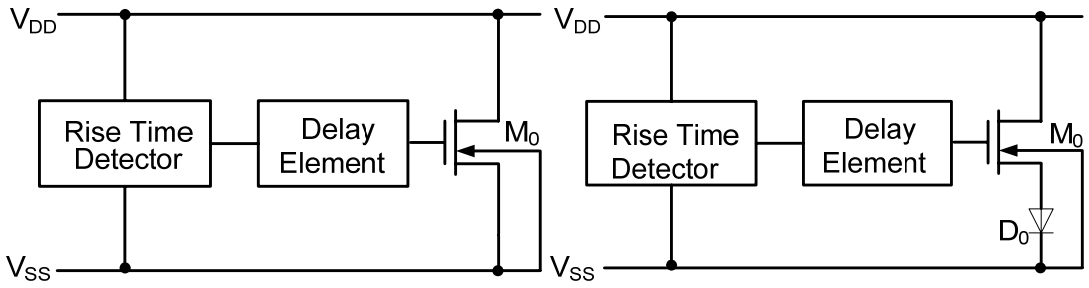
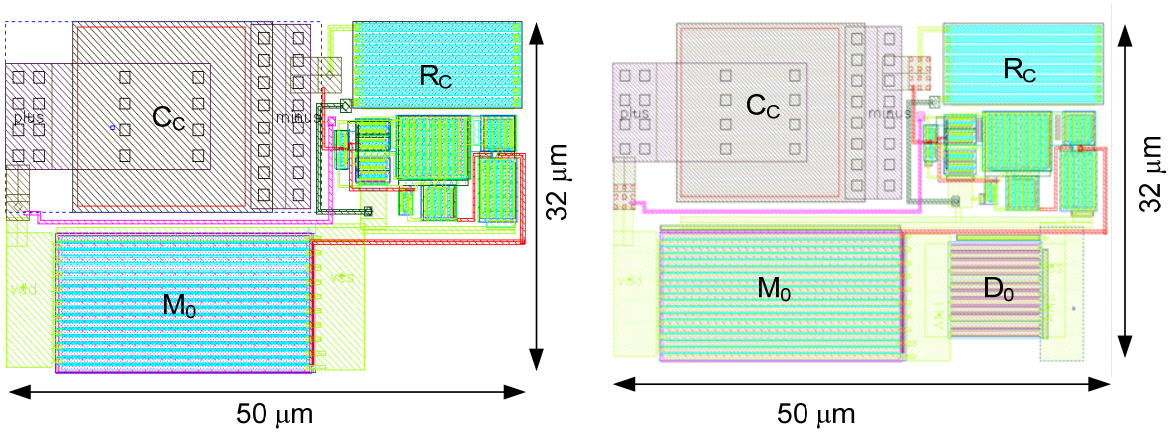


Figure 4-8 (a) Transient Clamp (b) Modified transient clamp to reduce leakage

After careful consideration, diode was found to be the best option for reducing the leakage current. Figure 4-8(b) shows the modified circuit for reducing the leakage current. Under the normal operating conditions, negative V_{GS} reduces the leakage current. Also the ESD performance is slightly affected, as built-in voltage of diode is small.

To test the effectiveness of the proposed methodology, a test chip was taped-out in 90nm technology provided by ST Microelectronics. The Flip-Flop based clamp [58] which has already been discussed in the previous section is used as a benchmark. The flip flop based clamp is designed in 90nm technology to handle 2kV HBM Stress. Also, a low V_{TH} NMOS transistor (M_{0LowVt} W= 400 μm) is chosen for a faster response time against CDM Stress. In order to compare and contrast the clamp with and without diode, both were fabricated in the 90nm technology. The diode width (D_{0LowVt} = 8.88X0.48 um^2) was chosen wide enough, to avoid thermal failure of the diode during the ESD Stress. Figure 4-9 shows the layout of the Flip-Flop based Clamp with and without diode.



(a) (b)

Figure 4-9 : Flip-Flop based Clamp (a) Without Diode (b) With Diode

4.3.1 Post Layout Simulations

Under normal operating conditions, i.e. I.C. is powered on, there is under drive voltage of -415mV (V_{GS}=-415mV i.e. V_G = 0 V & V_S = 415mV) in transistor M_0. This under-drive voltage reduces the leakage current of the main transistor and hence the leakage current of the Clamp. In our post layout simulations we found that leakage current of the main transistor M_0 reduced from 54.58 µA to 226.6pA, a reduction of more than 200,000X.

The ESD robustness of the structures of FF based Clamp with and without diodes was also evaluated. A 2 kV HBM Stress was applied to both clamps and the peak voltage was observed on the VDD rail. Figure 4-10 shows the post-layout simulation results for the ESD response for a flip flop based clamp with and without diode. As we can see from the Figure 4-9 the peak voltage has only increased from 3.5 V in FF Clamp w/o diode to 5.1V in FF Clamp with diode. So, there is a degradation of 45% in the peak voltage for the ESD robustness, whereas the leakage current is reduced by more than 200,000X. It should be

noted that the peak voltage increase is acceptable since it is well below the gate oxide breakdown voltage in 90nm and is at this level for very short time.

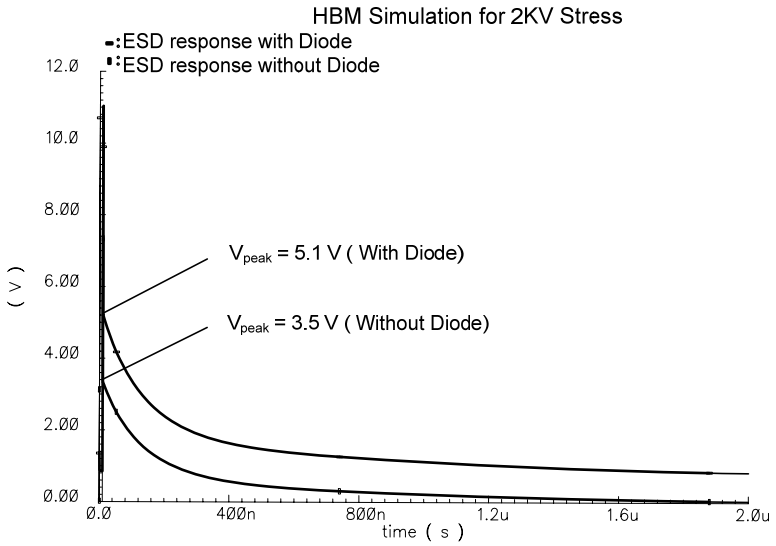


Figure 4-10:ESD Response for FF Clamp with & w/o Diode

4.4 Oscillation robust Clamp: TSPC based Clamp

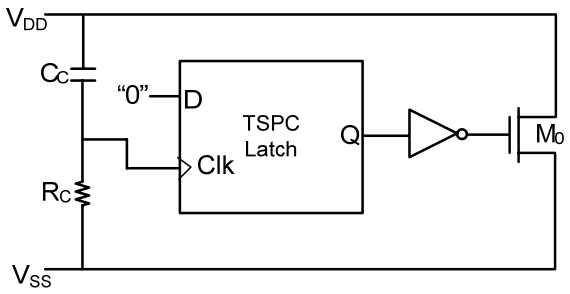


Figure 4-11: Block Diagram of TSPC Clamp

The TSPC based transient clamp is based on Flip-Flop based transient clamp. The only difference is that it uses True Single-Phase clocked latch (TSPC latch) [59] instead of C^2MOS Flip-Flop [68] as in Flip-Flop based Clamp to increase the time for which the transient clamp remains "on". The TSPC based Clamp uses a rising edge triggered D-type

latch [59] to latch the transistor M_0 into conductive stage for theoretically infinite time. Figure 4-11 shows the block diagram of the TSPC based Clamp.

When an ESD event occurs, a rising edge is detected at the clock input (clk) of the latch. The value of "D=0" becomes transparent to the latch and the output value of latch becomes "Q=0". The output value "Q" turns on the main transistor M_0 into conductive stage through a inverter for whole ESD event. Under the normal operating conditions, the D-input of the latch is always "0", therefore the output of latch is "0" and hence the clamp will turn-on. In order to ensure that the clamp remains "off" under normal operating conditions, the transistor M_1 and M_2 are sized larger as compared to M_3 or low V_{TH} transistors are used for M_1 and M_2. This design consideration ensures that the leakage current of M_1 and M_2 combined is more than the leakage current of M_3 transistor to set "Q=1" under normal operating conditions. The diode "D_0" has also been added in series with the main transistor "M_0" to reduce the leakage current under normal operating conditions.

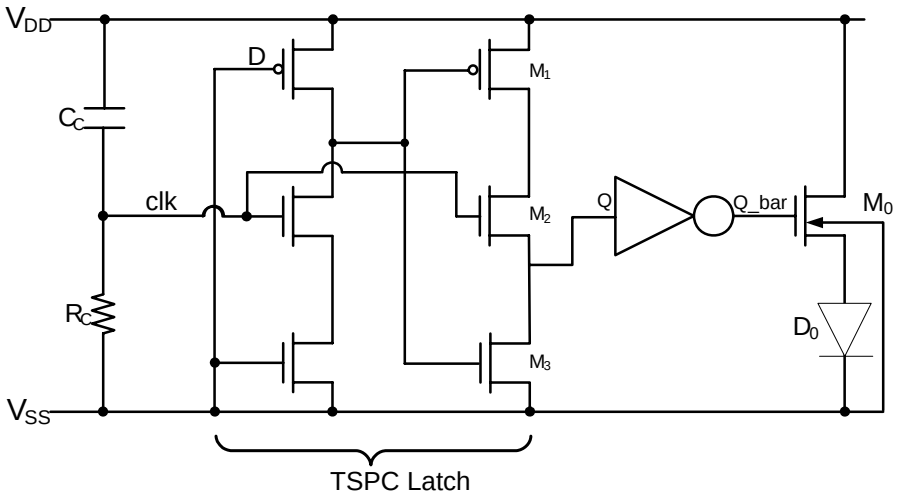


Figure 4-12: TSPC based Clamp

In order to evaluate the clamp, it was taped out in the 90nm test chip. Figure 4-13 shows the layout of the TSPC based clamp. The post-layout simulations were done under both normal operating conditions and ESD stress conditions to ensure the proper operation even after laying out the transistors. The section 4.4.1 and 4.4.2 will give you the post layout simulation results for the clamp working under ESD and during normal operating conditions. The last section 4.4.3 will evaluate the clamps immunity to oscillations and will compare it with some of the existing clamps.

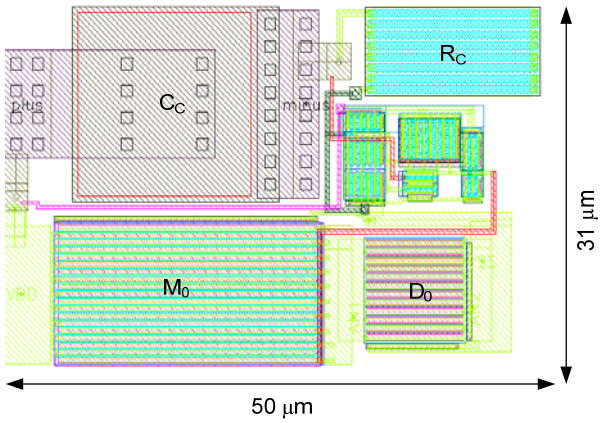


Figure 4-13:Layout of TSPC based Clamp in 90nm technology

4.4.1 ESD operation

The TSPC clamp is designed in the ST 90nm technology kit. The main transistor (M_0) is a minimum length low V_{TH} transistor (width = 400µm) and all the other transistors are high V_{TH} thick oxide transistors. A positive 2 kV HBM stress is applied and the peak voltage is observed on the VDD rail. Figure 4-14 shows the post layout simulation results for the TSPC based Clamp with diode to reduce the leakage current.

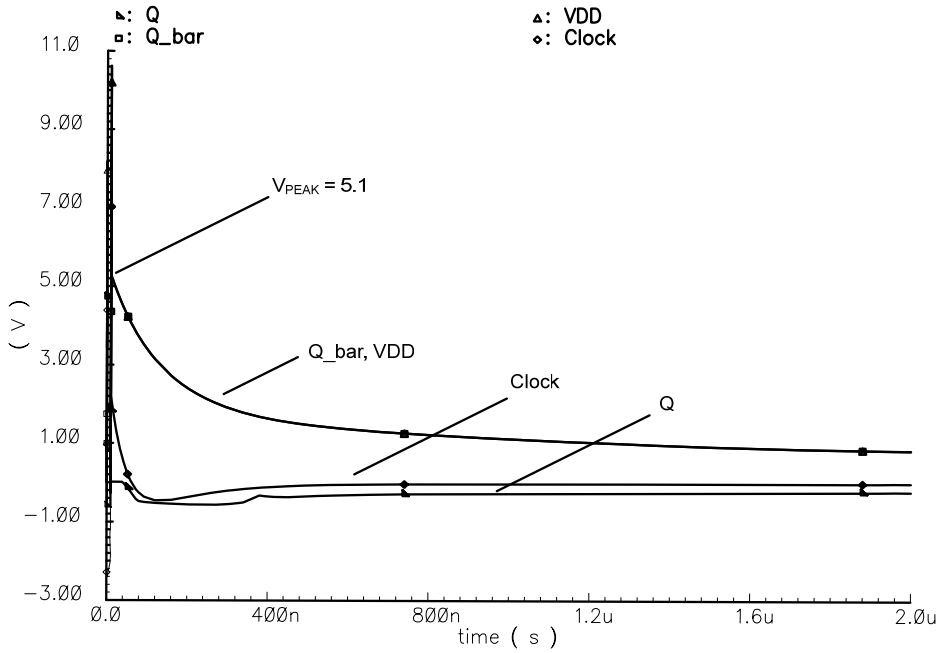


Figure 4-14: Post Layout Simulation results for 2kV HBM Stress

It is evident from Figure 4-14 that peak voltage on supply line during 2 kV HBM stress is 5.1 V. This voltage is low enough to provide ESD protection in 90nm technology for thin oxide transistors. Also, it is clear that the TSPC clamp is similar to FF- based Clamp and remains "on" for whole duration of ESD stress.

4.4.2 Normal operation

During the chip power-up, the power supply ramps at a predefined rate which typically has a rise time of several milliseconds. This ramp rate is several orders of magnitude slower than the ESD event. So, the "clk" node (Figure 4-12) remains at a potential near zero as RC time constant of 40ns is several orders smaller than the ramp time of power-up. However, for "hot-plug" operations, there is a very fast transition on the V_{DD} rail that can be as fast as 1µs. This fast transition can turn-on the clamp and it can interfere with the normal circuit

operation. The TSPC based clamp is also tested for false-triggering for fast transitions by ramping up the supply voltage in 1µs. Figure 4-15 shows the voltage across the different

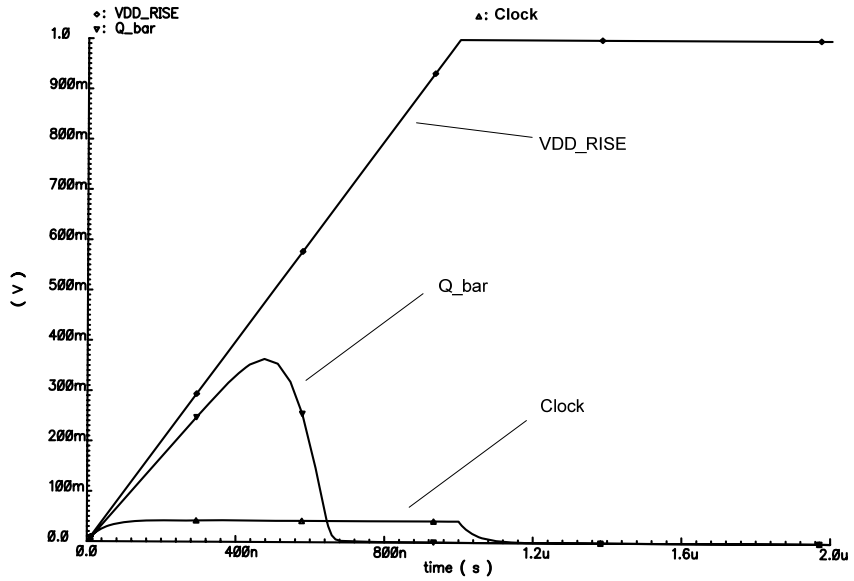
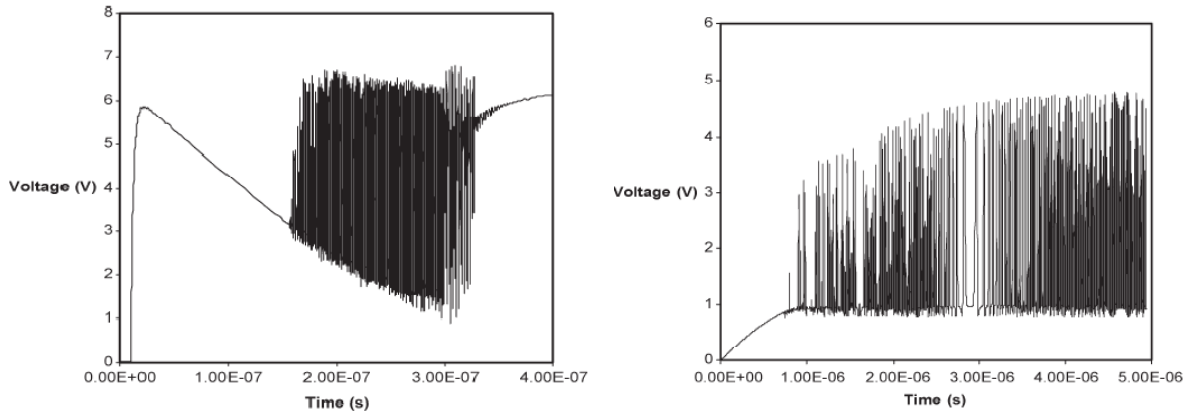


Figure 4-15: Post layout simulations for TSPC Clamp for 1µs power-up

nodes when a 1 µs ramp voltage is applied to V_{DD} node. It can be observed that the voltage at the gate of the main transistor "M_0" rises to 0.3V and then again goes back to "0". Hence the TSPC clamp is immune to false triggering for hot plug power applications. Also, in addition to false triggering, the TSPC clamp is monitored for leakage current under normal operating conditions. The leakage current of the clamp is 215.6 pA which is well within the specifications of the clamp.

4.4.3 Immunity to Oscillations

One of the other concerns of the transient clamps is oscillation during the ESD stress and/or power-up conditions [60][57][58]. Figure 4-16 shows the oscillations on the power supply rail (V_{DD}) during an HBM stress and during the power-up sequence which is having a rise



(a) (b)

Figure 4-16: Voltage at node V_{DD} of inverter based Clamp (a) HBM Stress (b) Power-up of 3µs [58]

time of 3µs.The time at which oscillations start is dependent on RC time constant, chain delay for a HBM stress, rise-time of power-up and load of the power line for power-up sequence[58]. If these oscillations persist for a longer time and are greater than the oxide breakdown voltage they can damage the thin oxide transistors and hence lead to device failures. Also, they can interfere with the circuit under the normal operating conditions and can cause serious issues. So, the transient clamps must be analyzed for the robustness against oscillations.

The test bench to simulate the oscillation robustness of transient clamp is based on method reported in [58]. It is based on calculating the open loop gain and phase of the transient clamp. According to barkhausen criteria [61], the oscillations occur when the open loop gain is "1" and the phase of the open loop is 180^0 . In the transient clamps, due to odd number of inversions in inverter based clamp the condition of 180^0 phase is easily satisfied. Hence, the open loop gain should be kept less than "1" to avoid the oscillations. The test bench to simulate the open loop gain of clamp is shown in Figure 4-17 [58]. The feedback loop is

opened at the node 1 (Figure 4-4(b)) and the impedance seen from each side is added to the other side.

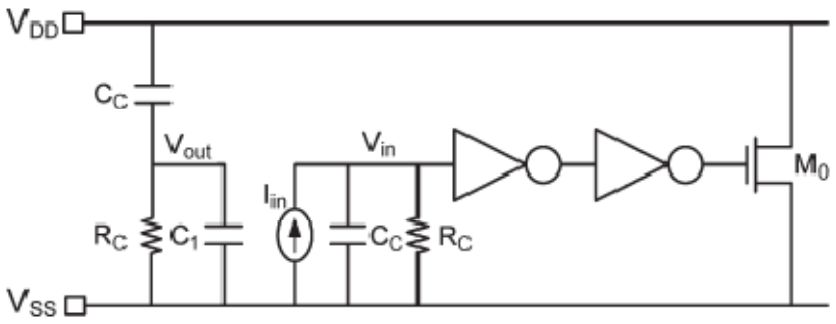


Figure 4-17: Test bench to simulate the open loop gain of inverter based clamp[58]

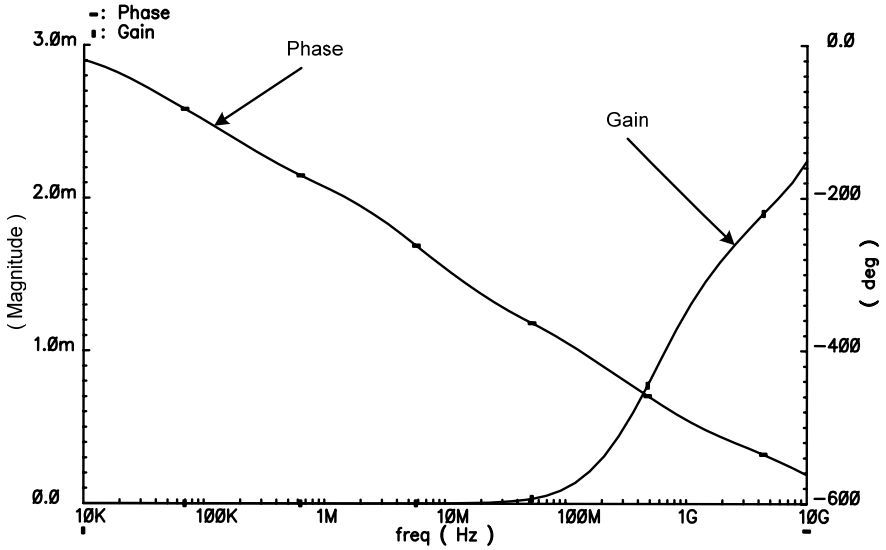


Figure 4-18: Open loop Magnitude and Phase of TSPC based Clamp

Figure 4-18 shows the simulation results for magnitude and phase of the open loop gain of TSPC based clamp. It can be seen that the magnitude of the open loop gain of the clamp is 0.0029 and is far less than 1. Hence the TSPC based clamp is highly stable. Moreover, compared with the SRAM based Clamp (Gain = 2), Thyristor based Clamp (Gain= 0.75) and

Flip-Flop based Clamp (Gain = 0.017), the TSPC based Clamp is the most stable transient clamp.

4.5 Low Noise Clamps

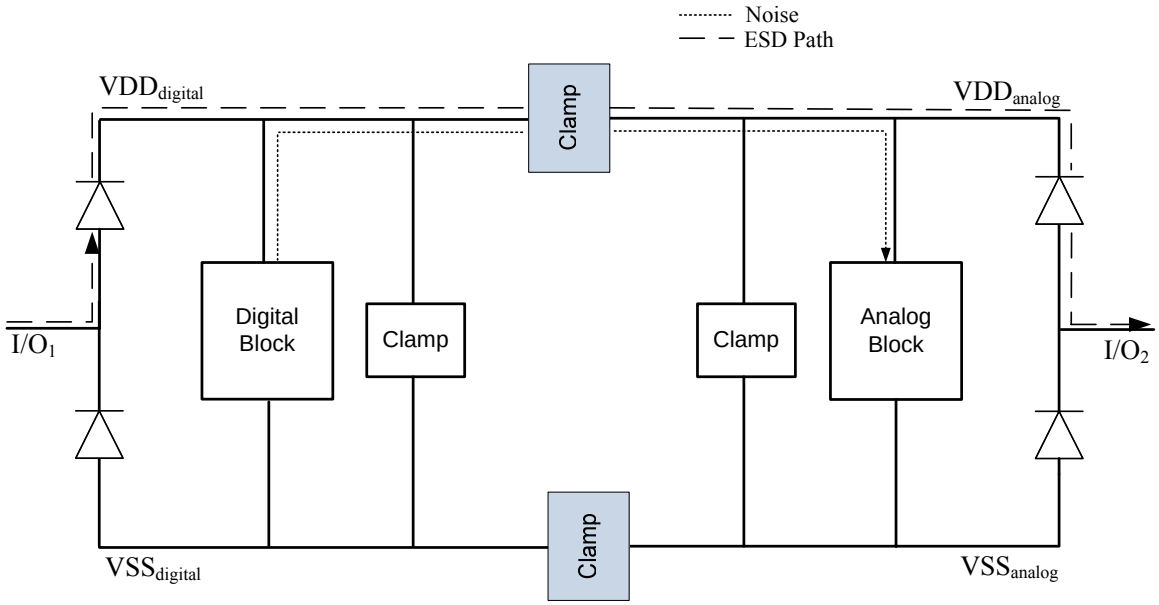


Figure 4-19: ESD Protection network showing ESD stress path and noise coupling

The scaling down of CMOS process technology has increased degree of integration, enabling growth of mixed-signal circuits. The integration of analog blocks such as ADC, PLL's, DLL's, oscillator etc. on digital chips has provided cheap system on chip (SOC) solutions. However, when analog and digital chip are combined into one single mixed-signal chip, on-chip noise coupling from the digital to the analog circuitry becomes a big concern. This problem can be solved by separating the on-chip power distribution networks for the analog and digital circuits. For noise immunity these power distribution networks should be isolated, however for ESD robustness of I/O pads there should be ESD protection circuits between the analog and digital supplies. Figure 4-19 shows an ESD protection network for a mixed-signal

chip containing analog and digital supply. There can be an ESD stress event between I/O pad of analog block and I/O pad of digital block. Hence, there are clamps/protection circuits between different supplies to provide the discharge path between the digital supply and analog supply. However, the noise coupled through clamp/protection circuits can significantly degrade the performance of mixed-signal circuits. This coupling noise cannot be suppressed easily because reducing the noise usually leads to the degradation of the ESD performance. Thus, typical ESD protection circuits and ESD circuit design methodology must be analyzed to find an optimum solution to increase the noise isolation as well as ensuring the ESD protection robustness.

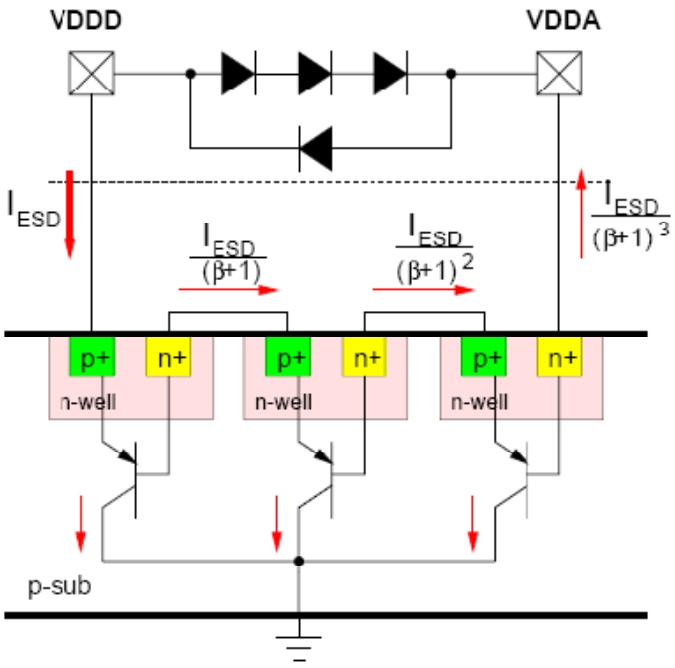


Figure 4-20: Schematic and Cross section of the Diode string based ESD protection methodology between analog(VDD_A) and digital(VDD_D) supply [66]

The typical ESD protection circuit used for power distribution networks is diode string structure (Figure 4-20). Diode string structures offer several advantages such as small size, ease of implementation etc. over [62][63] other typical ESD protection circuits like GGNMOS, LVTSCR, transients clamps etc. However, diode string protection circuits have a very poor noise rejection ratio due to variation of turn-on voltage of diode strings[64] and substrate injection current[65][66]. So, in our research a novel low noise ESD protection circuit has been proposed. The section 4.5.1 will introduce low noise Low Pass filter (LPF) based transient clamp. The section 4.5.2 will introduce an ESD circuit design methodology to reduce the supply noise by placing the analog block in the chip as far as possible from ESD protection circuits.

4.5.1 Low Pass Filter based Clamp

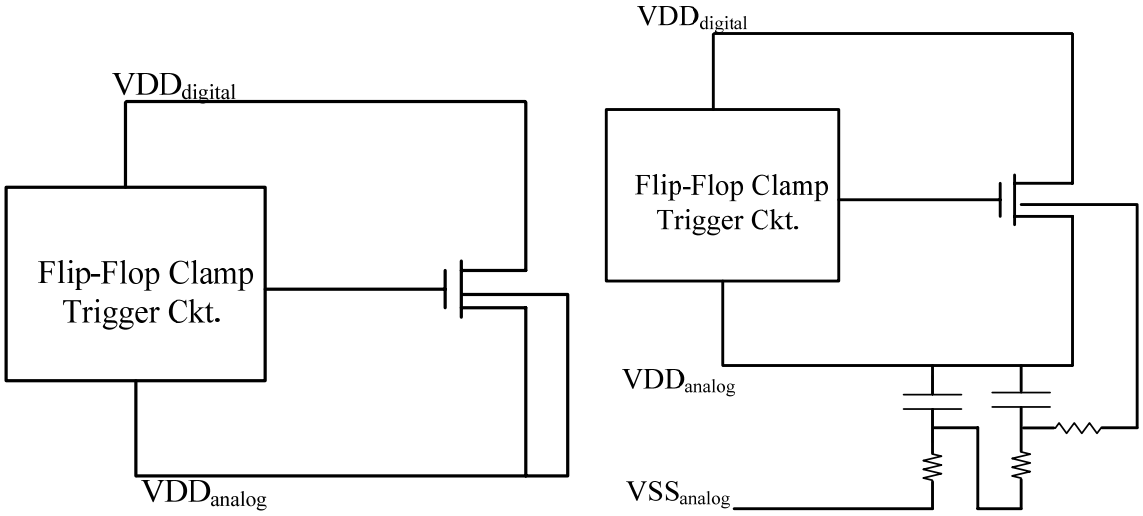


Figure 4-21: (a) Flip-Flop based Clamp (b) Proposed LPF based Flip-Flop Clamp

Figure 4-21(a) shows the normal Flip-Flop based Clamp [58] used between different power supplies i.e. analog supply and digital supply. The transistor offers better noise isolation

between the supplies as compared to the diode string. So, transient clamps are proposed instead of diode string structures for better noise isolation between the digital and analog supply. To further increase the noise isolation, a new Low pass filter based FF Clamp is proposed (Figure 4-21(b)). The LPF based FF Clamp is a modification of flip flop based clamp circuit. It has the following modifications (a) The substrate of the modified flip flop based clamp is grounded ($V_{SB} > 0$ V) which reverse biases the substrate-source junction. As a result, the threshold voltage (V_{TH}) increases and hence better noise supply isolation is achieved. (b) A low pass filter with resistor is added to the substrate , so high frequency digital noise is filtered from VSS_{analog} increasing the noise supply isolation.

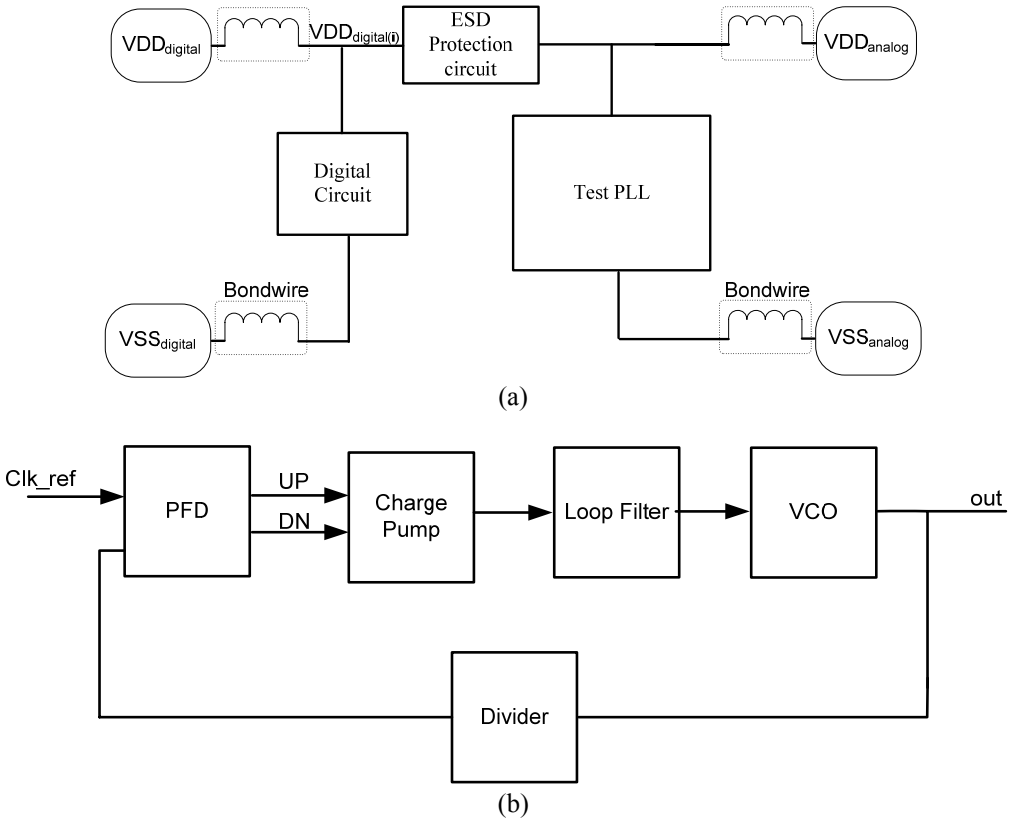


Figure 4-22: (a) Test bench to measure the noise performance of ESD devices (b) PLL block diagram

The simulations were done in the 90nm technology to verify the noise performance of the novel LPF based FF clamp. The supply noise isolation between the analog and digital circuit depends on various factors such as impedance of bond wire, capacitance between digital-analog supplies, capacitance between power-ground of analog/digital supplies and magnitude and frequency of switching noise on digital supply. The complex relationship between ESD performance and power supply noise isolation can be determined using the test bench shown in Figure 4-22(a) [66]. The test bench contains analog phase-locked loop (PLL) for monitoring noise or jitter, digital circuitry and ESD protection device between analog and digital supplies. The power busses (VDD_{analog} & $VDD_{digital}$) are connected through ESD protection circuits. This ESD protection circuit provide discharge path during the ESD stress, but it also provide path for noise coupling between VDD_{analog} and $VDD_{digital}$. The digital circuitry is modeled by the equivalent resistive and capacitive circuit. The noise is applied on the $VDD_{digital}$ and its effect on analog supply (VDD_{analog}) is measured by monitoring the jitter across the PLL.

The block diagram of the PLL used for our simulation is shown in the fig4-22(b). The Phase Frequency Discriminator (PFD) compares the phase of feedback signal with the reference clock and generates output signals UP and DOWN. The difference between the two signals is proportional to the phase difference between reference clock and feedback signal. Based on the output signal UP/DOWN the charge pump switches the current “in” or “out” to the loop filter. The loop filter converts the digital output into analog output to feed the voltage controlled oscillators (VCO) to perform corrective action.

The VCO inside the PLL is sensitive to the supply variations. The variation in the supply/ground voltages shifts the frequency of oscillation and increases the phase error of the PLL. The phase error accumulation takes place until the feedback loop corrects the frequency of the circuit. By measuring the jitter we can quantify the noise robustness of an ESD protection device. The lower the value of jitter, the higher is noise robustness and vice-versa.

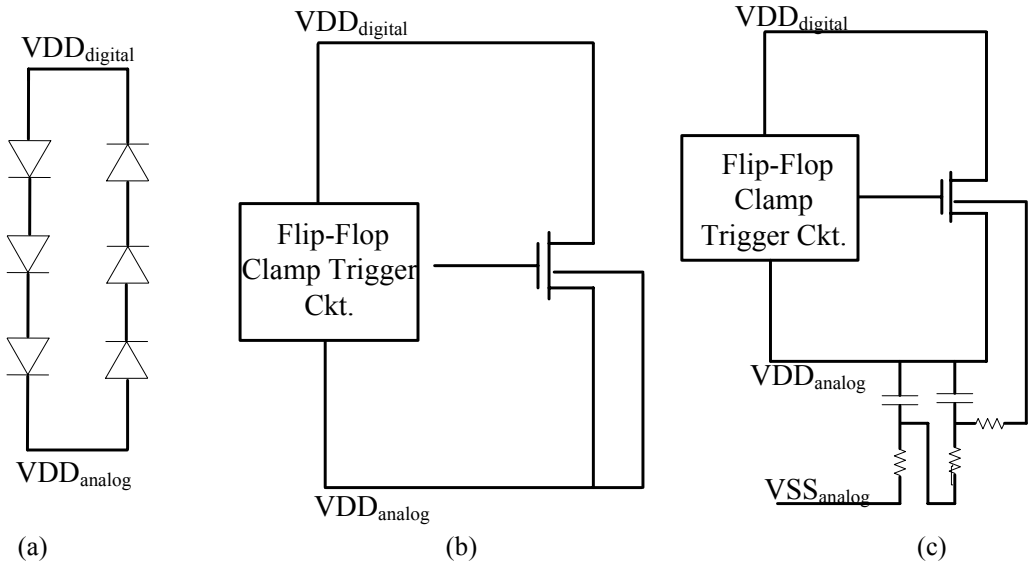


Figure 4-23: Block diagram of ESD structures (a) Diode String (b) FF Clamp (c) Low Pass filter based FF Clamp

The LPF based FF Clamp was taped-out in the ST 90nm test chip. To compare and contrast the performance of LPF based FF clamp with other clamps, two other transient clamps diode strings and FF Clamp were also taped- out. The clamps were designed to have the same ESD robustness using device simulator MEDICI. Figure 4-23 shows the block diagram and Figure 4-24 (a),(b),(c) show layout of different clamps taped out in the ST 90nm technology. In order to measure the quantitative performance of the clamps, PLL was also implemented in the test chip. The PLL can be tuned in the frequency range of 100 – 300

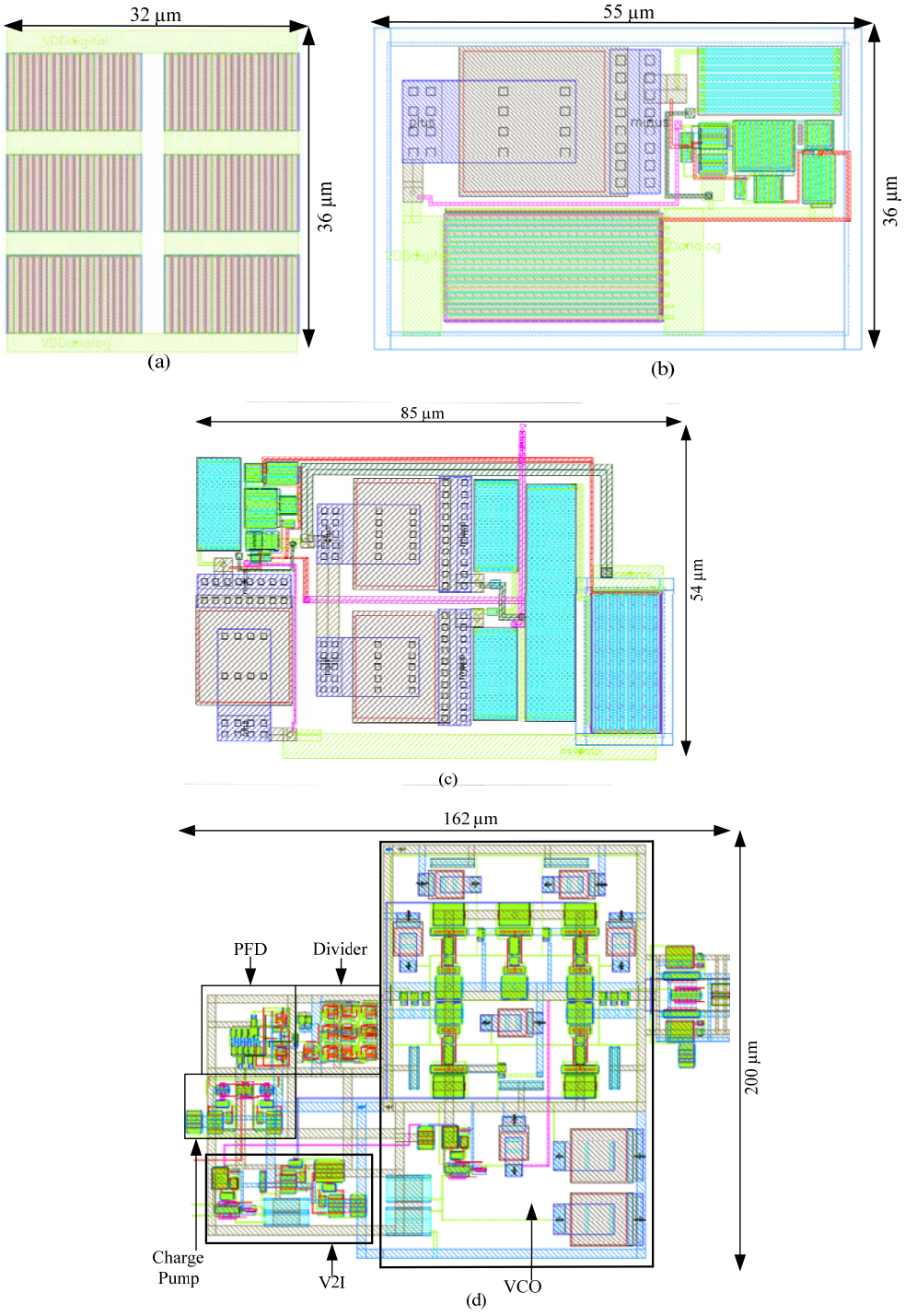


Figure 4-24: Chip Layout in ST 90nm (a) Diode String (b) FF based Clamp (c) LPF based FF Clamp (d) PLL

MHz . The loop filter if drawn in layout occupies a area of 2.2 mm^2. In order to save the area on the chip and to have flexibility, an off-chip passive filter was preferred. Figure 4-24(d) shows the layout of the PLL implemented in the test chip.

4.5.1.1 Post Layout Simulation Results

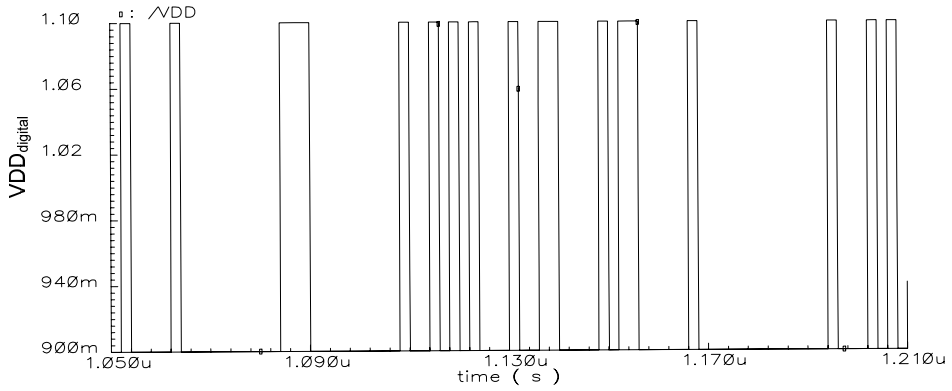


Figure 4-25: 2 Gb/s Pseudo Random Signal applied on $VDD_{digital}$

The digital noise is modeled by a pseudo random signal on $VDD_{digital(i)}$. A 2Gb/s 200 mV peak to peak PSRS (Figure 4-25) is applied to the digital supply ($VDD_{digital(i)}$). The PLL is locked at 178 MHz and the jitter is measured for different ESD devices when the same digital noise is applied to them. Table 4-1 compares the ESD performance and noise performance of

Table 4-1:Comparing Noise Isolation Of Different ESD Protection Methods

	HBM Protection	Jitter (p-p)
PLL without ESD protection	-	82.81ps
Diode String	2kV	139.07ps
FF based Clamp	2kV	117.62ps
FF based Clamp with LPF	2kV	102.81ps

different ESD structures when the same noise signal is applied to them. It can be seen that ESD protection circuits have significant impact on increasing jitter of analog phase-locked loop. Also, it can be observed that Flip Flop based Clamp with LPF has least impact on increasing the jitter of the circuit and hence has better noise isolation compared to diode string and FF based Clamp.

4.5.2 Impact of placement of Clamp on Jitter

The impact of placement of clamp with respect to analog blocks can also have a significant impact on the noise performances. In our research, we have tried to study this relationship by using a FF based Clamp as an ESD protection device and a PLL for measuring the noise

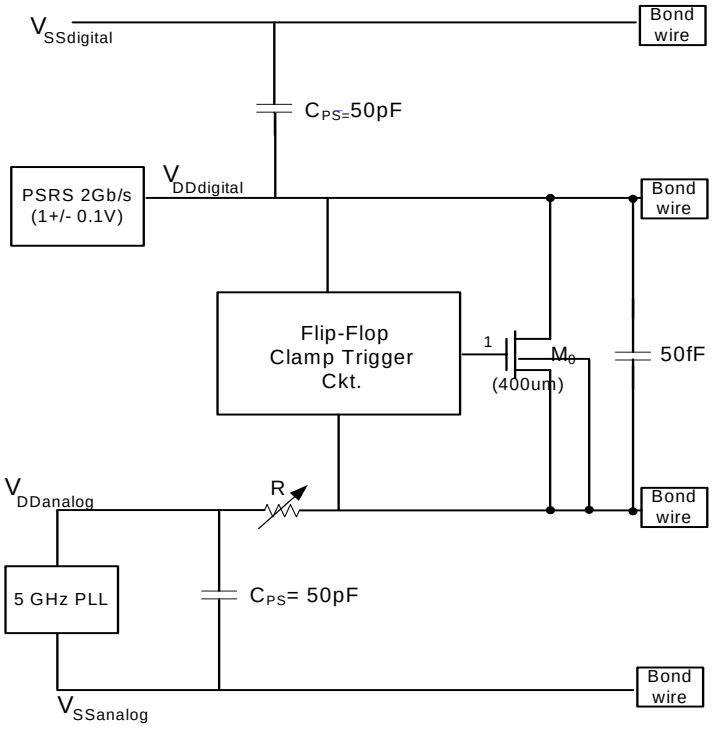


Figure 4-266: Test bench for measuring impact of placement of clamp with respect to analog block on jitter

performance of the analog system. Figure 4-26 shows the test bench for measuring the impact of placement of clamp with respect to analog block on jitter.

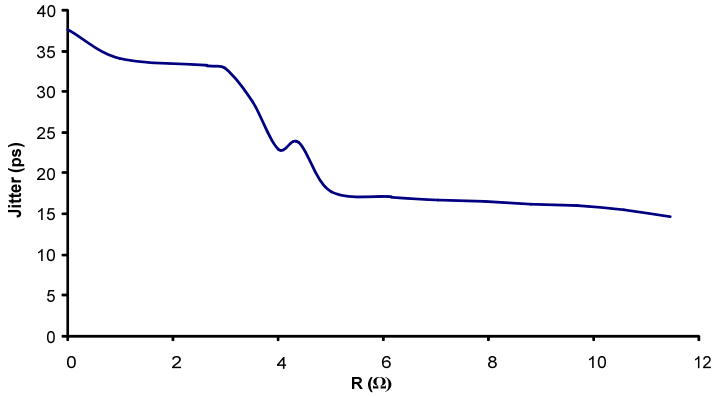
The ESD protection clamp is placed near I/O pad and the analog circuit is placed away from the pad as shown in Figure 4-26. The distance between the clamp and analog circuit is varied by varying the resistance (R) in multiples of the sheet resistance (R_{SHEET} = 0.11 $\Omega/\mu m^2$ for 90nm tech.) . The digital circuits and analog circuits is modeled by equivalent capacitance (C_{PS} = 50pF) and overlap capacitance between analog and digital supply is

Table 4-2: Jitter, peak-peak noise voltage variation on VDD_{analog} by varying R

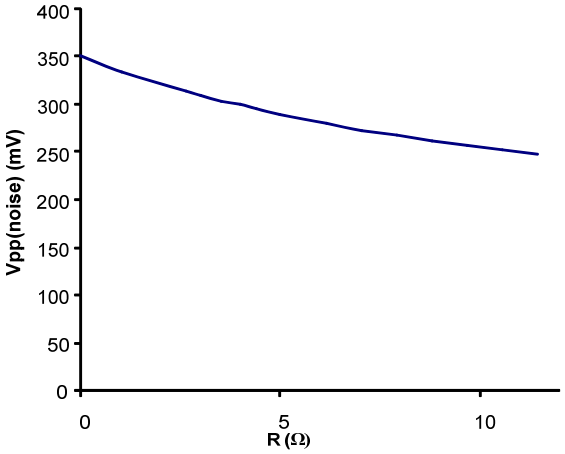
Res (Ω)	Jitter (ps)	VDD_{analog} (mV) (p-p)	Res (Ω)	Jitter (ps)	VDD_{analog}(mV) (p-p)
0	37.6	351.1	6.16	17.06	279.7
1	34.0631	334.9	7.04	16.6956	273.3
2.64	33.203	313.9	7.92	16.5481	267.9
3	32.8991	309.7	8.8	16.18	262.4
3.5	28.853	303.8	9.68	15.9336	257.3
4	22.902	300.3	10.56	15.4565	252.8
4.4	23.7004	295.4	11.44	14.7	248.5
5	17.7163	289.5			

modeled by 50fF capacitance. The digital noise is modeled by a pseudo random signal on $VDD_{digital}$. A 2Gb/s 200 mV peak to peak PSRS is applied to the digital supply $VDD_{digital}$ as shown in Figure 4-25. The phase-locked loop (PLL) is locked at 5 GHz and the peak-peak

jitter and peak-peak noise variation on VDD_{analog} is measured for different values of R when same digital noise is applied to them. The resistance "R" is varied from "0" sheet resistance (R = 0) to "100" sheet resistance (R= 11 Ω). The table 4-2 shows the jitter, peak-peak noise voltage variation for different values of R.



(a)



(b)

Figure 4-277: (a) Jitter v/s R (b) Vpp(noise) v/s R

It can be observed from the Figure 4-27(a) that as the resistance is increased, the jitter decreases linearly initially and then becomes almost constant after resistance becomes greater

than 6 Ω. The jitter has decreased from 37.6ps for R=”0” to 14.7ps for R=”11.44 Ω”, a reduction of more than 200%. Also, it can be observed from Figure 4-27(b) that the peak-peak voltage noise variations on VDD_{analog} decreases linearly with increasing resistance. Thus if possible the power clamps should be placed as far as possible from the analog blocks for superior noise performance.

4.6 Summary

The non-snapback devices particularly transient clamps have been explored in this chapter. Transient clamps have been purposed to address the critical issues like leakage current, supply noise isolation, oscillations etc. A new oscillation robust clamp based on TSPC latch has been proposed in this research. It has been found from our simulations that the TSPC based clamp is most stable clamp. Also, a novel method has been proposed to reduce the leakage current by more than 200,000X with minimal comprise on the ESD performance. Finally, a LPF based FF clamp has been purposed to increase supply noise isolation.

Chapter 5
Conclusion

Electrostatic discharge is increasingly becoming a major reliability threat in the semiconductor industry. The scaling of CMOS process technology is further aggravating the situation. The reduction of the breakdown voltage, increased failures due to CDM, noise coupling between analog and digital supply, increased leakage current etc. are all consequences of the scaling. Thus designing of ESD protection circuit satisfying all these criteria's is becoming increasingly difficult.

In chapter 2, whole chip ESD protection methodology has been discussed. The various zapping modes against which ESD protection must be provided were also discussed. The whole chip ESD protection methodology can be provided using either Pad or Rail based methodology. Both these methodology have been discussed in detail and it has been concluded that the pad based ESD protection methodology uses snapback devices due to their small size and Rail based ESD protection methodology uses mostly non-snapback devices. Finally, in which conditions to use pad based methodology and in which conditions to use rail based methodology has been proposed.

In chapter 3, the different snapback devices have been discussed. The chapter starts by explaining the principle and limitation of traditional snapback devices like GGNMOS, SCR, and LVTSCR. The traditional devices have either low holding voltage or high triggering voltage. Also, the turn-on time of these devices is very high, making them unsuitable for handling CDM stress. Some of the state of the art clamps like DbtSCR, NANSCR etc. have

been discussed to counteract the above mentioned problems. Finally two novel snapback devices – DSCR, NMOS-DSCR have been purposed. The DSCR offers a low capacitance solution without comprising the ESD protection level making them suitable for high speed applications. The NMOS-DSCR offers excellent CDM robustness, without sacrificing ESD protection level.

Chapter 4 discusses the non-snapback devices suitable for Rail based ESD protection methodology. Some of the state of the art clamps or non-snapback devices like FF based Clamp, SRAM based clamp etc. have been discussed. Transient clamps have been purposed to address the critical issues like leakage current, supply noise isolation, oscillations etc. A new oscillation robust clamp based on TSPC latch has been also proposed in this research. It has been found from simulations that the TSPC based clamp is most stable clamp. Also, a novel method has been proposed to reduce the leakage current by more than 200,000 times (simulation result) with minimal comprise on the ESD performance. Finally, a LPF based FF clamp has been purposed to increase power supply noise isolation.

Chapter 6
Future Work

In the thesis, post layout simulation results for the TSPC based Clamp, LPF based FF Clamp and low leakage clamps have been reported. In the future, the measurements will be done on the chip when it will come back from the fab. Also, the NMOS-DSCR device will be fabricated in the 90nm technology to validate its CDM performance on silicon. The improved CDM robustness of NMOS-DSCR device comes at the added cost of the increased capacitance. Therefore, in future devices must be investigated to improve the CDM performance without adding any extra capacitance.

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Glossary

C

CDM	Charged Device Model
CMC	Canadian Microelectronics Corporation

D

DbtSCR	IBM's Darlington based SCR
DSCR	Darlington based SCR
DUT	Device under Test

E

ESD	Electrostatic Discharge

G

GGNMOS	Grounded Gate NMOS
GST-LVTSCR	Gate Substrate triggered low voltage triggered SCR
GT-LVTSCR	Gate triggered low voltage triggered SCR

H

HBM	Human Body Model

L

LPF	Low pass filter
LVTSCR	Low Voltage Triggered SCR

M

MM	Machine Model

N

NANSCR	Native NMOS SCR
NMOS-DSCR	NMOS Darlington based SCR

P

PSRS	Pseudo Random Signal

S

SCR	Silicon Controlled Rectifier
SOC	System on Chip
ST-LVTSCR	Substrate triggered Low voltage triggered SCR

T

TLP	Transmission line pulsing

V

Vf-TLP	Very fast transmission line pulsing