Active Matrix Flat Panel Bio-Medical X-ray Imagers

by

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I hereby declare that I am the sole author of this thsis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be electronically available to the public.

Abstract

This work investigates the design, system integration, optimization, and evaluation of amorphous silicon (a-Si:H) active matrix flat panel imagers (AMFPI) for bio-medical applications. Here, two hybrid active pixel sensor (H-APS) designs are introduced that improve the dynamic range while maintaining the desirable attributes of high speed and low noise readout. Also presented is a systematic approach for noise analysis of thin film transistors (TFT) and pixel circuits in which circuit analysis techniques and TFT noise models are combined to evaluate circuit noise performance. We also explore different options of system integration and present measurement results of a high fill-factor (HFF) array with segmented photodiode.

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1 Introduction

Techniques for practicing x-ray imaging have largely unchanged despite continuous research efforts. It is not until recently that fully integrated digital detectors are made possible due to advancements in large area electronics. Digital imaging revolutionizes the procedure of radiology in many aspects. Conventional film/cassette method requires a time consuming photographic development process that necessitates human handling. This follows with storage and archiving of the processed film which needs tremendous resource. To the contrary, digital detectors provide immediate feedback to radiologists through computer displays, and enable electronic storage that is both convenient and economically attractive. Digital x-ray imaging also opens the door to many previously unachievable applications such as computer aided imaging processing, remote diagnosis, and more convenient patient and x-ray room management [1].

The driving force behind digital x-ray imaging is amorphous silicon (a-Si:H) technology, initially developed for liquid crystal displays (LCDs). The a-Si:H readout array coupled with x-ray sensors can be manufactured at very low cost especially in comparison with crystalline silicon alternatives such as Charge-Coupled Device (CCD) or CMOS technologies. In addition, the a-Si:H technology allows fabrication of detector arrays comparable in size with the body parts to be imaged, thus practically eliminating the need for lenses or x-ray focusing. Combined with the inherently desirable material and fabrication attributes such as low temperature processing and high uniformity over large area, the a-Si:H flat panel matrix array manifests itself as a promising candidate for digital x-ray imaging.

1.1 Digital Imaging Requirements

Since the adoption of x-ray imaging to medical applications, radiologists have developed various techniques for diagnosis and interpretation based on the processed film. Therefore, one of the key design requirements for digital imaging is backward compatibility. Exposures generated by flat panel detector should display similar image characteristics such as contrast ratio and coloring. It is for this reason, a list of parameters for specifications can be identified. Table 1-1 illustrates the technical specifications for three typical x-ray imaging modalities, namely radiology (chest x-ray) for bone fracture identification, fluoroscopy for real-time x-ray video, and mammography for soft tissue (breast) imaging [1][2].

The image charge per pixel data given in the table for various modalities is a useful quantity, and when combined with a given pixel capacitance, it allows to determine the minimum signal voltage strength and hence also the tolerable noise level. In addition, it allows determination of the photocurrent and photocurrent density as long as the total exposure time is known. This gives a ballpark idea of the performance requirements for each modality.

In addition, the three imaging modalities impose distinct system requirements that necessitate the design of specialized detectors. Conversely, a single detector design with the capability of multi-modality imaging is very attractive from the standpoint of compactness and economics. Hence, the design and study of digital x-ray imagers ought to progress in the direction of realization of detectors with adjustable signal sensitivity and readout rate to satisfy the wide range of requirements from different modalities. This

constitutes one focus of this thesis. In later chapters, we preent detectors designed for high dynamic range and programmable gain level that proves amenable for multi-modality x-ray imaging.

Table 1-1: Parameters for digital medical imaging systems [1][2].

Clinical Task	**Radiography**	**Mammography**	**Fluoroscopy**
Detector size (cm)	35 cm x 35	18 cm x 24	25 cm x 25
Pixel size (μm)	200 x 200	50 x 50	250 x 250
Number of pixels	1750 x 2150	3600 x 4800	1000 x 1000
Readout time (s)	< 5	< 5	1/30
X-ray spectrum (kVp)	110-120	30	70-80
Exposure range	30–3000 μR	0.6-240 mR	0.1-10 μR
Mean Exposure	300 μR	12 mR	1 μR
Image charge per pixel (e^- /pixel/mR)	3.45 $x10^6$	1.68 $x10^6$	4.91$x10^6$
Noise level (μR)	6	60	0.1

1.2 Imaging Architectures

There are two architectures currently employed in large area AMFPIs: the linear architecture, used in photocopiers, fax machines, and scanners, and the two-dimensional array architecture, employed in digital (including video) lens-less cameras as well as x-ray imaging systems [3] [4] [5]. In both architectures, the basic imaging unit is the pixel, which consists of an image sensor and on-pixel circuit. The pixel is accessed by a matrix of gate and data lines, and operated in storage (or integration) mode. Here, during the off-period of the pixel, the sensor charge is integrated in the sensor element, and when the pixel is addressed, the charge is transferred to the data line where it is then detected by a charge sensitive amplifier. Various metal interconnects are used to control the readout of image information from the array. The imaging system is completed with peripheral circuitry that amplifies, digitizes by analog-to-digital (A/D) conversion, and synchronizes the readout of the image. A computer then manipulates and distributes the final image to the appropriate soft- or hard-copy device. A sample array of imaging pixels with column parallel readout architecture is illustrated in Figure 1-1.

1.3 Detection Schemes

Different schemes can be employed for x-ray imaging. One configuration utilizes a phosphor layer which converts x-rays into visible photons which are subsequently detected by a-Si:H photo-sensors [6] [7]. An example of optical detection using a phosphor screen as the scintillating layer, an Indium Tin Oxide (ITO)/a-Si:H Schottky photodiode as the optical sensor, and a readout TFT is shown in Figure 1-2.

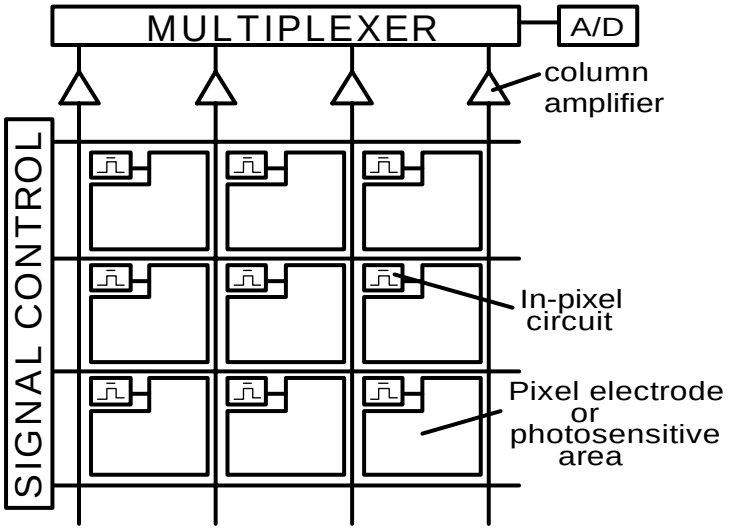

Figure 1-1: Schematic diagram of an active matrix detector array with peripheral electronics.

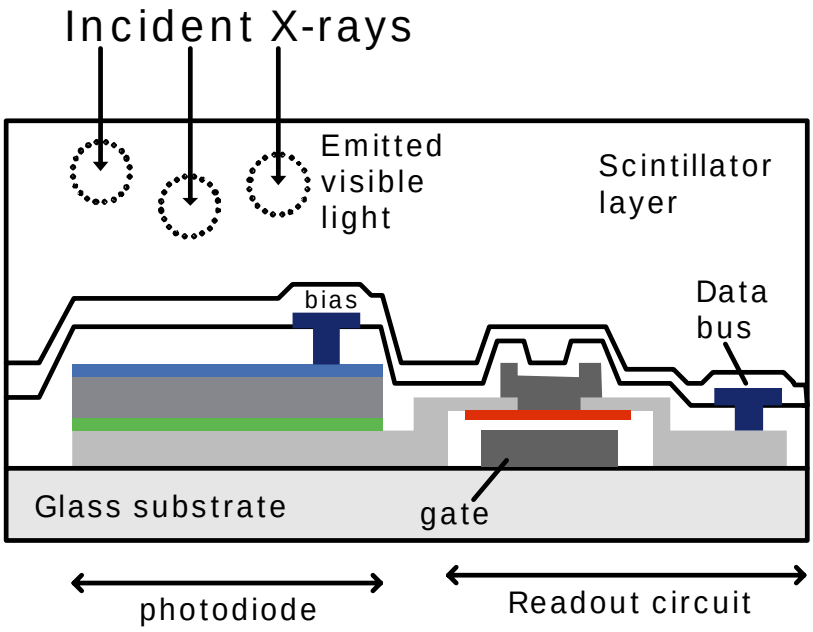

Figure 1-2: Indirect x-ray detection method based on ITO/a-Si:H Schotty photodiode integrated with phosphor layer.

An alternative arrangement uses a photoconductor such as bulk amorphous selenium (a-Se) for photo-electric conversion [8]. This type of detection requires high electric fields across a thick (~500 μm) a-Se layer for efficient electron-hole separation and collection. The generated charges are separated by a strong electric field established by the bias voltage, and accumulated in a storage capacitor that is connected to a read-out TFT [5] [9]. This scheme is illustrated in Figure 1-3.

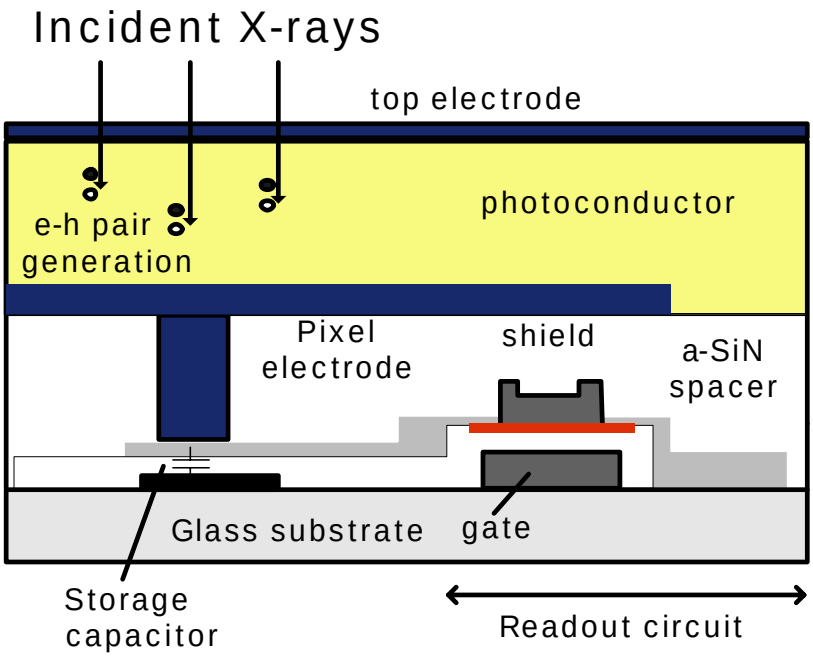

Figure 1-3: Direct x-ray detection method using amorphous selenium [5].

Currently, the design of arrays is constrained by a number of factors including device mobility, minimum feature size, alignment tolerances and yield. Thus it is very challenging to implement features that would speed up or simplify the operation of these arrays. Such features include pre-amplification and multiplexing circuitry, which would simplify external electronics and possibly improve the signal-to-noise performance. For example, as a shift register for control of the TFT gate lines implemented in a-Si:H would enable on-chip multiplexing for the gate/readout lines. This in turn would greatly reduce the number of electrical connections that would have to be made between the array and the external electronics, hence making the physical array more compact. More importantly, if amplification were performed in the pixel itself, it would reduce performance requirements on the charge amplifier or eliminate the need for a charge amplifier altogether. The price to pay for this reduction in external electronics is the

increased circuitry per pixel. However, some pixel configurations are not as amenable to on-pixel integration. An example is the indirect detection pixel architecture, where the TFT switch lies next to the sensor (see Figure 1-2), therefore taking up pixel area and lowering the fill-factor. In Chapter 5, a high fill factor architecture is presented where the TFT layers are vertically integrated to alleviate some of the limitations faced in the indirect detection scheme.

In contrast, a continuous layer architecture in the direct detection scheme provides a more practical array with a considerably finer pixel pitch (see Figure 1-3). In this configuration, the TFTs are directly positioned under their corresponding sensors. With such a configuration, there is no longer a need for TFT address lines extending from sensor to sensor as it serves to reduce the fill factor [10]. Furthermore, with such an array, the finest pixel pitch is only limited by the minimum TFT size and alignment/fabrication tolerances. The sensor shown in Figure 1-3 is an example of a continuous layer sensor using a thick photoconductor such as a-Se. This method of stacking the sensor on top of the TFT also enables the possibility of a multi-transistor pixel, i.e., an active pixel. The challenges with this architecture include the management of stress induced by many stacking layers [11] [12] as well as handling adjacent pixel cross-talk [7].

1.4 Thesis Organization

This thesis investigates the design, evaluation, and integration of pixel architectures for large area digital imaging for diagnostic medical applications. First, the underlying (amorphous silicon) technology is discussed with emphasis on the operation

and characteristics of a-Si:H TFTs. The TFT serves as the building block for the active matrix imaging array and it is discussed in Chapter 2.

Chapter 3 analyzes various designs of pixel readout circuitry. Here, conventional passive (PPS) and active (APS) pixel sensors are discussed along with highlights of their respective design tradeoffs. Two flavors of hybrid active pixel sensors (H-APS) are investigated with emphasis on improving signal gain and dynamic range. H-APS designs are capable of providing real-time, high gain, and wide dynamic range readout and are especially attractive for applications entailing low x-ray dosage.

Chapter 4 follows with an analysis of the noise performance of pixel circuits. The TFT noise (low and high frequency) are discussed and models verified with measurement results. The noise models are then extended to pixel circuit noise analysis. The noise in H-APS designs are then compared against theoretical estimates. Although the noise in the H-APS is found to be similar to the APS it provides superior dynamic range and technology scalability. Lastly, the noise models are used to optimize pixel designs with respect to parameters such as TFT bias, aspect ratio, channel length, and pixel capacitance.

Chapter 5 describes pixel integration with light sensitive detectors. Pixel integration architectures are discussed where fill-factor, capacitive coupling, and noise are considered. Also presented is an integrated pixel circuit using high fill-factor (HFF), segmented PIN.

Chapter 6 concludes the thesis and outlines the possible future work in the area of digital imaging.

2 Amorphous Silicon Technology

Amorphous silicon (a-Si) lacks the long range order in the lattice so differentiating it from its crystalline counterpart. The amorphous structure arises due to deviations in bond lengths and angles, structural defects, and variable bonding configurations, and impact different aspects of device performances. Nevertheless, one of the most attractive attributes of a-Si is its ability to be deposited uniformly on large substrates (up to several square meters) at a relatively low cost, and low temperatures [13]. a-Si also makes high quality hetero-interfaces, therefore, it can be deposited on various substrates such as insulators, metals, and semiconductors. a-Si TFTs have very low leakage current in the transistor off state and high on-resistance, making it very suitable to be used as switches in applications such as the liquid crystal displays (LCDs) and digital imagers [14].

One the major disadvantages of a-Si is the presence of metastable defects in the material that affects device reliability [14]. These defects cause the threshold voltage, V_T, of a TFT to increase significantly after prolonged operation pertaining in the ON state. Another significant disadvantage is that the electron and hole mobilities are extremely low (~ 1 cm^2/Vs and ~ 0.001 cm^2/Vs respectively) [14]. This consequently entails large transistor sizes to compensate the low current drive, and results in high capacitances, and large operating voltages. Such problems do not have a major adverse effect on passive pixel imaging arrays since TFTs in those panels operate as voltage switches, and do not need to supply constant currents. However, we are faced with design constrains when TFTs are extended from passive switches to active driving devices as we will see more in

Chapters 3 and 4. Moreover, the TFT switches operate at a very low duty cycle in imaging arrays, typically less than 0.2%, which limits the degree of V_T-shift. A shift in V_T increases the charge transfer time since the RC delay of the data path becomes higher when the switch resistance is higher. This can be overcome by factoring the worst-case V_T into the design by appropriate increase in driving potential.

Because of material and device shortcomings, researchers have explored other TFT technologies in an attempt to mitigate these issues through material quality improvement. Polysilicon (poly-Si) has intermediate-range order in its lattice structure, thus it has numerous 'grains' of crystalline silicon with amorphous grain boundaries between crystals with different orientations. Because each grain itself is highly crystalline, polysilicon TFTs experience minimal V_T-shift and have high mobilities (~100 cm^2/Vs). Polysilicon can be prepared by first depositing amorphous silicon over large area, and subsequently subjecting the material to laser annealing, which locally heats up the layer to several hundred degrees Celsius and gives the lattice enough energy to re-crystallize. Despite such commendable TFT characteristics, poly-Si technology is still in its early stages of development with many hurdles to overcome, such as grain boundary positioning, uniformity over large area, and manufacturing throughput [15].

Despite intensive research, there is no material that possesses the carrier mobility and stability similar to that of crystalline silicon, at the same time with the uniformity and cost effectiveness of a-Si. Table 2.1 summarizes and compares the key attributes of poly-Si, a-Si and crystalline silicon (adapted from [15] and [16]).

Attribute	Crystalline Silicon	Polysilicon	Amorphous Silicon
Mobility	~ 1000 cm^2/Vs	~ 100 cm^2/Vs	< 1 cm^2/Vs
Smallest Pixel Size	Small (~ 5μm x 15μm)	Medium (~ 100μm x 100μm)	Large (> 150μm x 150μm)
ΔV_T	Good	Good	Poor
V_T Uniformity	Good	Poor	Good
Manufacturability	Mature but expensive, Small wafer sizes only (12")	Research process, expensive, limited glass substrate sizes	Mature, inexpensive, Large glass substrates (2m x 2m)
Flexible Substrates	No	Possible – under development	Yes – plastic and metal foil

Table 2.1. Comparison of different transistor technologies.

2.1 Amorphous Silicon TFT Characteristics and Operation

As mentioned previously, amorphous silicon is inherently an imperfect material due to the fact that it lacks the long-range order that is characteristic of crystalline silicon. Initial studies of the material have shown that the high concentration of defect density prevents its use as a semiconductor, and doping was once considered impossible. It was later demonstrated that the defect density of the a-Si can be reduced substantially by introducing hydrogen during the deposition process through the use of glow discharge of

silane gas [17]. This discovery made way for the fabrication of p-n junctions and eventually the thin film transistor [13]. Since then, the a-Si:H TFT has made its way to becoming the enabling technology for the active matrix LCD display industry and subsequently digital x-ray imaging.

2.1.1 a-Si TFT Structure

It is possible to fabriate a-Si:H TFTs using different structures [20]. The most popular and robust structure is the inverted-staggered TFT as shown in Figure 2-1.The in-house fabrication TFT at University of Waterloo utilizes this structure and it is the building block of pixel architectures and arrays considered in this thesis.

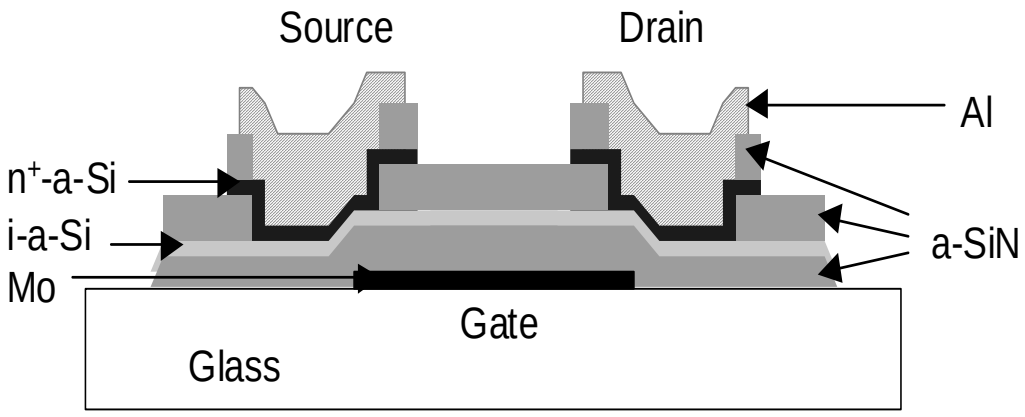

Figure 2-1. Cross-section of an inverted-staggered a-Si:H TFT.

The complete fabrication process requires five masks – gate metal, transistor islands (gate and top dielectric) and channel layer, n^+ patterning layer, via, and top metal layer masks. The integration of a TFT circuit with the sensor in an imaging array requires additional layers and masks. These are discussed in Chapter 5.

Unlike CMOS transistors in c-Si technology, the high concentration of defect states in a-Si makes it very difficult to achieve inversion. As a result, a-Si:H TFTs are operated in accumulation mode, which makes the device functionally similar to the enhancement mode NMOS transistor. It is very important to note, however, that the underlying physics that governs device operation is different between a-Si:H and c-Si.

2.1.2 Density of States in a-Si:H

Figure 2-2 illustrates the density of states (DOS) distribution versus energy for c-Si [21]. The perfect crystal lattice and the minimal structural defects in the material result in a periodicity of electron wave functions. Hence, the DOS is well defined with abrupt edges in both conduction and valence bands that leads to a distinguishable band gap.

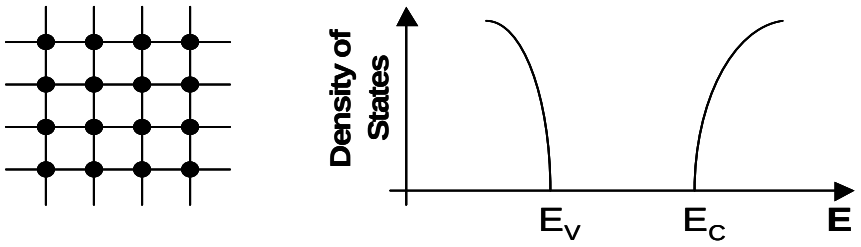

Figure 2-2. Atomic Structure and DOS distribution in crystalline silicon.

To the contrary, amorphous silicon possesses lattice periodicity only in short-range order (only up to 2 atomic distances). Since electronic properties are largely influenced by short range order, similar band diagram analysis can be modified to describe the electronic behavior with modification. The presence of long-range structural disorder in amorphous silicon affects the shape of the density of states (DOS). Consequently, the energy band model of crystalline silicon does not directly apply to the

case of a-Si:H. The DOS for amorphous silicon exhibits a complex dependence on energy and varies with the material preparation conditions [22].

Figure 2-3 shows the DOS distribution of typical amorphous silicon material [21]. Deviation from the crystal lattice bond lengths and angles in the amorphous material causes band tail states to extend beyond the conduction and valence band edge into the mobility gap. As it is discussed later in the TFT operations, the band tail states (especially the conduction band tail) influences the field effect mobility and consequently the current driving capability of TFTs.

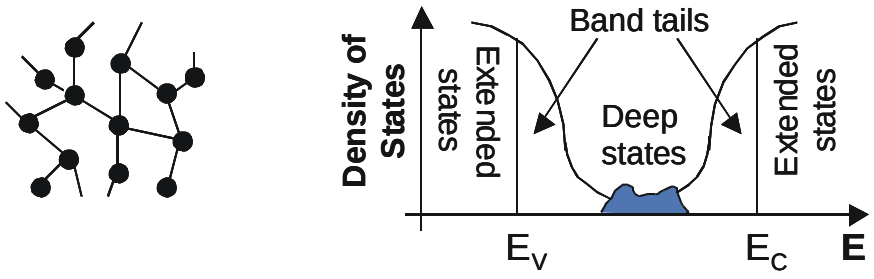

Figure 2-3. Atomic Structure and DOS distribution in a-silicon (adapted from [21]).

During the formation of energy bands from the overlap of electron wave functions, both bond length and angle deviation from perfect crystal lattice affects the valence band tail. It is for this reason, the valence band tail in a-Si:H is typically wider than the conduction band tail [23]. The material hole mobility is thus lower than electron mobility due to carrier trapping near the tail states. Additionally, the amorphous nature of a-Si:H has dangling silicon-silicon bonds that act as lattice defects. These defects correspond to carrier traps within the mobility gap, and are commonly known as deep

states. These deep defect states (see Figure 2-3) strongly influence the electronic properties of devices, such as the subthreshold slope of a-Si:H TFTs and V_T. [24]

It is worth of nothing that the band tail and defect states behave differently from the states up in the conduction and valence bands. Carriers in the conduction and valence bands are not spatially confined and are therefore free to move, thus these states are known as extended states. The mobility of the carriers in extended states is much higher than that of carriers in localized trap states. Conduction in the tail or deep states, on the other hand, is prone to carrier trapping and de-trapping, hence the carrier mobility is lower. The mobility edge is customarily defined as the energy level where the extended states meet the tail states in the DOS distribution, and is difficult to define for amorphous material [25]. Carriers within the gap do not contribute to significant current due to their low mobility. It provides a more practical means to gauge the material mobility gap (rather than the band gap concept in crystalline silicon) [23].

2.1.3 Device Operation: Static Characteristics

Similar to a c-Si MOSFET, an a-Si:H TFT is also a field effect three terminal device. The potential applied to the gate determines the band bending in the semiconductor channel layer, enabling current conduction. This section outlines the static TFT operation as a function of gate voltage.

The basic device operation in the static mode is strongly influenced by the localized electron states (both tail and deep) in the bandgap of amorphous silicon. In c-Si MOSFETs, the charge induced in the semiconductor by the applied gate voltage is primarily made up of free carriers. In a-Si:H TFTs, most of the induced charge is trapped

in localized states, and only a small portion (rarely larger than 10%) contributes to free carriers [25]. Moreover, the mobility of carriers in the extended states is also small comparing to c-Si because of the amorphous nature of the material, which causes additional limitation to the driving ability of the TFTs.

As previously mentioned, trapping of induced charge and resulting movement of Fermi level are responsible for the behavior of a-Si:H TFTs [20]. At zero gate voltage, there is very minimal band bending and is assumed as the flat band condition. When gate voltage is increased, downward band bending occurs at the silicon-insulator (bottom interface as shown in Figure 2-4). The band bending causes an accumulation of electrons near the surface in TFTs, occupying deep states as well as surface interface. This causes the Fermi level at the gate insulator-semiconductor interface to cycle through the deep states initially making its way up to the tail states [20]. The drain-source current in this regime is due to the small fraction of the band-tail electrons above the conduction band mobility edge. The space charge in the deep states increases in proportion to the gate voltage, but the current increases exponentially. If the deep state density was constant, then the logarithmic subthreshold slope would be inversely proportional to the square root of the density of states [20].This region of TFT operation is dominated by the behavior of the deep states and is commonly known as the subthreshold region.

As the gate voltage increases, the Fermi level further rises towards the conduction band. The majority of the induced charge becomes trapped in the tail states rather than the deep states as the latter become occupied. This gives rise to an above threshold region. The Powell model defines the TFT threshold voltage as the point where the Fermi level becomes “pinned” in the trap states [20]. The conduction band tail state density

increases so rapidly with energy that when the Fermi level enters these states, most of the induced charge occupies the states above the Fermi level. As a result, the shift of the Fermi level with the gate voltage in this regime is much smaller than in the sub-threshold regime [25]. The drain-source current then becomes a power law function of the gate of the gate voltage. It is worthy of note that the field-effect mobility is much less than the extended state mobility because most of the induced charge goes into the tail states with only a small fraction going into the conduction band. Mobility increases with the gate voltage as the Fermi level moves closer to the conduction band [26]. The Fermi level can be driven up into the tail states, and possibly reach the conduction band, however it is highly unlikely because such a high gate voltage will probably cause dielectric breakdown before reaching the conduction band. These regions of TFT operation are show in Figure 2-4 [20] [27].

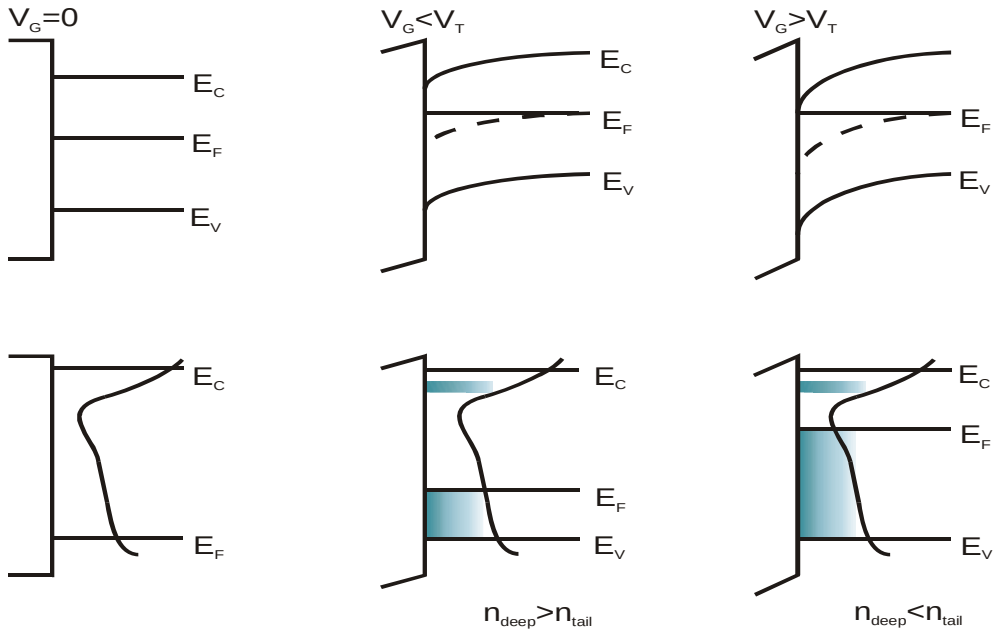

Figure 2-4. Regions of operation and corresponding positions of E_F in a TFT (adapted from [20] [27]).

2.1.4 Device Operation: Dynamic Characteristics

In an active pixel imaging array, a-Si:H TFTs are used both as a switch and as an analog amplifying device. Hence, its dynamic behavior is important from a circuit design's point of view. When a TFT is switched on, electrons are transported from the source/drain contacts to the a-Si:H/nitride interface. Some of these induced electrons start to occupy the deep states, giving rise to a transient current between the gate and source/drain due to the overlap capacitances. This transient current lasts about 1 μs for a 10 μm channel-length device [20]. After this period, the total charge in the channel remains constant, yet the drain-to-source current continues to decay for up to 1 s due to thermalization of charge into the deep states [28]. During the period after the switch is turned on, the charge density is low in the a-Si:H film region away from the interface, and thus a charge redistribution takes place. This leads to decay in drain-to-source current, which takes place in a time scale between 1 μs and 10 s and can be described as an effective dynamic threshold voltage shift. A similar phenomenon takes place while switching off the TFT [20]. This effect may be significant enough to cause noticeable variations in the output current of an amplifying TFT that is operating at high frequency.

2.2 TFT Terminal Behaviour

For the remainder of this thesis, a set of drain-source current equations similar to MOFETs are used for a-Si:H TFTs. The simplistic model provides adequate accuracy and is sufficient for design purposes. More accurate results can be obtained from circuit simulations and parameter extractions from measurements that are described in Appendix C. For a-Si:H TFT in linear regime,

$$I_{DS,lin} = \mu_{EFF} C_G \frac{W}{L}\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{1}{2}V_{DS}^2 \right] \tag{2.1}$$

where μ_{EFF} is the field effect mobility, C_G the gate oxide capacitance per unit area, $\frac{W}{L}$ the ratio between TFT channel width and length, V_T the threshold voltage, and V_{GS} ,V_{DS} the TFT gate-source and drain-source bias respectively.

Similarly, a-Si:H TFT drain-source current in the saturation regime can be defined as

$$I_{DS,sat} = \frac{1}{2}\mu_{EFF} C_G \frac{W}{L}\left(V_{GS} - V_T\right)^2 . \tag{2.2}$$

Parameter exaction methods outlined in the Appendix Appendix C can be used to extract accurate values of various variables used in these simple MOSFETs like models to improve the model accuracy. The current equations outlined in the appendix are used in modeling tasks in the pixel performance (Chapter 3) and noise analysis (Chapter 4). Measurement results have shown reasonable agreement with theoretical models, thus confirming the validity of the current equations.

3 Pixel Architectures

Pixel circuit design is the building block of any large area imaging array, and it strongly influences the overall functionality and performance of the panel. This chapter explains different pixel circuit designs in order to capture the progress and advancement in this area. The pixel circuit's sequence of operation, gain linearity, readout rate, and advantages and disadvantages are presented.

The chapter will start with the current state-of-the-art design, the passive pixel circuit (PPS), and outlines its strengths and weaknesses. Then, a few flavors of active pixel sensor (APS) circuit designs are introduced that addresses some disadvantages of the PPS that are essential overcome for particular medical imaging applications.

This chapter based the analysis on a-Si:H technology and TFT operations, and are introduced in the background chapter. A more throughout description of a-Si:H TFT can be found in the Appendix with highlights on detail device model derivation and parameter extraction from measurements.

3.1 Passive Pixel Sensor

The current state-of-the-art pixel design for digital radiography is the passive pixel sensor architecture. The pixel design was first introduced by G. Weckler in 1967 [33] where the integrated charge in a photodiode is readout by measuring the voltage (V) across a load resistor (R) required to reset the pixel via a switch S. One of the

disadvantages of this original readout technique is the time required to fully reset the diode through the resistor. This issue is especially pronounced in large arrays. A frame rate requirement may constrain the duration of the reset pulse, thus leading to incomplete reset which reduces the dynamic range of the sensor.

For diagnostic medical imaging applications, the array is typically large (~ 1000 X 1000 pixels for radiography) and the aforementioned disadvantage has to be considered. An alternative approach is to supply and measure the reset charge using a charge amplifier as proposed by Noble [34]. Here, there will be one charge amplifier per column data bus and the implementation of the PPS in a-Si:H technology is shown in Figure 3-2.

As shown in Figure 3-2, a PPS consists of a TFT acting as an electronic switch, and a photo-sensing element. The photo-sensing element can be a photoconductor such as a-Se or an a-Si:H photodiode in the integration mode such as a reversed biased n-i-p photodiode. The data line is common to an entire, and is connected to a column charge amplifier. The input of the charge amplifier is assumed to be virtual ground, which supplies current to recharge the photodiode in the addressed pixel. Such recharge action simultaneously perform a readout where the pixel accumulated charge is then stored in the amplifier feedback capacitor C_{FB}. A corresponding voltage output V_{OUT} can be then be measured.

In a common PPS array architecture, all the TFT gates in a row are connected together and scanning clock generator addresses all the rows in a sequential fashion. A row of TFT switches is activated during readout through the common gate line and the

signal charge from each pixel are readout at the same time via their respective data lines to the charge amplifiers. The output voltages from the amplifiers can then be sent to correlated double sampling (CDS) stages followed by digitization using analog-to-digital converters.

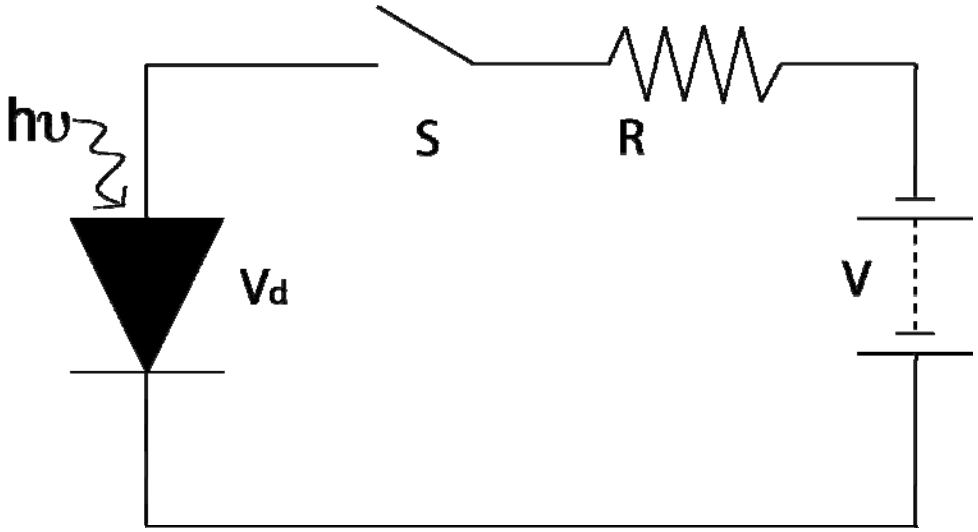

Figure 3-1: Original passive pixel sensor architecture by Weckler [33].

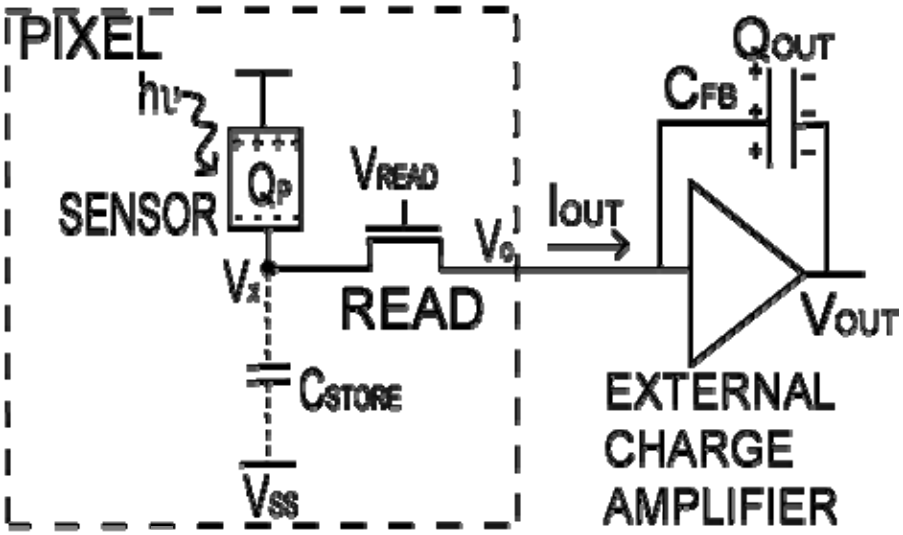

Figure 3-2: Passive pixel sensor architecture [33] [34].

3.1.1 Operation

The sequence of operation for the PPS begins when the READ TFT is turned off. Signal charge integrates at the sensor, inducing a voltage change at V_X that is proportional to the amount of incident radiation. It is noted that the magnitude of the induced voltage change at node V_X is a function of total pixel capacitance ($C_{PIX} = C_{SENSOR} + C_{parasitic}$), such that $\Delta V_X = \frac{Q_P}{C_{PIX}}$. The duration for which the READ TFT is off is the integration period, where signal accumulates at the pixel level.

Following signal integration, the READ TFT is pulsed on, allowing the signal charge to transfer from the pixel to the column charge amplifier through the common data bus. The photodiode or pixel capacitance is reset (or recharged) while signal is readout. The total pixel capacitance, C_{PIX}, is recharged to a steady state potential that is determined by the charge amplifier positive input terminal. After the reset is completed, the READ TFT is pulsed off again for the next integration period.

During the initial period of readout, the drain-source voltage across the READ TFT equals to the induced voltage at the pixel (ΔV_X). As the signal charge transfers from the pixel to the column amplifier feedback capacitor, the drain-source voltage decreases. Combined with the fact that ΔV_X is typically no more than a few hundred milli-volts, the READ TFT is mostly biased in the linear regime, providing a low ON resistance for quick readout. During the integration period, the READ TFT is pulsed off. Drain-source leakage current reduces the charge stored in the pixel, consequently limiting the lowest detectable signal of the pixel design. Leakage current of a-Si:H TFTs typically is of the

order of fA per μm width. On the other hand, as TFT channel width increases, drain-source ON resistance decreases. It is therefore one of the key design parameters to achieve sufficient readout rate while minimizing leakage current through careful TFT dimension and off voltage optimization.

3.1.2 Signal Gain and Linearity

The PPS design originally proposed by G. Weckler [1] (see Figure 3-1) measures the voltage of the pixel through the in-pixel resistance. In addition to the readout rate concern, this voltage sensing mechanism also suffers from low charge transfer efficiency. During readout, the signal charge is divided between the data line capacitance (C_{DL}) and the total pixel capacitance (C_{PIX}). The charge transferred to the data line represents the voltage appearing at the output terminal, and is

$$Q_{DL} = Q_P \frac{C_{DL}}{C_{DL} + C_{PIX}}. \tag{3.1}$$

where Q_P is the signal charge. It is evident that, for efficient charge transfer, C_{DL} has to be significantly larger than C_{PIX}. However, a large C_{DL} will reduce the magnitude of the output voltage, hence sacrificing voltage dynamic range. It is for this reason, voltage sensing is not recommended, and a signal integrator configuration (see Figure 3-2) should be used.

For an integrator configuration, the positive terminal of the charge amplifier acts as a virtual ground, so signal charge will be transferred entirely to the amplifier feedback capacitor (C_{FB}). The output voltage is obtained directly as

$$V_{OUT} = \frac{Q_P}{C_{FB}}. \tag{3.2}$$

Since the READ TFT simply acts as an electronic switch, the pixel circuit does not provide any signal gain. Here, if C_{FB} is the same as C_{PIX}, the output voltage (V_{OUT}) will be identical to V_X. It is possible to obtain a voltage gain by reducing the charge amplifier feedback capacitance; however, doing so will lead to an increase in reset noise$\left(\left\langle v_n^2 \right\rangle = \frac{kT}{C_{FB}} \right)$. From equation (3.2) and the pixel diagram (see Figure 3-2), the PPS design does not introduce any signal non-linearity to the signal output, so the output is linear as long as the sensing element response to incident light is linear.

3.1.3 Readout Rate

The readout rate of the imaging array is largely influenced by the pixel design, processing technology, device architecture (layout dependent), and configuration of readout electronics. For instance, crossover capacitances contribute significantly to the capacitive loading at the column data bus which affects the transient behavior of signal propagation. Such system analysis is complex and is included in the pixel integration chapter of this thesis. This chapter focuses on the pixel circuits and their influences to various pixel performance parameters, for more detailed readout rate analysis, the readers are referred to the pixel integration chapter.

During the readout period, the TFT is pulsed on allowing the pixel charge to transfer to the amplifier feedback capacitance. The pixel capacitance discharges exponentially at a rate that is governed by the time constant τ_{ON} given by,

$$\tau_{ON} = R_{ON} C_{PIX}\,, \tag{3.3}$$

where R_{ON} is the ON resistance of the READ TFT. For a small drain-source voltage, R_{ON} can be approximated by,

$$R_{ON} = \left[\frac{W}{L} \mu_{EFF} C_G \left(V_{ON} - V_T \right) \right]^{-1}, \tag{3.4}$$

where μ_{EFF} is the effective mobility, V_{ON} the TFT ON voltage, V_T the TFT threshold voltage, and C_G the gate insulator capacitance per unit area. For the PPS design, where the TFT dimension should be optimized for leakage current, and ON resistance. As an example, a TFT with $\left(\frac{W}{L} \right)_{READ} = \left(\frac{60}{23} \right)$, $\mu_{EFF} = 0.8 \text{ cm}^2 / V \cdot s$, $V_{ON} = 12 \text{ V}$, $V_T = 2 \text{ V}$, and $C_G = 25 \text{ nF/cm}^2$ gives $R_{ON} \sim 1.5 \text{ M}\Omega$.

The total pixel capacitance varies depending on the detection scheme. For direct detection, where an explicit capacitance has to be present for charge storage, the total pixel capacitance is dominated by the in-pixel capacitor. An in-pixel explicit capacitor with 100x100 μm^2 area, is approximately 2.5 pF using a parallel plate estimation. This results in a time constant of 3.75 μs. On the other hand, the total pixel capacitance will be dominated by the photodiode for an indirect detection scheme. Assuming the same 100x100 μm^2 area for the n-i-p diode, with $\varepsilon_o = 8.85 \times 10^{-12}$ F/m , , $\varepsilon_{a-Si:H} = 11$, and $d_{a-Si:H} = 0.5\ \mu\text{m}$, gives

$$C_{PD} = \frac{\varepsilon_o \varepsilon_{a-Si:H} A}{d_{a-Si:H}} \sim 1.95 \text{ pF}, \tag{3.5}$$

which results in a time constant 2.93 μs.

For complete charge readout, 3 to 5 time constants duration is typically needed to achieve 95% to 99.3% charge transfer efficiency. The estimated results for a 1000x1000 imaging array for both direct and indirect detection scheme are listed in Table 3-1.

Table 3-1: Readout rate comparison for PPS.

	Direct detection	**Indirect detection**
τ_{ON}	3.75 μs	2.93 μs
$5\tau_{ON}$	18.8 μs	14.6 μs
Frame rate for 1000x1000 pixel array	53 frames/second	68 frames/second

3.1.4 Measurements

The PPS design was fabricated using the in-house fabrication facility and a micrograph screenshot is shown in Figure 3-3. Three sets of 4x4 pixel arrays were fabricated with different in-pixel capacitors to verify the signal linearity. The in-pixel capacitance was measured and the column charge amplifier's feedback capacitance matched to provide unity gain. The measurement results are show in Figure 3-4. The slopes of the V_{OUT}-Q_P curves represent the capacitance and hence there is no inherent pixel gain. Measurement results agree reasonably well with theoretical predictions.

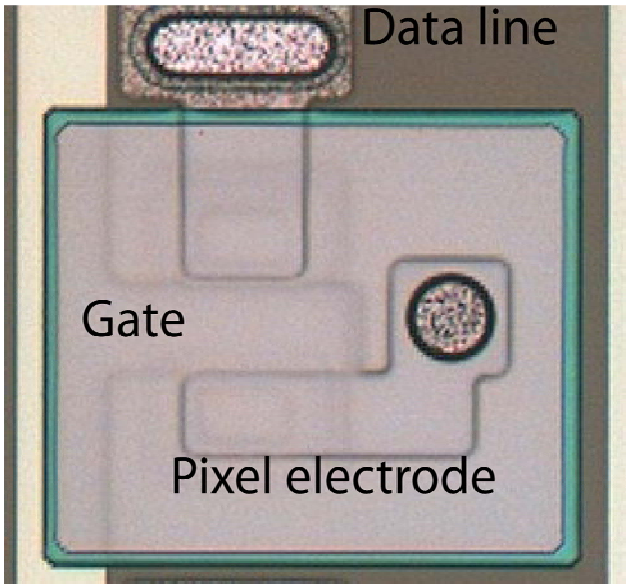

Figure 3-3: Micrograph of in-house fabricated PPS.

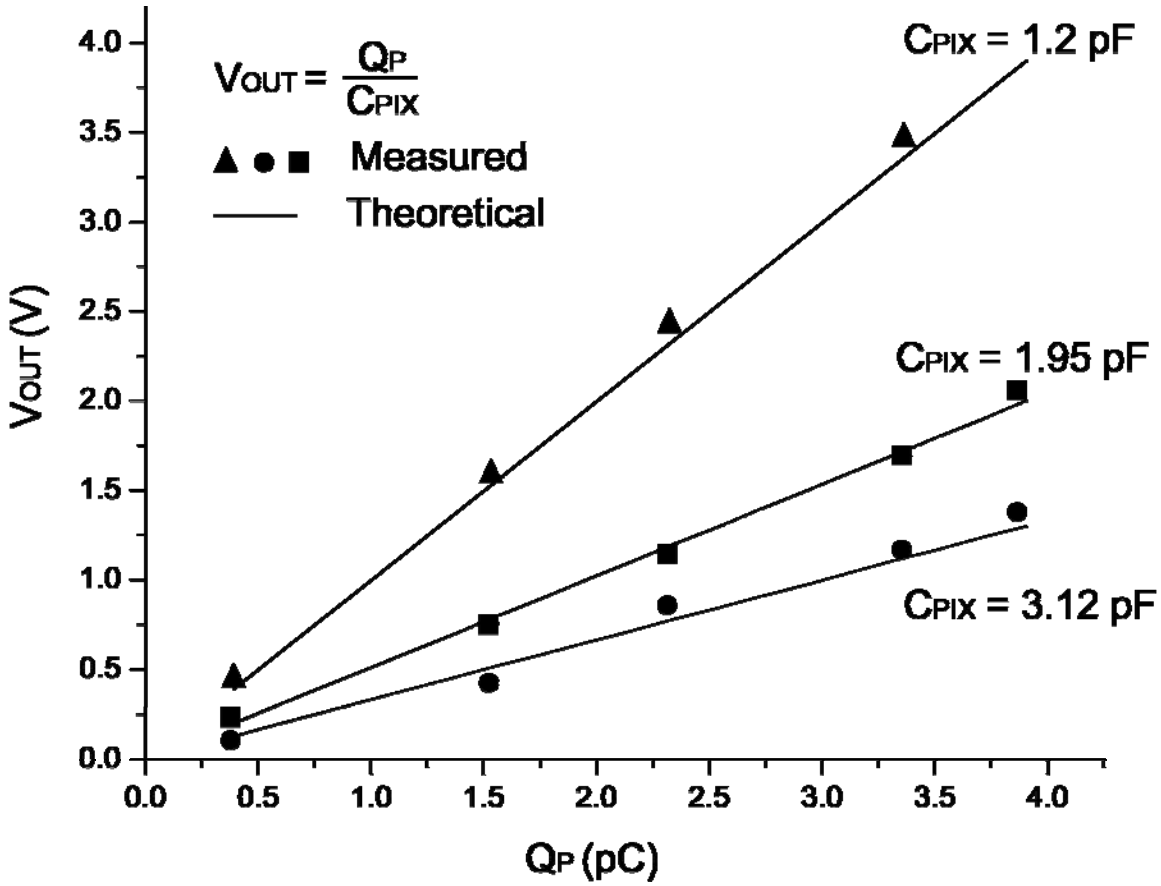

Figure 3-4: Signal linearity for in-house fabricated PPS.

3.1.5 Discussion

The PPS is undoubtedly the work horse for large area digital imaging. The main advantages are related to the simplicity of the design. Each pixel consists of only one TFT and requires two routing access lines. For co-planar architecture, where the TFT and photodiode compete for pixel area, a smaller transistor count allows the pixel geometric fill factor to be maximized. This enables better utilization of incident signal, in turn maintaining high system quantum efficiency.

In addition, the PPS enables smaller pixel pitch for a given technology. It potentially allows high resolution array to be fabricated. The smaller TFT count and fewer address lines enable high yield to be achieved, which translates into lower overall manufacturing cost.

On the other hand, the lack of pixel gain as described in earlier section prevents the PPS to be adopted for low dosage imaging applications such as fluoroscopy. The voltage gain of the system primarily relies on column charge amplifier. Hence any mismatch between amplifiers will contribute to array fixed pattern noise (FPN). Fortunately, such FPN can be alleviated via off-panel calibration. Also, the signal readout mechanism of the PPS relies on charge transfer between the pixel and feedback capacitors. The speed of charge transfer is affected by the TFT dimension, and the tradeoff between leakage current and on resistance set up a bottle neck in highest achievable frame rate.

In summary, despite the various advantages of the PPS design, its application is limited to arrays that are small (under 1500x1500) and requires only slow readout.

3.2 Active Pixel Sensor

In view of the shortcomings of the PPS, a more advanced pixel circuit design is developed to circumvent some of the hurdles in applying a-Si:H technology to large area imaging array applications. A logical extension of pixel design is to include more TFTs in a pixel to provide more inherent pixel gain and possibly increase the readout rate.

Noble [34] introduces an active pixel sensor (APS) design that he considered to be superior to the PPS for crystalline silicon technology. Shortly after that, a more extensive study was performed by Chamberlain for a similar pixel circuit [35]. The active pixel sensor design can be implemented in a-Si:H technology and the schematic is shown in Figure 3-5.

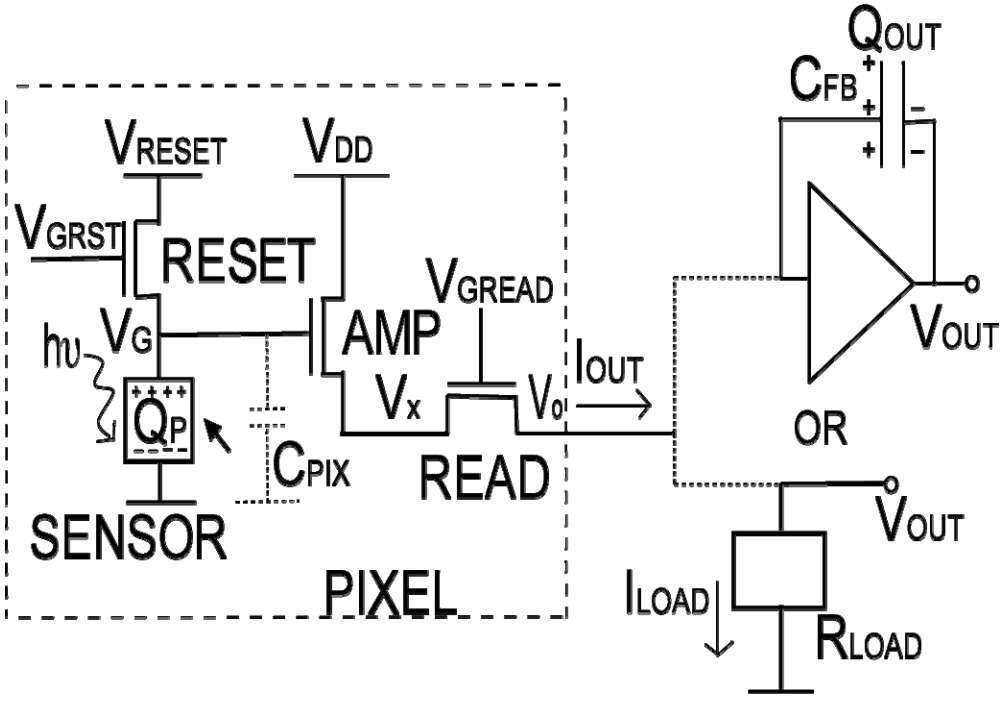

Figure 3-5: Active pixel sensor architecture

The APS circuit consists of three TFTs, namely the RESET, AMP, and READ TFTs. The sensor is connected to the gate of the AMP TFT, and a corresponding voltage will appear at node V_G upon charge collection. Signal charge is stored either in the photodiode or the in-pixel capacitor (shown in dotted line) for direct detection scheme. A small signal voltage swing (ΔV_G) will be amplified by the source follower composite circuit (AMP and READ) TFT, supplying an output current (I_{OUT}) down the common column data line. The RESET TFT is used to drain the accumulated charge during signal collection to prepare the pixel for the next integration frame.

3.2.1 Voltage Mediated APS

The APS design's output can be readout in two ways: voltage or current, as shown in Figure 3-5. APS voltage readout is conceptually a very attractive configuration due to its popularity in the crystalline silicon CMOS imager arena [36]. In this readout configuration, an active or resistive load is placed at each column to convert the pixel output current to a voltage output. With a high impedance column load, a stable voltage can be formed without charge amplifier, allowing easy signal manipulation. For crystalline silicon CMOS imagers, this configuration enables the integration of off-chip components such as analog-to-digital converters and correlated double sampling (CDS) with the array itself, i.e. single chip cameras.

While this concept potentially offers low noise readout, high level of integration, and low cost, its realization by a-Si:H technology is difficult. The challenge here is to provide a reliable on-chip column load. It is a common practice in CMOS imaging to have a transistor operating in saturation regime to act as an active load for the column

data line. The large output resistance of an active load provides good signal linearity and allows fast current sinking for high frame rate readout. Also, because the transistor is in saturation regime, it is relatively insensitive to drain-source voltage fluctuations making it a promising voltage loading element. However, such a load transistor requires a constant large gate bias to ensure output voltage immunity. To implement the same configuration with a-Si:H TFT will result in large threshold voltage shift due to inherent material metastability. The threshold voltage can change up to a few volts in the duration of hundreds of minutes, rendering the load unusable. On the contrary, physical resistors using n^+ a-Si:H or a-Si:H film provides much better stability [37][38]. However, a large load resistance is required for signal linearity; hence its realization will consume a considerable amount of real estate.

A second challenge to APS voltage readout is achieving fast readout rate. A detailed analysis for rise and fall times for APS with voltage readout is performed by Karim in 2002 [38]. For output rise time, both resistive and active load require a high pixel output current (I_{OUT}). Maximizing the AMP TFT can provide a current that is larger than the load can sink, thus most of the output current will charge up data line capacitances leading to a fast rise time. However, increasing the AMP TFT aspect ratio is accompanied by a larger pixel size, and most importantly, gate capacitance as seen from the integration node V_G. This consequently results in higher noise and it is discussed in the Chapter 4.

For obtaining fast fall times, the key challenge is to maintain a high output resistance while allowing a sizable current to flow through the load. Active load operating in the saturation regime performs very well in this case [38]. It is able to

maintain a unity voltage gain while allowing fast output discharge. However, resistive loads do not benefit from the output voltage insensitivity of an active load. The rise time scales linearity with output resistance. In other words, the output resistance has to be reduced to maintain a fast fall time, which sacrifices output dynamic range.

Considering all the above reasons, voltage readout for APS has limited applications for large area digital imaging. Despite its benefits over PPS that no external charge amplifiers are required, the speed of readout operation (ms delay per row) does not impose a great improvement. Combining with metastability concerns, the realization of a reliable, high performance imaging array in a-Si:H technology becomes questionable. The same pixel configuration might be feasible for other large area technologies, such as micro/nano-crystalline silicon or low temperature polycrystalline. Those alternatives are well known of their higher material carrier mobility, allowing pixel circuits to achieve higher current drive with smaller pixel size. This not only reduces in-pixel parasitic capacitances for better noise performances, also increases the readout rate capability. Moreover, these alternative technologies offer higher material atomic structure that leads to better device long term stability. Performance of active load can potentially be made reasonably reliable for on-chip integration.

3.2.2 Current Mediated APS

The APS design can be readout in the charge (current) domain and the configuration is shown in top right section of Figure 3-5. The pixel circuit consists of three TFTs and is identical to the voltage readout configuration at the pixel level. The AMP TFT supplies a current (I_{OUT}), which carries the small signal current proportional to

the accumulated charge. Unlike voltage readout, this output current is integrated at the charge amplifier feedback capacitor, much like the case for PPS described in the previous section. The load resistance (active or resistive) is eliminated, so any load related long term instability is removed. Furthermore, the readout rate no longer depends on load resistance and is largely determined by TFT switching speed and gain requirements (as discussed in the following sections).

3.2.2.1 Operation

The sequence of operation for the APS in current mediated mode can be summarized in three sections: initialization, integration, and readout. A timing diagram for the operation is shown in Figure 3-6.

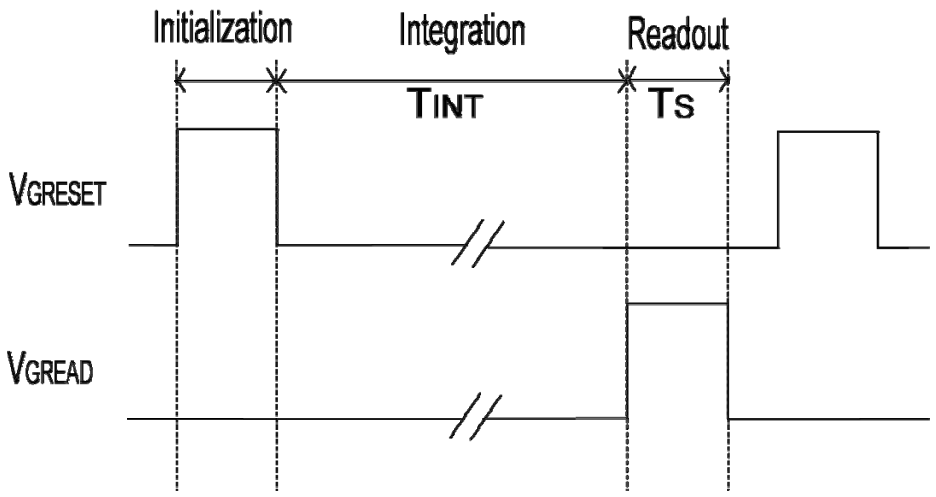

Figure 3-6: Timing diagram for APS.

Before any signal collection, the in-pixel photodiode or capacitor has to be initialized. Here, the RESET TFT is pulsed on, allowing the gate of the AMP TFT to charge up to the pre-determined value V_G. This effectively reverse biased the photodiode to a known state or charges C_{PIX} up to Q_P.

With the photosensitive element initialized, the RESET TFT is pulsed off and the integration period starts. Incident signal, $h\nu$, generates electron-hole pairs in the sensor and discharges the node V_G. The total accumulated charge ΔQ_P is generated at the end of the integration period and induces a small signal voltage swing ΔV_G at node V_G.

After the integration period (T_{INT}), the READ TFT is pulsed on and it connects the source of the AMP TFT to the input of the column charge amplifier via the data bus. The charge amplifier integrates the incoming current I_{OUT} for duration T_S. An output voltage is then developed and is proportional to both ΔV_G and T_S.

At the end of the readout period, the RESET TFT is pulsed high again and the operation continues to cycle through the three sequential steps mentioned for subsequent frames.

3.2.2.2 Signal Linearity

The signal linearity analysis for the APS circuit investigates how the output V_{OUT} varies with the accumulated charge at the sensor Q_P. It is customarily obtained from sensitivity analysis [39], and Karim further extend this analysis for APS [38].

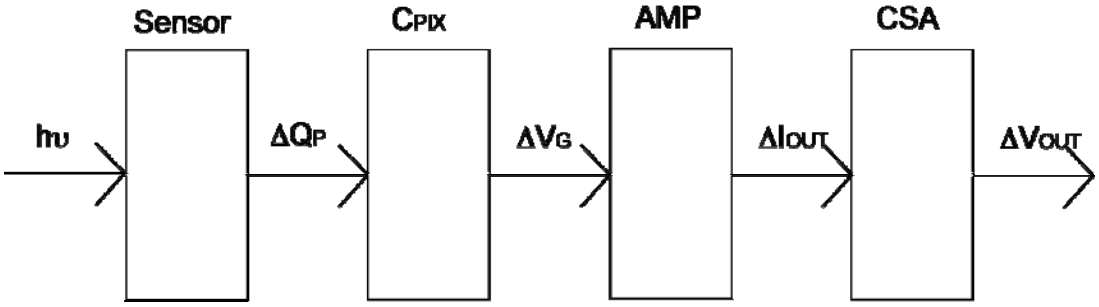

Figure 3-7: Block diagram for APS sensitivity analysis.

Figure 3-7 illustrates the sensitivity analysis pictorially. The first block corresponds to the sensor element's ability to accumulate a signal charge in respond to incident light. Typical photoconductors or photodiodes generate a linear charge (e-h pair) upon incident radiation, unless a multiplicative method is used to provide a non-linear signal gain (example, Avalanche photodiodes).

The second block refers to the ability of the sense node to convert the accumulated charge into small signal voltage change. For a photoconductor configuration, this corresponds to the in-pixel capacitance's ability (C_{PIX}) to stay constant with changing bias. Assuming the explicit capacitor dominating the C_{PIX}, this linearity is usually guaranteed. For photodiode configuration, C_{PIX} is dominated by the diode capacitance. The photodiode capacitance is insensitive to voltage across it within the reverse bias regime. It is advisable to carefully design the photodiode along with the APS circuit to ensure linear capacitance response.

The third block refers to the APS circuit's ability in producing a linear small signal current response to ΔV_G. Using a simple MOS like transistor current equation in the saturation regime gives us,

$$\begin{aligned} I_{OUT} + \Delta I_{OUT} &= \frac{\mu_{EFF} C_{OX} W}{2L} \left(V_{GS} + \Delta V_G - V_T \right)^2 \\ &= \frac{K}{2} \left(V_{GS} + \Delta V_G - V_T \right). \end{aligned} \tag{3.6}$$

Expanding the above equation and isolating dc and ac terms gives,

$$I_{OUT} + \Delta I_{OUT} = \frac{K}{2} (V_{GS} - V_T)^2 + K(V_{GS} - V_T)\Delta V_G + \frac{K}{2} \Delta V_G^2, \tag{3.7}$$

where the ac components can clearly be extracted from the equations. The ac current equation is given by,

$$\Delta I_{OUT} = K(V_{GS} - V_T)\Delta V_G + \frac{K}{2}\Delta V_G^2. \tag{3.8}$$

It is now evident that the second term should be minimized in order to obtain a linear ΔI_{OUT} with respect to ΔV_G. Hence the condition

$$\begin{aligned} &\frac{K}{2}\Delta V_G^2 \ll K(V_{GS} - V_T)\Delta V_G, \text{ and} \\ &\Delta V \ll 2(V_{GS} - V_T). \end{aligned} \tag{3.9}$$

The last block in Figure 3-7 refers to the charge amplifier (CSA) linearity with respect to input current I_{OUT}. The small signal voltage change ΔV_{OUT} is given by,

$$\Delta V_{OUT} = -\frac{1}{C_{FB}}\int_0^{T_S} \Delta I_{OUT} dt. \tag{3.10}$$

Assuming ΔI_{OUT} is constant during the readout period T_S, the linearity is ensured if the C_{FB} is constant. The feedback capacitance can be external or implemented as integrated capacitor, both of which can be easily made with a large range of linearity.

3.2.2.3 Signal Gain

During the integration period of APS operation, incident radiation creates signal charge in the pixel sensor. This signal charge is accumulated throughout the entire integration period (T_S), which in turn induces a small signal change ΔV_G at node V_G by the end of T_S. This small signal change as seen by the gate of the AMP TFT is amplified as the output current I_{OUT} given by,

$$I_{OUT} + \Delta I_{OUT} = \frac{\mu_{EFF} C_{OX} W}{2L} \left(V_{GS\_AMP} + \Delta V_{GS\_AMP} - V_T \right)^2, \tag{3.11}$$

where ΔI_{OUT} denotes the amplified signal charge integrated by the charge amplifier. In small signal analysis, this is analogous to,

$$\Delta I_{OUT} = g_{m\_APS} \cdot \Delta V_G, \tag{3.12}$$

where g_{m_APS} is the APS transconductance. For illustrative purposes, the source of the READ TFT can be assumed as a virtual ground as biased by the positive terminal of the column amplifier. So the APS transconductance becomes,

$$g_{m\_APS} = \frac{g_{m\_AMP}}{1 + g_{m\_APS} R_{DS\_READ}}, \tag{3.13}$$

where g_{m_AMP} is the AMP TFT transconductance and R_{DS_READ} is the drain-source on resistance of the READ TFT. Numerical values for the transconductance and ON resistance can be obtained from the TFT operating point, which is a function of biasing voltages as well as TFT dimensions. Here, we utilize simple CMOS like equations to derive an expression for pixel g_m , more accurate results can be obtained via measurements and simulations using an in-house developed a-Si TFT model [38][40][41]. During readout, the AMP TFT is operating in saturation regime, while the READ TFT is in linear regime due to small drain-source voltage. Thus, the individual current equations are given by,

$$I_{AMP} = \frac{\mu_{EFF} C_{OX} W_{AMP}}{2L_{AMP}} \left(V_{GA} - V_X - V_{TA} \right)^2 = \frac{K_{AMP}}{2} \left(V_{GA} - V_X - V_{TA} \right)^2, \tag{3.14}$$

and

$$I_{READ} = \frac{\mu_{EFF} C_{OX} W_{READ}}{2L_{READ}} \left[2\left(V_{GRD} - V_{SRD} - V_{TA}\right)(V_X - V_{SRD}) - (V_X - V_{SRD})^2 \right] = \frac{K_{RD}}{2} \left[2\left(V_{GRD} - V_{SRD} - V_{TA}\right)(V_X - V_{SRD}) - (V_X - V_{SRD})^2 \right], \quad (3.15)$$

where μ_{EFF} is the carrier field effect mobility, C_{OX} the gate oxide capacitance per unit area, W TFT channel width, L the TFT channel length, V_G and V_S the gate and source nodal voltages (subscript also denote AMP or READ TFT), V_T the threshold voltage, V_x the drain nodal voltage of READ TFT, and $K = \frac{\mu_{EFF} C_{OX} W}{L}$ for simplification purposes.

With biasing conditions, the only unknown variable is V_X, equating the two current equations (3.14) and (3.15) gives a quadratic equation as follows,

$$I_{OUT} = I_{AMP} = I_{READ}, \quad (3.16)$$

and

$$\frac{K_{AMP}}{2}\left(V_{GA} - V_X - V_{TA}\right)^2 = \frac{K_{RD}}{2} \left[2\left(V_{GRD} - V_{SRD} - V_{TA}\right)(V_X - V_{SRD}) - (V_X - V_{SRD})^2 \right]. \quad (3.17)$$

Rearranging equation (3.17) by collecting like terms gives,

$$V_X^2 \left(\frac{K_{AMP}}{2} + \frac{K_{READ}}{2} \right) + V_X \left[-K_{AMP}(V_{GA} - V_{TA}) - K_{RD}(V_{GRD} - V_{SRD} - V_{TRD}) - K_{RD} V_{SRD} \right] + \left[\frac{K_{AMP}}{2}(V_{GA} - V_{TA})^2 + K_{RD} V_{SRD}(V_{GRD} - V_{SRD} - V_{TRD}) + \frac{K_{READ}}{2} K_{SRD}^2 \right] = 0. \quad (3.18)$$

Equation (3.18) can be solved by the quadratic equation and obtaining the correct roots. The value of V_X allows the calculations of output current I_{OUT} and g_{m_AMP}. Dividing drain-source voltage across READ TFT by I_{OUT} gives us R_{DS_READ}.

Table 3-2: APS circuit parameters.

$(W/L)_{AMP} = 108/23$ $(W/L)_{READ} = 108/23$ $\mu_{EFF} = 0.8\ cm^2/V \cdot s$	**$V_{RESET} = 6$** **$V_{DD} = 15$**	**$V_{RESET} = 10$** **$V_{DD} = 15$**	**$V_{RESET} = 13$** **$V_{DD} = 15$**	**$V_{RESET} = 13$** **$V_{DD} = 12$**
V_X (V)	0.484	1.65	2.86	2.86
R_{DS_READ} (MΩ)	0.65	0.685	0.72	0.72
g_{m_AMP} (μS)	0.42	0.762	0.98	0.97
g_{m_APS} (μS)	0.33	0.5	0.57	0.57
I_{OUT} (μA)	0.74	2.42	3.97	3.97
I_{OUT} (μA) (measured)	0.69	2.33	3.65	3.80

Table 3-2 shows some of the APS parameters with different biasing conditions. The first three sets of experiments show a strong dependency of APS operating point on V_{RESET}. This is within expectation because the nodal reset voltage at V_X directly influences the gate-source voltage across the AMP TFT, thereby determining I_{OUT}. It is evident that the pixel transconductance (g_{m_APS}) is reduced due to voltage drop across the READ TFT. It is therefore advantageous to reduce R_{DS_READ}, by maximizing the width of

READ TFT within allowable limits. The measured I_{OUT} values demonstrate reasonable agreement with calculated results. The measured output current tend to be smaller than designed values, and is accredited to the additional voltage drop across bond pads and metal routing lines between the source of the READ TFT to the charge amplifier.

As explained earlier, the output current charges up the feedback capacitor at the column charge amplifier for duration T_S. The charge integrated at C_{FB} is thus a function of both g_{m_APS} and T_S. The charge gain as seen at the amplifier output is,

$$G_i = \frac{\Delta Q_{OUT}}{\Delta Q_P} = \frac{\Delta I_{OUT} \cdot T_S}{\Delta Q_P} = \frac{g_{m\_APS} T_S}{C_{PIX}}. \tag{3.19}$$

Using equation(3.19), we can alternatively find the voltage gain from the integration node to the output of the charge amplifier.

$$A_V = \frac{\Delta V_{OUT}}{\Delta V_G} = \frac{g_{m\_APS} T_S}{C_{FB}}. \tag{3.20}$$

From both equations (3.19) and (3.20), it is necessary to maximize $g_{m\_APS} T_S$ in order to achieve high voltage and charge gain. This can be done through pixel biasing adjustments, but larger increase can only be obtained through TFT scaling. A larger AMP TFT can provide more current drive that increases the gain. Also, this will increase total pixel capacitance due to larger transistor dimension. Meanwhile, the total pixel area must scale up to accommodate the increase in transistor size. It is therefore better to reduce pixel capacitance (C_{PIX}) to increase the charge gain. This method not only avoids imposing pixel size constraints, it also reduces the reset noise of the pixel. The drawback is the reduction of charge storage capacity at the integration node. For large area medical

imaging, the voltage signal magnitude typically ranges from a few hundred mV up to one volt, a pixel capacitance of approximately hundreds of fF will be sufficient. The next chapter will discuss APS noise performances, and it is shown that reset noise is a dominating noise contributor; hence the reduction of C_{PIX} is preferred.

. It is worthy of noting that a longer sampling time (T_S) at the charge amplifier will also have similar effect in boosting the charge gain. It is important, however, to design the pixel and charge amplifier to avoid output saturation. A charge amplifier with 15 V positive supply voltage and a 3 pF feedback capacitance, can hold an I_{OUT} of 1 μA for 45 μs.

3.2.2.4 Readout Rate

The APS design with current readout uses a charge amplifier to develop a voltage output. Such configuration is similar to the PPS design, is that the positive terminal of the amplifier provides a reference voltage to the entire data line. In APS, this reference voltage sets up the steady state conditions for the composite source follower (see Figure 3-5), which in turn governs the magnitude of output current. As shown in equation (3.19), the desired charge gain is programmable by varying T_S. The maximum readout rate has a tradeoff with required signal gain. From a theoretical standpoint, the maximum achievable readout rate is determined by the switching speed of the READ TFT, which is about a few μs in a-Si technology.

In practical imaging arrays, the parasitic capacitances of the data line and the TFT gate-source overlap contributes to a sizable data line capacitance C_{DL}. Figure 3-8 shows the column data line configuration. The output current from the pixel will flow in both

C_{DL} and C_F, and the current divides according to the impedances as seen from the input of the charge amplifier. The effective value of C_{FB} in parallel with C_{DL}, can be obtained from Miller's theorem, such that

$$C_{FB}^{'} = (1 + A)C_{FB}, \tag{3.21}$$

where A is the DC gain of the amplifier. Current divider yields the feedback capacitor current as

$$I_{FB} = I_{OUT} \frac{C_{FB}^{'}}{C_{FB}^{'} + C_{DL}}. \tag{3.22}$$

For example, a charge amplifier with a DC gain of 100 and C_{FB} of 3 pF yields 300 pF for $C_{FB}^{'}$. Assuming the dominat contribution to data line capacitance is the TFT gate-source overlap, C_{DL} will scale with the array size. For a 1000 x 1000 pixel array, 2 μm gate-source overlap, $(W/L)_{READ} = 108/23$, and $C_{dielectric} = 25$ nF/cm^2 yields

$$\begin{aligned} C_{DL} &= 1000 \times C_{\text{dielectric}} \times W_{\text{READ}} \times OL_{\text{READ}} \\ &\simeq 1000 \times 54\, fF \\ &\simeq 54\, pF. \end{aligned} \tag{3.23}$$

Using the numerical values from the above on equation (3.22) shows that I_{FB} is only ~90% of I_{OUT}, representing a significant loss of charge. Fortunately, the AMP TFT provides non-destructive readout and supplies a current drive as long as the READ TFT is pulsed ON. The loss of I_{OUT} only shows up as a delay in developing a corresponding V_{OUT} with acceptable sensitivity. Particular caution has to be placed in

design to accommodate this data line capacitance induced signal delay, so as to achieve adequate charge gain and avoid output saturation.

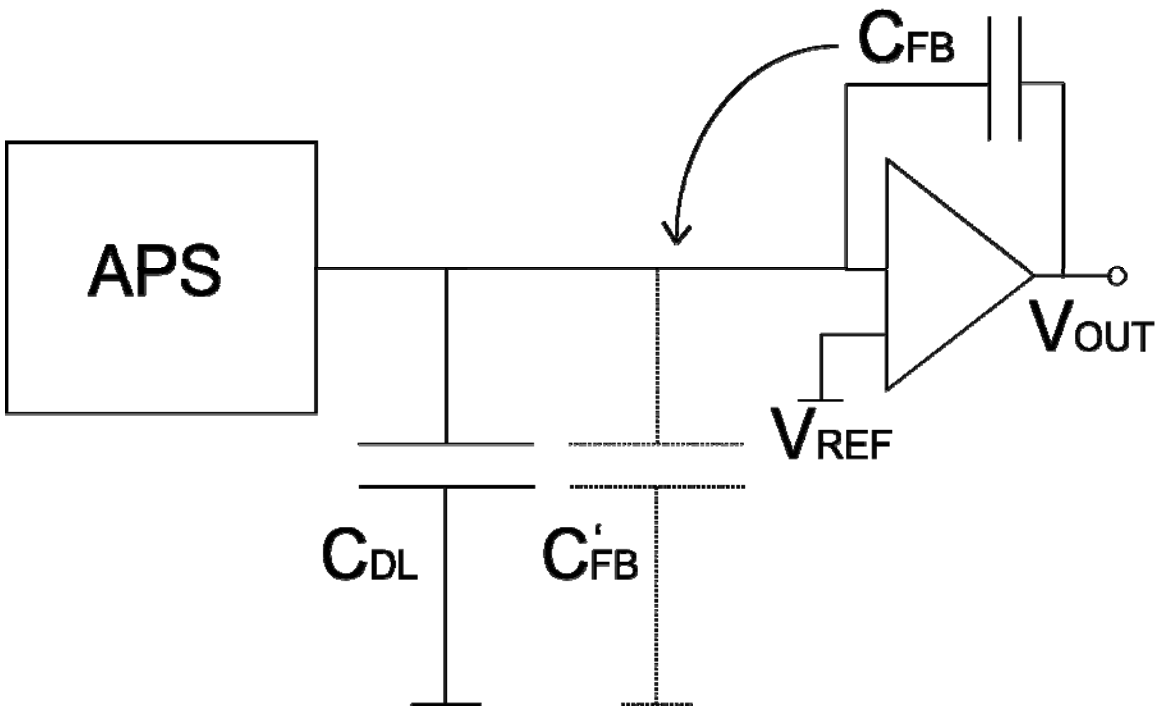

Figure 3-8: Charge amplifier feedback capacitance effect on readout rate.

3.2.2.5 Measurements

The APS design is made using an in-house fabrication facility. In particular, several 2x2 pixel arrays have been implemented with different in-pixel capacitance to provide verifications and insights into the analysis in this chapter. The fabrication details of each of the arrays are summarized in Table 3-3. Each array has four APS pixels and each of them consist of an explicit capacitor to increase the total in-pixel capacitance.

APS array # 4 has a bigger pixel pitch to accommodate the larger area usage to achieve C_{PIX} = 10 pF. For all four arrays, $\left(\frac{W}{L}\right)_{AMP} = \left(\frac{W}{L}\right)_{READ} = \frac{108}{23}$ and $\left(\frac{W}{L}\right)_{RESET} = \frac{60}{23}$.

Table 3-3: Details of the fabricated APS pixel arrays.

	Array 1	**Array 2**	**Array 3**	**Array 4**
Pixel pitch (μm^2)	350 x 300	350 x 300	350 x 300	400 x 400
C_{PIX} (pF) designed	1.5	3.5	5.5	10
C_{PIX} (pF) measured	1.67	3.42	5.17	10.8

The first stage of experiments is to determine the influence of V_{RESET} on voltage gain. As previously explained, V_{RESET} directly affects the gate-source biasing conditions for the AMP TFT, consequently the transconductance and voltage gain of the APS. Figure 3-9 plots ΔV_{OUT} against ΔV_G for three levels of V_{RESET}. Small signal linearity is demonstrated for all reset potential levels which agree within 11% of theoretically established values. In addition, it is demonstrated that a higher reset voltage gives a higher voltage gain as predicted by equation (3.20). It is noted that increasing V_{RESET} leads to an increase in I_{OUT}, hence increase the voltage across the READ TFT. V_X is increased as a result, serving as an inherent feedback system for limiting the benefits in V_{RESET} increase. This is verified by the smaller increase in A_V from V_{RESET} = 10 → 13V than V_{RESET} = 6 → 10V.

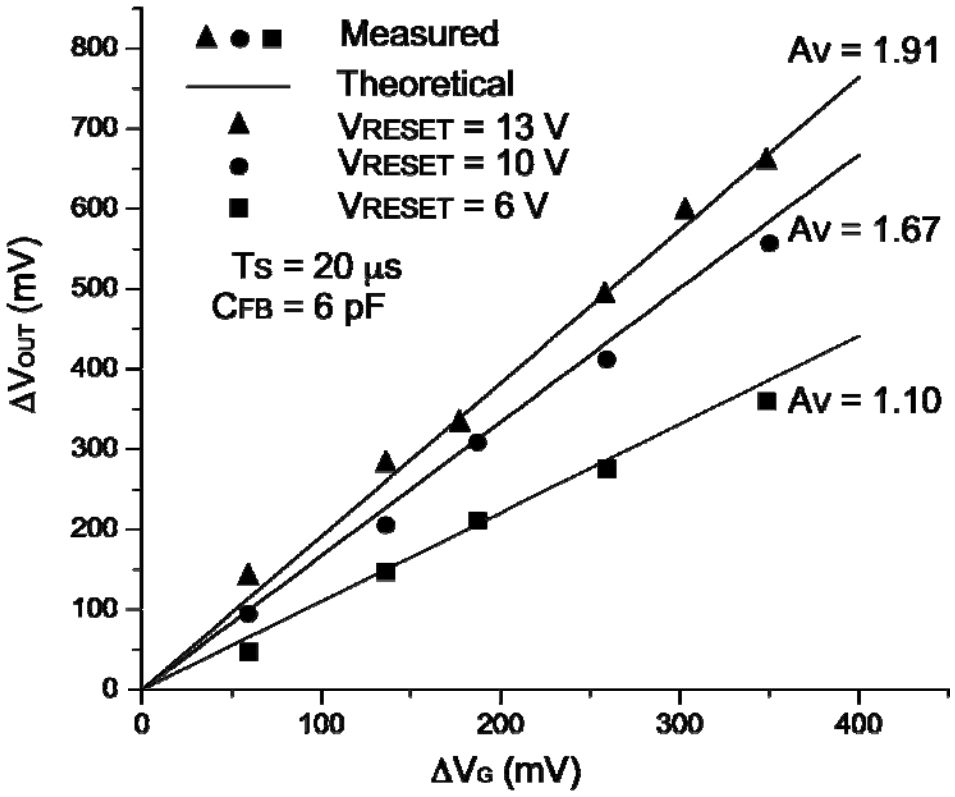

Figure 3-9: APS voltage gain variations with respect to V_{RESET}.

Figure 3-10 illustrates another important parameter that affects the voltage gain. The sampling time (T_S) is varied, in other words, the charge amplifier integrates for different durations. Recall that I_{OUT} and T_S have to be considered simultaneously to avoid output saturation, so V_{RESET} is set to 10 V to allow a wider range of T_S variations. From the experiments, A_V increases linearly with respect to T_S increase. Measurement results agree with theory to within ±13%.

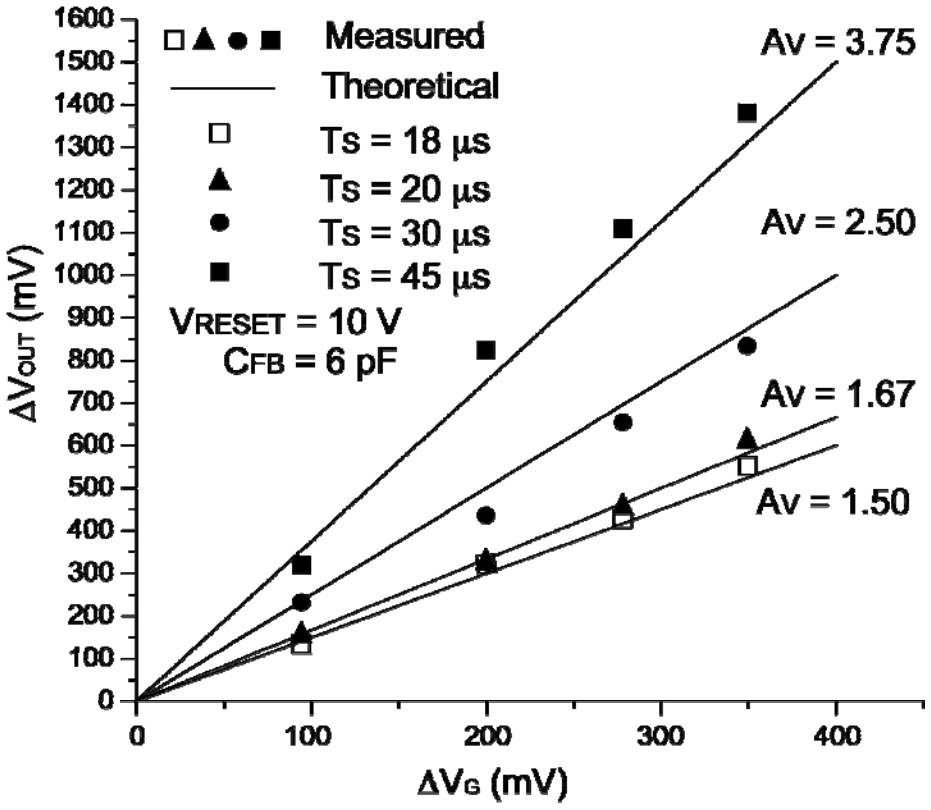

Figure 3-10: APS voltage gain variations with respect to T_S.

The voltage gain of APS is largely determined by sampling time, biasing conditions, as well as feedback capacitance C_{FB}. These parameters can be optimized to provide an appropriate gain. As demonstrated, the range of programmable gain is limited and rarely exceeds an order of magnitude. To further increase the gain, in-pixel capacitance C_{PIX} should be reduced. Figure 3-11 demonstrates the effect of C_{PIX} reduction. The charge gain (G_i) increases from 1.39 to 8.99 when C_{PIX} decreases from 10.9 pF to 1.67 pF. The increase in G_i scales proportionally with C_{PIX} reduction. It is noted that any further increase in C_{PIX} will result in the total capacitance dominated by AMP TFT gate capacitance. Under these conditions, C_{PIX} will be a function of V_G, thereby violating the sensitivity and linearity analysis in section 3.2.2.2. Moreover, in practical technology the approach of down scaling, TFT channel length is reduced,

resulting in higher AMP TFT aspect ratio. Thus, charge gain increase can be up to 20 times with these modifications to the design rules of the fabrication technology.

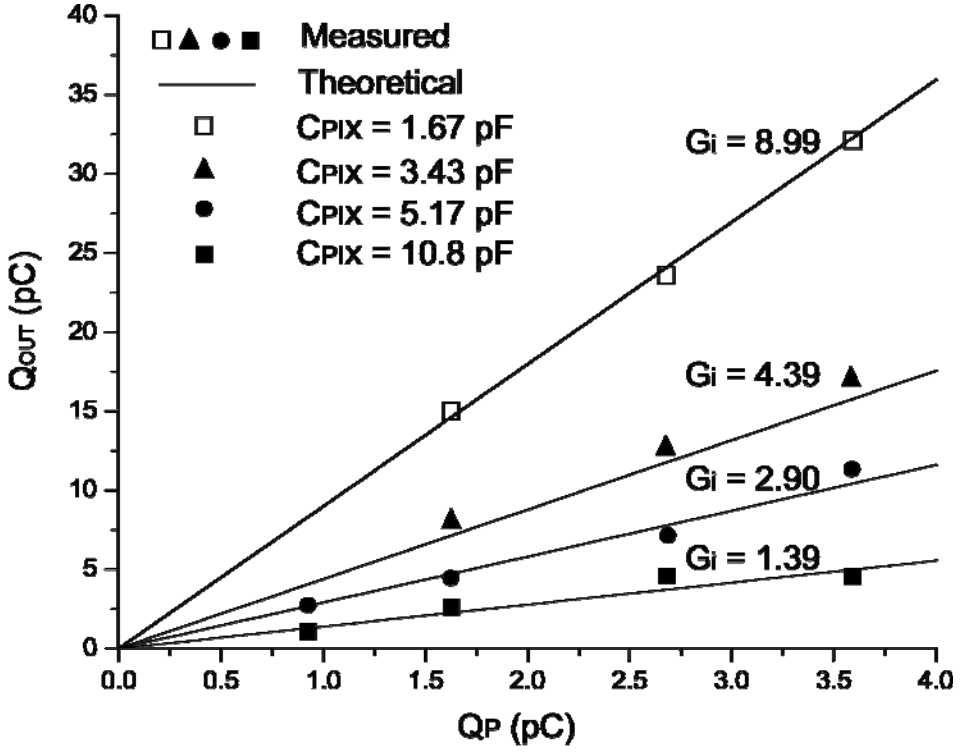

Figure 3-11: APS charge gain.

3.2.2.6 Discussion

The APS design with current readout undoubtedly provides definite improvements over PPS that will facilitate its use in medical x-ray imaging applications. Firstly, there is no load resistance so problem such as slow rise/fall times due to charging/discharging a load is eliminated. Secondly, pixel readout speed of 30 μs with a 2.5 voltage gain is demonstrated through prototyping. This allows a 30 ms frame time for a 1000x1000 imaging array, which proves suitable for digital fluoroscopy. Thirdly, the

circuit configuration allows programmable gain via biasing voltages, making system fine tuning possible without any hardware modification.

While the proposed APS design demonstrates, there are improvements yet to be desired. The dynamic range of the pixel is determined by the in-pixel total capacitance C_{PIX}, which imposes a tradeoff between signal linearity and gain. For a given C_{PIX}, an increase in accumulated charge induces a larger ΔV_G. Recall APS signal linearity holds only for $\Delta V_G \ll 2(V_{GS\_AMP} - V_{T\_AMP})$, hence limiting $\Delta V_G << 200$ mV. To increase the signal storage capacity, a larger C_{PIX} is required. However, this sacrifices charge gain and noise performance (as discussed in chapter 4). This tradeoff is due to the fact that signal charge storage and sensing (conversion from ΔQ_P to ΔV_G) are both performed at the same node V_G. As it will be discussed in further detail for the hybrid APS design, separating the signal storage and sensing functionalities into two separate nodes allows both higher dynamic range and increased signal gain.

From an application point of view, the tunable range of the APS rarely exceeds an order of magnitude. However, the mean exposure range from low dose fluoroscopy (1 μR) to radiography (300 μR/frame) exposure can span two and a half orders of magnitude (0.1 μR to 3000 μR). In addition, the input signal dosage can vary up to 100 times within 1 frame due to the un-attenuated incident radiation outside the edge of the patient body. It is evident that the dynamic and gain tunable gain range for APS is not as high as desirable.

3.3 Hybrid Active Pixel Sensor

3.3.1 Motivation

While the APS design demonstrates high speed readout and high gain, it is challenging to implement it for applications that require very high dynamic range. The requirement of a high dynamic range pixel comes from interest in a multi-modality imaging panel where the differing modalities have requirements for mean exposure differing by over 300 times. In addition, it is not usual to have input signal that varies more than 2 orders of magnitude within a same frame. It is hence of important to explore pixel architectures that offer the necessary dynamic range. Table 3-4 summarizes the APS and PPS gain performance for radiographic and fluoroscopic imaging.

Table 3-4: Gain performance of APS and PPS for radiography and fluoroscopy.

C_{PIX} = 1 pF C_{FB} = 1 pF	**APS**		**PPS**	
Imaging mode	Radiography	Fluoroscopy	Radiography	Fluoroscopy
Mean exposure (μR)	300	1	300	1
Input charge (C)	$6x10^{-13}$	$6x10^{-15}$	$6x10^{-13}$	$6x10^{-15}$
Integration time (μs)	10	33	10	33
ΔV (V)	0.6	$6x10^{-3}$	0.6	$6x10^{-3}$
ΔV_{OUT} (V)	3	0.1	0.6	$6x10^{-3}$

The APS design is capable of providing an output voltage swing of 0.1 V for fluoroscopy. Even though the relatively small signal swing imposes a stringent requirement on the external electronics, this configuration is feasible. However, the voltage swing is achieved by the small feedback capacitance (C_{FB} = 1 pF), and output charge amplifier saturation quickly becomes the limit to the readout rate. It is also noted that the APS generates a large 3 V swing for radiography, which can cause the external electronics to behave non-linearly. On the contrary, even though the lack of signal gain in PPS prevents its use for fluoroscopy, it is amenable to be used for radiography.

3.3.2 Image Mosaicing

Image mosaicing of images have been in practice since long before the age of digital computers and imaging [42]. Ever since its introduction in 1839, the technique was used as a photographic process for topographical mapping [43]. In recent years, image mosaicing with multiple exposures have been heavily used in CMOS image sensors [44][45]. It is particularly useful for applications when there is little to no exposure control in the environment (example: digital cameras in mobile phones), and accurate representation of both light and dark details are required (i.e., high dynamic range).

Medical diagnostic imagine shares vast similarities with the scenario mentioned above. Firstly, there is limited flexibility in increasing signal dosage due to safety regulations and equipment compatibility. Secondly, intensity values of radiograms can have a very wide dynamic range, and details of both extreme illuminated regions can be important for accurate diagnosis.

The idea of image mosaicing with multiple exposures is to capture images of the same scene at different levels of irradiation. For any imaging array, one may get a better representation of low light areas by increasing the exposure time, at the cost of losing information in areas of high illumination. Similarly, by using a reduced exposure time, one may sacrifice lowlight detail in exchange for improved details in area of high irradiation. If the dynamic range of the scene exceeds the imager's capability, then it is futile to adjust the exposure time, as detail will definitely be lost. However, off-chip image processing techniques can combine frames with different exposure levels to generate an image with levels of details beyond the dynamic range the imager can provide. The idea is illustrated pictorially in Figure 3-12. In this example, three images are taken at t_1, t_2, and t_3 that correspond to low, medium, and high irradiation of the same frame. The algorithms of image mosaicing are beyond the scope of this thesis, and readers are forwarded to references [44], [45], [46], [47], and [48] for full details. The following section presents two hybrid pixel circuits that can extend the use of PPS and APS for the purpose of achieving a wider dynamic range and high gain imaging array.

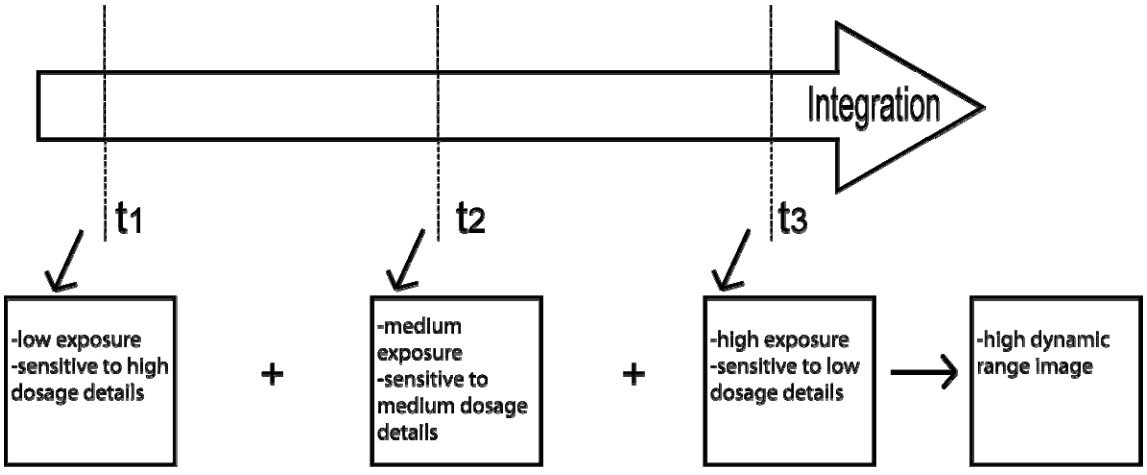

Figure 3-12: Image mosaicing with multiple exposures.

3.3.3 Hybrid APS with Dual Output

Figure 3-13 shows the schematic of a hybrid APS design with dual output. The pixel consists of four TFTs and can be read out through the two row select transistors, namely READ and READ_2 TFTs. The sensor, photoconductor or photodiode, form a 3-TFT APS with RESET, AMP, and READ TFTs, while simultaneously mimicing the PPS design with the READ_2 TFT. Accumulated charge at V_G amplified by AMP TFT can be readout via output bus 1, which is connected to a column charge amplifier with feedback capacitance C_{FB}. When READ_2 TFT is pulsed ON, signal charge Q_P will be transfered to the charge amplifier through output bus 2 with no inherent charge gain like the PPS configuration. The dual readout configuration is shown in Figure 3-14 where each pixel contains two output lines and corresponding charge amplifiers [50][51][52].

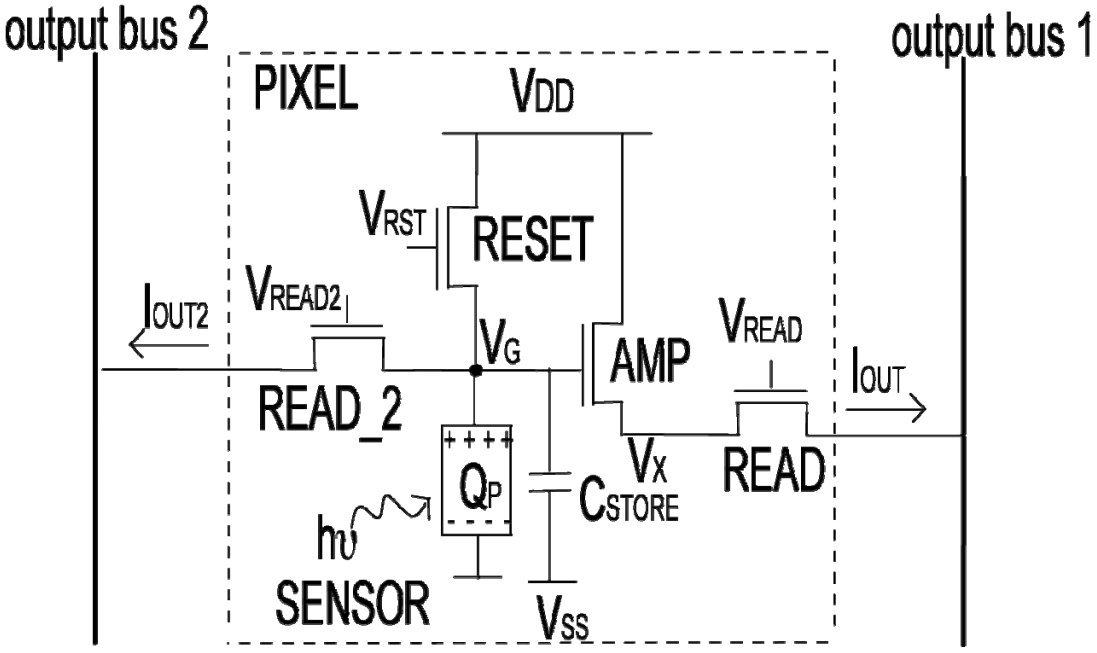

Figure 3-13: Hybrid APS with dual output.

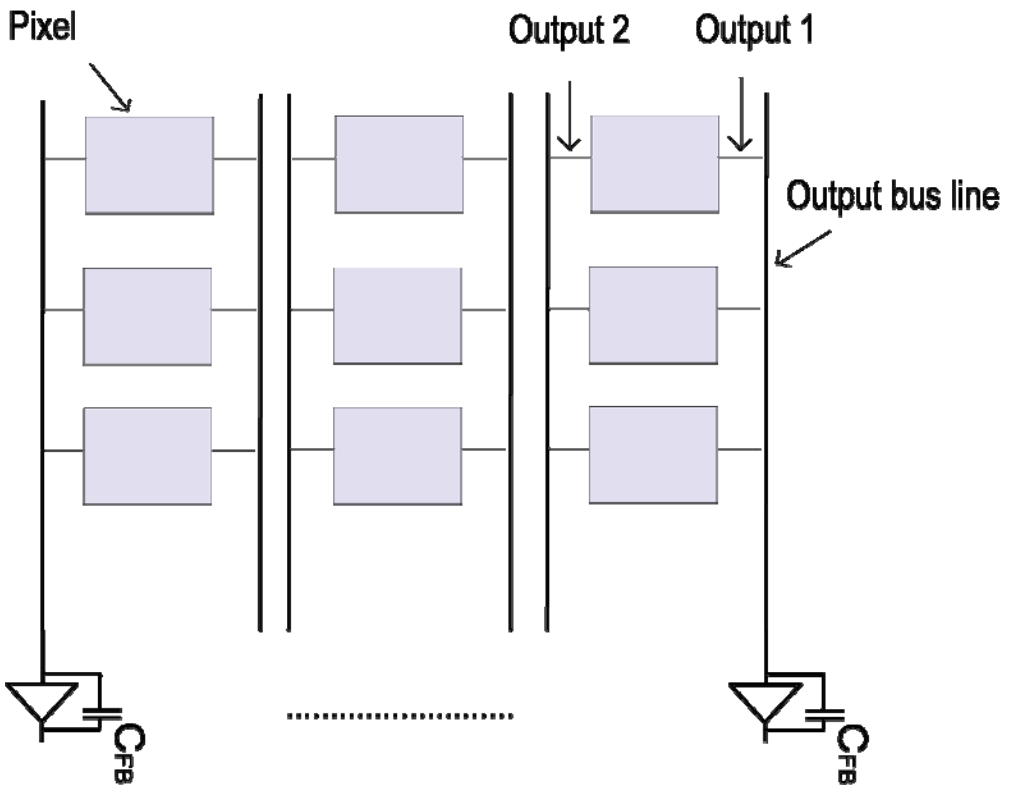

Figure 3-14: H-APS array with dual readout.

3.3.3.1 Operation

The sequence of operation for the proposed H-APS is shown in Figure 3-15 and Figure 3-16. Due to the high complexity and dual output buses, the readout operation can be configured in different modes. The initialization, and integration processes are identical to the APS, which a small signal voltage swing ΔV_G is developed at the end of the integration period T_{INT}. At this point, the readout schemes can be performed in two different ways, namely selective or sequential readout.

For selective readout, collected charge ΔQ_P is readout only in one of the two output paths (See Figure 3-15).

Amplified readout:

- When incident signal is small and amplification is required, it is readout through READ TFT. In such a case, the READ TFT is pulsed on after integration which allows the AMP current I_{OUT} to charge up the column amplifier. The duration of this charging process is termed T_{S1}, and a corresponding amplified signal is induced at the output of the charge amplifier. The RESET TFT is pulsed on again afterwards to prepare the pixel for the next image frame.

Un-amplified readout:

- When incident signal is large and amplification is not required, it is readout through the READ_2 TFT. READ_2 TFT is pulsed on and ΔQ_p is transferred to the feedback capacitor (C_{FB}) of the charge amplifier. Similar to the PPS, signal readout and reset are performed simultaneously after duration of T_{S2}.

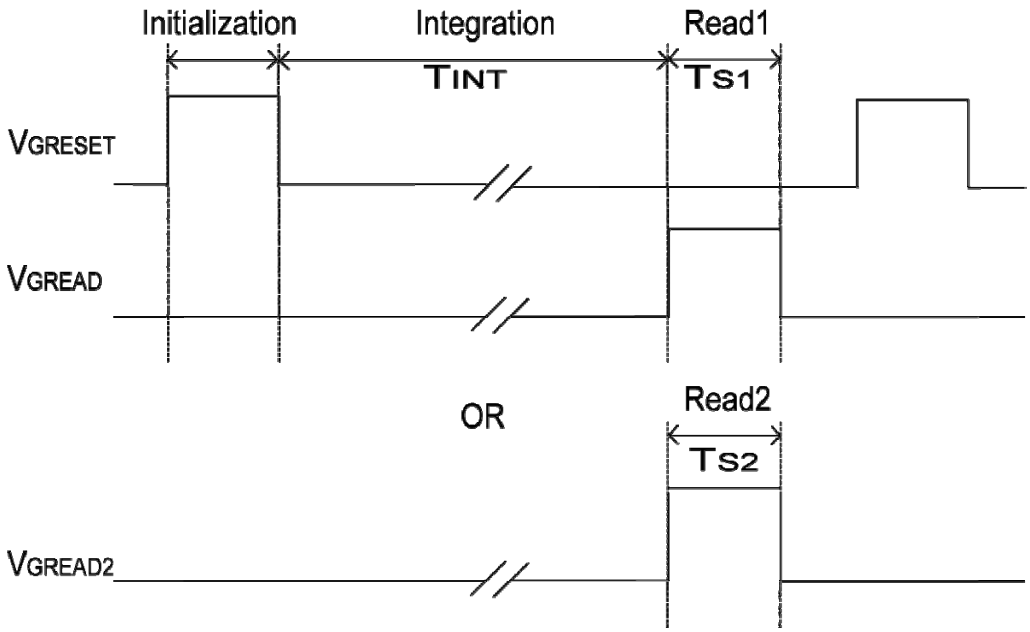

Figure 3-15: Timing diagram for selective readout scheme in H-APS with dual readout.

For sequential readout, the collected charge ΔQ_P is readout multiple times as shown in the timing diagram in Figure 3-16.Here, READ TFT is pulsed on and ΔQ_P is amplified and readout through output bus 1. READ TFT is then pulsed off, and READ_2 TFT is pulsed on for T_{S2}. This allows the transfer of signal charge to the column feedback capacitor C_{FB} without amplification. It is worthy of noting that READ_1 can be performed multiple times as long as RESET and READ_2 are not pulsed on. The AMP TFT provides a non-destructive readout, so image capture at multiple exposure levels is possible without interfering with signal integration. At the end of the integration period, reading out the signal through READ_2 provides a non-amplified frame, which can be used for calibration purposes, as well as pixel reset. Evidently, this sequential readout scheme provides the capability required for image mosaicing to widen the dynamic range as described in section 3.3.2.

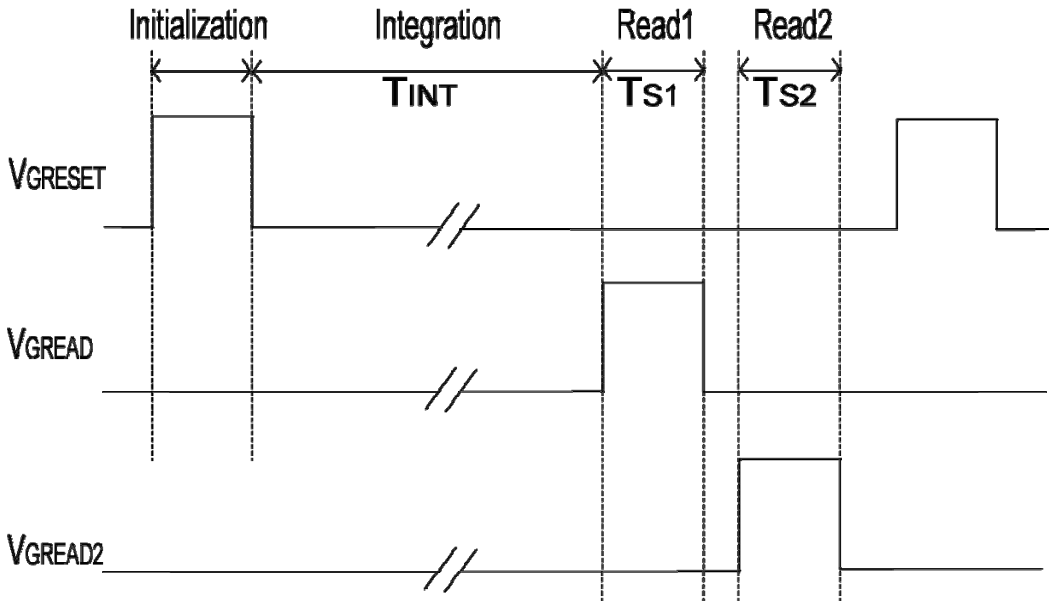

Figure 3-16: Timing diagram for sequential readout scheme in H-APS with dual readout.

3.3.3.2 Signal Gain and Linearity

The concept of this H-APS is to extend the use of previous pixel designs to accomplish higher performance. Thus, the signal gain and linearity analysis of H-APS is identical to those of PPS and APS.

Particular care has to be taken when designing H-APS to reach necessary performance criteria. The H-APS contains 4 TFTs in a single pixel and it adds to the total pixel capacitance unavoidably. Gate-source/drain overlap and AMP TFT gate capacitances have to be taken into consideration for total C_{PIX}, and is given by,

$$C_{PIX} = C_{STORE} + C_{g\_AMP} + C_{gs\_AMP} + C_{gd\_AMP} + C_{gs\_RST} + C_{gs\_READ2}, \qquad (3.24)$$

where the capacitances are shown in Figure 3-17.

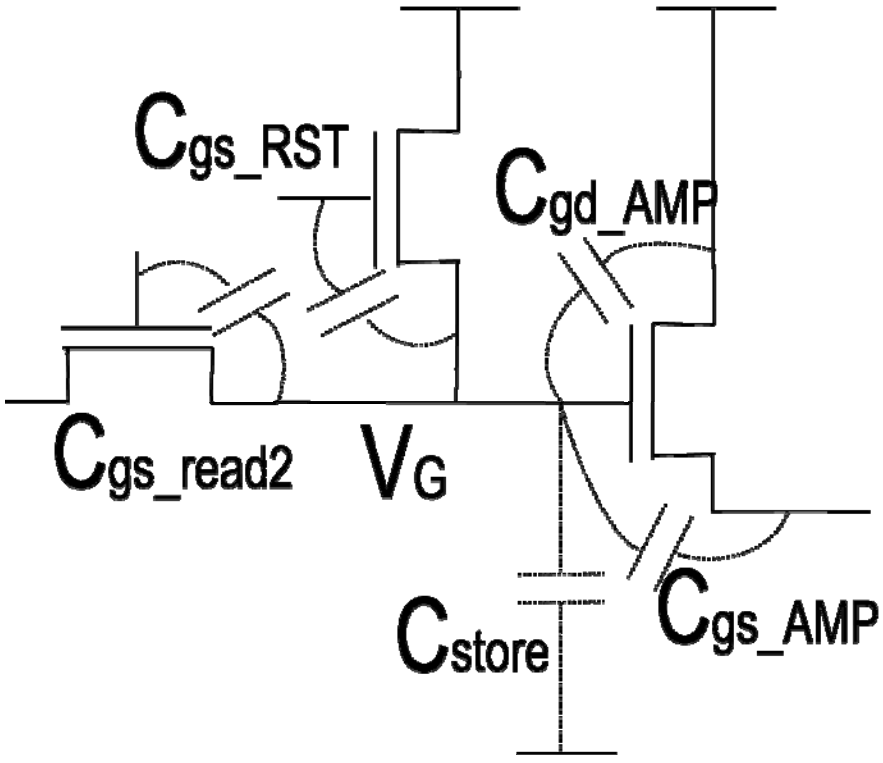

Figure 3-17: H-APS integration node capacitance.

Here, using the same TFT dimensions as the APS and PPS defined earlier, the total in-pixel capacitance for in-house fabricated prototype is 2.16 pF. In comparison to PPS, the extra parasitic capacitance from all the TFTs implies a higher C_{FB} is required. This imposes a bottleneck in small signal voltage swing at the output of the charge amplifier. For the amplified readout path, the extra parasitic capacitance from READ_2 TFT has minimal effect on signal gain. Thus, C_{PIX} should be minimized for higher signal gain.

For signal linearity, the PPS readout path does not require any specific design caution because the entire signal charge is transferred to the column amplifier. For APS readout path however, a reduction in C_{PIX} results in a smaller signal linearity range, i.e. $\Delta V_G \uparrow$ for $C_{PIX} \downarrow$ and $\Delta V \ll 2(V_{GS} - V_T)$. Hence, any drastic reduction in C_{PIX} can result in non-linear output response.

3.3.3.3 Readout Rate

The readout rate performance for H-APS is identical to those discussed for PPS (section 3.1.3) and APS (section 3.2.2.4) designs.

It is noted that the frame-rate for H-APS varies depending on which readout scheme is used. For selective readout, readout time for each row is $T_{S1} + T_{S2}$. For sequential readout, the frame rate scales according to how many read cycles are performed. For example, if READ TFT is pulsed on twice and READ_2 TFT pulsed on once, the time required for one row readout becomes $T_{S1} + T_{S1} + T_{S2} + 2\Delta t$, where Δt is the time delay between subsequent read pulses.

3.3.3.4 Measurements

The H-APS is fabricated using in-house facility, and the design parameters are listed in Table 3-5. The signal gain performance is summarized in Figure 3-18.

Table 3-5: Design parameters for H-APS.

$(W/L)_{AMP}$	$(W/L)_{READ}$	$(W/L)_{READ\_2}$	$(W/L)_{RESET}$	C_{PIX}	Pixel size
108/23	108/23	60/23	60/23	2.16 pF	$(380)^2$ μm^2

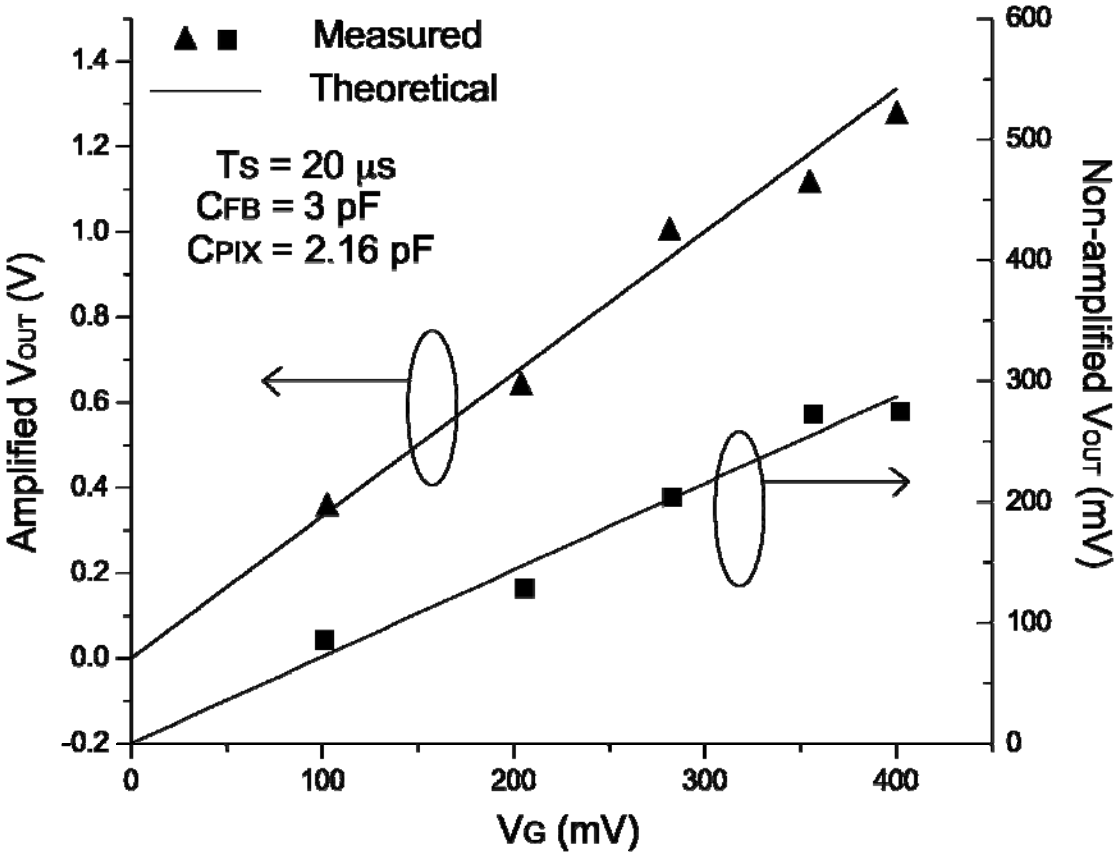

Figure 3-18: HAPS dual readout performance.

The prototype H-APS with dual readout was tested and measurements show a ±14% discrepancy from the theoretical calculations. Signal charge injected into the integration node V_G V_G is varied and a corresponding ΔV_G between 100 to 400 mV is induced. Signal is then readout through the AMP TFT first, then through READ_2 afterwards. It is demonstrated that signal charge can be readout in either of the two paths. The amplified signal (axis on the left) gives a 3.33 voltage gain, while the non-amplified path (axis on the right) gives 0.8 signal gain. The less than unity signal gain for the non-amplified path is due to the differences in C_{PIX} and C_{FB}, and this appears to be a bottleneck in measurements. It is because any input signal less than 100 mV will be further reduced at the output, rendering it un-readable due to equipment sensitivity limitation and additional noise from cabling.

In this experiment, C_{FB} for both amplified and non-amplified column charge amplifiers are the same. The reason for such configuration is to mimic actual array implement where data buses are shared and this topic will be discussed in the next section. Unfortunately, small C_{FB} imposes a limit to integration time for the amplified signal readout (from AMP TFT to charge amplifier). In this set of experiment, integration time is limited to 20 μs, any further increase will require reduction in gain or increasing C_{FB}.

3.3.3.5 Discussions

The H-APS presents itself as the first stage of a-Si:H APS development that extends beyond proving feasibility, to providing additional functionality for large area digital imaging.

Measurement results illustrated that for the same accumulated charge, H-APS allow readout in two modes (high and low signal gain). Non-destructive multiple readout is also possible, making the pixel design amenable to applications that required a wide dynamic range beyond APS (3-TFTs) can provide. Table 3-6 summarizes the design concerns and presents some tradeoffs for H-APS optimization.

Table 3-6: H-APS parameter tradeoffs.

	APS		PPS	
	g_{m_APS}	C_{PIX}	$(W/L)_{READ\_2}$	C_{PIX}
Gain	Maximize	Minimize	Maximize	$C_{PIX} = C_{FB}$
Linearity	NA	Maximize	NA	NA
Readout rate	NA	NA	Maximize	Minimize

It is intuitive that g_{m_APS} should be maximized for higher APS gain. The main design tradeoff is related to C_{PIX}, where the APS gain and linearity entails different requirement. Additionally, a smaller C_{PIX} will require a smaller C_{FB}, which act as a limitation to the range of output voltage swing. Therefore, the design process of H-APS should take careful consideration of the tradeoffs.

As discussed earlier, the PPS readout path performs signal readout and reset simultaneously. After readout, the voltage of the integration node V_G is charged up to V_{REF}, and it is determined by the positive terminal of the column charge amplifier.

Hence, an alternative H-APS design is to omit RESET TFT altogether, and use READ_2 TFT as readout and reset switch. The immediate benefit is a smaller pixel size, which is welcomed from a resolution and cost reduction perspective. However, since the gain of the APS path is strongly influenced by the dc reset voltage V_G, V_{REF} needs to be a positive potential above the threshold voltage V_{TAMP}.

A second possible modification to the H-APS design is to share adjacent data buses. Each H-APS requires two data line for the dual readout capability, and thus doubling data line counts in comparison to the conventional PPS and APS. The array configuration of data bus sharing is shown in Figure 3-19. The amplified and non-amplified outputs of adjacent pixels are connected to the same data bus, effectively reducing the total bus line counts by a half. The readout scheme illustrated before will require no modification, since readout of PPS and APS paths are performed at the same time. Although a time delay between readouts should be inserted to allow all transients to settle down in the charge amplifier. The main impact on performance is the added parasitic capacitance in the data line which in turn hinders the increase in readout rate. There are double the amount of TFTs (all READ and READ_2 TFTs in the same column) contributing to the total data line capacitance C_{DL}. For $W = 108\mu m$ and $W = 60\mu m$, data line capacitance C_{DL} becomes 84 pF comparing to 54 pF for APS and 30 pF for PPS. The higher C_{DL} reduces the readout rate for H-APS, and also reduces the sensitivity for the non-amplified readout as discussed in section 3.2.2.4. Increasing C_{FB} minimizes this effect at the cost of small output voltage swing.

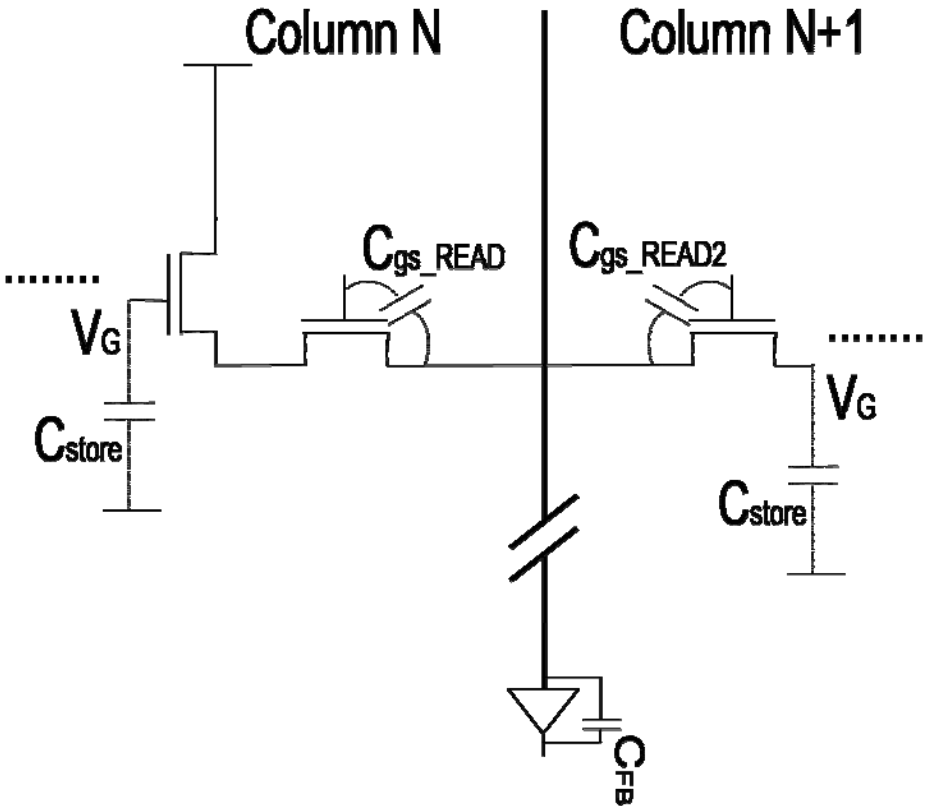

Figure 3-19: H-APS configuration for data line sharing.

Sharing data buses also complicates the optimization for V_{REF}, because the two readout schemes of H-APS necessitate different dc voltages. Recall for APS readout, the column data bus is assumed at zero potential, and V_G is reset to V_{RESET} to allow a sizable gate-source bias across AMP TFT. With data bus sharing and RESET TFT eliminated, $V_{RESET} = V_{REF} = 0$ V, and AMP TFT ceases to operate. A possible solution is to make V_{REF} clocking between readout and reset periods, unfortunately, it comes at a price of slower readout due to charge amplifier settling time and clock jitter. Clock distribution differences may also introduce non-uniformity in AMP TFT biasing points that lead to fixed pattern noise.

Lastly, in comparison to the PPS and APS designs, H-APS suffers from leakage current limitations. Neglecting AMP TFT gate dielectric leakage, there are two TFTs connected to the integration node V_G, namely RESET and READ_2 TFT. Accumulated charge leaks through the TFTs determine the minimum detectable signal level, thereby reducing the dynamic range on the low end. In addition, leakage current also reduces the reset voltage to $V_{REF} - \Delta V_{LEAK}$ where $\Delta V_{LEAK} = \frac{I_{LEAK} T_{INT}}{C_{PIX}}$ and I_{LEAK} is the total leakage current. The effective V_{REF} is decreased, and the maximum charge capacity is reduced, further compromising the dynamic range on the high end. Therefore, it is important to reduce the leakage currents at V_G through optimization of TFT dimensions and careful considerations of the tradeoffs between dynamic range and readout rates.

3.3.4 Hybrid Active Pixel Sensor with Global Shutter

The H-APS design with dual readout provides capabilities beyond the PPS and APS can offer, its complexities and stringent requirement on external electronics can lead to higher cost. Moreover, it does not offer much improvement over APS in terms of signal gain. Here, a new H-APS design with global shutter is presented, as shown in Figure 3-20. The design consists of 4 TFTs, namely AMP, READ, RESET, and TRANSFER. AMP, READ and RESET TFTs perform the usual APS operation and the TRANSFER TFT decouples the storage and sensing capacitances [49]. Unlike previous designs, in which both charge storage and signal sensing are performed through a single nodal capacitance, this design performs each operation with separate capacitances and the operation of the TRANSFER TFT. The storage node V_{STORE} with nodal capacitance C_{STORE} is connected to the sensor and accumulated charge is stored here. The sensing

node V_{SENSE} with nodal capacitance C_{SENSE} constitutes the sum of gate capacitances of the AMP TFT, physical capacitor (if any), and other parasitic capacitances.

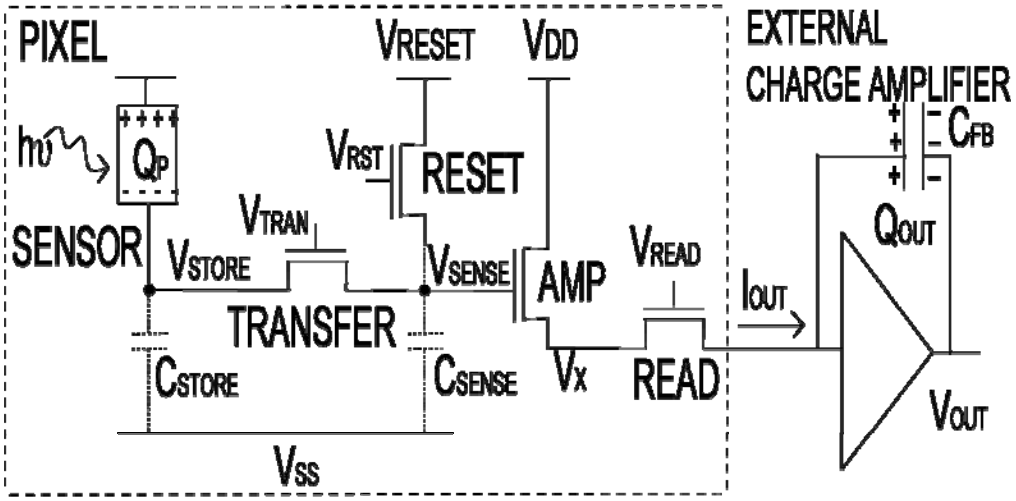

Figure 3-20: Hybrid APS with global shutter.

Similar architectures with in-pixel shutter capability is common for CCD and CMOS image sensors [53][54][55]. The implementation in a-Si:H technology is studied and the work is published in [56][57][58].

3.3.4.1 Operation

This H-APS design can be operated in two different modes, which has corresponding signal gain and linearity, as well as readout rate performances. This section will detail the sequence of operation for the two modes, namely sample-and-hold, and enhanced gain.

Sample-and-hold mode:

The timing diagram for this mode of operation is shown in Figure 3-21.

Initialization: READ TFT is pulsed off, while both TRANSFER and RESET are pulsed on. V_{TRAN} and V_{RST} is $\geq V_{DD} + V_T$, so both C_{SENSE} and C_{STORE} are charged up to V_{RESET}.

Integration: READ, RESET, and TRANSFER TFTs are pulsed off. Here, incident illumination discharges the node V_{STORE} by $\Delta V_{STORE} = Q_P / C_{STORE}$ at the end of integration period T_{INT}.

Sample-and-hold: Near the end of the integration period, the TRANSFER TFT is pulsed on for T_{Sample}. This allows the charge Q_P to transfer from C_{STORE} to C_{SENSE} such that $Q_{SENSE} = Q_P \frac{C_{SENSE}}{C_{SENSE} + C_{STORE}}$. It is also noted that the duration of external illumination is typically much smaller than T_{INT}, thus the short T_{Sample} will not influence total collect charge Q_P.

Readout: RESET and TRANSFER TFTs are pulsed off, and READ is on. The small signal voltage swing $\Delta V_{SENSE} = \frac{Q_{SENSE}}{C_{SENSE}} = \frac{Q_P}{C_{SENSE} + C_{STORE}}$ is amplified by AMP TFT. A small signal current ΔI_{OUT} charges the external charge amplifier feedback capacitor and a voltage output is obtained.

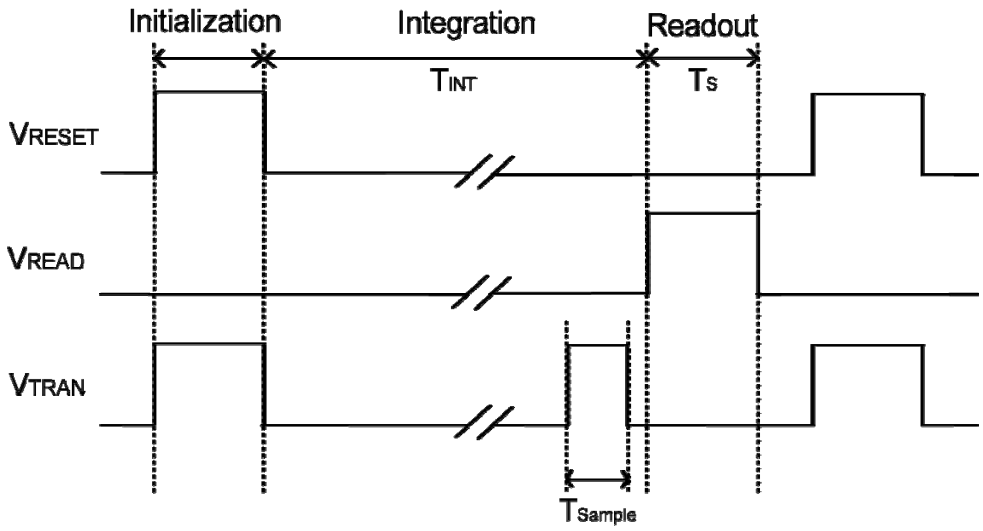

Figure 3-21: Timing diagram for sample-and-hold operation for H-APS with global shutter.

Enhanced gain mode:

The timing diagram for the enhanced gain mode is shown in Figure 3-22.

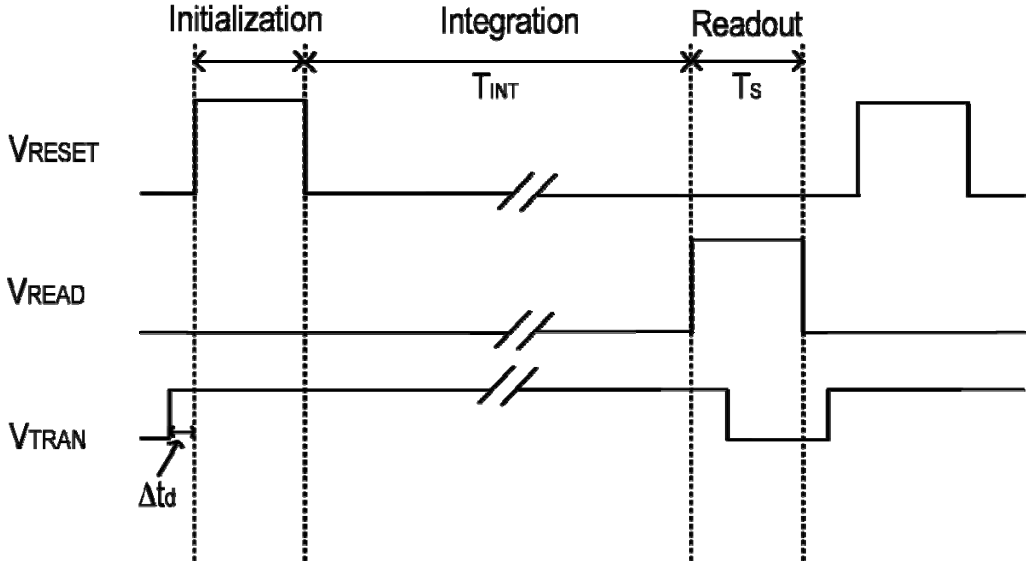

Figure 3-22: Timing diagram for enhanced gain operation for H-APS with global shutter.

Initialization: READ and TRANSFER TFT are pulsed on, while READ TFT is pulsed off. TRANSFER TFT is turned on a Δt_d before READ to allow TFT transient current to settle. It is noted that, unlike sample-and-hold mode, V_{TRAN} is biased at an analogue voltage such that $V_{DD} \geq V_{TRAN} \geq V_T$, but $V_{RESET} \geq V_{DD} + V_T$. As a result, V_{STORE} is reset to $V_{TRAN} - V_T$ while V_{SENSE} is at V_{DD}.

Integration: READ and RESET TFTs are pulsed off, while TRANSFER's gate is kept at its analogue voltage. The nodal voltages at initialization period and the sub-threshold conduction of TRANSFER maintain a potential in-balance between the storage and sense node, i.e. $V_{SENSE} \geq V_{STORE}$. As a result, all signal charge collected from the sensor is attracted to the sense node through TRANSFER, thus $\Delta V_{SENSE} = \frac{Q_P}{C_{SENSE}}$ while V_{STORE} remains unchanged by approximation. This mechanism is termed charge-skimming and is illustrated in Figure 3-23. Charge-skimming stops when $V_{SENSE} = V_{STORE}$, and both C_{STORE} and C_{SENSE} are electronically connected thereafter. Any further accumulated charge discharges both capacitors, given by $\Delta V_{SENSE} = \frac{Q_P}{C_{SENSE} + C_{STORE}}$.

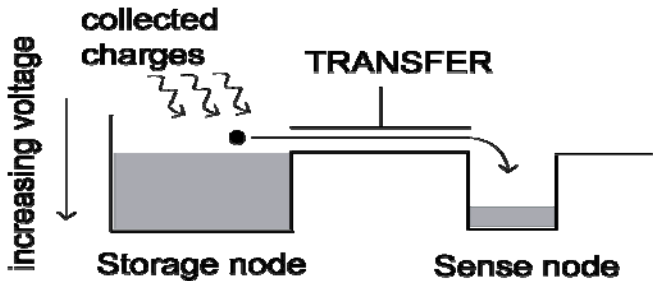

Figure 3-23: Potential for charge-skimming in enhanced mode for H-APS with global shutter.

Readout: RESET TFT is pulsed off, and READ TFT is on. Small signal voltage swing ΔV_{SENSE} is amplified by the AMP TFT and a corresponding V_{OUT} is developed across C_{FB}.

To illustrate the pixel response to incident signals, the transfer characteristics of the enhanced gain mode as seen from the gate of the AMP TFT is simulated as shown in Figure 3-24. Here, the total incident charge of 2 pC is injected into the node V_{STORE} for duration of 33 ms. The storage node has twice the capacitance of the sensing node, and thus the induced $\Delta V_{SENSE} = \Delta V_{G\_AMP}$ is twice as large as the case if the same charge is applied to C_{STORE}. Here, we define the voltage difference between the sense and storage nodes as $\Delta V_{enhanced} = V_{RESET} - (V_{TRAN} - V_T)$, and it determines the maximum of input charge that will receive the enhanced gain. This mechanism is shown in the pixel response in Figure 3-24 for $\Delta V_{enhanced} = 4$ V . Signal initially discharges V_{SENSE} only, when ΔV_{SENSE} reaches 4 V, V_{SENSE} and V_{STORE} discharges together. Note that the slope of the curve is different with the steeper slow at small input signal representing the enhanced gain.

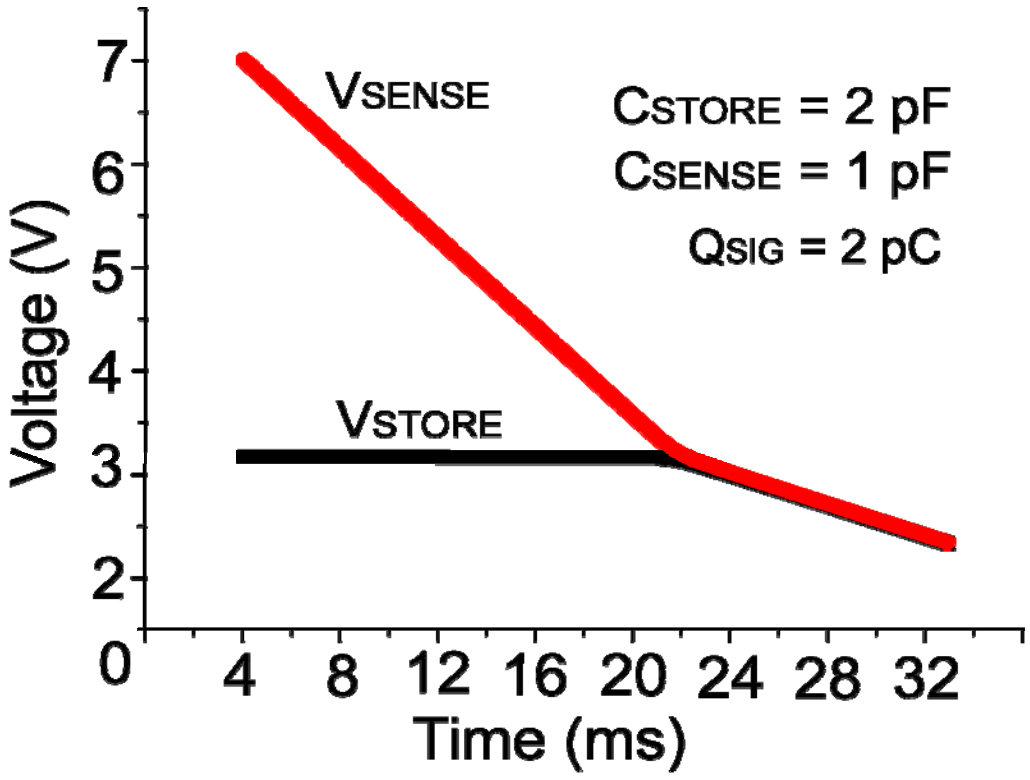

Figure 3-24: Pixel voltage response in enhanced gain mode for H-APS with global shutter.

Figure 3-25 explores the enhanced gain mechanism further by plotting the output voltage against different input current. The steeper slope (117 nV/electron) is a result of the enhanced gain mode, and the shallower slope (4 nV/electron) for high input signal. As a comparison, the APS pixel response as seen from the gate of AMP TFT is also plotted with $C_{PIX} = 1.65$ pF. The linear pixel response of APS has a similar slope with the enhanced gain mode, however the induced voltage swing quickly moves beyond any reasonable voltage range (over 20 V). For typical charge amplifier configuration, the maximum voltage range is limited by the supply voltage rails. It is evident that the H-APS dynamic range is much wider than conventional APS designs.

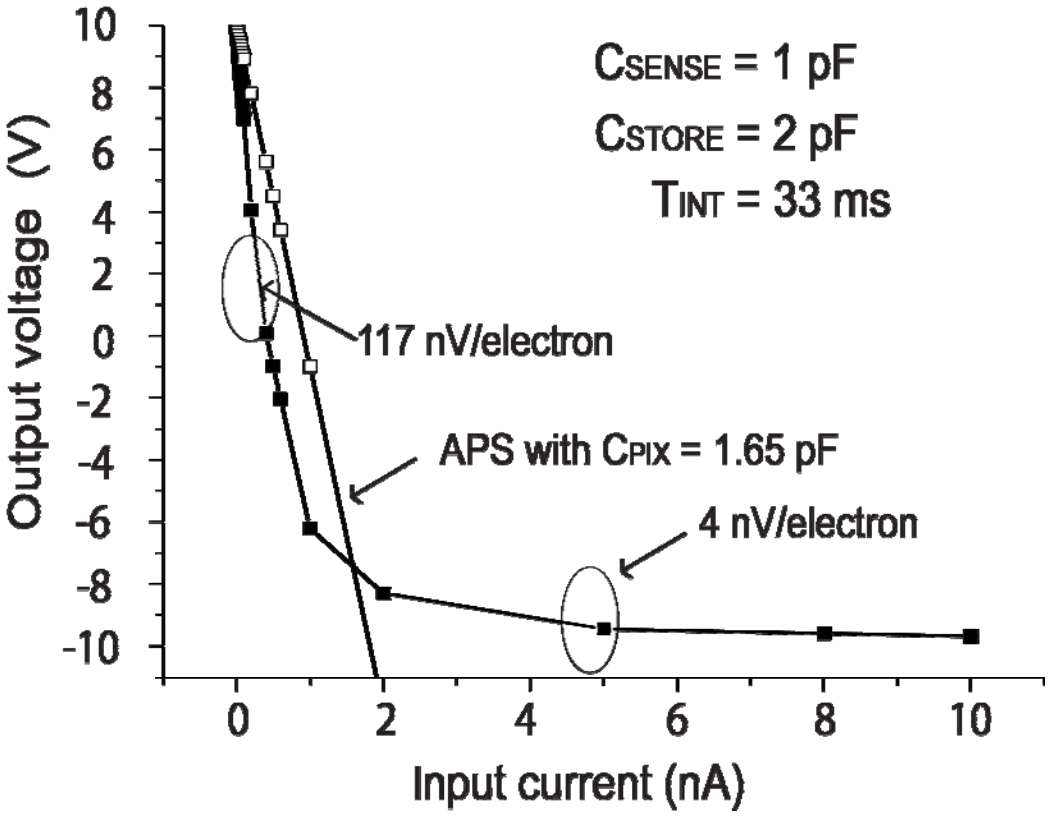

Figure 3-25: Broadened dynamic range for H-APS with global shutter.

3.3.4.2 Signal Gain

The two modes of operation for this H-APS design perform differently in terms of signal gain, and shall be discussed separately.

Sample-and-hold mode:

Accumulated charge Q_P is collected at the storage node during integration, and during sample-and-hold period, a portion of this charge is transferred to the sense node. The charge transfer is determined by the capacitance ratio, given by

$$\begin{aligned} Q_P &= Q_{STORE} + Q_{SENSE} \\ &= Q_P \frac{C_{STORE}}{C_{STORE} + C_{SENSE}} + Q_P \frac{C_{SENSE}}{C_{STORE} + C_{SENSE}}. \end{aligned} \tag{3.25}$$

From equation (3.25), the nodal small signal voltage swing can be obtained,

$$\Delta V_{SENSE} = \frac{Q_{SENSE}}{C_{SENSE}} = \frac{Q_P}{C_{SENSE} + C_{STORE}}. \tag{3.26}$$

Here, ΔV_{SENSE} is the voltage swing that is applied to the gate of the AMT TFT. The gain operation of the composite AMP and READ TFT with the charge amplifier is identical to the APS design, hence combining equation (3.26)and(3.19), the charge gain becomes,

$$\begin{aligned} G_i &= \frac{g_{m\_APS} T_S}{C_{SENSE}} \cdot \frac{C_{SENSE}}{C_{STORE} + C_{SENSE}} \\ &= \frac{g_{m\_APS} T_S}{C_{STORE} + C_{SENSE}}. \end{aligned} \tag{3.27}$$

Here, there are a few observations can be made. Firstly, the charge gain is reduced in comparison to the APS design where $C_{SENSE} = C_{PIX}$. Secondly, this reduction in gain is minimized when $C_{SENSE} \gg C_{STORE}$, by which the charge gain approaches the APS design assuming similar capacitance values. It is a direct consequence of charge transfer efficiency, where a large sense node capacitance will share a large portion of the charge during sample-and-hold operation as illustrated in equation (3.25). Thus, it is beneficial to maximize C_{SENSE} for the sample-and-hold mode of operation. From equation (3.27), the small signal output voltage swing becomes,

$$\begin{aligned} \Delta V_{OUT} &= \frac{G_i Q_P}{C_{FB}} \\ &= \frac{g_{m\_APS} \cdot T_S \cdot Q_P}{C_{FB}\left(C_{STORE} + C_{SENSE}\right)}. \end{aligned} \tag{3.28}$$

Enhanced gain mode:

On the contrary, the enhanced gain operation relies on charge skimming of TRANSFER and sense node capacitance. Signal charge discharges only the sense node and gives,

$$\Delta V_{SENSE} = \frac{Q_P}{C_{SENSE}}, \tag{3.29}$$

and as a result, charge gain becomes,

$$G_i = \frac{g_{m\_APS} T_S}{C_{SENSE}}. \tag{3.30}$$

Intuitively, it is of best interest to minimize C_{SENSE} for higher charge gain. It is also noted, unlike conventional APS design, the enhanced gain mode does not sacrifice dynamic range for gain. When incident signal increases beyond a threshold pre-determined by biasing, the charge gain reduces to

$$G_i = \frac{g_{m\_APS} T_S}{C_{SENSE} + C_{STORE}}. \tag{3.31}$$

Table 3-7 summarizes the signal gain performances for the two modes of operation.

Table 3-7: Gain performance of H-APS with global shutter.

	Sample-and-hold	**Enhanced gain (high gain)**	**Enhanced gain (low gain)**
Charge gain	$\frac{g_{m\_APS}T_S}{C_{STORE}+C_{SENSE}}$	$\frac{g_{m\_APS}T_S}{C_{SENSE}}$	$\frac{g_{m\_APS}T_S}{C_{STORE}+C_{SENSE}}$
ΔV_{OUT}	$\frac{g_{m\_APS}\cdot T_S\cdot Q_P}{C_{FB}\left(C_{STORE}+C_{SENSE}\right)}$	$\frac{g_{m\_APS}\cdot T_S\cdot Q_P}{C_{FB}C_{SENSE}}$	$\frac{g_{m\_APS}\cdot T_S\cdot Q_P}{C_{FB}\left(C_{STORE}+C_{SENSE}\right)}$

3.3.4.3 Signal Linearity

The great resemblance between H-APS and APS allow similar signal linearity analysis. Recall from section 3.2.2.2, signal linearity is ensured if the small signal voltage swing ΔV_G at the gate of the AMP TFT is sufficiently smaller than $\left(V_{GS}-V_T\right)_{AMP}$. The same constraint is applicable for H-APS design, however the different gain modes explained earlier have to be carefully taken into account.

For sample-and-hold mode, combining equation (3.26) and the linearity requirement above gives,

$$\Delta V_{SENSE}=\frac{Q_P}{C_{SENSE}+C_{STORE}}\ll\left(V_{GS}-V_T\right)_{AMP}. \tag{3.32}$$

It is noted the voltage swing due to incident charge is different before and after the sampling process. Prior to the sampling, incident charge is stored at the storage node, and correspondingly gives $\Delta V_{STORE}=\frac{Q_P}{C_{STORE}}$. Combining this with equation (3.32) gives,

$$\frac{C_{STORE} \cdot \Delta V_{STORE}}{C_{SENSE} + C_{STORE}} \ll \left(V_{GS} - V_T\right)_{AMP}. \tag{3.33}$$

From equations (3.32) and (3.33), it can be concluded that the maximum signal allowable without sacrificing linearity is larger in the sample-and-hold mode than conventional APS. It is a direct consequence of the two separate nodal capacitances for charge storage and sensing. It follows that, if $C_{STORE} \approx C_{PIX}$ and $C_{SENSE} \gg C_{STORE}$, both high signal gain and linearity are obtained. For example, if C_{SENSE} is ten times C_{STORE}, the linearity range is an order of magnitude higher than conventional APS.

For enhanced gain mode, the constraint on the gate voltage of the AMP TFT is still applicable. However, the pixel response of this mode of operation is dependent on the gate voltage bias V_{TRAN} and the capacitance ratio. An exact closed form expression for such linearity range is complicated and it is recommended to perform a circuit simulation similar to Figure 3-24.

For illustrative purposes and assuming the total incident charge is sufficiently large to discharge V_{SENSE} to V_{STORE}, the linearity range can be approximated. Recalling that the storage node is reset to a threshold voltage below V_{TRAN}, and the sense node is reset to V_{RESET}. It follows that, for a voltage swing of $V_{RESET} - (V_{TRAN} - V_T)$, only the sense node is discharge. Hence,

$$\Delta V_1 = V_{RESET} - \left(V_{TRAN} - V_{T\_RST}\right) = \frac{Q_{P1}}{C_{SENSE}}. \tag{3.34}$$

When the accumulated charge induces a voltage swing at the sense node larger than ΔV_1 , the pixel enhanced gain reduces and both capacitances discharge simultaneously. Therefore, the second section of the voltage swing becomes

$$\Delta V_2 = \frac{Q_{P2}}{C_{STORE} + C_{SENSE}}, \tag{3.35}$$

where $Q_P = Q_{P1} + Q_{P2}$. The total voltage swing becomes

$$\begin{aligned} \Delta V_{SENSE} &= \Delta V_1 + \Delta V_2 \\ &= \frac{\left[V_{RESET} - \left(V_{TRAN} - V_T\right)\right] C_{STORE} + Q_P}{C_{STORE} + C_{SENSE}}. \end{aligned} \tag{3.36}$$

Equation (3.36) agrees with intuition where the biasing voltage V_{TRAN} plays an influence in when the gain mode transition will occur, thereby changing the maximum allowable signal linearity range. Considering the above analysis, the signal linearity of enhanced gain mode is ensured when

$$\frac{\left[V_{RESET} - \left(V_{TRAN} - V_T\right)\right] C_{STORE} + Q_P}{C_{STORE} + C_{SENSE}} \ll \left(V_{GS} - V_T\right)_{AMP}. \tag{3.37}$$

3.3.4.4 Dynamic Range

The analysis for the dynamic range of the H-APS design is strongly related to the linearity range analysis presented above. The upper limit of the dynamic range is determined by the maximum allowable signal, thus the expressions (3.33) and (3.37) dictates are suitable for sample-and-hold and enhanced gain mode respectively.

The lowest detectable signal for this design, however, is determined by the leakage current of the RESET TFT. Signal charge collected at the sense node can leak

through the RESET TFT to the bias voltage V_{RESET}, thereby limiting the sensitivity of the pixel.

It is noted, leakage current of the TRANSFER TFT does not impose a sensitivity reduction in both modes of operation. In sample-and-hold mode, leakage through TRANSFER will be collected by sense node to be readout later, thus do not constitute any signal loss. In enhanced gain mode, the drain-source conduction is the driving mechanism for the signal gain.

The dynamic range of the detectable signal is then a ratio between the maximum and minimum allowable signal, i.e.,

$$DR_{sample-and-hold} = 20\log\left(\frac{C_{STORE}\cdot\Delta V_{STORE}}{C_{SENSE}+C_{STORE}}\cdot\frac{C_{SENSE}}{T_{INT}I_{leak}\cdot W_{RESET}}\right), \quad (3.38)$$

and

$$DR_{enhanced} = 20\log\left(\frac{\left[V_{RESET}-\left(V_{TRAN}-V_T\right)\right]C_{STORE}+Q_P}{C_{STORE}+C_{SENSE}}\cdot\frac{C_{SENSE}}{T_{INT}I_{leak}\cdot W_{RESET}}\right), \quad (3.39)$$

where I_{leak} is the reset TFT leakage current per unit width.

3.3.4.5 Readout Rate

The readout rate for H-APS is identical to the APS design. It is, however, worth re-stating that there is a relationship between readout sampling rate and signal gain. Increasing the readout duration (T_S) increases the signal gain due to longer charge integration in the charge amplifier feedback capacitor. Careful optimization for various

design and biasing conditions is required to obtain the gain, linearity, as well as readout rate required for specific target applications.

3.3.4.6 Measurement

The H-APS design with global shutter is fabricated with in-house facility in University of Waterloo. Four capacitance ratios are designed to verify both sample-and-hold and enhanced gain mode capabilities. Table 3-8 summarizes all the design parameters for the four fabricated samples. It is noted that capacitance values are taken from measurement values in order to provide a better agreement between theoretical and measurement data.

Table 3-8: List of parameters for H-APS with global shutter.

	Sample 1	Sample 2	Sample 3	Sample 4
$(W/L)_{AMP/READ}$	108/23	108/23	108/23	108/23
$(W/L)_{RESET/TRANSFER}$	60/23	60/23	60/23	60/23
C_{STORE} (pF)	3.12	1.54	9.09	1.20
C_{SENSE} (pF)	3.32	3.21	3.12	3.08

The first set of experiment verifies the sample-and-hold mode of operation as shown in Figure 3-26. The readout time T_S is 20 μs with $V_{RESET} = 10$ V and $V_{DD} = 15$ V. Experimental data agrees reasonably well with theoretical analysis with discrepancies

within 15%. The capacitance ratio CR varies from 0.32 up to 2.88. It is demonstrated that, a smaller the CR brings higher small signal output voltage swing ΔV_{OUT}. It agrees with the analysis performed for the sample-and-hold operation, where $Q_{SENSE} = Q_P \frac{C_{SENSE}}{C_{SENSE} + C_{STORE}}$. Intuitively, this result suggests that C_{SENSE} to be maximized for optimization of charge transfer efficiency. It is worthy of noting that, the reduction of sensitivity due to charge transfer efficiency made it difficult for measurement especially for small input charge. It also explains the large discrepancies with theoretical predictions for the lower signal in Figure 3-26.

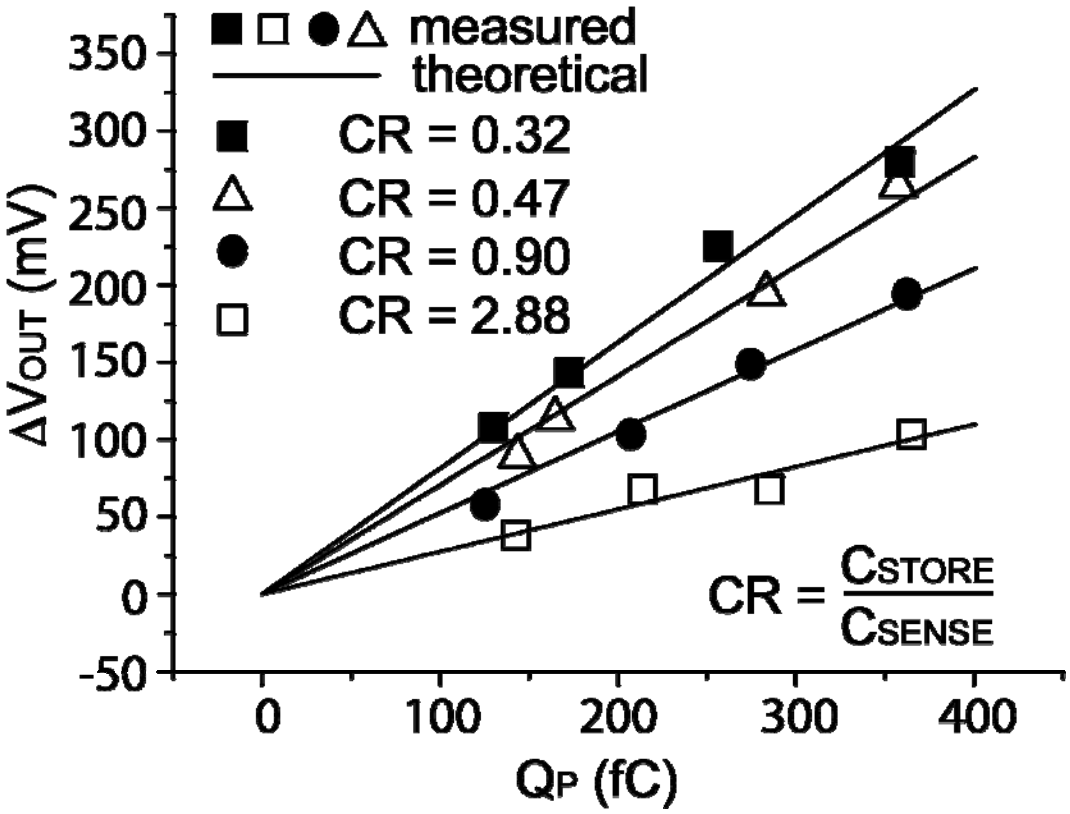

Figure 3-26: Signal gain for H-APS with global shutter in sample-and-hold mode.

Unlike sample-and-hold operation, enhanced gain mode provides a higher gain by means of charge skimming. Incident charge discharges only the sense node capacitance. The samples fabricated (listed in Table 3-8) all have the same C_{SENSE}, so it is logical to predict similar pixel performances for all sample unless $\Delta V_{SENSE} \geq \Delta V_{enhanced}$. This behavior is confirmed through experiment as shown in Figure 3-27. Samples with CR ratio 0.9 and 2.88 are plotted and show little discrepancies (within 6%). The particular experiment data shown in Figure 3-27 is done for $\Delta V_{enhanced} = 5$ V, and thus the enhanced gain mode is sustained through the entire experiment.

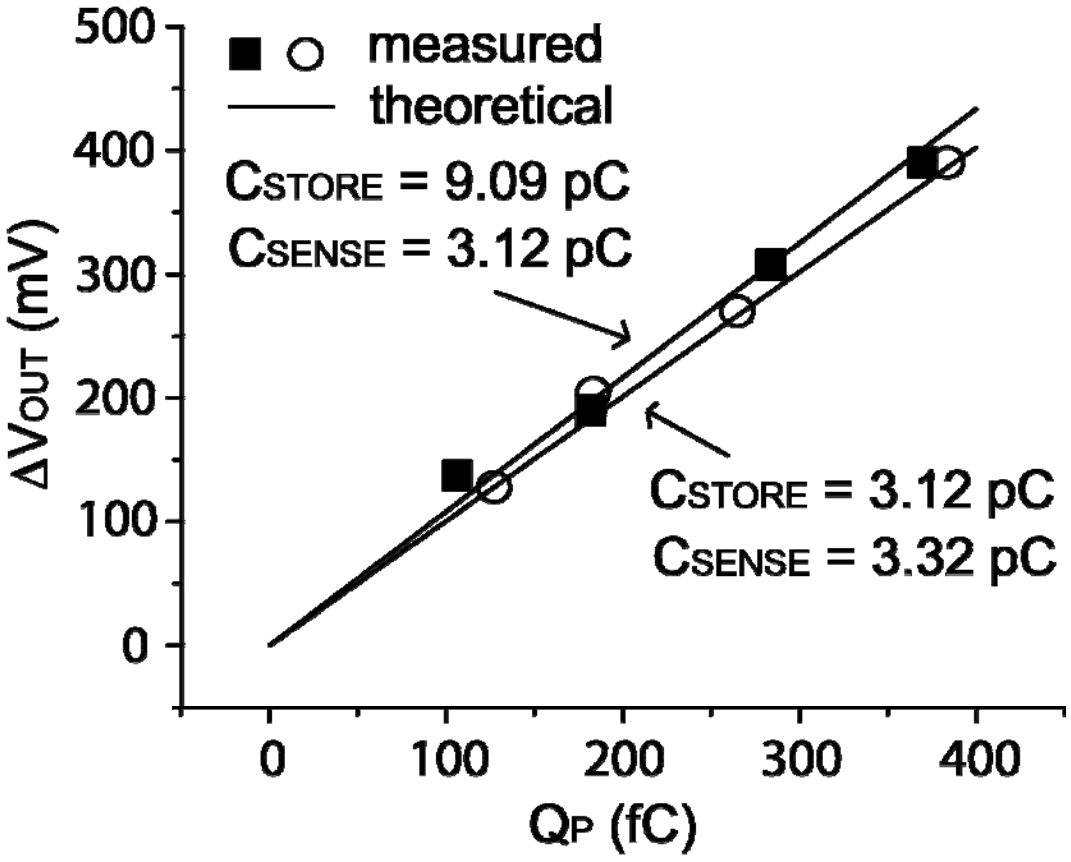

Figure 3-27: Signal gain for H-APS with global shutter in enhanced gain mode.

It is worthy of noting that any fluctuations in the gate clocking pulse during the on duration can accidentally turn on the TRANSFER TFT by providing a gate-source voltage greater than V_T. Thus allowing the potential to equalize between the sense and the storage nodes, and the enhanced gain mode seizes to operate. The above experiments were performed with a dc bias to the gate of the TRANSFER TFT to eliminate the concern. In imaging array design, it is important to make sure external electronics are capable of providing enough voltage stability; this can be done through a higher gate line capacitance at the cost of slower gate clocking frequency and delay.

Figure 3-28 investigates further how capacitance ratio and $\Delta V_{enhanced}$ affect the gain and the voltage at which gain transition occurs. Here, $\Delta V_{enhanced}$ is reduced from 5V from the previous experiments to 0.4 V to allow the gain mode transition to occur. For small Q_P, the pixel provides a gain of 62.8 nV/electron and it depends on C_{SENSE}. When the total accumulated induces $\Delta V_{SENSE} \geq 0.4$ V, the two capacitances are discharged together, reducing the gain to 33.0 nV/electron. The capacitance ratio determines the gain difference between low and high signal, and for $C_{SENSE} \simeq C_{STORE}$, the gain reduction is approximately half.

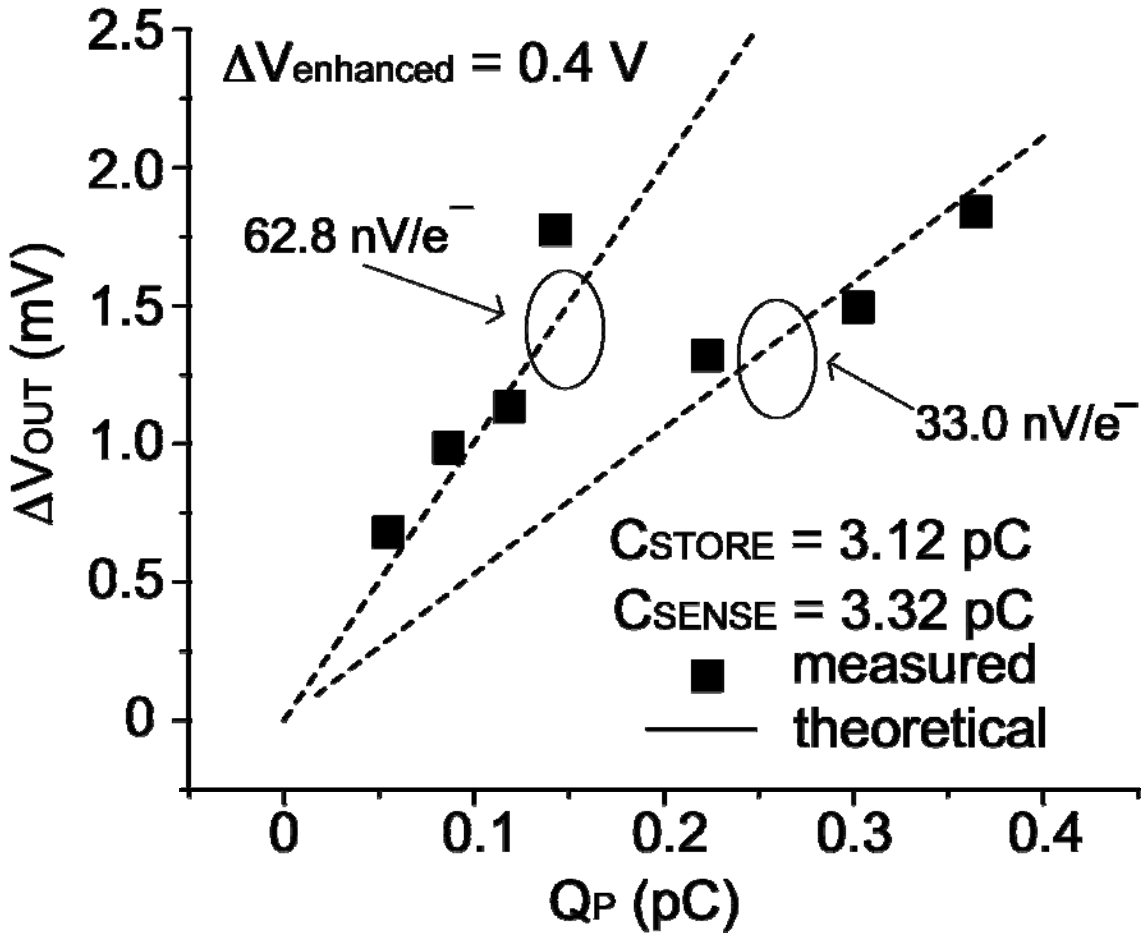

Figure 3-28: Enhanced gain measurements with $\Delta V_{enhanced}$ = 0.4 V and capacitance ratio of 1:1.

Figure 3-29 demonstrates the result for a similar experiment as Figure 3-28, but with a capacitance ratio of $C_{STORE} \simeq 3 \cdot C_{SENSE}$. Since the sense node capacitance is three times smaller, the gain reduction should be approximately 4 times after the gain mode transition. It is shown in Figure 3-29, signal gain reduced from 66.8 nV/electron to 17.2 nV/electron. It is noted for both experiments (Figure 3-28 and Figure 3-29), the discrepancies between measurement and theoretical data are especially pronounced after the gain mode transition, and is due to transient effects of the TRANSFER TFT. Recalling the potential difference between the gate of TRANSFER TFT and storage node

primarily determines the operation of the skimming action. When V_{SENSE} =V_{STORE}, additional signal charge will still discharge V_{SENSE} momentarily, but here V_{TRAN}-V_{SENSE} > V_{TRAN}-V_{STORE}, so the sense node becomes the source of the TRANSFER TFT. The additional current allows V_{TRAN} to discharge to the same level as V_{SENSE}, and this transient effect is the source of the larger discrepancies in measurement data. For the experiment in Figure 3-28, percentage error is 7% before gain transition, and 13% afterwards. For Figure 3-29, percentage error is 9% before the gain transition, and 12% thereafter.

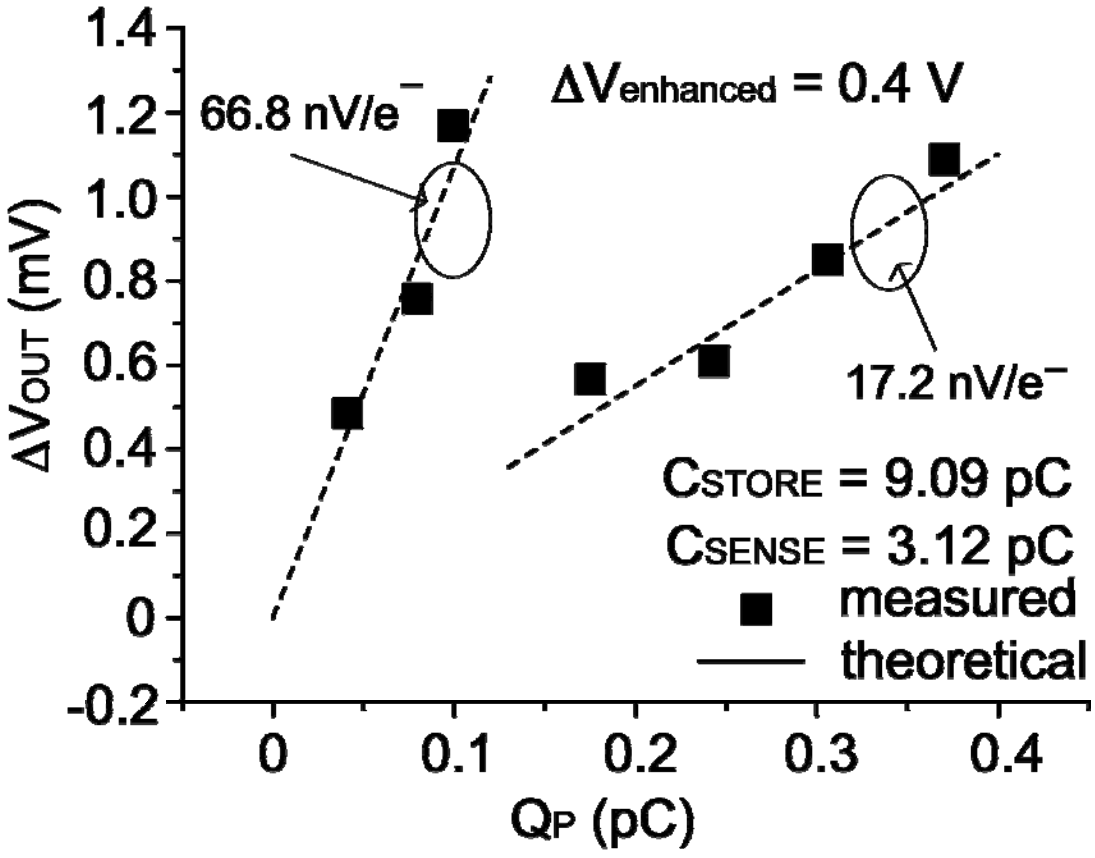

Figure 3-29: Enhanced gain measurements with $\Delta V_{enhanced}$ = 0.4 V and capacitance ratio of 3:1.

3.3.4.7 Transient Behavior

The transient behavior of the H-APS is important because of the delicate analogue operation of the TRANSFER TFT, as well as large TFT capacitances. Any large change in nodal voltages at the sense and storage nodes will impact the pixel performance especially in the enhanced gain mode. For this reason, the transient analysis provides critical information that aids in the design, optimization, and operation of the H-APS.

The two main sources of transients that impact the H-APS operation (or APS for that matter) are TFT channel charge and drain/source overlap capacitance [59][60]. Firstly, when a TFT turns off, charge in the active layer that forms the electronic channel must evacuate to either source or drain terminals. The evacuation of channel charge distributes between source and drain depending on V_{DS} and the speed of transistor turn off transition. For a fast ramp down pulse, i.e. fast fall times, and a small V_{DS} voltage, it is safe to assume an equal spilt of channel charge between the two terminals. The channel charge can be approximated by,

$$Q_{channel} = WLC_{OX}(V_{GS} - V_T). \tag{3.40}$$

Hence, the channel charge to source and drain terminals become,

$$Q_{ch-source} = Q_{ch-drain} = \frac{1}{2}Q_{channel} = \frac{1}{2}WLC_{OX}(V_{GS} - V_T). \tag{3.41}$$

For H-APS, the turn off transients affect the RESET, READ, and TRANSFER TFT only in the sample-and-hold mode. In enhanced gain mode, the TRANSFER TFT is

biased at an analogue voltage and thus the impact of turn off transient is minimized. Using the same TFT dimensions as stated earlier, Table 3-9 is generated.

Table 3-9: Transient channel charge and voltage swing due to TFT turn off.

	RESET	**TRANSFER**	**READ**
$Q_{ch-source}$ (pC)	1.35	1.35	3.16
$\Delta V_{channel}$ (V)	0.45	0.45	2.79

For both RESET and TRNASFER TFTs, the sense node voltage varies only by a few hundred mV, so it can be approximated as $V_{DS} \sim 0$ V . Assuming a 12 V gate bias, $\left(\frac{W}{L}\right)_{RESET,TRANSFER} = \frac{60}{23}$, and $C_{SENSE} = 3$ pF , the channel charge induced voltage swing is 0.45 V. At the end of the initialization phase (see section 3.3.4.1), channel charge is injected from the TFTs into the sense node, thereby lowering V_{SENSE} by approximately 0.9 V in sample-and-hold mode. Fortunately, this injected charge is deterministic, and can be calibrated out by external circuitry. This voltage swing should be factored in during the design phase as it lowers the operating point (V_{GS}) of the AMP TFT and reduces the charge gain. Similarly, channel charge injected from the RESET TFT lowers the sense node voltage in the enhanced gain mode. This voltage drop enlarges the range of the enhanced gain mode (i.e. $\Delta V_{enhanced}$), and extends the position of gain transition (from high to low gain mode).

For READ TFT, the channel charge attracted to the data bus is not going to affect signal readout since the bus is connected to the positive terminal of the charge amplifier with V_{REF}. Channel charge injected into the source of the AMP TFT (V_X in Figure 3-20) induces a much large voltage swing due to the lack of sense node capacitance. The nodal capacitance at V_X consists of overlap and channel capacitance components and is typically in the order of tens of fF. This channel charge potentially induces a transient current when READ TFT is turn on during readout and can last up to a few μs [37][38][41]. Fortunately, external charge amplifier typically has a switch applied across the feedback capacitor. So the READ TFT can be turned on prior to signal integration for the transient to settle at an expense of slower readout rate.

The second transient mechanism that impacts the H-APS operation originates from TFT overlap capacitances. Assuming an overlap of 2 μm between gate and source/drain, and a 20 V swing (12V on and -5V off pulse), Table 3-10 is formulated.

Table 3-10: Transient TFT overlap charge and voltage swing due to TFT turn off.

	RESET	**TRANSFER**	**READ**
ΔV_{ov} (V)	0.19	0.19	0.35

The overlap capacitance induced voltage swing can be written as,

$$\Delta V_{OV} = \left| V_{ON} - V_{OFF} \right| \frac{C_{GS}}{C_{GS} + C_{SENSE}}. \tag{3.42}$$

Here, it is assumed that for RESET and TRANSFER TFTs, the overlap capacitances are in series with the sense node capacitance to ground (V_{RESET} or). So the charge injecting in the overlap capacitance is the same as the ones injected to C_{SENSE} when the gate is pulsed, thereby justifying equation (3.42). Similar analysis can be applied to READ TFT, however, the charge injected into node V_X does not affect the sense node. READ TFT overlap capacitance imposes similar effects on pixel readout performance as channel charge injection. Additionally, according to Table 3-10, the effect of overlap capacitance induced voltage swing is much smaller channel charge injection.

As a comparison, if the TFT process is scaled down to allow a smaller channel length as well smaller gate oxide capacitance, the transient induced voltage errors can be reduced. Table 3-11 summarizes the transient induced errors if the TFT widths are left unchanged, but L = 5 μm and C_{OX} = 25 nF/cm^2. It is evident that process scaling will bring significant benefit in minimizing transient induced errors and allow more flexibility in H-APS design.

Table 3-11: Sample calculations for the reduction in transient induced error with process scaling. L = 5 μm and C_{OX} = 25 nF/cm^2.

	RESET	**TRANSFER**	**READ**
$\Delta V_{channel}$ (V)	0.09	0.09	2.17
ΔV_{ov} (V)	0.12	0.12	0.21

3.3.4.8 In-pixel Correlated Double Sampling

For sample-and-hold mode of operation, the signal sampling action allows in-pixel correlated double sampling to be performed. Correlated double sampling (CDS) is a technique frequently used in digital imaging to reduce various types of noise [61][62][63][64][65]. There are many efforts in utilizing CDS circuits to effectively eliminate fixed pattern noise, and other dominating noise source in active pixel sensors such as reset noise. Conventionally, CDS is performed at the output, but recently CMOS image sensor development has been successful in integration the functionality in the pixel level [61][64][65]. The H-APS presented here is capable of performing CDS in the pixel level and the driving scheme can be explained by Figure 3-30.

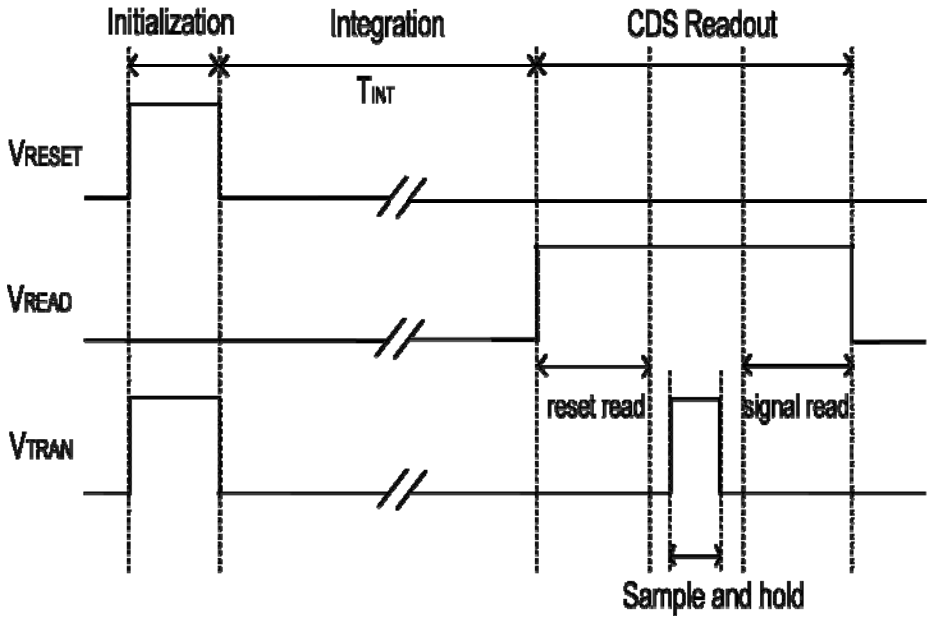

Figure 3-30: Timing diagram for in-pixel CDS for H-APS with global shutter.

The pixel CDS is performed by first reading out the reset signal level via AMP TFT to the charge amplifier and then followed by a sample-and-hold via TRANSFER TFT. Then the pixel is reset, allowing a reference voltage to appear at the sense node for the next frame. The two signal samples are tightly spaced in the time domain, allowing a true CDS to be performed. . The signals can be manipulated at external circuit to suppress fixed pattern and other low frequency random noise. The pixel CDS is always applied with respect to the reset of the current frame rather than with respect to the previous reset signal. This yields minimum correlation time compred with a subsequent frame reset level and thus provides the best 1/f noise reduction (noise analysis is discussed in a later chapter).

3.3.4.9 Discussions

The H-APS with global shutter design offers higher gain, automatically adjustable gain levels, as well as higher dynamic range comparing to previously discussed designs. The table below summarizes the results of the analysis into one table for easier references.

A few observations can be made from Table 3-12. Firstly, the gain expression of the enhanced gain mode reduces to that of sample-and-hold when the incident signal swing exceeds $V_{RESET} - \left(V_{TRAN} - V_T\right)$. This reduction in gain occurs seamlessly without the need of any bias change, and effectively widens the dynamic range without sacrificing signal linearity. Secondly, even though the pixel design allows operation in either of the two modes without any hardware modification (assuming external circuitry provides all necessary bias and pulse addressing), the two modes entail different capacitance ratios

from signal gain perspective. Sample-and-hold mode requires a smaller CR to maximize charge transfer efficiency, while enhanced gain mode relies on smaller C_{SENSE} to provide higher gain. It is therefore a design tradeoff between functionality and gain requirements. As a note, a smaller C_{SENSE} can provide higher signal gain in the enhanced mode; however the larger voltage swing pushes the pixel to reach $\Delta V_{SENSE} > \Delta V_{enhanced}$ sooner, thereby limiting the amount of signal that can benefit from the enhanced gain.

Table 3-12: Summary of performances for H-APS with global shutter.

	Sample-and-hold	**Enhanced gain**	
		High gain $\Delta V_{SENSE} \le \Delta V_{enhanced}$	**Low gain** $\Delta V_{SENSE} > \Delta V_{enhanced}$
Charge gain	$\frac{g_{m\_APS} T_S}{C_{STORE} + C_{SENSE}}$	$\frac{g_{m\_APS} T_S}{C_{SENSE}}$	$\frac{g_{m\_APS} T_S}{C_{SENSE} + C_{STORE}}$.
Signal linearity	$\frac{C_{STORE} \cdot \Delta V_{STORE}}{C_{SENSE} + C_{STORE}} \ll (V_{GS} - V_T)$	$\frac{\left[V_{RESET} - (V_{TRAN} - V_T)\right] C_{STORE} + Q_P}{C_{STORE} + C_{SENSE}} \ll (V_{GS} - V_T)$	
Readout rate	Switching speed of READ TFT and trade off between signal gain		
Dynamic range	$\frac{C_{STORE} \cdot \Delta V_{STORE}}{C_{SENSE} + C_{STORE}} \cdot \frac{C_{SENSE}}{T_{INT} I_{leak} \cdot W_{RESET}}$	$\frac{\Delta V_{enhanced} C_{STORE} + Q_P}{C_{STORE} + C_{SENSE}} \cdot \frac{C_{SENSE}}{T_{INT} I_{leak} \cdot W_{RESET}}$	
C_{STORE}/C_{SENSE}	Minimize	Maximize	

The dynamic range of the H-APS is undoubtedly one of the attractive attributes of the design. Comparing to APS, where the dynamic range (DR) is limited by the linear pixel response, H-APS with global shutter can provide at least a ten-fold increase in DR. The higher DR makes the design amenable to applications where high image contrast is required and possibly opens the door to multi-modality imager. For enhanced gain mode, the TRANSFER TFT's gate is biased at an analogue voltage V_{TRAN}, and it is shown that the magnitude of this bias also has an effect on dynamic range. It is advisable to set V_{TRAN} at a higher value closer to the pixel reset voltage at the sense node (V_{RESET}) for a wider dynamic range, and there is a bonus effect of smaller carrier trapping during charge skimming. Recalling that defect densities in the mid gap governs the subthreshold performance of TFTs, a higher gate voltage results in more occupied mid-gap defects, resulting in less drain-source carrier trapping. Thus, there is a tradeoff between the enhanced signal gain range, dynamic range and carrier trapping for the optimization of V_{TRAN} bias. Table 3-13 compares the dynamic range performances for the two modes of H-APS operation against conventional APS design. Here, it is assumed the leakage current of TFT is 1 fA/μm TFT width, integration time of 1 s, a maximum voltage swing of 400 mV at the gate of the AMP TFT, $\Delta V_{enhanced} = 0.2$ V , $C_{PIX} = C_{SENSE} = 1$ pF, and $C_{STORE} = 10$ pF.

Table 3-13: Dynamic range comparison.

	APS	**H-APS Sample and hold**	**H-APS enhanced gain**
Dynamic Range (dB)	136	156	152

Here, the dynamic range is approximately 10 dB larger than conventional APS design. CMOS or CCD imager can typically achieve over 100 dB of dynamic range, a-Si:H TFT based imaging array has much larger capacitances, which serve as a bottleneck in achieving higher DR. It is also worthy of noting that the both modes of operation of H-APS provides more functionality or higher charge gain in addition to the wider dynamic range.

3.4 Comparison of Pixel Architectures

There are a total of four pixel architectures discussed and analysis in this chapter, each has its own strength in terms of performance and architectural complexity. The last section in this chapter attempts to draw a few insights to compare these designs and investigates their suitability to different areas of large area medical imaging. Pixel designs are compared according to their performances and area constraint is discussed with possible suggestions to increase feasibility.

3.4.1 Suitability to Medical Imaging

The characteristics and performances of the pixel designs are simplistically summarized in the table below. All four pixel designs are compared based on linearity, signal gain, readout rate, dynamic range and TFT count to provide some insights to their respective suitability for different modalities of large area medical x-ray imaging.

Table 3-14: Comparison of pixel designs.

	PPS	**APS**	**H-APS dual readout**	**H-APS global shutter**
Linearity	Large	Small	Large	Large
Signal gain	Unity	>Unity	>Unity	>>Unity
Readout rate	Static	Real-time	Real-time	Real-time
Dynamic range	Medium	Narrow	Wide	Wide
TFT count	1	3	4	4
Modality	Radiography	Radiography, fluoroscopy	Radiography, mammography	Radiography, fluoroscopy

It is evident that the APS design improves over PPS by providing inherent signal gain and real time readout. The H-APS designs, on the other than, extends and combine the PPS and APS designs to provide higher signal gain, while improving the dynamic range by at least an order of magnitude. The gain, linearity, and dynamic range performances suggest suitability to different imaging modalities for different pixel design and are also listed in Table 3-14. Even though APS and H-APS performances are undoubtedly superior to PPS, their circuit complexity and TFT counts imposes area constraints to their implementations, hence highest achievable array resolution.

3.4.2 Area Constraints

The high TFT count and circuit complexity of H-APS entails more real estate usage in comparison to the PPS and APS. Conventional APS requires 2 bias, 2 address and one output lines. Both of the discussed H-APS require one additional address line, with the H-APS with dual output needing an extra output line. With X-ray imaging modalities requiring pixel size below 300 μm x 300 μm, it is a challenge to implement and design arrays based on H-APS. Fortunately, there are layout and circuit design techniques that can alleviate the concern.

3.4.2.1 Bias and Address Line Sharing

Unlike CMOS, large area technologies such as a-Si:H have few layers of metallization that can be used for bias and address buses. A direct consequence is the reduction of geometrical fill factor when pixel designs require high TFT and bias line counts. In some pixel designs, bias and address lines can be shared, effectively increasing the fill factor, thereby reducing the pixel pitch. For active pixel sensors, the most common topology is to share the reset bias and supply lines. Figure 3-31 illustrates the sharing scheme and the same setup can be implemented in APS, and both H-APS designs.

Noticeably, adjacent pixels need to be mirrored vertically and horizontally in order for both bias lines to be shared. From a device layout perspective, the periodicity of the imaging array is hindered, possibly causing fixed pattern noise and modification to the modulated transfer function (MTF) of the array.

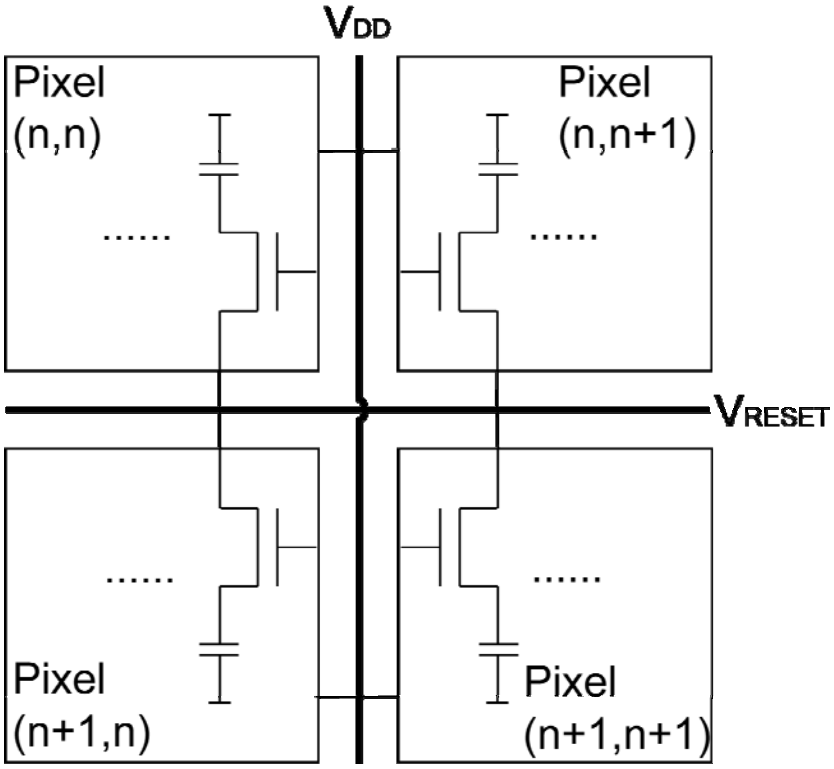

Figure 3-31: Bias and address sharing for pixel array.

In addition, it is also possible to share gate lines for adjacent pixels within the same row. An example will be the TRANSFR TFT gate line, where a sample-and-hold pulse is applied to the entire row. Sharing gate lines do not contribute to any extra parasitic capacitances as long as pixels are from the same row, but requires pixel mirroring. Assuming state-of-the-art processing technology, bias and address line widths are approximately 6 to 10 μm. Line sharing will reduce the pixel pitch by 10 μm in both horizontal and vertical direction, and contributes to a 7% increase in geometrical fill factor for a 300 μm x 300 μm pixel.

3.4.2.2 Transistor Sharing

In addition to bias and gate line sharing, APS and H-APS architectures can be extended to share TFT between adjacent pixels. Transistor sharing is not uncommon in CMOS imager arena in order to achieve small pixel pitch for high resolution imaging applications. In specific, RESET, AMP, and READ TFTs can be shared among two [66] or four pixels [67][68][69][70]. This sharing scheme is shown in Figure 3-32, where four adjacent pixels are connected to the same AMP TFT via separate ACCESS TFTs. Such a sharing scheme can reduce the overall TFT count to 1.75 TFT per pixel, hence reducing area usage. In addition, since the bias and gate lines for the common TFTs are shared between four pixels, the total number of metal lines required is drastically reduced. The normal H-APS having four TFTs typically occupies about 380 μm x 380 μm, and scaling the design accordingly for TFT sharing scheme yields a pixel size of approximately 250 μm x 250 μm. This corresponds to a 34.2% reduction in pixel size.

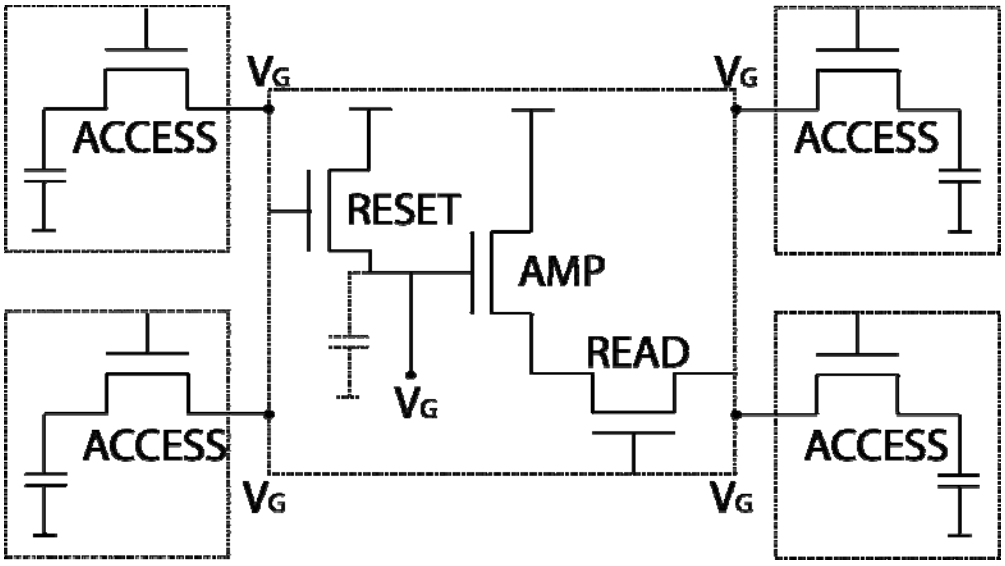

Figure 3-32: TFT sharing scheme for pixel array.

On the other hand, the sharing of TFT introduces design and analysis complexity. Firstly, there are additional capacitive coupling for sharing pixels since all ACCESS TFTs are connected to the same node. Charge leakage through ACCESS TFTs to V_G constitutes inter-pixel crosstalk. The clocking of ACCESS gate of one pixel can also induce leakage fluctuations of the rest of the pixels, leading to higher crosstalk. Moreover, gate-source overlap of ACCESS TFTs contributes to the nodal capacitance at V_G, which leads to higher noise. It is for these reasons TFT sharing is not implemented in prototypes at this stage to avoid complications in pixel design evaluation, and such technique is reserved as one of the future considerations.

4 Noises in TFT and Pixel Circuits

This chapter begins by discussing the various TFT noise sources and their impact on the implementation, design, and operation of pixel circuits. Analysis and measurements are presented and their relevance to pixel designs is evaluated. Next, noise performances of various pixel designs in Chapter 3 are compared through experiments. Lastly, noise behavior improvement due to technology scaling is discussed in order to draw some insights towards future pixel performance trend.

4.1 Thermal Noise

In 1927, J.B. Johnson observed random fluctuations in the voltages across electrical resistors [71]. A year later, H. Nyquist published a theoretical analysis of this noise and associated the origin to thermal agitation of electrons inside the resistor [71]. Nyquist proposed that randomized scattering between electrons and atoms inside the material is elevated by thermal energy, causing fluctuations in the current and voltage. Physically, such mechanism is attributed to the variations of conductance/resistance, but is more customarily modeled by voltage/current fluctuations. Hence, this type of noise is known as Johnson noise, Nyquist noise, or Thermal noise.

Active device such as field effect transistors conduct current through an induced electronic channel, thus the drain-source current also suffers from thermal noise. Van der Ziel [72] confirms the existence of this noise component and demonstrated the current spectral density fluctuation in a MOSFET is

$$S_I(f) = \frac{1}{L^2}\int_0^L 4kTg(y)dy \tag{4.1}$$

where L is the channel length, k the Boltzmann constant, T the temperature, and g(y) is the conductivity of the channel at a distance y away from the source. Note that the expression does not depend on frequency, suggesting a flat noise spectrum for thermal noise. In addition, the conductance g(y) is directly proportional to free carriers in the channel, which in turn has a strong dependency on transistor operation. Hence, equation (4.1) is only the general form and it is considered for different modes of operation for a transistor (linear and saturation regime).

In the linear regime, the drain-source bias for a transistor is small, resulting in a relatively uniform channel conductance. As a result, it is typically valid to assume

$$g(y) = L \cdot g_{Vds=0} \tag{4.2}$$

where $g_{Vds=0}$ is the zero drain bias conductivity and is

$$g_{Vds=0} = \frac{W}{L} C_G \mu (V_{GS} - V_T). \tag{4.3}$$

Combining (4.3) and (4.2), and substituting into (4.1) gives

$$S_I(f)_{linear} = 4kTg_{Vds=0} = 4kT\frac{W}{L} C_G \mu (V_{GS} - V_T). \tag{4.4}$$

However, the expression in (4.4) do not hold true when the drain bias is increased. Drain-source voltage results in a non-uniform channel charge distribution, leading to

spatially varying conductance that needs to be calculated. Recalling the definition of conductance of carriers is

$$g(y) = \mu \cdot W \cdot Q(y) \tag{4.5}$$

where $Q(y)$ is the channel charge at position y. The total charge can then be defined as

$$Q_G = \int_0^L Q(y)dy = C_G W \int_0^L \left(V_{GS} - V_T - V(y)\right) dy. \tag{4.6}$$

The variable $dy = \frac{I_{DS}}{g(y)} dV$, applying change of variable technique and using the simple MOS linear I_{DS} equation gives

$$dy = \frac{WL}{(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2} \left[V_{GS} - V_T - V(y)\right]. \tag{4.7}$$

The integration in equation (4.6) can be carried out with dV and it yields

$$Q_G = \frac{2}{3} C_{OX} WL \frac{\left(V_{GS} - V_T\right)^3 - \left(V_{GD} - V_T\right)^3}{\left(V_{GS} - V_T\right)^2 - \left(V_{GD} - V_T\right)^2}, \tag{4.8}$$

where the identity

$$2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2 = \left(V_{GS} - V_T\right)^2 - \left(V_{GD} - V_T\right)^2 \tag{4.9}$$

is used to simply the expression. Combining equations (4.1), (4.6) and (4.8) yields the power spectral density for thermal noise when transistor in saturation mode of operation

$$S_I(f)_{saturation} = \frac{2}{3}(4kT)\left(\mu C_G \frac{W}{L}\right)\frac{(V_{GS}-V_T)^3-(V_{GD}-V_T)^3}{(V_{GS}-V_T)^2-(V_{GD}-V_T)^2}. \quad (4.10)$$

At saturation, transistor's drain-source can be assumed as $V_{DS} = V_{GS} - V_T$, hence $V_{GD} - V_T = 0$ and equation (4.10) simplifies to the well known formula

$$S_I(f)_{saturation} = \frac{2}{3}(4kT)\, g_{Vds=0}. \quad (4.11)$$

In summary, the transistor thermal noise power spectral density is

$$S_I(f) = A \cdot (4kTg_{Vds=0}) \quad (4.12)$$

where

$$A = \begin{Bmatrix} 1 \text{ in linear} \\ \frac{2}{3} \text{ in saturation} \end{Bmatrix} \quad (4.13)$$

and

$$g_{Vds=0} = \frac{dI_{DS}}{dV_{DS}}. \quad (4.14)$$

The above formulation was originally developed for MOSFET in crystalline silicon. Many authors have studied the thermal noise behavior on a-Si:H TFT and confirmed similar noise behavior. Boundry and Antonuk [73], and K.S. Karim [74] modeled the TFT thermal noise using the same equation in (4.12) where a simplified TFT drain-source current equation is used, such that

$$g_{Vds=0} = \frac{dI_{DS}}{dV_{DS}} = \mu_{EFF} C_G \frac{W}{L} \left(V_{GS} - V_T\right)^n \tag{4.15}$$

where $n = \left(\alpha - 1\right)$ and is extracted to be 1.3 for TFTs fabricated in University of Waterloo. As a result, the thermal noise equation becomes

$$S_I(f) = A \cdot \left(4kT\right) \cdot K \cdot \left(V_{GS} - V_T\right)^n \tag{4.16}$$

where $K = \mu_{EFF} C_G \frac{W}{L}$.

Measurement of thermal noise for a-Si:H TFT is not a trivial task for a few main reasons. Firstly, it is difficult to isolate the contribution of flicker noise from thermal noise in a-Si:H, largely due to the reason of trap states in the channel causing a significant 1/f component. It is therefore needed to minimize the drain-source current to suppress flicker noise in measurement. In addition, measurements should be taken at frequencies well beyond the 1/f corner frequency. Secondly, the intrinsically low free carrier count in a-Si:H material causes the thermal fluctuation to be small in comparison to MOSET devices, making it difficult to measure without any significant amplification. It is for these reasons, thermal noise measurement for TFT in saturation regime is not recommended.

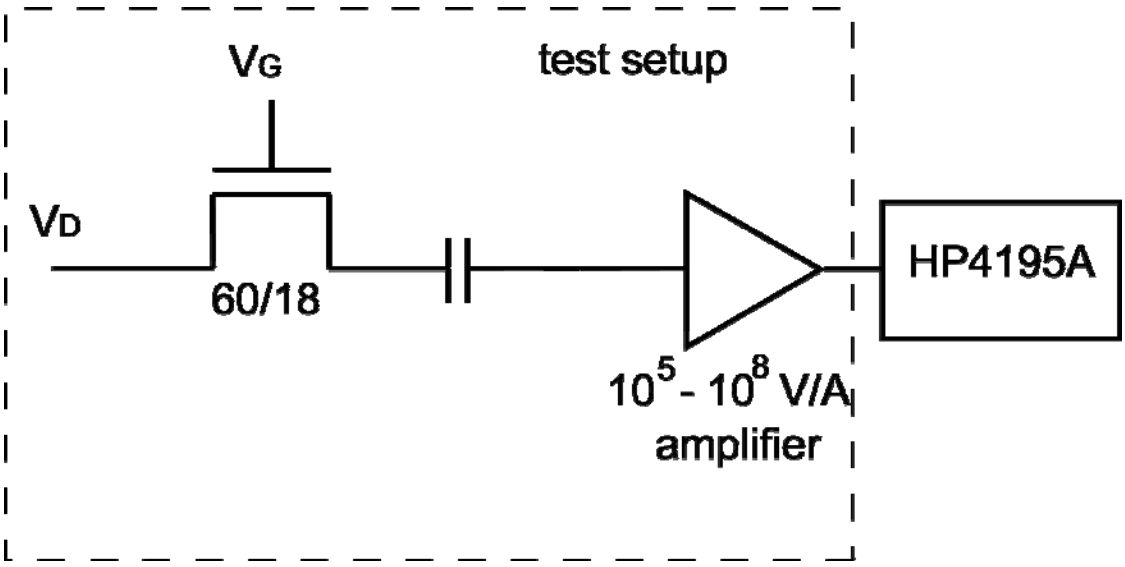

Figure 4-1: Thermal noise test setup.

Figure 4-1 illustrates the setup for TFT thermal measurement. The TFT dimension used in RESET and READ TFT is placed under test to correlate with the actual pixel design discussed in the previous chapter. The gate and drain bias for the TFT, V_G and V_D, are provided by low noise rechargeable batteries. The drain source current is connected to a low noise transimpedance amplifier through ac coupling. The amplifier is used to amplify the thermal noise to allow a detectable signal for the spectrum analyzer HP 4195A. The transimpedance amplifier provides an AC gain of 10^5 to 10^8 between 10 kHz to 1 MHz. The measurement is performed at least 20 times and the noise power spectra curves are then averaged and re-constructed from small bandwidth results. The dc biases are applied to the TFT and measurements are performed an hour afterwards to eliminate all currents transients.

In the above setup, the amplifier also contributes to the total noise measured and it has to be extracted. The total noise power measured by the spectrum analyzer is the noise voltage fluctuation and it is

$$S_V(f) = A \cdot (4kT) \cdot K \cdot (V_{GS} - V_T)^n \int_0^\infty [G(f)]^2 \, df + S_{AMP}(f) \tag{4.17}$$

where $S_{AMP}(f)$ is the output noise generated by the amplifier itself, and $G(f)$ the gain of the amplifier at frequency f. The amplifier gain $G(f)$ at various frequencies can be independently measured, so $\int_0^\infty [G(f)]^2 \, df$ can be determined. Thus, by measuring $S_V(f)$ and plot it against applied gate bias (V_{GS}), one extracts the thermal noise from the slope and the abscissa gives $S_{AMP}(f)$.

Using the above method, the thermal noise is measured and the result is shown in Figure 4-2 with the y-axis in log-2 scale. Gate voltage is varied from 4 to 10 V in 2 V increments and the diagram plots 5 measured results to verify the accuracy. The output amplifier noise referred back to the input is extracted from the intercept and is approximately 3×10^{-28} A^2/Hz. The amplifier noise is at least 1 to 2 orders of magnitude smaller than the measured TFT thermal noise. The theoretical current noise power exhibits almost a power law relation with gate bias and the shape draws similarity to TFT I_{DS} current. This agrees with the power spectral density formulation developed in equation (4.16).

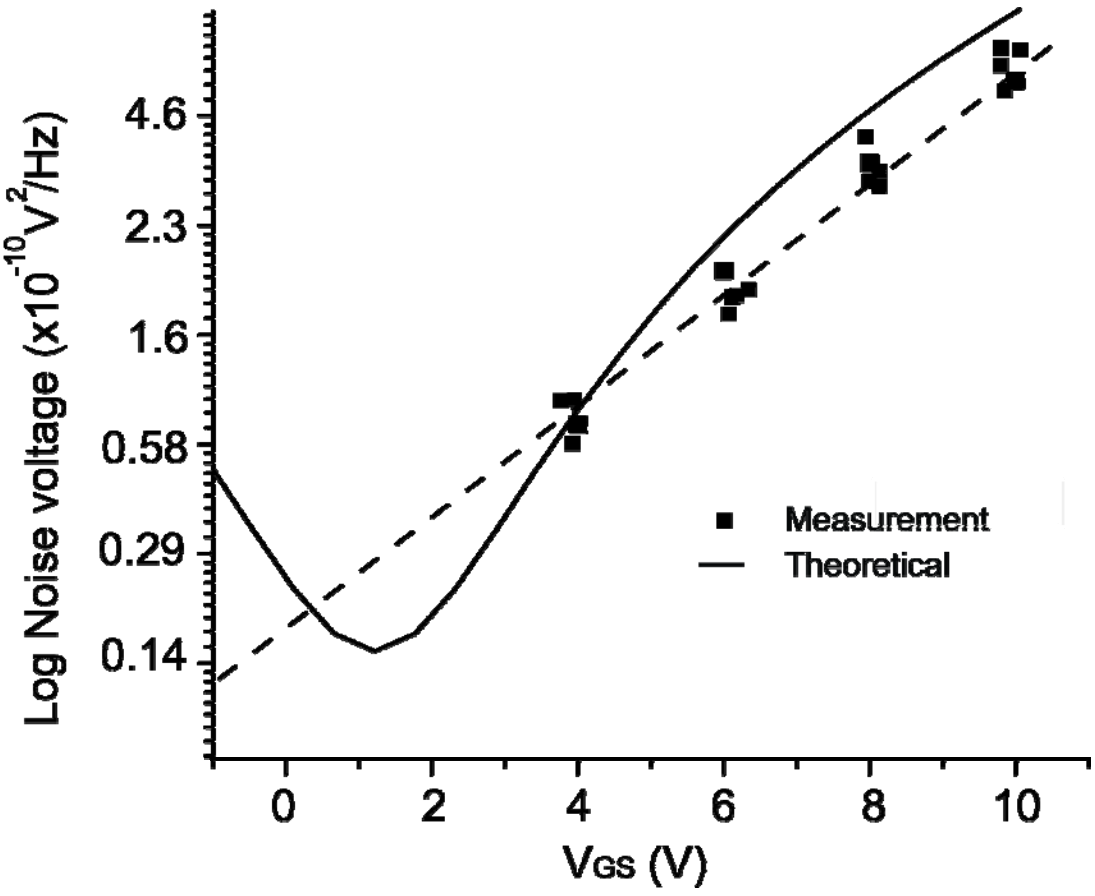

Figure 4-2: Thermal noise measurement and extraction.

From Figure 4-2, comparison between theoretical prediction and measurement results show reasonable agreement for low gate biases. As the gate bias increases, the discrepancies grow and the measured noise power is typically larger than predictions. This is mainly due to the larger TFT series resistance contribution to total drain-source resistance, because the channel resistance is reduced as gate bias increases. The channel resistance dominates the total drain-source resistance at small V_{GS}, hence the lower discrepancy. It is also worthy of noting that the larger measured noise at high gate voltage is unlikely due to the contribution of 1/f noise, since the ac coupled transimpedence amplifier act as a high pass filter to suppress low frequency noise.

Table 4-1: Thermal noise power measurements for TFT in linear regime.

W/L = 60/23 V_{DS} = 0.4 V	Theoretical $S_I(f)$ (A^2/Hz)	Measured $S_I(f)$ (A^2/Hz)	Percentage Error
V_{GS} = 4 V	2.71×10^{-27}	2.80×10^{-27}	3%
V_{GS} = 6 V	6.69×10^{-27}	6.07×10^{-27}	10%
V_{GS} = 8 V	1.13×10^{-26}	9.7×10^{-26}	14%
V_{GS} = 10 V	1.65×10^{-26}	9.07×10^{-26}	45%

Table 4-1 summarizes the measurement and theoretical results and clearly demonstrates the larger percentage error for higher gate bias scenarios. For the same TFT operating in saturation, the measurements do not generate meaningful results with the same setup and experimental technique. The larger drain-source current leads to higher flicker noise component and also the much smaller channel resistance render experiment non-representative.

4.2 Flicker Noise

Flicker (or 1/f) noise was first observed by Johnson in 1925 from an experiment designed to test Schoottky's shot noise theory in vacuum tubes [71]. Johnson discovered the direct current through a conductor exhibits higher fluctuation at low frequencies, unlike the white (or flat spectrum) thermal noise [75]. This fluctuation is experimentally

found to have a 1/f dependency, hence the name, and the general power spectral density is

$$S_I(f) = \frac{A \cdot I^2}{f^a}. \tag{4.18}$$

where I is the magnitude of the direct current, a the 1/f slope that lied between 08 to 1.4 in general [71][75][76], A the constant that is proportional to the conductor's area. Flicker noise has been verified to exist in addition to thermal noise and its 1/f slope extends to 10^{-6} Hz without any signs of flattening out [71][75]. Field effect transistors such as MOSFETs and TFTs also exhibits flicker noise and many authors have studied the effects [74][76][77][78]. Since then, two main theories for the physical origin of 1/f noise in transistors are developed, namely the carrier number fluctuations theory, and the mobility fluctuation theory. McWhorter first introduced a sophisticated model which 1/f noise is attributed to the random trapping and de-trapping of carriers in surface states. This is known as the number fluctuation model. Accordingly, the power spectral density of the current is

$$S_I(f) = \frac{k^*}{f} \frac{\mu}{C_{OX} L^2} \frac{I_{DS} V_{DS}}{(V_{GS} - V_T)} \tag{4.19}$$

where k^* is related to the electron tunneling from insulator traps near the interface to the conducting channel and vice versa and is

$$k^* = \frac{q^2 k T D_t(E_F)}{\ln(\tau_1 / \tau_2)}. \tag{4.20}$$

$D_t(E_F)$ is the active trap density in the vicinity of the Fermi level (E_F), and the quantities τ_1 and τ_2 the lower and the upper boundaries of the time constants involved in the trapping-de-trapping process. While McWhorter theory's theory explains flicker noise in MOSFETs, it does not adequately explain 1/f observations in homogeneous ionic gas where there is no interface traps.

The second theory considers the 1/f noise as a result of the fluctuation in the carrier mobility. Hooge and Hoppenbrouwers proposed the random fluctuation in carrier mobility results in the 1/f spectrum observed in conducting medium [77]. The power spectrum of 1/f noise according to the mobility fluctuation model is

$$S_I(f) = \frac{\alpha_H I^2}{N_{tot} f^a} \tag{4.21}$$

where I is the direct current, α_H the dimensionless coefficient, N_{tot} the total number of carrier in the medium. The Hooge coefficient α_H is typically found through experiments for different mediums.

Both theories succeeded in partially explaining some of the experimental data. Since it is very difficult to experimentally verify the origins of noise generation, there is no conclusive evidence to date to support either theory. A lot of efforts have been dedicated into the convergence of the two theories into one unified model especially for CMOS transistors [78][79]. In light of the advancements of CMOS technologies, FETs with very low surface states can be made, allowing the simplification of the number fluctuation theories. Unified 1/f noise models have been studied by various authors in

references [78][79][80]. Unfortunately, a-Si:H TFTs suffer from the disordered lattice orientation in the active layer do not benefit in the unified 1/f noise model study. Hence, the two theories for flicker noise are both considered here for comparative purposes.

For the number fluctuation model, assuming TFT operating in the linear regime with an I_{DS} equation

$$I_{DS} = K\left(V_{GS} - V_T\right)^{\alpha-1} V_{DS} \tag{4.22}$$

where V_{DS} is small, and $K = \mu_{EFF} C_G \frac{W}{L}$. Substituting equation (4.22) into (4.19) gives the power spectral density for TFT in linear mode as

$$S_{I\_linear}(f) = \frac{k^*}{f} \frac{\mu_{EFF}}{C_G L^2} \left[K \cdot \left(V_{GS} - V_T\right)^{n-1} V_{DS}^2 \right]. \tag{4.23}$$

From equation (4.23), the PDF for TFT in saturation regime is found by substituting $V_{DS} = \left(V_{GS} - V_T\right)$ and that yields

$$S_{I\_saturation} = \frac{k^*}{f} \frac{\mu_{EFF}}{C_G L^2} \left[K \cdot \left(V_{GS} - V_T\right)^{n+1} \right]. \tag{4.24}$$

On the other hand, the total number of channel carrier has to be found for the mobility fluctuation theory. For TFT working in linear regime,

$$N_{tot} = WLC_G\left(V_{GS} - V_T\right) \tag{4.25}$$

and combining this with equation (4.21) gives

$$S_{I\_linear} = \frac{\alpha_H}{f}\frac{q\mu_{EFF}}{L^2}\left[K\left(V_{GS}-V_T\right)^n V_{DS}^2\right]. \tag{4.26}$$

The PDF for flicker noise in saturation regime is found the same way as the number fluctuation model, giving

$$S_{I\_saturation} = \frac{\alpha_H}{f}\frac{q\mu_{EFF}}{L^2}\left[K\left(V_{GS}-V_T\right)^{n+2}\right]. \tag{4.27}$$

Table 4-2: Flicker noise power spectral densities for number and mobility fluctuation models.

	Number fluctuation	Mobility fluctuation
S_{I_linear}	$\frac{k^*}{f}\frac{\mu_{EFF}}{C_G L^2}\left[K\cdot\left(V_{GS}-V_T\right)^{n-1}V_{DS}^2\right]$	$\frac{\alpha_H}{f}\frac{q\mu_{EFF}}{L^2}\left[K\left(V_{GS}-V_T\right)^n V_{DS}^2\right]$
$S_{I\_saturation}$	$\frac{k^*}{f}\frac{\mu_{EFF}}{C_G L^2}\left[K\cdot\left(V_{GS}-V_T\right)^{n+1}\right]$	$\frac{\alpha_H}{f}\frac{q\mu_{EFF}}{L^2}\left[K\left(V_{GS}-V_T\right)^{n+2}\right]$

Table 4-2 summarizes the PDF formulation for both TFT linear and saturation regimes based on two theories. It is noted that, despite the various coefficients, the main difference between the two theories lies in the dependency on $\left(V_{GS}-V_T\right)$, where the mobility fluctuation model shows a higher relation in the exponent.

The experimental setup for thermal noise (see Figure 4-1) can also be used for flicker noise measurement. Recalling in the setup for thermal noise, the transistor I_{DS} is minimized and the measurement is performed well beyond the low frequency range to reduce the flicker noise contribution. Here, it is intuitive that the experiment has to be

performed at sufficiently low frequency to highlight the flicker noise trend. The experiment is performed at least 20 times and the data are averaged to verify the consistency. All biases are applied an hour prior to data acquisition to allow all transient current to settle. In addition, the dc (direct) current is monitored by the transimepdiance amplifier before and after experiments to obtain threshold voltage shift due to prolonged bias. In these experiments, the threshold voltage shift is less than 6% after one and a half hour of bias.

To begin the analysis for flicker noise measurement, the first task is to identify which model is more suitable for a-Si:H TFT. The two sets of modeled PDFs for 1/f noise differ mainly in the characteristic slope when plotted against $(V_{GS}-V_T)$ as illustrated in Table 4-2. For the number fluctuation theory, $S_I(f)$ varies with $(V_{GS}-V_T)^{n-1}$ and $(V_{GS}-V_T)^{n+1}$ in linear and saturation regimes respectively. On the other hand, $S_I(f)$ varies with $(V_{GS}-V_T)^{n}$ in linear regime and $(V_{GS}-V_T)^{n+2}$ in saturation for the mobility fluctuation model. Thus, through extracting the slopes from the log-log plot of $S_I(f)$ vs. $(V_{GS}-V_T)$ in both regimes of operation, one can determine which model generates a better fit to experimental data. Figure 4-3 illustrates the plot used to extract the characteristic slopes, and it demonstrates an exponent of 2.81 for saturation and 1.23 for linear regime. The comparison between the experimental data and the two 1/f models are tabulated in Table 4-3. The in-house fabricated TFTs appear to match the Hooge theory (mobility fluctuation) better and this is also in agreement with other authors [81][82][83].

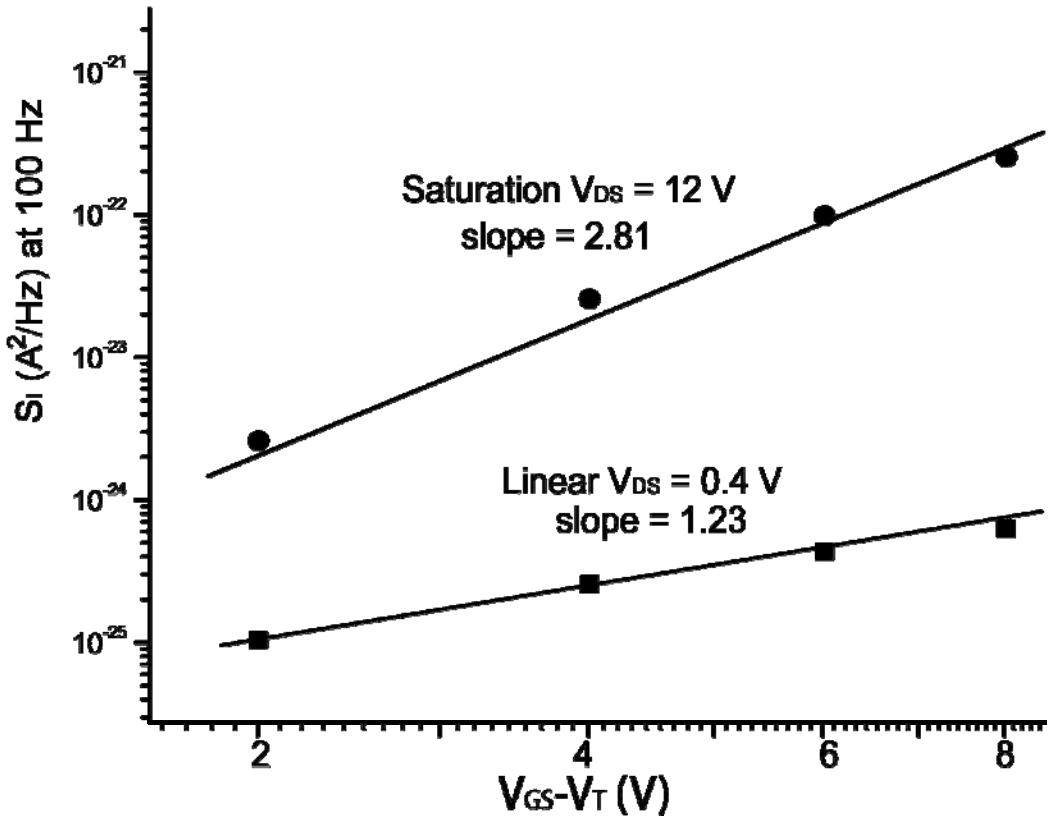

Figure 4-3: Flicker noise characteristic slopes for linear and saturation regimes.

Table 4-3: Comparison for measured characteristic slopes between experimental data and the two 1/f noise models.

$(V_{GS} - V_T)^X$	**Measured**	**Number fluctuation**	**Mobility fluctuation**
x for linear regime	1.23	0.3	1.3
x for saturation regime	2.81	2.3	3.3

Figure 4-4 and Figure 4-5 show the power spectra for a-Si:H TFT in linear and saturation regimes at different gate bias. Here, flicker noise dominates most of the spectrum at low frequencies. However, thermal noise drowns out flicker noise near 7 kHz and become indistinguishable thereafter. In both figures, flicker noise increases as the gate bias increase, which agrees with prediction it is directly proportional to direction current. Measured data shows a 21% maximum error with the theoretical (Hooge's model) prediction in linear regime, and an 18% maximum error in saturation regime.

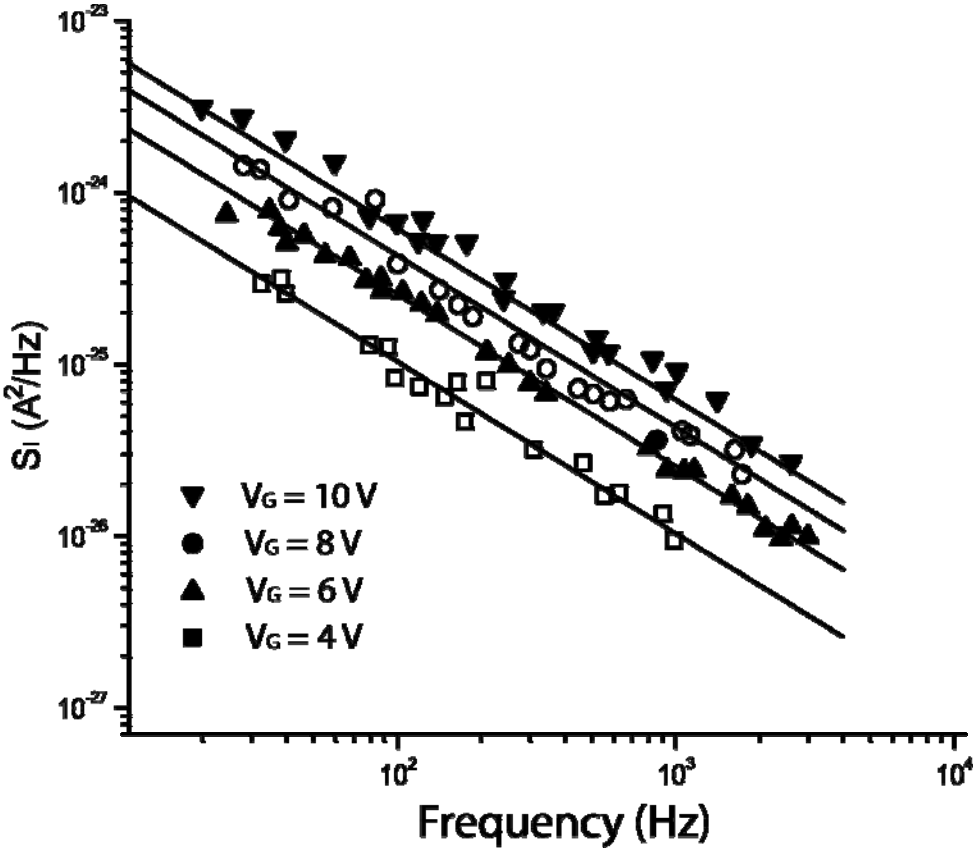

Figure 4-4: Flicker noise spectra for a-Si:H TFT in linear regime.

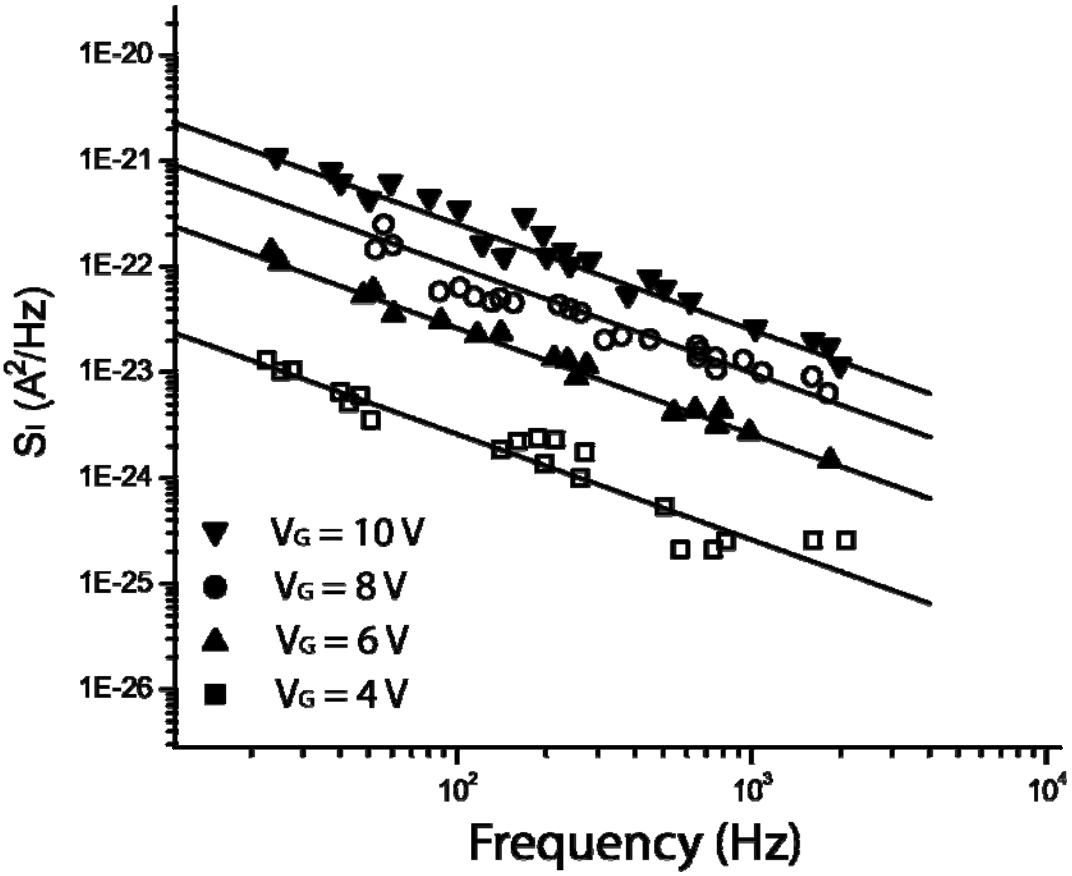

Figure 4-5: Flicker noise spectra for a-Si:H TFT in saturation regime.

4.3 Reset Noise

Charge detection in imaging circuits requires the photo-sensitive element to be reset to a know reference value after readout, allowing signal to be integrated for the next image frame. This reset operation is commonly used in many areas of imager design, such as CCD, CMOS image sensors, and the pixel architectures discussed in Chapter 3. The reset structure can be simplified and generalized as shown in Figure 4-6. Here, the charge collection node is denoted by its equivalent capacitance C, and the reset transistor

drains the accumulated charge after readout to the reference voltage generator. The detection node is typically connected to an amplification stage, such as the source follower configuration in APS, and is represented as the amplifier in the diagram for simplicity. The details of pixel operation are explained in Chapter 3 for various pixel designs and are not repeated, and this section focuses on the reset operation and its noise generation. .

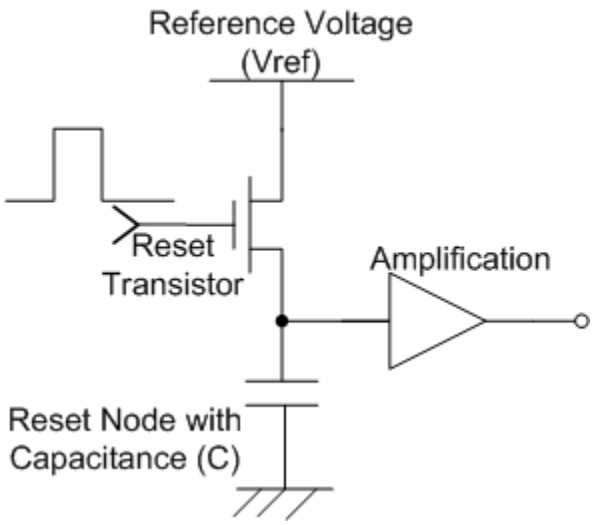

Figure 4-6: General reset structure in image sensor architecture.

Charge detection in pixel circuits relies on the repeatability to generate a reference voltage (or "known voltage") at the detection node after each reset cycle. However, capacitive node cannot be reset to the same voltage according to thermodynamic principles. Even for the scenario when there is no accumulated charge, reference voltage still suffers from slight fluctuations that is related to the thermal conductance variations of the reset device. This fluctuation is non-deterministic and is termed as reset noise or kTC noise [92]. The name kTC noise stems from its well-known closed form expression for the noise variance, and it takes the form

$$\frac{1}{2}\left\langle v_n^2 \right\rangle C = \frac{1}{2}kT \text{ or } \left\langle v_n^2 \right\rangle = \frac{kT}{C} \text{ or } \left\langle Q_n^2 \right\rangle = kTC \tag{4.28}$$

where C is the capacitance of the reset node, k the Boltzmanns' constant, and T the temperature. Equation (4.28) is useful in providing a numerical value for the voltage or charge fluctuations, but lacks the ability to provide the spectral information of such noise source. In complex pixel circuits, TFT operation imposes frequency limitation that directly affects the power spectrum of the noise as seen at the output. The spectral density of such a reset operation was first analytically studied by Hynecek on CCDs [93].

$$S_c(\omega) = S_o \left|H(\omega)\right|^2 \left[1 + \zeta + \frac{1}{2}(\omega_f \tau)\zeta^2 F_1 \cdot \text{sinc}^2\left(\frac{\omega\delta}{2}\right) + \zeta F_2 \text{sinc}^2\left(\frac{\omega\delta}{2}\right)\right], \tag{4.29}$$

where the various quantities are defined as

$$S_o = \frac{1}{\pi}kTR. \tag{4.30}$$

$$\zeta = \frac{\delta}{\tau}, \tag{4.31}$$

$$\omega_f = \frac{1}{RC}, \tag{4.32}$$

$$\left|H(\omega)\right|^2 = \frac{\omega_f^2}{\omega_f^2 + \omega^2}, \tag{4.33}$$

$$F_1 = \frac{\omega_f^2}{\omega_f^2 + \omega^2} \cdot \frac{\sinh\left[\omega_f(\tau - \delta)\right]}{\cosh\left[\omega_f(\tau - \delta)\right] - \cos(\omega\tau)}, \tag{4.34}$$

$$F_2 = 2\left|H(\omega)\right|^2 \frac{\cos\left(\frac{\omega\tau}{2}\right)\cosh\left[\omega_f(\tau-\delta)\right]-\cos\left[\omega_f\left(\tau-\frac{\delta}{2}\right)\right]}{\cosh\left[\omega_f(\tau-\delta)\right]-\cos(\omega\tau)}. \qquad (4.35)$$

The derivation of the above formulas and expressions are explained in Appendix A, readers are forwarded there for more detailed information. This work is also fully documented and published by the author in [95][96][97][98].

The PDF at the output of the amplifier exhibits a sinc function behavior with respect to frequency. In particular, the term with $\text{sinc}^2\left(\frac{\omega\delta}{2}\right)$ dominates the whole expression such that it is intuitively understandable that as reset duration (i.e. δ) becomes smaller, so will the reset noise spectrum. In addition, reset noise originates from thermal noise, which is a flat spectrum across all frequencies. The sampling of a flat spectrum signal generates a sinc function behavior is a direct consequence of time domain signal analysis. Hence, the sinc behavior of reset noise agrees with intuition.

Reset noise measurement is particular challenging for amorphous silicon devices due to large noise contribution of flicker noise. In a typical imaging setup like the APS where the integration node is connected to the gate of a source follower TFT, flicker noise from the drain-source current rendering isolation of reset noise a particular difficult task. Thus, the use of a-Si:H based amplifier (AMP TFT) is not recommended, and the drain-source current of the reset TFT is minimized by reducing V_{DS} across the device.

The measurement setup is shown in Figure 4-7. Here, a reset TFT of W/L = 60/18 is used to reset a nodal capacitance of approximately 21 pF. Here, the source follower amplifier is replaced by a low noise amplifier (LNA 138 from Burrbrown), and the

integration node is directly connected to the positive terminal. The reset transistor's gate is driven by a pulse generator and the amplifier's input capacitance as well as other parasitic capacitance constitutes the total nodal capacitance. Since reset noise is of particular interest here, the drain-source bias of the reset TFT is minimized, hence $V_{REF} < 200$ mV. Moreover, the gate and source of the TFT is connected using a variable high resistance voltage divider to alleviate any amplifier saturation issue. The first amplifier stage (LNA 138) provides a gain of 10, and subsequently a gain of 50 is provided by a wideband FET-input amplifier. The RC high pass filter (HPF) is included to remove any wide band amplifier noise that may contaminate reset noise measurement.

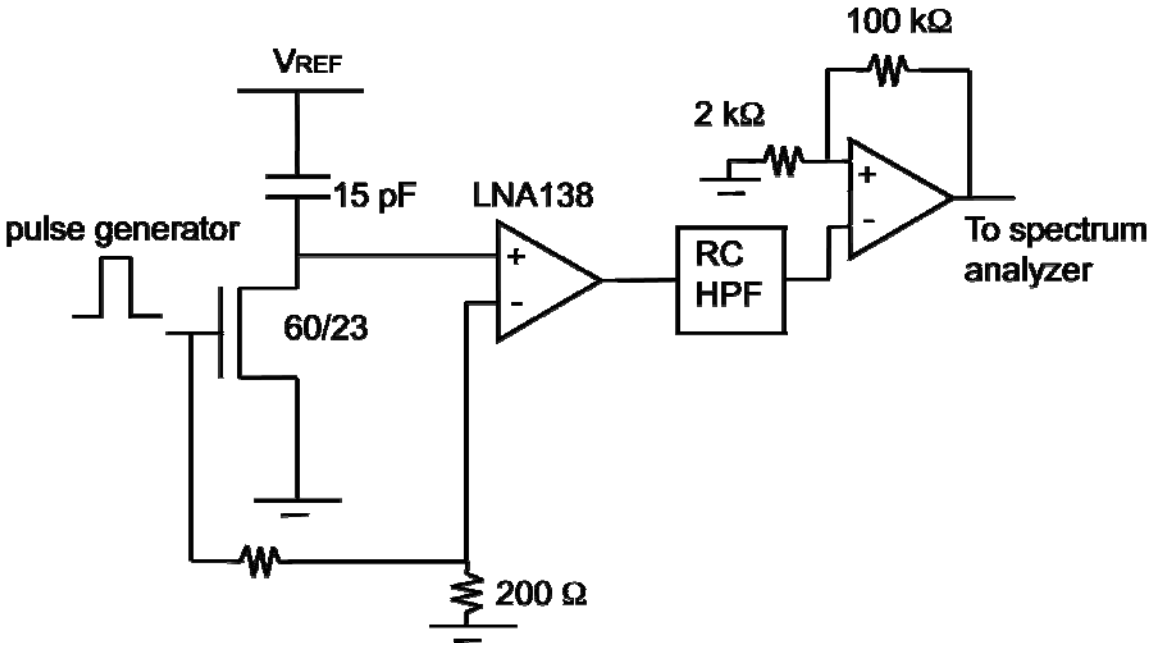

Figure 4-7: Reset noise measurement setup.

Despite the effort in the measurement setup in isolating reset noise, the amplification stage contributes to the total noise measured and it is necessary to take it

into consideration. The equivalent simplified circuit for the measurement setup is shown in Figure 7-2 where V_g^2 is the amplifier noise and A_o is the gain.

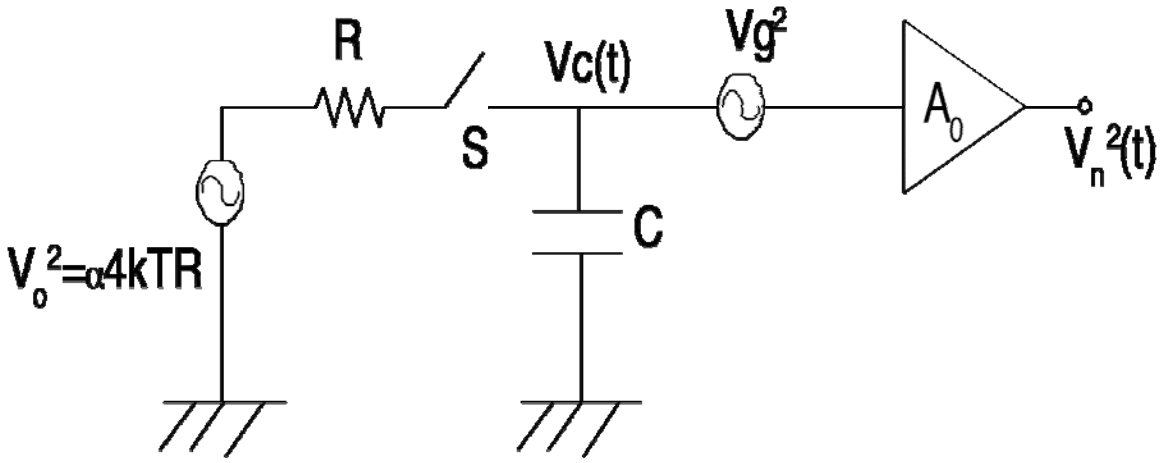

Figure 4-8: Reset noise measurement setup equivalent circuit.

Note that in Figure 7-2, the thermal noise component is $\alpha 4kTR$ and deviates from the Johnson noise quantity. The parameter α is typically greater than unity and provides information about the spurious noise, namely partition noise, contribution from the reset operation and is further discussed in a later section.

The formulation in equation (4.29) uses frequency domain and is measured in radians per second. It will be changed to a more customary units of frequency measured in hertz and it will extend from 0 to +∞ in the limits of integration. This modification introduces a multiplicative factor of 4π into the formula. As a result,

$$\left\langle v_n^2 \right\rangle = \int_{-\infty}^{\infty} S_c(\omega) d\omega, \tag{4.36}$$

and switching to frequency in hertz gives,

$$V_n^2(f) = \left|H_a(2\pi f)\right|^2 A_o^2 \left[V_g^2 + 4\pi S_c(2\pi f)\right], \tag{4.37}$$

where $\left|H_a(2\pi f)\right|^2$ is the normalized frequency response of the amplifier, and is assumed unity for the case studied here. In addition, writing equation (4.37) in terms of the ideal kTC noise variance can further simplify the expression to a representative form. The kTC noise variance is defined as

$$V_k^2 = \frac{kT}{q} S_a A_o, \tag{4.38}$$

where S_a is the amplifier charge conversion factor and it is defined as

$$S_a = \frac{q}{C} A_o \tag{4.39}$$

Combining equations (4.37), (4.38), and (4.39) yields,

$$V_n^2(f) = V_g^2 A_o^2 + \alpha 4V_k^2 \left(\frac{1}{\omega_f}\right) \frac{S_c(2\pi f)}{S_o}. \tag{4.40}$$

Equation (4.40) contains three parameters, namely α, ω_f, and V_g, and they can extracted from measurements first before the model can be used for experimental data comparison. The parameter α contains the spurious noise in the circuit and a convenient way of extraction is to plot the noise power spectral density at frequency f = 0 as a function of reset pulse period τ. With the assumption of $\omega_f \tau \gg 1$, the slope of such plots gives

$$\frac{dV_n^2(0)}{d\tau} = \alpha 2V_k^2 \zeta. \tag{4.41}$$

The extraction for the measurement data is shown in Figure 4-9 for different gate pulse period. It is noted that the extracted value of α is larger than unity, implying there are additional noise source in addition to reset noise that is related to the reset operation.

The parameter V_g can be easily found by simply leaving the reset TFT off, so that

$$V_{op} = V_n(f) = A_o V_g. \tag{4.42}$$

Particular care in measuring V_g is done beyond the flicker noise frequency corner since the model does not incorporate flicker noise.

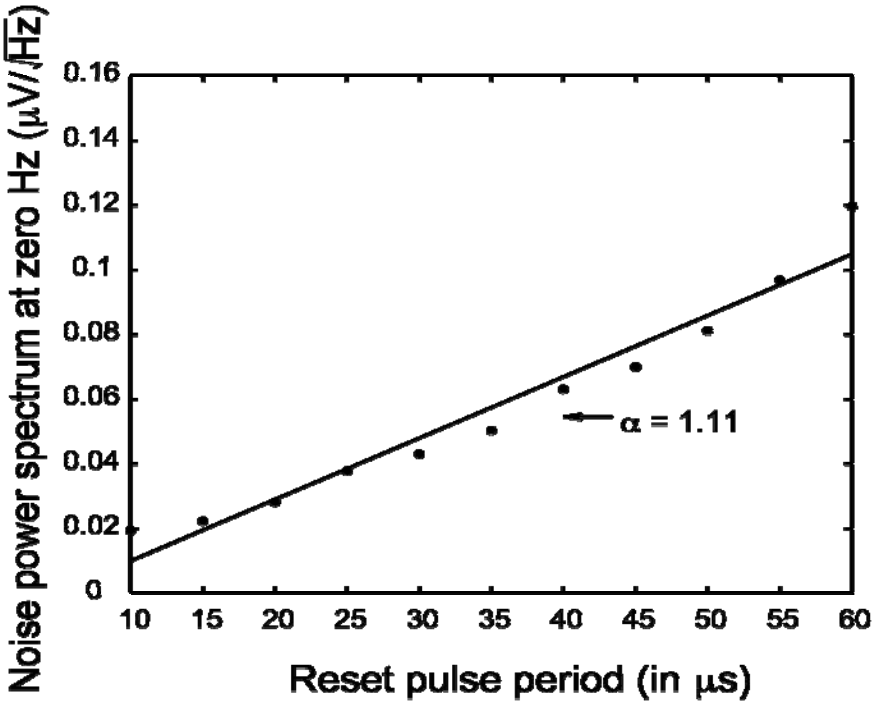

Figure 4-9: Noise power spectrum at zero frequency versus reset pulse for α extraction.

After the extraction of α and V_g, ω_f can be determined by using the measured data for f=0 for a single value of τ. Rearranging equation (4.40)gives

$$\omega_f = \frac{\alpha 4V_k^2(1+\zeta)}{V_n^2(0) - V_g^2 A_o^2 - \alpha 2V_k^2 \tau \zeta^2}. \tag{4.43}$$

It is also noted that ω_f provides information about the reset speed and thus measures the degree of correlation of consecutive resets.

Figure 4-10 illustrates the measurement of reset noise using the setup in Figure 4-7. The power spectrum is measured for a duty cycle of 10% and a reset pulse width of 10 ms. Here, with the extracted parameters mentioned earlier, the experimental data is plotted against the model and shows reasonable agreement. Larger discrepancy between model and theory is observed near the harmonics of the reset pulse (~100 Hz) and is due to clock feed-through of the reset TFT.

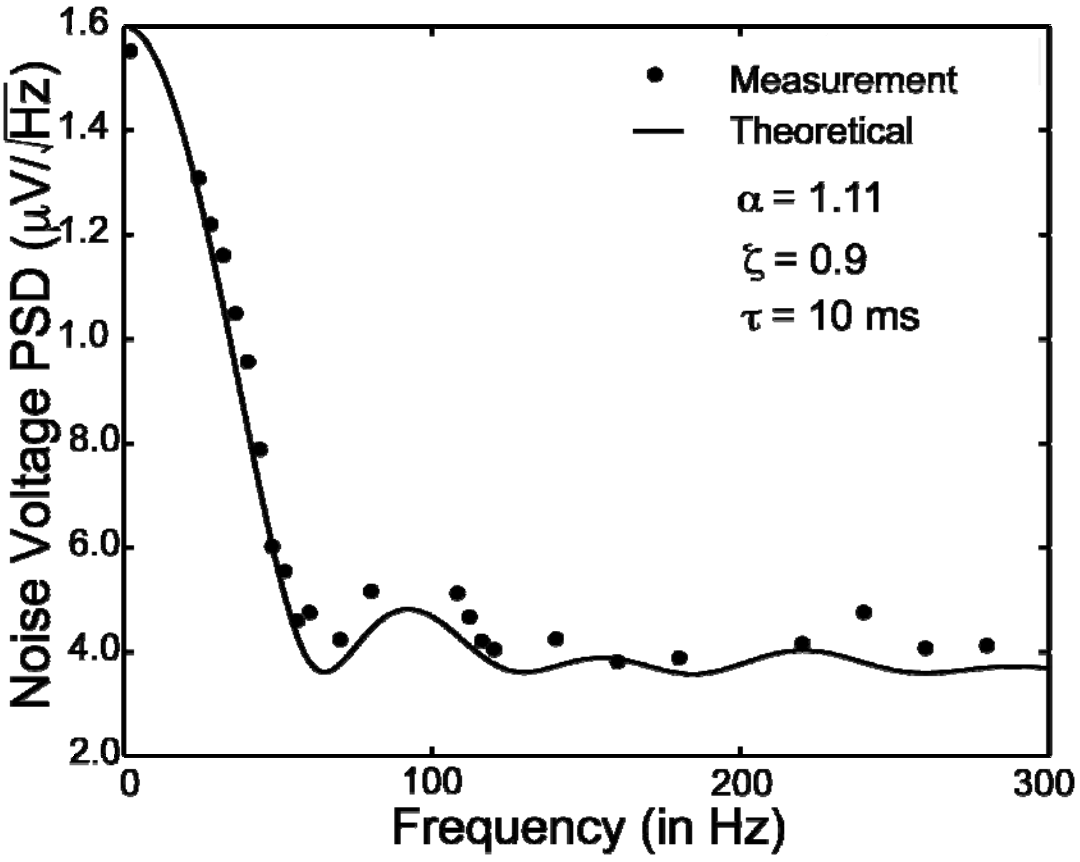

Figure 4-10: Reset noise measurement results.

In diagnostic medical imaging, the array readout is typically performed sequentially, resulting in a small duty cycle (~0.1%). Evidently, duty cycle influences the shape of the PDF as shown in Figure 4-11. Note that as the reset pulse duty cycle is increased (from 10% to 30%), the noise tends to spread out in frequencies and the noise at zero frequency is reduced. This behavior can be explained as the signal sampling deviates further from an ideal impulse response, the noise observed approaches the thermal noise flat spectrum. In other words, it is of best interest to operate the array in small duty cycles and use low pass filtering circuit (such as CDS) to suppress reset noise.

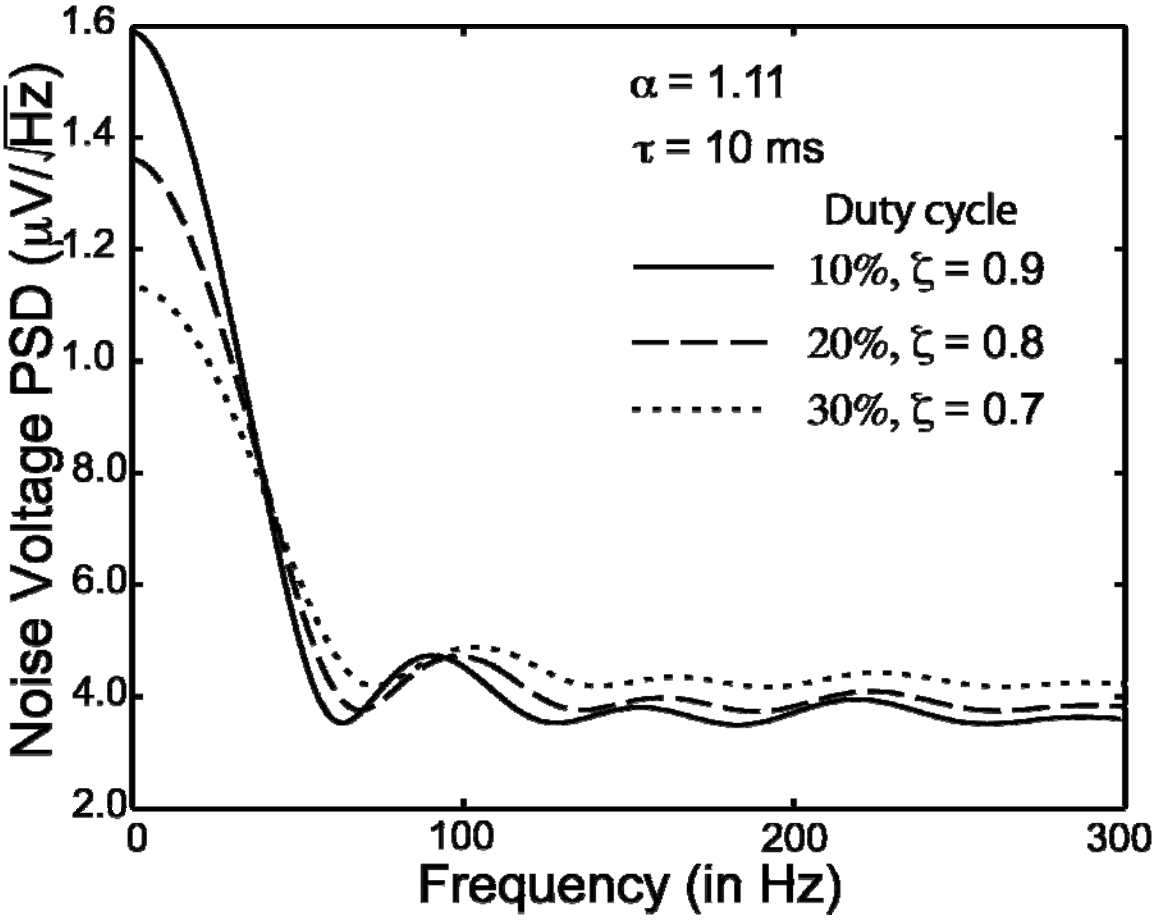

Figure 4-11: Reset noise PDF with various duty cycles.

4.4 Partition Noise

Teranishi and Mutoh observed a noise component related to the fall times of applied gate pulse and is in conjunction with reset noise at the integration node of a sensor element in 1986[94]. This noise is treated as a spurious noise component by Hynecek [93] in his reset noise analysis. The parameter α introduced earlier for the reset noise analysis is typically extracted and is great than unity, suggesting the existence of a noise source that is not explained by the reset noise model.

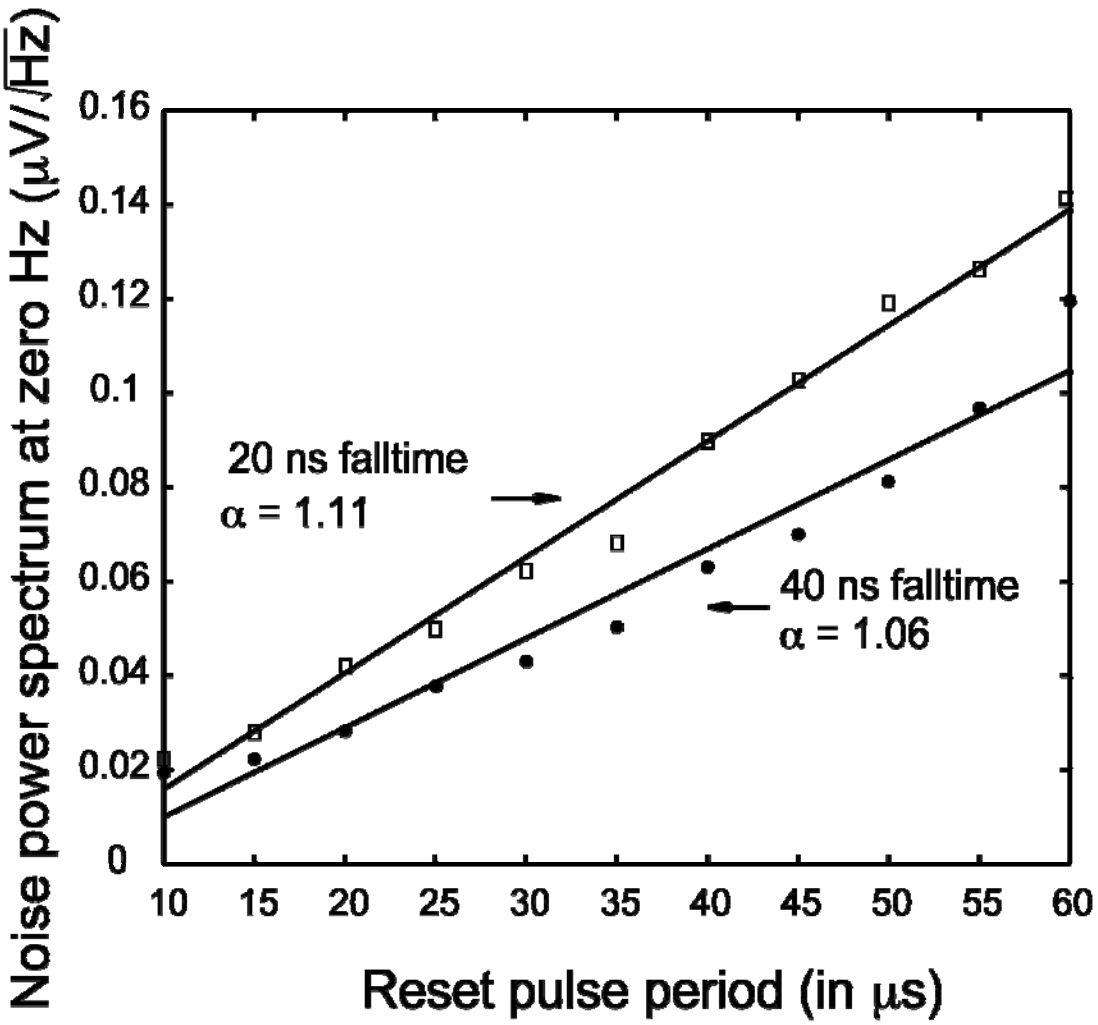

Figure 4-12: Reset and partition noise from α extraction.

Figure 4-12 illustrates the α extraction for two gate pulse fall times and clearly shows a dependency. A faster fall time results in a steeper sloop, hence a higher value of α. This noise component is termed partition noise by Teranishi and Mutoh [94] and related to the stochastic nature of channel charge evacuation during transistor turn off.

As transistor is turned off, electrons under the gate that form the channel have to quickly transit to the source and drain. This mechanism is consistent between CMOS MOFSET and TFTs. However, the evacuation of these electrons cannot be accomplished

instantly and more importantly; it is not always due to carrier drift. Initially, the evacuation mechanism is drift due the externally applied bias across source/drain. The dominant mechanism for carrier movement switches from drift to diffusion as the gate potential reduces and the time taken for this transition decreases with faster fall times. Diffusion is dependent on the carrier gradient and mobility, and is comparatively much slower [99]. So a faster fall time results in a higher amount of residual charge, which has to be evacuated by diffusion. Furthermore, diffusion has an associated noise component due to the non-deterministic behavior of charge diffusion, and manifests itself between successive resets. Thus, a faster time results in higher noise [94][95][96]. Consequently, both the drift and diffusion components of the electron current have to be considered at all times in order to accurately estimate the charge profile. The charge profile estimation method for reset operation is documented in the Appendix and the work has been published by the author in [95][96][97][98].

Teranishi and Mutoh developed an equation for the noise associated with charge partition noise based on probability theory [94],

$$n_{partition}^2 = \int_0^L n(x) P_L(x) P_R(x) dx, \tag{4.44}$$

where

$$P_L(x) = 1 - \frac{x}{L}, \tag{4.45}$$

and

$$P_R(x) = \frac{x}{L}. \tag{4.46}$$

Here, the integration variable x denotes the position under the gate with x = 0 denoting the source edge and x = L the drain edge of the channel, n(x) the electron carrier concentration, and P_L and P_R the position-dependent probabilities that an electron will move to the left or the right (drain and source), respectively. The carrier concentration n(x) has been assumed constant along the channel even at the onset of transistor pinch-off [94]. This assumption leads to an underestimation of partition noise because it does not consider the location-dependence of channel charge profile. Hence, it is recommended o utilize the developed model in the Appendix to estimate the charge distribution. Equation (4.44) can then be numerically integrated to obtain the charge partition noise.

Figure 4-13 shows two noise power spectra of the same reset configuration with 20 ns and 40 ns fall time respectively. The 20 ns fall time gate pulse generates a PDF that is shifted upwards in comparison with the PDF with a 40 ns gate fall time gate pulse. Modeled data agrees within 15% of the model estimation in both scenarios.

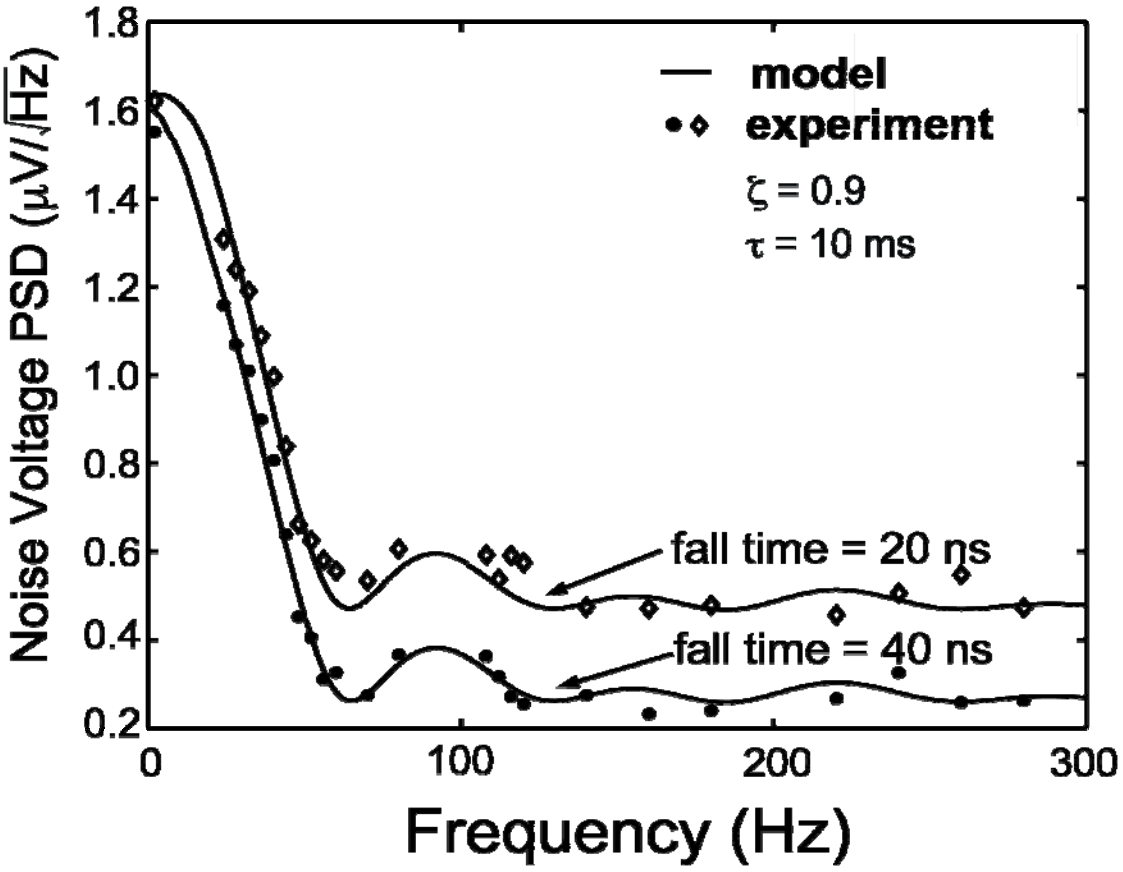

Figure 4-13: Noise power spectrum for different gate pulse fall times.

The difference in the two power spectra demonstrates the effect of charge partition noise. As the gate fall time increases, there are more channel charge left to be evacuated through diffusion. While the total amount of channel charge is deterministic as predicted by charge feed-through analysis, the diffusion of residual channel charge is random and presents itself as partition noise. To further investigate the magnitude and possible trend of partition noise in a-Si:H TFT, the gate pulse fall time is varied and the partition noise component is found as shown in Figure 4-14 for a 21 pF capacitive node.

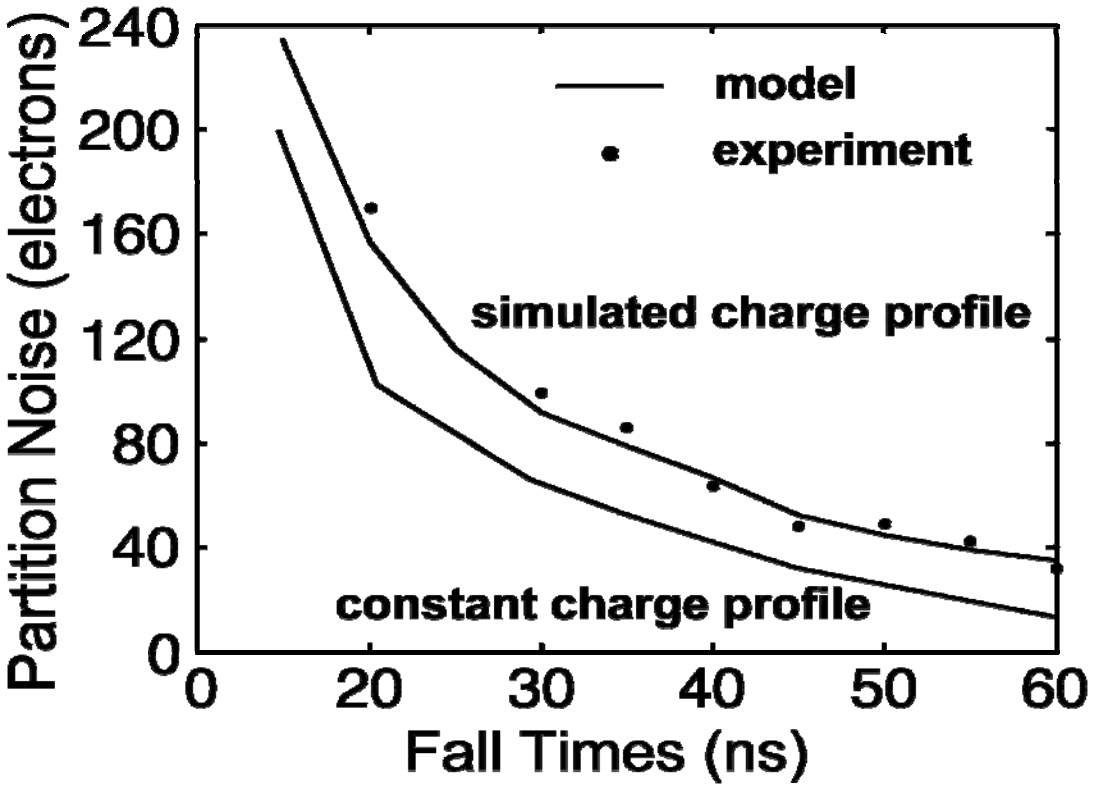

Figure 4-14: Partition noise trend for transistor reset operation.

Evidently, the partition noise component increases as the fall time decreases. The trend agrees with the prediction and model proposed by Hynecek and Teranishi and Mutoh [93][94]. The model is extended and predicted a charge partition noise of over 500 electrons for fall times less than 20 ns. It is noted the partition noise originates from channel charge evacuation, and thus it does not scale with integration node capacitance as in the case of reset noise. In other words, increasing the reset node capacitance will increase reset noise while partition noise is left relatively unchanged, hence the lower α parameter. From equation (4.44), it is intuitive that the channel charge scales with TFT channel length L, leading to a higher partition noise.

Lastly, the improved charge profile simulation method in the Appendix is used and compared with the constant charge profile suggested by [94]. The improved model provides better agreement between theoretical and experimental data. The work is published for both CMOS image sensors and a-Si:H APS in [96][97].

For large area medical imaging arrays using a-Si:H technology, the noise requirement is approximately 1000 to 2000 electrons in order to provide sufficient signal-to-noise ratio for low dosage imaging. Partition noise, in comparison, do no present itself as a dominating noise contributor even for large TFT dimensions (W/L = 60/18). Smaller channel length TFTs can be design to further suppress partition noise and is associated with faster reset speed. Nevertheless, partition noise contributes to the total noise as seen by readout electronics and should be carefully considered for low-noise panel design and optimization.

4.5 Noise in Pixel Circuits

The various noise contributions in a-Si:H TFT have been individually considered and modeled in the previous sections. However, they are not sufficient to be used as pixel level noise analysis or providing a platform for circuit designs comparison. Since the operation of the pixel circuit have a strong influence in noise behavior, the combined noise contributions at different pixel operating schemes have to be individually analyzed.

Reviewing the pixel architectures in Chapter 3, it is recast that pixel operation is generally divided into three main sequences: Initialization, Integration, and Readout. In this section, the general noise equivalent circuits for the different phases are developed for the pixel circuits in Chapter 3. Then the power spectral densities modeled described in

this chapter will be extended and combined with the equivalent circuits to arrive at analytical expressions for circuit noise performance. Measurement results are compared against theoretical models here to draw some insights in H-APS' improvements over APS designs. The systematic approach presented in this chapter also provides a gateway for design optimization for achieving high signal-to-noise ratio (SNR). This subject is discussed and studied at the end of this section. It is noted the vast similarity between APS and H-APS with dual readout, thus the analysis is focused on H-APS with global shutter. The derived models are simplified for APS (and H-APS with dual readout) for comparison.

4.5.1 Noise Equivalent Circuits

Initialization:

During the pixel initialization phase, only the RESET and TRANSFER TFTs are considered and the simplified circuit is shown on the left hand side in Figure 4-15. The potentials at the sense and storage nodes (V_{SENSE} and V_{STORE}) rarely drops over a few hundred milli-volts, thus it is justified to assume both RESET and TRANSFER are operating in the linear regimes due to small drain-source voltages. The small signal equivalent circuit is displayed in the right hand side of Figure 4-15 where i_{n_RESET} and $i_{n\_TRANSFER}$ denotes the noise currents from the RESET and TRANSFER TFT respectively. The TFT drain-source resistance is represented by $r_{ds} = \frac{dI_{DS\_linear}}{dV_{DS}}$ and is approximated as $\left[\mu_{EFF} C_G \frac{W}{L} \left(V_{GS} - V_T - V_{DS} \right) \right]^{-1}$ in the linear regime.

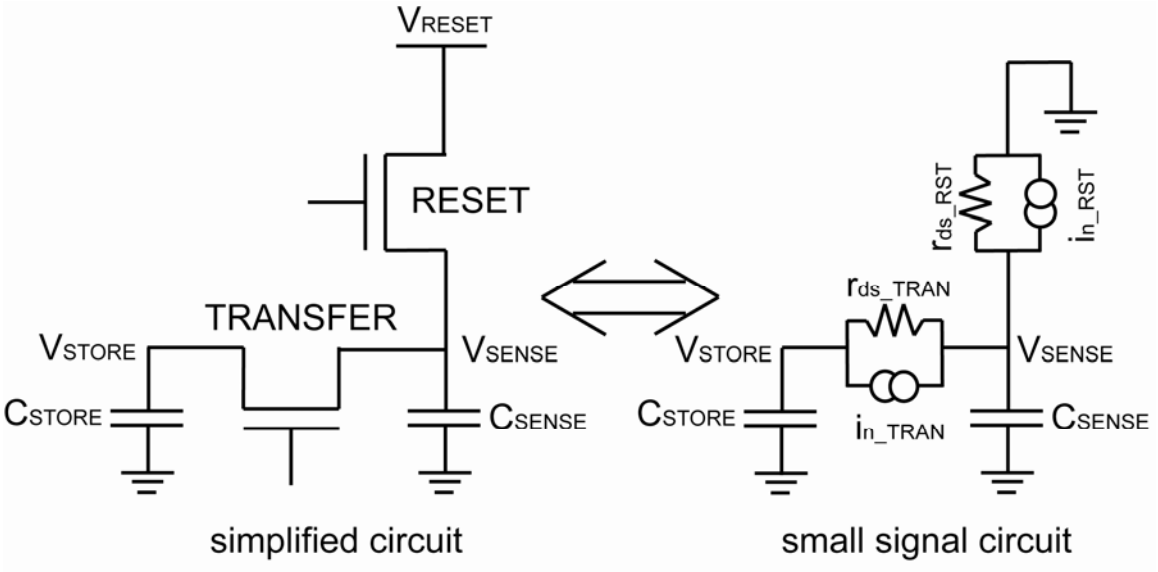

Figure 4-15: Simplified and small signal equivalent circuit for initialization phase.

Performing circuit analysis in frequency domain on the small signal circuit schematic and express the sense node voltage in terms of noise currents gives

$$V_{SENSE}\left[\frac{\left\{r_{ds\_RST}+sC_{SENSE}r_{ds\_TRAN}r_{ds\_RST}+r_{ds\_TRAN}\right\}\left(sC_{STORE}r_{ds\_TRAN}+1\right)-r_{ds\_RST}}{r_{ds\_RST}r_{ds\_TRAN}\left(sC_{STORE}r_{ds\_TRAN}+1\right)}\right] \quad (4.47)$$
$$=i_{n\_RST}-i_{n\_TRAN}\frac{sC_{STORE}r_{ds\_TRAN}}{sC_{STORE}r_{ds\_TRAN}+1}.$$

Equation (4.47) gives the noise voltage at the sense node, however, it is too complicated and is simplified to provide some insights. Firstly, the operating frequency is assumed to be smaller (at least an order of magnitude) than pole frequency created by the RC product of TRANSFER TFT on resistance and C_{STORE}, i.e. $s \ll \frac{1}{C_{STORE}r_{ds\_TRAN}}$. Secondly, the two noise sources i_{n_RST} and i_{n_TRAN} are un-correlated. Equation (4.47) can then be simplified to

$$V_{SENSE} = r_{ds\_RST}\left[i_{n\_RST} - si_{n\_TRAN}C_{STORE}r_{ds\_TRAN}\right]. \quad (4.48)$$

If both TFTs in this phase have similar TFT dimensions and noise performance, it is clear that the component with i_{n_TRAN} is reduced by applying $s \ll \frac{1}{C_{STORE}r_{ds\_TRAN}}$. The entire term with i_{n_TRAN} can be reasonably ignored. Thus, the voltage spectral density becomes

$$S_{V_{SENSE}} = r_{ds\_RST}^2 S_{n\_RST}. \quad (4.49)$$

Integration:

During the signal integration phase, all TFTs except TRANSFER are turned off in the H-APS design. The TRANSFER TFT is biased at the subthreshold regime where drain-source potential is signal dependent. Here, the flicker noise of the TRANSFER TFT is the main contributor. With a small gate voltage combining with a small V_{DS} for the TRANSFER TFT, the 1/f component becomes insignificant and can be neglected.

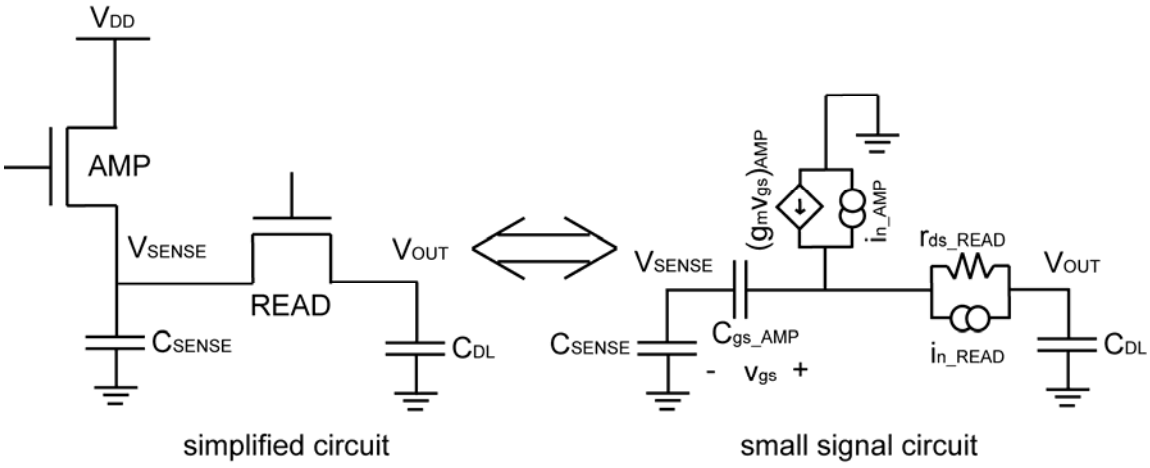

Figure 4-16: Simplified and small signal equivalent circuit for readout phase.

Readout:

The equivalent circuit and small signal schematics are shown in Figure 4-16. The data line capacitance is denoted as C_{DL} and is the distributed contributions of all the connecting TFT gate-source overlap parasitic capacitances. In this phase, the AMP TFT is operating in saturation while the READ TFT in linear. Hence, the small signal schematic of the simplified circuit can be obtained (shown in right half of Figure 4-16). The TFT noise sources are represented by i_{n_READ} and i_{n_AMP} for READ and AMP TFT respectively. Similar to the initialization phase, circuit nodal analysis in the frequency domain can be performed here and yield

$$V_{OUT} = \frac{g_{ds\_READ} i_{n\_AMP}\left(C_{SENSE} + C_{gs\_AMP}\right) + i_{n\_READ}\left(g_{m\_AMP} C_{SENSE} + sC_{SENSE} C_{gs\_AMP}\right)}{\left[\begin{array}{l} g_{m\_AMP} g_{ds\_READ} C_{SENSE} \\ +s\left(g_{m\_AMP} C_{PIX} C_{DL} + C_{SENSE} C_{GS\_AMP} g_{ds\_READ} + C_{SENSE} g_{ds\_READ} C_{DL} + C_{gs\_AMP} g_{ds\_READ} C_{DL}\right) \\ +s^2\left(C_{SENSE} C_{gs\_AMP} C_{DL}\right) \end{array}\right]}. \quad (4.50)$$

Assuming that the data line capacitance is significantly larger than the pixel sense node and the gate-source overlap capacitances ($C_{DL} \gg C_{SENSE} \gg C_{gs\_AMP}$), and $s \ll \frac{g_{m\_AMP}}{C_{gs\_AMP}}$, equation (4.50) can be simplified as

$$V_{OUT} = \frac{i_{n\_AMP} R_{eq\_AMP} + i_{n\_READ} r_{ds\_READ}}{1 + j\left(\frac{\omega}{\omega_{eq}}\right)}, \quad (4.51)$$

where ω_{eq} is the bandwidth of the composite AMP and READ amplifier circuit, and

$$R_{eq1} = \frac{C_{SENSE} + C_{gs\_AMP}}{g_{m\_AMP} C_{SENSE}}, \text{ and } \omega_{\text{eq}} = \frac{1}{C_{DL}} \cdot \frac{g_{ds\_READ} g_{m\_AMP}}{g_{ds\_READ} + g_{m\_AMP}}. \tag{4.52}$$

It is again reasonable to assume the two noise sources are un-correlated, giving the voltage spectral density as

$$S_{V_{OUT}} = \frac{S_{n\_AMP} R_{eq1}^2 + S_{n\_READ} r_{ds\_READ}^2}{1 + \left(\frac{\omega}{\omega_{eq}} \right)^2}. \tag{4.53}$$

4.5.2 Noise Model for Pixel Sensors

The voltage spectral densities in equations (4.49) and (4.53) for initialization and readout phases provide generic equivalent noise expressions regardless of which noise component is under consideration. Here, each type of noise is considered and combined with the derived expressions to obtain specific noise spectral densities.

For thermal noise, the noise variance can be computed using the spectral densities for TFT in linear and saturation regimes. In the initialization phase, the sampling action of RESET transistor and thermal noise gives rise to reset noise and is considered separately. For readout phase, the noise variance becomes

$$\sigma_{readout}^2 (th) = \left(f_{eq} \cdot \frac{\pi}{2} \right) \left(R_{eq1}^2 a_{th\_AMP} + r_{ds\_READ}^2 a_{th\_READ} \right) \tag{4.54}$$

where $a_{th\_AMP} = \frac{8}{3} kTg_{ds\_AMP}$ and $a_{th\_READ} = 4kTg_{ds\_READ}$ follows the definitions in section 4.1 and $f_{eq} = \frac{\omega_{eq}}{2\pi}$ is the bandwidth of the composite amplifier circuit.

For flicker noise, the voltage spectral densities need to be integrated in frequency between f_L and f_H, which represents the low and high cut off frequency of the circuit. For initialization phase, f_L is defined by the on time of RESET TFT, while f_H is limited by the noise bandwidth of the composite source follower amplifier stage. For readout phase, f_L is set to an arbitrary observation frequency f_{obs} [84]. High cut off frequency is set to infinite, even though in practical imaging array it is limited by the charge amplifier noise bandwidth. The flicker noise variances for different phases becomes

$$\sigma^2_{initialization}(fl) = r^2_{ds\_RST} a_{fl\_RST} \ln\left(f_H - f_L\right), \tag{4.55}$$

where

$$\sigma^2_{readout}(fl) = \frac{\left(R^2_{eq1} a_{fl\_AMP} + r^2_{ds\_READ} a_{fl\_READ}\right)}{2} \ln\left(1 + \frac{f^2_{eq}}{f^2_{obs}}\right), \tag{4.56}$$

where a_{fl} for linear and saturation regimes are discussed in section 4.2 and recast here for convenience,

$$a_{fl\_linear} = \alpha_H \frac{q\mu_{EFF}}{L^2}\left[K\left(V_{GS} - V_T\right)^n V^2_{DS}\right], \tag{4.57}$$

and,

$$a_{fl\_saturation} = \alpha_H \frac{q\mu_{EFF}}{L^2}\left[K\left(V_{GS} - V_T\right)^{n+2}\right]. \tag{4.58}$$

As briefly discussed earlier, thermal noise during the initialization phase is sampled by the reset operation. The generated noise is stored in the pixel capacitance

C_{SENSE} and since this originates from the sampling action, it does not follow the voltage spectral density derived from nodal analysis in equation (4.49). The reset noise variance is given by

$$\sigma_{reset}^2 = \frac{kT}{C_{EFF}}, \tag{4.59}$$

where C_{EFF} is the effective capacitance as seen by the gate of the AMP TFT. The effective nodal capacitance comprises of both the sense and storage capacitances and also the parasitic capacitances from the TFTs, and is

$$\begin{aligned} C_{EFF} &= C_{SENSE} + C_{STORE} + C_{ch\_TRAN} + C_{gs\_TRAN} \\ &+ C_{gd\_TRAN} + \frac{1}{2}C_{ch\_RESET} + C_{gs\_RESET} \\ &+ C_{ch\_AMP} + C_{gd\_AMP} + (1 - A_{V0}C_{gs\_AMP}). \end{aligned} \tag{4.60}$$

Here, the gate-source capacitance of the amplifier transistor needs to be reflected back to the gate of the AMP TFT. The DC gain of the circuit A_{V0} can be obtained from nodal analysis and is

$$A_{V0} = \frac{g_{m\_AMP}\left(g_{ds\_READ} + g_{DL} + g_{m\_READ}\right)}{\left(g_{ds\_READ} + g_{m\_READ} + g_{DL}\right)\left(g_{ds\_AMP} + g_{m\_AMP} + g_{ds\_READ}\right) - \left(g_{ds\_READ} + g_{m\_READ}\right)g_{ds\_READ}} \tag{4.61}$$

where $g_{DL} = \frac{1}{R_{DL}}$ is the data line resistance.

The various noise sources are tabulated in table below for easier reference.

Table 4-4: List of noise sources for H-APS.

Initialization phase	
Reset noise	$\sigma^2_{reset} = \frac{kT}{C_{EFF}}$,
Flicker noise	$\sigma^2_{initialization}(fl) = r^2_{ds\_RST} a_{fl\_RST} \ln(f_H - f_L)$,
Readout phase	
Thermal noise	$\sigma^2_{readout}(th) = \left(f_{eq} \cdot \frac{\pi}{2}\right)\left(R^2_{eq1} a_{th\_AMP} + r^2_{ds\_READ} a_{th\_READ}\right)$
Flicker noise	$\sigma^2_{readout}(fl) = \frac{\left(R^2_{eq1} a_{fl\_AMP} + r^2_{ds\_READ} a_{fl\_READ}\right)}{2} \ln\left(1 + \frac{f^2_{eq}}{f^2_{obs}}\right)$,

4.5.3 Data Line Noise

In imaging array, the data line is commonly shared between all the pixels in the same column. The data line parasitic resistance (R_{DL}) and the capacitance (C_{DL}) not only provide a low pass filtering action to signal readout, it also contributes to thermal noise.

Figure 4-17 shows the equivalent circuit for data line thermal noise where the distributed contribution of R_{DL} and C_{DL} are divided into segments corresponding to the number of pixels in the column. In other words, $R_{DL(1)} + ... + R_{DL(n)} = R_{DL}$ and $C_{DL(1)} + ... + C_{DL(n)} = C_{DL}$.

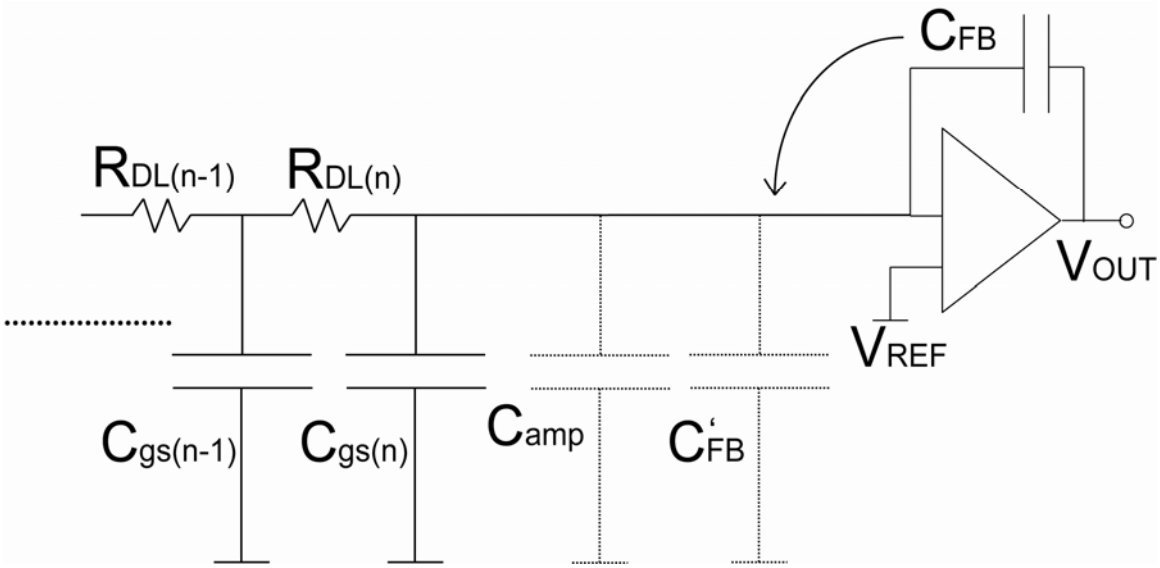

Figure 4-17: Distributed data line resistance and capacitance for noise analysis.

The amplifier input capacitance and $C_{FB}^{'}$ are bypassed by the virtual ground from the positive terminal of the charge amplifier, so these two capacitors do not store the thermal noise charge. Rather, the noise is stored in the rest of the capacitors, and the noise variance is given by

$$\sigma_{DL\_th}^2 = \frac{\pi f_o}{2} 4kTR_{DL}. \tag{4.62}$$

where f_o is the amplifier noise bandwidth. The validity of the amplifier noise bandwidth limitation is reasonable because the corner frequency imposed by R_{DL} C_{DL} is typically much smaller than that of the amplifier. This assumption is contrary to the TFT thermal noise analysis where the noise bandwidth is bottle-necked by composite AMP and READ TFT or the pixel time constant.

4.5.4 Charge Amplifier Noise

The presence of the charge amplifier at each column data bus not only amplifies the signal, it also provides a gain to associating noise. In other words, the amplifier noise and the gain to any input noise have to be considered. The schematic for the amplifier setup is shown in Figure 4-18.

The total input noise σ_{in} consists of amplifier input noise and the noise from the addressed pixel.

$$\sigma_{in} = \sqrt{S_{V_{amp}}^2 + S_{in\_tot}^2} \tag{4.63}$$

where $S_{V_{amp}}^2$ is the noise voltage input from the amplifier itself. Furthermore, the input output noise relationship of the amplifier is $\sigma_{in} = \frac{1}{G_n} \cdot \sigma_{out}$, and the gain G_n is function of line and feedback capacitance from simple capacitance divider, i.e.

$$G_n = \frac{C_{FB}}{C_{FB} + C_{DL}}. \tag{4.64}$$

Equation (4.64) demonstrates an interesting behavior between data line and the feed back capacitances. Although it is possible to increase the signal gain by reducing C_{FB}, it is accompanied by a higher noise gain.

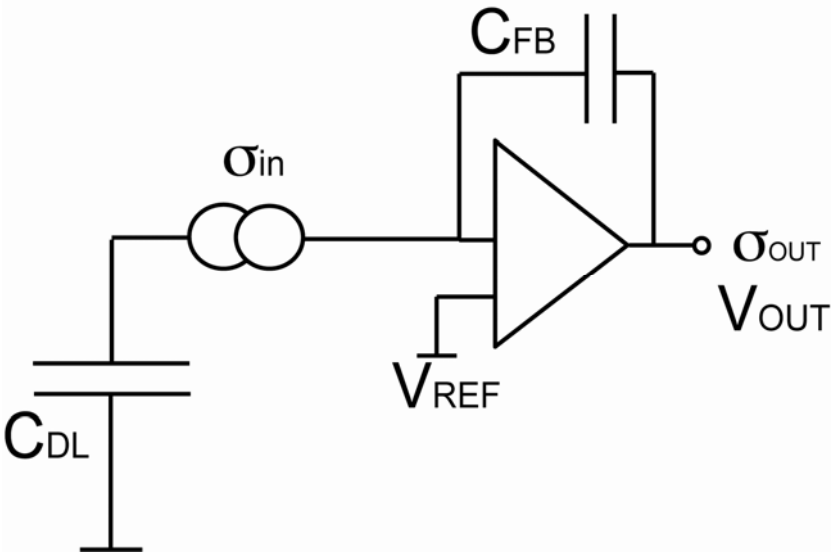

Figure 4-18: Charge amplifier schematic for noise analysis.

4.5.5 Input and Output Referred Noise

The various for noise discussed so far are assumed un-correlated, and they can be summed up in quadrature. The noise at the input of the charge amplifier is converted using the noise gain method discussed in the previous section. Hence,

$$\sigma_{OUT}^2 = A_V^2\left(\sigma_{reset}^2 + \sigma_{initialization}^2(fl)\right) + \left(G_n^2\right)\left[\sigma_{readout}^2(th) + \sigma_{readout}^2(fl) + \sigma_{amp}^2 + \sigma_{DL}^2(th)\right]. \quad (4.65)$$

The voltage gain A_V amplifies the reset and 1/f noise at the integration node to the output of the charge amplifier and is derived in Chapter 3 as

$$A_V = \frac{g_{m\_pixel}T_S}{C_{FB}}. \quad (4.66)$$

The incident input signal is in charge form, so it is customary to convert the total output noise variance σ_{OUT}^2 back to the sense node for SNR calculation. The input referred noise (at V_{SENSE}) can be computed from the pixel voltage gain,

$$\sigma_{input} = \frac{\sqrt{\sigma_{OUT}^2}}{A_V}. \tag{4.67}$$

The incident signal is typically quoted in number of electrons, thus it is beneficial to convert the noise variance into electrons for more direct comparison. It is noted the noise variance in electrons depends on the nodal capacitance, and are expressed as such [38]

$$\sigma_{OUT}(e) = \frac{\sqrt{\sigma_{OUT}^2} C_{FB}}{q}, \tag{4.68}$$

and

$$\sigma_{input}(e) = \frac{\sqrt{\sigma_{OUT}^2} C_{EFF}}{qA_V} = \frac{\sqrt{\sigma_{OUT}^2} C_{FB}}{qG_i} \tag{4.69}$$

where G_i is the charge gain of the pixel from the sense node to charge amplifier output.

4.5.6 Measurements and Discussions

First and foremost, the validity of the noise model present so far is verified through measurements with the H-APS with global shutter design. The measurement setup shown in Figure 4-1 is used where all V_{DD} , V_{TRAN} , V_{G_READ} ,and V_{G_RESET} are provided by low noise high amp hour batteries. The transimepdance amplifier provides gain to the

noise signal while the spectrum analyzer (HP4195A) measures the noise power. Similar to the technique for thermal and flicker noise, the measurements are performed at least 15 to 20 times and the narrowband data are averaged to reconstruct the noise power curves. The voltage biases are applied at least an hour prior to measurements in order to mitigate all transient effects, and the threshold voltage variation is monitored through the transimpediance input current meter. In addition, the system gain is measured (from AMP TFT gate to transimpediance amplifier output) over all the considered frequency to provide the proper noise extraction. The measurement results is shown in Figure 4-19 for an H-APS design with $C_{STORE} = 9.09$ pF and $C_{STORE} = 3.12$ pF .

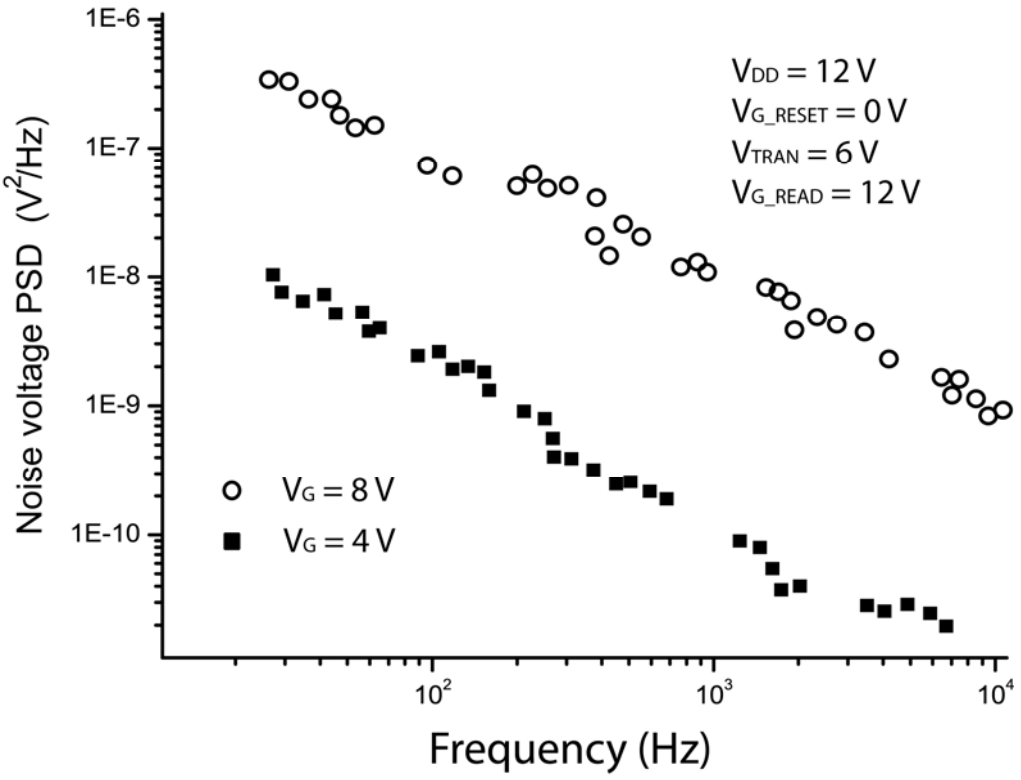

Figure 4-19: H-APS noise PSD for different AMP TFT gate bias.

With the $V_{G\_RESET} = 0$ V during the measurements, the reset and 1/f noise components from the RESET TFT is suppressed. It is clear that flicker noise dominates the total noise especially in the low frequency ranges. The results show reasonable agreement with the noise model with less than 19% of discrepancy. Note that the dependency on AMP TFT gate voltage, where a higher gate bias brings higher 1/f noise. In addition, thermal noise begins to drown out 1/f noise near 10 kHz, and for small gate bias ($V_{G\_AMP} = 4$ V) the 1/f slope starts to trail at approximately 4 kHz. This particular behavior is verified with 10 samples and has shown good consistency.

In practical imaging array scenarios, the RESET and READ TFTs are both pulsed, and this lead to a reduction in the 1/f noise component. However, the contribution of reset noise is likely to increase the total noise figure especially in the low frequency range as illustrated in the reset noise spectral analysis in section 4.3.

To investigate the noise performance difference between the H-APS design with global shutter and the conventional 3-TFT APS, the experimental data are compared between the two designs. Figure 4-20 shows the noise power curves for the two pixel designs. Evidently, both designs demonstrate the same behavior due to 1/f noise domination in low frequencies. It is also noted, even though APS generates less total noise, the difference between the two designs are minimal (with 8% difference). The TRANSFER TFT in H-APS contributes to flicker noise and thus helps to explain the stronger 1/f dependency. The larger difference near the higher frequency range (near 5 kHz) is possibly due to the thermal noise drown out effect that happens for APS at a lower frequency than H-APS.

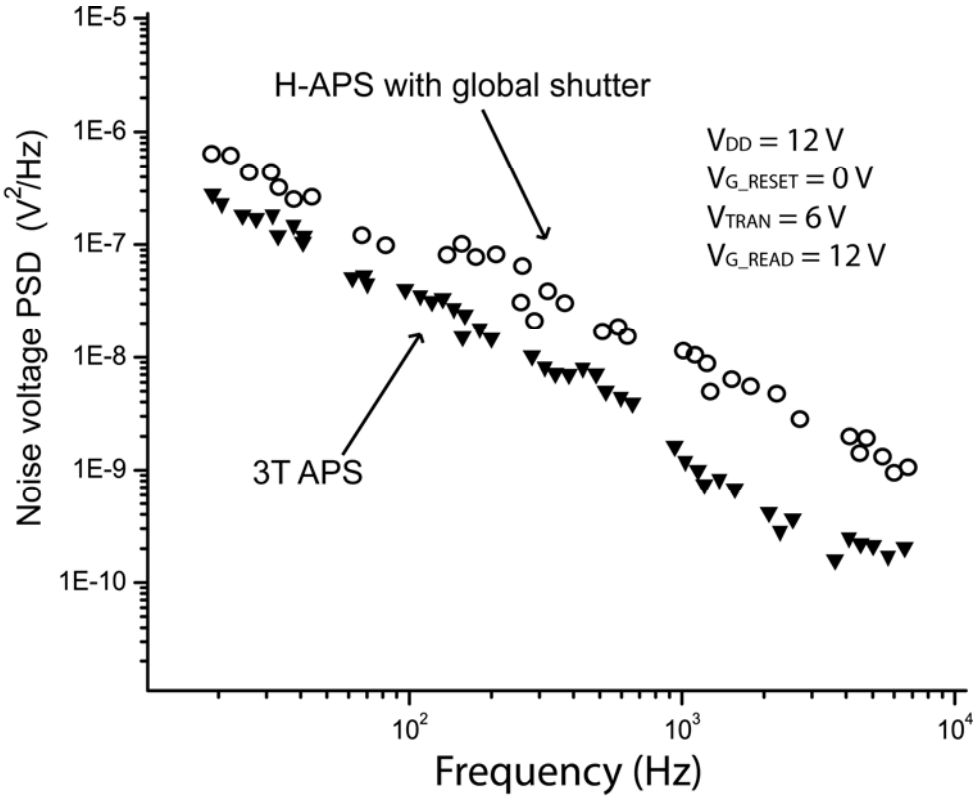

Figure 4-20: Noise PSD comparison between H-APS and 3-TFT APS.

The noise measurement is carried out for all the H-APS test samples with varying capacitance ratios. The amplifier and the test board appear to be the limiting factor in noise measurements. The noise stemming from the test fixture present itself as a noise floor, which prevents the accurate re-construction of noise power curves for devices with low noise performance. The noise performance of the test fixture is first measured separately using the spectrum analyzer and yields approximately 10^{-10} V^2/Hz output noise voltage. This observation is also confirmed via a digital oscilloscope through extracting the variance of the noise voltage on the test setup. Assuming the noise generated to be Gaussian in nature, the noise voltage can be fit to a normal distribution with a large number of measured samples. This measurement method of extracting output rms noise is

popularly used to measuring the noise performance of CMOS imagers [62]. Hence, only devices with large total capacitances are measured and are operated purposefully in higher noise configuration to cope with measurement limitation.

The input referred noise data for APS and H-APS designs with various capacitance ratios are tabulated in Table 4-5. Here, the APS design is compared against the H-APS design with $C_{STORE} = 3$ pF and $C_{STORE} = 1$ pF where the total noise is slightly higher (less than 10%). It is noted however, the high gain mode of H-APS provides 3 times higher signal conversion gain (C_{SENSE} is 1 pF instead of 3 pF). The H-APS designs with higher capacitance ratios are associated with higher noise, specifically in reset and flicker noise. This is largely due to a higher nodal capacitance (for reset noise), and the reduction in system gain due to capacitance loading in the pixel (for 1/f noise).

Table 4-5: Input referred noise for pixel circuits.

	APS	**H-APS**		
C_{SENSE} (pF)	3	1	3	3
C_{STORE} (pF)		3	3	9
Thermal	354	372	494	914
Flicker	673	780	939	1738
Reset	904	976	1068	1453
Total	1548	1642	1808	2640

4.5.7 Optimization

The analysis and measurements in the pervious sections have demonstrated reasonable accuracy in estimating both TFT and pixel circuit noise. The novelty in such exercise does not lie in the actual formulation, but in the general approach that provides the opportunity to systematically optimize pixel design for high performance.

Recalling that the pixel noise analysis begins with circuit nodal analysis, and then the expressions are combined with TFT level noise spectral density formulation. Such sequence of techniques can be performed by circuit simulator with proper TFT models. Thus, the approach opens the door to system and design optimization for a-Si:H pixel circuit. This section attempts to provide some insights in design optimization using the approach outlined in this chapter. The results of this noise analysis on specific pixel designs are published in [86] and the approach of noise analysis has lead to a US patent [87].

Optimization of pixel design involves analyzing the influence of several designs and operating parameters. The main parameters under investigation can be divided into three categories, TFT geometry, pixel biasing, and process improvements. The first two categories cover the benefits from variations of pixel design and operation details for a specific processing technology, while the study of key parameters related to process advancements provide an outlook to more long term performance trend.

Figure 4-21 shows the total noise plotted against varying AMP TFT channel width. Intuitively, a bigger AMP TFT width for a given READ TFT provides better noise

performance due to higher current drive leading to larger pixel gain. This benefit rapidly sets in when W_{AMP} is increased from 50 μm, but gain in performance starts to saturate near 110 μm. This is due to the increasing voltage drop across the READ TFT due to increasing I_{OUT} , acting as an inherent feedback system. In addition, the increasing contribution to C_{EFF} from larger AMP TFT also serves as a limitation to signal gain. The effect of larger C_{EFF} is mostly noticeable for W_{AMP} beyond 200 μm where the reset noise component becomes significant, resulting in the slight increase in total noise. From the results shown in Figure 4-21, it is recommended to choose a W_{AMP} anywhere between 100 to 130 μm, any further increase is not justifiable considering both gain and pixel area usage.

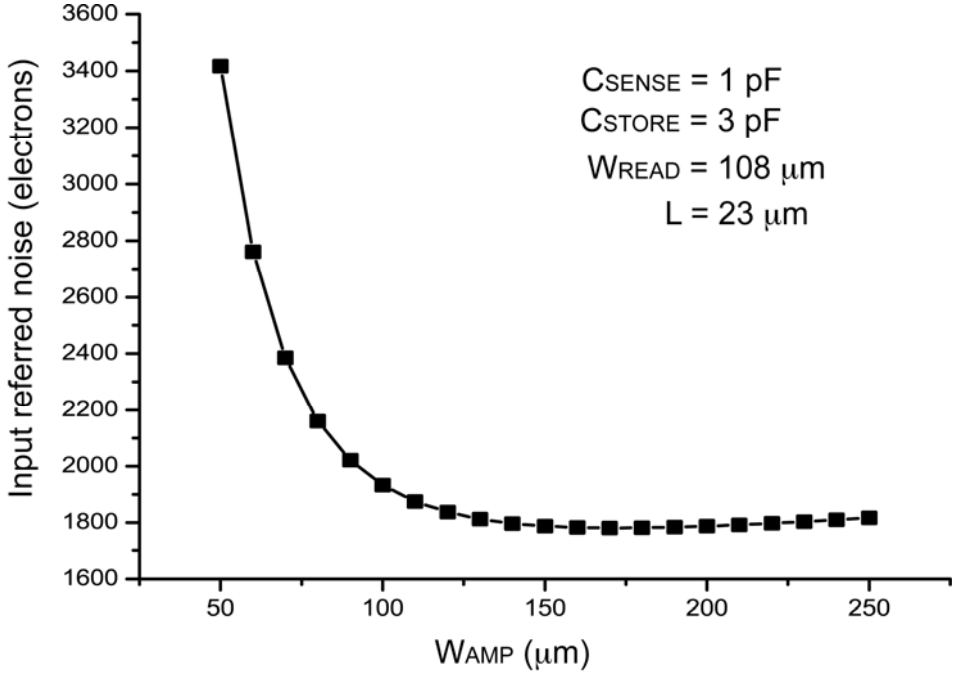

Figure 4-21: Total noise change with respect to AMT TFT width.

The system performance variation with respect to W_{READ} presents some interesting findings and the result is shown in Figure 4-22. Despite the small range of variation (less than 200 electrons), the input referred noise appears to have a local minimal when W_{READ} is varied. The input referred noise reduction ($50\ \mu m \le W_{READ} \le 150\ \mu m$) originates from the smaller on resistance across the READ TFT, thereby increasing I_{OUT} giving rise to a higher pixel gain. Further increasing W_{READ}, however, leads to a smaller V_{DS_AMP} and V_{GS_AMP}, pushing the AMP TFT away from the saturation region. This is illustrated in Figure 4-23 where the charge gain is plotted against W_{READ} and the validity of the prediction is verified with measurement results.

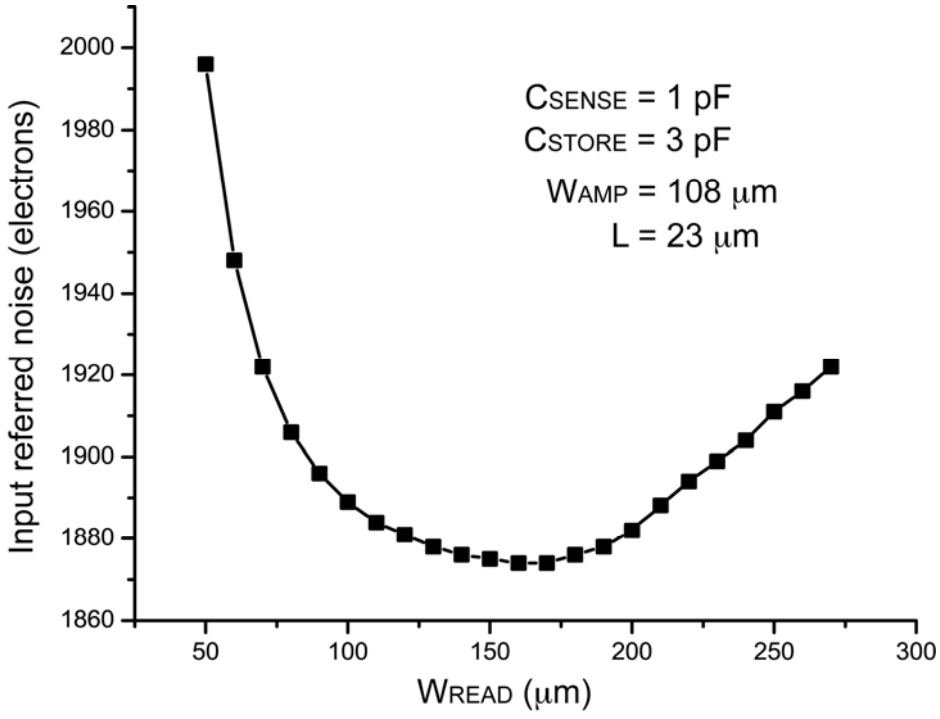

Figure 4-22: Total noise change with respect to READ TFT width.

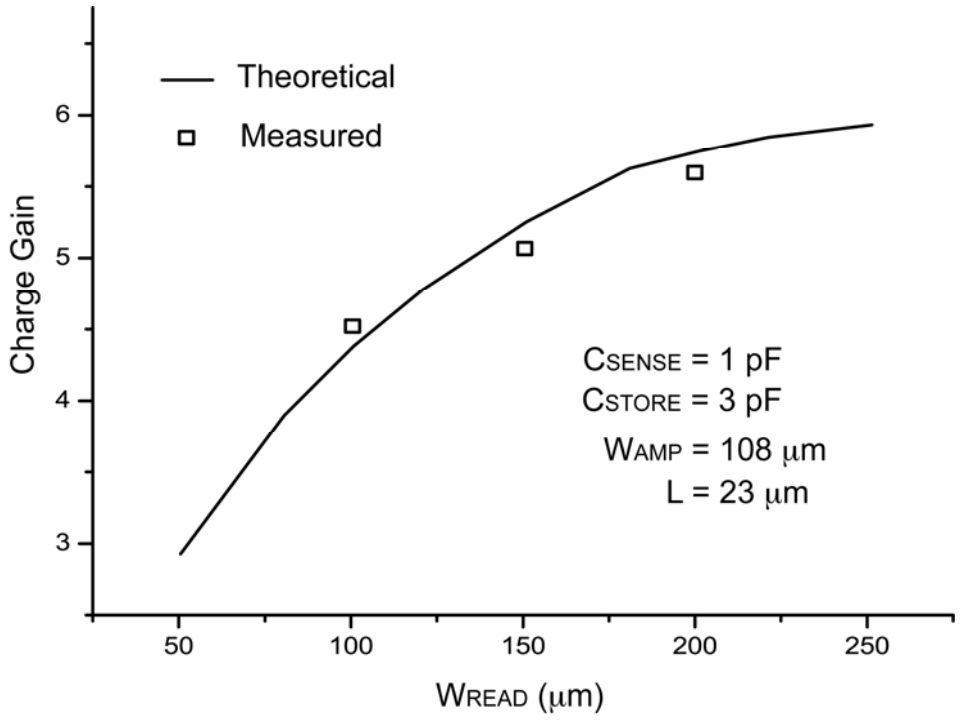

Figure 4-23: Charge gain variation with respect to READ TFT width.

The findings from Figure 4-22 entails a more in depth investigations into the design of READ TFT dimension. Here, the total noise is plotted against W_{READ} for different AMP TFT width in Figure 4-24. The local minimum behavior in total noise exists in the top two curves where W_{AMP} is 80 μm and 108 μm respectively. The local minimum for both cases appears to be limited by reset, and flicker noise at approximately 1800 noise electrons. On the other hand, the total noise reduces to below 1500 electrons for $W_{AMP} = 150\mu m$, by which the much higher current drive suppresses most noise except reset and amplifier noise. However, area usage for both $W_{READ,AMP} \geq 150\mu m$ precludes it to be used for many imaging applications when pixel pitch requirement is within 300^2 $(\mu m)^2$. Hence, the H-APS in this thesis is chosen to have dimensions $W_{AMP} = W_{READ} = 108\mu m$ to strike a balance between area usage and performance.

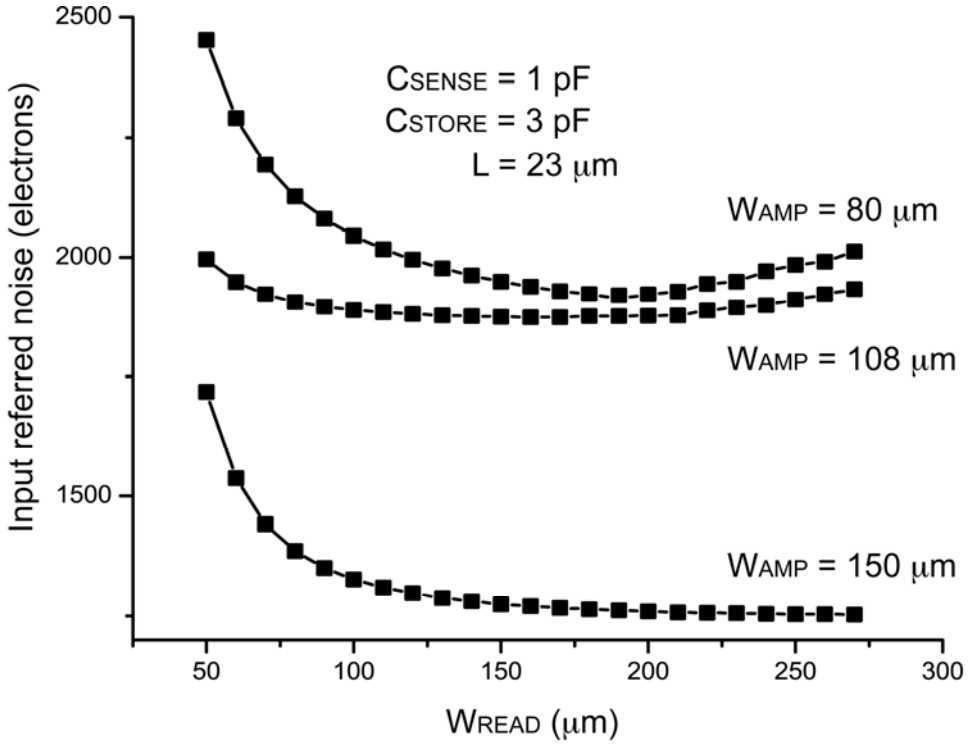

Figure 4-24: Total noise change with respect to READ TFT width and different AMP TFT width.

It is noted that the conclusion of having the same channel width for both AMP and READ TFT disagrees somewhat with intuition. It is customarily in CMOS imager design to minimize the aspect ratio of the READ transistor for leakage current purposes. This practice is not necessarily true for a-Si:H TFT arrays since the drain-source leakage current is low (~ fA/μm channel width), allowing flexibility to increase the READ TFT channel width for better performance.

Figure 4-25 shows the total input referred noise variation with respect to AMP TFT gate bias. It is noted that the AMP TFT gate bias is in fact the dc reset voltage of the integration node and is determined by V_{RESET} .A reduction in V_{G_AMP} results in lower noise and is in agreement with predictions for both thermal and flicker noise. The lower limit of

such bias reduction is the threshold voltage (V_T) of the AMP TFT, where $V_{GS\_AMP} \geq V_{T\_AMP}$ is needed. The source of the AMP TFT is determined by the operating point of the composite source follower circuit and is analyzed in section 3.2.2.3 and is typically around 1V, thus the AMP TFT seizes to operate for any V_{G_AMP} reduction beyond 3 V.

Next, Figure 4-26 shows the importance of choosing an appropriate charge amplifier feedback capacitance. It is restated that the feedback capacitance determines maximum allowable integration time at the output without saturation, meanwhile influences the noise gain. A large feedback capacitor (C_{FB}) alleviates both issues and is advisable as demonstrated.

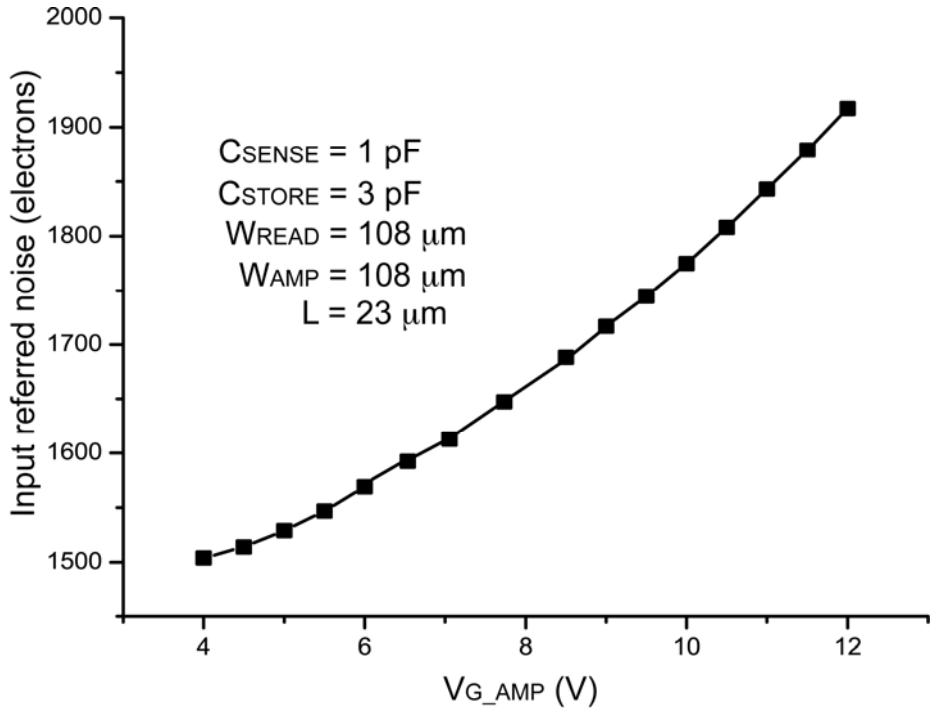

Figure 4-25: Total noise change with respect to AMP TFT gate bias.

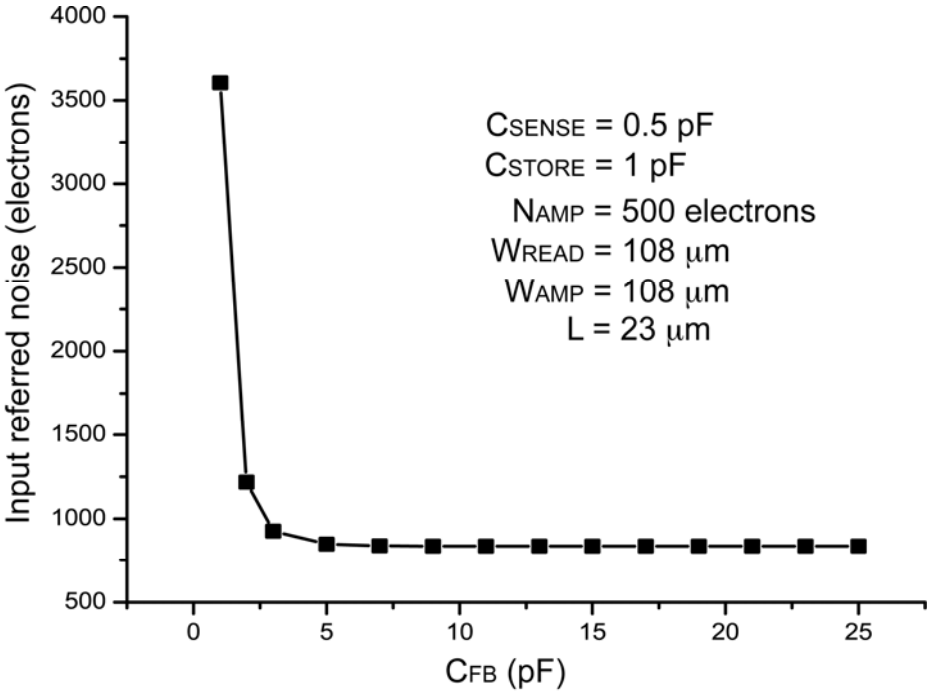

Figure 4-26: Total noise change with respect to charge amplifier feedback capacitor.

From the analysis thus far, it is evidently that higher TFT aspect ratios, and lower TFT operating voltages are desirable from system noise and signal gain perspective. Considering both threshold voltage and area usage limitations, it appears any improvements from processing technology advancement can potentially enable high performance pixel architecture. Figure 4-27 shows the noise performance trend with respect to channel length reduction. Here, the system is assumed to have a 0.5 pF sensing capacitance, a low noise amplifier (500 noise electrons), and the channel width on both AMP and READ to be 108 μm. Total input referred noise can be reduced to approximately 700 electrons which provides to be promising for low dosage imaging applications where x-ray quantum signal is as low as 1000 electrons.

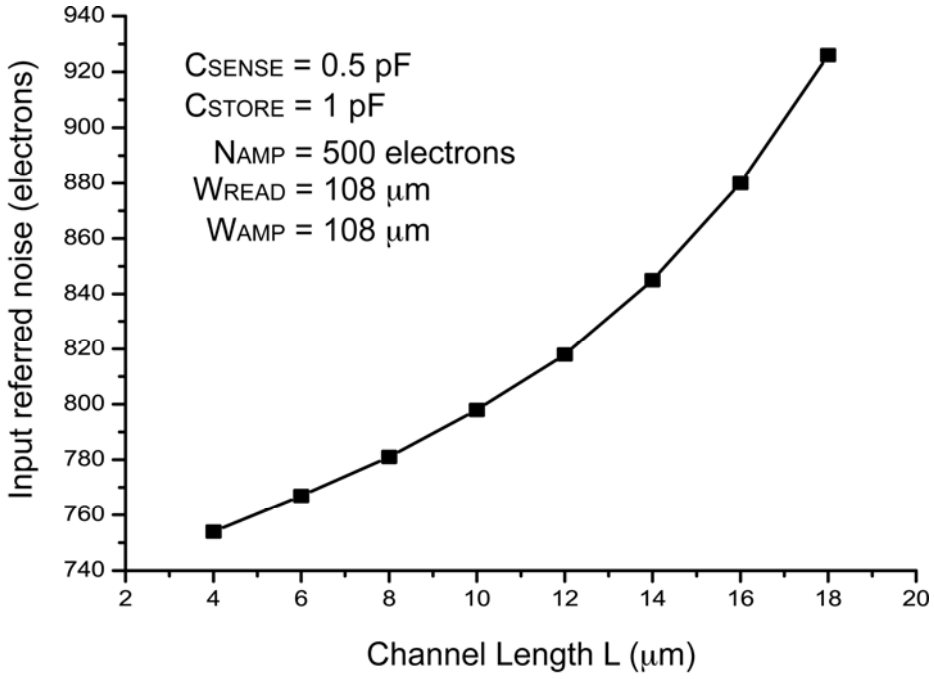

Figure 4-27: Change in input referred noise with channel length reduction.

Figure 4-27 demonstrates superior performances of the pixel circuit, which is largely due to capacitance reduction and the use of high performance low noise charge amplifier. To highlight the benefits of the H-APS design, the sense node capacitance is varied and a 1000 output noise charge amplifier is assumed. The total output noise and dynamic range plot is shown in Figure 4-28. Here, the noise and dynamic performances of the H-APS and APS are compared. Both designs demonstrate similar noise behavior, having a minimum noise of approximately 1500 electrons which is largely dominated by reset and amplifier noise. H-APS is clearly a close competition to APS by only having less than 8% of additional noise. The dynamic range of APS, as explained earlier in Chapter 3 decreases by almost two orders of magnitude with C_{SENSE} reduced from 8 pF to 0.5 pF while H-APS dynamic range stays relatively unchanged. It is noted that C_{SENSE} of less than 500 fF becomes comparable to the AMP TFT gate capacitance (~ 400 fF).

Hence, the need of an explicit capacitor is eliminated, and C_{EFF} solely comprises of nodal parasitic capacitance. This is in favor of pixel size reduction and fill factor maximization.

The implications of a stable dynamic range over sense node capacitance reduction combined with similar noise performance in comparison with APS design means the H-APS can provide high pixel performance without the need of drastic technology advancement. Even with existing state of the art a-Si:H TFT technology of L = 5-6 μm, pixel performance of under 1000 electrons with high dynamic range capability is achievable.

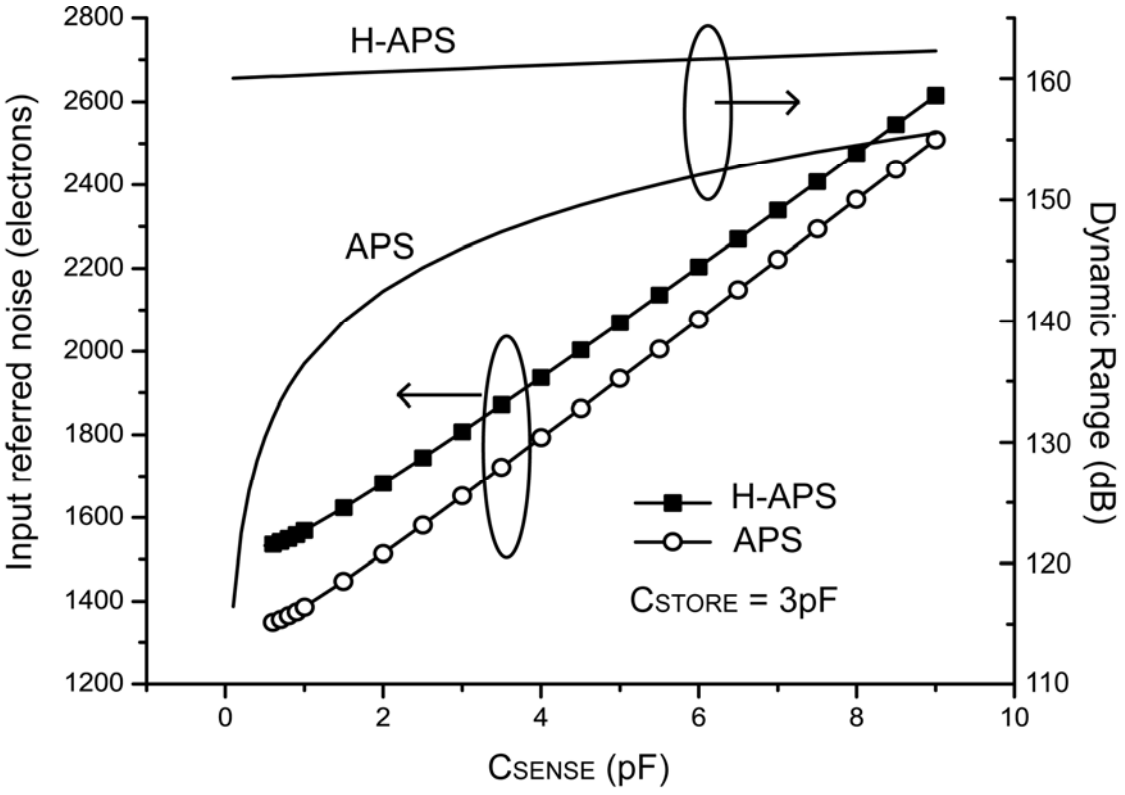

Figure 4-28: Input referred noise and dynamic range change with respect to sense node capacitance.

To summarize the analysis in this section, Table 4-6 is presented for H-APS fabricated with different processing technologies. The in-house fabrication facility can reliable reproduce a-Si:H TFT with 18 to 23 μm channel lengths while current state-of-the-art in the industry can be as low as 5 or 6 μm. Hence, channel length of 10 μm does not impose any processing challenge even for research facilities. The smaller critical dimension allows smaller TFT widths without sacrificing noise performance and dynamic range. H-APS design with total noise of 675 electrons appears to be promising for diagnostic medical imaging where low dosage input becomes the bottleneck (~ 1000 signal electrons).

Table 4-6: H-APS performance summary.

N_{AMP}(output) = 500 electrons C_{FB} = 3pF	L = 10 μm	L = 18 μm
$(W/L)_{AMP,READ}$	108/10	108/18
$(W/L)_{READ,TRANSFER}$	45/10	60/18
C_{SENSE} / CS_{TORE} (pF/pF)	0.5/0.5	1/1
Total noise (electrons)	675	943
Dynamic range (dB)	68.2	71.2
Charge gain	9.02	3.07
SNR (dB)	3.02	0.51

5 Pixel Integration

This chapter describes the integration of pixel architectures to from an image detector. The entire architecture that connects the TFT circuit to the photosensitive element impacts array performances through capacitive coupling, fill factor (consequently detector's quantum efficiency), and manufacturing yield. This chapter begins with a study of a few selective architectures and discussions on their respective impact on noise performances. Next, one pixel architecture is recommended and measurement results will be presented.

5.1 Co-planar Architecture

A conventional co-planar pixel process places the sensor and TFT beside each other on the imaging panel. A cross-sectional diagram for a conventional non-overlapped pixel process using an a-Si:H p-i-n photodiode appears in Figure 5-1 [88].

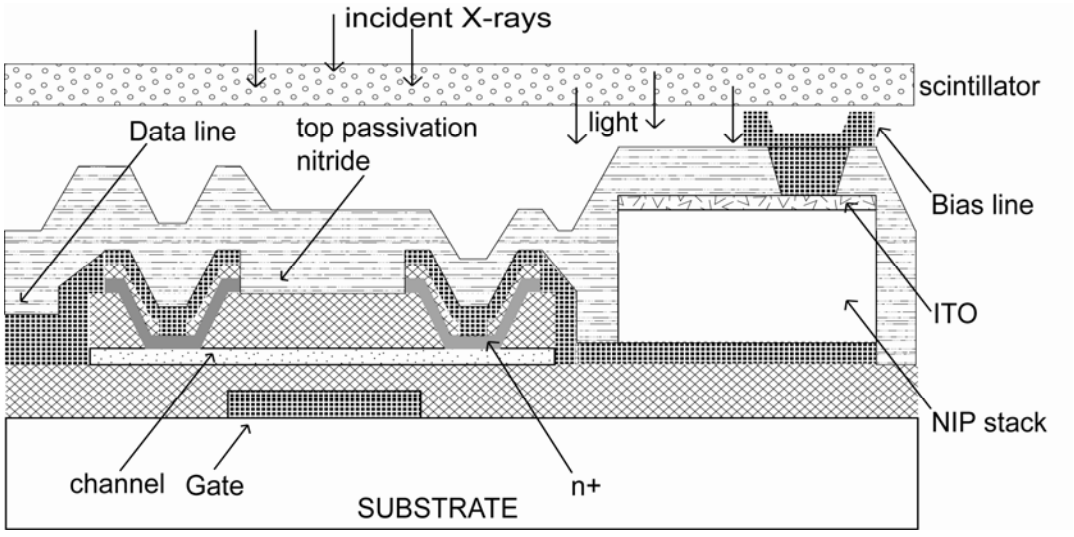

Figure 5-1: Co-planar pixel architectures

The in-pixel readout circuit, photodiode, and interconnecting metal lines together define the pixel pitch. Incident x-rays are converted into photons in the visible spectrum (~540 nm wavelength) by the scintillator and are subsequently detected by the photodiode. While this provides consistent manufacturing yield [88][89], the photodiode competes with the TFT and metal lines for pixel space, leading to a reduced pixel fill factor. The typically low fill factor in co-planar design serves as one of the bottlenecks for both high-resolution imaging and achievable signal-to-noise ratio.

Furthermore, since the signal and address lines are placed in the same plane as the photo-sensor and TFT, they are close to the substrate and are separated only by the thin CVD inter-layer dielectric. This results in high parasitic capacitive coupling either with the substrate or with cross-over gate lines [86], resulting in an increased data line capacitance (C_{DL}). Assuming good isolating between the data line and the photodiodes, C_{DL} mainly constitutes gate-source overlap capacitances from the READ TFTs and cross-over capacitances. For a 1000 x 1000 pixel array with 18 μm data and gate line metal width, the data line capacitance is approximately 135 pF for the co-planar architecture where the $C_{dielectric} = 25nF/cm^2$. As it shall be discussed later in this chapter that the increase in capacitance is coupled with higher data line thermal noise that impacts the overall performance. The co-planar architecture is used as a baseline for comparisons between pixel architectures in this section

5.2 High Fill Factor Architecture

The inherent architectural limitation in fill-factor for the co-planar design serves as the main reason for reduced signal collection efficiency and hence the bottleneck for the maximum achievable signal-to-noise ratio. An alternative approach is a vertically integrated high fill factor architecture where the photo-sensor (or photoconductor) is implemented as segmented [88] or non-segmented continuous layer [89]. Vertically integrated architectures increase the fill factor to alleviate the concern of signal collection efficiency, leading to better SNR that is crucial to applications with stringent signal specification.

5.2.1 Continuous Sensor

Continuous pixel architecture is distinctly different from co-planar architecture, and can be implemented to incorporate both direct and indirect x-ray detection schemes. The cross sectional diagram for the directly detection design is shown in Figure 5-2 while Figure 5-3 outlines a similar design for indirection scheme. In both architectures, the bottom mushroom electrode for the sensor/conductor defines the pixel pitch. The overlapping structure eliminates the pixel space sharing issues, and can theoretically achieve fill factor over 90%.

Direct detection scheme for x-ray imaging converts incident x-ray into electron-hole pairs, and provides some signal collection efficiency benefits over indirect detection scheme [90]. However, the use of photoconductors entails a large capacitance in the integration node for signal storage because incident signals are converted into current instead of charge. As explained earlier in Chapter 3 and 4, this requirement imposes

design difficulties especially for high gain and low noise achievements. For indirect detection, the light emitted by the scintillator is stored as signal charge in the photodiode. The photodiode capacitance act as signal storage and additional explicit capacitance becomes optional. It is for these reasons and also for easier comparison with the co-planar design, only the continuous sensor design for indirect detection scheme is considered here.

Comparing the continuous sensor design to the co-planar architecture, the data line is still placed at the same layer; hence there is no benefit in coupling capacitance. Meanwhile, the large sensor (due to higher fill factor) results in an increased photodiode pixel capacitance. This increases the signal storage capacity but at an expense of higher pixel reset noise.

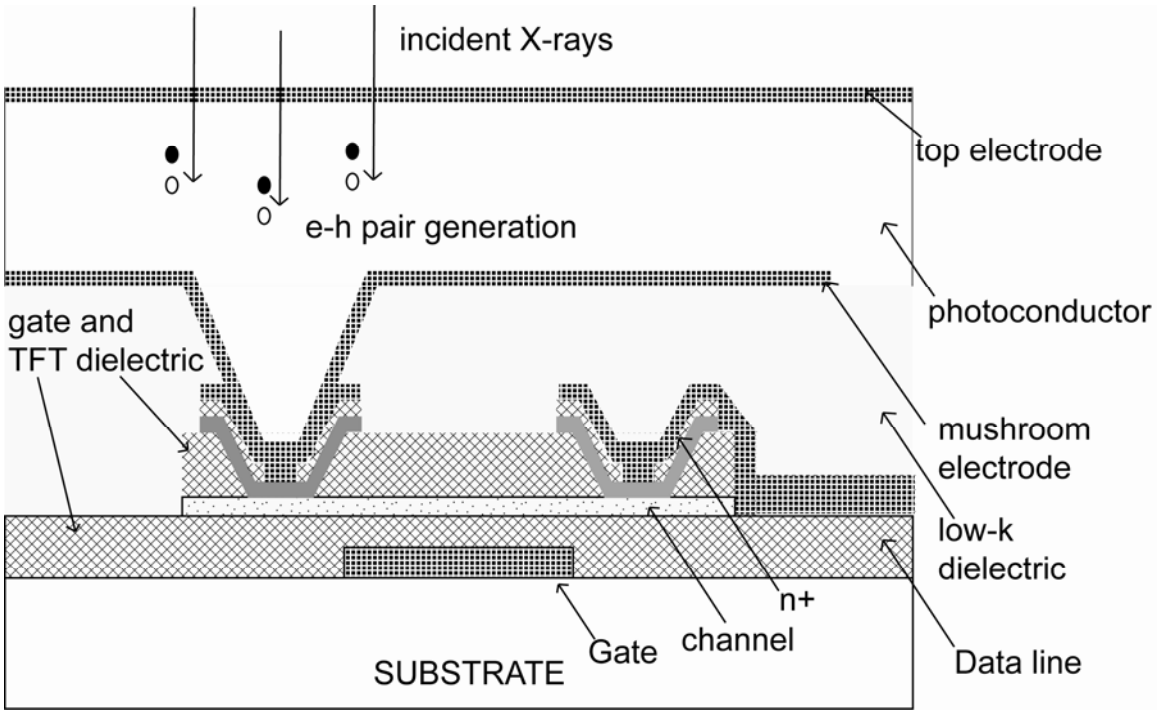

Figure 5-2: Continuous sensor based on direct detection.

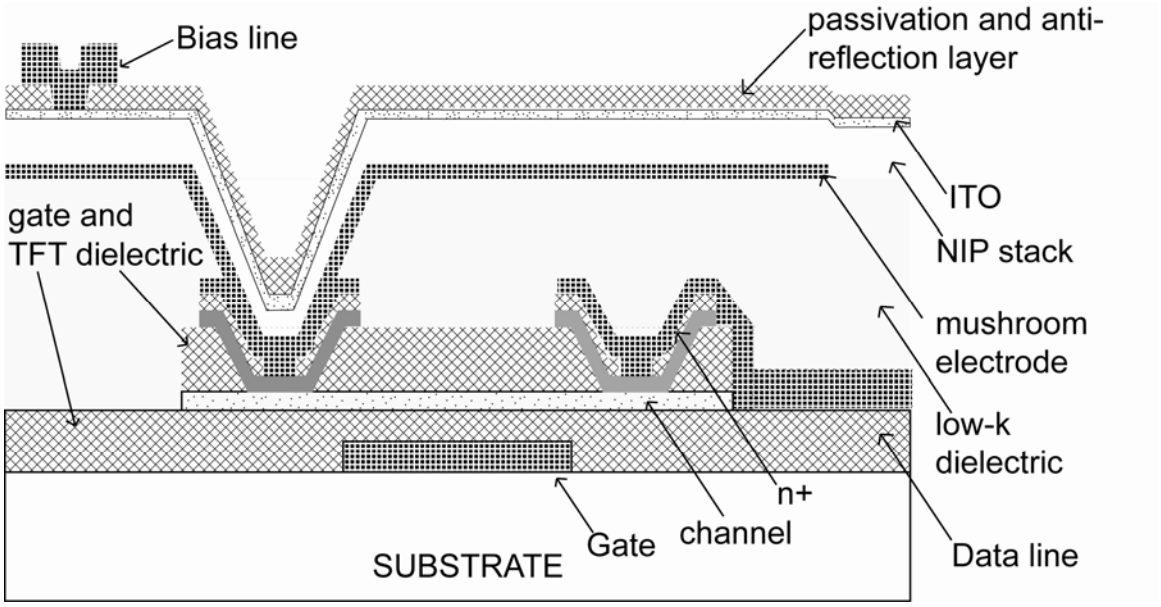

Figure 5-3: Continuous sensor based on indirection detection and photodiodes.

For photodiode capacitance estimation, it is reasonable to assume that it can be obtained from the intrinsic a-Si:H layer when the sensor is fully depleted. For a 500 nm thick intrinsic a-Si:H layer with dielectric constant of 11, a pixel with 95% fill factor and a pitch of 150 μm x 150 μm gives a 41.7 pF capacitance. In comparison, co-planar structure with 60% fill-factor has a photodiode capacitance of 2.63 pF. Hence, the continuous sensor capacitance result in a 25.8% higher reset noise than co-planar scenario. It is recalled that reset noise is one of the main noise contributors, combining with the minimal advantage in data line thermal noise over co-planar design, intensive optimization is required to obtain high performance using continuous sensor architecture.

5.2.2 Segmented Sensor

High fill factor (HFF) pixel architecture is shown in Figure 5-4. The cross sectional diagram shows the segmented photodiode stack and it is integrated above the TFT layers to form a vertically overlapping structure.

The segmented sensor design alleviates the design limitations presented in the other pixel architectures. Firstly, by building the sensor stack on top of the TFT layers, the fill factor is increased in comparison to the co-planar structure. From Figure 5-4, the pixel pitch is limited by the data line width and inter-pixel separation. The data line width can be reduced according to the processing capability for via opening in the low-k dielectric. In the in-house fabrication facility, a fill-factor of 85% can be achieved and is reported in [86].

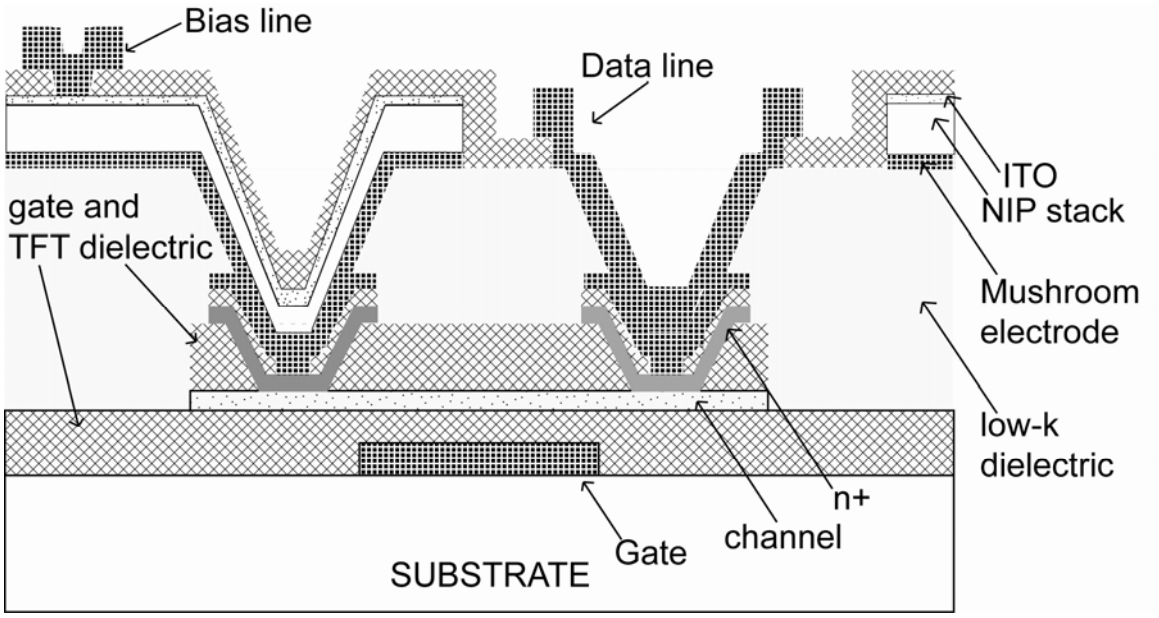

Figure 5-4: High fill factor pixel architecture with segmented photodiode.

Secondly, the p-i-n photodiode is segmented, thus assist in suppressing crosstalk between adjacent pixels that exist in continuous sensor structures. In addition, the entire sensor stack can be deposited in one PECVD step without intermediate patterning. Hence, the integrity of the interfaces are preserved, leading to lower sensor dark current that aids in low signal level detection.

Thirdly, the signal and sensor bias lines are placed on top of the entire structure. This metal is typically deposited as the last step of fabrication, thus allowing better flexibility to the choice of material. This flexibility also allows thickness optimization for lower line resistance that assists in achieving lower RC time delay as well as wider data line bandwidth.

Fourthly, the data metal lines are located relatively far away from the substrate in comparison to the other pixel architectures. This effectively minimizes the crossover capacitance between data and gate lines. At the crossover paths, the two metal lines are now separated by the gate, low-k inter-layer, and the top passivation dielectrics. If the low-k dielectric to be BCB with thickness of 3 μm and 2.7 dielectric constant, and the same dielectric is used for both gate and top passiviation, the data line capacitance per pixel is 56 fF. Comparing to the 135 fF for co-planar structure, it accounts for a factor of 2.4 reduction in parasitic capacitance.

Table 5-1 illustrates the direct comparison based on the noise analysis outlined in Chapter 4 for the H-APS design. The total input referred noise for the HFF design is at least 13% and 32% improvement over co-planar and continuous architectures. It is

evident that HFF demands further investigations and the remainder of this chapter will focus on this design.

Table 5-1: Noise performance comparison for pixel architectures.

	Co-planar	**Continuous**	**HFF**
C_{DL} (pF)	135	135	56
C_{SENSE} (pF)	2.63	4.16	3.72
Fll-Factor (%)	65	95	85
Input referred noise (electrons)	1640	1903	1445

5.2.3 Fabrication of HFF Segmented Pixel Architecture

The fabrication of HFF segmented requires additional processing steps and masks after the TFT layers for pixel integration. The processing steps are outlined in Table 5-2.

The TFT layers are fabricated using the in-house standard TFT process. A total of 5 masks are required. Then a thick layer of BCB is used for the low-k inter-layer dielectric. The dielectric constant of BCB is typically around 2.7 and can be deposited at relatively high thickness which serves as good material to reduce coupling capacitance. Since the mushroom electrode is fully overlapping the TFTs, it is possible to have high top gate leakage through the top TFT passiviation nitride. Thus, it is important to reduce

the coupling capacitance from the low-k dielectric. The BCB via etch opens up both the mushroom electrode and data line contact.

Next, the mushroom electrode is deposited and patterned. This mushroom electrode serves as both the bottom contact of the n-i-p photodiode stack, as well as the definition of the pixel area. After the mushroom electrode, the sensor stack is deposited. It is important to deposit the entire n-i-p stack in one PECVD step without breaking the vacuum. This helps in minimization particle contamination at the interfaces that act as defects and contributes to dark current. In addition, the stack is etched through reactive ion etching (RIE) to reduce edge photodiode edge leakage. A layer of top passitivation nitride is then used to cover the edge and act as protection for the sensor stack.

Table 5-2: Processing steps for HFF segmented pixel architectures.

Process	**Material thickness**	**Comments**	**Mask**
TFT layers		Inverted staggered TFT 5 masks process	1-5
Deposit photo BCB	3-4 μm	Open sensor and data line via	6
Deposit mushroom metal	100 nm	Mo mushroom electrode	
Deposit NIP stack	n+ a-Si:H ~ 50 nm i-a-Si:H ~ 500 nm p+ a-Si:H ~ 20 nm	NIP stack deposition done in 1 CVD step without vacuum breakage. RIE etch.	7
Deposit a-SiN:H	500 nm	PIN sidewall passiviation	8
Deposit ITO	65 nm	Polycrystalline ITO	9
Deposit metal	~1000 nm	Top metal for data and bias line.	10

ITO is used on top of the n-i-p stack to assist in providing a uniform top bias. This ITO is very thin to minimize any loss in light transmission. Afterwards, a thick metal layer is deposited and is used as both sensor stack bias and address/data line routing. The material of choice is flexible since it is the last step of fabrication, and so there is little limitations imposed by further processing steps. A thick layer (~1000 nm) of MO/Al alloy can reduce the resistivity from 1.3×10^{-7} Ω/m (Cr) to 4×10^{-8} Ω/m (Mo/Al), which is a 3 times decrease in line resistance.

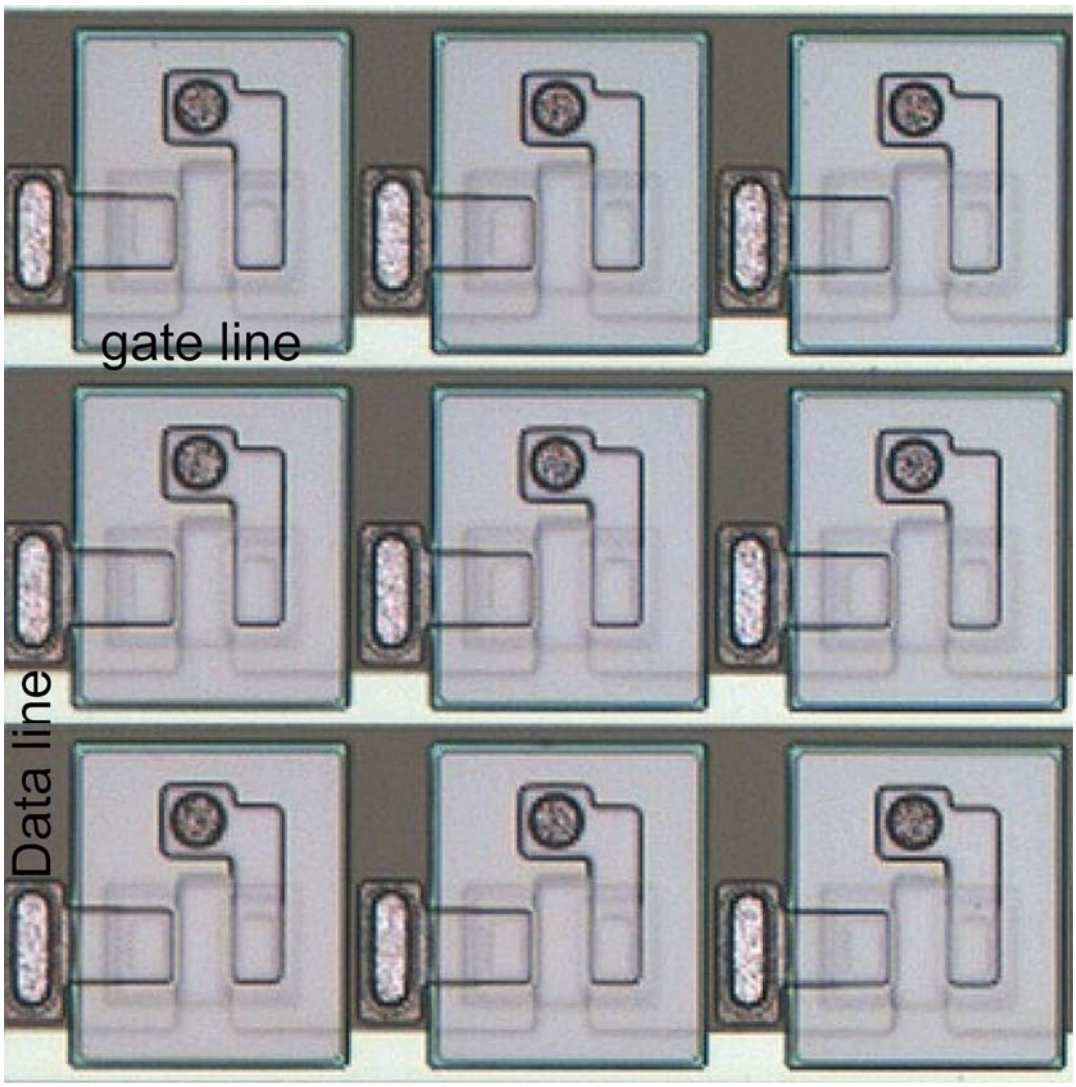

Figure 5-5: Screenshot of HFF segmented PIN diode test structure.

Figure 5-4 shows the in-house fabricated HFF pixel with segmented PIN diode using the PPS design. The diagram shows a small test structure with 3x3 pixels with ~65% fill-factor. There are a total of 12 copies of this test structure and this particular design is used for subsequent analysis in this chapter. The PPS design is chosen here for its simplicity for the demonstration of feasibility for the HFF segmented sensor architecture.

5.2.4 Measurement Results and Discussions

This section investigates the measurement results for the HFF segmented sensor architecture. Two additional test structures are fabricated to assist the experiments for the TFT circuit and sensor integration. A TFT test structure with the same fabrication process is designed and the source-drain contacts are routed to the top metal through the low-k dielectric vias. A second test structure with PIN photodiodes is designed without underlying TFT layers. The bottom mushroom electrode is routed along with the top (data line) metal for diode bias access. These two test structures provide individual device performances data for the HFF process, and are useful for gauging the feasibility of pixel integration.

5.2.4.1 TFT Performance

Figure 5-6 shows the micrograph of a TFT test structure fabricated using the HFF segmented sensor process outlined in Table 5-2. The test structures on the top row are discrete TFTs while the TFTs on the bottom row are 10 parallel-connected TFT for leakage current measurements. The TFT aspect ratios are 40/23, 60/23, and 108/23 and covers a good range of dimensions for TFT used in the pixel designs.

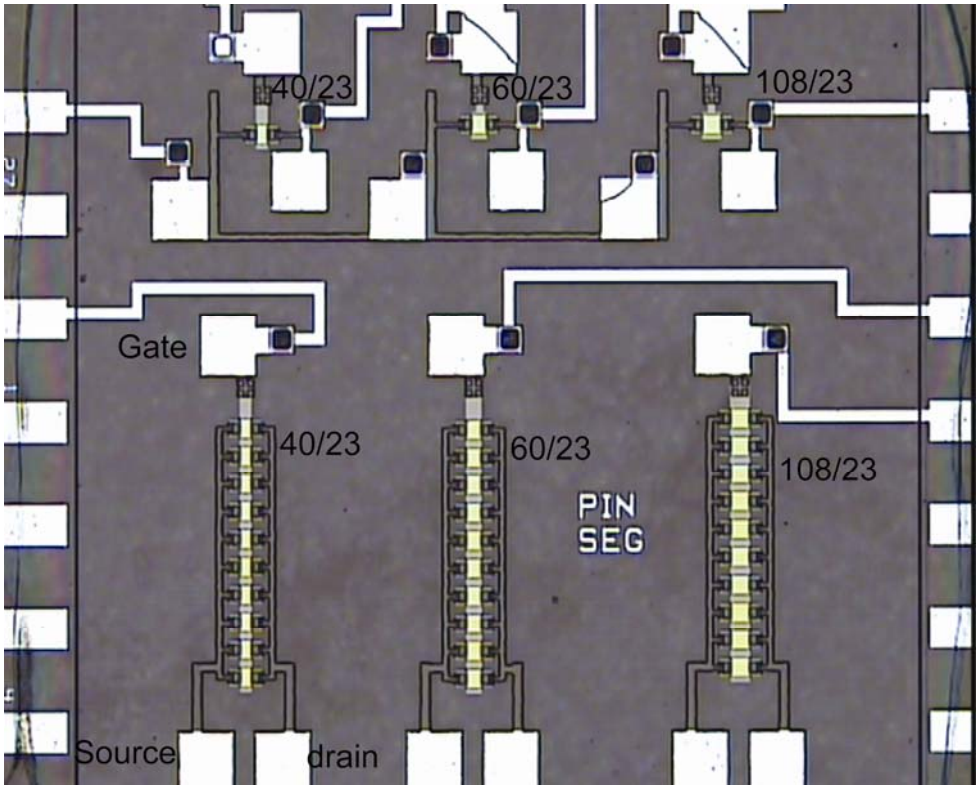

Figure 5-6: TFT test structures micrograph using HFF segmented sensor process.

The TFT transfer characteristics for various drain-source biases are shown in Figure 5-7. The leakage currents for $V_{DS} = 1\,\mathrm{V}$ is approximately 100 fA for a TFT with W=108 μm, corresponding to a ~1 fA/μm. The TFT at larger V_{DS} exhibits much higher leakage current especially for V_{DS} larger than 10V. The TFTs in the pixel circuit designs in Chapter 3 are mostly operating in the linear regime, with the exception of the AMP TFT. So the leakage current performance is acceptable for typical imaging operations.

This TFT test structures here are accessed through the top metallization. The source/drain metal is connected to the top metal through the low-k dielectric (BCB) vias. The contact resistances potentially add to drain/source series resistances, and helps explain the voltage dependence at TFT turn off (V_{GS} <0V)at higher V_{DS} bias.

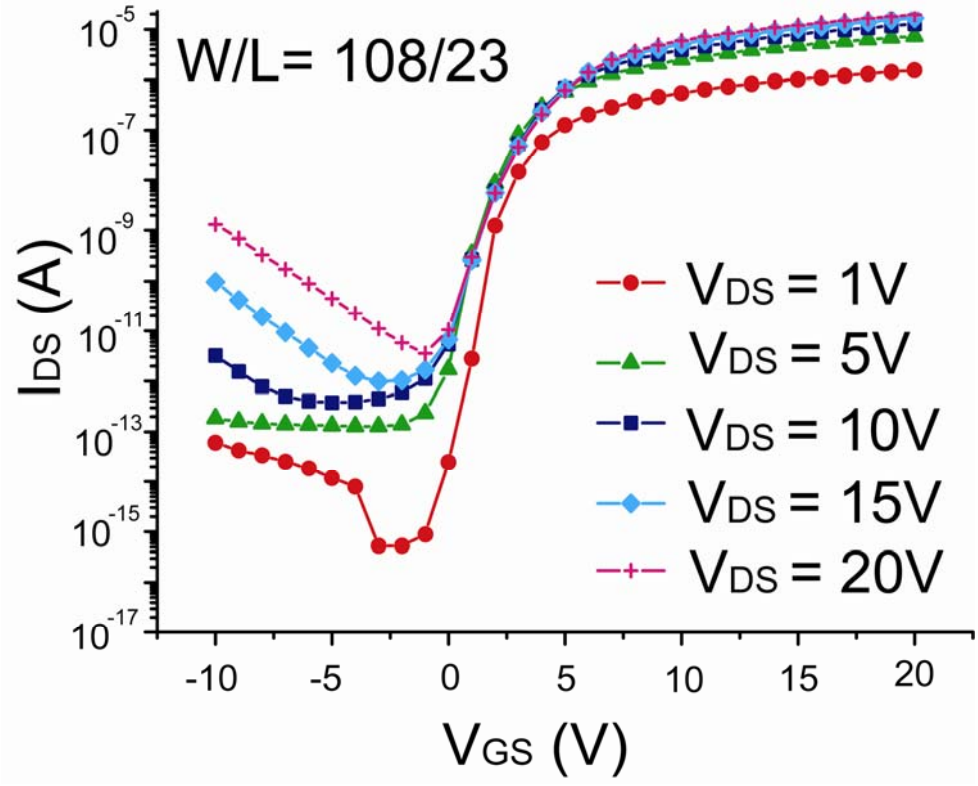

Figure 5-7: Transfer characteristics for TFT fabricated using HFF segmented sensor process.

The added series resistances from the BCB contacts have to be taken into account for modeling purposes. A more details series resistance extraction method is explained in Appendix C. For the sake of simplicity, the TFT with series model can be represented as Figure 5-8. Using the model, the TFT drain source current in linear regime can be written as

$$I_{DS} = \frac{1}{2}\mu_{EFF} C_G \frac{W}{L}\left[2\left(V_{GS}^{'} - V_T\right)V_{DS}^{'} - \left(V_{DS}^{'}\right)^{'}\right] \tag{5.1}$$

where

$$V_{GS}^{'} = V_{GS} - I_{DS}R_S \text{ and } V_{DS}^{'} = V_{DS} - I_{DS}\left(R_D + R_S\right). \tag{5.2}$$

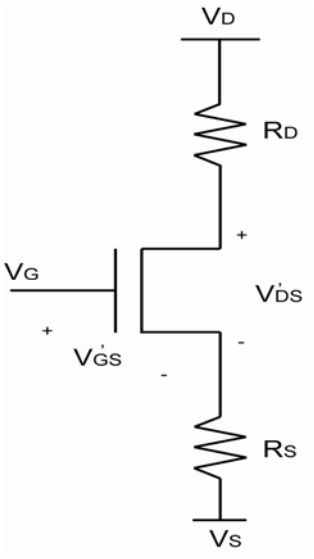

Figure 5-8: Simplified TFT series resistance model.

The effective mobility can be extracted from the measurement first by assuming $R_S = R_D = 0$. Assuming symmetrical TFT drain and source, R_S and R_D are then equal. The results of the TFT performances for conventional (without BCB) and HFF segmented sensor process are summarized in Table 5-3.

Table 5-3: Summary of TFT performances.

	R_S , R_D (MΩ)	V_T (V)	Subthreshold slope (V/decade)	Leakage current (fA/μm)
Conventional TFT	2.1	2.2	0.3	~1
HFF segmented TFT	1.5	2.3	0.3	~1

Here, it is evident that the TFTs fabricated using different process exhibits similar performances except for series resistances. The BCB contacts contribute to the series resistance by a significant amount. Considering TFT in linear mode having a channel resistance of approximately 3 MΩ, the combined series resistances become comparable. Recalling the pixel and noise analysis in Chapter 3 and 4 that the drain-source resistance of the READ TFT affects the operating point of the AMP TFT in H-APS, thereby limits the gain of system. The vertically integration structure allows more flexibility to increasing the width of the READ TFT to alleviate this concern without severe impact on pixel area usage.

5.2.4.2 PIN Performance

Figure 5-9 shows the micrograph of some segmented PIN diode test structures fabricated using the HFF process outlined in Table 5-2. Here, the diode electrodes are routed using the mushroom electrode (mask 7) and top metallization (mask 10).

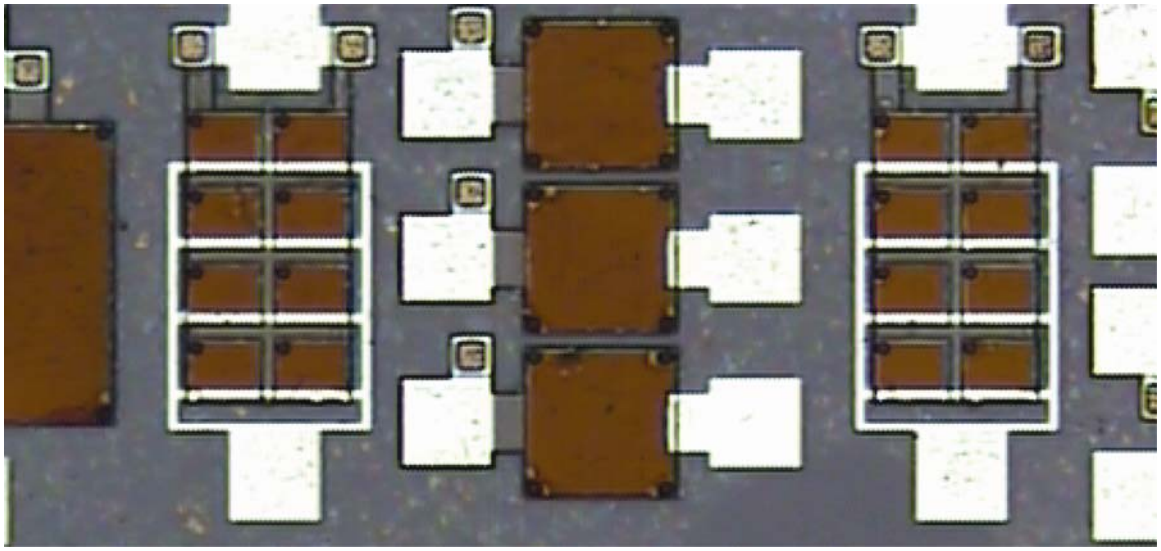

Figure 5-9: Micrograph of test structure for segmented PIN diodes.

Diode size of 150^2 $(\mu m)^2$, 250^2 $(\mu m)^2$, and $500^2(\mu m)^2$ are designed while diodes with smaller dimensions are connected in parallel for dark current measurements. These test structures are exposed to 540 nm incident light corresponding to wavelength of photon emission from the phosphor scintillator screen. The diode is reversed bias at -1 V and the light sensitivity result is demonstrated in Figure 5-10. The initial current transient is due to the change in applied bias. A delay of 400 s is inserted before the incident light is applied to eliminate any transient effects. The light signal is applied for 50 s and the diode reverse current rose about an order of magnitude. Clearly, light sensitivity of diodes is obtained, with steady-state dark current level at ~ 2pA.

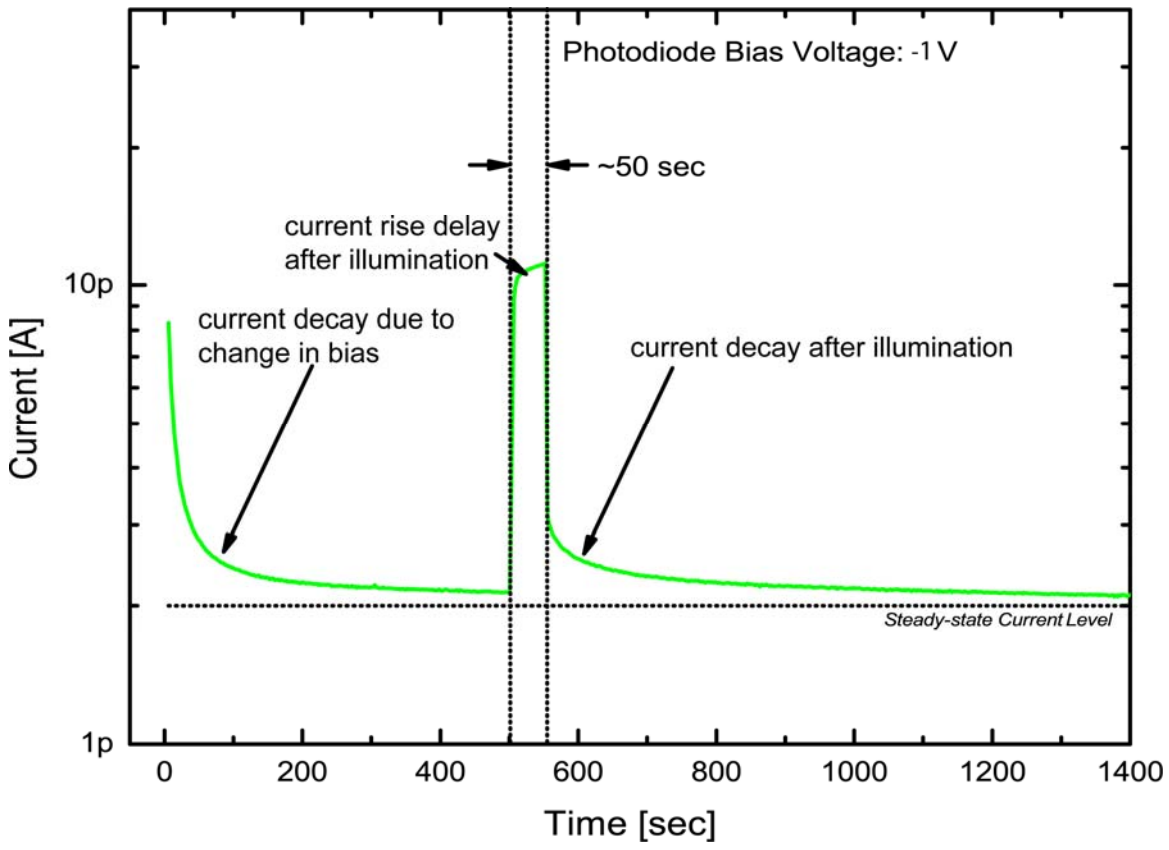

Figure 5-10: Demonstration of light sensitivity of segmented PIN diode.

Next, the light sensitivity to varying light pulse is explored and the results are shown in Figure 5-11. Here, the duration of light pulse is varied, corresponding to an increasing amount of incident photon. Evidently, a longer light pulse generates a larger amount of current. It is worthy of noting that the signal collection is in charge domain, hence explains the small current increase in response to doubling the duration of illumination. The area under the curve corresponds to the amount of charge collection and that scales linearly with the amount of incident photons.

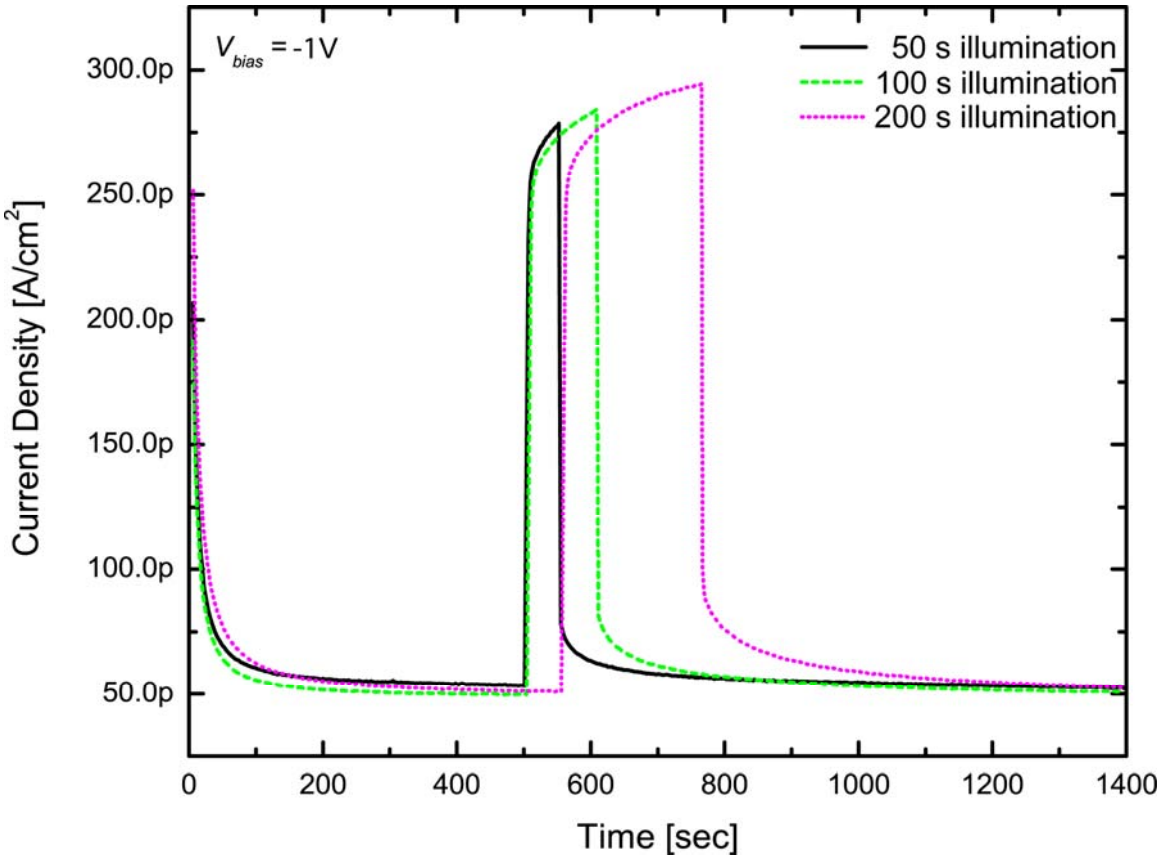

Figure 5-11: Demonstration of light sensitivity of segmented PIN diode with varying light pulse duration.

5.2.4.3 Pixel Performance

The prototype HFF with segmented sensor in Figure 5-5 is tested using the in-house cascade low noise cascade prober connected via SMUs to a test board with readout electronics. The setup of the cascade prober is shown in Figure 5-12 where the test sample is loaded in wafer form. An LED light is mounted inside the chamber to provide light signal in ~540 nm range. The metallic cover and test system fixture provides light shielding, and a black cloth is used to cover the lid to prevent light leak. The test board is designed and fabricated by Dr. Jeff Chang and the design details are documented in [91]. The schematic diagram for the test board is shown in Figure 5-13.

Figure 5-12: Cascade low noise prober for wafer testing.

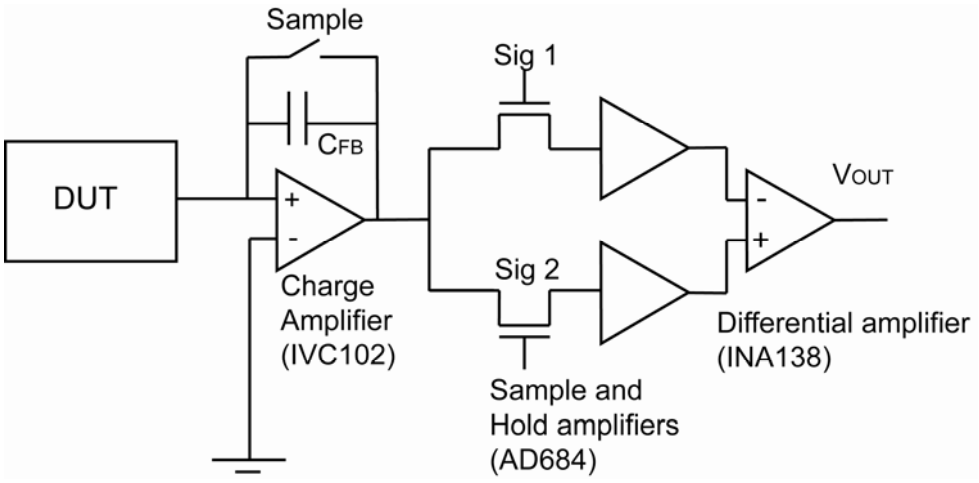

Figure 5-13: Test board schematic

The required pulsing signals are generated by a custom programmed microchip (also designed by Dr. Jeff Chang), and provide all the necessary bias and addressing signals required by the device under test (DUT). The output is connected to a charge amplifier with selectable C_{FB} (10, 40, or 100 pF). The sample-and-hold amplifiers provide the two samples necessary for signal readout, while the differential amplifier stage subtracts the two signal samples and removes any dc offset. The waveforms for the various control lines are summarized in Figure 5-14.

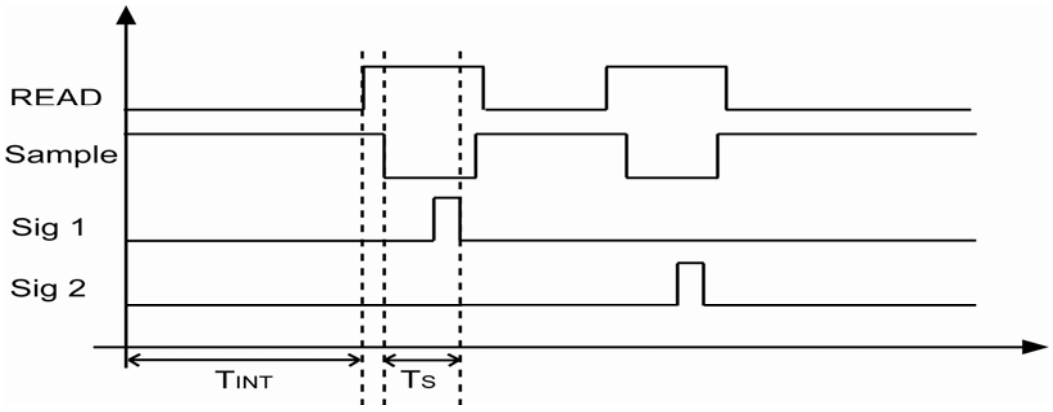

Figure 5-14: Waveform for the operation of test board for HFF prototype.

Here, the integration time (T_S) is controlled by the LED light pulse and the READ TFT gate pulse. The READ TFT is turned on prior to signal sample to allow transients to settle. The signal sample is first stored in Sig 1, and then the reset signal is stored in Sig 2. The differential amplifier then generates an input V_{OUT} according to the difference in the samples, which corresponds to the incident light charge. It is worthy of nothing, the waveform is expected to change if an H-APS design is used, where non-destructive readout is possible. In which case, Sig 1 and Sig 2 can be both store the sample with signal in the first T_S, this is typically done to avoid large voltage variations at V_{OUT} due to DC output bias. For the device under test here (a PPS design), readout is accompanied with pixel reset, hence sampling the signal at both Sig 1 and Sig 2 reduces the signal swing in half. Moreover, for a pixel with current driving capability (AMP TFT), an in-pixel reset pulse has to be inserted between the READ pulses.

Figure 5-15 shows the testing results for the HFF pixel architecture with segmented sensors. The light pulse is applied for 1 s while the sampling time is 150 μs. The rather long sampling time is due to charge sharing nature of the PPS design, and this readout time is expected to be reduced to tens of μs for pixels with amplifications. The reset voltage of the pixel is determined by the positive terminal of the charge amplifier and is biased at ground. The feedback capacitor (C_{FB}) is chosen to be 10 pF and is the smallest value provided by the charge amplifier. It is noted, for a PPS design with ~3.5 pF pixel capacitance, a large C_{FB} ensures good charge transfer efficiency at an expense of smaller voltage swing.

It is clearly shown in the reset sample at V_{OUT}, at which a small voltage (~30 mV) appears as the reference voltage. The incident signal between the two samples induced a 0.96 V different between the two samples, and it agrees reasonably with estimation. The voltage at the reference sample is potentially due to image lag, stemming from incomplete charge transfer from the first signal readout. Considering the series resistance extracted from the TFT test structures in section 5.2.4.1, the RC time constant for this PPS is approximately 24.5 μs. Using 6 time constant gives, 147 μs readout time, hence helps explain the small but finite residual charge at the reference sample.

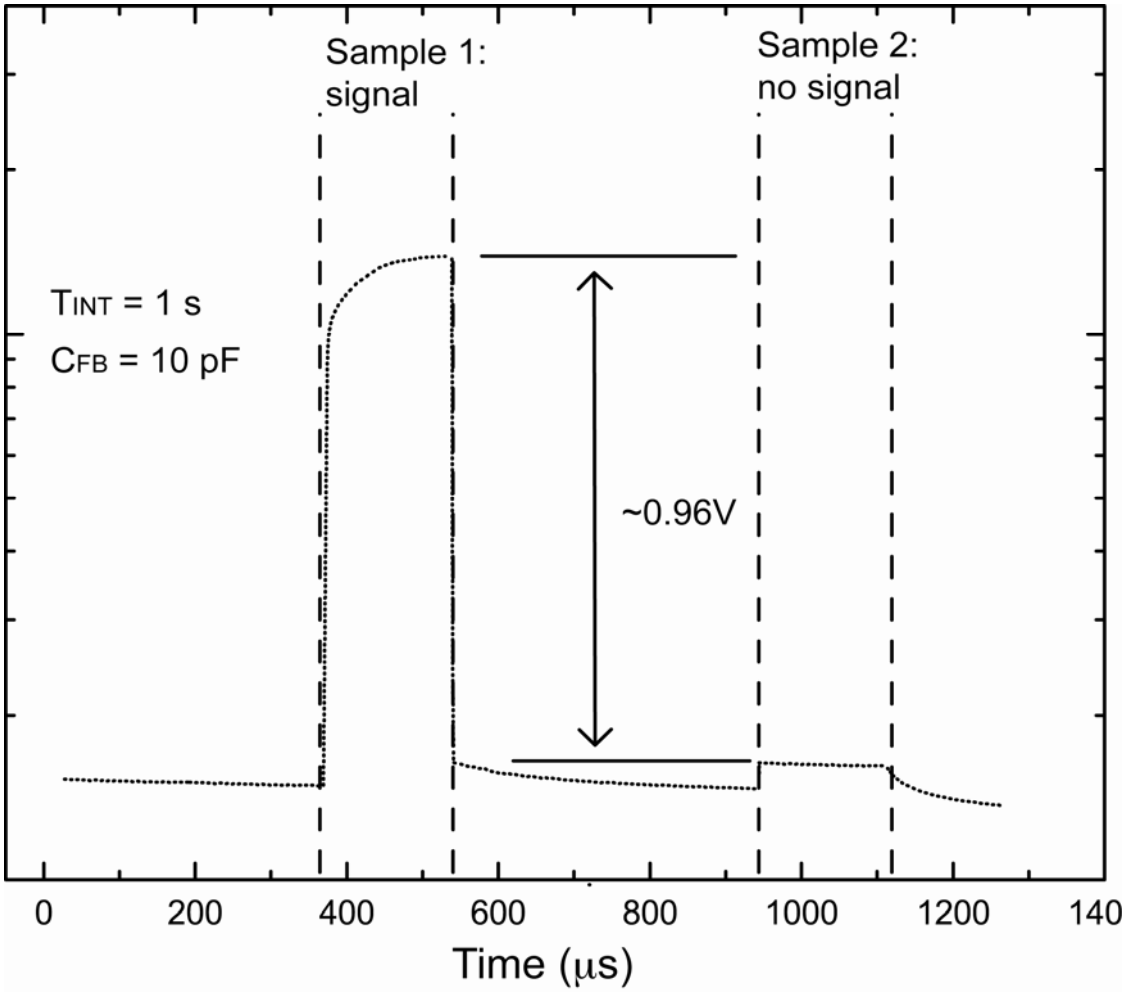

Figure 5-15: Test results for PPS HFF pixel with segmented diode.

6 Conclusions and Future Work

This thesis addresses the development of analytical models and circuit design techniques for high performance digital imaging arrays. It is demonstrated that proper pixel circuit design and optimization can alleviate the shortcomings of the a-Si materials technology, with respect to current drive, noise, and pixel size. In particular, this work targets the unique requirements of bio-medical imaging where high signal-to-noise ratio, wide dynamic range operation, and high fill factor ratio are key attributes. The development of pixel readout circuits discussed in Chapter 3 improves the current state-of-the-art by boardening the dynamic range and providing higher signal gain. In addition, the H-APS circuits (particularly the version with global shutter) provide enhancements in technology scalability with minimal impact on signal amplification and achievable dynamic range. These attributes are favorable for higher manufacturing yield, and consequently lower cost. More importantly, the pixel architectures presented here benefits from technology advancements related to scalability of both performance and geometry.

In terms of noise analysis, accurate estimation of both transistor and circuit level noise is critical in pixel design especially for bio-medical applications where it is desirable to reduce the x-ray incident signal for safety reasons. The results presented here demonstrate successful modeling of noise in pixel circuits, including the signal-to-noise ratio analysis of H-APS designs. Here the novelity lies in the approach in which a circuit simulator can be employed. This allows systemic design optimization to be performed.

The design and evaluation methodologies presented here can be utilized for large area imaging array where an analytical toolset for development is currently lacking.

Despite the novelity of the pixel designs demonstrated here, there still remains additional development to adapt to manufacturing. Both versions of the H-APS require 4 TFTs in each pixel, and together with the low driving capability of the a-Si:H TFT, serve as a bottleneck in pixel size reduction. The complexity of the circuit and the routing of multiple metal lines potentially limit fabrication yield. Future investigations in pixel design can focus on TFT sharing (as briefly outlined in section 3.3.4.9), which can bring forth significant average size reduction that is both desirable. Applications such as mammography can benefit greatly from the increased resolution, high gain, and wide dynamic range.

The circuits and devices fabricated focus on reliability and reproducibility for prototyping purposes. However, in the long term, the incorporation of TFTs with smaller channel length (~4 to 6 μm in industrial processes) is inevitable for large scale manufacturing. It is noted that effect of series resistance of the TFT quickly becomes a limiting factor when channel length is reduced, thereby limiting the pixel gain. Both circuit and pixel design needs to take this into consideration which results in higher complexity in the design phase. The systematic design and evaluation approach presented in this work will become increasingly essential to allow a smooth transition to manufacturing. Future considerations in this area can consider integrating the noise and TFT model presented in this work into one unified package. This helps reduce circuit simulation complexity and lead to higher accuracy in performance estimation. In addition, fixed pattern noise (FPN) and photo-response non-uniformity (PRNU) are also

important areas that should be considered. However, the characterization and verification of this requires large arrays (at least 500 x 500 pixels) that are beyond the capability of the in-house facility. Technology transfer to outside foundaries with larger array fabrication capability will allow such experiments.

The pixel integration in Chapter 5 has considered a few sensor architectures and demonstrated successful prototype based on PPS and the HFF designs. The successful integration between sensor and TFT is realized using the HFF segmented PIN diode process with 65% fill factor. The PPS design is used for its simplicity which is ideal for concept verification and feasibility confirmation. The next step is to extend the fabrication knowledge into prototyping APS and H-APS designs on HFF architectures. The higher TFT counts in these pixel designs and much more complex driving schemes entails thorough investigation especially for the mushroom electrode overlap which potentially leads to TFT top gate leakage. Moreover, initial pixel integration results have shown stress related issues in fabrication, especially in the inter-layer low-k dielectric. The fabrication process includes 10 masks, and the TFT layers are separated by a thick (~3μm) BCB layer. It is found out the BCB is prone to cracking during dicing as shown in Figure 6-1. The crack appears first at the edge of the dicing streets (near the bond pad) and propagates into the device. This post-fabrication anomaly induces shorts between the source/drain metal and the mushroom electrode, rendering the device non-functional. It is partially for this reason that the measurements for pixel integration are performed at a wafer level to avoid unnecessary loss of test samples. Future work in this area must involve fabrication optimization to improve device yield and minimize film stress.

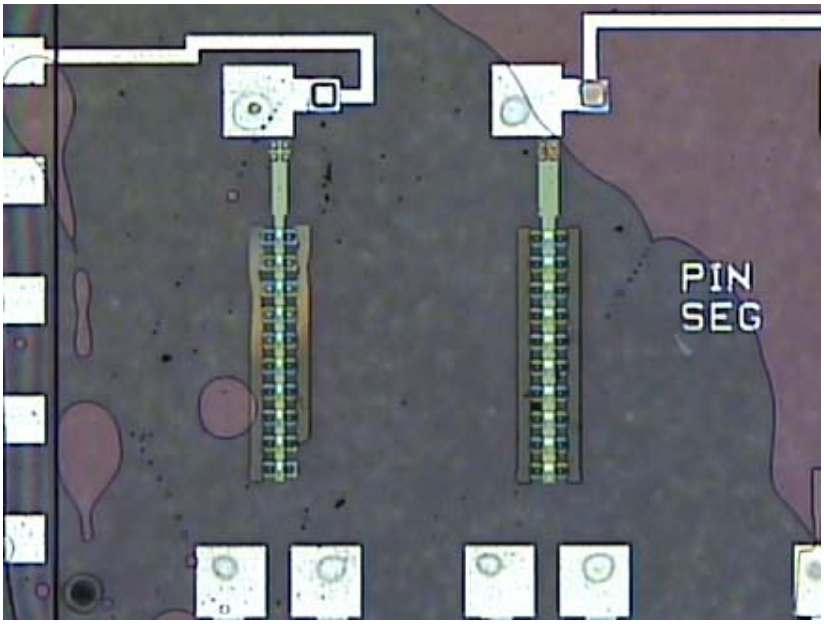

Figure 6-1: BCB cracking after dicing and sawing for test structures.

7 Contributions

The details of contributions in this thesis are summarized in the few sections below.

7.1 Circuit Designs

- The first a-Si:H TFT based H-APS pixels and arrays are fabricated and test successfully.
- Two flavors of the H-APS pixel, namely dual readout and global shutter, are investigated and measured to have improved over an order of magnitude (up to 160 dB) in dynamic range performance in comparison with conventional 3-TFTs APS. High speed (33 frames per second) readout is possible on both H-APS designs.
- The proposed H-APS design with global shutter mitigates the tradeoff between highest achievable dynamic range and pixel gain. This tremendously benefits in pixel design flexibility when both high signal gain and wide dynamic range are desired (fluoroscopy and mammography).

7.2 Noise Analysis

- The major a-Si:H TFT noise contributors to imaging applications such as thermal, flicker and reset noise are studied and modeled. Measurement results have confirmed reasonable accuracy.

- Partition noise, which is commonly observed in crystalline silicon MOSFETS, are investigated for a-Si:H TFT for the first time. Here, the existence of partition noise is confirmed for a-Si:H TFTs, even though the magnitude is concluded to be significantly smaller than MOSFETs counterpart.
- A systematic approach for pixel noise analysis is introduced in Chapter 4 where circuit nodal analysis is combined with the TFT noise models. The approach enables noise analysis to be performed using circuit simulator with high accuracy.
- Using this novel analysis approach, optimization of pixel architectures on various design parameters (W/L ratios, C_{SENSE}, channel length, bias, etc.) have been performed, discussed, and then verified with experimental results. Pixel system noise of less than 1200 electrons can be achieved with careful biasing and design considerations.

7.3 Pixel Integration

- The first high fill-factor (HFF) pixel architecture with segmented PIN photodiode is fabricated and successfully measured.
- A 65% fill factor HFF pixel with PPS architecture is tested with reduced data line capacitive coupling. This assist in reducing data line thermal noise which is one of the major noise contributors for practical imaging array, and its benefits are especially pronounced for larger arrays (up to 2000 x 2000).

Appendix A Power Spectrum Formula Derivation for TFT Reset Operation

The TFT reset operation can be modeled by mathematical formula that predicts the power spectrum of the output with respect to frequency. In imaging array applications, the reset transistor is connected to either the photodiode or a charge collection node (such as a storage capacitor). In addition, the node to be reset is almost always connected to an amplification stage, thus the general form of such a topology can be described in the Figure 7-1.

It is customarily to assume the reset transistor has negligible resistance in the ON-state. However, this assumption is not practical in every case and especially in the case of high frequency operation in typical imaging applications. In this derivation, the ON resistance of the reset transistor is considered and lumped together with the output resistance of the reference generator. By applying basic circuit theory, the circuit can be simplified.

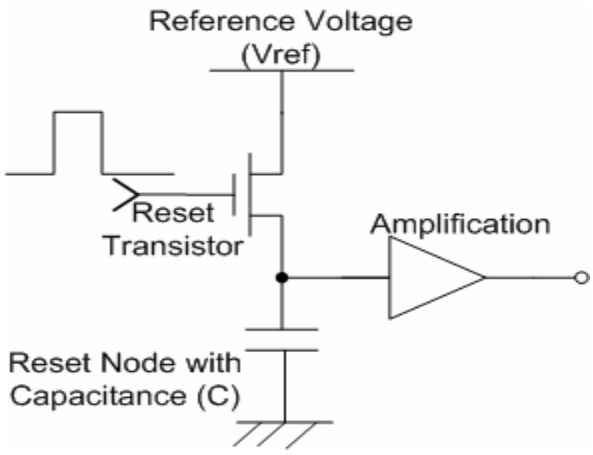

Figure 7-1: General structure for transistor reset operation.

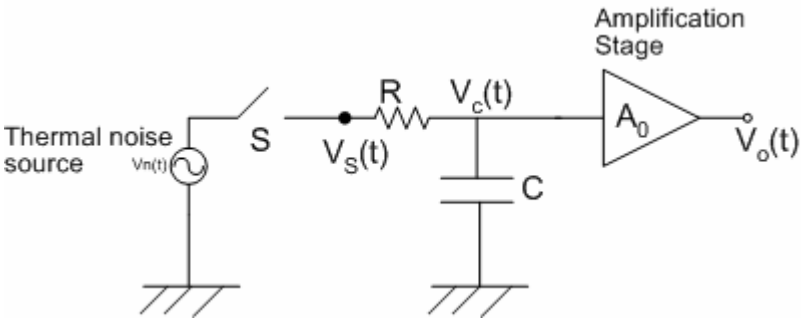

Figure 7-2: Equivalent circuit for transistor reset.

The equivalent circuit diagram shown in Figure 7-2 is derived by applying the following rules.

1. Reference voltage generator can be replaced by its Thevinen Equivalence.

2. The reset transistor switch can be replaced by an ideal switch with corresponding ON resistance. The ON resistance is combined together with any parasitic resistance as seen by the reset node.

3. The photodiode and any nodal parasitic capacitance are represented as a capacitor in the equivalent circuit diagram.

4. The voltage source in the equivalent circuit will be turned off for noise analysis and the noise source for the resistor is replaced.

Here, we define two scenarios during the reset operation, one when the switch is closed and the other when the switch is open.

$$\begin{aligned} v_s(t) &= v_c(t) \text{ when S is open} \\ v_c(t) &= v_n(t) \text{ when S is closed.} \end{aligned} \tag{A.1}$$

This configuration is analogous to a signal (or noise source) being sampled and subsequently filtered by a RC low pass filter (LPF). As a result, two signals can be consequently defined, namely $p_1(t)$ and $p_2(t)$ to represent the intervals where the switch is closed or opened respectively. The signal sampling cases are shown graphically in Figure 7-3.

The signal $v_c(t)$ is the filtered signal of $v_s(t)$ through the low pass RC filter. The objective here is to obtain a representation of $v_s(t)$ first by defining $v_s(t) = v_{s1}(t) + v_{s2}(t)$ where

$$v_{s1}(t) = \left\{ \begin{array}{l} v_n(t); \text{ for } n\tau + \dfrac{\delta}{2} < t < (n+1)\tau - \dfrac{\delta}{2} \\ 0; \text{ elsewhere} \end{array} \right\} \text{when S is closed,} \qquad \text{(A.2)}$$

and,

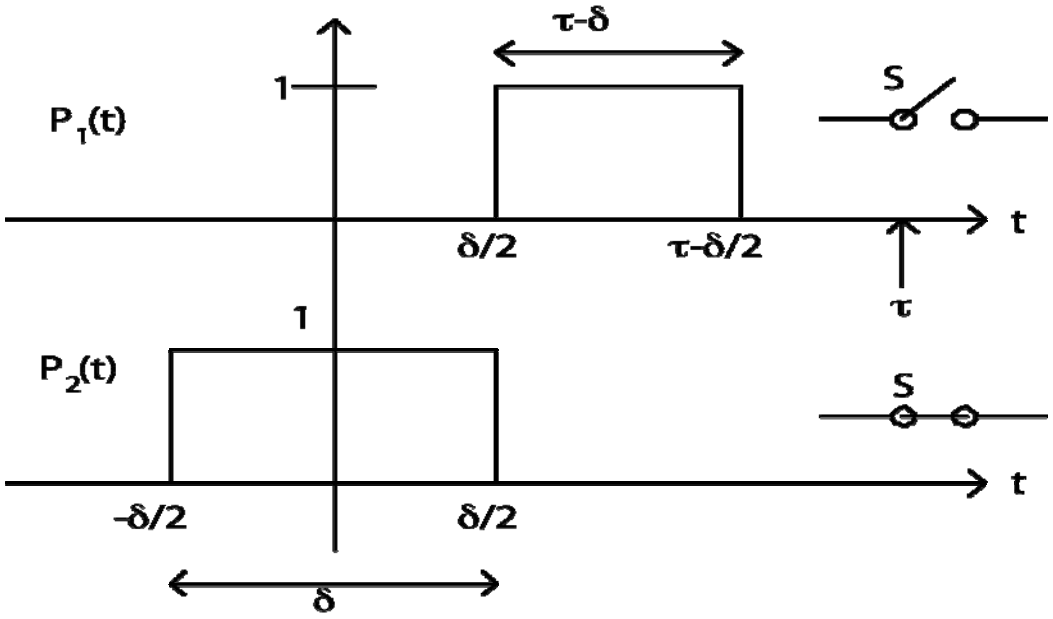

Figure 7-3: Two cases of signal sample.

$$v_{s2}(t) = \left\{ \begin{matrix} v_c(t); \text{ for } n\tau - \dfrac{\delta}{2} < t < n\tau + \dfrac{\delta}{2} \\ 0; \text{ elsewhere} \end{matrix} \right\} \text{when S is opened.} \tag{A.3}$$

Combining with the definition of $p_1(t)$ and $p_2(t)$ gives

$$\left\{ \begin{matrix} v_{s1}(t) = \sum_{k=-\infty}^{\infty} v_n(t)\, p_1(t - k\tau) \\ v_{s2}(t) = \sum_{k=-\infty}^{\infty} v_c(t)\, p_2(t - k\tau) \end{matrix} \right\} \tag{A.4}$$

If the RC LPF is said to have and impulse response of $h(t)$, then $v_c(t)$ becomes the convolution of the functions $v_s(t)$ and $h(t)$. So the general form becomes,

$$v_c(t) = \int_{-\infty}^{\infty} h(u) v_s(t-u)\, du. \tag{A.5}$$

Applying the theory of convolution to equation (A.5) gives

$$\begin{aligned} v_c(t) &= \int_{-\infty}^{\infty} h(u)v_{s1}(t-u)du + \int_{-\infty}^{\infty} h(u)v_{s2}(t-u)du \\ &= v_{c1}(t) + v_{c2}(t). \end{aligned} \tag{A.6}$$

Recall the definition of $v_{s2}(t)$ in equation (A.4), $v_c(t)$ becomes

$$v_c(t) = \int_{-\infty}^{\infty} h(u)v_{s1}(t-u)du + \int_{-\infty}^{\infty} h(u)\sum_{k=-\infty}^{\infty} v_c(t-u)\,p_2(t-u-k\tau)du \tag{A.7}$$

and simplifies to

$$v_c(t) = v_{c1}(t) + \int_{-\infty}^{\infty} h(u)\sum_{k=-\infty}^{\infty} v_c(t-u)\,p_2(t-u-k\tau)du. \tag{A.8}$$

It is reasonable to assume that $v_c(t)$ will not change when switch S is opened, so $v_c(t)$ is constant during the time $n\tau - \frac{\delta}{2} < t < n\tau + \frac{\delta}{2}$. As a result, the voltage at the mid point of the interval can be used, such that

$$\sum_{k=-\infty}^{\infty} v_c(t)\,p_2(t-k\tau) = \sum_{k=-\infty}^{\infty} v_c(k\tau)\,p_2(t-k\tau). \tag{A.9}$$

Thus, the expression simplifies to

$$v_c(t) = v_{c1}(t) + \int_{-\infty}^{\infty} h(u)\sum_{k=-\infty}^{\infty} v_c(k\tau)\,p_2(t-u-k\tau)du. \tag{A.10}$$

The power spectral density of $v_c(t)$, i.e. $S_c(\omega)$, is of interest here. Recall that the power spectral density (PSD) describes how the power (or variance) of a time series is

distributed over frequency. In order to obtain that, the Fourier transform of $v_c(t)$ is found first, i.e. $V_c(\omega)$ .The Fourier transform is obtained as follows

$$\begin{aligned} V_c(\omega) &= \int_{-\infty}^{\infty} v_c(t)\exp(-j\omega t)dt \\ &= \int_{-\infty}^{\infty} v_{c1}(t)\exp(-j\omega t)dt + \int_{-\infty}^{\infty}\left\{\int_{-\infty}^{\infty} h(u)\sum_{k=-\infty}^{\infty} v_c(k\tau)\,p_2(t-u-k\tau)du\right\}\exp(-j\omega t)dt. \end{aligned} \tag{A.11}$$

Since the convolution in the time domain results in the multiplication in the frequency domain, the transformation of $h(u)$ can be taken out of the convolution integral as a multiplication factor.

$$\begin{aligned} V_c(\omega) &= \int_{-\infty}^{\infty} v_{c1}(t)\exp(-j\omega t)dt + H(\omega)\cdot\int_{-\infty}^{\infty}\left(\sum_{-\infty}^{\infty} v_c(k\tau)\,p_2(t-k\tau)\right)\exp(-j\omega t)dt \\ &= \int_{-\infty}^{\infty} v_{c1}(t)\exp(-j\omega t)dt + H(\omega)\sum_{-\infty}^{\infty} v_c(k\tau)\left(\int_{-\infty}^{\infty} p_2(t-k\tau)\exp(-j\omega t)dt\right). \end{aligned} \tag{A.12}$$

Using the time shifting theorem of Fourier transform where

$$\int_{-\infty}^{\infty} p_2(t-k\tau)\exp(-j\omega t) \Rightarrow \exp(-j\omega k\tau)\int_{-\infty}^{\infty} p_2(t)\exp(-j\omega t)dt \tag{A.13}$$

Therefore, the Fourier transform of $V_c(\omega)$ becomes

$$\begin{aligned} V_c(\omega) &= \int_{-\infty}^{\infty} v_{c1}(t)\exp(-j\omega t)dt + H(\omega)\sum_{-\infty}^{\infty} v_c(k\tau)\exp(-j\omega k\tau)\left(\int_{-\infty}^{\infty} p_2(t)\exp(-j\omega t)dt\right) \\ &= \int_{-\infty}^{\infty} v_{c1}(t)\exp(-j\omega t)dt + H(\omega)\sum_{-\infty}^{\infty} v_c(k\tau)\exp(-j\omega k\tau)P_2(\omega). \end{aligned} \tag{A.14}$$

The second part of equation (A.14) still needs to be considered. According to Poisson's sampling theorem,

$$\sum_{n=-\infty}^{\infty} x(n\tau)\exp(-j\omega nT) = \frac{1}{T}\sum_{k=-\infty}^{\infty} X^F\left(\omega - \frac{2\pi k}{T}\right). \tag{A.15}$$

where T is the period of the signal.

Using the sampling theorem in equation (A.15), the first term in equation (A.14) becomes

$$\sum_{-\infty}^{\infty} v_c(k\tau)\exp(-j\omega k\tau) = \frac{1}{\tau}\sum_{-\infty}^{\infty} V_c\left(\omega - \frac{2\pi n}{\tau}\right). \tag{A.16}$$

Let $\omega_o = \frac{2\pi}{\tau}$ gives

$$\sum_{-\infty}^{\infty} v_c(k\tau)\exp(-j\omega k\tau) = \frac{1}{\tau}\sum_{-\infty}^{\infty} V_c(\omega - n\omega_o) = \frac{1}{\tau}\sum_{-\infty}^{\infty} V_c(\omega + n\omega_o). \tag{A.17}$$

The last two expressions in equation (A.17) are interchangeable because the summation is done from -∞ to ∞, so addition and subtraction inside the summation becomes numerically identical. Substituting the expression in (A.17) back into equation (A.14) yields

$$V_c(\omega) = \int_{-\infty}^{\infty} v_{c1}(t)\exp(-j\omega t)dt + H(\omega)P_2(\omega)\left\{\frac{1}{\tau}\sum_{k=-\infty}^{\infty} V_c(\omega + k\omega_o)\right\}, \tag{A.18}$$

and consequently,

$$\tau V_c(\omega) = \tau\int_{-\infty}^{\infty} v_{c1}(t)\exp(-j\omega t)dt + H(\omega)P_2(\omega)\sum_{k=-\infty}^{\infty} V_c(\omega + k\omega_o). \tag{A.19}$$

From equation (A.19), it is necessary to solve for $V_c(\omega)$ in terms of $v_{s1}(t)$, because $v_{s1}(t)$ is a known quantity when the switch is closed. Rearranging the equation by bringing all terms on one side gives,

$$0 = \tau \int_{-\infty}^{\infty} v_{c1}(t)\exp(-j\omega t)dt + H(\omega)P_2(\omega)\sum_{k=-\infty}^{\infty} V_c(\omega + k\omega_o) - \tau V_c(\omega). \qquad \text{(A.20)}$$

Taking one element out of the summation (k=0) and combine it with $V_c(\omega)$ gives,

$$0 = \tau \int_{-\infty}^{\infty} v_{c1}(t)\exp(-j\omega t)dt + H(\omega)P_2(\omega)\sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} V_c(\omega + k\omega_o) + \left[H(\omega)P_2(\omega) - \tau\right]V_c(\omega). \qquad \text{(A.21)}$$

Isolating $V_c(\omega)$ to one side of the equation then yields,

$$\begin{aligned} V_c(\omega) &= \int_{-\infty}^{\infty} V_{c1}(\omega)\exp(-j\omega t)dt + H(\omega)\left\{\frac{1}{D\tau}\sum_{n=-\infty}^{\infty}\int_{-\infty}^{\infty} v_{c1}(t)\exp\left[-j(\omega + n\omega_o)t\right]dt\right\} \\ &\quad \cdot \int_{-\infty}^{\infty} p_2(t)\exp(-j\omega t)dt \\ &= H(\omega)\int_{-\infty}^{\infty} v_{s1}(t)\exp(-j\omega t)dt + H(\omega)\left\{\frac{1}{D\tau}\sum_{n=-\infty}^{\infty}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} h(u)v_{s1}(t-u)du\exp\left[-j(\omega + n\omega_o)t\right]dt\right\} \\ &\quad \cdot \int_{-\infty}^{\infty} p_2(t)\exp(-j\omega t)dt, \end{aligned} \qquad \text{(A.22)}$$

and simplifying it further gives,

$$V_c(\omega) = H(\omega)\int_{-\infty}^{\infty} v_{s1}(t)\exp(-j\omega t)dt + H(\omega)\left\{\frac{1}{D\tau}\sum_{n=-\infty}^{\infty} H(\omega+n\omega_o)\int_{-\infty}^{\infty} v_{s1}(t)\exp\left[-j(\omega+n\omega_o)t\right]dt\right\}$$
$$\cdot\int_{-\infty}^{\infty} p_2(t)\exp(-j\omega t)dt$$
$$= H(\omega)\int_{-\infty}^{\infty} v_{s1}(t)\exp(-j\omega t)dt + H(\omega)\left\{\frac{1}{D\tau}\sum_{n=-\infty}^{\infty} H(\omega+n\omega_o)\exp(-jn\omega_o t)\int_{-\infty}^{\infty} v_{s1}(t)\exp(-j\omega t)dt\right\}$$
$$\cdot\int_{-\infty}^{\infty} p_2(t)\exp(-j\omega t)dt$$

(A.23)

where

$$D = 1-\frac{1}{\tau}\sum_{n=-\infty}^{\infty} H(\omega+n\omega_o)\int_{-\infty}^{\infty} p_2(t)\exp\left[-j(\omega+n\omega_o)t\right]dt, \qquad \text{(A.24)}$$

and then define

$$F = 1+\frac{1}{D\tau}\int_{-\infty}^{\infty} p_2(t)\exp(-j\omega t)dt,$$
$$\omega_o = \frac{2\pi}{\tau}, \text{ and} \qquad \text{(A.25)}$$
$$v_{s1}(t) = v_{s2}(t) = \sum_{k=-\infty}^{\infty} v_c(t)\,p_2(t-k\tau)$$

Combining all of the above expressions, equation (A.23) becomes

$$V_c(\omega) = H(\omega)\int_{-\infty}^{\infty} v_{s1}(t)\left[1+F\sum_{n=-\infty}^{\infty} H(\omega+n\omega_o)\exp(-jn\omega_o t)\right]\exp(-j\omega t)dt. \qquad \text{(A.26)}$$

The above expression has almost reached its final form except the evaluation of the integral for the random signal $v_c(t)$. To do so, the Fourier-Stieltjes integral can be used, where it is defined as

$$v_c(t) = \int_{-\infty}^{\infty} \exp(j\omega' t) dZ(\omega'). \tag{A.27}$$

Therefore, $v_{s1}(t)$ becomes

$$v_{s1}(t) = \sum_{k=-\infty}^{\infty} \int_{-\infty}^{\infty} \exp(j\omega' t) dZ(\omega') p_1(t - k\tau). \tag{A.28}$$

Substituting equation (A.28) into equation (A.26), the expression simplifies to,

$$V_c(\omega) = H(\omega) \int_{-\infty}^{\infty} \left[\sum_{k=-\infty}^{\infty} \int_{-\infty}^{\infty} \exp(j\omega' t) dZ(\omega') p_1(t - k\tau) \right] \left[1 + F \sum_{n=-\infty}^{\infty} H(\omega + n\omega_o) \exp(-jn\omega_o t) \right] \exp(-j\omega t) dt . \tag{A.29}$$

Grouping the exponentials $\exp(j\omega' t)$ and $\exp(-j\omega t)$ generates

$$V_c(\omega) = H(\omega) \int_{-\infty}^{\infty} \left[\sum_{k=-\infty}^{\infty} \int_{-\infty}^{\infty} \exp\left[j(\omega' - \omega) t \right] p_1(t - k\tau) \right] \cdot \left[1 + F \sum_{n=-\infty}^{\infty} H(\omega + n\omega_o) \exp(-jn\omega_o t) \right] dZ(\omega') dt . \tag{A.30}$$

Rearranging the formula, it is evident that there is a Fourier transform integral embedded inside. It is noted that the two integrals, namely dt and $dZ(\omega')$, are

interchangeable. Here, dt is evaluated first and then $dZ(\omega')$ next. The section in the below expression in {} is the aforementioned Fourier integral.

$$V_c(\omega) = H(\omega)\int_{-\infty}^{\infty}\sum_{k=-\infty}^{\infty}\int_{-\infty}^{\infty}\left\{p_1(t-k\tau)\cdot\left[1+F\sum_{n=-\infty}^{\infty}H(\omega+n\omega_o)\exp(-jn\omega_o t)\right]\right\} \exp\left[j(\omega'-\omega)t\right]dtdZ(\omega'). \quad \text{(A.31)}$$

Using the time shifting properties of Fourier transform once again (see equation (A.13)), $p_1(t-k\tau)$ can be further decomposed into,

$$V_c(\omega) = H(\omega)\int_{-\infty}^{\infty}\sum_{k=-\infty}^{\infty}\exp\left[j(\omega'-\omega)k\tau\right]\int_{-\infty}^{\infty}\left\{p_1(t)\cdot\left[1+F\sum_{n=-\infty}^{\infty}H(\omega+n\omega_o)\exp(-jn\omega_o t)\right]\right\} \exp\left[j(\omega'-\omega)t\right]dtdZ(\omega'). \quad \text{(A.32)}$$

To simply the equation to make a less clumsy representation, define

$$K(\omega,\omega') = \int_{-\infty}^{\infty} p_1(t)Q(\omega,t)\exp\left[j(\omega'-\omega)t\right]dt, \quad \text{(A.33)}$$

and

$$Q(\omega,t) = 1+F\sum_{n=-\infty}^{\infty}H(\omega+n\omega_o)\exp(-jn\omega_o t). \quad \text{(A.34)}$$

Then, the compact version of the Fourier transform $V_c(\omega)$ becomes

$$V_c(\omega) = H(\omega)\sum_{k=-\infty}^{\infty}\int_{-\infty}^{-\infty}\exp\left[j(\omega-\omega')k\tau\right]K(\omega,\omega')dZ(\omega'). \quad \text{(A.35)}$$

The final steps of this derivation involve finding the power spectral density using equation (A.35). Recalling the relationship between the Fourier transform of a signal and its PDF is

$$S_c(\omega) = \lim_{N\to\infty} \left\langle V_c(\omega) \cdot V_c^*(\omega) \right\rangle \frac{1}{2\pi\tau(2N+1)}, \tag{A.36}$$

where the point brackets denote the mean ensemble average and $V_c^*(\omega)$ is the complex conjugate of $V_c(\omega)$. Taking the limit to infinity, and assuming the input noise spectrum is white, with period $T = 2\pi\tau$ and R being the resistance yields

$$S_o = \frac{1}{\pi} kTR. \tag{A.37}$$

The expression of $S_c(\omega)$ simplifies to

$$S_c(\omega) = \frac{S_o}{2\pi\tau} \left|H(\omega)\right|^2 \sum_{k=-\infty}^{\infty} \int_{-\infty}^{\infty} \exp\left[j(\omega - \omega')k\tau \right] K(\omega,\omega') \cdot K^*(\omega,\omega') d\omega'. \tag{A.38}$$

Equation (A.38) describes the power spectrum of the noise signal due to reset operation of a TFT. However, for comparison between experimental and model data, the expression thus far is still too complicated. Hence, it is further simplified to provide a more closed form expression.

Using the Poisson's sum formula,

$$S_c(\omega) = S_o \left|H(\omega)\right|^2 \left(\frac{1}{\tau}\right)^2 \sum_{k=-\infty}^{\infty} I(\omega, k\omega_o) I^*(\omega, k\omega_o), \tag{A.39}$$

where

$$I(\omega, k\omega_o) = K(\omega, \omega - k\omega_o) = \int_{-\infty}^{\infty} \exp(-jk\omega_0 t)\, p_1(t) Q(\omega, t) dt. \tag{A.40}$$

Using the Poisson's sum formula again on the summation in equation (A.39), it is possible to write

$$\sum_{k=-\infty}^{\infty} II^* = \tau \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \delta(t' - t - n\tau) \cdot p_1(t)\, p_1^*(t') Q(\omega, t') dt dt'. \tag{A.41}$$

The expression in equation (A.41) has only one non-zero term in the summation, which is when n=0. This allows the entire expression to be written as

$$\begin{aligned} \sum_{k=-\infty}^{\infty} II^* = \tau \int_{\delta/2}^{\tau-\delta/2} & \left[1 + F \sum_{n=-\infty}^{\infty} H(\omega + n\omega_o) \exp(-jn\omega_o t) \right] \\ & \cdot \left[1 + F^* \sum_{m=-\infty}^{\infty} H^*(\omega + m\omega_o) \exp(-jm\omega_o t) \right] dt. \end{aligned} \tag{A.42}$$

The summation and the integration can be carried out in closed form and the result, combining with equation (A.39) yields

$$S_c(\omega) = S_o \left| H(\omega) \right|^2 \left[1 + \zeta + \frac{1}{2}(\omega_f \tau)\zeta^2 F_1 \cdot \mathrm{sinc}^2\left(\frac{\omega\delta}{2} \right) + \zeta F_2 \mathrm{sinc}^2\left(\frac{\omega\delta}{2} \right) \right] \text{ when } R \neq 0, \tag{A.43}$$

where ζ is the complement of the duty cycle for the reset pulse. The definitions for the various quantities are

$$\zeta = \frac{\delta}{\tau}, \tag{A.44}$$

$$\omega_f = \frac{1}{RC}, \tag{A.45}$$

$$\left|H(\omega)\right|^2 = \frac{\omega_f^2}{\omega_f^2 + \omega^2}, \tag{A.46}$$

$$F_1 = \frac{\omega_f^2}{\omega_f^2 + \omega^2} \cdot \frac{\sinh\left[\omega_f(\tau - \delta)\right]}{\cosh\left[\omega_f(\tau - \delta)\right] - \cos(\omega\tau)}, \tag{A.47}$$

$$F_2 = 2\left|H(\omega)\right|^2 \frac{\cos\left(\frac{\omega\tau}{2}\right)\cosh\left[\omega_f(\tau - \delta)\right] - \cos\left[\omega_f\left(\tau - \frac{\delta}{2}\right)\right]}{\cosh\left[\omega_f(\tau - \delta)\right] - \cos(\omega\tau)}. \tag{A.48}$$

The expression $S_c(\omega)$ is the desired expression for the noise-power spectral density of a periodically reset node with reference source having an arbitrary noise level with a white spectrum S_o. In the case when the ON-resistance of the switching transistor and the output resistance of the reference voltage generator is negligible, i.e. $R \to 0$, $S_c(\omega)$ can be simplified. In addition, if $\omega_f \gg 1$ is assumed, the expression will converge to the result as reported by Hynecek [93], i.e.

$$S_c(\omega) = \frac{1}{\pi}\left(\frac{kT}{C}\right)\left[\frac{(1-\zeta)\omega_f}{\omega_f^2 + \omega^2} + \frac{1}{2}\tau\zeta^2 \operatorname{sinc}^2\left(\frac{\omega\delta}{2}\right)\right] \text{ when } R \to 0. \tag{A.49}$$

Appendix B Channel Charge Estimation for Transistor Reset Operation

The TFT reset operation carried out in imaging sensor is associated with reset noise, and the noise power spectrum is derived in Appendix A. Partition noise is closely related to the reset operation, unlike reset noise which originates from thermal fluctuations of conductance in the TFT, it stems from the diffusion of TFT channel charge. As a result, the channel charge profile estimation algorithm in the transistor channel during device turn off is required in order to predict the amount of residual charge and its respective contribution to noise.

Teranishi and Mutoh assume a constant charge density at the onset of transistor pinch off, and use that for the estimation of partition noise [94]. While this assumption simplifies the calculation and proved the existence of partition noise, it lacks the accuracy and typically estimates the noise figure. To improve the accuracy, the charge distribution is calculated numerically by solving the partial differential equation governing current conservation. The results of this formulation predict the charge profile at any time instant during transistor off. This method allows the estimation of residual charge that is to be evacuated through diffusion, which consequently contributes to noise.

Conventional analytical methods for charge distribution estimation do not take into account the diffusion components [100][101]. However, charge transport mechanism after device pinch off is based on diffusion, hence neglecting such current component results in the loss of accuracy on charge evacuation during transistor turn off transients.

Various authors have studied the transients of charge profile during transistor turn off. Notably, Kuo *et al* [102] and Paul Wiercienski [103] studied the reset of floating diffusion or capacitive nodes via active devices. Burns' derived a model for channel charge simulation, but neglected the saturation region of transistor operation altogether [104]. In imaging sensor, the reset TFT operates in the linear regime most of the time, nevertheless, it might enter the saturation regime at the initial stage of reset phase. Hence, it is recommended to consider both saturation and linear regimes of operation of the TFT. Here, the modeling of charge profile begins with the general drift-diffusion current density equation in the transistor channel and it takes the usual form

$$\overrightarrow{J_n} = -q\mu_n n\nabla\varphi + qD_n\nabla n, \tag{B.1}$$

where q is the electron charge, μ_n the electron mobility, φ the potential, D_n the diffusion constant of electrons, and n is the electron concentration. The time-dependent electron current continuity dictates that

$$\frac{\partial n}{\partial t} + \nabla\cdot\left[\frac{-\overrightarrow{J_n}}{q}\right] = G - R, \tag{B.2}$$

where G-R is the net charge generation in the channel. The continuity equation can be decomposed into x- and y- components as follows:

$$\frac{\partial n}{\partial t} + \frac{\partial}{\partial x}\left[\frac{-J_x}{q}\right] + \frac{\partial}{\partial y}\left[\frac{-J_y}{q}\right] = G - R \tag{B.3}$$

where the coordinate axes are set such that the x-axis is parallel to the channel length while the y-axis points towards the substrate. Here, it is assumed that current flow is

restricted to, and flows only, along the channel and there is no component in z-direction. Rewriting equation (B.1) in terms of quasi-fermi potential ϕ_n yields

$$\overrightarrow{J_n} = -q\mu_n n \nabla \phi_n. \tag{B.4}$$

Combining equations (B.3) and (B.4) gives

$$\frac{\partial n}{\partial t} + \mu_n \frac{\partial}{\partial x}\left[n \frac{\partial \phi_n}{\partial x} \right] - \frac{1}{q}\left[\frac{\partial J_y}{\partial y} \right] = G - R. \tag{B.5}$$

In equation (B.5), the substrate current component, J_y, refers to the component of charge pumping stemming from the recombination of trapped electrons and holes from the substrate pinch-off [105][106][107]. However, the thin active layer of typical TFT used in imagers render this current component negligible. In addition, the reference voltage at the drain is at a high potential, therefore any electrons released from the trap will be attracted and are unlikely to contribute to any significant substrate current. As a result, $J_y = 0$ and the net recombination rate, G-R, can also be neglected. Thus, equation (B.5) further reduces to

$$\frac{\partial n}{\partial t} + \mu_n \frac{\partial}{\partial x}\left[n \frac{\partial \phi_n}{\partial x} \right] = 0. \tag{B.6}$$

Integrating the equation through the channel thickness Δ and channel width W yields

$$W \int_0^{\Delta} \frac{\partial n}{\partial t} dt + \mu_n W \int_0^{\Delta} \frac{\partial}{\partial x}\left[n \frac{\partial \phi_n}{\partial x} \right] dy = 0. \tag{B.7}$$

It is noted for a-Si:H, the active layer is thin to minimize the amount of mid-gap defect states, so Δ refers to the active layer thickness. The charge per unit length is defined as

$$Q_n(x,z,t) = qW\int_0^{\Delta} n(x,y,z,t)dy \tag{B.8}$$

where n(x,y,z,t) is the time- and location-dependent channel charge profile. Embedding equation (B.8) leads to a partial differential equation (PDE) in charge and quasi-Fermi potential as

$$\frac{\partial Q_n}{\partial t} + \mu_n \frac{\partial}{\partial x}\left[Q_n \frac{\partial \phi_n}{\partial x} \right] = 0. \tag{B.9}$$

On the other hand, the voltage across the gate oxide can be approximated with the following relations:

$$V(x,t) = \frac{Q_n(x,t)}{C}, \tag{B.10}$$

and,

$$V(x,t) = V_{RST}(t) - \phi_n(x,t) - V_T, \tag{B.11}$$

where C is the gate oxide capacitance per unit length, V_T the TFT threshold voltage, and V_{RST} the reference voltage applied to the TFT drain. Here, the channel profile is assumed to be uniform in the z-direction along the channel width, so Q_n varies only in the x-

direction at any given time instant. Substituting (B.10) and (B.11) into (B.9) and applying the chain rule, we can reduce the differential equation to

$$\frac{\partial V}{\partial t} - \frac{\mu_n}{2}\frac{\partial^2 V^2}{\partial x^2} = 0 \tag{B.12}$$

Equation (B.12) describes the time-dependent gate oxide potential along the channel, and can only be solved numerically. The form of differential equation is well known and has been studied for many years by chemical engineers [108] for gas phase particle diffusion. Here, the work numerical analysis method introduced by Wagner [109] is used and the equation is distretized using the Theta method [110]. The partial differential equation is effectively transformed into a system of algebraic equations as follows:

$$\begin{aligned}&\frac{V_j^{n+1} - V_j^n}{\Delta t} \\ &= \frac{\mu_n}{2(\Delta x)^2}\left\{\theta\left[\left(V^2\right)_{j+1}^{n+1} - 2\left(V^2\right)_{j-1}^{n+1}\right] + (1-\theta)\left[\left(V^2\right)_{j+1}^{n} - 2\left(V^2\right)_{j}^{n} + \left(V^2\right)_{j-1}^{n}\right]\right\}\end{aligned} \tag{B.13}$$

where the subscript j refers to the space increment and n refers to the time increment. For instance, V_j^n refers to the voltage at position J in time n units from t =0. Note that the system of equations contains variables V_j^{n+1} and V_j^n which refers to two time increments. It is advisable to approximate all voltage at time n+1 by voltage information at time increment n in order to simplify the system. This approximation can be performed provided the voltage V does not change too rapidly with time, thus

$$\left(V^2\right)_j^{n+1} \approx \left(V^2\right)_j^n + 2\left(V^2\right)_j^n\left(V_j^{n+1} - V_j^n\right). \tag{B.14}$$

In addition, the difference of voltage between two time instants is defined as

$$W_j = V_j^{n+1} - V_j^n. \tag{B.15}$$

Combining equation (B.15), (B.14), and (B.13) generates

$$-rV_{j+1}^n W_{j+1} + (1+2rV_j^n)W_j - rV_{j-1}^n W_{j-1} = r\left[\left(V^2\right)_{j+1}^n - 2\left(V^2\right)_j^n + \left(V^2\right)_{j-1}^n\right], \tag{B.16}$$

where r is introduced to simply the expression and is

$$r = \frac{\mu_n}{2} \cdot \frac{\Delta t}{\left(\Delta x\right)^2}. \tag{B.17}$$

The systems of equation (B.16), with definitions (B.15) and (B.17) forms a system of J x (J+2) matrix, hence, two more equations outlining the boundary equations are required. The first boundary condition is found by considering the channel potential at t = 0. At t = 0, the conducting transistor channel is biased to the reference voltage (V_{REF}) by the drain side connection. It is therefore safe to approximate the entire channel potential to be constant, hence

$$\phi_n(x, t=0) = 0, \tag{B.18}$$

and

$$\phi_n(x=0, t) = V_{REF} \tag{B.19}$$

states that the drain side of the channel is pinned at V_{REF} due to biasing. Combining equations (B.18) and (B.19) gives the first boundary condition as

$$W_0 = V_{RST}^{n+1} - V_{RST}^{n}. \tag{B.20}$$

The second boundary condition considers the source side of the TFT that is connected to the integration node capacitance. C_N The potential at that node is given by the potential generated by C_N and is

$$\phi_n(x=L,t) = -\frac{1}{C_N}\int_0^t \mu_n Q_n(x=L,t)\left.\frac{\partial \phi_n(x,t)}{\partial x}\right|_{x=L} dt. \tag{B.21}$$

The differential equation (B.21) can also be transformed using the Theta method, and it takes the form

$$-\frac{\alpha}{2}V_J^n W_{J-1} + W_J + \frac{\alpha}{2}V_J^n W_{J+1} = V_{RST}^{n+1} + \frac{\alpha}{2}V_J^n V_{J-1}^n - \frac{\alpha}{2}V_J^n V_{J+1}^n, \tag{B.22}$$

where

$$\alpha = \frac{\mu_n C \Delta t}{C_N \Delta x}. \tag{B.23}$$

The equations (B.22), (B.16), and (B.13) forms J+2 equations and J+2 unknowns. The numerical solution can be obtained for the voltage along the channel for any given time step. The system of equation is formulated such that all the non-zero elements lie in the three principle diagonals, forming a tri-diagonal matrix. The resulted matrix takes the form.

$$
\begin{bmatrix}
1 & & & & & & & \\
-rV_0^n & 1+2rV_1^n & -rV_2^n & & & & & \\
 & -rV_1^n & 1+2rV_2^n & -rV_3^n & & & & \\
 & & \cdots\cdots\cdots & & & & & \\
 & & & -rV_{J-2}^n & 1+2rV_{J-1}^n & -rV_J^n & & \\
 & & & & -rV_{J-1}^n & 1+2rV_J^n & -rV_{J+1}^n & \\
 & & & & -\frac{\alpha}{2}V_J^n & 1 & \frac{\alpha}{2}V_J^n &
\end{bmatrix}
\bullet
$$

$$
\begin{bmatrix} W_0 \\ W_1 \\ W_2 \\ \cdots \\ W_{J-1} \\ W_J \\ W_{J+1} \end{bmatrix}
=
\begin{bmatrix}
V_{RST}^{n+1} - V_{RST}^n \\
r\left[\left(V^2\right)_2^n - 2\left(V^2\right)_1^n + \left(V^2\right)_0^n\right] \\
r\left[\left(V^2\right)_3^n - 2\left(V^2\right)_2^n + \left(V^2\right)_1^n\right] \\
\cdots\cdots\cdots \\
r\left[\left(V^2\right)_J^n - 2\left(V^2\right)_{J-1}^n + \left(V^2\right)_{J-2}^n\right] \\
r\left[\left(V^2\right)_{J+1}^n - 2\left(V^2\right)_J^n + \left(V^2\right)_{J-1}^n\right] \\
\frac{\alpha}{2}V_J^n\left[V_{J-1}^n - V_{J+1}^n\right] + V_{RST}^{n+1} - V_{RST}^n
\end{bmatrix}. \tag{B.24}
$$

The system of equations (B.24) can be numerically solved using any mathematical software packages. It is noted that an appropriate time and spatial increment should be chosen to provide a sufficiently accurate solution within reasonable simulation time. In addition, the convergence of the matrix system depends on the value of θ in the expression, which is the Theta transformation parameter. Setting $\theta = 0.5$ generates the Crank-Nicholson formulation [111], it is chosen because of its excellent convergence.

Appendix C Parameter Extraction

Parameter extraction methods provide a valuable means for correlating TFT models with the device fabrication process. The improvements to the technology require accurate extraction of model parameters, and such practice can be complex and falls in the category of device characterization. Methods for parameter extraction for crystalline silicon based transistors such as MOSFETs have been studied for years by various authors [112] [113]. Robust optimizations method to extract threshold voltage, effective channel length, and mobility are presented by [113] and [114] taking device non-idealities such as series resistance into consideration.

This chapter presents reliable extraction methods for different operating regimes of a-Si:H TFTs. Here, the extraction methods of above-threshold parameters including effective mobility, threshold voltage, power parameter, and contact resistance are presented. Methods of parameter extraction in TFT reverse and subthreshold regimes are investigated afterwards.

This section presents methods for extraction of model parameters associated with the steady-state (static) current-voltage characteristics of the TFT. The static characteristics can be divided into three distinct regions, i.e., above-threshold, subthreshold, and Poole-Frenkel.

C.1 Above-Threshold

We start with the methods of extractions for the above-threshold parameters. It is important to note that in this region, the TFT provides the highest current level. Thus, the

effect of contact resistance and its properties is mostly visible and should be systematically characterized.

Above-threshold parameters such as mobility and threshold voltage for MOSFETs are conventionally extracted from the current in the linear region. For an n-type MOSFET, the linear current reads

$$I_{DS,lin} = \mu_{FE} \frac{W}{L} C_i (V_{GS}^{'} - V_T) V_{DS}^{'} \tag{C.1}$$

where μ_{FE} is the electron field-effect mobility. Other parameters are defined similar to a TFT. μ_{FE} may be found as

$$\mu_{FE} = \frac{L}{C_i W V_{DS}^{'}} \frac{\partial I_{DS,lin}}{\partial V_{GS}^{'}} \tag{C.2}$$

In other words the slope of the best fit to the I_{DS} versus V_{GS} curve provides information on mobility while the intercept on the horizontal axis yields the threshold voltage. Due to mobility degradation by virtue of surface scattering at high voltages, the fit at low voltages (or other words, maximum g_m) is considered for extraction for V_T. This is referred to as the maximum g_m method [112].

Power Parameter (α), Threshold Voltage, and Contact Resistance

Although the extraction method for a-Si:H TFTs can be based on the conventional methods for MOSFETs, it may be more complex by virtue of the departure from the square law dependence of current-voltage characteristics. In a-Si:H TFTs, the power

parameter is related to the band tail states and needs to be extracted. If the square law relationship is assumed, inaccuracy of the model will be resulted [116]. Cerdeira *et al.* [116] have included the effect of α in a unified extraction method, based on the AIM-SPICE model. Here, and integral technique is used to extract α and threshold voltage (V_T) simultaneously. We refer to this as the integral method. In this method, the current measurement data $_{IDS,\,lin}$ in the linear region (V_{DS} = 50-100 mV) is used to numerically calculate $H(V_{GS})$ as a function of V_{GS} according to

$$H(V_{GS}) = \frac{\int_0^{V_{GS}} I(V_{GS}'')dV_{GS}''}{I(V_{GS})} \tag{C.3}$$

In addition, parametric integration over the ideal linear characteristics of the TFT yields $H(V_{GS}) = (V_{GS} - V_T)/ \alpha$, which predicts a linear behavior for $H(V_{GS})$ as a function of V_{GS}. As a result, the slope and intercept on the horizontal axis of the best fit to the plot of $H(V_{GS})$ as a function of V_{GS} may yield α and V_T, respectively.

Although the integral method is powerful when the results follow the ideal current equation, in the presence of non-idealities such as contact resistance it can introduce errors in the extracted values. These non-idealities may vary by orders of magnitude due to process variations, thus strongly influencing the extracted values. Therefore, the impact of such non-idealities is not rigorously treated in the integral method, which must be systematically investigated and accounted for.

The method above suggests that the contact resistance, power parameter and threshold voltage should be extracted simultaneously. The sequence for parameter

extraction should start with estimation for the value of contact resistance. For this estimation, we need two TFTs with different channel lengths, namely L_{min} and L_{max}. The measured resistance between drain and source terminals for these TFTs ($R_{DS} = V_{DS}/I_{DS,lin}$) is then scaled by the ratio of the channel lengths, i.e. $k = L_{min}/L_{max}$. The contact resistance is the dominant part of the measured resistance for small channel length TFTs, while its numerical significance prevails for long channel TFTs. The TFT contact resistance can then be normalized using this ratio (k).

Having estimated R_{DS}, α and V_T can be extracted. Here, we introduce a mathematical method similar to the integral method. From the linear and saturation I_{DS} equations,

$$I_{DS,lin} = \mu_{eff}\zeta\frac{W}{L}C_i^{\alpha-1}(V_{GS}^{'} - V_T)^{\alpha-1}V_{DS}^{'} \tag{C.4}$$

and

$$I_{DS,sat} = \frac{\mu_{eff}}{\alpha}\zeta\frac{W}{L}\gamma_{sat}C_i^{\alpha-1}(V_{GS}^{'} - V_T)^{\alpha}x_{cm} \tag{C.5}$$

We obtain

$$\frac{I_{DS,lin}}{g_{m,lin}} = \frac{V_{GS} - V_T - 0.5V_{DS}}{\alpha - 1}\frac{V_{DS}}{V_{DS} - R_{DS}I_{DS,lin}} \tag{C.6}$$

and

$$\frac{I_{DS,sat}}{g_{m,sat}} = \frac{V_{GS} - V_T + 0.5R_{DS}I_{DS,sat}(\alpha - 1)}{\alpha} \tag{C.7}$$

where parameters $g_{m,sat}$ and $g_{m,lin}$ are defined as

$$g_{m,lin} \equiv \frac{\partial I_{DS,lin}}{\partial V_{GS}} \text{ and } g_{m,sat} \equiv \frac{\partial I_{DS,sat}}{\partial V_{GS}} \tag{C.8}$$

respectively [117][118]. The left hand side of equations can be determined from the data obtained in the linear and saturation regions. Assuming the contact resistance related terms are negligible in these equations (i.e. $R_{DS}I_{DS,lin} << V_{DS}$ and $R_{DS}I_{DS,sat} <<$VGS-VT for linear and saturation regions, respectively), we have

$$\frac{I_{DS,lin}}{g_{m,lin}} = \frac{V_{GS} - V_T - 0.5V_{DS}}{\alpha - 1} \text{ and } \frac{I_{DS,sat}}{g_{m,sat}} = \frac{V_{GS} - V_T}{\alpha}. \tag{C.9}$$

Thus, for the low contact resistance case ($R_{DS}W$ < 0.5 kΩ-cm), a plot of $I_{DS,lin}/g_{m,lin}$ or $I_{DS,sat}/g_{m,sat}$ versus V_{GS} must be a straight line whose slope and intercept on the horizontal axis yield α and V_T, respectively. This is similar to the result of the integral method.

However, for the high contact resistance scenario ($R_{DS}W$ > 0.5 kΩ-cm), the value of α extracted has a significant error due to the simplification. Here, we modify the $I_{DS,lin}/g_{min,lin}$ and $I_{DS,sat}/g_{m,sat}$ values calculated from the measurements results to find

$$\left(\frac{I_{DS,lin}}{g_{m,lin}}\right)_1 = \left(\frac{I_{DS,lin}}{g_{m,lin}}\right)\frac{V_{DS} - R_{DS}I_{DS,lin}}{V_{DS}}. \tag{C.10}$$

$$\left(\frac{I_{DS,sat}}{g_{m,sat}}\right)_1 = \left(\frac{I_{DS,sat}}{g_{m,sat}}\right) - (1 - 1/\alpha)R_{DS}I_{DS,sat}/2. \tag{C.11}$$

Now, plots of $\left(\frac{I_{DS,lin}}{g_{m,lin}}\right)_1$ and $\left(\frac{I_{DS,sat}}{g_{m,sat}}\right)_1$ versus V_{GS} contain minimal contact resistance induced errors [117]. For measurement results in saturation (V_{DS} = 20 V), the channel length modulation effect can also cause error in the extracted parameters and hence should be considered. In this case, we modify the $I_{DS,sat}/g_{m,sat}$ values for both contact resistance and channel length modulation effects using

$$\left(\frac{I_{DS,sat}}{g_{m,sat}}\right)_2 = \left(\left(\frac{I_{DS,sat}}{g_{m,sat}}\right) - (1-\kappa/\alpha)R_{DS}I_{DS,sat}/2\right)/\kappa, \tag{C.12}$$

where

$$\kappa^{-1} = 1 - \frac{\lambda R_{DS} I_{DS,sat}}{1+\lambda V_{DS}}. \tag{C.13}$$

Here, λ is the channel length modulation parameter. The modified versions for both linear and saturation regions will yield different slopes (i.e., different values of α), highlighting the significance of contact resistance on the extracted values. This is even more pronounced in the linear region.

In summary, the value of α should be extracted from $(I_{DS,lin}/g_{m,lin})_1$ and then verify by the $(I_{DS,sat}/g_{m,sat})_2$. It should be noted that $I_{DS,sat}/g_{m,sat}$ is less sensitive to effects of contact resistance in comparison to $I_{DS,lin}/g_{m,lin}$.

Based on the extracted value of α, V_T can be extracted fro TFTs with different channel length using the best fit to the $I_{DS,lin}^{1/(\alpha-1)}$ versus V_{GS} graph at small currents, where the contact resistance induced error is trivial.

Having extracted α and V_T, we can find a more accurate value for contact resistance using the measurement results for TFTs with different channel lengths. The measured resistance of a TFT with unit width (R_mW) can be written as

$$R_m W = \frac{V_{DS}}{I_{DS.lin}} W = R_{DS} W + \frac{L_{eff} + \Delta L}{\mu_{eff} \zeta C_i^{\alpha-1} (V_{GS} - V_T)^{\alpha-1}} = R_{DS} W + R_{ch}(L_{eff} + \Delta L), \quad \text{(C.14)}$$

where L is substituted for $L_{eff} + \Delta L$. Here, the effective channel length L_{eff} is the value that provides good agreement between theory and experiment. Similar to MOSFETs, L_{eff} may differ from the mask-defined and physical channel length L due to channel enlargement at the edge of the source and the drain contacts. According to the above equation, R_mW versus L curves plotted for different values of V_{GS} should have an intercept point with coordinates L and $R_{DS}W$ [115]. Note that since each transistor has an identical V_T, the measured data must be corrected to have a constant applied (V_{GS}-V_T) for each curve.

To determine the intercept point (L, $R_{DS}W$) more accurately [114], equation (14) is rewritten as

$$R_m W = R_{ch} L + B, \quad \text{(C.15)}$$

where

$$B = R_{DS} W + R_{ch} \Delta L. \quad \text{(C.16)}$$

Equation (16) indicates that a plot of B as a function of R_{ch} is a line with $R_{DS}W$ and L as the ordinate intercept point and the slope, respectively. The accuracy of the

extracted values for $R_{DS}W$, L, V_T, and α may be further improved through an iterative process.

Effective mobility

A plot of $R_{ch}^{-1/(\alpha-1)}$ versus V_{GS}-V_T can be used to extract the effective mobility since the impact of contact resistance, power parameter, and the threshold voltage variation is included in R_{ch}. This contact resistance included (CRI) mobility plot is similar to the $_{IDS,lin}$/W versus V_{GS} curve used to extract mobility in MOSFETs. The slope (s) of the best fit to the CRI curve may be used to find μ_{eff} as

$$\mu_{eff} = \frac{1}{\zeta}\left(\frac{s}{C_i}\right)^{\alpha-1}. \tag{C.17}$$

Saturation parameters

For extraction of α_{sat} (or γ_{sat}), the measurement data in saturation region (V_{DS} = V_{GS} or V_{DS} = 20 V) for the TFT with maximum channel length is used so as to minimize contact resistance effects. Based on the I_{DS} current equation in saturation region, the slope S of the best fit to the $(I_{DS,sat}L_{eff}/W)^{1/\alpha}$ versus V_{GS} curve for the long channel TFT yields γ_{sat} as,

$$\gamma_{sat} = \frac{\alpha S^{\alpha}}{\mu_{eff}\zeta C_i^{\alpha-1}x_{cm}}. \tag{C.18}$$

The parameter α_{sat} may then be found using

$$\alpha_{sat} = 1-\left(1-\gamma_{sat}\right)^{1/\alpha}. \tag{C.19}$$

Since the channel length modulation effect decreases with increasing channel length, it is more accurate to extract λ from the output characteristics (I_{DS} versus V_{DS}) of the TFT with minimum channel length. Here, $\lambda = L_{eff} / V_A$, where V_A is the Early voltage and is defined in the usual sense as the absolute value f the intercept on the V_{DS} axis.

Finally, we define

$$k_m = \frac{I_{DS}(V_{DS} = V_{DSat})}{I_{DS,sat}}, \tag{C.20}$$

where $I_{DS,sat}$ and $I_{DS}(V_{DS}=V_{DSat})$ are the saturation current and the current at $V_{DS} = V_{DSat}$ of the TFT at high V_{GS}, respectively. Then, the smoothness parameter m maybe found as

$$m = \left[\log_2 \frac{\alpha_{sat}}{1-(1-k_m\gamma_{sat})^{1/\alpha}} \right]^{-1}. \tag{C.21}$$

C.2 Subthreshold

For extraction of subthreshold parameters, the current-voltage characteristics in the gate bias range of -10 to 2 V is considered. This includes both forward and reverse subthreshold regions and their corresponding parameters. Here, the measurement results for the drain bias of V_{DS} = 20 V is considered. The delay for the measurement of the current in the reverse subthreshold should be selected up to 1 min due to the slow transients in the off state.

Of importance are the forward and reverse subthreshold slopes (i.e., the voltage needed for the current to change by one order of magnitude, with the unit of V/dec), which are measures for sensitivity of the TFT character to the gate bias. In particular, the

forward subthreshold slope is a determining performance parameter, which describes the sensitivity of the TFT current to the gate bias during the turn on process. A smaller subthreshold slope is preferable and iplies that the TFT requires less voltage for transition from off to on state. The voltage needed to move the TFT from off to on state ($\Delta V_{turn-on}$) in simple terms is given by

$$\Delta V_{turn-on} = S_f \log(I_{ON} / I_{off}) \tag{C.22}$$

where I_{on} and I_{off} are the corresponding on and off current levels. The subthreshold slope S_f is simply the slope of the best fit to the logarithmic current plot (in base 10). The subthreshold slope can be related to the effective capacitances of the front interface and deep states by

$$C_{ssf} + C_d = C_i(S_f / 2.3V_{th} - 1) \tag{C.23}$$

For example, as subthreshold slope of $S_f = 0.45$ V/dec yields $C_{ssf} = 49$ nF/cm^2 or $D_{ssf} = 3\times10^{11}$ /cm^2 / eV for the front interface. Here, C_d is found as 83 nF/cm^2 based on the approximate values for the DOS and considering $\psi_{sb} = 0.2\ eV$.

Similarly, the reverse subthreshold slope can be related to the effective capacitance at the back interface by

$$\psi_{sf} + \psi_{sb} = \frac{C_{ssb}}{C_s}\left(\psi_{sb0} - \psi_{sb}\right) - \frac{C_d}{C_s}\psi_{sf} \tag{C.24}$$

where ψ_{sf} is the front interface potential, ψ_{sb} the back interface potential, ψ_{sb0} the no voltage band bending, C_{ssb} the effective back interface capacitance, C_s the semiconductor

layer capacitance, and C_d the effective capacitance of the deep states in the a-Si:H bulk ($C_d = q\frac{\partial n_d}{\partial \psi_{sf}} \sim \frac{q^2 N_{di} t_s}{kT_{dc}} \exp\left(q\psi_{sf} / kT_{dc}\right)$). A reverse subthreshold of S_r = 1.3V/dec results in C_{ssb} = 230 nF/cm^2 and hence a (high) density of states as D_{ssb} = 1.43 x 10^{12} /cm^{2}eV for the back interface. The transition from forward to reverse subthreshold region is identified by the change in the slope of the current logarithmic plot. The voltage and current at the knee are assumed to be V_{TS} and I_{sub0} as defined by equation (C.24).

C.3 Poole-Frenkel Regime

The exponential behavior of the current at high negative gate voltages may be related to parameters such as V_{pf} and J_{pf0}. These values can be simply extracted from the slope and magnitude of the logarithmic plot of current as a function of voltage. Conventionally, the Poole-Frenkel current is written in terms of the electric field (E) as $J_{pf0}\exp(\beta\sqrt{E})$, β is the field-enhancement factor (=1/E_{pf}), which is given by the following:

$$\beta = t_{sc,\min} / V_{pf}. \tag{C.25}$$

Here, $t_{sc,\min}$ is screening parameter and is defined by

$$t_{sc,\min} = t_s(1 + C_s / C_i). \tag{C.26}$$

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