# Electrostatic Discharge Protection Circuit for High-Speed Mixed-Signal Circuits

by

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# Abstract

ESD, the discharge of electrostatically generated charges into an IC, is one of the most important reliability problems for ultra-scaled devices. This electrostatic charge can generate voltages of up to tens of kilovolts. These very high voltages can generate very high electric fields and currents across semiconductor devices, which may result in dielectric damage or melting of semiconductors and contacts. It has been reported that up to 70% of IC failures are caused by ESD. Therefore, it's necessary to design a protection circuit for each pin that discharges the ESD energy to the ground. As the devices are continuously scaling down, while ESD energy remains the same, they become more vulnerable to ESD stress. This higher susceptibility to ESD damage is due to thinner gate oxides and shallower junctions. Furthermore, higher operating frequency of the scaled technologies enforces lower parasitic capacitance of the ESD protection circuits. As a result, increasing the robustness of the ESD protection circuits with minimum additional parasitic capacitance is the main challenge in state of the art CMOS processes.

Providing a complete ESD immunity for any circuit involves the design of proper protection circuits for I/O pins in addition to an ESD clamp between power supply pins. In this research both of these aspects are investigated and optimized solutions for them are reported. As Silicon Controlled Rectifier (SCR) has the highest ESD protection level per unit area, ESD protection for I/O pins is provided by optimizing the first breakdown voltage and latch-up immunity of SCR family devices. The triggering voltage of SCR is reduced by a new implementation of gate-substrate triggering technique. Furthermore, a new device based on SCR with internal darlington pair is introduced that can provide ESD protection with very small parasitic capacitance. Besides reducing triggering voltage, latch-up immunity of SCR devices is improved using two novel techniques to increase the holding voltage and the holding current.

ESD protection between power rails is provided with transient clamps in which the triggering circuit keeps the clamp "on" during the ESD event. In this research, two new

clamps are reported that enhance the triggering circuit of the clamp. The first method uses a CMOS thyristor element to provide enough delay time while the second method uses a flip flop to latch the clamp into “on” state at the ESD event. Moreover, the stability of transient clamps is analyzed and it’s been shown that the two proposed clamps have the highest stability compared to other state of the art ESD clamps.

Finally, in order to investigate the impact of ESD protection circuits on high speed applications a current mode logic (CML) driver is designed in 0.13μm CMOS technology. The protection for this driver is provided using both MOS-based and SCR-based protection methods. Measurement results show that, compared to MOS-based protection, SCR-based protection has less impact on the driver performance due to its lower parasitic capacitance.

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# Chapter 1

# 1. Introduction

## 1.1 Motivation

One of the most well known sources of electrostatic charge is the shock caused by touching a doorknob after walking in a carpeted room. Rubbing shoes on the carpet creates electrostatic charge in the body which is discharged by touching the conductive object. Normally, this electrostatic voltage can be as high as a few kilo-volts. As the voltage created during this event is very high, a discharge through a semiconductor device can result in its failure. This phenomenon is called ElectroStatic Discharge (ESD). A more general definition of ESD is charge transfer between any two objects with different potentials.

In semiconductor industry, ESD is considered as a subset of a class of failures called Electrical OverStress (EOS). EOS represents failures caused by applying conditions outside the designated operating range. These conditions can be voltage, current or temperature. EOS is usually divided into three categories [1]

1. EOS specific: In this category a relatively small voltage (i.e. 16V) is applied to the device for a long period of time (i.e. 1-10ms). In this category the delivered power is low.
2. ESD: In this category a high voltage (i.e. 1-15kV) is applied to the device in a short period (i.e. 1-100ns). The delivered power in this category is low as well.
3. Lightning: This category involves extreme high voltage and power.

The importance of ESD in semiconductor industry can be appreciated by examining the rate of failures caused by ESD. These data are usually provided by different semiconductor companies. It has been reported that, based on the design and application of the circuits, 23% to 72% of total failures in semiconductor industry are caused by ESD/EOS [2]. Therefore, it's necessary to understand this phenomenon and design protection circuits against it. These protection circuits should be able to discharge the ESD energy while having minimal impact on normal circuit behavior. Before discussing the details of protection methods the nature of electrostatic charge and its interaction with semiconductor circuits should be understood.

Static electricity is the creation of electrical charge by an imbalance of electrons on the surface of a material. The most common mechanism of charging an object is triboelectric charging, which is the creation of charge by contact and separation of two materials. Consider contact and separation of two uncharged objects. Based on the nature of these two materials, electrons transfer from one object to the other. Therefore, one of the objects is negatively charged while the other one is positively charged. The amount and polarity of this electrostatic charge depends on the characteristic of the two materials in addition to the contact area, speed of separation, and relative humidity. Electrical characteristic of materials is often determined by their position in the triboelectric series table. Table 1-1 shows a part of the triboelectric series table that compares electrical property of different materials [3]. It can be seen that air and human skin are capable of carrying the most positive charge, while Teflon and silicon are capable of carrying the most negative charge. In addition to generation of charge, the ability to store the generated charge is another important characteristic of materials. Insulators, due to their very high resistance, are capable of storing a huge amount of electrostatic charge. On the

other hand, conductors, due to their very low resistance, are not able to store any charge. Table 1-2 compares the average stored electrostatic charge under different conditions [4].

*Table 1-1: A typical triboelectric series table*

| Material | Electrostatic Polarity |
|---|---|
| Air | Most Positive (+) |
| Human skin | |
| Glass | |
| Human hair | |
| Wool | |
| Paper | |
| Nickel, copper | |
| Polyester (mylar) | |
| Polystyrene (styrofoam) | |
| Saran | |
| Polyvinyl chloride | |
| Silicon | |
| Teflon | Most Negative (-) |
| Silicon rubber | |

*Table 1-2: Electrostatic charge stored in different objects*

| Condition | Average Reading (V) |
|---|---|
| Person walking across linoleum floor | 5000 |
| Person walking across carpet | 15000 |
| Ceramic dips in plain plastic tube | 700 |
| Ceramic dips in plastic set-up trays | 4000 |
| Circuit packs as bubble plastic cover removed | 20000 |
| Circuit packs (packaged) as returned for repair | 6000 |

It can be seen that the amount of stored electrostatic charge during regular use or assembly steps can easily exceed a few kilo-volts. These high voltages can create high

currents and high electric fields in semiconductor devices. High currents can melt different regions of the semiconductor structure, while high electric fields can rupture dielectrics. In sub-micron CMOS technologies, due to very thin oxide dielectrics, gate oxide breakdown is the most common ESD failure mechanism. A simple analysis gives a better understanding of the maximum allowed voltages in submicron CMOS technologies. Consider a 0.18μm CMOS technology where gate oxide thickness ($t_{ox}$) is 40Å and supply voltage is 1.8V. In this technology, under DC conditions, the maximum electric field that the gate oxide can tolerate ($E_{max}$) is around 10MV/cm. Hence, the maximum allowed DC voltage that can be applied across the gate oxide is:

$$V_{max} = E_{max} t_{ox} = 10 \times 10^{6} \times 40 \times 10^{-8} = 4V \quad (1\text{-}1)$$

As a result, a few kilovolts across this device can easily destroy the transistor. The ESD problem becomes even worse as the technology scales into deep sub-quarter-micron technologies and oxide thickness becomes smaller. Furthermore, by scaling the technology, junction depths are becoming shallower as well, which makes the devices more susceptible to ESD damage. In advanced CMOS technologies, in addition to scaling devices, the operating frequency of circuits is increasing as well. Hence, parasitic capacitance of the I/O pad should be minimized. As a result, the additional parasitic capacitance that can be added by the ESD protection circuit is limited. It can be seen that the design of an optimum ESD protection circuit is becoming an increasingly challenging task.

In the next few sections of this chapter, different models for ESD event are discussed and the two most common protection schemes are presented.

## 1.2 ESD Failure Mechanisms

ESD failures are caused by at least one of these sources: high current densities, high electric field intensities. The current densities associated with ESD stress cause high power dissipation in semiconductor devices. As a result, the lattice temperature increases which often results in thermal damage. Furthermore, silicon has a negative resistance relationship with temperature. Hence, very high power dissipation in a small volume

results in higher temperature and thermal runaway. For CMOS circuits, the electric field intensity refers to the voltage developed across the dielectric and junctions of the device. As the gate oxide is the thinnest dielectric of a CMOS circuit, it is the most vulnerable dielectric to ESD damage. This damage is in the form of oxide breakdown. Oxide breakdown can be either soft or hard. In soft breakdown, the performance of the transistor is not significantly changed, however the leakage is increased. On the other hand, after hard breakdown a current path is created from the gate to the channel and the transistor is destroyed.

ESD induced failures can be grouped in two categories: soft and hard failures [3]. In case of soft failure, the device has a partial damage typically resulting in an increased leakage current that might not meet the requirements for a given logic. Still, the basic functionalities of the device are operative but without any guarantee about potential latency effects. In case of hard failures, the basic functionalities of the device are completely destroyed during the ESD event.

## 1.3 Modeling the ESD Event

In order to design an ESD protection circuit the impact of ESD on integrated circuits must be quantified. Therefore, an electrical model for the ESD event should be developed. Depending on the nature of interaction between the charged object and the semiconductor device (which is called Device Under Test or DUT) three different models have been developed for the ESD phenomenon [4].

1. **Human Body Model (HBM):** This model considers the impact of touching the DUT by a charged person. This model usually represents the handling of ICs by a human. In this case, the body discharges to ground through the semiconductor device. Figure 1-1 shows the standard model for an HBM ESD event. In this model, $C_b$ and $R_b$ represent the human body capacitance and resistance respectively. When the switch is in state ‘A’, the capacitance is charged to a predetermined voltage ($V_{ESD}$) and when the switch is in state ‘B’, this electrostatic charge discharges through the DUT.

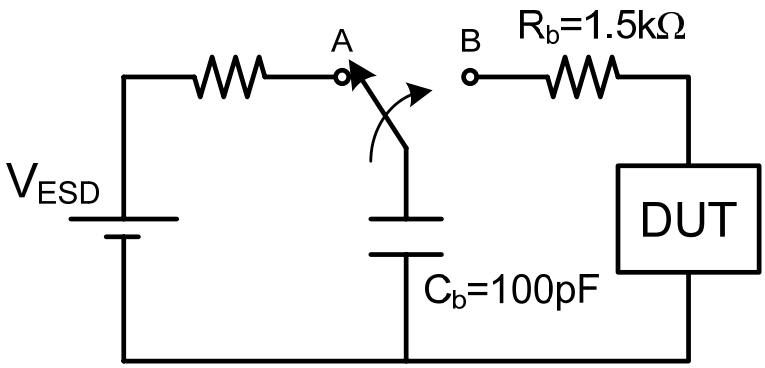


*Figure 1-1: Human body model*

2. **Machine Model (MM):** The discharge of a charged machine through the DUT is modeled with machine model, which represents the handling of the DUT by robots and other machines. Therefore, $R_b$ and $C_b$ in human body model are replaced by the impedance of a charged machine. This model is shown in Figure 1-2.

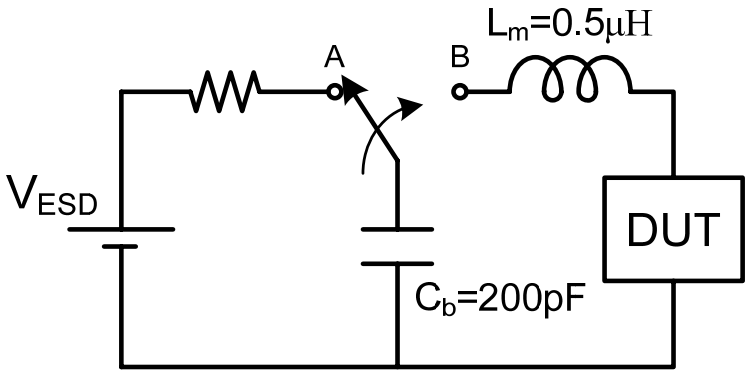


*Figure 1-2: Machine model*

3. **Charged Device Model:** This model considers the effect of the discharge of a charged device by coming in contact with grounded equipments. Usually the IC packages get charged during automated assemblies and tests. This charge can be discharged to ground and cause damage to the IC. Figure 1-3 shows the electrical model for the CDM event.

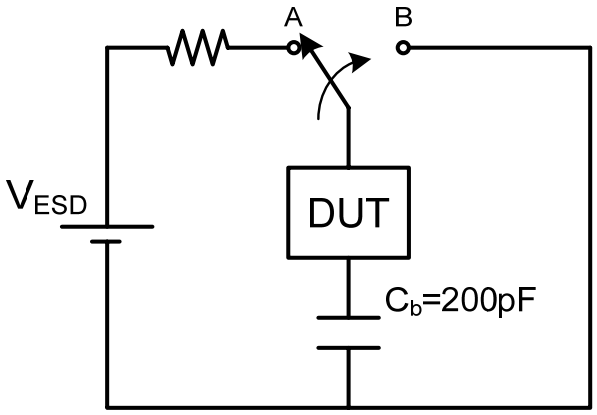


*Figure 1-3: Charged device model*

As the nature of ESD event is different in each model, different requirements are associated with each model as well. Usually for HBM, the minimum protection level is 2kV, for MM the minimum protection level is 200V and for CDM is 500V [1]. HBM and MM are related together. A protection circuit with HBM protection level of 2kV has around 100V MM protection level [1]. On the other hand, since CDM model is completely different from HBM and MM, there isn't such a correlation between CDM and other models. Therefore, CDM and HBM tests are more common to test ESD protection circuits. Figure 1-4 shows typical current waveforms for HBM, MM and CDM events.

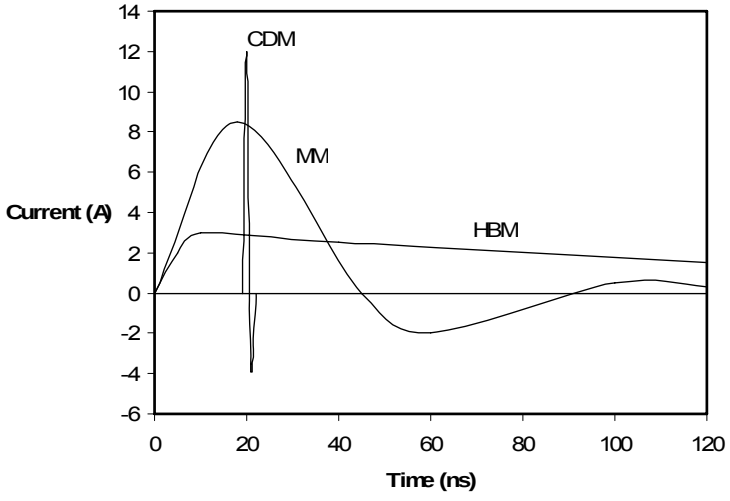


*Figure 1-4: Comparing HBM, MM and CDM models*

It can be seen that CDM has higher peak with smaller duration compared to HBM. Due to higher frequency of the CDM event, it is more sensitive to parasitics in the test hardware. Furthermore, since the capacitance of different packages is different, CDM is sensitive to packages as well. For example, it is reported that considering a maximum tolerable current of 8A the CDM protection level for a chip with the TQFP package is 750V while this value for the u*BGA package is 1200V [1].

## 1.4 ESD Zapping Modes

Depending on the polarity of electrostatic charge and the discharge path, four possible zapping modes exist for an ESD event [4]. These modes are called PS-mode, NS-mode, PD-mode and ND-mode. Figure 1-5 shows the discharge path for these zapping modes.

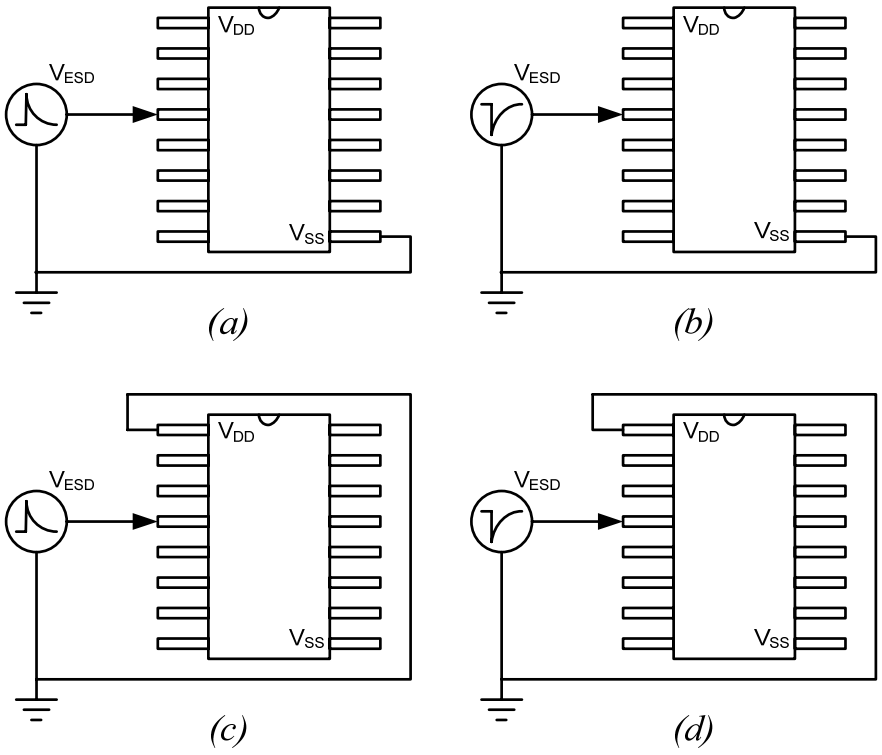


*Figure 1-5: Zapping modes: (a) PS-mode (b) NS-mode (c) PD-mode (d) ND-mode*

In PS-mode ESD event, a positive ESD voltage is applied to an I/O pin as $V_{SS}$ node is grounded. In this mode the rest of the pins including $V_{DD}$ are floating and ESD current

discharges through $V_{SS}$ pin. This zapping mode is shown in Figure 1-5(a). With a similar setup, in NS-mode, a negative ESD voltage is applied to an I/O pin as $V_{SS}$ node is grounded (Figure 1-5(b)). On the other hand, in PD-mode stress, a positive ESD voltage is applied to an I/O pin, while $V_{DD}$ node is grounded and the rest of the pins including $V_{SS}$ are floating. This zapping mode is shown in Figure 1-5(c). Finally, in ND-mode stress, a negative ESD voltage is applied to an I/O pin and discharges through $V_{DD}$ node as shown in Figure 1-5(d).

ESD protection circuits for advanced submicron CMOS ICs should provide an effective ESD discharging path from input and output pads to both $V_{SS}$ and $V_{DD}$ power lines. This is especially necessary for nanometer CMOS circuits with larger chip size and longer $V_{DD}$ and $V_{SS}$ power rails with higher parasitic resistances and capacitances [5].

The ESD failure threshold of a pin is defined as the lowest (in absolute value) ESD-sustaining voltage of the four-mode ESD stresses on the pin. For example, if an output pin can sustain even up to 4 kV ESD voltage in the PS, NS, and PD mode ESD stresses, but can only sustain 1 kV ESD voltage in the ND mode ESD stress, the ESD failure threshold for this output pin is defined as 1 kV only.

## 1.5 ESD Protection Methods

As mentioned in the previous section, ESD stress can be in four different forms: PS, NS, PD and ND modes. Therefore, for each I/O pin, ESD protection for all four zapping modes should be provided. Furthermore, one ESD protection circuit is necessary between $V_{DD}$ and $V_{SS}$ lines, which is called DS protection. As a result, complete ESD protection scheme for each IC should be in the form of Figure 1-6 [6].

In more complicated chips, where more than one supply voltage exists, extra ESD protection circuits should be added between different power supply pads as well. In order to understand possible ESD discharge paths in a typical CMOS circuit, consider a simple buffer which consists of a PMOS and an NMOS transistor. Figure 1-7 shows the schematic and cross section of this buffer.

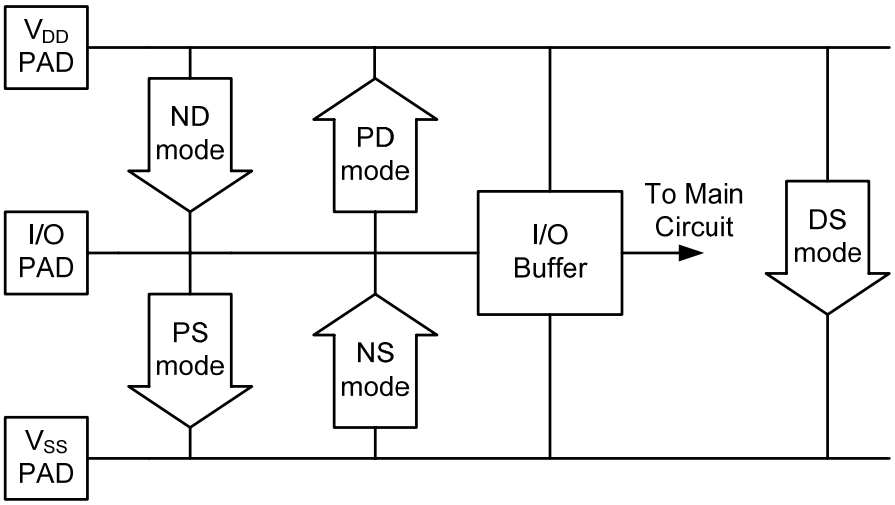


*Figure 1-6: Full chip ESD protection*

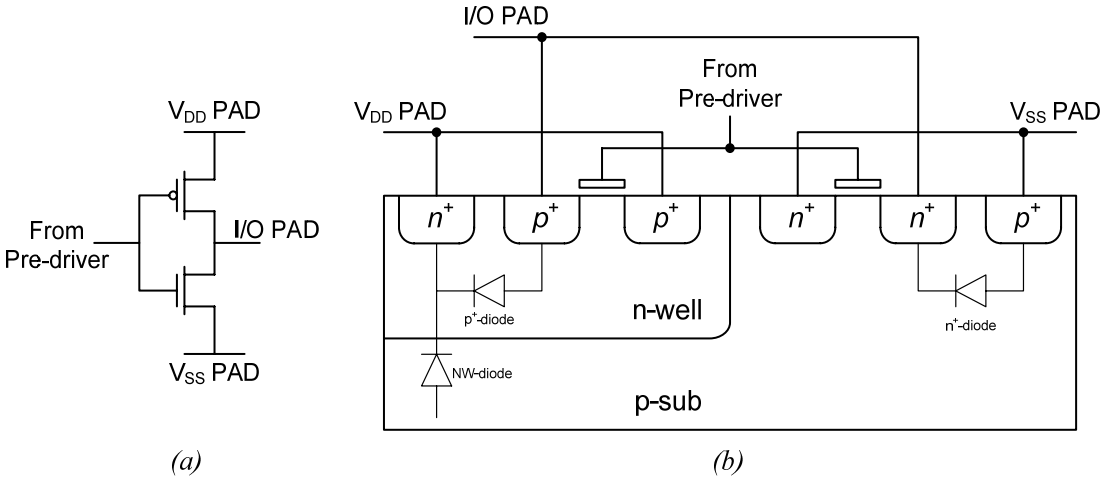


*Figure 1-7: A typical CMOS buffer stage (a) schematic (b) cross section*

When an ESD event occurs, the buffer is not powered and therefore, it can be modeled with three diodes as shown in Figure 1-7(b). Let's compare the behavior of this driver under different ESD zapping modes. In NS-mode, a negative ESD stress is applied to the I/O pad and is discharged through the $V_{SS}$ pad, while the $V_{DD}$ pad is floating. Hence, the discharge path is through the $n^+$-diode in forward biased condition. Diode in forward biased condition has a very low parasitic resistance and can carry large currents. Furthermore, the width of the transistors in a driver are usually very large and therefore this $n^+$-diode should be able to carry a large portion of the ESD current without any additional protection circuit. Unlike NS-mode, the current path for PS-mode stress, where

a positive stress is applied between pad and $V_{SS}$, is through the same diode in the reverse biased condition. In reverse biased condition the parasitic resistance of the diode is very large and hence, it cannot carry a large current. Therefore, additional protection circuit is required to avoid failure. Similar discussion applies for PD and ND mode stresses as well. In these modes, ESD stress is applied to the pad and is discharged towards $V_{DD}$ while $V_{SS}$ is floating. It can be seen that for positive stress (PD-mode) the discharge path is through the $p^+$-diode in forward biased condition. As a result, the driver can provide the required protection. On the other hand, for negative stress (ND-mode) the discharge path is through the same diode in reverse biased condition and hence, an additional protection circuit is required.

Based on the above discussion, it can be seen that the challenge in ESD protection circuit design is to provide immunity against PS- and ND-mode stresses. For simplicity, in the rest of this section we focus on PS-mode stress only. Similar discussions are applied to ND-mode stress.

The first method to provide protection against PS-mode stress is to add a protection circuit between pad and $V_{SS}$. This protection circuit should be able to carry a large current under ESD conditions, while having minimum impact on normal behavior of the circuit. As a result, ESD stress will be discharged through this circuit instead of the reverse-biased $n^+$-diode. Figure 1-8 shows the protection scheme for a PS-mode stress and highlights the discharge path.

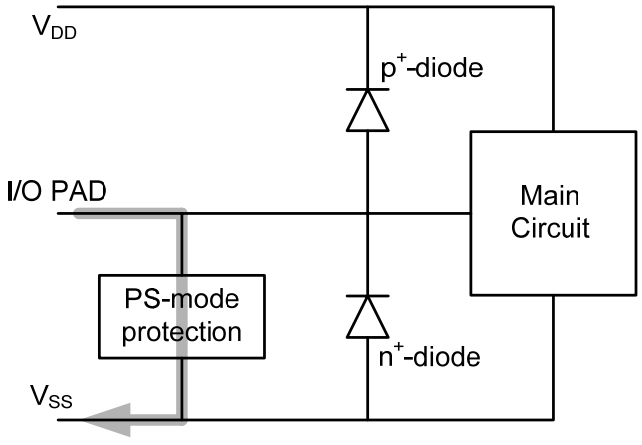


*Figure 1-8: Snapback-based ESD protection for PS-mode*

It can be seen that an additional block called PS-mode protection is added in parallel with the $n^+$-diode. In this method the protection circuit is designed using avalanching junctions. MOSFET and Silicon Controlled Rectifier (SCR) are the most popular devices that are used as the protection circuit. Under ESD conditions, these devices operate in their breakdown region. As it will be discussed in chapter 2, their breakdown has a snapback characteristic. Hence, this method is called snapback protection method. For ND-mode protection a similar circuit should be added between pad and $V_{DD}$ (in parallel with the $p^+$-diode) to discharge the ND-mode ESD stress.

In addition to snapback-based protection, PS-mode protection can be realized by transferring the ESD charge to the $V_{DD}$ node using the forward-biased $p^+$-diode. Then, this charge is discharged to $V_{SS}$ through another ESD protection circuit called ESD clamp. As the clamp is usually implemented without avalanching junctions, this method is called non-snapback protection scheme. Figure 1-9 shows non-snapback protection scheme and highlights the discharge path for PS-mode stress.

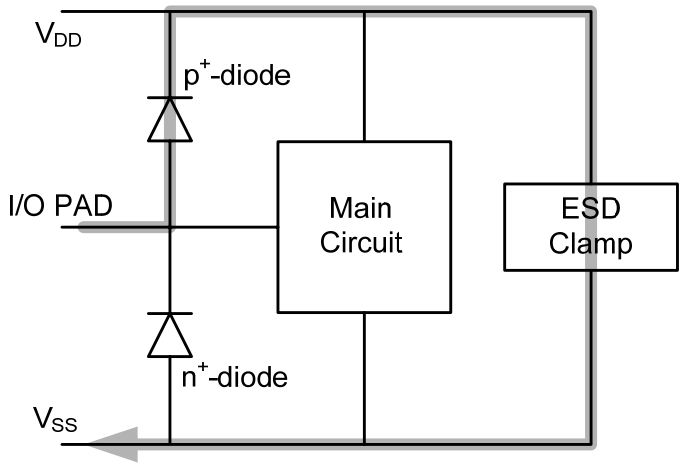


*Figure 1-9: Non-snapback-based ESD protection*

The clamp circuit should turn on when an ESD event occurs to discharge the ESD current. The most common clamp circuit uses a huge NMOS transistor that can carry the ESD current (a few amperes) without going into avalanche breakdown region. This transistor is triggered with an RC network that senses rapid increase in the voltage across $V_{DD}$ and $V_{SS}$. One of the main features of this clamp is that it can be simulated in circuit

level simulators as the transistors are not working in their breakdown region. The circuit in Figure 1-9 can be used for ND-mode stress as well. For this zapping mode the discharge path is through the forward-biased $n^+$-diode and the clamp. It can be seen that, in this method, unlike snapback-based method, one clamp circuit is placed between $V_{DD}$ and $V_{SS}$ lines which is shared among all other I/O pins.

The detail of the two snapback and non-snapback protection methods is discussed in the coming chapters.

## 1.6 Comparing Snapback and Non-snapback Protection Methods

In section 1-5 two main ESD protection schemes were discussed. There are advantages and disadvantages associated with each of them. In this section these two methods are compared [7].

The most important features of snapback based protection are as follows:

- By optimization it can be more robust
- It is generally immune to false triggering
- It can be used for fail safe applications

On the other hand,

- It is very process sensitive
- It may need extra process steps like salicide blocking and ESD implants
- It cannot be designed with minimum design rules (it needs ballast resistor)
- The simulations should be done by device level simulators (such as Medici) which are difficult and time consuming.

The most important features of non-snapback protection are as follows:

- It is more portable from fab to fab around the world
- It can be easily simulated using SPICE
- It can be designed with minimum design rules
- It doesn't need any extra process steps

On the other hand,

- It is susceptible to false triggering
- It is susceptible to oscillation
- It is difficult to be implemented for fail safe applications
- It may add power rail leakage.

## 1.7 Summary and Thesis Outline

In this chapter, electrostatic discharge, as a major reliability threat in modern semiconductor technologies, was introduced. General failure mechanisms were discussed with more emphasis in CMOS technology. Three main models for an ESD event were presented along with different zapping modes. Finally, ESD protection circuits were divided into two main categories and these two methods were compared in detail.

The rest of the thesis is organized as follows: Chapter 2 focuses on snapback-based ESD protection method where two novel techniques to reduce the first breakdown voltage and two methods to improve latch-up are introduced. Non-snapback-based ESD protection method is discussed in Chapter 3 and two novel clamps with better performance and stability are proposed. In Chapter 4 the interaction between a high-speed CML driver and different ESD protection strategies are explored. Finally, conclusions and future work are presented in Chapter 5.

# Chapter 2

# 2. Snapback-Based ESD Protection

As mentioned in the first chapter, snapback-based ESD protection is based on using semiconductor devices in their avalanche breakdown region. In this chapter a complete discussion on different aspects of this method along with a few novel improvement techniques are presented. In Section 2.1 different semiconductor devices are compared in high current regime and is concluded that SCR-based devices are an optimum solution in ESD protection applications. Section 2.2 provides an overview of the state of the art SCR-based ESD protection circuits. Finally, Section 2.3 discusses the new proposed ESD protection techniques.

## 2.1 Semiconductor Devices

As mentioned in the previous chapter, semiconductor devices that are used in the snapback-based protection scheme are operating in their breakdown region, where they can carry large currents. In this region the operation of devices is different from their

operation in nominal conditions. In an ESD event, failure of devices is caused by excessive heating which is due to high current and electric field. Therefore, J×E, where J is current density and E is the electric field, is considered as a measure to compare ESD robustness of semiconductor devices [1].

In CMOS technology, diode, MOSFET and Silicon Controlled Rectifier (SCR) are the most common devices in ESD protection applications. Although diode is not used as a snapback protection device, as mentioned in the previous chapter, it's still a part of the overall ESD protection scheme. Therefore, in the following subsections, the operation of these devices in high current mode is discussed and compared in detail.

### 2.1.1 Diode as an ESD protection device

The *pn* junction diode is the simplest semiconductor device. It can be used in either forward or reverse-biased mode. In forward-biased mode, the diode has a low turn on voltage and very low "on" resistance. As a result, it can carry very high currents without much thermal heating, which makes it a very good ESD protection device. On the other hand, in reverse biased mode, as the diode is operating in avalanche breakdown region, it has a high breakdown voltage and resistance. Therefore, it cannot carry high currents and has a poor ESD performance.

In a standard single well CMOS process with a p-type substrate, $p^+$-diode and $n^+$-diode are the most common diodes used as an ESD protection device. Figure 2-1 shows the cross section of these diodes. It should be noted that as an ESD protection device, these diodes should be biased in their forward-biased region.

The $n^+$-diode is formed between an $n^+$ junction and the p-substrate as shown in Figure 2-1(a). As substrate should be connected to ground/$V_{SS}$ in CMOS technology, as an ESD protection device, this diode should be used only between pad and ground/$V_{SS}$. Figure 2-1(b) shows the $p^+$-diode which is formed between a $p^+$ and an n-well region. Again, as n-well region should be connected to $V_{DD}$, cathode of this diode should be connected to $V_{DD}$ as well. Hence, as an ESD protection device, this diode should be used between pad and $V_{DD}$.

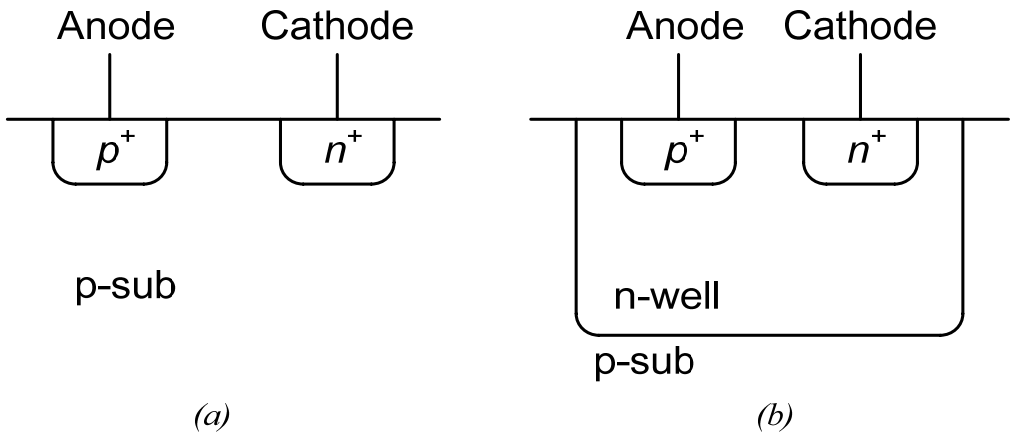


*Figure 2-1: Diode in CMOS technology (a) $n^+$-diode (b) $p^+$-diode*

### 2.1.2 MOSFET as an ESD protection device

As an ESD protection device, the simplest form of an NMOS is the grounded gate configuration (GGNMOS), where the gate and the source of the transistor are connected to ground. Figure 2-2 shows the cross section and I-V characteristic of this device. The behavior of this device under high current conditions can be explained using its parasitic bipolar transistor which is shown in Figure 2-2(a).

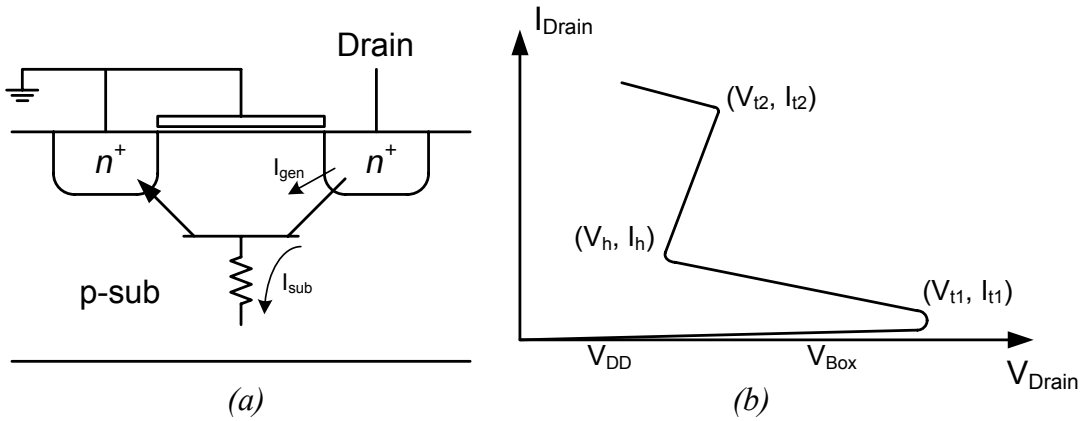


*Figure 2-2: Grounded gate NMOS (a) cross section (b) I-V characteristic*

In order to give an idea of the value of supply and oxide breakdown voltages, they are specifically shown in Figure 2-2(b). The I-V characteristic of the GGNMOS can be explained as follows: As the drain voltage increases, the drain-substrate junction becomes

more reverse-biased until it goes into avalanche breakdown. At this point, the drain current increases and the generated holes drift towards the substrate contact ($I_{sub}$). Therefore, the base voltage of the parasitic bipolar transistor increases, making the base-emitter junction of the parasitic bipolar transistor more forward biased. As the base-emitter voltage reaches ≈0.7V, the parasitic bipolar transistor turns on. The drain voltage at this point is $V_{t1}$ which is called the first breakdown voltage. This bipolar action generates more current, and therefore, there is no need to keep the drain voltage at $V_{t1}$ to maintain the drain current. Hence, the drain voltage reduces to the holding voltage ($V_h$), and snapback behavior is observed. After the bipolar transistor turns on, increase in the drain voltage increases the current further, until thermal damage occurs. This point is called the second breakdown point and the voltage and current at this point are $V_{t2}$ and $I_{t2}$, respectively.

As an ESD protection device, the drain of the GGNMOS is connected to the I/O pad. Therefore, under normal operating conditions, the NMOS transistor is "off" and the current of the ESD protection device is very small. Under ESD conditions and when the pad voltage exceeds $V_{t1}$, the transistor goes into snapback mode and ESD current is discharged through GGNMOS. The maximum ESD current that can be discharged through this transistor is determined by the value of the second breakdown current. This value is usually in the order of 3-10mA/μm. The width of the GGNMOS can be calculated based on the required ESD protection level. For example, to achieve a 2kV HBM protection and considering $I_{t2}$=4mA/μm, the width of the transistor can be calculated from the following equations:

$$V_{HBM} = \left(R_{ON(ESD)} + R_{HBM}\right) I_{t2} \tag{2-1}$$

$$R_{ON(ESD)} << R_{HBM} = 1.5k\Omega \Rightarrow W = 333\mu m \tag{2-2}$$

As it can be seen from the above example, the required width of a GGNMOS is typically a few hundred microns. Therefore, GGNMOS is usually realized in a multi-finger configuration.

In the DC characteristic of the GGNMOS shown in Figure 2-2(b), $V_{t1}$, $V_h$, $V_{t2}$, and $I_{t2}$ are the most important parameters. In order to design an ESD protection circuit, the following requirements must be met:

1. $V_{t1}$ must be less than the gate oxide breakdown voltage to protect the gate during an ESD event. This condition assures that the GGNMOS turns on before the gate oxide breaks down.
2. $V_{t2}$ must be greater than $V_{t1}$ to ensure uniform triggering. Therefore, even if one finger triggers first, the voltage build-up can turn on other fingers before the first finger reaches the second breakdown point. Otherwise, the effective width of the device is decreased and the performance of the GGNMOS is degraded.
3. $I_{t2}$ determines the robustness of the ESD protection device and should be as high as possible.
4. $V_h$ should be greater than $V_{DD}$. Otherwise, GGNMOS may turn on during normal operating conditions, which is called latch-up. Typically, $V_h$ is considered to be 10%-20% more than $V_{DD}$.

However, it is impractical to implement a GGNMOS in deep submicron CMOS technology that meets all the above requirements [4]. Hence, some new techniques have been developed to modify the GGNMOS structure in order to meet all requirements. Some of these techniques are discussed in Section 2.2.

In advanced CMOS technologies, a number of new process steps have been added to the standard CMOS technology to improve the performance of transistors. At the same time, some of these process steps have negative impact on ESD protection devices. Silicidation is the most critical process step that affects ESD protection devices. Silicidation is the addition of a Tungsten or Cobalt interface to the semiconductor material [8]. It is usually applied to the polysilicon gate and diffusions. The silicided poly and diffusions have a sheet resistance of at least one order of magnitude lower than non-silicided ones; hence, the speed of transistors improves. On the other hand, as an ESD protection device, the resistance between gate and drain contacts, which is called the ballast resistance, forces a more uniform current flow through all the fingers of the NMOS transistor. As a result, all fingers of the transistor will trigger uniformly. In non-silicided technologies, this resistance is created by the spacing between gate and drain contacts. In silicided technologies, due to the silidation of the diffusion regions, the resistance created by this spacing is very small and cannot ensure uniform triggering. There are a number of solutions for this problem.

1. Silicide blocking: This is the most popular solution to restore the ballast resistor. In this method, another process step is added to the standard CMOS process in order to prevent silicidation of source and drain diffusions of the ESD protection MOS transistor [8]. This process step patterns the wafer with a blocking layer (typically nitride) and involves three extra steps of deposition of nitride, photo mask and etching. The most important disadvantage of this method is the increase in fabrication cost due to extra process steps.
2. N-well resistor: In this method a ballast resistor is added externally. Figure 2-3 shows the layout of an NMOS using a ballast n-well resistor [9].
3. Back-end ballasting: This method uses the high resistivity of contacts, vias and interconnects in advanced CMOS technologies to build the ballast resistor. Hence, a chain of metal-interconnect layers is used in this method [8]

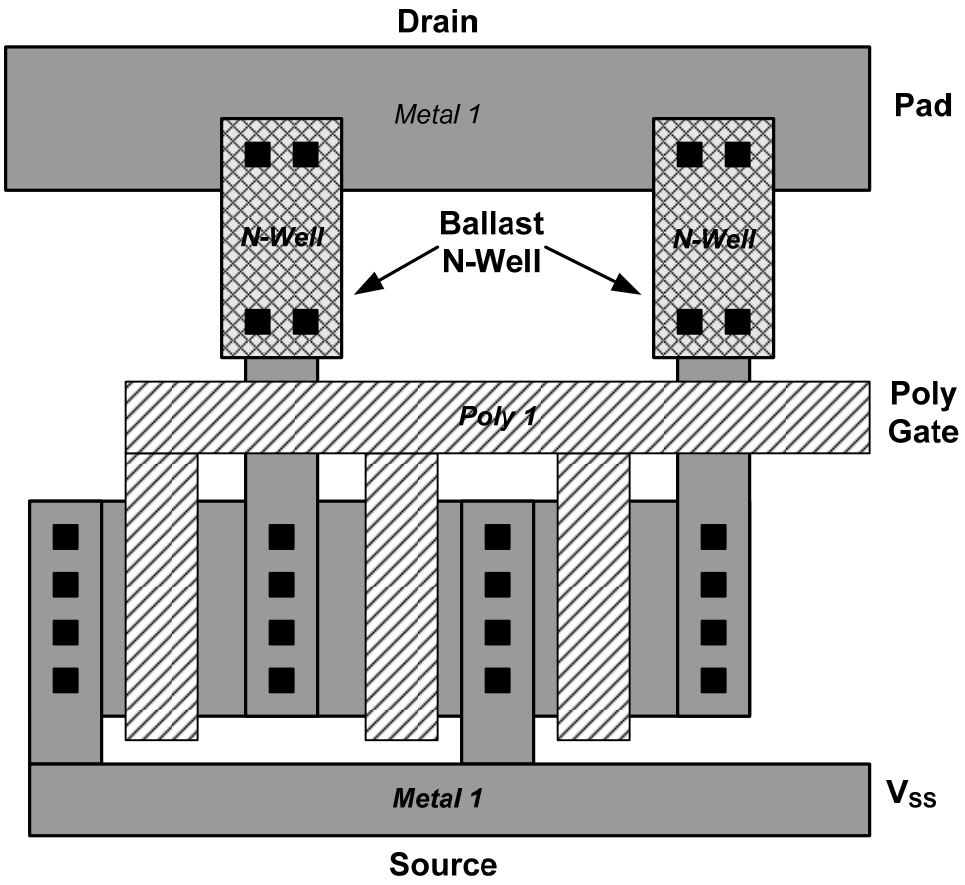


*Figure 2-3: Use of an n-well resistor to restore the ballast resistor*

### 2.1.3 Silicon Controlled Rectifier (SCR) as an ESD protection device

Silicon Controlled Rectifier (SCR) is another active device that is often used as a protection element. Figure 2-4(a) shows the cross section of an SCR in standard CMOS technology which consists of a *pnpn* structure. The $p^+$ diffusion in the n-well forms the anode and the $n^+$ diffusion in the p-sub forms the cathode of the SCR. As an ESD protection device, the n-well contact is connected to the anode, and the p-sub contact is connected to the cathode. The anode is connected to the I/O pad, and the cathode is connected to the ground. An SCR is often represented with its parasitic bipolar transistors as shown in Figure 2-4(b).

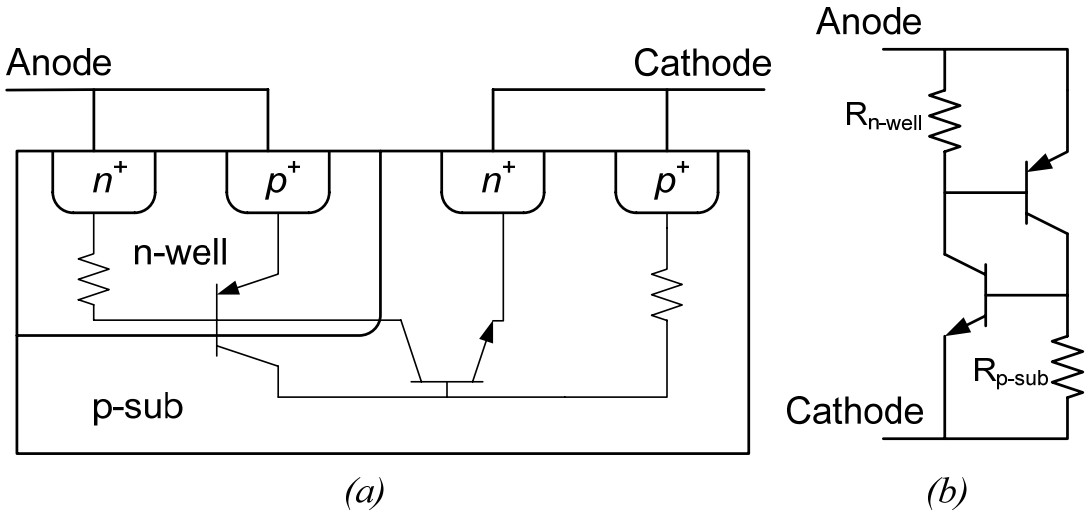


*Figure 2-4: Silicon controlled rectifier (a) cross section (b) equivalent schematic*

As the anode voltage increases, the well-substrate junction becomes more reverse biased until it goes into avalanche breakdown. The generated current can turn on either of the two parasitic bipolar transistors. Typically, the gain of the *npn* transistor is an order of magnitude higher than that of the *pnp* transistor. Therefore, the *npn* transistor turns on more easily than the *pnp* transistor [4]. When the *npn* transistor turns on, its current generates a voltage drop across $R_{n\text{-well}}$ and turns on the *pnp* transistor. The current of the *pnp* transistor, in turn, creates a voltage drop across $R_{p\text{-sub}}$ and helps to keep the *npn* transistor on. At this point, due to the current of the *pnp* transistor, there is no need for the

anode to provide the bias of the *npn* transistor. Hence, the anode voltage is reduced to $V_h$. It can be seen that the I-V characteristic of the SCR is similar to that of the GGNMOS.

It should be noted that the triggering of SCR is initiated by avalanche breakdown of the well-substrate junction, while GGNMOS is triggered by avalanche breakdown of the $n^+$-substrate junction. Hence, the first breakdown voltage for these two devices is different. In order to compare $V_{t1}$ between GGNMOS and SCR, consider the avalanche breakdown equation for a p-n junction [10]:

$$BV = \frac{\varepsilon(N_A + N_D)}{2qN_AN_D}E_{crit}^2 = 3.25\times10^6\frac{N_A + N_D}{N_AN_D}E_{crit}^2 \quad (2\text{-}3)$$

In CMOS technology, substrate and well dopings are in the order of $10^{16}$-$10^{17}$ $cm^{-3}$, while $p^+$ and $n^+$ doping are in the order of $10^{20}$ $cm^{-3}$. Therefore, in GGNMOS, $N_D$ (drain doping) is much higher than $N_A$ (substrate doping). On the other hand, in SCR, $N_D$ (well doping) is in the same order as $N_A$ (substrate doping). As a result, the first breakdown voltage of GGNMOS is less than SCR. Typically, in advanced technologies, the breakdown voltage of GGNMOS is between 5V and 10V while the breakdown voltage of SCR is between 20V and 25V.

Due to the very high breakdown voltage of SCR, this device is usually used in a modified configuration, which is called Low Voltage Triggered SCR (LVTSCR) [11], [12]. In LVTSCR, an $n^+$ region is inserted in the boundary of the well-substrate junction. As a result, breakdown of the device is initiated by the avalanche breakdown voltage of the $n^+$-substrate junction. Furthermore, a gate contact is added to further reduce the breakdown voltage of the device. Figure 2-5 shows the cross section of the LVTSCR.

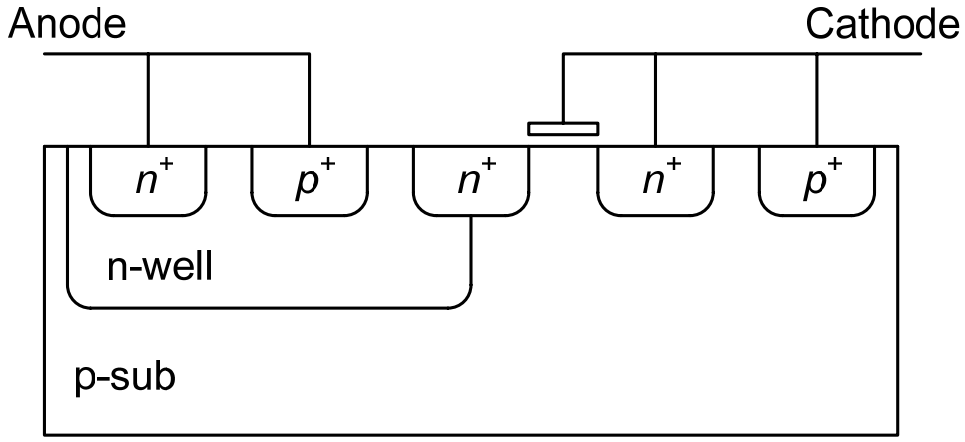


*Figure 2-5: Cross section of the LVTSCR*

The first breakdown voltage of the LVTSCR is equal to the breakdown voltage of its internal NMOS structure. Although in this device the first breakdown voltage is reduced significantly, this device is still not able to meet all the requirements for an ESD protection circuit. In the following sections this device is discussed in more detail.

### 2.1.4 Comparing diode, GGNMOS and SCR

In order to compare different protection devices, the DC characteristics of a typical diode, GGNMOS and SCR are shown in Figure 2-6 [1].

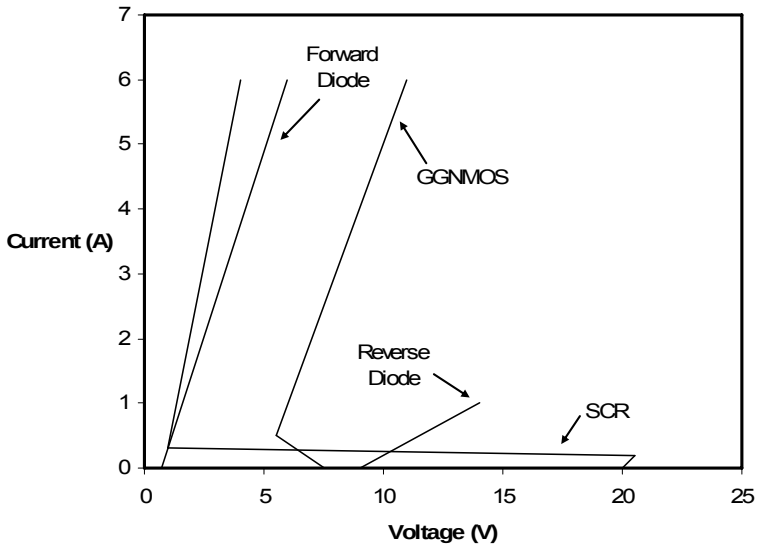


*Figure 2-6: Comparing the diode, SCR and GGNMOS*

As an ESD protection device, failure mechanism of these devices is thermal run away. Internal temperature of a semiconductor device is proportional to the power dissipation inside the device or current and voltage across the device. Hence, the most robust ESD protection device has the lowest area between the curve and y-axis. It can be seen that SCR and diode in forward biased region are the best among other devices shown in Figure 2-6. The first breakdown voltage of these devices can be compared in Figure 2-6 as well. It can be seen that SCR and reverse biased diode have very high first breakdown voltages. Although GGNMOS has low breakdown voltage, this voltage is not

low enough to provide enough protection in advanced technologies. Finally forward biased diode has the lowest breakdown voltage, which is too low for some applications. Comparing the holding voltage of SCR and GGNMOS shows that SCR needs some modifications to increase its holding voltage and avoid latch-up.

Based on the above discussion, it can be concluded that none of these devices meets all requirements as an ESD protection device. However, SCR has the best protection level per unit area which motivates us to modify it based on ESD protection needs. In the following sections SCR family devices are discussed in detail to design an optimum ESD protection circuit.

## 2.2 Triggering mechanisms

As mentioned in the previous section, MOSFET or SCR cannot provide the required ESD protection due to their high first breakdown voltage. Therefore, these devices have been modified to reduce their first breakdown voltage. As MOSFET was the first device to be used in ESD protection applications, these modifications were introduced for an NMOS transistor. However, they can be applied to SCR as well. Gate coupling and substrate triggering are the most popular techniques that are applied to both MOS and SCR devices.

### 2.2.1 Gate coupling technique

Polgreen and Chatterjee showed that applying a small voltage to the gate lowers the first breakdown voltage of an NMOS transistor [13]. This is due to the current generated in the channel, which is a result of the MOS operation. This current helps to forward bias the source-substrate junction and trigger the parasitic bipolar transistor. Therefore, the first breakdown voltage is reduced. The effect of the gate voltage on the first breakdown voltage of an NMOS transistor is shown in Figure 2-7.

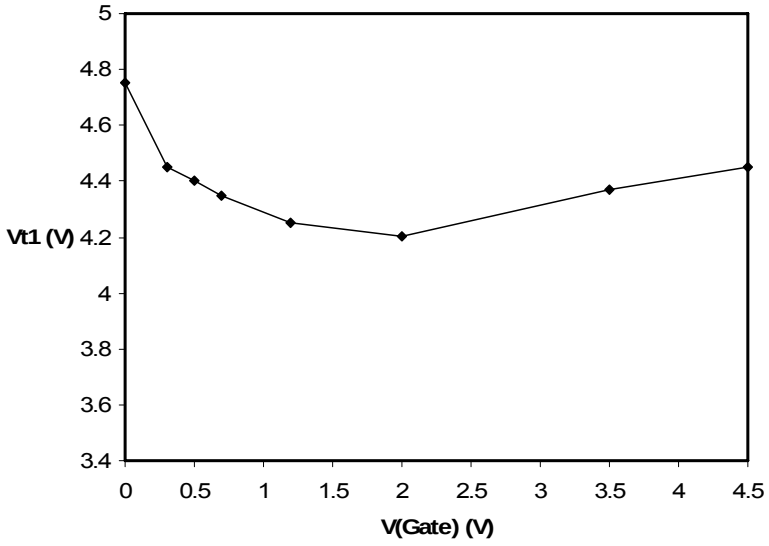


*Figure 2-7: Impact of the gate voltage on the first breakdown voltage of an NMOS transistor*

It can be seen that by increasing the gate voltage $V_{t1}$ decreases. However, for higher gate voltages $V_{t1}$ starts to increase. This is due to decreased impact ionization rate. In other words, the pinch-off region in the MOS channel disappears and impact ionization becomes limited by carrier scattering in the inversion region. Therefore, there is an optimum gate voltage that gives the minimum first breakdown voltage. As an ESD protection device, the first breakdown voltage should be smaller than the oxide breakdown voltage to prevent failure under ESD conditions. Moreover, it should be smaller than the second breakdown voltage to ensure uniform triggering of all fingers.

As the ESD event might happen when the IC is not powered, the gate bias should be provided by the pad voltage through a coupling circuit. Figure 2-8 shows an NMOS with gate coupling, which is called Gate-Coupled NMOS (GCNMOS) [14], [15].

The $R_C$-$C_C$ network is used to couple a fraction of the ESD charge to the gate of the NMOS transistor. As the gate voltage is increased, the first breakdown voltage is decreased. Choosing proper values for $R_C$ and $C_C$ makes the first breakdown voltage lower than the second breakdown voltage and therefore, uniform triggering is achieved. Another important point in designing $R_C$ and $C_C$ is that this protection circuit should be activated in ESD stress conditions only. Therefore, $R_C$ and $C_C$ should be chosen in such a

way that when the pad voltage is increased from 0 to $V_{DD}$, the gate voltage stays below the threshold voltage of the NMOS transistor.

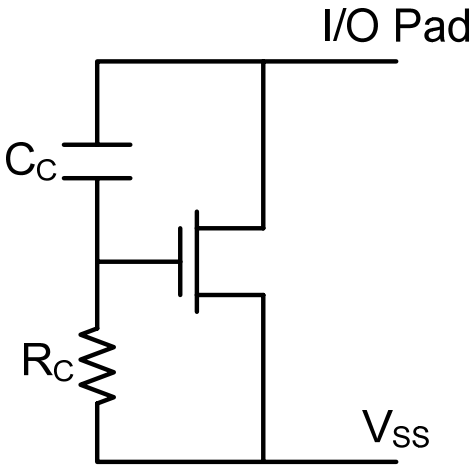


*Figure 2-8: Gate-coupled NMOS*

Although it seems that the gate coupling technique is an effective solution for both uniform triggering and reducing the first breakdown voltage, it has one major limitation [16], [17]. The coupled gate voltage turns on the strong-inversion channel of the NMOS transistor and the ESD current is discharged through this region. Moreover, deep submicron technologies use shallow junction depths, which make MOSFETs more susceptible to ESD damage. Therefore, gate coupling becomes less effective. This effect is shown in Figure 2-9 [16].

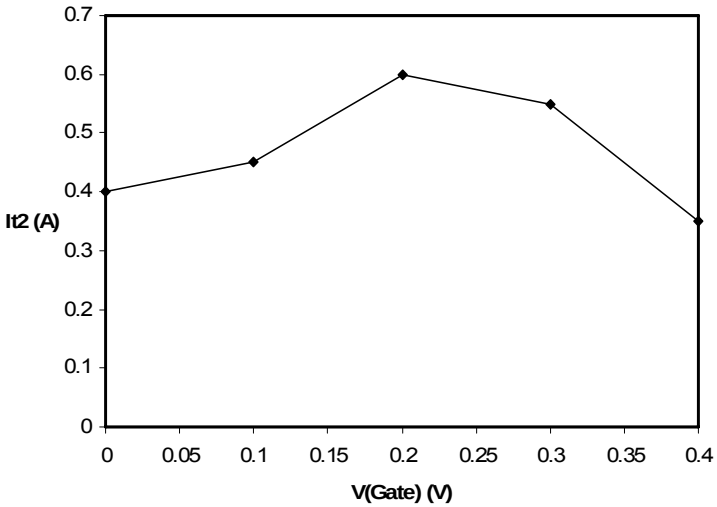


*Figure 2-9: Impact of the gate voltage on the second breakdown current of an NMOS*

It can be seen that, up to a critical point, gate coupling increases $I_{t2}$. But after that point, $I_{t2}$ drops suddenly. Therefore, the effectiveness of gate coupling is limited.

This technique is used to reduce the triggering voltage of SCR devices as well. Gate coupling with RC network is applied to LVTSCR and similar results are reported [18], [19].

### 2.2.2 Substrate triggering technique

Polgreen and Chatterjee discussed the effect of substrate voltage on $V_{t1}$ of a MOS transistor as well [13]. They showed that applying a positive voltage to the substrate lowers the first breakdown voltage and hence, allows uniform triggering of all fingers. This is due to the increased base voltage of the parasitic bipolar transistor. Therefore less built in voltage is needed to turn on the parasitic bipolar transistor. The dependence of the first breakdown voltage on the substrate bias is shown in Figure 2-10.

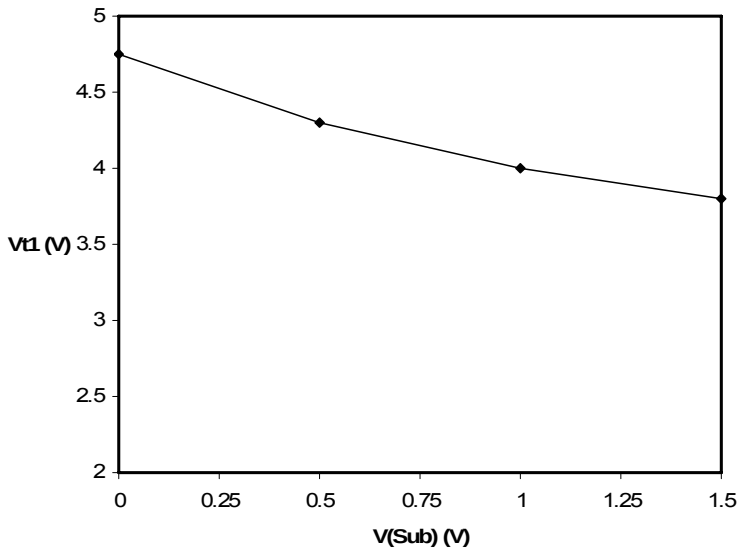


*Figure 2-10: Impact of the substrate voltage on the first breakdown voltage of an NMOS*

Similar to the gate coupling technique, in this method the substrate voltage should be provided through the pad to be effective when the circuit is not powered. The most common method uses another NMOS transistor as a pump to inject current into the

substrate of the main NMOS transistor. Figure 2-11 shows the schematic of the substrate triggered NMOS where $M_0$ is the main protection transistor and $M_S$ provides the substrate triggering [20].

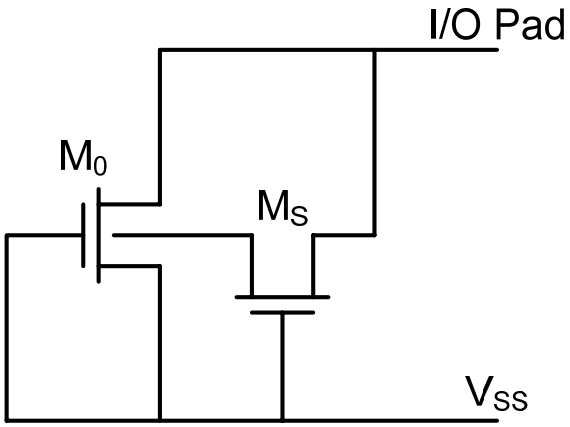


*Figure 2-11: Substrate-triggered NMOS*

It can be seen that using substrate triggering, the additional charge is going through the substrate instead of the channel. Hence, unlike the gate coupling technique, this technique doesn't degrade the second breakdown current and ESD performance. As a result, this method is usually preferred to the gate coupling technique. Figure 2-12 shows the impact of the pumped substrate current on the second breakdown current of an NMOS transistor [16].

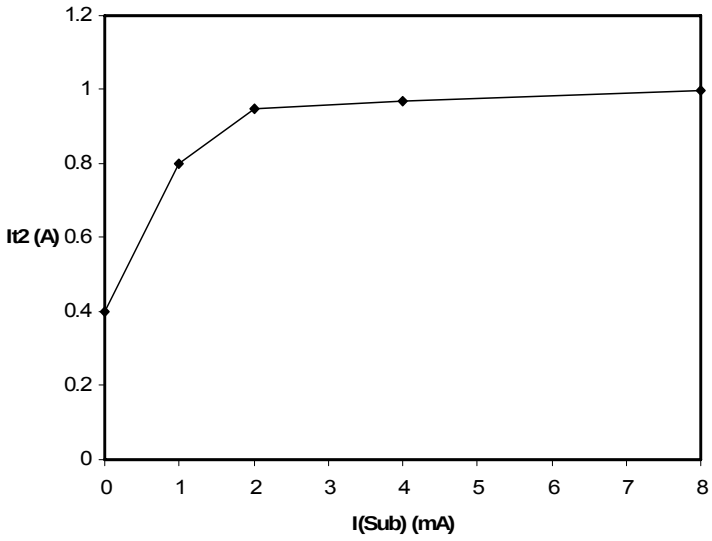


*Figure 2-12: Impact of the substrate current on the second breakdown current of an NMOS*

It can be seen that, as expected, the second breakdown current is improved by applying the substrate triggering technique.

Similar to gate coupling, this technique is applied to LVTSCR as well and similar results are reported [21].

## 2.3 State of the Art SCR-Based Devices

### 2.3.1 Reducing the first breakdown voltage

Although substrate triggering and gate coupling reduce the first breakdown voltage of both SCR and MOSFET devices, they are not capable of providing low enough breakdown voltage for deep submicron technologies. Therefore, in more advanced methods, a combination of different triggering mechanisms is used to meet the ESD protection requirements. In this section, a few of the state of the art triggering methods for SCR-based devices are presented.

As substrate triggering is a more effective way to reduce the first breakdown voltage, the double-triggered SCR was introduced by adding another triggering to the well of the SCR [22], [23]. In this device, an additional current is pumped into both well and substrate during an ESD event. Referring back to the parasitic bipolar transistors of the SCR (Figure 2-4), the additional current in the well helps to turn on the *pnp* transistor, while the current in the substrate helps to turn on the *npn* transistor. Figure 2-13(a) shows the cross section of this device. The triggering for well and substrate is provided using the circuit shown in Figure 2-13(b).

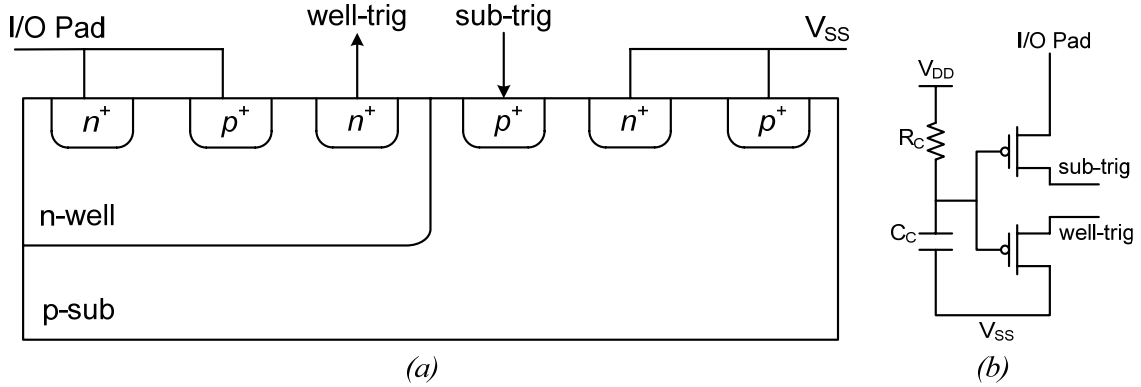


*Figure 2-13: Double triggered SCR (a) cross section (b) triggering mechanism*

In this device, an $n^+$ region is added inside the n-well region to provide the triggering in the well and a $p^+$ region is added inside the p-sub region to provide the triggering in the substrate. The triggering circuit is based on a MOS transistor that injects the current into the well/substrate. As the reduction in the first breakdown voltage is a function of the amount of the injected current, an RC circuit is used to set the first breakdown voltage. It has been reported that using this method, the first breakdown voltage can be designed as low as 2V [22]. One of the features of this design is the ability to achieve a low first breakdown voltage using SCR instead of LVTSCR that has an extra gate contact. As a result, the parasitic capacitance of this structure is the parasitic capacitance of the SCR and the triggering circuit, while in LVTSCR based structures, the parasitic capacitance is the parasitic capacitance of the SCR, gate, and the triggering circuit.

In order to further reduce the parasitic capacitance of the SCR-based protection circuits, a polysilicon SCR device has been introduced, where the *pnpn* structure is implemented in the polysilicon region instead of silicon [24]. Furthermore, as this device is isolated from the substrate, it offers better noise coupling immunity. Figure 2-14 shows the cross section of the polysilicon SCR.

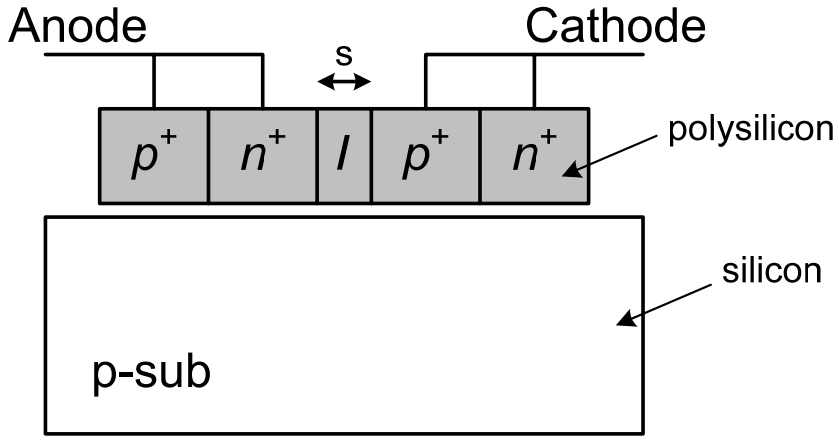


*Figure 2-14: Cross section of the polysilicon SCR*

In this structure, $p^+$ and $n^+$ regions in polysilicon are doped along with the $p^+$ and $n^+$ diffusions of MOS transistors and hence, no other process steps are required. On the other hand, as the polysilicon region is silicided in advanced technologies, silicide block option is required to avoid shorting the regions together. It can be seen that an undoped region called 'I' exists between anode and cathode of this SCR. The length of this region, which

is called ‘s’, determines the first breakdown voltage of this device. It has been shown that in 0.35μm technology, by changing ‘s’ from 0 to 2.4μm, the first breakdown voltage is changed from 9V to 15V. Although this device has a relatively high first breakdown voltage, it has a very low parasitic capacitance of only 92.3fF at 2.4GHz, which makes it a promising choice in high speed applications.

In addition to ESD protection circuits for the standard CMOS process discussed so far, there are a number of techniques to reduce the first breakdown voltage based on the triple-well CMOS technology as well. Applying substrate triggering with a native NMOS in a triple-well technology is the most effective solution [25]. In a triple-well technology a native NMOS transistor is a transistor built in a low-doped substrate instead of p-well. Figure 2-15 shows the cross section of this device. It should be noted that as this device is based on SCR instead of LVTSCR, it has lower parasitic capacitance. The gate of the native NMOS should be connected to a negative bias to turn off the device under normal operating conditions. In 0.13μm CMOS process, this device can reduce the triggering voltage to 2.5V.

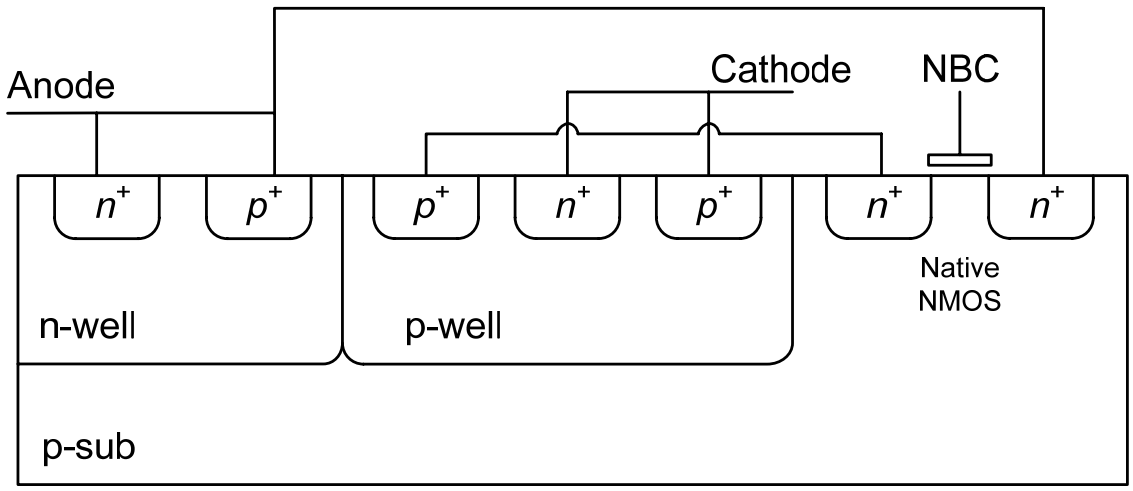


*Figure 2-15: Cross section of the native NMOS triggered SCR*

### 2.3.2 Improving latch-up immunity

As mentioned earlier, SCR devices are susceptible to trigger during normal operating conditions and cause latch-up. The latch-up problem is mainly due to the low holding

voltage of the SCR. As the holding voltage of the SCR is lower than $V_{DD}$, a small current in the substrate during normal operating conditions may increase the SCR current beyond the holding current and trigger the SCR. The easiest solution for this problem is to increase the holding voltage above $V_{DD}$. One of the first solutions to increase the holding voltage in standard CMOS technology is to cascode SCR devices [26]. The overall holding voltage is the sum of the holding voltage of individual SCRs. As a result, the overall holding voltage can be tuned by changing the number of SCR devices. Although this method increases the holding voltage, it increases the first breakdown voltage as well. Therefore, another triggering technique should be applied to SCRs to reduce the overall triggering voltage below the oxide breakdown voltage. Furthermore, this method increases the turn on resistance of the overall circuit as well and hence, wider SCRs are needed to maintain the original ESD protection level. This method can be modified by cascoding one SCR with a stack of diodes [27]. This method reduces the increase in the first breakdown voltage of the overall protection circuit. Figure 2-16 shows this technique were an SCR based device is cascoded with a stack on 'n' diodes.

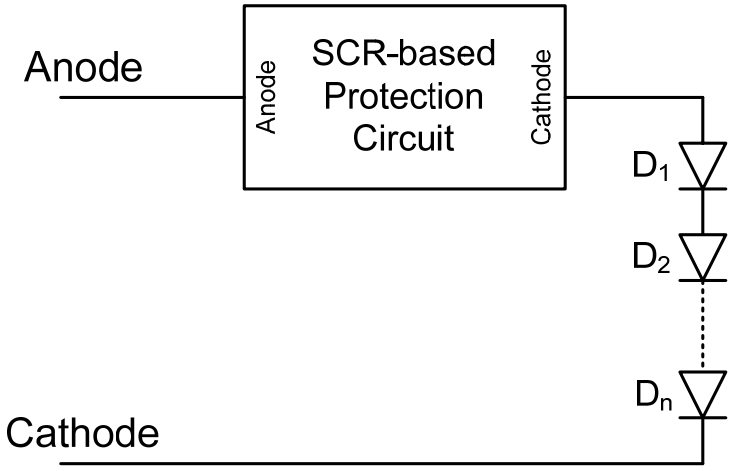


*Figure 2-16: Increasing $V_h$ by cascoding SCR with a stack of diodes*

Similar to stack of SCRs, this circuit still suffers from high triggering voltage and on resistance. Hence, some new techniques have been proposed to overcome these limitations. One of the most popular solutions is the SCR with dynamic holding voltage [28]. In this method a dynamic resistor is placed in parallel with the $R_{p\text{-}sub}$ resistor in the SCR equivalent circuit (refer to Figure 2-4(b)). Figure 2-17(a) shows the schematic of this device.

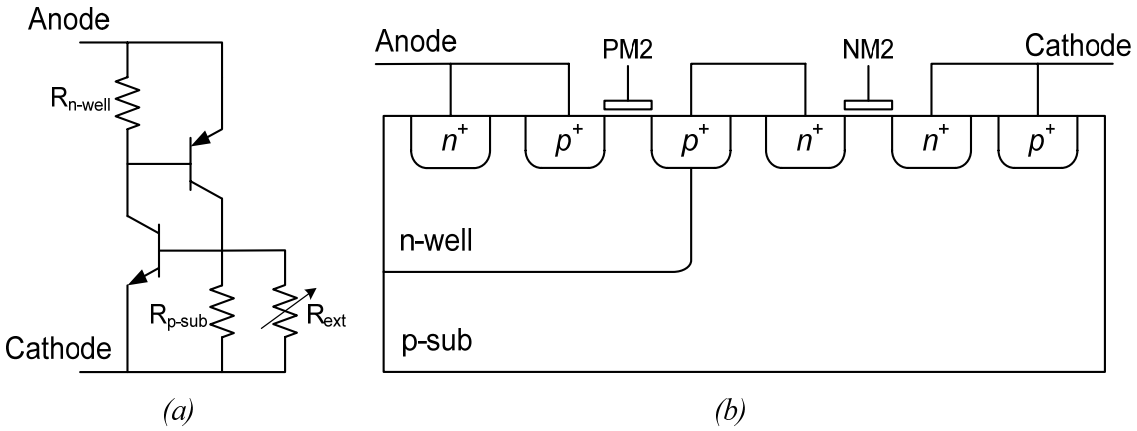


*Figure 2-17: SCR with dynamic holding voltage (a) schematic (b) cross section*

Under normal operating conditions $R_{ext}$ is lower than $R_{p\text{-}sub}$ and reduces the holding voltage while under ESD conditions $R_{ext}$ is higher than $R_{p\text{-}sub}$ and the holding voltage doesn't change significantly. As a result, under normal operating conditions the holding voltage is high and prevents latch-up, while under ESD conditions the holding voltage is low and increases the ESD robustness. Figure 2-17(b) shows the cross section of this device where a PMOS and an NMOS are inserted in the SCR device to create two external resistors in parallel with $R_{n\text{-}well}$ and $R_{p\text{-}sub}$. Under ESD conditions, the gate of these transistors is connected to ground and the holding voltage is 2V. On the other hand, under normal operating conditions the gate of these transistors is connected to $V_{DD}$=2.5V and the holding voltage is increased to 3V to avoid latch-up.

In addition to increasing the holding voltage, latch-up can be prevented by increasing the first breakdown current or holding current as well. Higher first breakdown/holding current reduces the chance for a noise in the substrate to turn on the SCR and cause latch-up. Hence, setting the first breakdown/holding current high enough ensures latch-up immunity even with a holding voltage less than $V_{DD}$. High holding current SCR (HHI-SCR) is one of the solutions reported to increase the holding current [29]. In this device, reduction in the first breakdown voltage of SCR is achieved by connecting an external GGNMOS element to the SCR [30]. In order to increase the holding current, an external poly resistor is added between GGNMOS and $V_{SS}$. Figure 2-18 shows the schematic of the HHI-SCR. Using this method, the holding current of 68mA is reported in 0.1μm CMOS technology.

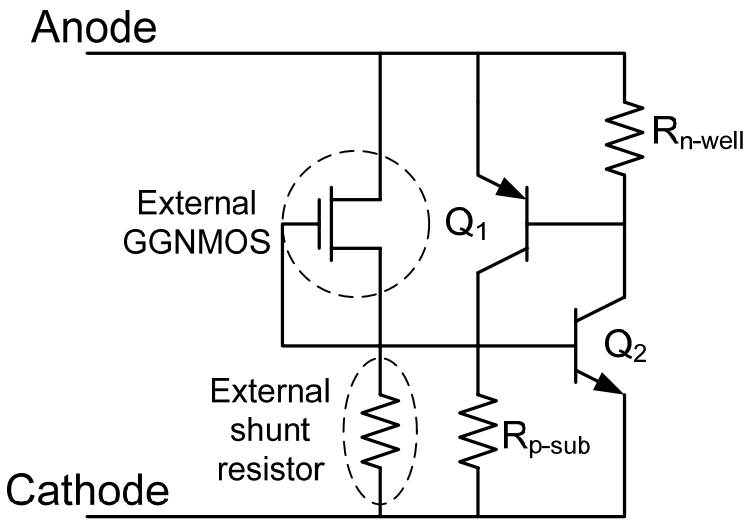


*Figure 2-18: Schematic of the high holding current SCR (HHISCR)*

In addition to increasing the holding current, a high triggering current SCR has been reported as well where a diode is added to increase the first breakdown current [31].

## 2.4 The Proposed Solutions

As SCR has the highest ESD protection level per unit area, this family of devices is used to design an optimum snapback-based ESD protection circuit. The new designs are based on reducing the first breakdown voltage and improving latch-up immunity in SCR devices.

### 2.4.1 Gate-substrate triggered LVTSCR

As mentioned, one of the first modifications done on GGNMOS and LVTSCR was the gate-coupling technique that reduces the first breakdown voltage. At the same time, this technique adds a relatively large capacitance to the pad. In this research a new method to reduce the parasitic capacitance of the gate-coupling technique is presented. In this method, the required gate voltage is provided by a coupling NMOS transistor. This technique is shown in Figure 2-19.

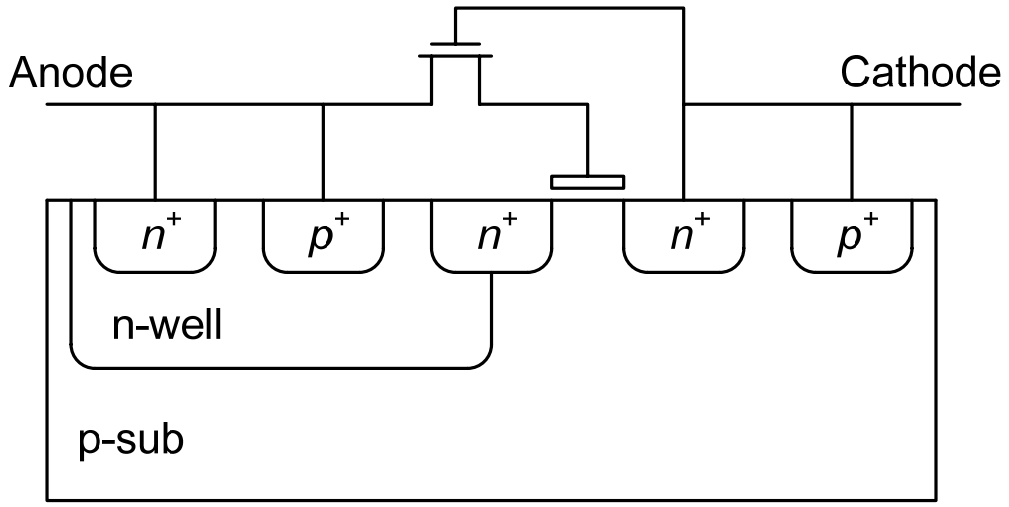


*Figure 2-19: The new gate-coupled LVTSCR*

The simulation results show that with a 5μm NMOS transistor, the reduction in the first breakdown voltage is comparable to the conventional gate-coupled LVTSCR with $R_C$=9.4kΩ and $C_C$=200fF. Hence, this method reduces the parasitic capacitance by almost 20 times. To further reduce the first breakdown voltage, this gate-coupling method is combined with the substrate triggering technique. Figure 2-20 shows a cross section of the proposed gate-substrate-triggered LVTSCR (GST-LVTSCR).

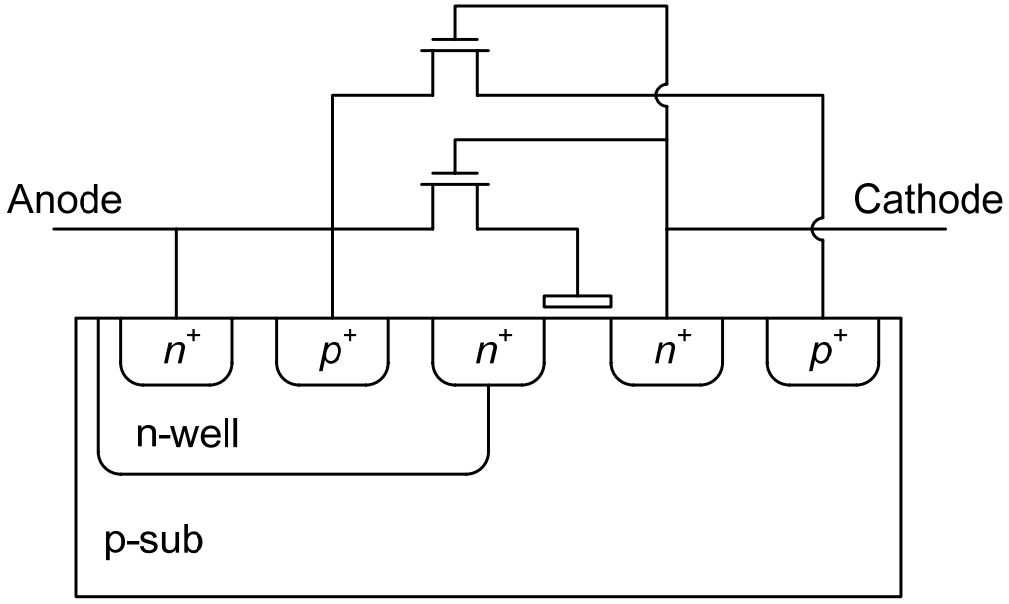


*Figure 2-20: The gate-substrate triggered LVTSCR (GST-LVTSCR)*

In order to simulate these structures, two different device level simulators were used: Medici from Synopsys and Sequoia from Sequoia Design Systems. The first step in device-level simulation is to create 2-D mesh models of the fabricated devices. GST-LVTSCR is simulated in 0.18μm CMOS technology. Hence, the device cross section in Medici is based on the process parameters of this technology. The values of the oxide thickness, well and diffusion junction depths, and the substrate doping can be found from the technical documents. However, most of the process parameters are not available and should be estimated. The estimation is done by simulating an NMOS transistor to obtain the typical values for the main transistor parameters such as threshold voltage, saturation current and current gain.

Figure 2-21 shows the cross section of the LVTSCR device used in the simulations. In this device, different regions are designed with uniform doping. The substrate doping is $1\times10^{16}$, the well doping is $9\times10^{16}$, and dopings of $n^+$ and $p^+$ diffusion regions are $2\times10^{20}$.

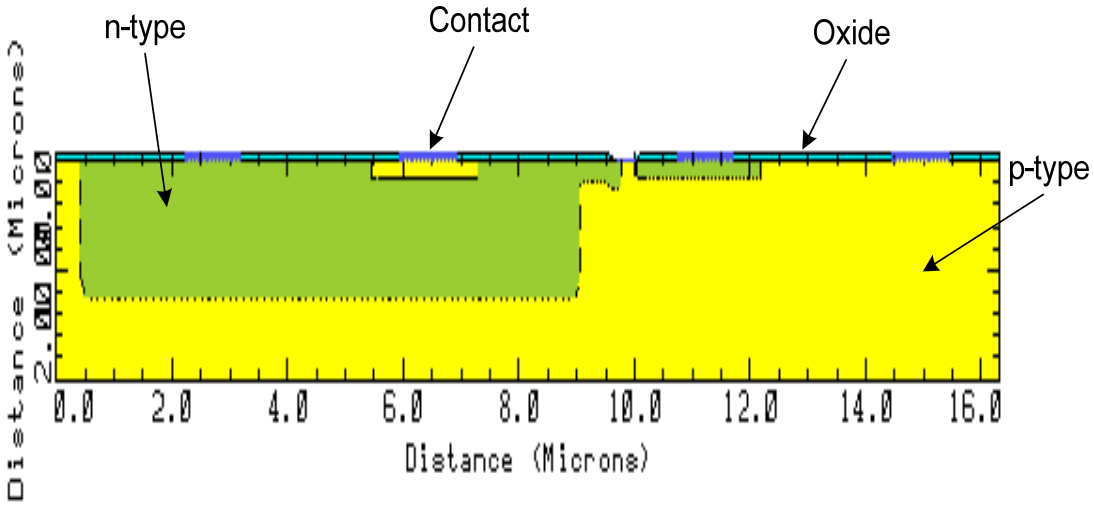


*Figure 2-21: Cross section of the LVTSCR created in Medici*

The I-V characteristic of different ESD structures is derived through quasi-DC simulation. In the quasi-DC simulation, the pad voltage is ramped with a very high rise time (a few seconds) and the current of the device is simulated. Figure 2-22 compares the I-V characteristic of LVTSCR with the gate-substrate-triggered LVTSCR.

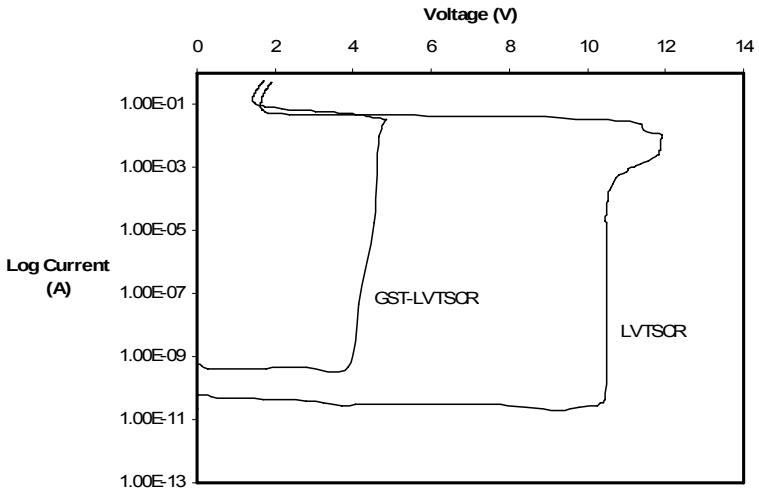


*Figure 2-22: Simulated I-V characteristic of LVTSCR and GST-LVTSCR*

It can be seen that for the conventional LVTSCR, the first breakdown voltage is 12V and the holding voltage is 1.5V. With the gate-substrate triggering technique, the first breakdown voltage is reduced to 4.85V, while the holding voltage is 1.45V. In order to confirm that this circuit can provide enough protection, the thin oxide breakdown voltage for different technologies is shown in Figure 2-23 [32].

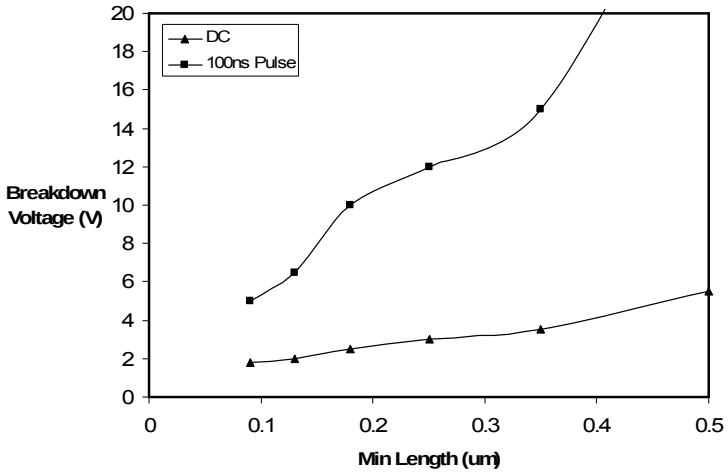


*Figure 2-23: Breakdown voltage of the thin oxide for different CMOS technologies*

It can be seen that for 0.18μm technology, the oxide breakdown voltage for a 100ns ESD stress is 10V. Hence, the first breakdown voltage in the proposed protection circuit is low enough to provide the required ESD protection.

This gate-substrate triggered LVTSCR was fabricated in 0.13μm UMC CMOS process. The width of the LVTSCR was set to 100μm. The widths of the substrate triggering NMOS and gate coupling NMOS were set to 20μm and 5μm respectively. The effectiveness of this structure has been evaluated using two major test methods: Transmission Line Pulse (TLP) and HBM tests.

Transmission Line Pulse (TLP) test is a method to characterize the I-V characteristic of ESD protection devices, which was first introduced by Maloney and Khurana in 1985 [33]. This method, which is the most common test in industry, allows reliable and repeatable test of ESD structures. TLP uses the rectangular pulse testing to simulate the damage level caused by an HBM stress. These pulses are 100ns wide with 2-10ns rise time [34]. It should be noted that the TLP waveform doesn't represent any real world ESD event.

HBM test is simply done by applying an HBM stress to the device and monitoring its failure. In other words, the I-V characteristic of the device is tested before and after the stress to determine a pass or fail. The voltage level is increased until the device fails.

In this work, TLP measurements were provided using Pulsar 900 TLP system from SQP products. Figure 2-24 shows the TLP measurement results for the gate-substrate triggered LVTSCR shown in Figure 2-20.

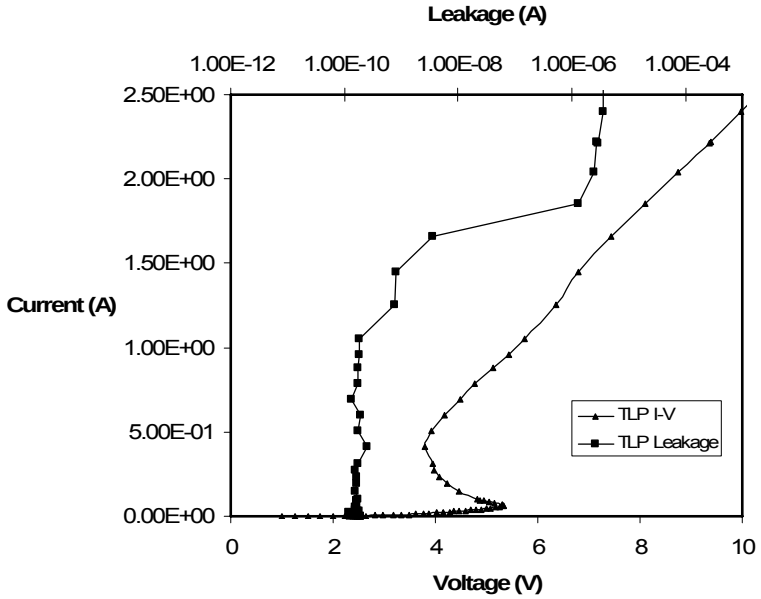


*Figure 2-24: TLP measurement results for gate-substrate triggered LVTSCR*

It can be seen that TLP results are in the form of two graphs: current vs. voltage and current vs. leakage. The former represents the I-V characteristic of the device and the latter shows the leakage of the device under normal operating conditions. The second breakdown current of the device is also determined from the current-leakage graph. The current at which the leakage current shows a rapid change is the second breakdown current. Hence, it can be seen that for gate-substrate triggered LVTSCR the first breakdown voltage is 5V and the second breakdown current is 1.8A.

Referring back to Figure 2-22, simulation results predict a first breakdown voltage of 4.85V for GST-LVTSCR, which shows a good agreement with the 5V resulted from TLP measurements.

It has been shown that the HBM protection level and the second breakdown current are related in the form of $V_{HBM}(kV)=K\times I_{t2}(A)$, where, depending on technology and test setup, K is between 0.96 and 1.71. Therefore, 1.8A second breakdown current corresponds to an HBM protection level of up to 3.1kV.

In addition to the TLP measurement, we did the HBM test on this device as well. These measurements were done using IMCS-700 HBM/MM ESD tester. We applied both positive and negative HBM stresses with 500V step sizes. The gate-substrate triggered LVTSCR passed 3kV stress but fails 3.5kV stress. Therefore, this device has 3kV ESD robustness.

### 2.4.2 Darlington-based SCR

As mentioned in Section 2.3, the most common method to reduce the first breakdown voltage of SCR-based devices is to apply different triggering mechanisms to either SCR or LVTSCR. The most important drawback of this method is the addition of extra parasitic capacitance to the pad, which can limit the performance in high speed mixed-signal applications. In this work, we tried to modify the cross section of a typical SCR device to reduce its first breakdown voltage without adding extra parasitic capacitance to the pad. In order to understand the principle of the new device, consider the schematic of an SCR which is shown in Figure 2-25(a). Referring back to the breakdown mechanism

of this device, the first breakdown voltage is the anode-cathode voltage when the generated avalanche breakdown current of the well-substrate junction turns on the bipolar transistors. This voltage can be reduced by increasing the current gain of the bipolar transistors. Therefore, if a darlington pair is used instead of a single bipolar transistor the first breakdown voltage of the new device should be less than SCR. Figure 2-25(b) shows the schematic of this device.

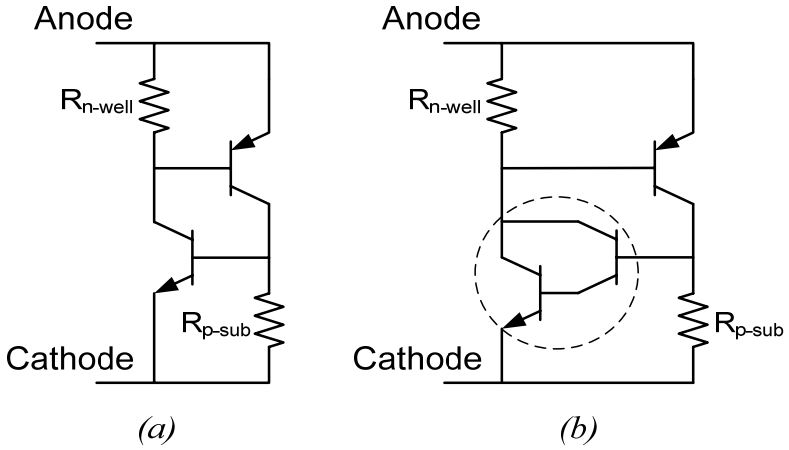


*Figure 2-25: (a) conventional SCR (b) darlington-based SCR*

The extra transistor is implemented by inserting an extra n-well region in the SCR structure. Figure 2-26 shows the cross section of this device.

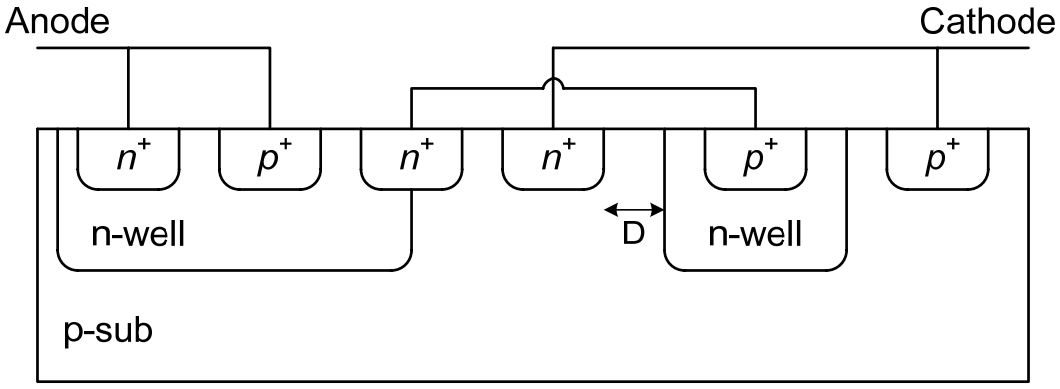


*Figure 2-26: Cross section of the darlington-based SCR device*

Gain of the additional transistor, and hence, the first breakdown voltage of the device, is a function of the distance between the n-well and the $n^+$ diffusion regions which is called "D". In order to verify the effectiveness of this method, this device is simulated in Medici using the parameters of the 0.18μm CMOS technology. The simulations are done

in quasi-dc conditions to generate the I-V characteristic of the new device. Figure 2-27 shows the I-V curve for the new device with D=0.7μm and 1μm and compares it with the conventional SCR device. It should be noted that the y-axis is in logarithmic scale.

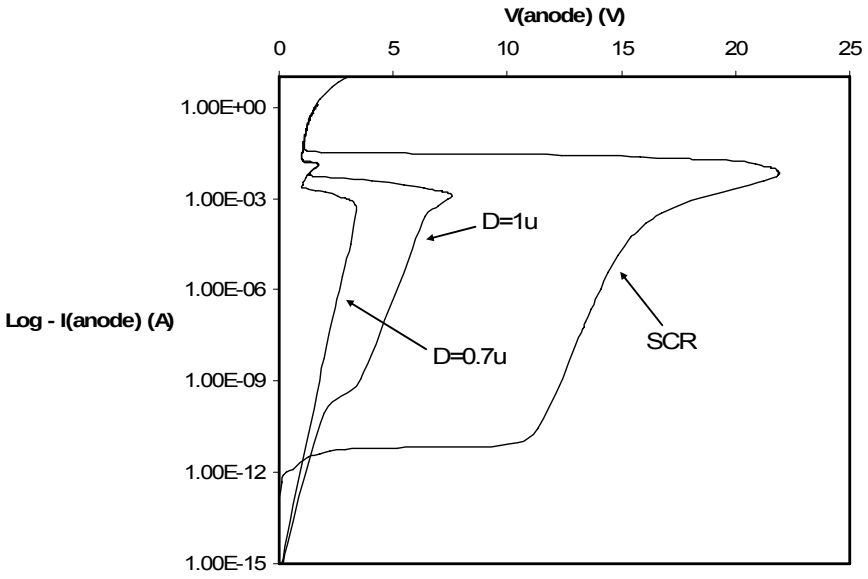


*Figure 2-27: Simulating darlington-based SCR and conventional SCR*

It can be seen that with proper design, inserting a darlington pair in the SCR structure reduces the first breakdown voltage from 22V to 3.2V which is low enough for 0.18μm CMOS technology. This voltage can be further reduced to 1.5V by setting D=0.5μm.

Another important feature of this device is that its parasitic capacitance is similar to the original SCR, which can be easily verified by comparing the cross section of the two devices. The parasitic capacitance of both devices is mainly the capacitance of the well-substrate junction. On the other hand, in an LVTSCR-based design with a triggering mechanism, the parasitic capacitance is the well-substrate junction capacitance in addition to the gate capacitance of the LVTSCR plus the parasitic capacitance of the additional transistors required for triggering. Hence, it is expected that, for a first breakdown voltage of less than 5V, the proposed darlington-based SCR device has a much lower parasitic capacitance compared to other SCR-based protection devices. In order to verify this issue, the parasitic capacitance of these devices should be simulated. The ESD protection device is modeled with its parasitic capacitor $C_{ESD}$ and parasitic resistor $R_{ESD}$. Both AC and transient simulations were done to ensure the accuracy of the

results. Figure 2-28 shows the setup used to simulate the capacitance of ESD protection devices.

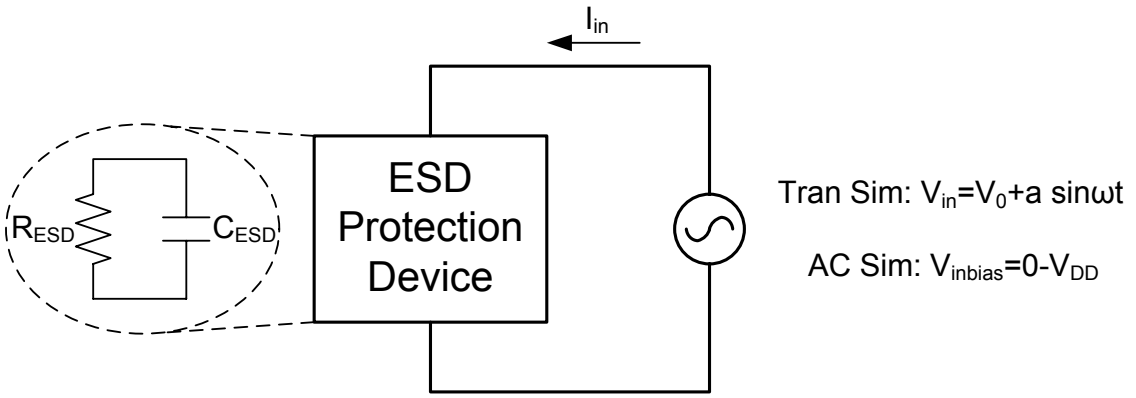


*Figure 2-28: Simulating the capacitance of ESD structures*

In transient simulation, a sine input voltage is applied to the device. The magnitude of this sine wave is very small (less than 20mV). Modeling the device with a parallel RC, the input current is calculated as follows:

$$I_{in} = \frac{V_{in}}{R_{ESD}} + C_{ESD}\frac{dV_{in}}{dt} = \frac{V_0}{R_{ESD}} + \frac{a}{R_{ESD}}\sin\omega t + aC_{ESD}\omega\cos\omega t \tag{2-4}$$

The peak values of $I_{in}$ are found by setting $dI_{in}/dt$ to zero:

$$\frac{dI_{in}}{dt} = 0 \Rightarrow \frac{a\omega}{R_{ESD}}\cos\omega t - aC_{ESD}\omega^2\sin\omega t = 0 \tag{2-5}$$

Running the simulation in Medici, the $I_{in}$ waveform is obtained. By applying equations 2-4 and 2-5 to one of the maximum points in the $I_{in}$ waveform, the two unknowns $R_{ESD}$ and $C_{ESD}$ for different values of $V_0$ are calculated.

In the second method, an AC simulation is done for different DC input voltages between 0 and 1.8V. Using the dc input current the value of $R_{ESD}$ is calculated as $V_{DD}/I_{in}$. In the next step $C_{ESD}$ is calculated from the input impedance that is extracted from the AC simulation. The difference between $C_{ESD}$ calculated from the above two methods is less than 5%. Figure 2-29 compares the capacitance of the darlington-based SCR, LVTSCR and substrate triggered LVTSCR at 1GHz when the pad voltage is increased from 0 to 1.8V.

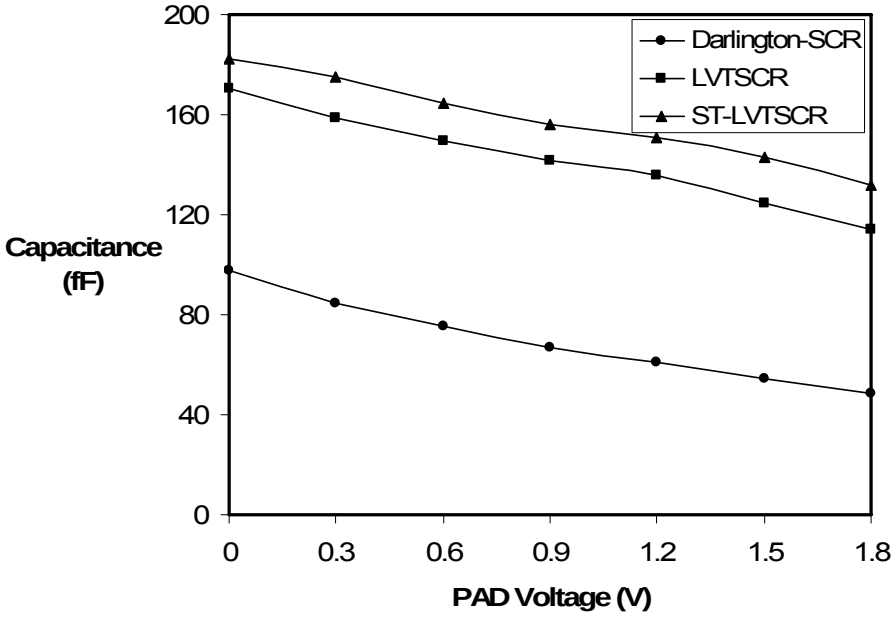


*Figure 2-29: Simulating the capacitance of different ESD structures*

In this figure, the widths of all SCR-based devices are set to 100µm. It can be seen that the darlington-based SCR has a very low parasitic capacitance compared to other SCR-based devices. For a similar first breakdown voltage of 5V or less, darlington-based SCR reduces the parasitic capacitance from 185fF to 97fF.

In order to verify the simulation results, a 100µm wide darlington-based SCR with D=0.7µm was fabricated in 0.18µm CMOS technology to verify the simulation results. For this device, both TLP and HBM measurements have been done. Figure 2-30 shows the TLP measurement results for this device.

It can be seen that the first breakdown voltage of this device is 3V. Referring back to Figure 2-27, simulation results predict a first breakdown voltage of 3.2V. Hence, TLP measurement results confirm our simulations. Furthermore, the second breakdown current is over 4A (the complete waveform is not shown in here for more visibility of the I-V curve).Therefore, the HBM protection level of this device is expected to be above 6kV.

In addition to TLP measurement, HBM test has been done on this device as well. As it was expected from TLP results, the device passed ±6kV HBM stresses.

It should be noted that, as 6kV HBM protection level is much more than usual standard requirement, the width of the darlington-based SCR can be reduced to further reduce the parasitic capacitance.

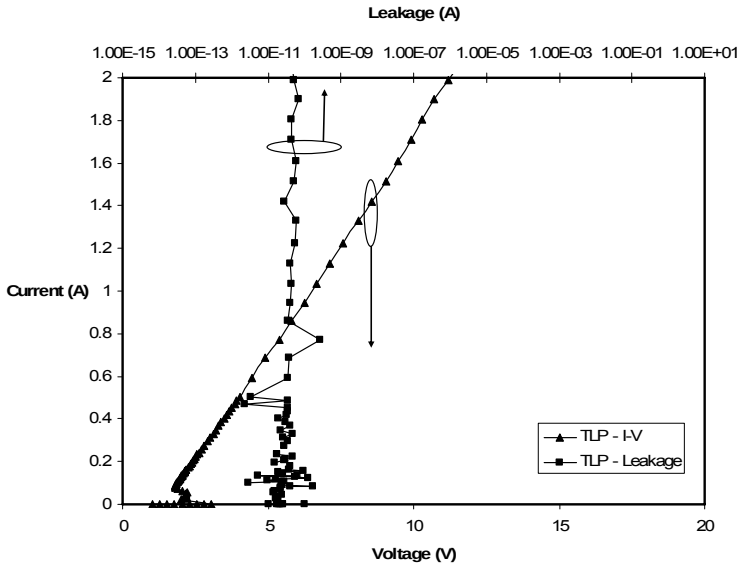


*Figure 2-30: TLP measurement results for the darlington-based SCR*

### 2.4.3 Increasing the holding voltage

In order to understand the concept of increasing the holding voltage, consider the equivalent circuit of an SCR, which is shown again in Figure 2-31.

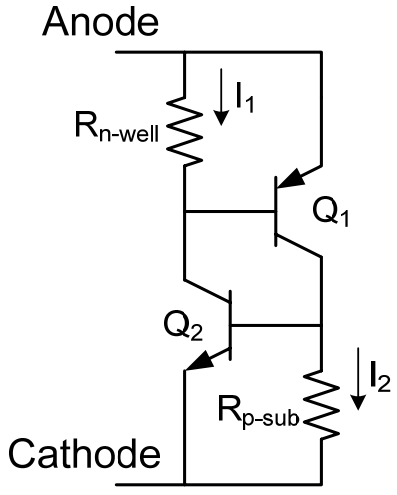


*Figure 2-31: Equivalent circuit of SCR*

After SCR triggers and goes into holding region, due to the internal positive feedback, both bipolar transistors are conducting and are biased in the saturation region. Holding voltage is the voltage across anode-cathode that keeps both transistors in the saturation region. Therefore, the holding voltage of the SCR can be calculated from the following equation.

$$V_h = V_{EB1} + V_{CE2(sat)} \tag{2-6}$$

Knowing that $V_{EB1}$ is between 0.7V and 1V and $V_{CE2(sat)}$ is around 0.5V, the holding voltage of the SCR is expected to be less than 2V.

In order to increase this voltage, the voltage needed to keep both bipolar transistors "on" should be increased. The simplest method is to decrease either $R_{n\text{-well}}$ or $R_{p\text{-sub}}$. As a result, higher avalanche breakdown current is needed to create enough voltage across these resistors to keep the bipolar transistors "on" and hence, $V_h$ is increased. As this method involves increasing well or substrate doping, it's not a practical solution for a circuit designer. Instead of increasing the well or substrate doping, one can increase the required voltage across $R_{n\text{-well}}$ or $R_{p\text{-sub}}$ by inserting a resistor in series with the emitter of one of the two bipolar transistors. Figure 2-32 shows the equivalent circuit and the cross section of this device.

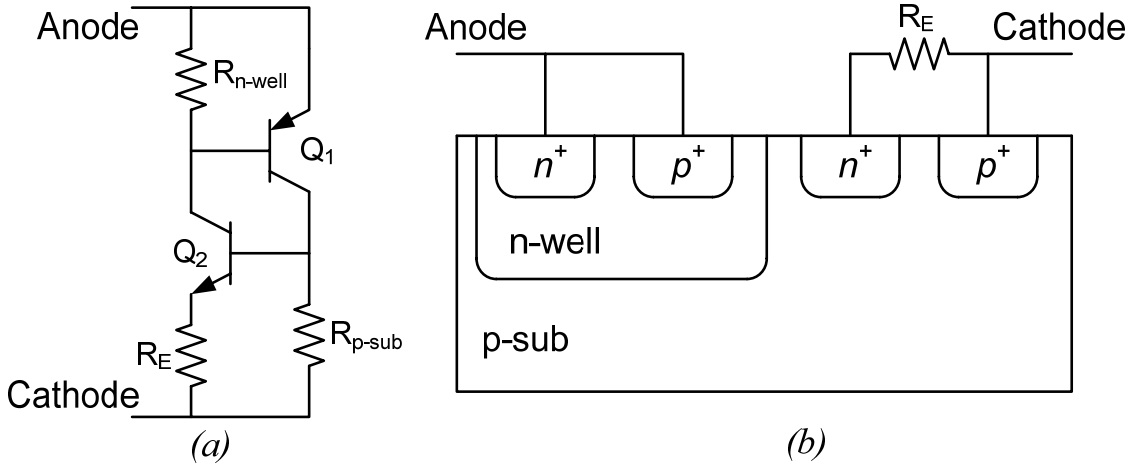


*Figure 2-32: Increasing the holding voltage of SCR (a) equivalent circuit (b) cross section*

Based on Figure 2-32(a), the holding voltage of this device can be calculated from the following equation.

$$V_h = V_{EB1} + V_{CE2(sat)} + I_{E2}R_E = V_{EB1} + V_{CE2(sat)} + \frac{V_{EB1}R_E}{R_{n-well}} \quad (2\text{-}7)$$

In this equation it is assumed that the base currents of the two bipolar transistors are negligible. This is not a very accurate assumption, especially that the base areas of these two transistors are very large, which means that their current gain (β) is small. But it suggests that a relatively linear increase in holding voltage is expected. As the actual value of $I_{E2}$ is $V_{EB1}/R_{n\text{-well}}$ plus two base currents, the increase in holding voltage for higher values of $R_E$ is expected to be more than the linear approximation. This discussion can be verified using Medici simulation results. The cross section of SCR is created based on the process parameters of 0.18μm CMOS technology. Figure 2-33 shows the holding voltage of the new SCR for different values of $R_E$.

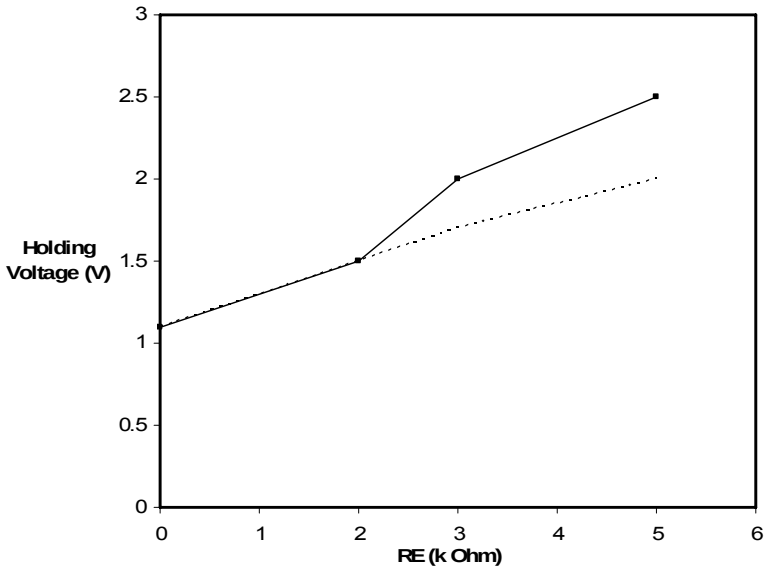


*Figure 2-33: Impact of $R_E$ on the holding voltage of SCR*

Figure 2-34 shows the I-V characteristic of the SCR with high holding voltage option for different values of $R_E$. It should be noted that using this method, while the holding voltage is increased, the first breakdown voltage is constant.

It should be noted that the above discussion is valid for any device that is based on SCR operation. The added resistor in this modified SCR can be implemented using a poly resistor, a diode or a MOS transistor. Figure 2-35 shows the cross section of this SCR where $R_E$ is implemented with a MOS transistor.

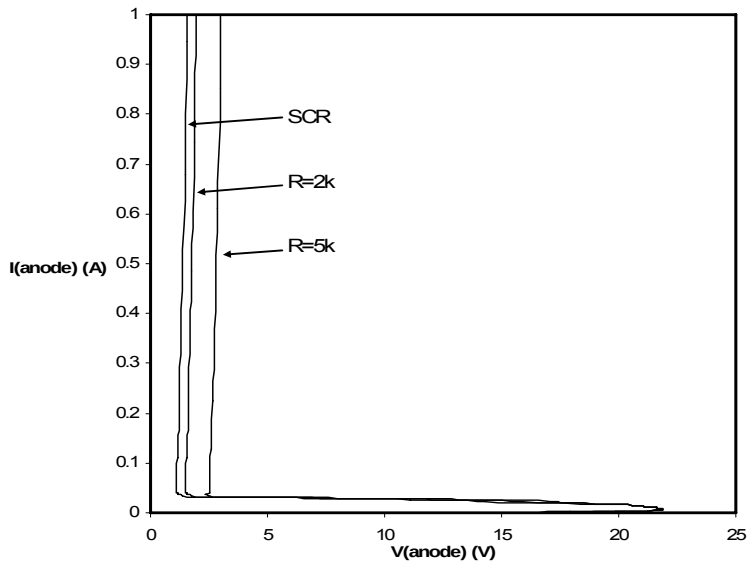


*Figure 2-34: Simulating the I-V characteristic of SCR with high holding voltage option*

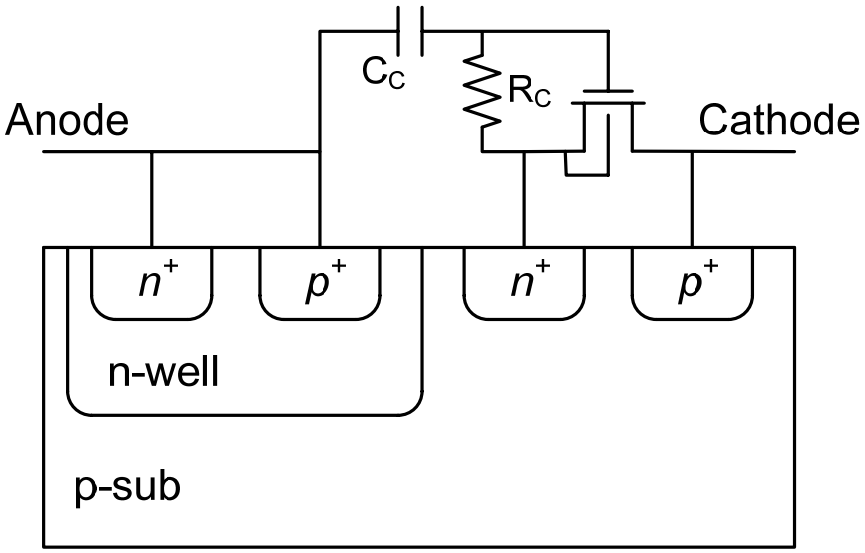


*Figure 2-35: Implementing high holding voltage option with an NMOS transistor*

In order to verify the simulation results, an LVTSCR with different high holding voltage options was implemented in 0.13μm CMOS technology. The resistor $R_E$ was implemented with MOS and diode. Figure 2-36 shows the TLP measurements for these two implementations and compares them with a conventional LVTSCR.

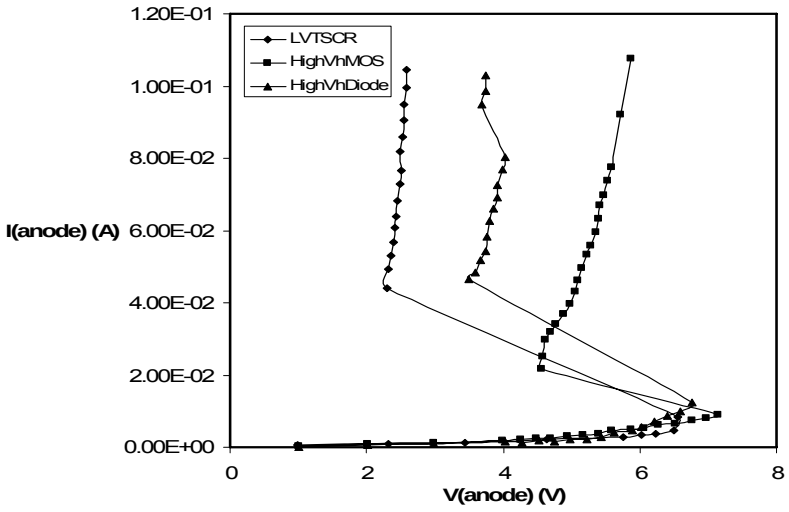


*Figure 2-36: TLP measurement results for LVTSCR with high holding voltage option*

It can be seen that using a diode, the holding voltage is increased from 2.29V to 3.49V. Using an NMOS the holding voltage is further increased to 4.55V. At the same time, the first breakdown voltage is slightly increased as well by 2% and 8% for diode and NMOS representation of $R_E$ respectively.

### 2.4.4 Increasing the holding current

In addition to increasing the holding voltage, latch-up immunity can be achieved by increasing the holding current or first breakdown current as well. In this research a new method to increase the holding current is presented. Considering the equivalent circuit of the SCR shown in Figure 2-31, the holding current of SCR can be calculated from the following equations.

$$I_2 + I_{B2} = I_{C1} = \beta_1 I_{B1} \tag{2-8}$$

$$I_1 + I_{B1} = I_{C2} = \beta_2 I_{B2} \tag{2-9}$$

$$I_h = I_1 + I_{E1} = \frac{V_{EB1}}{R_{n-well}} + (\beta_1 + 1) I_{B1} \tag{2-10}$$

By calculating $I_{B1}$ from equations (2-8) and (2-9) and substituting it into (2-10) the holding current of SCR is calculated from the following equation.

$$I_h = \frac{\beta_1(\beta_2+1)}{\beta_1\beta_2-1}\frac{V_{EB1}}{R_{n-well}} + \frac{\beta_2(\beta_1+1)}{\beta_1\beta_2-1}\frac{V_{BE2}}{R_{p-sub}} \quad (2\text{-}11)$$

This equation can be simplified by neglecting the base currents of the two bipolar transistors. In other words, assuming that $\beta_1$, $\beta_2 >> 1$, the holding current is calculated from the following equation.

$$I_h = \frac{V_{EB1}}{R_{n-well}} + \frac{V_{BE2}}{R_{p-sub}} \quad (2\text{-}12)$$

In order to increase the holding current, an extra current path is added to the SCR. Figure 2-37(a) shows the equivalent circuit of the new SCR where the extra path is added through a resistor. In order to implement this structure an $n^+$ region is added to the boundary of the well-substrate junction as shown in Figure 2-37(b).

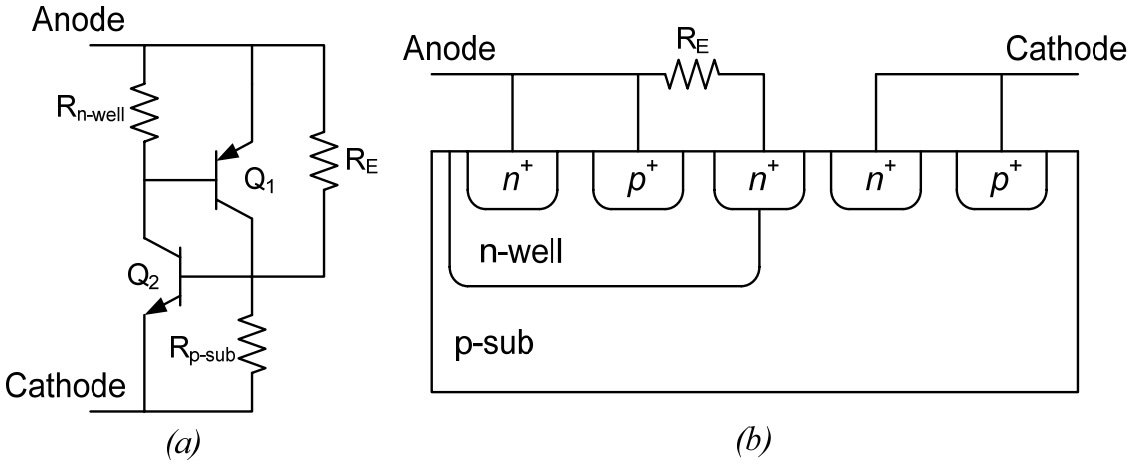


*Figure 2-37: Increasing the holding current (a) schematic (b) cross section*

The holding current of the new SCR is increased by the current of the resistor $R_E$.

$$I_h = \frac{V_{EB1}}{R_{n-well}} + \frac{V_{BE2}}{R_{p-sub}} + \frac{V_{CE1(sat)}}{R_E} \quad (2\text{-}13)$$

Hence, the amount of the increase in the holding current is directly proportional to the conductance of the added resistor. This relation can be verified by simulating the device in Figure 2-37(b) using Medici device simulator. Figure 2-38 shows the impact of $R_E$ on the holding current. Linear dependence of the holding current on $1/R_E$ is clearly visible in this graph.

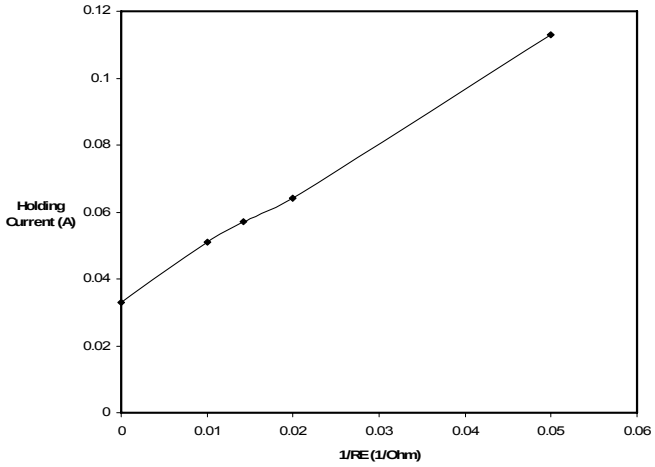


*Figure 2-38: Impact of $R_E$ on the holding current of the SCR*

Figure 2-39 shows the I-V characteristic of the new SCR. It can be seen that using this method, as the holding current increases, the holding voltage and the first breakdown voltage remain constant. Hence, this method improves the holding current without sacrificing other important ESD parameters. This resistor can be realized using either a poly resistor or a forward biased diode.

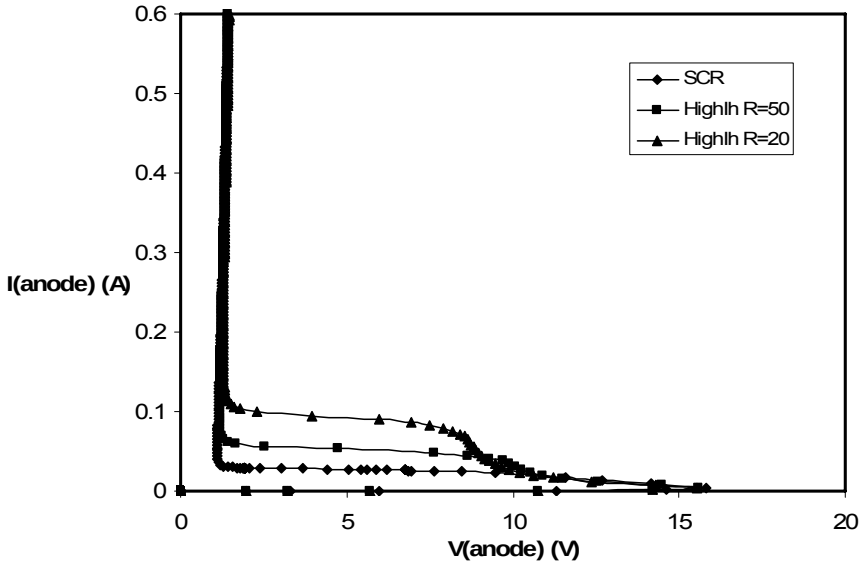


*Figure 2-39: Simulating the I-V characteristic of the new SCR for $R_E$=20Ω and 50Ω*

In order to verify the simulation results, an LVTSCR with different high holding current options was implemented in 0.13μm CMOS technology. The resistor $R_E$ was implemented with a 20Ω and 50Ω poly resistors in addition to a forward biased diode.

Figure 2-40 shows the TLP measurement results for these three implementations and compares them with a conventional LVTSCR.

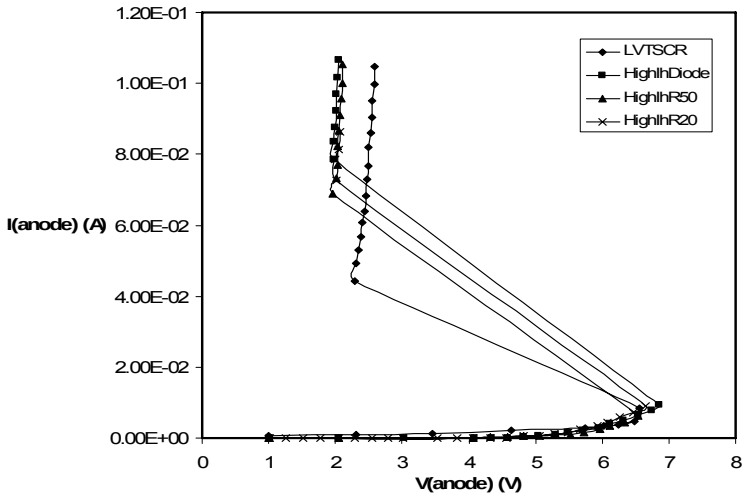


*Figure 2-40: TLP measurement results for LVTSCR with high holding current option*

It can be seen that, by reducing $R_E$, the holding current is increased. The highest increase in holding current is with forward biased diode where the holding current of LVTSCR is increased from 44.1mA to 78.5mA.

Simulation results in Figure 2-39 predict a holding current of 100mA for SCR with $R_E$=20Ω. On the other hand, TLP measurements show a holding current of 74mA for LVTSCR with similar value for $R_E$. This difference can be due to tolerance of the poly resistor and using LVTSCR instead of SCR.

## 2.5 Summary

In section 2.4 novel techniques were presented to overcome SCR limitations: high first breakdown voltage and latch-up susceptibility. Gate-substrate triggered LVTSCR and darlington-based SCR were designed to reduce the first breakdown voltage and high holding voltage and high holding current LVTSCR devices were designed to improve latch-up immunity. In order to evaluate the effectiveness of these methods, a brief comparison between the proposed methods and state of the art designs is provided in tables 2-1 and 2-2.

Table 2-1 compares different methods to reduce the first breakdown voltage. In addition to ESD response, the parasitic capacitance of the ESD protection circuit is very important in high speed applications. As the parasitic capacitance of DT-SCR and NAN-SCR were not provided in literature, their parasitic capacitance was estimated based on their dimensions provided in the paper. Poly SCR has been reported to have the smallest parasitic capacitance [24]. Based on the Table 2-1, it can be seen that the proposed darlington-based SCR has the second smallest parasitic capacitance. However, the poly SCR was designed with smaller width and hence, with lower HBM protection level. Furthermore, the first breakdown voltage of the poly SCR is very high, which may not be suitable for deep submicron CMOS technologies. As a result, darlington-based SCR provides the lowest first breakdown voltage with lowest parasitic capacitance and highest ESD protection level.

*Table 2-1: Summary of different methods to reduce the first breakdown voltage*

| | Technology | HBM level | $V_{t1}$ | Capacitance | Comments |
|---|---|---|---|---|---|
| DT-SCR, 2003 [23] | 0.25µm | >6kV | 7V | 160fF | - |
| NAN-SCR, 2005 [25] | 0.13µm | 3kV | 4V | 130fF | - |
| Poly SCR. 2005 [24] | 0.35µm | 3.15kV | 9V | 92.3fF | W=75µm |
| GST-LVTSCR | 0.13µm | 3kV | 5V | 185fF | - |
| Darlington SCR | 0.18µm | >6kV | 3V | 97fF | W=100µm |

Table 2-2 provides a comparison between different techniques that improve latch-up immunity. It can be seen that high holding voltage has been achieved with different methods. However, they increase the first breakdown voltage as well. This increase is very significant in methods provided in [26] and [27]. In these two references, the first breakdown voltage is reduced by applying substrate triggering to the SCR or LVTSCR.

On the other hand, the high $V_h$ method proposed in this work shows an increase of only 8% in the first breakdown voltage. Similarly, the proposed high $I_h$ technique increases the first breakdown voltage by only 4%. Hence, the two proposed methods are the most effective solutions to improve latch-up immunity.

*Table 2-2: Summary of different methods to improve latch-up immunity*

| | Technology | $V_h$ | Impact on $V_{t1}$ | $I_h$ |
|---|---|---|---|---|
| Cascode LVTSCR, 1998 [26] | 0.35µm | 6.3V | 6V→11V | - |
| Cascode SCR+Diode, 2003 [27] | 0.25µm | 5.8V | 22V→28V | - |
| Dynamic $V_h$, 2004 [28] | 0.25µm | 2.7V | 3.5V→7V | - |
| HHI-SCR, 2002, [29] | 0.1µm | 2.4V | - | 68mA |
| High $V_h$ LVTSCR | 0.13µm | 4.55V | 6.5V→7.1V | - |
| High $I_h$ LVTSCR | 0.13µm | 1.9V | 6.5V→6.8V | 78.5mA |

# Chapter 3

# 3. Non-Snapback-Based Protection

Based on the discussion in Chapter 1, non-snapback-based protection methoduses diodes and a clamp to provide ESD protection for all four zapping modes. The clamp is designed based on non-avalanching junctions to allow use of circuit level simulators. In Section 3.1 a brief overview of the non-snapback based protection is provided and two categories of clamps are introduced. Section 3.2 discusses static ESD clamps, while transient clamps, which are used in non-snapback-based protection scheme, are described in Section 3.3. State of the art transient clamps are reviewed in Section 3.4. Oscillation of transient clamps along with a novel analysis method is discussed in Section 3.5. Finally, Sections 3.6 and 3.7 discuss two new clamps proposed in this work.

## 3.1 Introduction

As mentioned in the first chapter, ESD protection circuit is required for both I/O and supply pads. The devices discussed in chapter 2 operate in avalanche breakdown region

under ESD conditions and are used in snapback-based protection. On the other hand, non-snapback-based protection method uses non-avalanching junctions where the ESD charge is transferred to power rails and discharged through the clamp. Figure 3-1 shows the block diagram of this method.

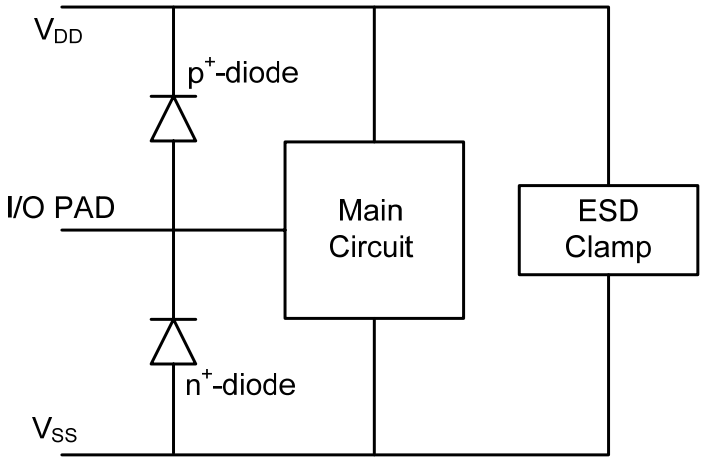


*Figure 3-1: Non-snapback-based protection method*

Although in non-snapback method clamps are designed with non-avalanching junctions, ESD clamps, as the protection between $V_{DD}$ and $V_{SS}$, have more implementations.

Clamps are grouped into two categories: static clamps and transient clamps. Static clamps provide a static or steady-state current and voltage response. A fixed voltage level activates static clamps. As long as the voltage is above this level, the clamp conducts current. Based on the discussions in chapter 2, it can be seen that a diode, MOSFET or SCR based circuit can be used in static clamps. On the other hand, transient clamps take advantage of the rapid changes in voltage and/or current that accompanies an ESD event. During this transient, the clamp is turned on very quickly and turned off very slowly. This type of clamp conducts for a fixed time when it is triggered. An RC network determines the time constant. These clamps are typically triggered by very fast events on the supply line.

Transient clamps are more common than static clamps mainly because they are easier and faster to simulate. Furthermore, they trigger faster and are capable of handling large transient events. Usually in transient clamps devices are not operating in their breakdown

region and hence, are able to be simulated in circuit level simulators such as Cadence. As a result, non-snapback protection method uses transient clamps.

## 3.2 Static ESD Clamps

Static clamps should provide a low impedance discharge path during an ESD event, while consuming minimum current when the supply voltage is connected to $V_{DD}$. Hence, the triggering voltage of the clamp should be higher than the maximum supply voltage. In other words, the first breakdown voltage of the devices in an ESD clamp should be higher than the supply voltage. As mentioned earlier, diode, MOS and SCR are the most common devices in static ESD clamps. The device selection is usually done based on process limitations, current carrying capability and turn on time.

### 3.2.1 Diode-based ESD clamps

The forward biased diode is usually used in static clamps due to its high current carrying capability. However, as its breakdown voltage is very low, a stack of forward biased diodes are placed between $V_{DD}$ and $V_{SS}$ [35]. On the other hand, as the number of diodes in the stack is increased, the leakage of the supply line is increased as well. Furthermore, as leakage increases with temperature, this problem becomes more severe in high temperature applications. Therefore, in order to overcome this limitation, cantilever diode string was introduced to block the diode string when the IC is in the normal operating mode [36], [37]. Figure 3-2 shows the schematic of the static clamp with cantilever diode string.

In this figure, the PMOS transistor $M_1$ is used to terminate the diode string from $V_{SS}$ in normal operating mode. But it sinks a substantial amount of current when an ESD pulse occurs. The PMOS transistor $M_2$ and the MOS-capacitor C are used as an RC-based ESD detection circuit to distinguish the ESD stress from normal $V_{DD}$ voltage and trigger $M_1$ accordingly. PMOS transistors M3 and M4 are long channel devices that are used as

the bias network. The small NMOS transistor M5 provides a ground connection without allowing a power supply voltage drop across the single thin gate oxide.

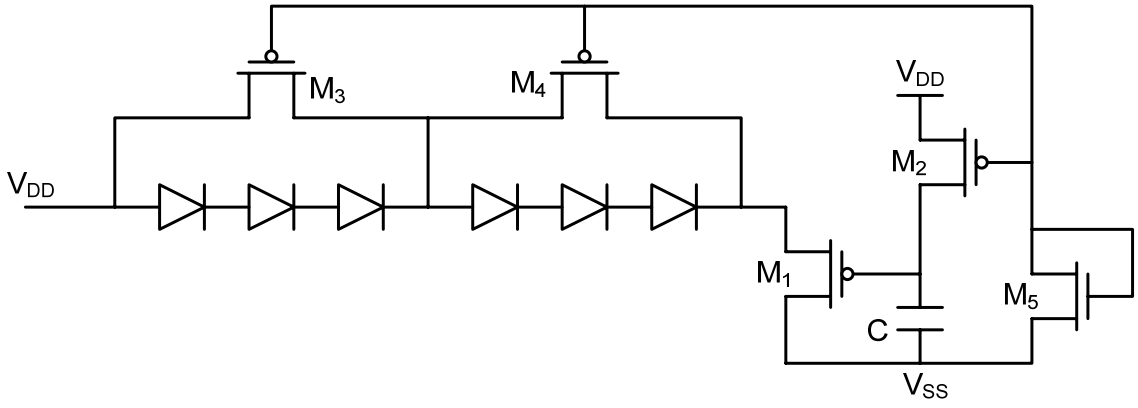


*Figure 3-2: Cantilever diode string*

### 3.2.2 MOS-based ESD clamps

The most common MOS-based ESD clamp consists of a simple grounded-gate NMOS, which was discussed in detail in Chapter 2. The advantage of this structure is its relatively small area. On the other hand, high triggering voltage and slow response time are the main concerns of in this clamp. Therefore, often gate triggering by a zener diode or a stack of diodes is applied to the original grounded gate NMOS [38], [39].

### 3.2.3 SCR-based ESD clamps

Due to its high current capability, lateral SCR device is often used in static clamps as well. On the other hand, as it was discussed in chapter 2, high triggering voltage and low holding voltage of this device requires extra modifications. Therefore, LVTSCR with high holding voltage [26] and LVTSCR with high holding current [29] are often used as static clamps.

## 3.3 Transient Clamps

Transient clamps take advantage of rapid changes in the voltage and/or current that accompanies an ESD event. In other words, they are triggered by very fast events on the supply lines. During this fast transition, a semiconductor device is turned on very quickly and is turned off very slowly to discharge all the ESD energy. This type of clamp conducts for a fixed time interval when it is triggered. In the simplest form, a transient clamp consists of an NMOS transistor that discharges the ESD energy and is triggered with an RC circuit. Several key advantages of transient clamps are the ability to provide ESD protection at low voltages, no extra process step requirement, relaxed layout constraints, and easy SPICE simulations [40], [41]. Their disadvantage is that they also respond to any fast event on the supply line, even noise. Hence, the most common drawback of these clamps is false triggering where they trigger during normal power-up conditions.

Figure 3-3 shows the schematic of the first implementation of a transient clamp which is called the inverter-based transient clamp [42], [43].

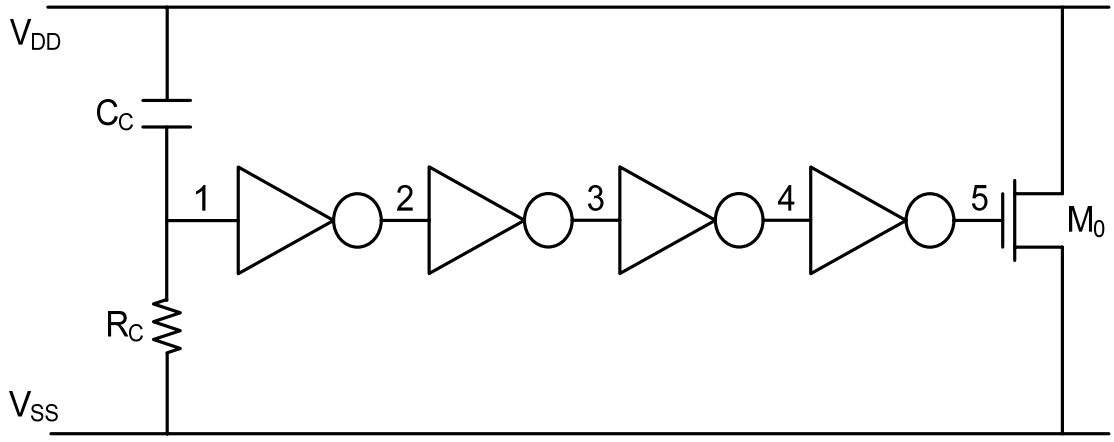


*Figure 3-3: Inverter-based transient clamp*

In this clamp, the transistor $M_0$ discharges the ESD current. As this clamp is designed to be simulated with circuit level simulators, this transistor should be able to carry the ESD current without going into breakdown region. As a result, knowing that the peak ESD current is few amperes during an HBM ESD stress, $M_0$ is should be up to a few

millimeters wide. The trigger circuit consists of a simple $R_C C_C$ network which is activated during an ESD event. This trigger circuit should turn on $M_0$ at an ESD event and keep it on for the whole ESD duration. The operation of this clamp is as follows: when an ESD event between $V_{DD}$ and $V_{SS}$ occurs, the voltage of the $V_{DD}$ node increases rapidly. This sudden increase in the voltage of the $V_{DD}$ node is transferred to node 1 as well. After passing through four inverters, the voltage of the node 5 increases as well and turns on the transistor $M_0$. The four stage inverter is used to drive the huge transistor $M_0$ in addition to reduce the impact of high frequency noise on the supply line.

In order to avoid turning on the clamp during a normal power-up event, the trigger circuit takes advantage of the difference between the rise time of an ESD event and the rise time of a normal power-up event. Typically, the power-up of an IC has a rise time in the millisecond range. On the other hand, the rise time of an ESD event is between 100ps and 60ns and it lasts for less than 1µs. Hence, a simple RC network can distinguish these two events. In Figure 3-3, $R_C C_C$ time constant is usually set to 600ns-1µs to be able to discharge the ESD energy completely. Therefore, it requires a huge on-chip resistor and capacitor.

It can be seen that this method requires huge transistors and capacitors and hence, consumes a very large area. However, only one transient clamp is required for the whole chip and the rest of the pads are connected to $V_{DD}$ and $V_{SS}$ through diodes. Therefore, compared to the total area of a chip, the area of the clamp is negligible. Figure 3-4 shows a diagram of the complete protection of an IC.

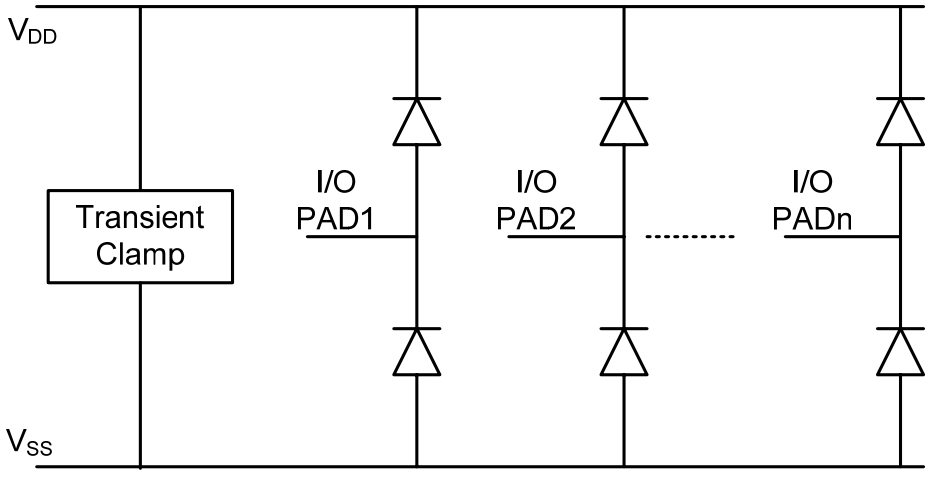


*Figure 3-4: Complete protection of an IC*

Figure 3-4 shows that in this method the parasitic capacitance added to I/O pads is only the capacitance of the two diodes. The parasitic capacitance of the clamp is added to $V_{DD}$ and $V_{SS}$ lines where there isn't any low parasitic requirement.

Although Figure 3-4 shows that one clamp is enough to provide ESD protection for the whole chip, in large chips the resistance of $V_{DD}$ and $V_{SS}$ busses causes non-uniform ESD path for different pads. Knowing that the current of an ESD event is in ampere range, even a few ohm resistance creates a big voltage drop across $V_{DD}$ and $V_{SS}$ lines. For example, assume that the total resistance of the $V_{DD}$ and $V_{SS}$ lines is 2Ω. Hence, a 3A ESD current creates 6V voltage drop across the supply lines which makes it impossible to protect the circuit without biasing the main transistor in the snapback region. Therefore, instead of designing one big clamp to discharge all the ESD current, the clamp is divided into several smaller clamps and each of them is placed near an I/O pin [44]. Sizing of the smaller clamps is done in such a way that the total area of clamps is equal to the size of the original big clamp. Using this method, uniform ESD performance for all pins is obtained. It should be noted that only one trigger circuit is required for all the clamps. Figure 3-5 shows the distributed clamp network.

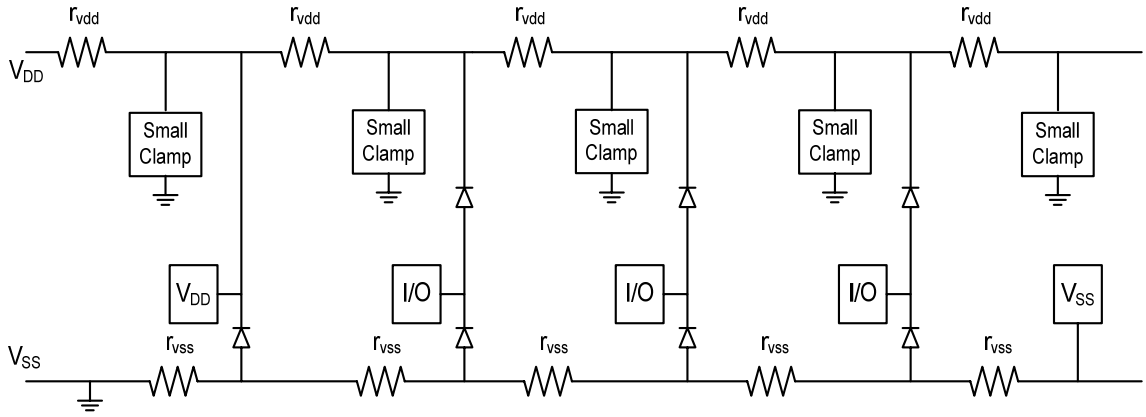


*Figure 3-5: Distributed clamp network*

One of the major drawbacks of the inverter-based transient clamp is false triggering. As mentioned earlier, the $R_C C_C$ time constant of the trigger circuit in this clamp is usually set to 600ns-1μs. Therefore, if the power-up of the IC has a millisecond rise time the clamp doesn't turn on and is immune to false triggering. However, some applications such as "hot-plug" operations or switching networks controlling the sleep power mode in

low-power high-performance microprocessors result in much faster power up times in the order of a few microseconds [45] or even hundreds of nanoseconds [46]. Therefore, the trigger circuit responds to normal power-up of the circuit as well and turns on the clamp during normal operating conditions.

Moreover, it has been recently shown that this clamp may be unstable as well [47]. This instability is usually observed as high frequency oscillation on the $V_{DD}$ and $V_{SS}$ rails during power-up or ESD event. The source of these oscillations is discussed in detail in section 3-5.

In order to solve the false triggering problem, the triggering circuit is divided into two sections: rise time detector and delay element. The rise time detector is a simple RC network, which determines the rise time of an ESD event and is usually set to 40ns [40]. Hence, even very fast power-up events with microsecond rise time range do not trigger the clamp. The delay element creates a delay equal to the whole ESD event to keep the main protection transistor $M_0$ "on" to discharge all the ESD energy. Figure 3-6 shows the block diagram of this modified transient clamp.

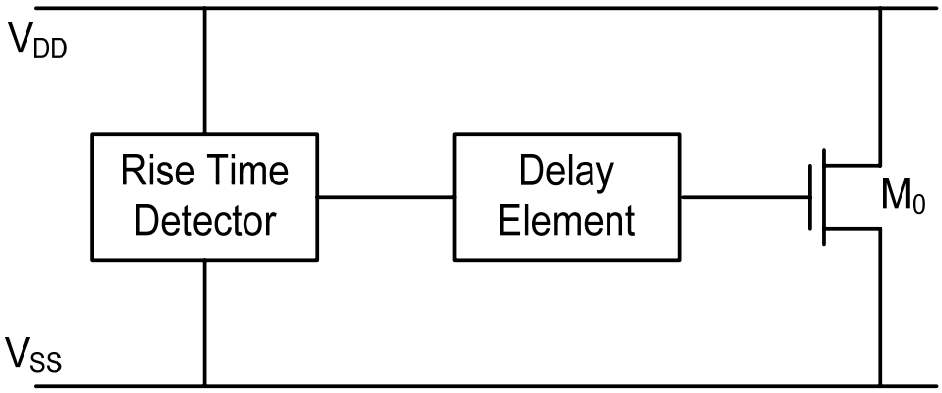


*Figure 3-6: Transient clamp architecture to avoid false triggering*

The main challenge in this clamp is to design a delay element that allows the complete discharge of the ESD event. Therefore, the delay must be designed to be at least 1μs. If the clamp turns off before the ESD energy is discharged completely, due to the very low leakage of the clamp, the residue charge causes an increase in the voltage of the $V_{DD}$ node. It has been reported that this voltage can prevent the clamp from turning on and cause unexpected failure [48].

## 3.4 State of the Art Transient Clamps

### 3.4.1 Boosted Rail Clamp with Dual Time Constant Trigger Circuit

As mentioned earlier, in order to avoid false triggering, the triggering circuit of the clamp should consist of a rise time detector and a delay element. In this method the delay element is based on a mono-stable circuit [40], [49]. Figure 3-7 shows the schematic of this clamp.

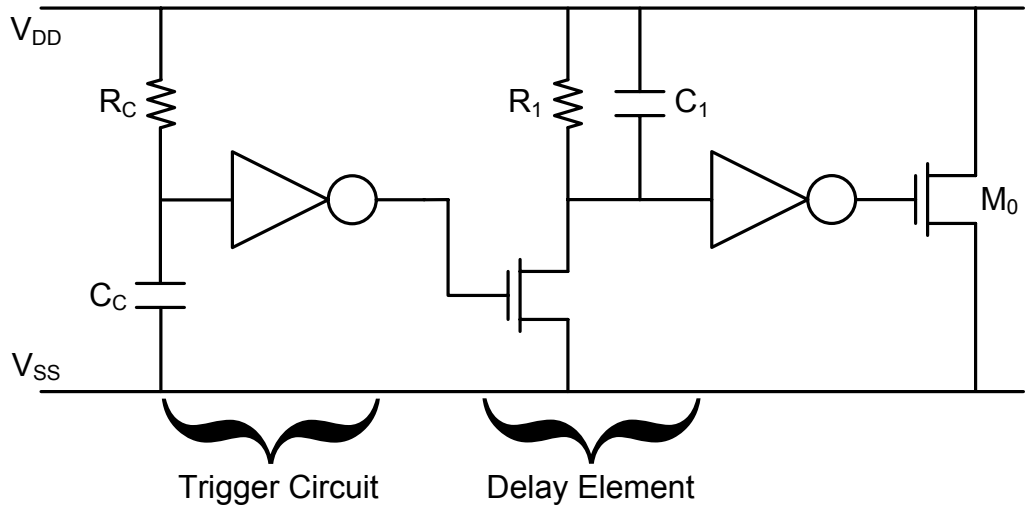


*Figure 3-7: Dual time constant trigger circuit*

In this clamp, $R_C$ and $C_C$ along with the first inverter are used to detect the rise time of the ESD event and hence, their time constant is set to 40ns. The delay element is based on a mono-stable latch. It has another time constant ($R_1C_1$) which is set to 600ns to keep the clamp "on" during the whole ESD event. In this configuration, $C_1$ is often provided by the capacitance of the last inverter which reduces the total area of the clamp.

The total area of the clamp can be further reduced by reducing the size of the main transistor $M_0$. The easiest way to reduce the size of a transistor, while having the same current capability, is to increase its gate-source voltage. To increase the gate voltage of $M_0$, a boosted supply bus using another diode network is added [49]. This method is explained with an example [7]. Consider that the requirement for ESD protection is to limit the pad voltage to 7V during a 3.8A ESD current in PS-mode. First consider the

standard non-snapback protection method. Under ESD conditions, when the pad voltage is limited to 7V, the gate voltage of NMOS is set to 3.9V and the required width of the transistor is 4080µm. Figure 3-8 shows non-snapback method along with the voltage of different nodes during a PS-mode ESD stress.

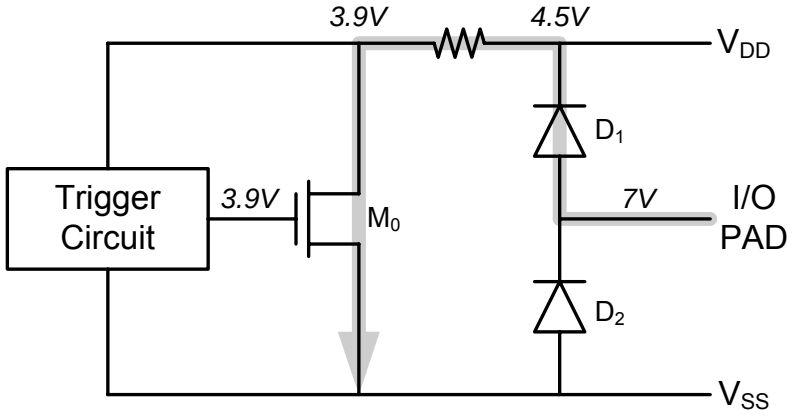


*Figure 3-8: Conventional non-snapback scheme under ESD conditions*

Note that, in Figure 3-8, as the ESD current is very high, the bus resistance, which is usually between 0.15Ω and 0.2Ω, is considered as well. It can be seen that the gate voltage of $M_0$ is 3.9V. In order to create a boosted supply bus, another diode ($D_3$) is added to the pad. Sizing of this diode is done in such a way that in an ESD event, the voltage of the boosted bus is higher than the voltage of the $V_{DD}$ bus. Figure 3-9 shows the boosted supply method along with the voltage of different nodes.

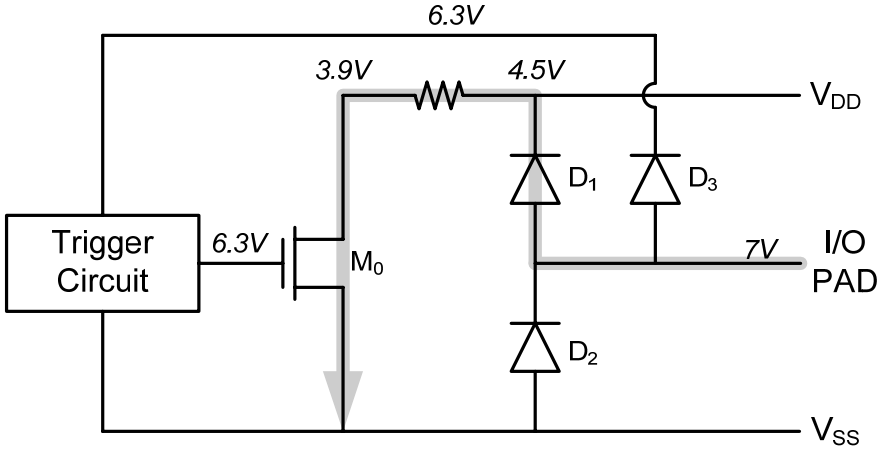


*Figure 3-9:Boosted rail clamp under ESD conditions*

It can be seen that using boosted rail clamp method, the gate voltage of $M_0$ is increased from 3.9V to 6.3V and therefore, the required width of the clamp transistor is reduced to 2220µm. This width is only 54% of the size of the required NMOS in the conventional method. Combining the techniques of Figure 3-7 and 3-9, the total area of the clamp is reduced significantly.

In [49], distributed rail clamp method has been applied to boosted supply bus method. The circuit was optimized in order to limit the pad voltage to 7V in 3.8A ESD zap. A comparison between the two methods is done in Table 3-1.

*Table 3-1: Comparing the clamp size of the distributed clamp with boosted-distributed clamp*

| | Large Clamp NMOS Width | Small Clamp NMOS Width |
|---|---|---|
| Distributed rail clamp | 4080µm | 714µm |
| Distributed rail clamp with boosted supply method | 2220µm | 301µm |

It has been reported that combining the distributed clamp idea with boosted rail clamp and dual time constant trigger circuit allows a compact protection scheme with false triggering immunity [49].

### 3.4.2 MOS Transient Clamp with Feedback Enhanced Triggering

Based on the earlier discussions, one of the major bottlenecks in the design of transient clamps is to design an optimum delay element that keeps the clamp "on" during the whole ESD stress. In addition to using another RC time constant to create the required delay, a feedback circuit can be used to implement the delay element as well. Figure 3-10 shows the schematic of a transient clamp where the delay element is based on an SRAM cell [50].

As an ESD event occurs at the $V_{DD}$ line, the voltage of node 1 rises rapidly. As a result the voltage of node 2 goes towards $V_{SS}$, while the voltage of node 3 goes towards

$V_{DD}$. At the same time, Inv3 discharges node 2 further towards $V_{SS}$. Therefore, as a result of this latch mechanism, node 2 is discharged to $V_{SS}$ and node 3 is charged to $V_{DD}$, keeping $M_0$ on during the ESD event. Simulation results show that using this method $M_0$ is "on" for 700ns [50].

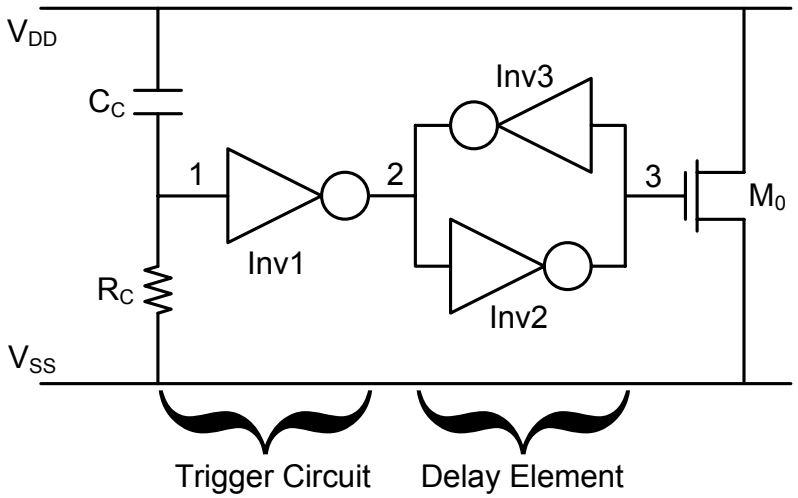


*Figure 3-10: SRAM based transient clamp*

Furthermore, it has been reported that this clamp is immune to false triggering as well. Simulation results show that during a very fast power-up with rise time of 1μs the voltage of node 3 is raised to 0.1V and goes back to 0 within 500ns. Hence, this clamp doesn't trigger during power-up and is immune to false triggering. Moreover, this clamp is reported to be immune to power supply noise as well.

## 3.5 Oscillation in Transient Clamps

As mentioned earlier, transient clamps suffer from large area and false triggering. Another concern about transient clamps that has been addressed recently is the possibility of oscillation during power-up and/or ESD conditions [47]. This issue has been observed as a high frequency oscillation on the power rails. To understand the nature of these oscillations, consider the inverter-based clamp shown in Figure 3-3. Under ESD conditions the voltage of the $V_{DD}$ line increases suddenly. Due to the capacitor $C_C$, this jump is transferred to the node 1 as well. Going through four inverters, the gate voltage of

the main transistor increases and turns on $M_0$. As the ESD energy starts to decay, the voltage of the $V_{DD}$ line starts to decrease. The voltage of the node 1 decreases with a slower rate due to the high RC constant. As the voltage of node 1 reaches the triggering voltage of the first inverter (beginning of oscillation in Figure 3-11), the inverter chain turns off $M_0$. Hence, the voltage of the $V_{DD}$ line increases, which increases the voltage of the node 1 as well. If the RC time constant is high enough, the voltage increase in node 1 turns on the inverter again. This process is observed as an oscillation on the $V_{DD}$ line as shown in Figure 3-11. In other words, as the voltage of nodes $V_{DD}$ and 1 reduces, at certain supply and node 1 voltage condition, inverters act as small signal amplifiers. As a result, for a given frequency, the total phase shift of the loop satisfies the criterion for oscillation. The time at which the oscillation starts is a function of $R_CC_C$ time constant and inverter chain delay. In Figure 3-11, as the turn on time of the clamp was less than duration of the ESD event, voltage of the $V_{DD}$ node increases after the oscillation.

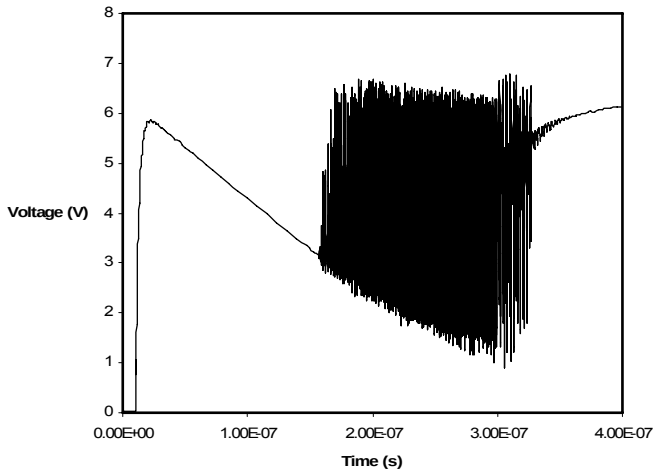


*Figure 3-11: The voltage of the $V_{DD}$ node of an inverter-based clamp during 2kV ESD stress*

Similar phenomenon happens during power-up as well. In this case, as the voltage of the power line increases from zero to $V_{DD}$ (with a much slower rate than the ESD event), the voltage of node 1 increases as well. Due to the high RC delay time, the voltage difference between nodes 1 and $V_{DD}$ starts to increase. Therefore, after a while, the voltage of node 1 will be below the triggering voltage of the inverter and the clamp will turn off. As a result, the voltage of the $V_{DD}$ line increases, which increases the voltage of the node 1. This rapid change in the voltage of the $V_{DD}$ line creates oscillation on the

power line. Figure 3-12 shows the oscillation in an inverter-based clamp for a 3μs rise time power-up condition.

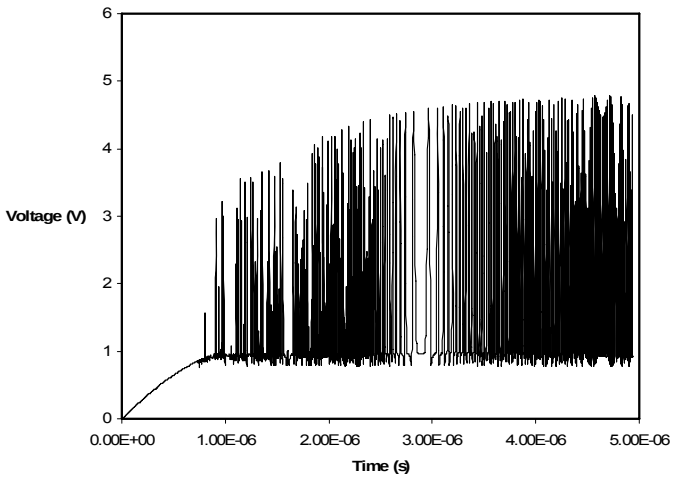


*Figure 3-12: The voltage of the $V_{DD}$ node of an inverter-based clamp during power-up*

The frequency and existence of this oscillation is a function of the rise time of power-up as well as the load of the power line. Unlike the oscillations under ESD conditions, the oscillations under normal power-up can cause serious issues in normal operating conditions of the main circuit and should be avoided.

In order to investigate the possibility of oscillation in different clamps, we propose a quantitative analysis of their stability. Referring back to the oscillation theory, the condition of oscillation is based on the open loop gain of the clamp [51]. The loop is unstable when the magnitude of the open loop gain is 1 and the phase of the open loop gain is 180º. In transient clamps the loop is closed through the power supply rail. Due to the logic of the transient clamps, an odd number of inversions (including the $R_C$-$C_C$ network) exist in the loop. Hence, the condition of 180º phase is satisfied and in order to stabilize the loop, the magnitude of the open loop gain should be kept below 1.

### 3.5.1 Analyzing the stability of the inverter-based clamp

In order to simulate the open loop gain of the inverter-based clamp, the feedback loop is opened at node 1 and the impedance seen from each side is added to the other side.

Figure 3-13 shows the setup used to simulate the open loop gain of the inverter-based clamp.

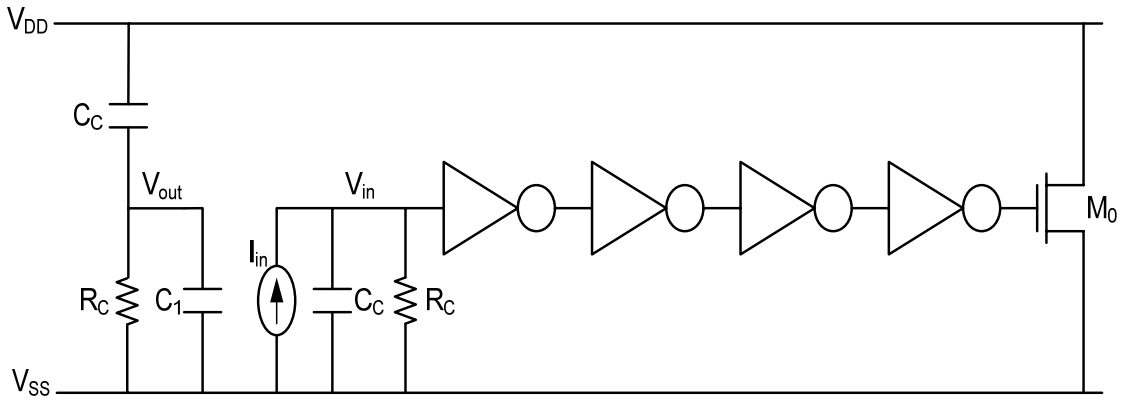


*Figure 3-13: Setup used to simulate the open loop gain of the inverter-based clamp*

In this figure, $C_1$ is the input capacitance of the first inverter and the loop gain is defined as $V_{out}/V_{in}$. By running an AC simulation in Cadence, the magnitude and phase of the loop gain is evaluated. Figure 3-14 shows the magnitude and phase of the open loop gain.

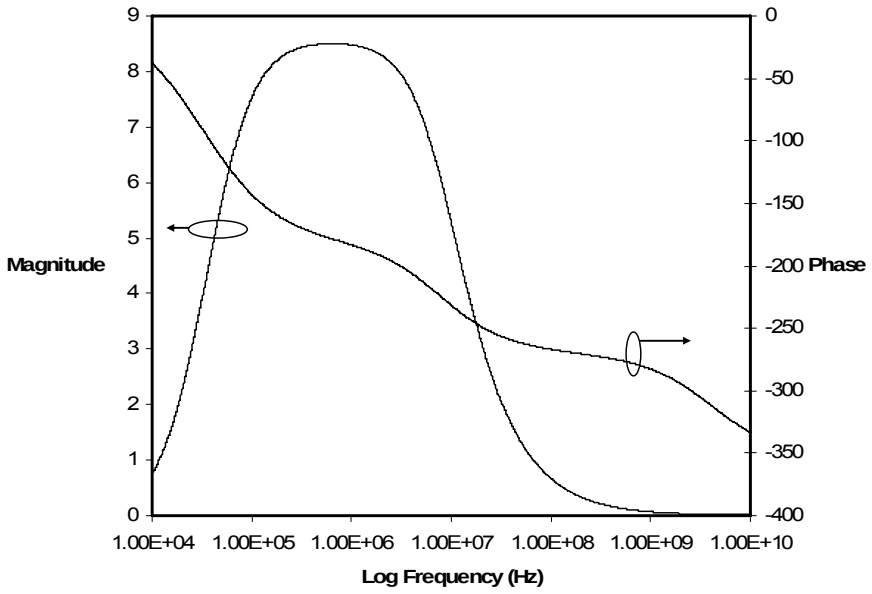


*Figure 3-14: Magnitude and phase of the open loop gain of the inverter-based clamp*

It can be seen that for the inverter-based clamp a possibility of oscillation exists where the magnitude and phase of the loop gain are 8.49 and -180º respectively. This

simulation result confirms that a possibility of oscillation exists in the inverter-based clamp.

### 3.5.2 Analyzing the stability of the dual time constant clamp

Similar to the inverter-based clamp, for the dual time constant clamp shown in Figure 3-7 the loop is opened from node 1 and the impedance of each side is added to other side. Again the loop gain is defined as $V_{out}/V_{in}$, which should be lower than 1 to ensure stability. Figure 3-15 shows the magnitude of the open loop gain of the dual time constant clamp. It can be seen that the peak of the magnitude of the loop gain is 2, which reveals a possibility of oscillation.

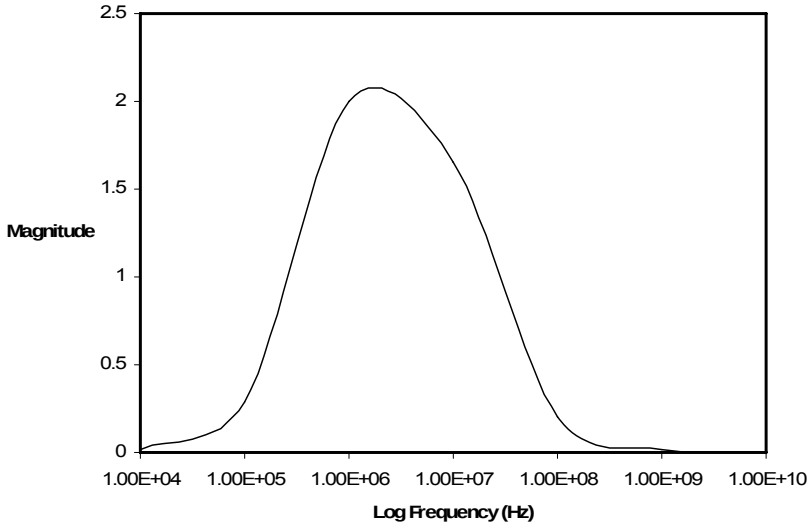


*Figure 3-15: Magnitude of the open loop gain of the dual time constant clamp*

### 3.5.3 Analyzing the stability of the SRAM-based clamp

Finally, the stability of the SRAM-based clamp, shown in Figure 3-10, is simulated. The loop is opened from node 1 and the loop gain is defined as $V_{out}/V_{in}$. Figure 3-16 shows the magnitude of the open loop gain of the SRAM-based clamp.

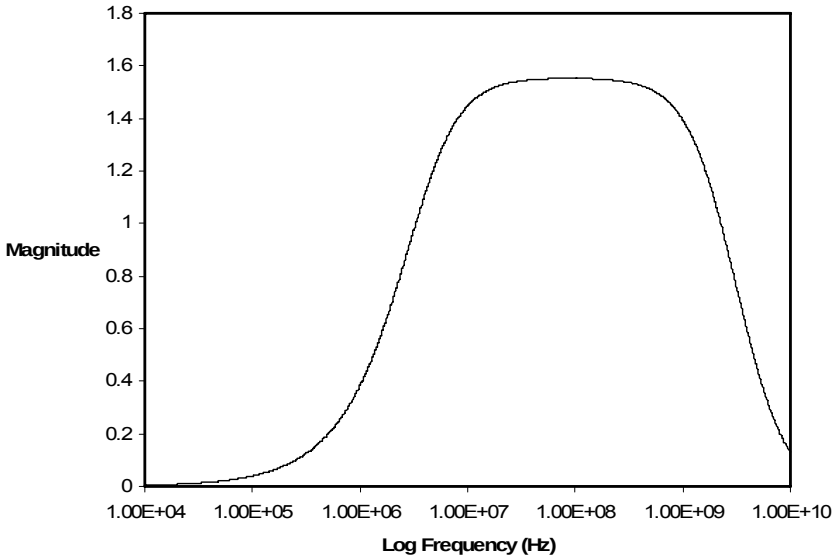


*Figure 3-16: Magnitude of the open loop gain of the SRAM-based clamp*

It can be seen that the magnitude of the open loop gain is 1.6. Hence, there is a possibility of oscillation in this clamp as well.

## 3.6 Thyristor-Based Clamp

As mentioned earlier, the challenge in the design of transient clamps is to implement an optimum delay element to keep the main transistor "on" during the whole ESD event. Hence, a novel ESD clamp circuit is proposed where a CMOS thyristor circuit is used as the delay element. It has been shown that the CMOS thyristor can generate a delay from a few nanoseconds to millisecond range with low sensitivity to environmental conditions and low static power consumption [52]. Figure 3-17 shows the new clamp with CMOS thyristor delay element. The resistor $R_1$ is added to turn off the main clamp transistor $M_0$ under normal operating conditions. Under normal operating conditions the capacitor $C_C$ is fully charged and the voltage of node 1 is '0'. As a result, the voltage of node 2 is '1', which makes $M_4$ off. The resistor $R_1$ pulls the voltage of node 3 to '0' turning off the thyristor delay element. Hence, the transistor $M_0$ is off under normal operating conditions.

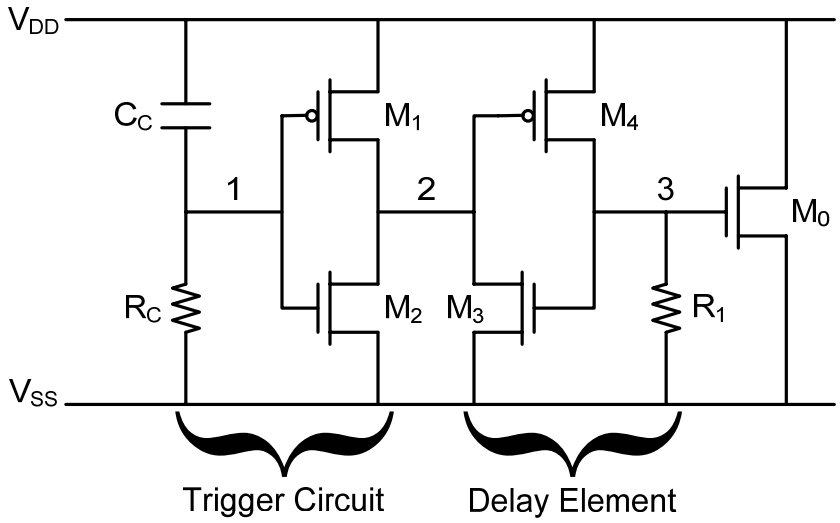


*Figure 3-17: Thyristor-based transient clamp*

In the thyristor-based clamp, when an ESD event occurs, the voltage of node 1 becomes '1' and the voltage of node 2 becomes '0'. As a result, both transistors of the delay element turn on, pulling the voltage of node 3 to '1' and turning on the clamp. At this point the current going through $M_3$ is sub-threshold current only. Due to the low $R_CC_C$ time constant, the voltage of node 1 starts to decrease very quickly. Therefore, transistor $M_1$ turns on trying to pull up V(2). At the same time $M_3$ is trying to pull down V(2). Based on the sizing of the two transistors, V(2) charges with a delay towards '1'. After $M_4$ turns off, the positive feedback of the thyristor structure turns off $M_3$ as well. Therefore, V(3) is pulled to '0' via the resistor $R_1$.

The delay of this clamp can be estimated as well. The delay is defined as the time transistor $M_0$ is "on". Hence, $V(3)=V_{Tn}$ is the condition used to calculate the delay of the clamp. When an ESD event occurs, voltage of node 1 becomes '1', turning on $M_0$. At this point, both transistors $M_3$ and $M_4$ are in triode region. Due to low $R_CC_C$ time constant V(1) becomes '0' very quickly turning on $M_1$. At this point, and during the delay time of the thyristor, $M_1$ is in saturation while $M_3$ and $M_4$ are in triode. However, towards the end of the delay, when $M_0$ is about to turn off, transistor $M_4$ goes into saturation region. Hence, the currents flowing through transistors $M_1$, $M_3$ and $M_4$ are as follows.

$$\frac{k_p}{2}\left(\frac{W}{L}\right)_1\left(V_{DD}-V(1)-V_{Tp}\right)^2=k_n\left(\frac{W}{L}\right)_3\left[V(2)\left(V(3)-V_{Tn}\right)-\frac{V(2)^2}{2}\right] \quad (3\text{-}1)$$

$$\frac{k_p}{2}\left(\frac{W}{L}\right)_4\left(V_{DD}-V(2)-V_{Tp}\right)^2=\frac{V(3)}{R_1} \quad (3\text{-}2)$$

As $M_3$ is in triode region and voltage of node 2 is very small, to simplify the equations, we assume that V(2) is much smaller than $V_{DD}$. As mentioned earlier, the condition to calculate the delay is $V(3)=V_{Tn}$. Hence, from equation (3-2) the voltage of the $V_{DD}$ node at the end of the delay period can be calculated from the following equation.

$$\frac{k_p}{2}\left(\frac{W}{L}\right)_4\left(V_{DD}-V_{Tp}\right)^2=\frac{V_{Tn}}{R_1} \quad (3\text{-}3)$$

$$V_{DD}=\sqrt{\frac{2V_{Tn}}{R_1 k_p\left(W/L\right)_4}}+V_{Tp} \quad (3\text{-}4)$$

In 0.18μm technology, $k_p$=90.3μA/V$^2$, $k_n$=380μA/V$^2$, $V_{Tn}$=0.42V and $V_{Tp}$=0.5V. In the clamp, $R_1$=1kΩ while transistors $M_3$ and $M_4$ are designed 10μm wide with minimum length. By substituting these values into equation (3-4), voltage of the $V_{DD}$ node at the end of the delay period becomes 0.9V.

In order to find the delay time, the time at which $V_{DD}$=0.9V should be calculated. Hence, the time constant of the discharge of the ESD energy should be calculated. In other words, the total resistance seen by $C_{ESD}$=100pF (for HBM model) should be calculated. Based on linear approximation of the circuit, the time constant approximately equals to:

$$\tau=C_{ESD}\left[R_{ESD}+\left(1/g_{m1}\right)\|\left(r_{ds4}+R_1\right)\|r_{ds0}\right] \quad (3\text{-}5)$$

, where $R_{ESD}$=1.5kΩ and models the HBM resistance. In this equation $r_{ds}$ of $M_0$ and $M_4$ can be ignored and again ignoring the non-linearity in the value of $g_{m1}$, total time constant becomes 350ns.

Finally, in order to be able to calculate the delay, the initial value of $V_{DD}$ at the beginning of the ESD event should be calculated as well. When an ESD event occurs, the voltage across $C_{ESD}$ jumps to 2kV. As a result, the voltage of the $V_{DD}$ node jumps by a

value called $V_D$. Due to capacitive coupling, V(3) should see a sudden increase of approximately $V_D$ as well. As the peak ESD current for 2kV stress is 1.33A [53] and is flowing mainly through the 400μm wide $M_0$, using circuit level simulation, the required gate voltage for $M_0$ (which equals to $V_D$) is calculated to be 6V.

The above results are summarized in the following equations:

$$V_{DD} = V_D e^{-t/\tau} \tag{3-6}$$

$$\tau = 350\,\text{ns}, \; V_D = 6\text{V}$$

$$V_{DD} = 0.9\text{V} \quad \Rightarrow \quad t = \text{delay}$$

Based on the above equations, delay of the clamp is estimated to be 700ns. It should be noted that due to high current and non-linear behavior of the clamp under ESD conditions, we are expecting to have some error in our delay calculation.

In order to evaluate the thyristor-based clamp, the circuit shown in Figure 3-17 is simulated under various conditions. The ESD response of the clamp is simulated using both circuit level and device level simulators for a 2kV HBM ESD stress. In the next step the immunity to false triggering and power supply noise is investigated with the circuit level simulator. Finally, using the method presented in section 3.6, the stability of this clamp is examined.

### 3.6.1 ESD operation

As HBM is the most common test method, the proposed clamp is simulated for a 2kV HBM stress. The HBM test is defined in the MIL-STD-883 standard (method 3015.7) [53]. In this standard the HBM waveform has a rise time of less than 10ns and a delay time of 120-180ns. For a 2kV ESD stress the peak current is 1.33A±10%. The transient current waveform used in our simulations is shown in Figure 3-18.

As mentioned earlier, one of the main advantages of transient clamps is the possibility to use circuit-level simulators to simulate their ESD behavior. The ESD stress shown in Figure 3-18 is applied to the $V_{DD}$ line of the clamp with grounded $V_{SS}$. The clamp is simulated in 0.18μm TSMC CMOS technology with $t_{ox}$=41Å. All transistors are low threshold devices with minimum length. The width of the main discharging transistor

($M_0$) is set to 400µm, which is realized in a 40 finger configuration. The transistors of the thyristor delay element are 10µm wide each. Figure 3-19 shows the voltage of different nodes under ESD conditions.

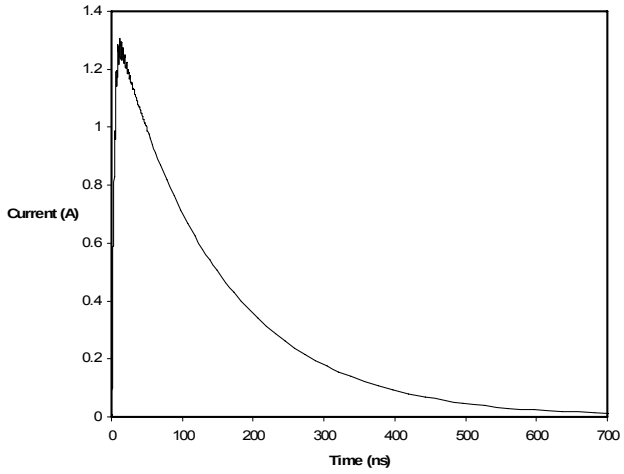


*Figure 3-18: 2kV HBM ESD current waveform*

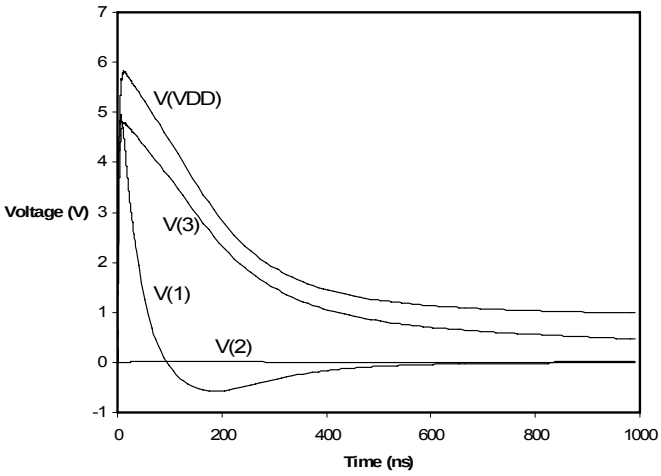


*Figure 3-19: Simulating the thyristor-based clamp under 2kV HBM stress*

It can be seen that at the ESD event, the voltage of node 1 rises to 5V and goes back towards zero very quickly. However, the voltage of node 3 remains high for a much longer time to discharge the complete ESD stress. Based on the response shown in Figure 3-19, the delay element keeps the clamp on for over 1µs. Our calculations in the previous section predict 700ns delay. The difference is due to nonlinear behavior of transistors under ESD conditions. The peak voltage of the $V_{DD}$ node is a function of the width of the

main transistor. In our design, the voltage of the $V_{DD}$ node is kept below 5.8V during the 2kV stress.

Although transient ESD clamps can be simulated with circuit-level simulators, their high current behavior and self-heating effect require a device-level simulation. For this clamp we did the device-level simulation with Sequoia. The transistor structures in the ESD clamp are designed using process parameters of the 0.18μm silicided TSMC CMOS technology. The physical structure of the ESD device used in our simulations is shown in Figure 3-20. To run thermal simulations, a thermal electrode is placed at the bottom of the substrate and the temperature of this electrode is assumed to be the same as the ambient temperature (300K). All contacts are ideal ohmic electrodes. As mentioned in the first chapter, in order to verify the reliability of the transistors, their maximum temperature should be less than the melting point of metallization (660 ºC for aluminum based metallization and 1034 ºC for copper based metallization), and the melting point of silicon (1412 ºC) [54].

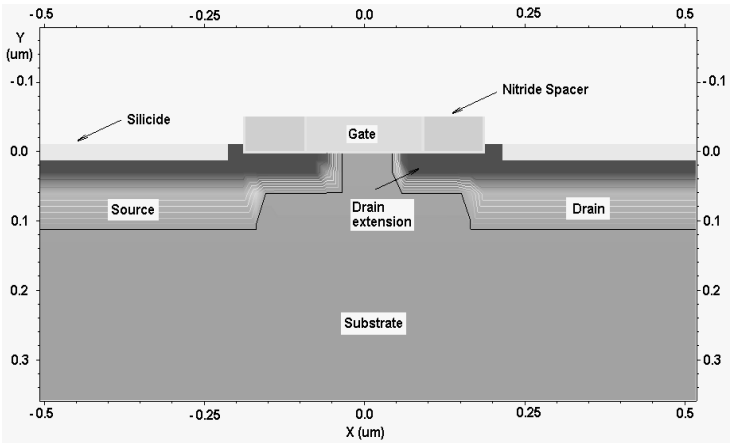


*Figure 3-20: Cross section of the 0.18μm NMOS transistor*

Similar to the circuit level simulation, the 2kV HBM stress is applied to the $V_{DD}$ line of the thyristor-based clamp in the device-simulator, while $V_{SS}$ line is grounded. To test the failure of the clamp, the maximum temperature of all transistors is monitored. The peak temperature during this stress is in the main transistor $M_0$ and the hot spot is in the drain/gate boundary. Figure 3-21 shows the cross section of $M_0$ with its temperature distribution and Figure 3-22 shows the maximum temperature of $M_0$ during the 2kV HBM stress.

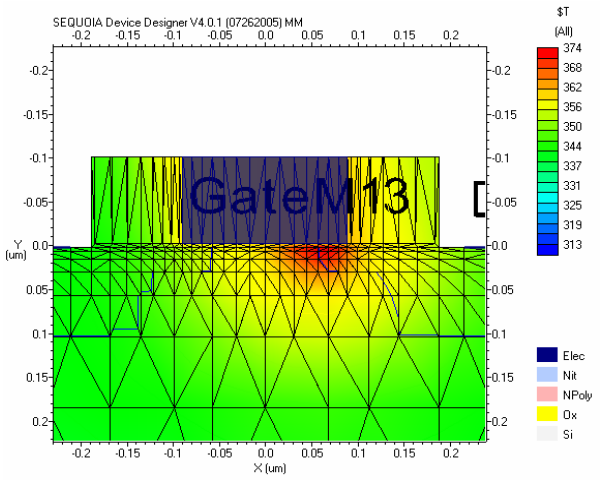


*Figure 3-21: Temperature distribution in $M_0$ showing the maximum temperature during 2kV stress*

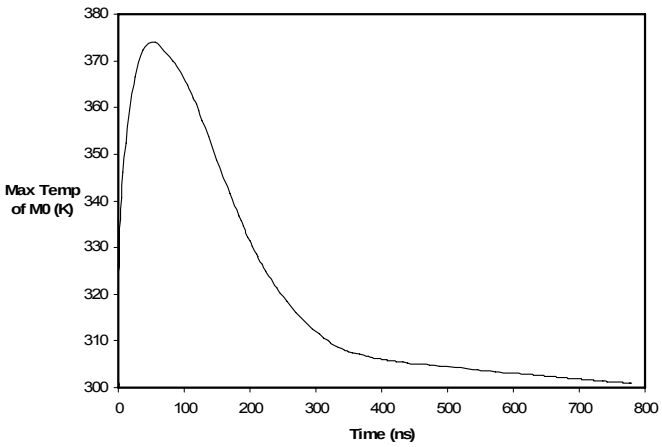


*Figure 3-22: Maximum temperature of the clamp during 2kV HBM stress*

It can be seen that the maximum temperature of this clamp is less than 400K which is less than the melting point of metallization and silicon. Hence, this clamp passes the 2kV HBM stress. The delay of the thyristor circuit can be verified with the device simulator as well. Figure 3-23 shows the voltage of the $V_{DD}$ node under this stress.

Comparing the simulation results from Cadence (Figure 3-19) with Sequoia (Figure 3-23) shows that the device simulator is predicting a lower peak voltage under ESD conditions. This difference is because of the impact ionization effect, which is becoming significant in high current mode. In circuit simulators, such as Cadence, the impact of the parasitic bipolar transistor of $M_0$ is neglected. Therefore, the current flow through the protection device is underestimated [55]. However, it can be seen that similar to Cadence results, the clamp is "on" for over 1μs.

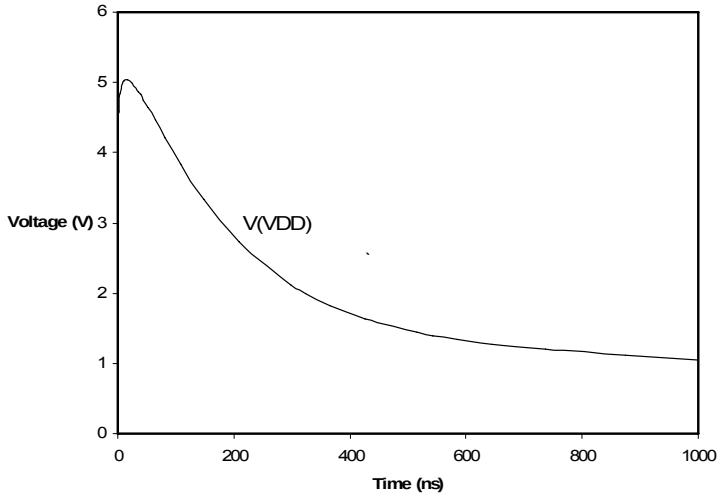


*Figure 3-23: The voltage of the $V_{DD}$ line under 2kV stress using Sequoia*

### 3.6.2 Normal conditions

In addition to the ESD response, the new clamp should be tested under normal operating conditions as well. The first experiment is the total current of the clamp under normal operating conditions. Circuit level simulations show that under normal operating conditions the transistor $M_0$ is off and the total current of the clamp is 8.5nA for 1.8V supply voltage.

The next experiment is to test the immunity of the clamp to false triggering. The immunity to false triggering is evaluated by applying a ramp from 0 to $V_{DD}$ with different rise times. In regular applications, power-up is a very slow event where the rise time is in millisecond range. Hence, considering the small RC time constant of the triggering circuit, the clamp is immune to false triggering. However, in some applications such as hot plug operations the rise time can be as low as 1μs that may cause false triggering. Hence, to test the worst case, the new clamp is simulated for a 1μs power-up. In order to avoid false triggering the gate voltage of $M_0$ (node 3) should be less than its threshold voltage (≈0.45V). Figure 3-24 shows the voltage of different nodes for a 1μs power-up. It can be seen that the voltage of node 1 increases up to 70mV only, while the voltage of node 3 is almost zero all the time. Hence, even a very fast power-up (1μs) does not trigger the clamp and this design is immune to false triggering.

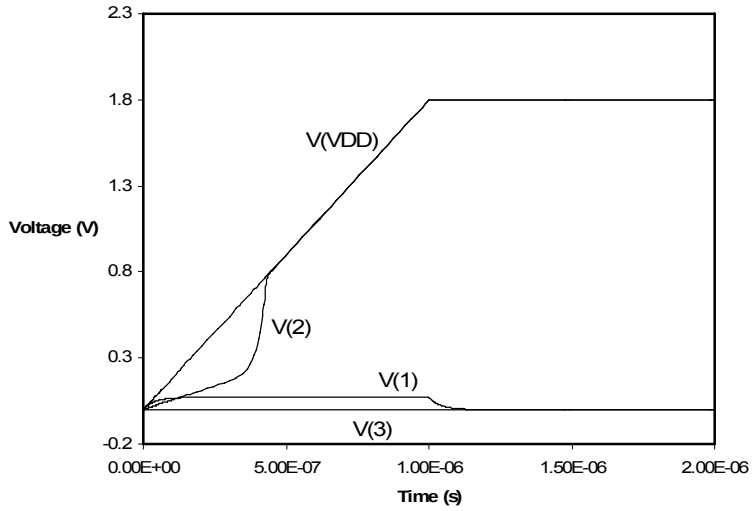


*Figure 3-24: Simulating the thyristor-based clamp under 1μs power up conditions*

In addition to false triggering, especially in circuits with high switching rates, power supply noise is becoming an important factor in transient clamps as well [50]. In order to simulate the impact of power supply noise on the clamp, a pseudo-random pulse is added to the supply voltage. The additional noise has a rate of 500Mbps and an amplitude of $600mV_{p\text{-}p}$. The immunity to power supply noise is evaluated by monitoring the gate voltage of $M_0$ (node 3) and the current of $M_0$. Figure 3-25 shows the voltage of nodes $V_{DD}$ and 3 and Figure 3-26 shows the current of the transistor $M_0$.

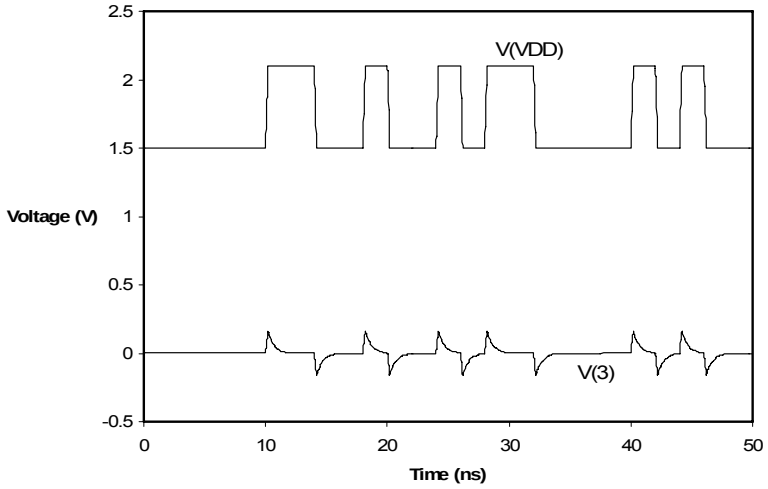


*Figure 3-25: Power supply noise immunity: the voltage of nodes $V_{DD}$ and 1*

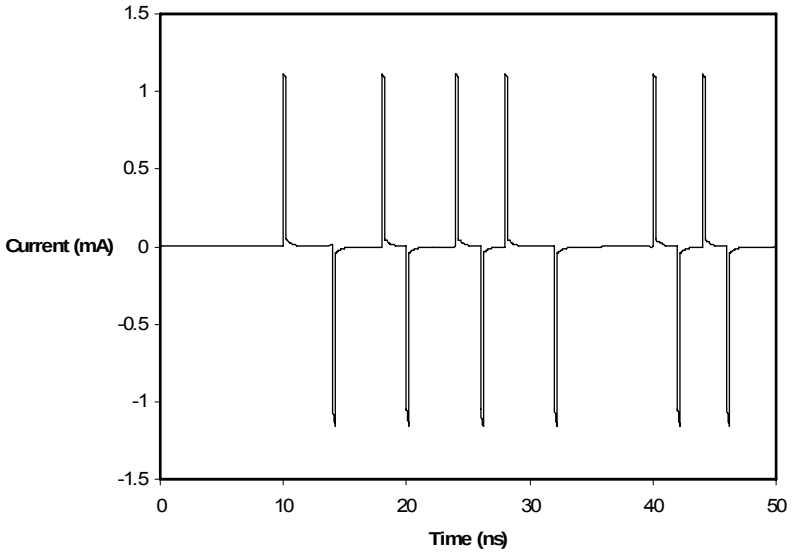


*Figure 3-26: Power supply noise immunity: the current of $M_0$*

It can be seen that the peak current of the clamp is approximately 1mA which is very small considering the amplitude of the noise on the supply line [50]. Hence, the new clamp is immune to power supply noise.

### 3.6.3 Immunity to oscillation

In order to test the stability of the thyristor based clamp, similar to the method explained in section 3-6, the loop is opened from node 1. Then the impedance seen from each side is added to the other side. The magnitude of the loop gain $V_{out}/V_{in}$ should be less than 1 to ensure stability. Figure 3-27 shows the magnitude and phase of the loop gain. It can be seen that in this clamp, the magnitude of the loop gain is always less than 1. Therefore, this clamp is immune to oscillation.

Furthermore, different clamps can be compared based on their stability. Therefore, the clamps with smaller loop gain are more stable. Based on this comparison, knowing that the loop gain of the inverter-based clamp is 8.5, SRAM-based is 1.6 and dual trigger clamp is 2, the new thyristor-based clamp offers the best stability.

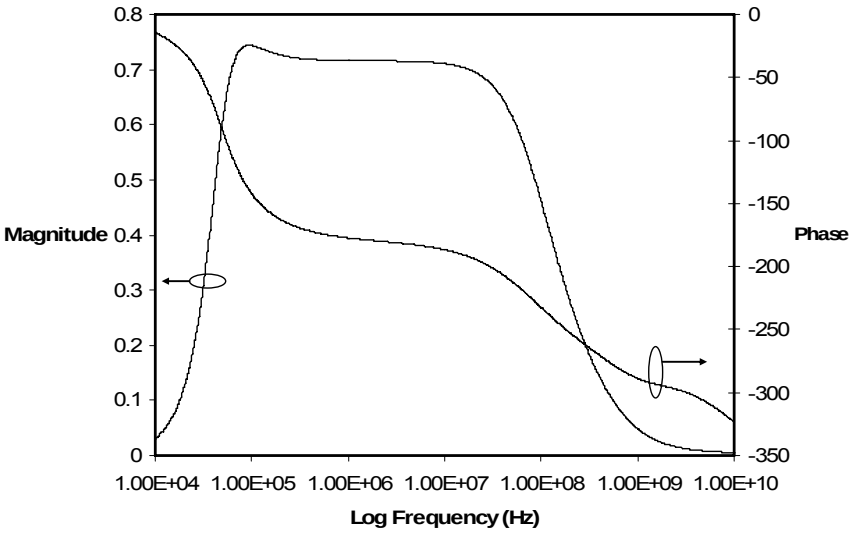


*Figure 3-27: Magnitude and phase of the loop gain of the thyristor-based clamp*

### 3.6.4 Measurement results

The proposed thyristor-based clamp has been fabricated in 0.18μm TSMC CMOS technology. In this clamp $R_C$ and $C_C$ were set to 500fF and 80kΩ respectively to detect the rise time of the ESD event. $M_0$ was 400μm wide realized with 20 fingers and the total design was 50μm×60μm. Figure 3-28 shows the layout of the proposed clamp.

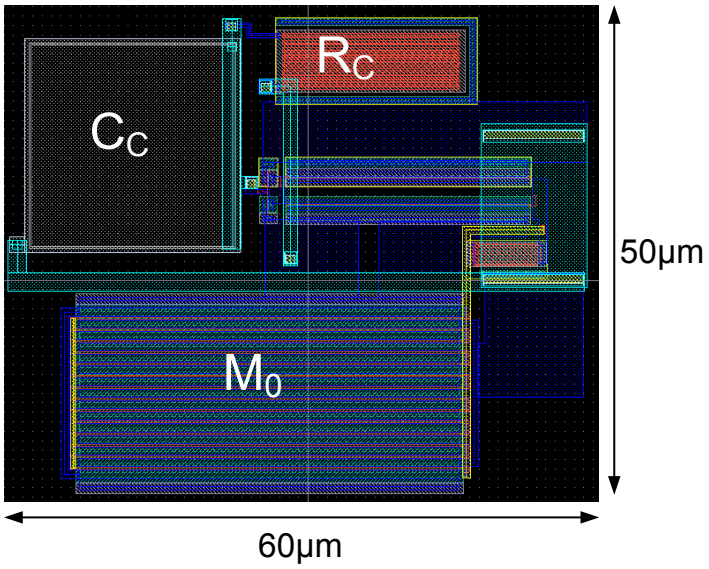


*Figure 3-28: Layout of the thyristor-based clamp*

To test this clamp, we did both TLP and HBM measurements on the test chip. TLP measurements have been done using the Pulsar 900 TLP system from SQP products. Figure 3-29 shows the TLP measurement results for this clamp using 100ns wide pulses with 10ns rise time. It can be seen that the leakage current at $V_{DD}$=1.8V is 7nA. The second breakdown current is determined by the current at which a significant increase in leakage is observed. Hence, the second breakdown current of this clamp is 1.8A.

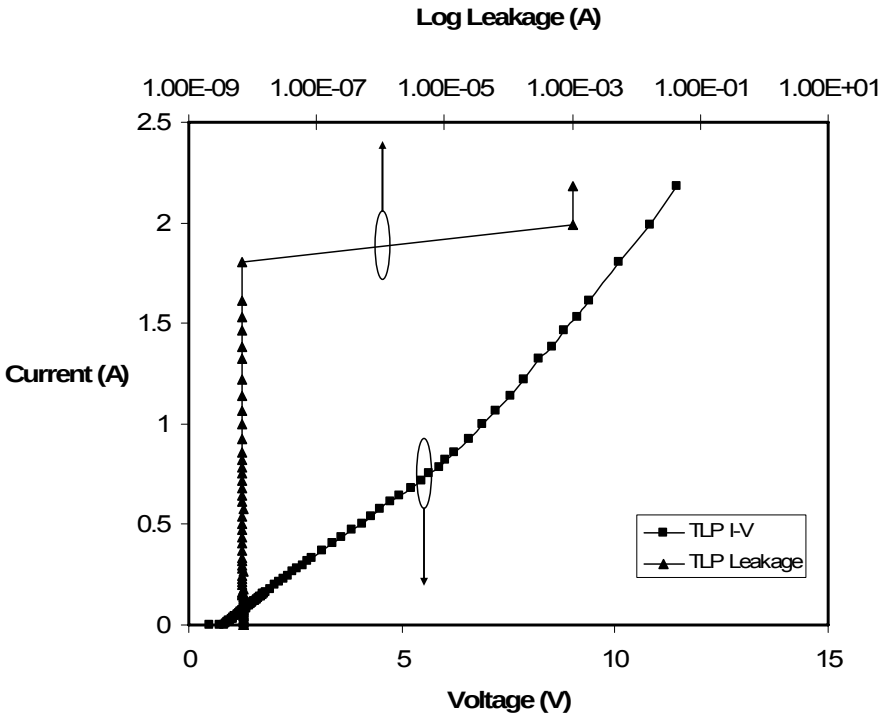


*Figure 3-29: TLP measurement results for the thyristor-based clamp*

Furthermore, HBM test has been done on the clamp as well. This measurement was done using IMCS-700 HBM/MM ESD tester. We applied both positive and negative HBM stresses with 500V step sizes. This clamp passes both +3kV and -3kV stresses. But when we increased the stress to 3.5kV, it passes +3.5kV stress while it fails -3.5kV stress. These results are confirmed using the device simulator as well. For 3kV input stress, the peak temperature of the transistors exceeds 500k, while for 4kV the peak temperature was over 1000K. Hence, this clamp should pass 3kV but fail at 4kV HBM stress.

## 3.7 Flip-Flop Based Transient Clamp

As the goal in the design of transient clamps is to increase the delay of the delay element, in this design a rising edge triggered D-type flip-flop is used to create a delay element that can keep $M_0$ in "on" state for theoretically infinite time. Figure 3-30 shows the block diagram of this clamp.

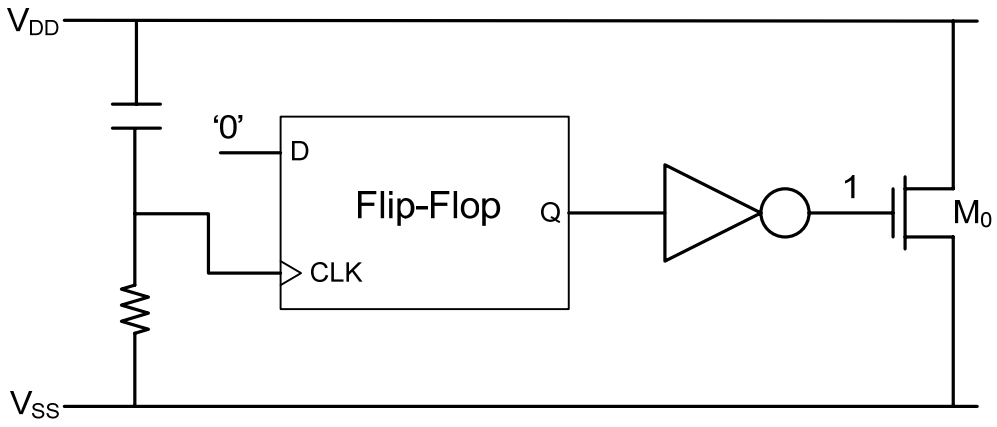


*Figure 3-30: A transient clamp with a flip-flop as the delay element*

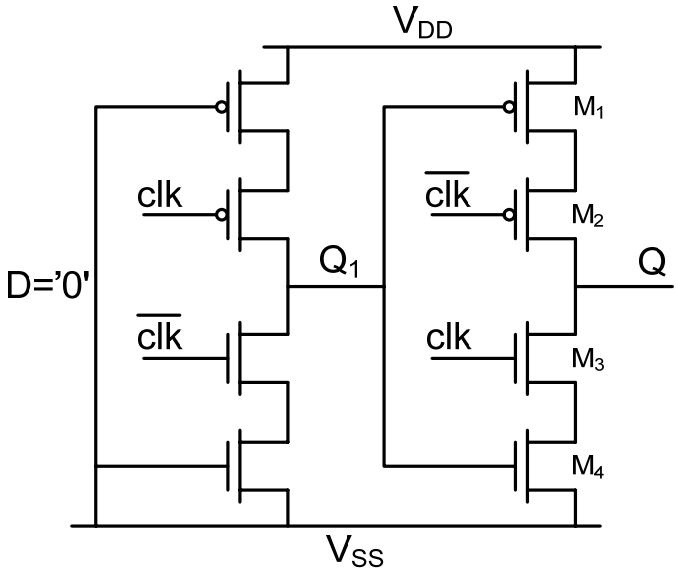


*Figure 3-31: Schematic of the flip-flop with grounded input*

When an ESD event occurs, a rising edge is detected at the clock input of the flip flop. Therefore, as the input D of the flip-flop is connected to ground, the output of the flip-flop becomes zero turning on $M_0$ through the inverter. This flip-flop holds its value until another rising edge is seen at the clock, which means that $M_0$ continues to conduct during the whole ESD event. Figure 3-31 shows the schematic of the D-type flip-flop with grounded input that is used in our research [56].

An obvious problem with this circuit is that it's impossible to turn off the clamp after it has been triggered. Therefore, the flip-flop should be modified to solve this problem. As the D-input of the flip-flop is always '0', $Q_1$ is '1' which turns on the $M_4$ transistor. Therefore, $M_4$ can be simply removed. In order to turn off the clamp in normal conditions, the gate of $M_2$ should be connected to clk. As a result, in normal conditions where $V_{DD}$ is connected to power supply and $C_C$ is fully charged, the voltage of clk is '0' and $M_2$ is turned on to help charge Q and turn off $M_0$. Considering these modifications the schematic of the new clamp is shown in Figure 3-32.

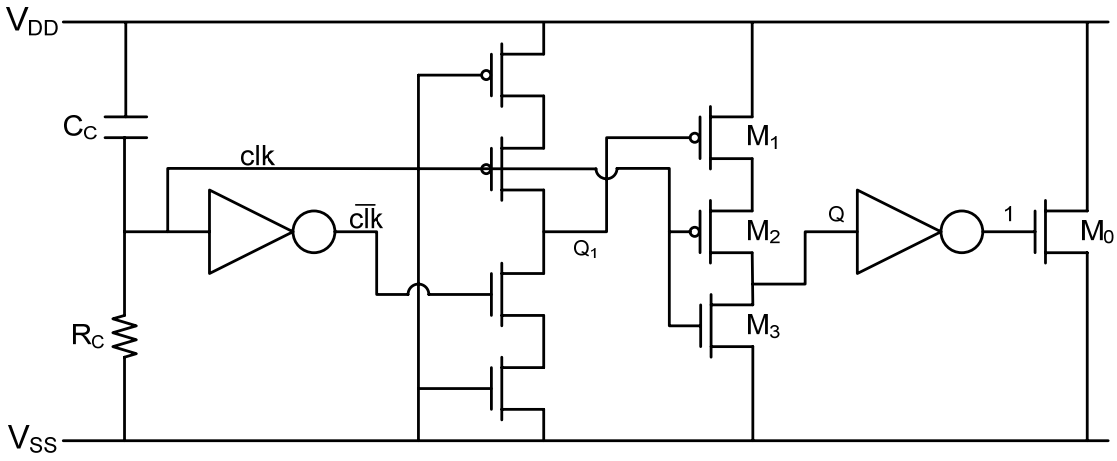


*Figure 3-32: Flip-flop triggered transient clamp*

In order to ensure proper operation, $M_1$ should be designed to be larger than $M_2$ and $M_3$ to be able to pull up the input of the inverter under normal operating conditions. In order to evaluate this clamp, similar to section 3.6, this clamp is tested under both ESD and normal operating conditions. At the end, immunity to oscillation and measurement results are presented for this clamp.

### 3.7.1 ESD operation

Similar to the thyristor-based clamp, in this section the response of the clamp shown in Figure 3-32 to a 2kV HBM stress is simulated. The simulations are done with both Cadence and Sequoia. The transistors are designed with minimum length in 0.l8µm TSMC CMOS technology. Figure 3-33 shows the voltage of different nodes of the clamp when the ESD stress is applied to the $V_{DD}$ node and $V_{SS}$ is grounded.

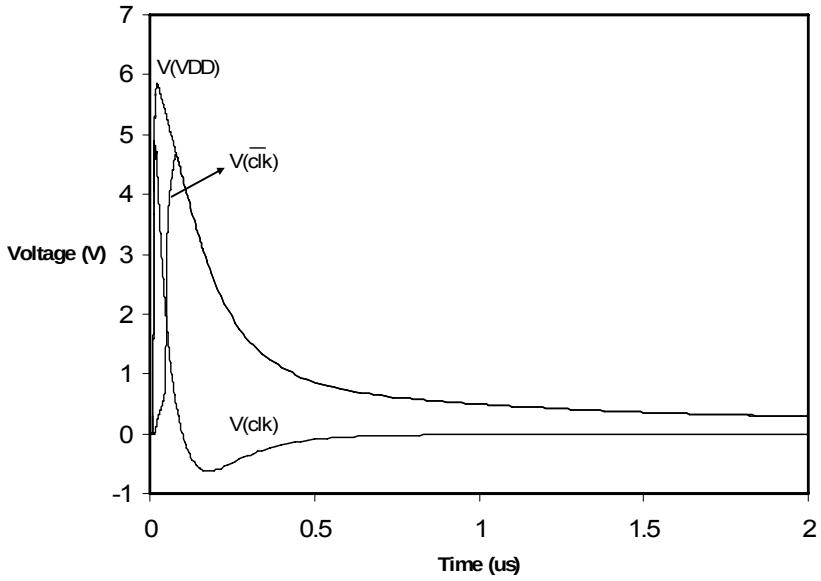


*Figure 3-33: Simulating the flip-flop based clamp under 2kV HBM stress*

Based on the voltage of the $V_{DD}$ node, it can be seen that the clamp is "on" for over 2µs and until the ESD event decays completely. The peak voltage of the supply line during the 2kV stress is 5.8V. Referring back to Figure 2-23, it can be seen that this voltage is low enough to provide ESD protection in 0.18µm CMOS technology.

In the next step, this clamp is simulated with the device simulator to check the thermal behavior of the transistors. In this simulation, similar transistors as those in section 3.6.1 are used. Again the maximum temperature is in the main transistor $M_0$ and the hot spot is in the drain/gate boundary. Figure 3-34 shows the maximum temperature of the clamp during the 2kV HBM ESD stress. It can be seen that the maximum

temperature is less than 400K which is less than the melting temperature of silicon and metalizations.

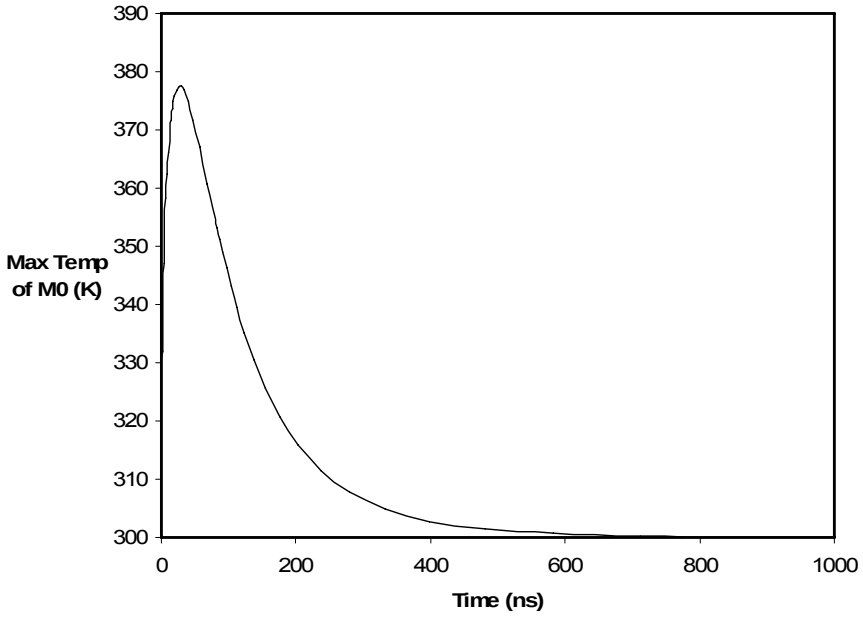


*Figure 3-34: Maximum temperature of the clamp during 2kV HBM stress*

Figure 3-35 shows the voltage of the $V_{DD}$ node during the 2kV stress. It can be seen that, similar to simulations in section 3.6.1, Sequoia predicts lower peak voltage compared to Cadence, which is due the impact ionization effect.

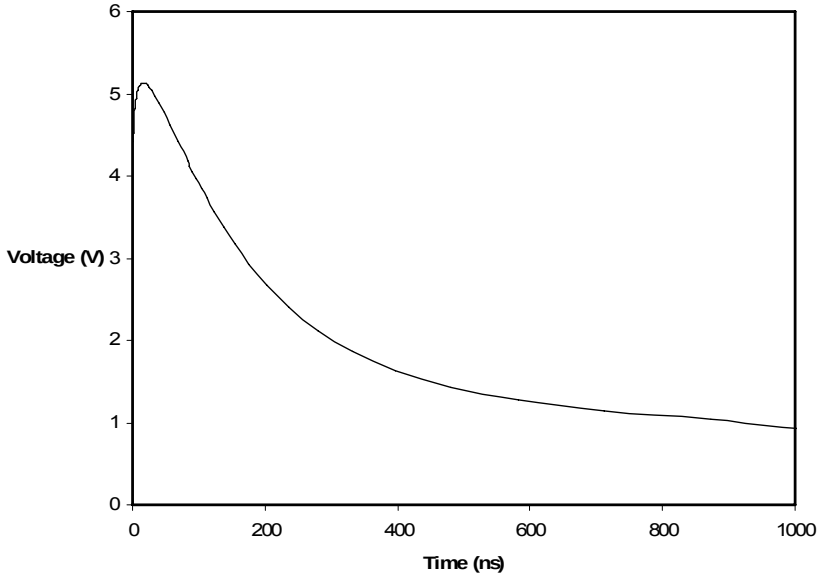


*Figure 3-35: The voltage of the $V_{DD}$ node under 2kV ESD stress using Sequoia*

### 3.7.2 Normal operation

In addition to ESD response, this clamp should be tested under normal operating conditions as well. As the first step, it should be ensured that the clamp is off during normal operating conditions. Cadence simulations show that under 1.8V supply voltage, the clamp is off and has a very low leakage of 8nA.

The next experiment is to test the immunity of the clamp to false triggering. Similar to the thyristor-based clamp, false triggering immunity is evaluated by ramping up the supply voltage in 1μs. Figure 3-36 shows the voltage of different nodes for a 1μs power-up.

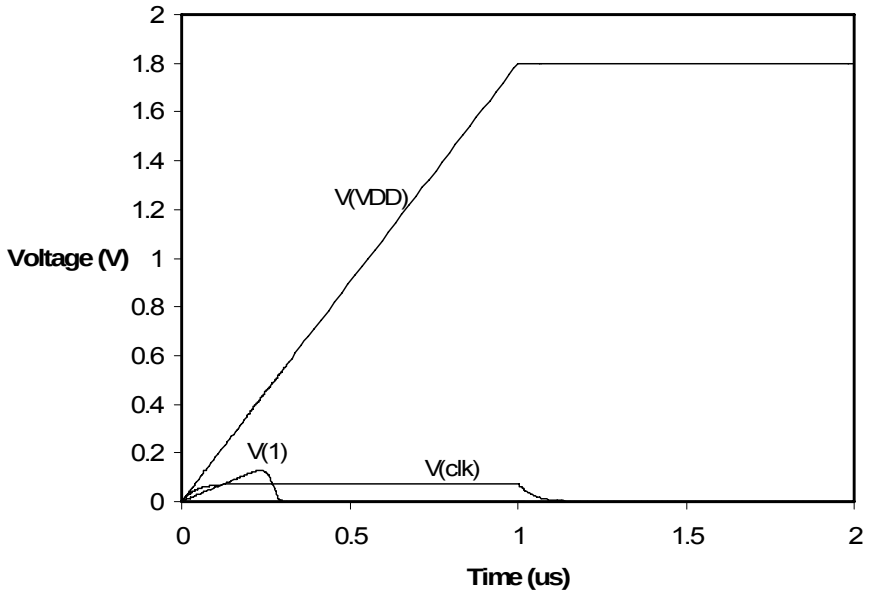


*Figure 3-36: Simulating the flip-flop based clamp for a 1μs power-up event*

It can be seen that the gate voltage of $M_0$ (node 1) rises to 0.12V and goes back to 0 immediately. Hence, even with a very fast power-up event, this clamp doesn't trigger which ensures the immunity to false triggering.

As mentioned earlier, the concept of using a flip-flop to latch the gate of $M_0$ to '1' under ESD conditions brings the concern of turning off the clamp after triggering. Therefore, another set of experiments is necessary to make sure the clamp turns off after false triggering. As a result, the rise time of the power-up event is further reduced to

200ns, 125ns and 50ns. Figure 3-37 shows the voltage of node 1 during these power-up events.

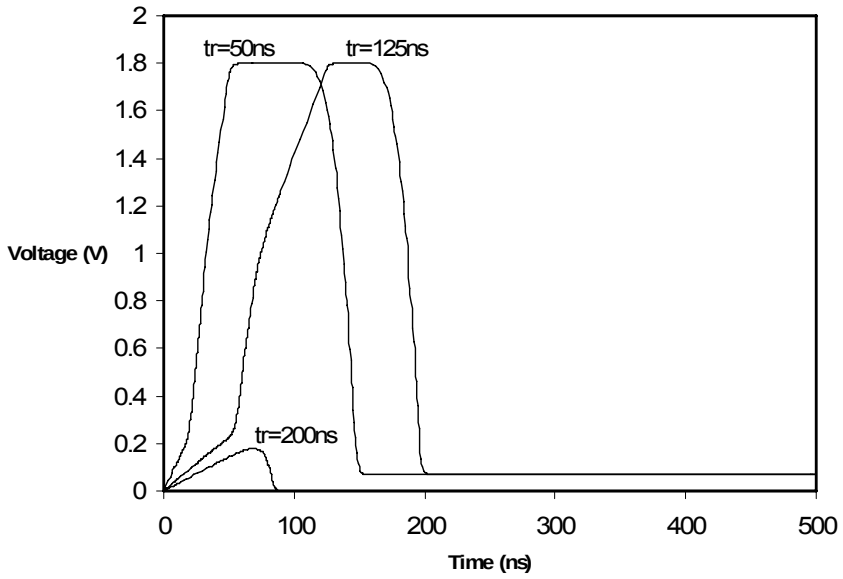


*Figure 3-37: The voltage of node 1 for $t_r$=50ns, 125ns and 200ns*

It can be seen that for the highest rise time of 200ns, which is not detected by the rise time detector, the clamp doesn't trigger. On the other hand, for smaller rise times of 125ns and 50ns, which are detected by the rise time detector, the clamp turns on at the power-up event but turns off after less than 50ns. This simulation ensures that the turn off mechanism of the clamp, which is implemented by modifying the flip-flop, is effective in case of false triggering.

Finally, the immunity to power supply noise is simulated for this clamp. Similar to section 3.6.2, the noise is added as a pseudo-random pulse to the supply voltage and the voltage of node 1 and the current of the transistor $M_0$ are monitored. The noise has 500Mbps data rate and 600m$V_{p-p}$ amplitude. This bit sequence along with the voltage of the node 1 is shown in Figure 3-38, while Figure 3-39 shows the current of the main clamp transistor $M_0$.

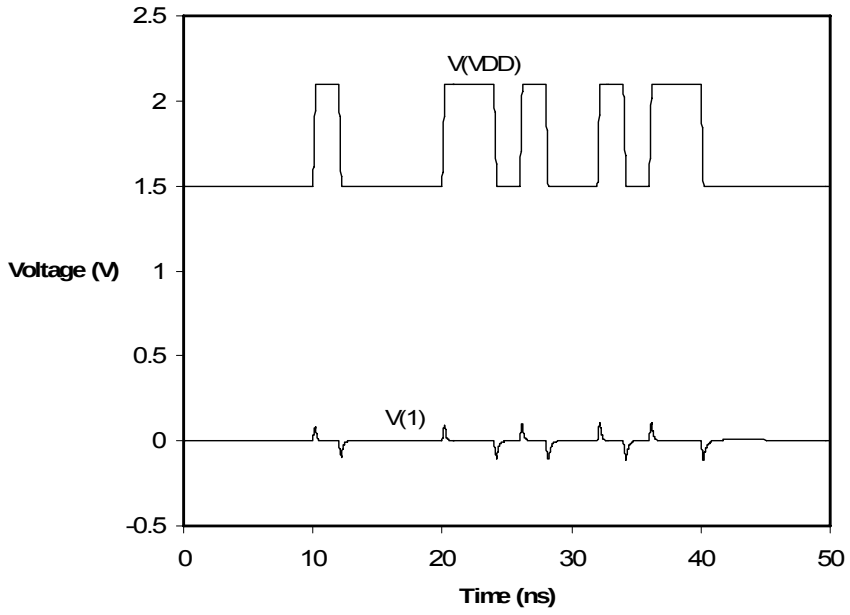


*Figure 3-38: Power supply noise immunity: the voltage of nodes 1 and $V_{DD}$*

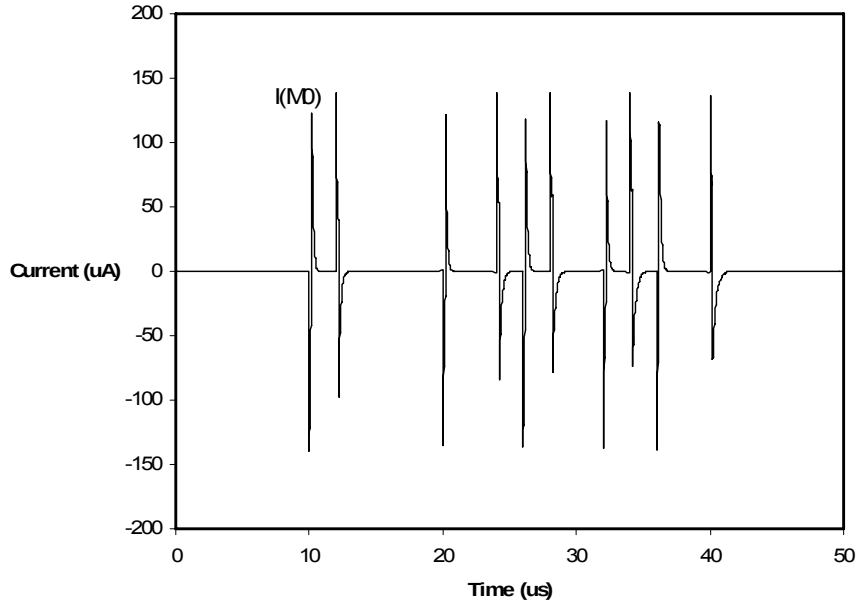


*Figure 3-39: Power supply noise immunity: the current of the transistor $M_0$*

It can be seen that the peak current of the clamp is approximately 150μA, which is very small considering the amplitude of the noise on the supply line [50]. Hence, the new clamp is immune to power supply noise.

### 3.7.3 Immunity to oscillation

In order to test the stability of the flip-flop based clamp, similar to the method used in section 3.5, the clamp is opened at node clk and the impedance seen from each side is added to the other side. Figure 3-40 shows the magnitude and phase of the open loop gain of this clamp.

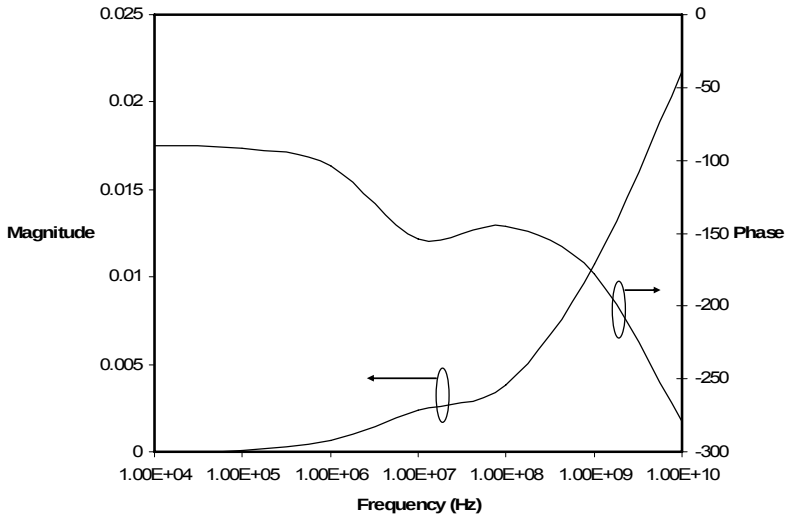


*Figure 3-40: Magnitude and phase of the loop gain of the flip-flop based clamp*

It can be seen that the magnitude of the loop gain of the proposed clamp is always less than 1 and hence immune to oscillation. Compared to other transient clamps, it can be seen that this clamp has the lowest loop gain magnitude and therefore, is the most stable transient clamp.

### 3.7.4 Measurement results

The flip-flop based clamp has been fabricated in 0.18μm TSMC CMOS technology. In this clamp, similar to the thyristor-based clamp, $R_C$ and $C_C$ were set to 500fF and 80kΩ respectively. $M_0$ was 400μm wide which was realized with 20 fingers and the total design area was 50μm×55μm. Figure 3-41 shows the layout of this clamp.

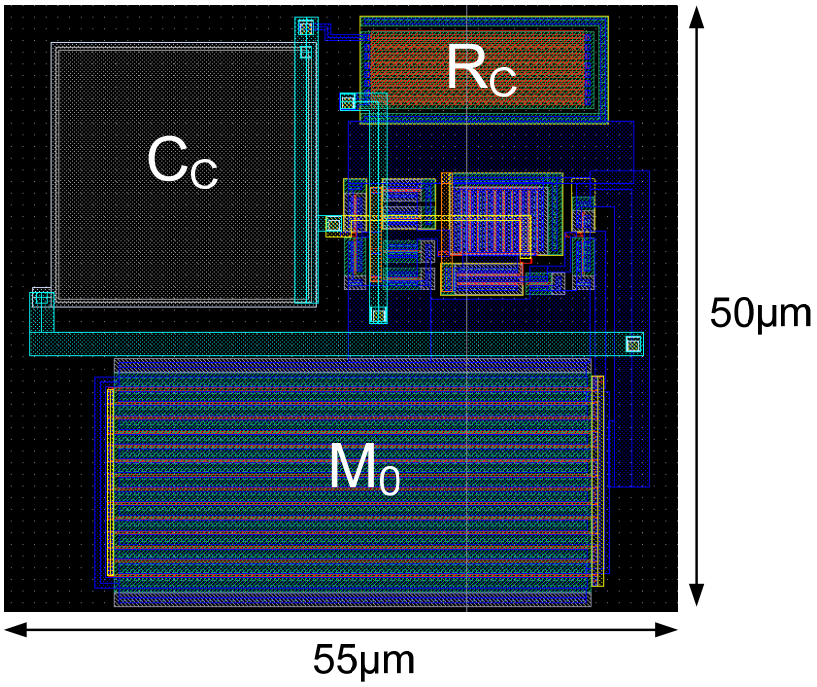


*Figure 3-41: The layout of the flip-flop based clamp*

For this clamp we did both TLP and HBM measurements. Figure 3-42 shows the TLP measurement results for this clamp using 100ns wide pulses with 10ns rise time. It can be seen that the leakage current at $V_{DD}$=1.8V is 6nA and the second breakdown current is 1.83A.

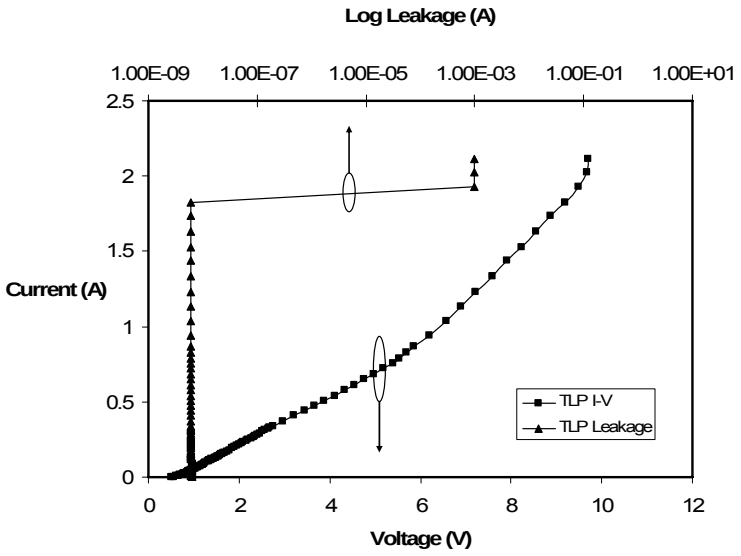


*Figure 3-42: TLP measurement results for the flip-flop based clamp*

Furthermore, HBM test has been done on the clamp as well. These measurements were done using IMCS-700 HBM/MM ESD tester. We applied both positive and negative HBM stresses with 500V step sizes. This clamp passes both +3kV and -3kV stresses. But when we increased the stress to 3.5kV, it passes +3.5kV but fails -3.5kV stress. These results are confirmed using the device simulator as well. For 3kV input stress the peak temperature of the transistors exceeds 500k, while for 4kV the peak temperature was over 1000K. Hence, this clamp should pass the 3kV stress but fail the 4kV HBM stress. It can be seen that the protection level for this clamp is the same as the thyristor-based clamp. The reason is that in both clamps the main transistor that conducts the ESD current is designed identically.

## 3.8 Summary

In sections 3.6 and 3.7 two novel clamps were presented: Thyristor-based clamp and flip-flop-based clamp. In thyristor-based clamp a CMOS thyristor element was used to create the required delay to completely discharge the ESD energy. In flip-flop-based clamp a modified flip-flop was used to further enhance the turn on time of the clamp. In order to evaluate the effectiveness of the two proposed clamps, they are compared with the state of the art clamps in Table 3-2.

*Table 3-2: Summary of different transient clamps*

| | Technology | Turn-on time | HBM level | W($M_0$) | Loop-gain |
|---|---|---|---|---|---|
| Dual TC, 2005 [49] | 0.13µm | 600ns | >5kV | 2300µm | 2 |
| SRAM-based, 2005 [50] | 90nm | 700ns | >5kV | 2300µm | 1.6 |
| Thyristor-based | 0.18µm | 1µs | 3kV | 400µm | 0.75 |
| Flip-flop-based | 0.18µm | >1µs | 3kV | 400µm | 0.017 |

In this table, in order to simulate the loop-gain of dual time constant and SRAM-based clamps, they were redesigned in 0.18μm technology with 400μm clamp transistor. It can be seen that not only thyristor-based and flip-flop-based clamps have the highest turn-on time, but they have the lowest loop gain as well, which makes them more stable compared to other state of the art transient clamps. The low HBM protection level of these two clamps is due to their smaller discharge transistors which is six times less than dual time constant and SRAM-based clamps. As mentioned in sections 3.6.1 and 3.7.1, in these clamps the failure is caused in the main discharge transistor $M_0$. Hence, by increasing the width of $M_0$, the HBM protection level of these clamps is increased as well.

# Chapter 4

# 4. High-Speed I/O with ESD Protection

In the previous chapters, different ESD protection circuits were discussed and a few novel techniques to improve their overall performance were presented. In this chapter, in order to experience the impact of the ESD protection circuit on high speed behavior of analog/mixed signal circuits, a high speed driver is designed and protected. Section 4.1 discusses the possible drivers to be used in this work. The design of the driver is presented in Section 4.2. The ESD protection circuits are explained in Section 4.3. Finally, the impact of the ESD protection circuit on the driver performance is explored in Section 4.4.

## 4.1 Introduction

The growth of data transfer rate in telecommunication networks necessitates the design of high-speed circuits. Furthermore, scaling of CMOS technology into nanometer

regime allows the full implementation of CMOS integrated high speed circuits. Buffers are one of the main blocks of high speed circuits such as clock and data recovery, serial to parallel converters and multiplexers/demultiplexers. The simplest implementation of a buffer consists of CMOS inverters. Figure 4-1 shows the schematic of a CMOS inverter along with its DC $V_{out}$-$V_{in}$ characteristic.

In addition to its simplicity, this buffer has a number of other advantages as well: It has a very low leakage current; as it can be concluded form Figure 4-1(b), this buffer has a very large small signal gain compared to other one stage buffers; finally, it has a very large noise margin. However, there are some major limitations in this buffer which makes it less suitable for very high-speed applications. The existence of a PMOS transistor lowers the maximum frequency of operation. Furthermore, as the inverter is a single ended circuit, it is very sensitive to noise sources such as supply noise, substrate noise and cross talk. Therefore, due to the above limitations, this buffer is not used in very high speed applications [57].

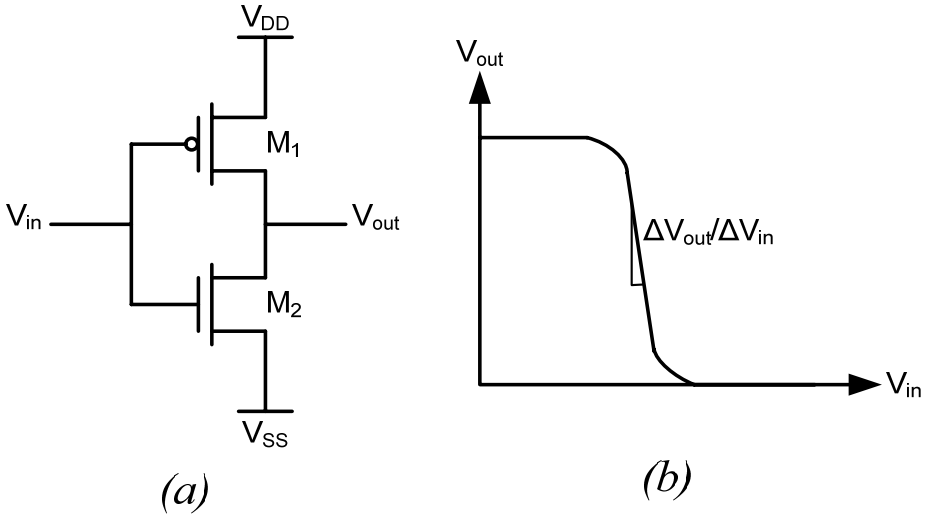


*Figure 4-1: CMOS inverter (a) schematic (b) $V_{out}$-$V_{in}$ characteristic*

In high frequency applications where CMOS inverters cannot be used as buffers, current mode logic (CML) drivers are often used [57]. Figure 4-2 shows the schematic of a current mode logic buffer.

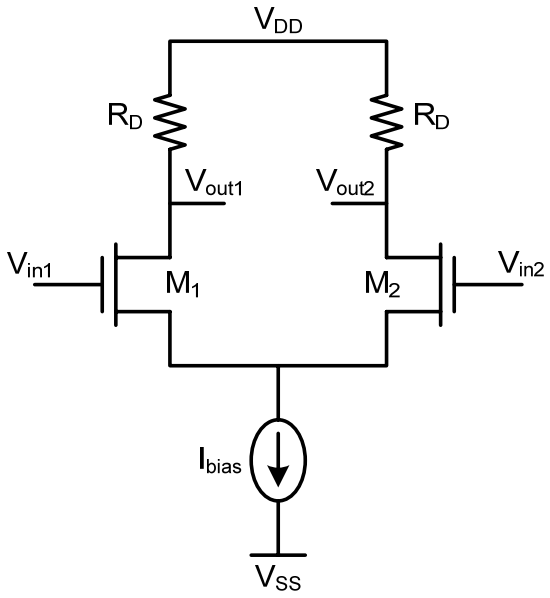


*Figure 4-2: Current mode logic buffer*

This buffer consists of a CMOS differential pair with a tail current source $I_{bias}$. The input voltage swing is large enough so that depending on the input voltage, the current of the current source flows through one branch only. Hence, when the current is going through $M_1$, the output voltages are found from the following equations:

$$V_{out1} = V_{DD} - R_D I_{bias},\ V_{out2} = V_{DD} \tag{4-1}$$

and when the current is going through $M_2$, the output voltages are found equal to:

$$V_{out1} = V_{DD},\ V_{out2} = V_{DD} - R_D I_{bias} \tag{4-2}$$

Therefore, it can be seen that the differential output swing ($V_{out1}$-$V_{out2}$) equals to $2R_D I_{bias}$.

Current mode logic circuit was first used in gigahertz MOS adaptive pipeline technique [58]. However, due to its superior performance, it's been used in many other applications such as ultra-high-speed buffers [59], latches [60] and frequency dividers [61]. The main advantage of a CML circuit is the ability to operate with lower signal voltage and higher frequency at lower supply voltage. Furthermore, due to its differential structure and high common-mode rejection, CML buffer is insensitive to noises on power and ground nodes. Although they suffer from static power dissipation, due to their superior performance, they are the best choice for high speed applications [57]. Hence, in

order to study the impact of different ESD protection methods on the behavior of high-speed circuits, a 3Gbps CML driver is used as a reference. ESD protection for this driver is provided for all four zapping modes and based on both MOS and SCR devices. A comparison at the end of this chapter shows that SCR-based devices have less impact on the driver due to their lower parasitic capacitance.

## 4.2 CML Driver Design

As mentioned earlier, in this work a CML driver is designed as a reference to compare different ESD protection methods. Table 4-1 shows the specs that were targeted in the design of the CML driver in 0.13μm UMC CMOS process.

*Table 4-1: Design requirements for the CML driver*

| | |
|---|---|
| Input differential swing | $400mV_{p-p}$ |
| Output differential swing | $800mV_{p-p}$ |
| Data rate | 3Gbps |
| Rise/fall time | 150ps |
| On-chip load resistor | 50Ω |
| Capacitive load | 1pF |
| Jitter | 1ps |

In order to meet all the specs, we designed a two stage CML driver with 50Ω on-chip loads at the second stage. As the measured differential output swing should be $800mV_{p-p}$, the impact of the measurement equipment on the driver should be considered. The model that was used for the measurement equipment is shown in Figure 4-3. It can be seen that another 50Ω resistor will be placed in parallel with the on-chip load resistor, which divides the output swing by 2. Hence, the driver is designed for 1600mV differential output swing.

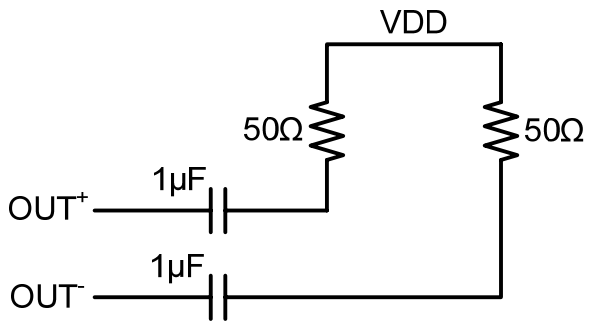


*Figure 4-3: Modeling the measurement equipment*

As the differential swing is 1600mV, and knowing that the load resistor $R_D$ is 50Ω, $I_{bias}$ of the second stage becomes 16mA. Figure 4-4 shows the schematic of the two stage CML driver, while the size of transistors and the value of resistors are given in Table 4-2.

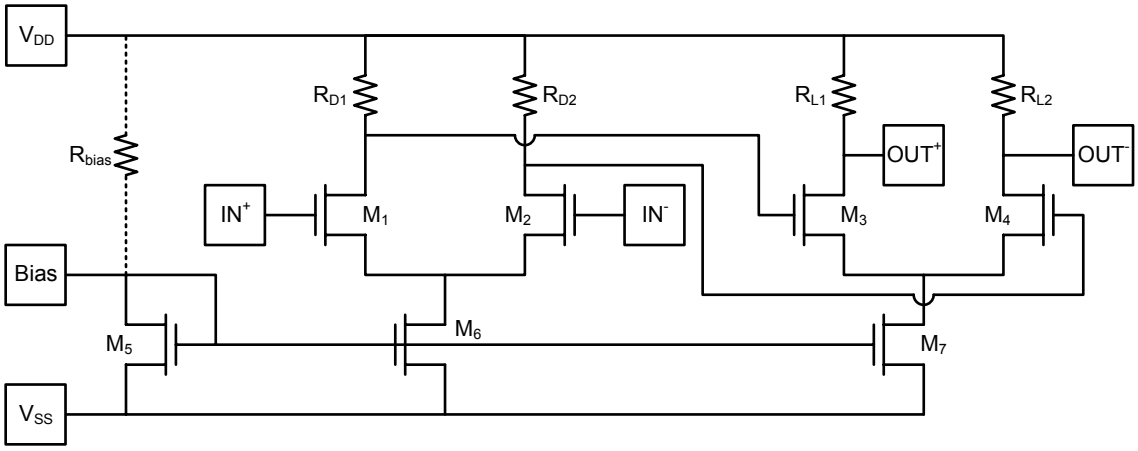


*Figure 4-4: Two stage CML driver*

*Table 4-2: Sizing of the two stage CML driver*

| | |
|---|---|
| $M_1$ & $M_2$ | 50μm/0.12μm |
| $M_3$ & $M_4$ | 90μm/0.12μm |
| $M_5$ | 15μm/0.12μm |
| $M_6$ | 30μm/0.12μm |
| $M_7$ | 160μm/0.12μm |
| $R_{D1}$ & $R_{D2}$ | 260Ω |
| $R_{L1}$ & $R_{L2}$ | 50Ω |
| $R_{bias}$ | 300Ω |

In order to be able to tune the output swing of the driver, $R_{bias}$ is considered as an external resistor. Hence, the driver has 5 I/O pins and 2 supply pins which are shown in Figure 4-4. The resistors $R_{D1}$, $R_{D2}$, $R_{L1}$ and $R_{L2}$ are realized with poly resistors.

This driver was designed for the 700mV-900mV input voltage range. In order to test the swing and rise time of this driver, a 2GHz differential pulse voltage is applied to the input and the output voltage is simulated. Figure 4-5 shows the differential input and output voltage of this driver.

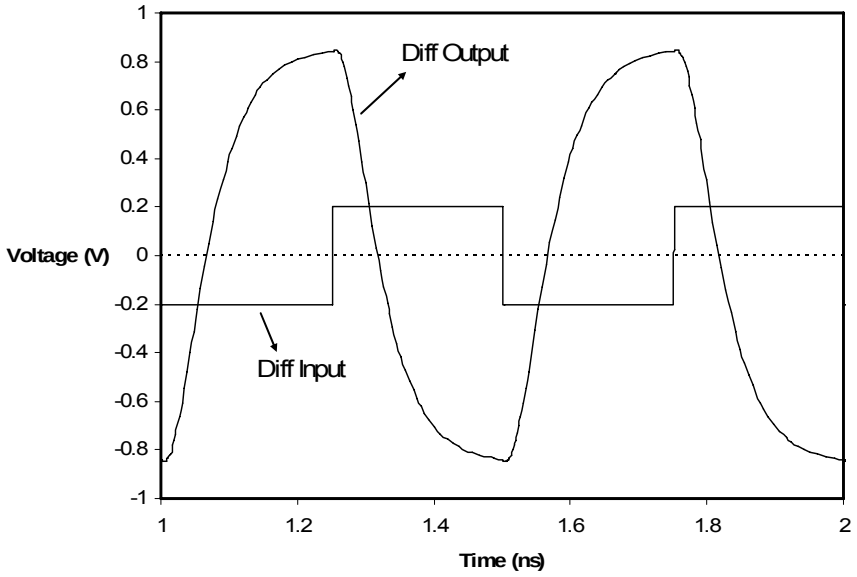


*Figure 4-5: Differential input and output voltages of the CML driver*

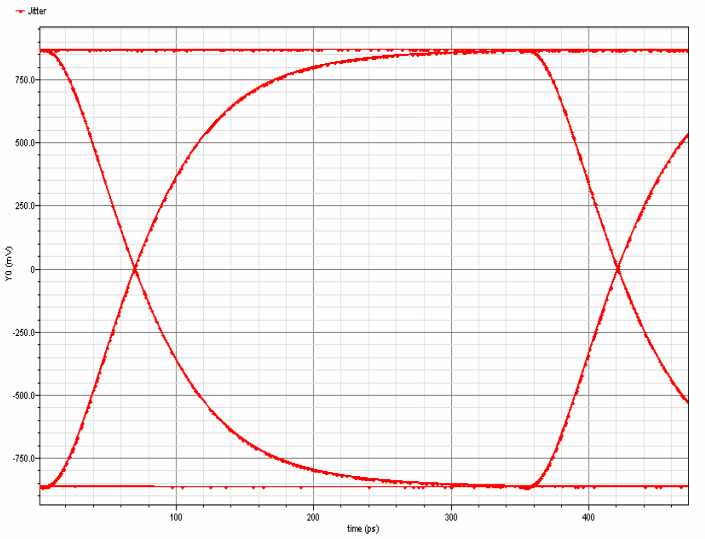


*Figure 4-6: Simulated eye-diagram of the CML driver*

It can be seen that the rise time is 116ps and the differential output swing is 1700mV. Hence, this driver meets the requirements of the Table 4-1. In order to simulate the jitter, a 3Gbps pseudo random input sequence is applied to the driver. Figure 4-6 shows the eye diagram of the differential output for 2000 samples. From this graph the jitter is calculated to be only 229fs, which is much less than our 1ps limit.

## 4.3 ESD Protection Methods

In order to provide complete ESD protection for the driver in Figure 4-4, two families of devices are used: MOSFET and SCR. The ESD protection circuit should provide full protection against all four zapping modes. SCR-based devices have been used extensively in high speed applications due to their low parasitic capacitance [62], [63], [64]. As the circuit has five I/O and two supply pins, five ESD protection circuits are required for the I/O pins and one clamp between $V_{DD}$ and $V_{SS}$. Figure 4-7 shows the protection scheme for this driver.

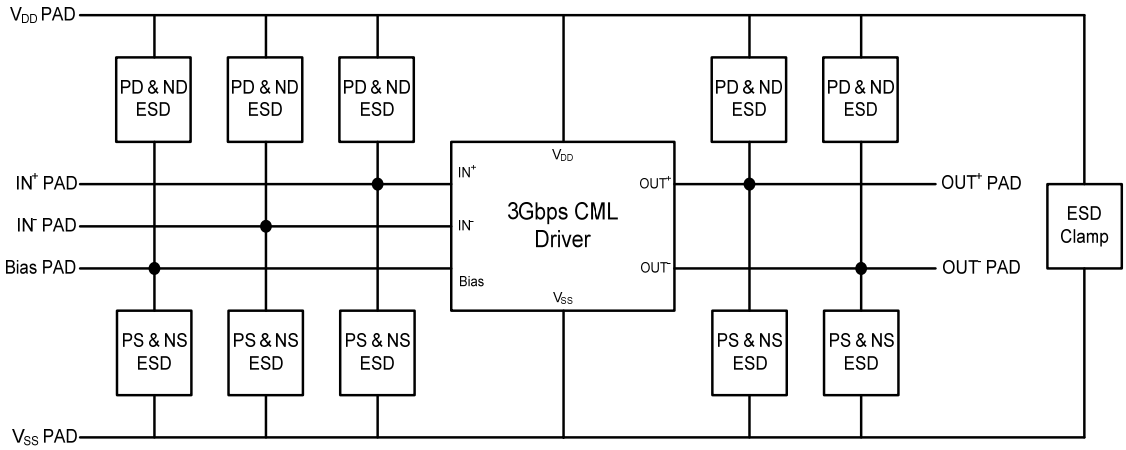


*Figure 4-7: ESD protection scheme for the CML driver*

In order to compare MOS and SCR based protection strategies, two separate drivers are implemented, where one of them is protected using gate-substrate triggered MOS and the other is protected using gate-substrate triggered LVTSCR. In the next two sub-sections these two ESD protection circuits are discussed in detail.

### 4.3.1 MOS-based ESD protection circuit

The MOS-based protection circuit uses the gate-substrate triggered technique that was introduced in section 2.4.1. Hence, two additional transistors are added to the main NMOS to provide gate triggering and substrate triggering. However, increasing both gate and substrate voltage of an NMOS transistor reduces the threshold voltage and increases the leakage current of the transistor. Therefore, in order to reduce the leakage current, another transistor is added to tie the gate to ground under normal operating conditions. Figure 4-8 shows an NMOS transistor with gate-substrate triggering where the transistor $M_{nl}$ is added to reduce the leakage.

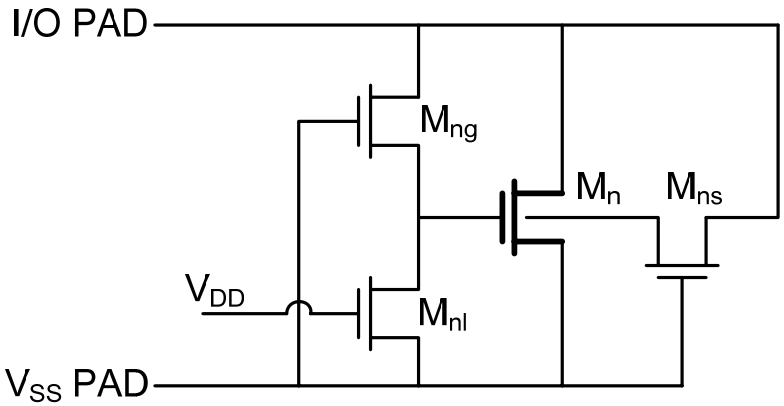


*Figure 4-8: Gate-substrate triggered NMOS with low leakage option*

Under ESD conditions, $V_{DD}$ is floating. Therefore, $M_{ng}$ and $M_{ns}$ provide gate and substrate triggering for the main protection transistor $M_n$. Under normal operating conditions $M_{nl}$ turns on tying the gate of $M_n$ to ground. The impact of $M_{nl}$ on the leakage of the gate-substrate triggered NMOS is simulated in Cadence. Figure 4-9 shows the total current of the circuit in Figure 4-8, where the pad voltage is increased from 0 to $V_{DD}$ and compares it with the gate-substrate triggered NMOS.

In this simulation the width of the main transistor $M_n$ is 320µm and the transistors $M_{nl}$ is 0.5µm wide. It can be seen that using $M_{nl}$ the leakage current is reduced significantly. It should be noted that in the experiment of Figure 4-9, all the transistors are low threshold transistors. Hence, if high threshold transistors are used, the leakage of the gate-substrate triggered NMOS will be much smaller.

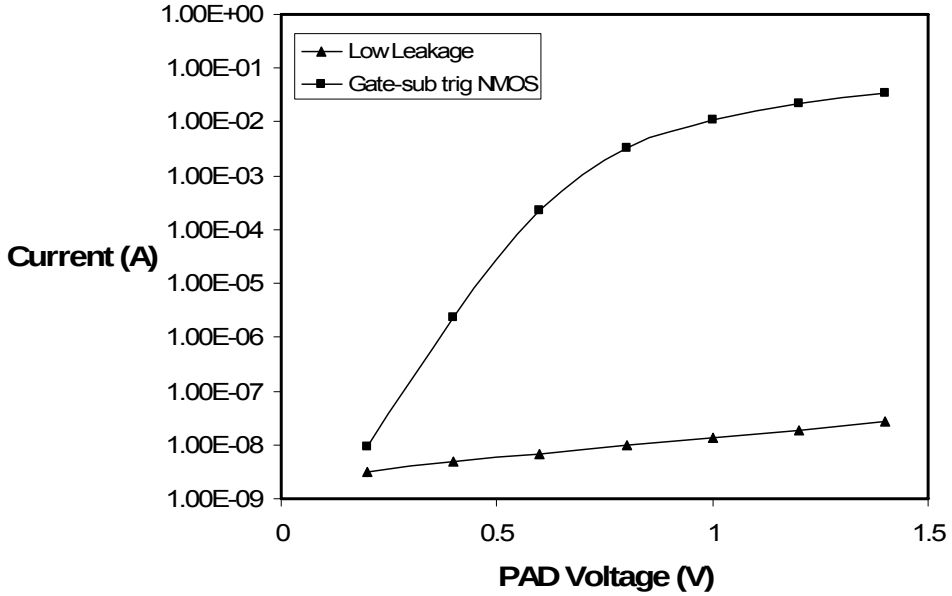


*Figure 4-9: The reduction in leakage current by adding $M_{nl}$*

In order to simulate the low-leakage gate-substrate triggered NMOS shown in Figure 4-8 under ESD conditions, a model of the transistors is prepared in Medici. Figure 4-10 shows the I-V characteristic of this structure under quasi-DC conditions in 0.13µm technology.

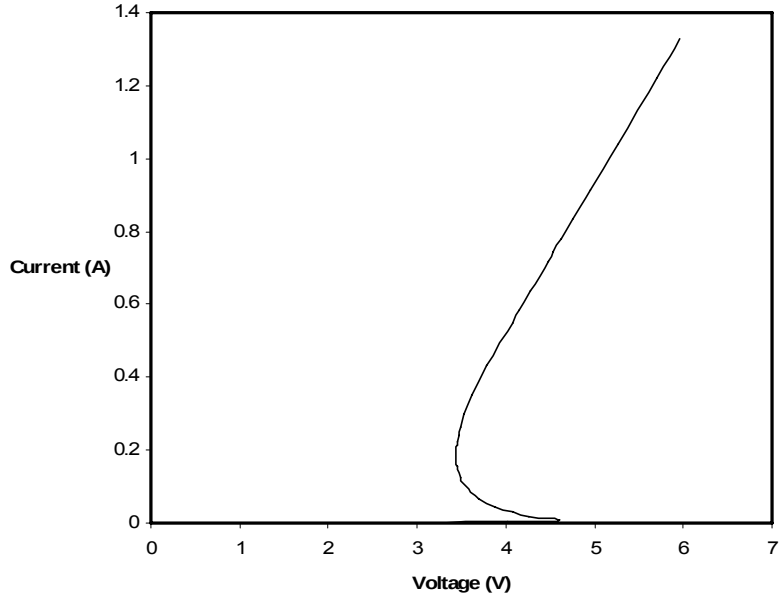


*Figure 4-10: I-V characteristic of the low-leakage gate-substrate triggered NMOS*

It can be seen that the first breakdown voltage of the structure is 4.6V which is lower than the oxide breakdown voltage in 0.13μm CMOS technology.

The protection for the PS-mode is done through NMOS transistors as shown in Figure 4-8. The ESD protection for ND-mode is provided with PMOS transistors. Figure 4-11 shows the schematic of the full-mode protection that is used to protect the CML driver. The main protection transistors are $M_n$ and $M_p$ which are 320μm wide. Substrate triggering is provided with $M_{ns}$ and $M_{ps}$ and their width is 80μm. Gate triggering is provided with 5μm wide $M_{ng}$ and $M_{pg}$. Finally, the leakage reduction is done with transistors $M_{nl}$ and $M_{pl}$.

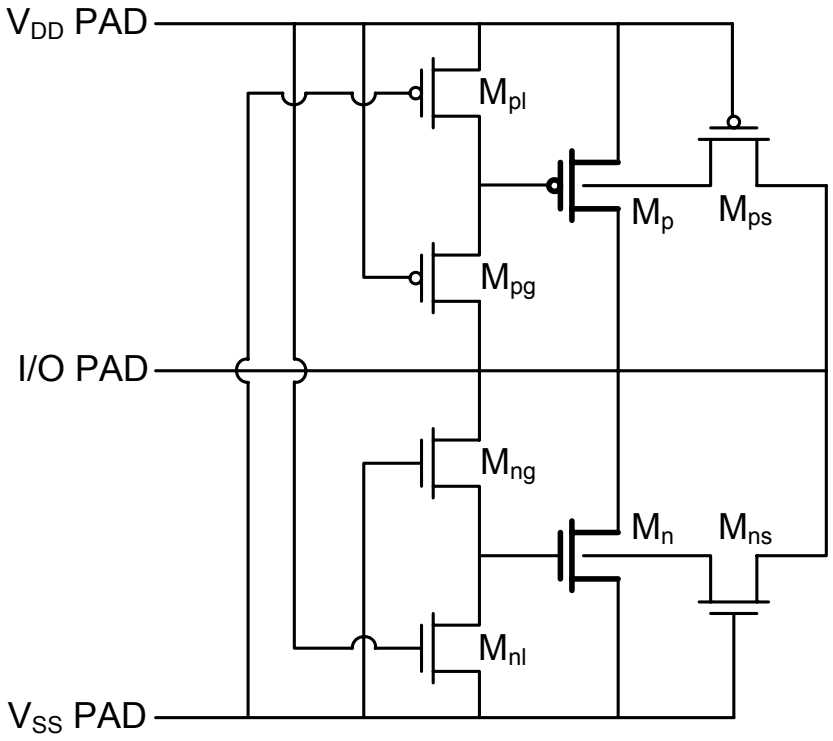


*Figure 4-11: Full-mode ESD protection using low-leakage gate-substrate triggered NMOS*

### 4.3.2 SCR-based ESD protection circuit

In order to provide ESD protection for the driver with SCR-based devices, LVTSCR with gate-substrate triggering is used (Figure 2-20). The ESD protection for all four zapping modes is provided based on the concept of all direction SCR that has been used

extensively in high speed applications [65], [66], [67], [68], [69]. The cross section of the all direction SCR along with its parasitic bipolar transistors is shown in Figure 4-12.

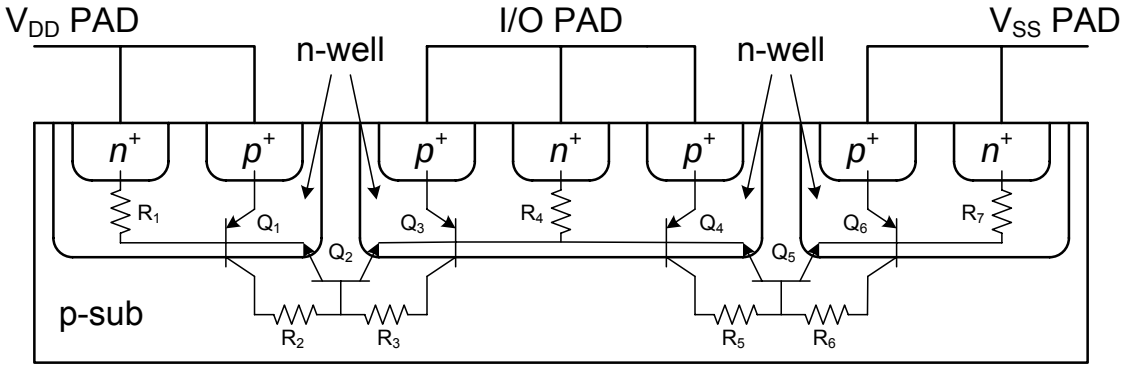


*Figure 4-12: All-direction SCR*

This structure consists of four SCR devices where one SCR exists for each zapping mode. The path for PS-mode is through the SCR formed by $Q_4$, $Q_5$, $R_4$ and $R_6$. The path for NS-mode is formed by $Q_5$, $Q_6$, $R_5$ and $R_7$. Similarly, the path for PD-mode is through the SCR formed by $Q_2$, $Q_3$, $R_2$ and $R_4$ and the path for ND-mode is formed by $Q_1$, $Q_2$, $R_1$ and $R_3$. As this device has similar discharge path for all zapping modes, it has symmetrical DC characteristic for both negative and positive stresses. The most important benefit of this structure is that it replaces four SCR devices while it has the parasitic capacitance of one device. It has been reported that using this method the parasitic capacitance is reduced by eight times [65].

In order to design an LVTSCR-based device for all four zapping modes the all direction SCR concept is used. The cross section of the gate-substrate-triggered LVTSCR used to protect the CML driver is shown in Figure 4-13.

In this figure $M_{ng}$ and $M_{pg}$ are used for gate-coupling, and $M_{ns}$ and $M_{ps}$ are used for substrate triggering. The SCR device is 100µm wide. Substrate triggering MOSFETs are 20µm wide while gate triggering MOSFETs are 5µm wide.

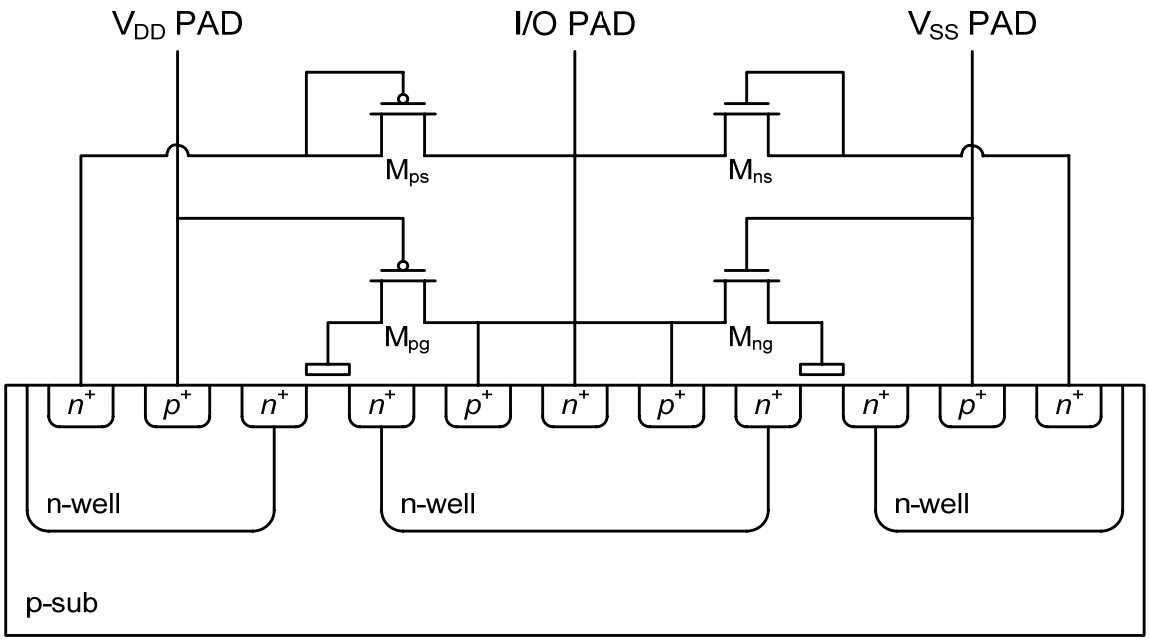


*Figure 4-13: Cross section of the all-direction gate-substrate triggered LVTSCR*

## 4.4 Complete I/O with ESD Protection

The final step is to combine the driver designed in section 4.2 with the ESD protection circuits presented in section 4.3. The protection scheme is based on the block diagram shown in Figure 4-7. As mentioned in section 4.3, two CML drivers are implemented where the first one is protected with MOS-based protection and the second one is protected with SCR-based protection. These two complete I/Os are explained in sections 4.4.1 and 4.4.2 and their performance is simulated using a circuit level simulator. Finally, these simulation results are confirmed with measurement results.

### 4.4.1 CML driver with MOS-based ESD protection

The first I/O that is designed and tested consists of the CML driver shown in Figure 4-4 that was protected with the low-leakage gate-substrate triggered MOS shown in Figure 4-11. As the protection circuit adds additional parasitic capacitance to the pads, it is expected to see degradation in the driver's performance. In order to test the overall

driver under normal operating conditions, the layout of the driver and the ESD protection circuit were prepared. The performance of the overall driver is tested by running a post layout simulation. A 2GHz, 400mV$_{p-p}$ pulse voltage is applied to the differential input of the driver. Figure 4-14 shows the differential output waveform.

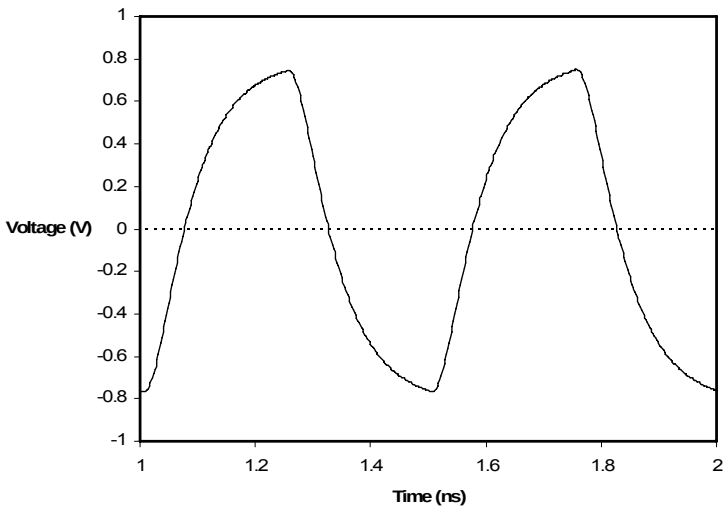


*Figure 4-14: Simulated differential output voltage of the CML driver with MOS-based ESD protection*

It can be seen that the output swing is 1550V and the rise time is 134ps. In the next step the jitter of the driver is simulated. Similar to the experiment done in section 4-2, a 3Gbps pseudo random data is applied to the driver. Figure 4-15 shows the eye-diagram which represents 3.4ps jitter.

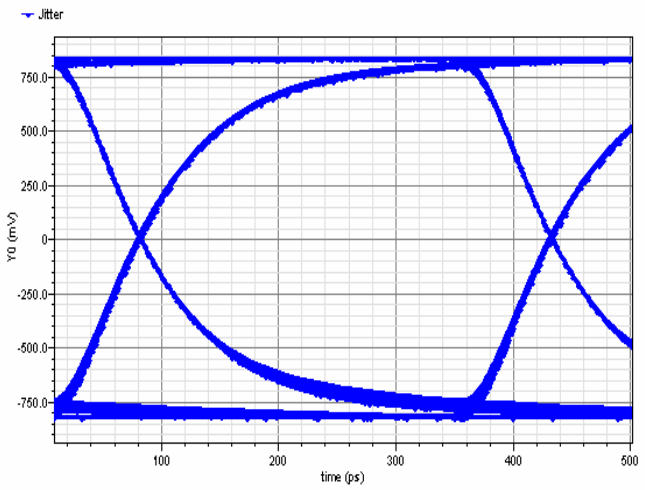


*Figure 4-15: Simulated eye-diagram of the CML driver with MOS-based ESD protection*

Finally, the driver with MOS-based ESD protection has been fabricated in 0.13µm UMC CMOS process. In order to test the performance of the driver, a Lecroy SDA 100G sampling oscilloscope was used. Jitter measurement was done using Centellax TG1B1 pseudo-random bit sequence generator. We used a 2GHz input voltage to test the driver's output waveform and jitter. As our signal generator wasn't accurate enough the input signal has an initial jitter. Figure 4-16 shows the jitter of the input signal.

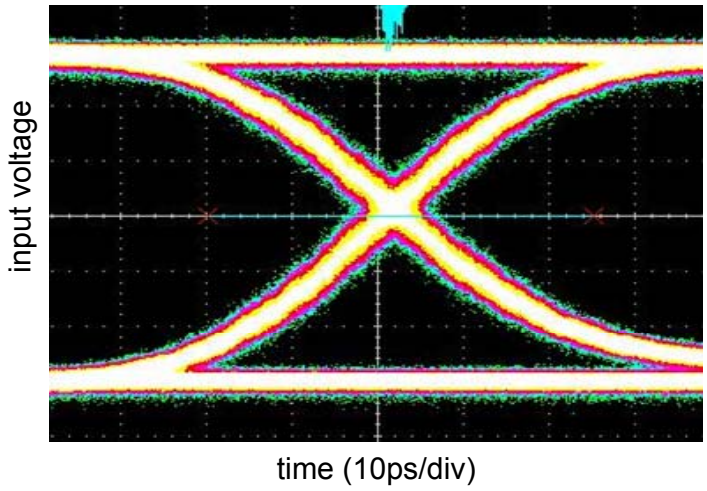


*Figure 4-16: Measuring jitter of the input signal*

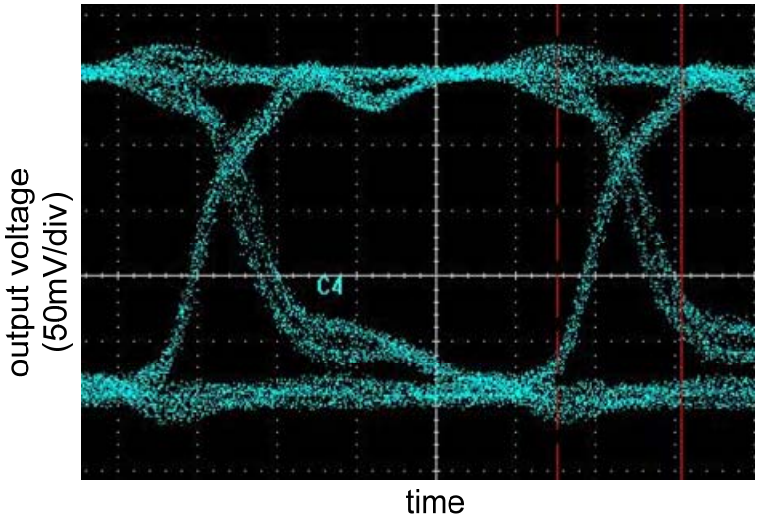


*Figure 4-17: Measured output voltage of the driver with MOS-based ESD protection*

It can be seen that the jitter of the input signal is 7ps. Hence, in measuring the jitter of the driver with ESD protection circuits the impact of the input jitter should be considered.

Figure 4-17 shows the single ended output waveform of the driver. As another 50Ω resistance is in connected to the output pad through the measurement equipment, the expected single-ended output voltage swing is 400mV. It can be seen that the MOS-based protection circuit has lowered the output swing to 250mV and the rise time is increased to 315ps.

The jitter is measured by applying a 4Gbps data rate to the input of the driver. Figure 4-18 shows the eye-diagram of the output voltage. It can be seen that the jitter is 10.7ps. Hence, the driver with MOS-based protection adds 3.7ps to the jitter.

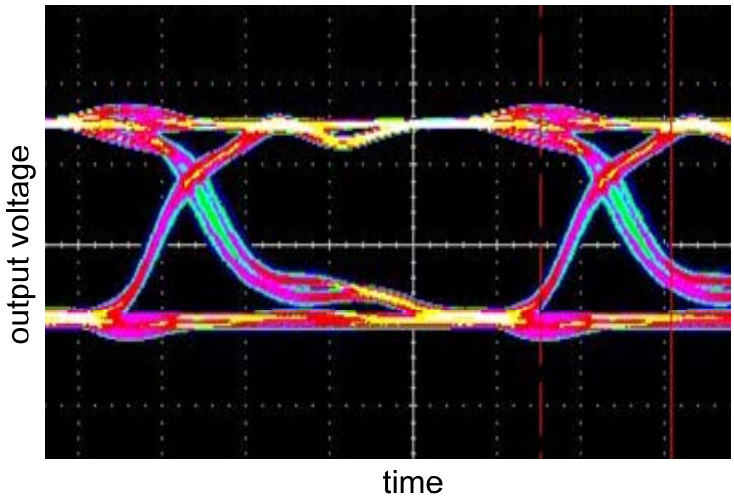


*Figure 4-18: Measured eye-diagram of the driver with MOS-based ESD protection*

Table 4-3 summarizes the specs of the CML driver and the driver with MOS-based ESD protection circuit.

*Table 4-3: MOS-based protection of the CML driver*

| | $V_{out(p-p)}$ – single ended | Rise time | Input jitter | Output jitter |
|---|---|---|---|---|
| CML driver | 425mV | 116ps | 0 | 229fs |
| CML + MOS ESD – Simulation | 287mV | 134ps | 0 | 3.4ps |
| CML + MOS ESD – Measurement | 250mV | 315ps | 7ps | 10.7ps |

The results in Table 4-3 show that using a MOSFET-based protection, the driver performance is degraded significantly. Furthermore, it can be seen that a difference exists between simulation and measurement results for the output jitter and rise time. These differences are due to several non-idealities: In simulation, ideal input pattern (zero jitter and very low rise time) was used, while in measurement input signal has 7ps jitter and 45ps rise time; simulation was done without considering all parasitics such as board and interconnect resistance and capacitance.

### 4.4.2 CML driver with SCR-based protection

The second driver uses SCR-based protection for the CML driver. The ESD protection is provided using the gate-substrate-triggered LVTSCR shown in Figure 4-13. Similar to section 4.4.1 in the first step the layout of the ESD protection circuit is provided to run a post layout simulation of the driver with ESD protection circuit. In order to test the output swing and rise time of the driver with ESD protection, a $400mV_{p-p}$ differential voltage is applied to the driver. Figure 4-19 shows the differential output voltage. It can be seen that SCR-based protection reduces the output swing from 1700mV to 1660mV while the rise time is increased from 116ps to 125ps. Jitter of the driver is tested by applying a 3Gbps pseudo random pulse to the input of the driver. Figure 4-20 shows the eye-diagram where the jitter is measured to be 338fs.

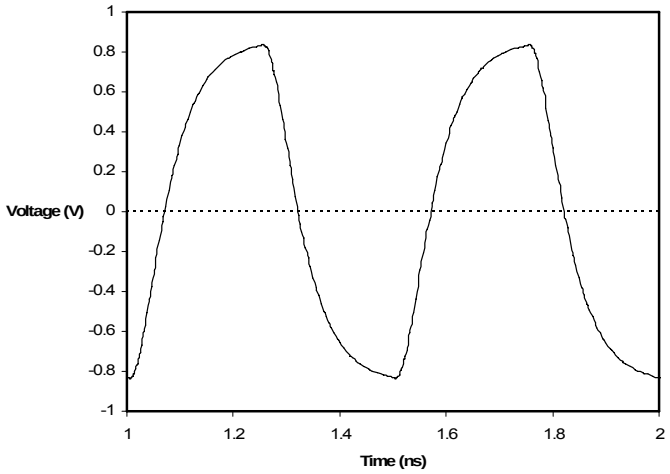


*Figure 4-19: Simulated differential output voltage of the CML driver with SCR-based ESD protection*

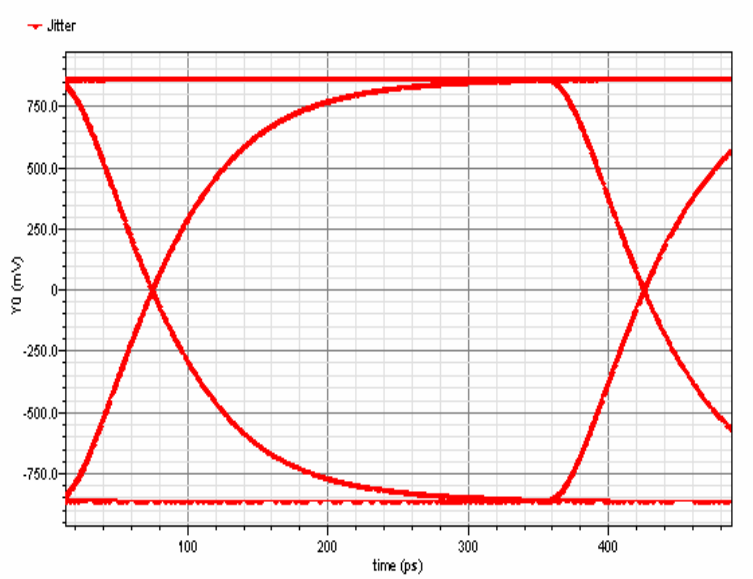


*Figure 4-20: Simulated eye-diagram of the CML driver with SCR-based ESD protection*

This CML driver has been implemented in 0.13µm UMC CMOS process. The performance of the driver is tested similar to section 4.4.1. A 2GHz input voltage is used to test the swing, rise time and jitter of the driver. Figure 4-21 shows the single ended output waveform of the driver with ESD protection circuit.

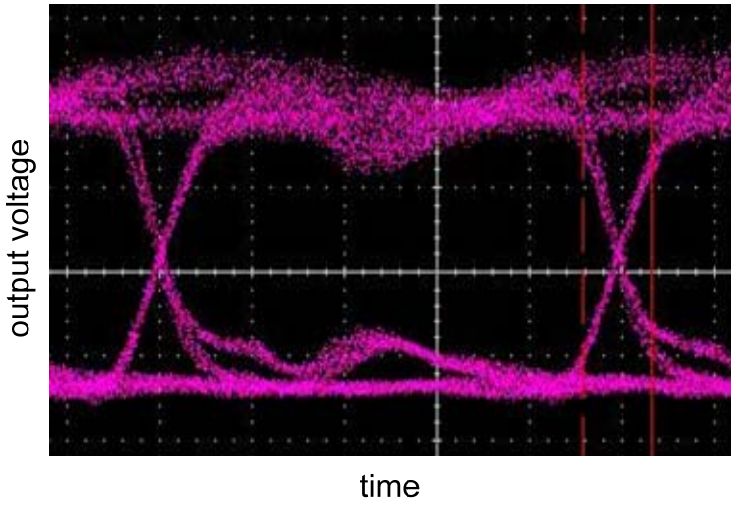


*Figure 4-21: Measured output voltage of the driver with SCR-based ESD protection*

Similar to section 4.4.1, as in this measurement another 50Ω resistance is in parallel with the output of the driver, the expected single ended swing of the driver is $400mV_{p-p}$. It can be seen that the output swing is $350mV_{p-p}$ and the rise time is 148ps. Therefore,

compared to MOS-based protection, the degradation in swing and rise time is much smaller with SCR-based protection. Jitter measurement has been done on this driver as well. Figure 4-22 shows the eye-diagram of the driver with SCR-based protection for 2000 samples.

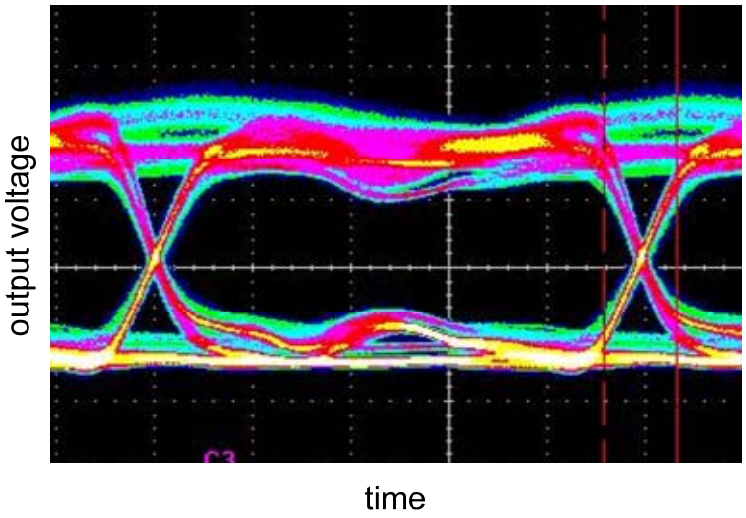


*Figure 4-22: Measured eye-diagram of the driver with SCR-based ESD protection*

Again, in measuring jitter, the jitter of the input signal, which is 7ps, should be considered. Based on this eye-diagram the jitter of the driver is 7.7ps which shows an increase of 700fs in the jitter of the input signal. Table 4-4 summarizes the specs of the driver with SCR-based protection circuit.

*Table 4-4: MOS-based protection of the CML driver*

| | $V_{out(p-p)}$ – single ended | Rise time | Input jitter | Output jitter |
|---|---|---|---|---|
| CML driver | 425mV | 116ps | 0 | 229fs |
| CML + SCR ESD – Simulation | 415mV | 125ps | 0 | 338fs |
| CML + SCR ESD – Measurement | 350mV | 148ps | 7ps | 7.7ps |

It can be seen that, compared to MOS-based protection, SCR-based ESD protection has much smaller impact on the driver performance. This difference is mainly due to

lower parasitic capacitance of the SCR-based protection circuit. Similar to results of Table 4-3, the difference between simulation and measurement results are due to non-idealities in input signal and parasitics of the board and interconnects.

### 4.4.3 Comparison and discussion

Simulation and measurement results in sections 4.4.1 and 4.4.2 show that ESD protection circuits, if not designed properly, can have significant impact on the core circuit performance. Therefore, it is useful to know the maximum allowed capacitance that can be added by ESD protection circuit without sacrificing the performance. Hence, the ESD protection circuit is modeled with a capacitor and overall performance is simulated using Cadence for different capacitor values. Table 4-5 shows maximum swing, rise time and jitter for different capacitor values.

*Table 4-5: Impact of parasitic capacitance on the driver performance*

| Capacitance (fF) | Swing (mV) | Rise time (ps) | Jitter (fs) |
|---|---|---|---|
| 50 | 1676 | 121 | 284 |
| 150 | 1648 | 132 | 511 |
| 300 | 1584 | 146 | 1160 |
| 600 | 1422 | 163 | 4060 |

It can be seen that, by changing the ESD capacitance from 50fF to 600fF, swing is reduced by only %15 while rise time is increased by %34 and jitter is increased by more than 14 times. Therefore, for those applications where jitter is a requirement, such as cable drivers, optimizing parasitic capacitance of ESD protection circuit is very critical and should be kept less than 150fF.

# Chapter 5

# 5. Conclusion

Electrostatic discharge has been considered as a major reliability threat in semiconductor industry for decades. It was reported that EOS/ESD are responsible for up to 70% of failures in IC technology. Therefore, each pad must be designed with a protection circuitry that creates a discharge path for ESD current. Moreover, the protection circuit should remain transparent to the main circuit under normal operating conditions. As CMOS technology scales down, the design of ESD protection circuits becomes more challenging. This is due to thinner gate oxides and shallower junction depths in advanced technologies that make them more vulnerable to ESD damages. Furthermore, higher frequency of operation in advanced CMOS circuits necessitates lower parasitic capacitance on the pads. Hence, an ESD protection circuit with high protection level and low parasitic capacitance is a demand in high speed CMOS applications.

There are two major schemes to provide ESD protection for integrated circuits: snapback-based and non-snapback-based protection. In snapback-based method, a protection circuit is connected to each pad, which provides ESD protection for all four

zapping modes. The devices in the protection circuit are operating in their avalanche breakdown region. On the other hand, in non-snapback-based method, each pad is connected $V_{DD}$ and $V_{SS}$ with two diodes and the protection for the four zapping modes is provided through these diodes and a clamp between $V_{DD}$ and $V_{SS}$. In this method none of the devices is operating in the avalanche breakdown region. Therefore, this method can be simulated in circuit simulators such as Cadence.

Silicon controlled rectifiers have the highest protection level per unit area which makes them the best choice in snapback-based protection scheme. However, they suffer from high first breakdown voltage and latch-up susceptibility. In this research both of these limitations have been fully investigated. In order to reduce the first breakdown voltage, two novel techniques were presented. Gate-substrate triggered LVTSCR was introduced to reduce the first breakdown voltage of the LVTSCR with minimum additional parasitic capacitance. This device has a first breakdown voltage of 5V with 3kV protection level. The parasitic capacitance of this device is 185fF. To further reduce the parasitic capacitance of this structure, darlington-based SCR was designed which is based on increasing the current gain of the parasitic bipolar transistors. This device lowers the first breakdown voltage to 3V without a gate contact or any triggering mechanism. This device has over 6kV protection level with less than 100fF parasitic capacitance. Hence, it has the smallest parasitic capacitance compared to other state of the art SCR-based devices.

In order to improve latch-up immunity, two novel techniques were presented in this work. The first method increases the holding voltage above $V_{DD}$. Using an additional MOS transistor the holding voltage is increased to 4.55V, while the first breakdown voltage is increased by only 8%. The second method is based on increasing the holding current to reduce the chance of latch-up. In this method by adding a forward biased diode the holding current is increased to 78.5mA while the first breakdown voltage is increased by only 4%.

In non-snapback-based scheme, the main challenge is to design a transient clamp with high enough delay to discharge all the ESD energy. In this research we designed two transient clamps with a delay of at least 1μs. The first clamp uses a CMOS thyristor as the delay element. This clamp has a delay of 1μs and has 3kV protection level. In the

second method a flip-flop is used to turn on the clamp under ESD conditions and ensure that it remains "on" for a long time interval. However, the flip-flop has been modified to turn off the clamp after false triggering. Using this method a delay of over 1μs for 3kV protection level is achieved. Moreover, oscillation problem of transient clamps was addressed in this research and an analytical method to compare the stability of transient clamps was proposed. Using this method it was shown that thyristor-based and flip-flop-based clamps have the highest stability compared to other published clamps.

Finally, in order to study the impact of ESD protection circuits on normal operating condition of high speed circuits, a 3Gbps CML driver was designed. This driver was protected with MOS-based and SCR-based protection methods. For both MOSFET and LVTCR, gate-substrate triggering technique proposed in this work was used. Both protection circuits were designed with 3kV ESD protection level. The CML driver with Gate-substrate triggered MOSFET has 500mV differential output swing with 315ps rise time. This method increases the input jitter by 3.7ps. On the other hand, the CML driver with gate-substrate triggered LVTSCR has 700mV differential output swing with 148ps rise time and increases the input jitter by 0.7ps. The SCR-based protection circuit has less impact on driver performance due to its lower parasitic capacitance.

## 5.1 Main Contributions

In this thesis, several contributions for different aspects of ESD protection were presented. However, some of these designs are suitable for very high-speed state of the art circuits which are considered as the main contributions in this thesis.

a) A novel darlington-based SCR which provides very low first breakdown voltage with high ESD protection level and very low parasitic capacitance
b) A new flip-flop-based transient clamp that provides very high delay to completely discharge all the ESD energy and offers very high stability

## 5.2 Future Work

As CMOS technology is scaled, the operating frequency of circuits is increasing as well. Hence, the impact of ESD protection circuit on very high speed circuits such as 5-10Gbps clock and data recovery (CDR) circuits should be investigated. Based on the research done in this work, darlington-based SCR is suggested as a promising device to provide both high ESD protection level and better performance for the CDR.

Furthermore, as modern chips consist of analog and digital blocks with multiple supplies and ground pins, a proper ESD protection scheme between these pins is becoming very challenging. These ESD protection circuits should be able to provide the required protection in addition to proper isolation between analog and digital blocks. This issue is more critical in ground pins where the noise coming from the digital block should be completely isolated from the analog block.

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# Publications Resulted from this Work

## Papers

- H. Sarbishaei, O. Semenov, M. Sachdev, "A Transient Power Supply ESD Clamp with CMOS Thyristor Delay Element", *to be presented in EOS/ESD Symp*, 2007
- H. Sarbishaei, O. Semenov, M. Sachdev, "A New Flip-Flop Based Transient Power Supply Clamp for ESD Protection", *submitted to IEEE Trans Dev Materials Reliability*, March 2007, 7 pages
- H. Sarbishaei, O. Semenov, M. Sachdev, "A Darlington-Based SCR ESD Protection Device for High-Speed Applications", *submitted to IEEE Trans Dev Materials Reliability*, May 2007, 6 pages
- H. Sarbishaei, O. Semenov, M. Sachdev, "Optimizing Circuit Performance and ESD Protection for High-Speed Differential I/Os", *submitted to Custom Int Cir Conf*, 2007, 4 pages
- O. Semenov, H. Sarbishaei, V. Axelrad, M. Sachdev, "Novel gate and substrate triggering techniques for deep sub-micron ESD protection devices", *Microelectronics Journal*, vol. 37, pp. 526-533, 2006
- O. Semenov, H. Sarbishaei, M. Sachdev, "Analysis and design of LVTSCR-based EOS/ESD protection circuits for burn-in environment", *Int Symp Quality Electron Dev*, pp. 427-432, 2005

- O. Semenov, H. Sarbishaei, V. Axelrad, M. Sachdev, “The impact of CMOS technology scaling on MOSFETs second breakdown: Evaluation of ESD robustness”, *Microelectronics Reliability*, vol. 44, pp. 1817-1822, 2004
- O. Semenov, H. Sarbishaei, V. Axelrad, M. Sachdev, “The impact of CMOS technology scaling on MOSFETs second breakdown: Evaluation of ESD robustness”, *European Symp Reliability of Electron Dev Failure Physics Analysis*, 2004

## Books

- O. Semenov, H. Sarbishaei, M. Sachdev, ESD protection device and circuit design for advanced CMOS technologies, Approx 250 pages, Springer Academic Publishers (in progress)

# Glossary

**C**

| | |
|---|---|
| **CDM** | Charged Device Model |
| **CML** | Current Mode Logic |

**D**

| | |
|---|---|
| **DUT** | Device Under Test |

**E**

| | |
|---|---|
| **EOS** | Electrical Over Stress |
| **ESD** | ElectroStatic Discharge |

**G**

| | |
|---|---|
| **GCNMOS** | Gate-Coupled NMOS |
| **GGNMOS** | Grounded-Gate NMOS |
| **GST-LVTSCR** | Gate-Substrate Triggered LVTSCR |
| **GST-NMOS** | Gate-Substrate Triggered NMOS |

**H**

| | |
|---|---|
| **HBM** | Human Body Model |

**L**

| | |
|---|---|
| **LVTSCR** | Low Voltage Triggered SCR |

**M**

| | |
|---|---|
| **MM** | Machine Model |
| **MOSFET** | Metal Oxide Semiconductor Field Effect Transistor |

**S**

| | |
|---|---|
| **SCR** | Silicon Controlled Rectifier |
| **SRAM** | Static Random Access Memory |

**T**

| | |
|---|---|
| **TLP** | Transmission Line Pulse |