Push-Pull Based High Efficiency and High Power Broadband Power Amplifiers for Wireless Base Stations

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

The monthly data throughput by 2021 is forecasted to be ten times that of December 2015. As a result of the on going dramatic increase in demand, service providers are assigned new frequency bands to accommodate more channels to carry more data. However, the usable part of the spectrum is a limited resource so modern communication signals were designed to be more spectrally efficient to send more bits over the same channel bandwidth. However, these spectrally efficient signals have high peak to average power ration (PAPR). The immediate reaction to these changes was to add additional RF front-end branches to accommodate the new frequency bands. Initially, the power amplifier (PA)s used at the time were not optimized for back-off efficiency and where operating at low efficiency which caused significant increase in heat generation for the same average power produced which in turn increased cooling costs and reduced the life time of the PA. After the introduction of back-off efficiency enhancement techniques the PAs became more efficient however they were limited in bandwidth which is typically 10-15%. This work focuses on reducing the redundancy of power amplifiers in communication base stations while maintaining high back-off efficiency.

After exploring the literature to understand the limitations of current implementations, it was found that the push-pull topology is often used at low frequency in broadband high power PAs. In the absence of a complimentary transistor pairs the push-pull implantation requires the use of balanced to unbalanced (balun) transformers. Various balun implantations were hence investigated to identify the most suitable option for broadband planar implementation. As a result, a methodology was proposed to co-design the balun and the matching network in order to have better control over the harmonic impedance. An 85 W push-pull PA was then designed based on the proposed methodology with a multi-octave bandwidth as a demonstration of the broadband potential of push-pull PAs at radio frequency (RF) frequencies.

Next, the two most popular techniques for back-off efficiency enhancement, i.e., envelope tracking (ET) and load modulation, were studied and the principle of load modulation was found to be more suitable for broadband signal transmission. The Doherty architecture is the most common implementation of load modulation and it comes in two basic variations, the parallel-connected load (PCL) and series-connected load (SCL) Doherty Power Amplifier (DPA)s. The original architecture concepts are not only band limited but also ill-suited for high frequency designs where the transistors' parasitics introduce significant effect. However, later literature expanded on the original concept of the PCL variation which provided the needed flexibility for wider bandwidth implementations at a higher frequency. Using the broadband implementation and the co-design methodology

two push-pull amplifiers were used in a PCL DPA topology and demonstrated that the push-pull utilization doesn't have a significant impact on the bandwidth of the output combiner as an octave bandwidth was achieved with the use of digital Doherty.

Lastly, the thesis proposes a new approach for designing high power DPAs with extended bandwidth. It starts with a generic SCL DPA architecture to derive the equations that relate its underlying combiner's ABCD parameters to the transistor's optimum impedance and load impedance. These equations featured the possibility of significantly increasing the load impedance in SCL DPA compared to the one of the popular PCL DPA architecture. This is particularly beneficial when targeting very high power DPAs for macro-cell base stations and broadcast applications where very low load impedance can seriously complicate the design and limit the achievable bandwidth. To further maximize the load impedance increase, the proposed SCL DPA uses a push-pull topology for the main and peaking amplifier stages. A low-loss planar balanced to unbalanced transformer (balun) combiner network is then utilized to realize the SCL DPA combining. The proposed approach was finally applied to design a proof-of-concept 350 W SCL DPA which operates over the band spanning from 720 to 980 MHz. The prototype demonstrated a peak output power of about 55 dBm over a 30% fractional bandwidth (FBW) with a 6 dB back-off efficiency, measured using pulsed signal, between 46.6% and 54.6%. Furthermore, the modulated signal based measurement results confirmed the linearizability of the SCL DPA prototype while maintaining a back-off efficiency over 50% for a 7.1 dB peak to average power ratio signal.

Acknowledgements

My deepest gratitude to my supervisor, Professor Slim Boumaiza, for his constant help and support throughout my research. I truly appreciate his diligence in involving me in various projects to increase my exposure to the research in the field. Moreover, I would like to thank my committee members for taking the time to review this work and providing me with feedback. I have had the honor to be part of an amazing research group. Throughout the years, everyone in EmRG have been friendly, supportive and helpful. A special thanks to Yushi Hu for being a brother and a fellow philosopher where no topic is off limits and no depth is too deep. I would also like to thank my family and would like to tell them that their love and support have been very valuable to me.

Dedication

This work is dedicated to Friends and Family.

Table of Contents

List of Tables

List of Figures

Abbreviations

3GPP 3rd generation partnership project 11

ACLR adjacent channel leakage ratio 62, 92

ADS advanced design systems 58

AWG arbitrary wave generator 59

BBE baseband equivalent 63

CW continuous wave 68

DE drain efficiency 11, 44, 59, 61, 62, 68, 71

DPA Doherty Power Amplifier iv, v, xiv, xvi, 4–7, 38–41, 43, 66–69, 71, 73–76, 80–83, 86, 88, 90, 92, 93, 95–99

DPD digital pre-distrotion 42, 62, 63, 99

DUT device under test 59

EA envelope amplifier 37, 38

ET envelope tracking iv, 2, 4, 37, 38, 63, 96

FBW fractional bandwidth v, 35, 43

GaN gallium nitride 42, 43, 68, 71, 74

HEMT high electron mobility transistors 42, 43, 68, 71

HFSS high frequency structure simulator 58, 87

LTCC low temperature co-fired ceramic 87, 99

LTE long term evolution 62, 63

OFDM orthogonal frequency-division multiplexing 1, 2

PA power amplifier iv, 2–6, 8, 12, 13, 27, 35–38, 41, 42, 44–46, 54, 56, 59, 61–63, 66, 73, 92, 94, 96–99

PAE power added efficiency 11

PAPR peak to average power ration iv, 2, 36, 38, 61–63, 66, 91, 92, 95–98

PCB printed circuit board 4, 51, 99

PCL parallel-connected load iv, v, 4–7, 73–76, 81, 83, 88, 93, 95, 96, 98

PP-DPA push-pull Doherty power amplifier 6, 43, 66, 67, 69, 71, 73, 87, 98

PPPA push-pull power amplifier 6, 23, 42–45, 47, 55, 56, 59, 63, 71, 73

PSD power spectral density 62

RF radio frequency iv, xv, 2, 4, 9, 11, 22, 27, 36, 38, 54, 57, 59, 68, 75, 96

S-parameters scattering matrix parameters xv, 23–27, 54, 56, 58

SCL series-connected load iv, v, xvi, 4, 6, 7, 73–76, 79–81, 83, 88, 92, 95, 97–99

SMD surface mount device 64, 87

WCDMA wideband code division multiple access 37, 61–63

Chapter 1

Introduction

1.1 Motivation

The demand for more bandwidth is growing at a quick rate. The monthly mobile communication data throughput, according to Cisco [1], is expected to grow by ten folds by 2021 in comparison to the end of 2015 Fig. 1.1. The mobile communication infrastructure is adapting to keep pace with the demand by scaling its capacity in two fundamental ways. Additional bands of the microwave spectrum are allocated to mobile communication. The new bands are assigned based on availability and suitability, and they are rarely a continuation to existing communication bands. As a result, there are now numerous mobile communication bands in use today and there is a wide spread of these bands over frequencies from as little as 380 MHz up to frequencies as high as 2.7 GHz as shown in Table. 1.1 with planned expansions to $3.4 - 6$ GHz [2–4]. In practice, however, the allocation of new communication bands alone is not sufficient due to the scarce nature of this resource. In order to address the limited spectral scalability issue, new communication standards are created to be more spectrally efficient. Spectral efficiency of modern communication signals has been increased significantly using advanced modulation schemes such as orthogonal frequency-division multiplexing (OFDM). These changes have significantly affected the utilization efficiency of existing base stations. Moreover, they have driven the cost of deployment significantly in order to accommodate both the new bands and the advanced modulation schemes.

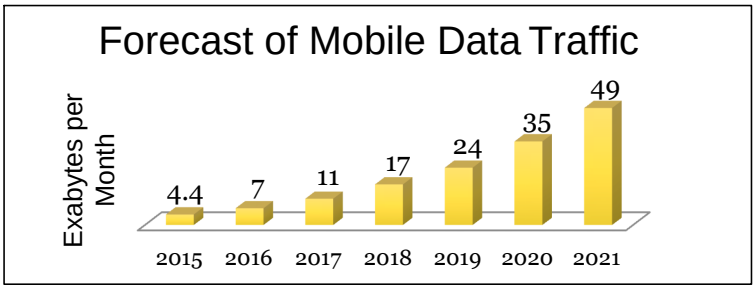


Figure 1.1: The monthly mobile communication data throughput.

1.2 Problem Statement

The improved spectral efficiency provided by OFDM comes at the expense of higher PAPR which in turn leads to lower operating efficiency of PA Fig. 1.2. In order to improve the efficiency of the PA with high PAPR signals, the back-off efficiency has to be increased using back-off efficiency enhancement techniques such as ET or load modulation. Typically, power amplifiers are either designed for broadband operation or high back-off efficiency for signals with high PAPR and a relatively much narrower frequency range. A modern base station needs to support a plethora of frequency bands and two or even three communication standards simultaneously. Initial implantation of base station transceivers used multiple RF front-end paths where each utilized a PA targeting a few bands and standards as illustrated in Fig. 1.3. The most critical block in the RF front-end is the PA due to its relatively high cost and design difficulty due to its nonlinear nature which is often hard to predict and model accurately. The PAs deployed in such applications could be narrowband in which case a high level of redundancy is needed to meet requirements. A solution utilizing redundancy might be acceptable in the case of micro-cell base stations where PAs are operating at low power and the transistors' cost is relatively cheap. However, it is not appealing in the case of macro-cell base stations where the power requirement is much higher driving the cost of each RF path to a significant portion of the base station. On the other hand, lack of support for many bands limits the flexibility of the base station and affects its future proofing. To reduce this redundancy broadband PAs can be utilized in these applications where they cover multiple bands and allow efficient transmission of high PAPR signals. An ideal solution would consist of a single RF path. This would result in a reduction in complexity and space requirements while maintaining flexibility and future proofing [5, 6].

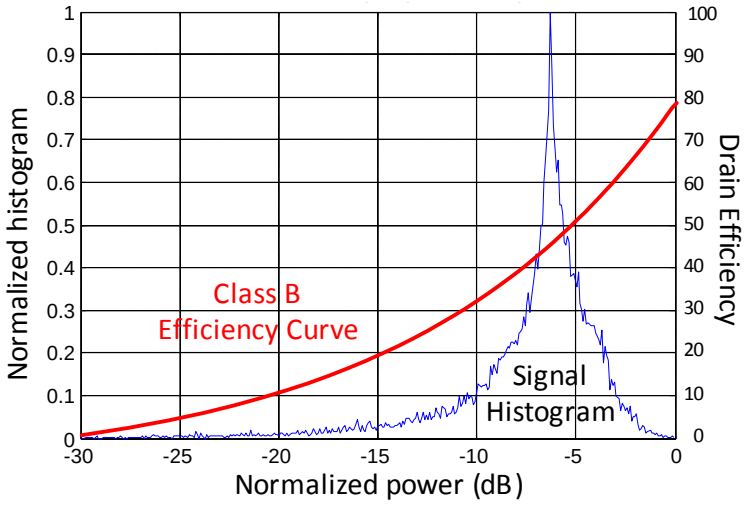


Figure 1.2: Illustration of the histogram of high PAPR signal projected an efficiency plot of a class-B amplifier as a function of normalized power.

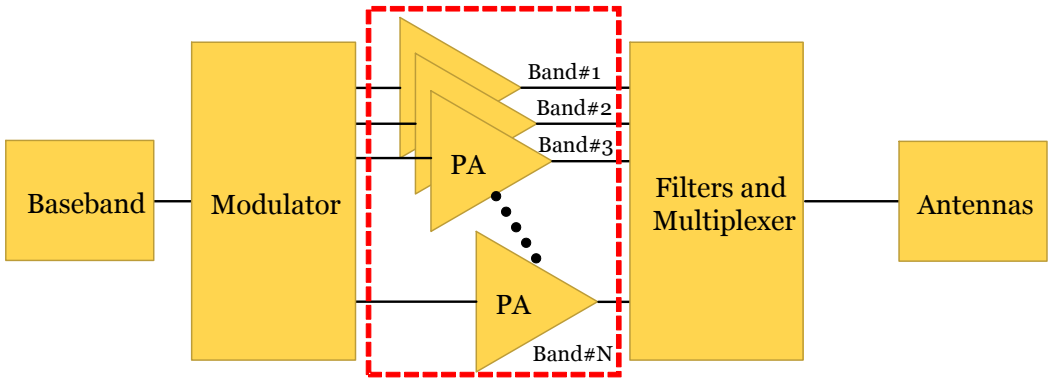


Figure 1.3: Redundant use of PAs to cover multiple bands.

1.3 Methodology

Advances in PA design have lead to significant improvements in bandwidth and efficiency. A broadband high efficiency PA provides a major cost advantage when deploying new infrastructure, as demonstrated in section 1.1. To achieve efficient broadband operation, it was found that the second harmonic termination is of great importance. Hence, the push-pull topology has a significant advantage over traditional implementations as it allows the best

Table 1.1: Mobile communication standards and assigned frequency bands.

Standard	Freq. Bands (MHz)	Channel Bandwidth	Modulation	Avg EIRP (dBm)	Max PAPR	ACPR
GSM	380 − 500 698 − 960 1710−1991	200 KHz	GMSK	33 − 39	∼0	-60 @400 KHz
UMTS	410 − 500 716 − 960 1710−2690	5 − 10 MHz	QPSK, 64 QAM	33	∼3.5 dB	-54 @400 KHz
LTE	698 − 960 1427−2200 2500−2690	5 − 100* MHz	OFDM	23	∼10 dB	-45 @400 KHz

* Aggregated

second harmonic control over a broad bandwidth. The operation of push-pull PAs requires the use of baluns of which there are many variations some of which could be implemented on a typical RF printed circuit board (PCB). On the other hand, to achieve high efficiency at back-off power level, two techniques were identified to have the most relevance to this research which are ET and load modulation. The load modulation technique, known as Doherty, offers the best instantaneous bandwidth and broadband operation of this technique has been investigated in the literature. Few publications pertaining to discrete transistor implementation of back-off efficiency enhancement techniques have addressed using push-pull for better efficiency and bandwidth [7]. Moreover, almost all publications in this area have used a parallel implementation of Doherty which at very high output power requires extremely low output impedance in the range of few Ohms [8]. This low impedance makes it quite challenging to design very high output power broadband DPAs using PCL DPA topology.

This thesis presents a new approach to design very high output power broadband DPAs by increasing the output impedance required at the load. The new approach was able to increase the required load impedance by more than an order of magnitude. Moreover, it allows for much tighter control over second harmonic terminations independently of the fundamental impedance. This flexibility is critical for high efficiency PAs if designed to operate beyond the octave bandwidth. The technique is based on generalized form of SCL Doherty in combination with push-pull transistors. The main applications that could benefit from this are mobile communication base stations and broadcast transmitters. A

prototype demonstrator is successfully designed, tested and linearized under modulated signal conditions.

1.4 Summary of Contributions

This work has produced several contributions of both theoretical and technical nature. The contributions of this work are as follows:

1. Developed a co-design methodology specific to push-pull based PAs which utilizes the baluns as a design parameter. The methodology addresses the design of planar circuits for high power high frequency applications utilizing transistors with significant parasitics. It was found that the traditional design methodology of high power push-pull based PAs causes significant dispersion to the second harmonic termination at frequencies over 1 GHz. This dispersion could place the second harmonic impedance in a low efficiency range. This problem is particularly relevant to broadband PAs. Limiting the dispersion of the second harmonic is achieved by bringing the balun as close as possible to the transistor terminals. However, there are challenges with this approach as the balun has to become an integral part of the design process unlike the traditional modular approach. The co-design methodology addresses this challenge by using the balun as one of the dynamically changeable design parameters. A multi-octave push-pull PA was designed using the developed co-design methodology. During the design of the prototype we have addressed two practical challenges dealing with the package parasitics and bias network. The prototype demonstrated a bandwidth and peak efficiency performance comparable to leading publications in the literature while outputting higher power and utilizing off-the-shelf packaged transistors. This contribution provides a methodology to design broadband PAs with high peak-power efficiency.

2. The methodology is then extended to design broadband DPAs in order to boost the back-off efficiency as well. The output combiner of broadband PCL DPA was investigated in order to incorporate push-pull main and auxiliary transistors. While existing literature demonstrated the incorporation of baluns in the output combiner, they have not placed the balun as close as possible to the transistor to reduce dispersion since they were operating at a relatively lower frequency. Moreover, the balun was fixed during the network synthesis process. The co-design methodology was adapted to broadband PCL DPAs by completely absorbing the package leads into the balun's layout and allowing dynamic balun parameters to vary during the

synthesis of the output combiner. A dual input prototype push-pull Doherty power amplifier (PP-DPA) is then designed to operate over an octave of bandwidth with a 6 dB back-off efficiency greater than 50%.

3. Investigated series-connected-load DPA as a solution for the low load impedance requirements of very high power DPA. The PCL DPA output combiner requires a load impedance (R_L) that is half the optimum impedance of the transistor. At high power R_L can approach 1 Ω which can be extremely challenging to realize over a broadband. The conventional output combiner of SCL DPA requires an R_L that is four times higher than the PCL DPA counterpart. A generalized formulation of the SCL DPA's output combiner is presented which results in an even higher scaling of the required R_L. In addition this formulation provides guidance for output combiner synthesis using the extended co-design methodology for DPAs. A broadband high power SCL DPA with push-pull main and auxiliary transistors is designed with an output impedance which is an order of magnitude higher than the conventional approach. This demonstrated that the load impedance bottleneck can be alleviated using the proposed topology.

1.5 Thesis Outline

This thesis is organized as follows. Chapter 2 will outline the theory behind conventional power amplifier design illustrating the differences between different classes of operation. Broadband operation will be explained through the introduction of the design space concept and class-B/J. Then, the push-pull topology will be presented as the topology most suited to design broadband and high efficiency amplifiers. Several balun topologies will be analyzed and compared in terms of suitability to this work. Finally, an overview of existing back-off efficiency enhancement techniques such as load and drain modulation techniques is provided.

In chapter 3, a co-design methodology for designing broadband high efficiency push-pull based PAs using packaged off-the-shelf transistors and planar baluns will be presented. The chapter starts by discussing the limitation of current implementations of push-pull in litrature. It then proposes a new methodology with multiple improvements in order to optimize the performance of push-pull based PAs. This methodology is used to design a multi-octave push-pull power amplifier (PPPA) and an octave bandwidth PP-DPA.

In chapter 4, a new approach for designing broadband high power DPA is proposed. It starts with a generic SCL DPA architecture to derive the equations that relate its com-

biner's ABCD parameters to the transistor's optimum impedance and load impedance. These equations feature the possibility of significantly increasing the load impedance in SCL DPA compared to the more popular PCL DPA architecture. The design of a prototype broadband SCL DPA with push-pull main and auxiliary amplifiers demonstrator is discussed in this chapter. It is also shown that the demonstrator can be linearized under modulated signal conditions using practical signal stimuli.

In chapter 5 the contributions of this work are outlined and possible future research work is discussed.

Chapter 2

Broadband Power Amplifiers and Efficiency Enhancement Techniques

2.1 Introduction

This chapter will outline the theory behind conventional PA design illustrating the differences between classes of operation. An ideal transistor model will be used to explain a simplified design methodology showing how the bias voltage and load termination affects the amplifier performance. The broadband operation will be explained through the introduction of the design space concept. class-B/J use the design space concept to extend the possible range of impedances that provide a theoretically identical performance to the conventional class-B PA. The push-pull topology will be presented as the topology best suited to design high-efficiency amplifiers with over an octave of bandwidth. In non-complimentary transistor technology, push-pull topology relies on the use of baluns. Therefore, the most popular balun topologies will be presented and analyzed for suitability. Finally, an overview of existing back-off efficiency enhancement techniques such as load and drain modulation techniques is provided.

2.2 Ideal Transistor Model

In this chapter, we will use an ideal linear transistor model to illustrate the various power amplifier classes and topologies mentioned in the previous section. The ideal transistor shown in Fig. 2.1 consists of a linear voltage controlled current source with V_{gs} as the

input voltage and I_{ds} as the output current. The current source operates linearly with input voltage levels above the pinch-off voltage V_p and below the saturation voltage as shown in Fig. 2.2a. Moreover, the current source requires a positive voltage higher than the knee voltage V_k and lower than the breakdown voltage applied to its drain terminal. In this chapter V_k will be assumed to be equal to zero volts to simplify the analysis. The DC-IV characteristics are shown in Fig. 2.2b. The following simplified analysis assumes no parasitic elements associated with the transistor. This assumption is valid in the context of illustrating the basic operation of various classes. The DC component of voltages and currents will be distinguished by capital letter subscripts and an average bar over the term while the AC or RF terms will have small letter subscripts. The terms with capital letter subscripts and no average bar denote the total signal.

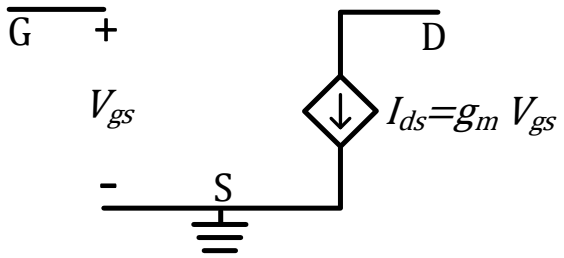


Figure 2.1: The ideal FET model.

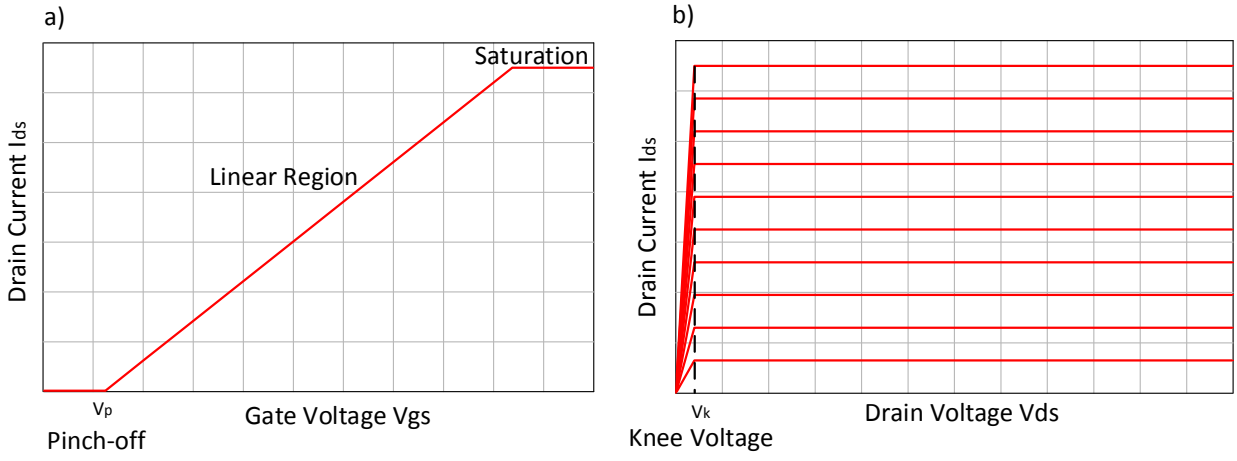


Figure 2.2: The characteristics of the ideal linear transistor model a) V_{gs} to I_{ds} transfer characteristic b) I_{ds} vs. V_{ds} for varying V_{gs}.

2.3 Conventional Power Amplifier Classes

2.3.1 Class-A

Class-A is the simplest class of operation of power amplifiers and is usually used as a benchmark for other classes. Class-A is biased such that the DC component of I_{DS} denoted by ($\overline{I_{DS}}$) is half the maximum current that can be provided by the transistor. On the other hand, the drain DC voltage is set as the average of the knee voltage and break down voltage. The input voltage is allowed to swing strictly between the pinch-off voltage and the saturation voltage while the output voltage is allowed to swing between the knee voltage and the breakdown voltage. The maximum power is achieved by aligning the maximum swing at the input with the maximum swing at the output using the proper output resistance denoted as R_{opt} [9]. Fig. 2.3 shows the relationship between input and output voltages. The slope of the AC load line is set by the value of the load impedance and for maximum output power the value of the load impedance R_{opt} is given by,

$$R_{opt} = \frac{V_{max}}{I_{max}} = \frac{2(\overline{V_{DS}})}{2(\overline{I_{DS}})} = \frac{\overline{V_{DS}}}{\overline{I_{DS}}}. \tag{2.1}$$

For this case the maximum output power will be,

$$max(P_{out}) = \frac{1}{2}\overline{V_{DS}}\,\overline{I_{DS}} = 1/8 V_{max} I_{max}. \tag{2.2}$$

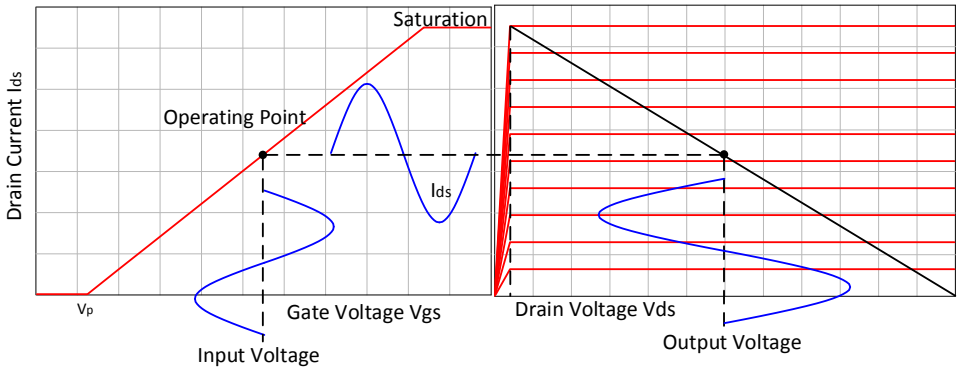


Figure 2.3: The relationship between input and output waveforms of class-A power amplifiers.

One of the important metrics in power amplifier design is the efficiency. The efficiency of a power amplifier is the measure of how good it is in converting DC power into AC power and is measured as the ratio between output RF power and input DC power. There are two major ways to define an amplifier's efficiency and they are namely the drain efficiency and the power added efficiency (PAE). The two terms are related to each other such that the PAE is always less than the drain efficiency (DE) because it subtracts the input RF power from the output RF power. The two measures are illustrated in equations 2.3 and 2.4,

$$DE = \frac{[P_{out}]_{RF}}{[P_{in}]_{DC}} 100\%, \tag{2.3}$$

$$PAE = \frac{[P_{out}]_{RF} - [P_{in}]_{RF}}{[P_{in}]_{DC}} 100\%. \tag{2.4}$$

In the case of class-A operation the maximum efficiency happens at maximum output power and is computed as follows,

$$DE = \frac{[P_{out}]_{RF}}{[P_{in}]_{DC}} 100\% = \frac{1}{2}\frac{\overline{V_{DS}}\,\overline{I_{DS}}}{\overline{V_{DS}}\,\overline{I_{DS}}} 100\% = 50\%. \tag{2.5}$$

Since the maximum theoretical efficiency for class-A does not exceed 50%, it is not used for high efficiency applications. However, class-A provides the best linearity. The definition of linearity varies based on context and in the case of power amplifiers it is defined by the relationship between input fundamental power and output fundamental real power. Linear power amplifiers do not produce any intermodulation products in theory. However, in practice there is always non-linearity present. Therefore, the term "linear" is used loosely to describe a state of acceptable non-linearity. The level of non-linearity is well defined for standardised communication applications through organizations such as 3rd generation partnership project (3GPP). Due to the relatively good linearity of class-A, it is still used in some applications where the signal quality is critical such as in pre-amplifiers [9].

2.3.2 Class-B

As mentioned previously class-A amplifiers are biased such that DC power is dissipated even if there is no input. Class-B amplifiers are biased with a gate voltage at pinch-off such that the transistor is not dissipating any current in the absence of an input signal, i.e., $\overline{I_{DS}}$ is zero. The drain voltage $\overline{V_{DS}}$, however, is biased midway between the maximum

voltage and the knee voltage, just as in class-A. The AC load-line is different than that of class-A but it leads to the same maximum output power. The relationship between input and output signals is shown in Fig. 2.4 [9].

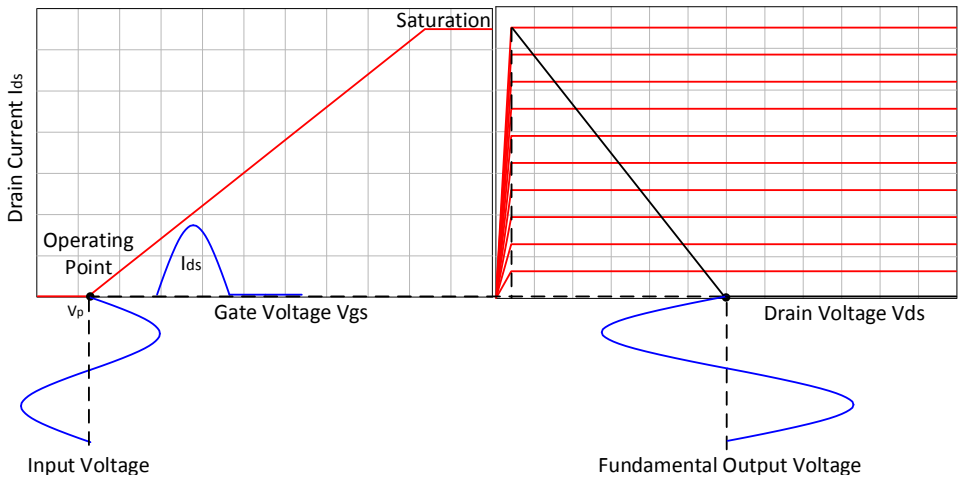


Figure 2.4: The relationship between input and output waveforms of class-B power amplifiers.

Even though the maximum output power is the same as that of class-A, class-B PA need to be driven with two times the voltage. For a fixed input impedance that translates into four times as much input power to produce the same output power as a class-A PA. Based on that, the power gain of class-B PA is one quarter that of class-A PA. Note that power gain (G) of a PA is defined as follows,

$$G = \frac{[P_{out}]_{RF}}{[P_{in}]_{RF}}. \tag{2.6}$$

For a proper class-B operation, higher-order harmonics have to be shorted out in order to get maximum voltage swing over the fundamental frequency to produce the maximum output power at the fundamental frequency. This shorting of harmonics will lead to bandwidth limitations as will be discussed in later sections. From the waveform of the current I_{DS} we can deduce the DC, fundamental and harmonic content using Fourier series expansion. By taking Fourier transform of the half sinusoid we get the following,

$$\overline{I_{DS}} = \frac{1}{2\pi} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \frac{I_{max}}{1 - cos(\frac{\pi}{2})} [cos(\theta) - cos(\frac{\pi}{2})] d\theta, \tag{2.7}$$

$$I_{ds}^{n} = \frac{1}{\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \frac{I_{max}}{1-cos(\frac{\pi}{2})}[cos(\theta) - cos(\frac{\pi}{2})]cos(n\theta)d\theta, \tag{2.8}$$

where, I_{ds}^{n} denotes the current amplitude of the nth harmonic. Note that the signal is assumed to be symmetric around the y-axis hence it does not contain any sine terms and it purely consist of cosine terms given that the function is even. If the function was not even then we would require an additional term to describe the signal fully. The DC component can be written in terms of I_{max} as,

$$\overline{I_{DS}} = \frac{1}{\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \frac{I_{max}}{1-cos(\frac{\pi}{2})}[cos(\theta) - cos(\frac{\pi}{2})]d\theta = \frac{I_{max}}{\pi}\ A, \tag{2.9}$$

while the amplitude of the fundamental can be written as,

$$I_{ds}^{1} = \frac{1}{\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \frac{I_{max}}{1-cos(\frac{\pi}{2})}[cos(\theta) - cos(\frac{\pi}{2})]cos(\theta)d\theta = \frac{I_{max}}{2\pi}\ A. \tag{2.10}$$

The efficiency of class-B is computed by writing everything in terms of I_{max} and V_{max} as follows,

$$DE = \frac{[P_{out}]_{RF}}{[P_{in}]_{DC}}\,100\% = \frac{\frac{1}{2}\frac{V_{max}}{2}\frac{I_{max}}{2}}{\frac{V_{max}}{2}\ \frac{I_{max}}{\pi}}\,100\% = \frac{\pi}{4}\,100\% = 78.5\%. \tag{2.11}$$

Therefore, 78.5% is the maximum efficiency of a class-B PA with the assumed knee voltage of zero volts. The maximum output power which also corresponds to the maximum drain efficiency is given by,

$$[P_{out}]_{RF} = \frac{1}{2}\,\frac{I_{max}}{2} \times \overline{V_{DS}}. \tag{2.12}$$

Class-B power amplifiers are considered linear in terms of input and output power levels. This is in contrast to other classes with a conduction angle less than 2π that can be found in literature. As mentioned in the previous section linearity in power amplifiers is not based on voltage and current waveforms but is based on the relationship between input and output real power levels at the fundamental frequency. Even though class-B operation produces harmonic content due to the fact that the current is half a sinusoid, it does not produce any intermodulation products unless the amplifier saturates and enters the knee region. However, in practice there are other non-idealities in the transistor, such as soft turn-on voltage and nonlinear g_m, which forces class-B to behave non-linearly [9].

2.3.3 Class-AB

It was shown in the earlier section that by biasing the gate of the transistor exactly at pinch-off the maximum efficiency was enhanced beyond the 50% limit of class-A. One might conclude that there should be a class of operation between class-A and class-B where the gate is biased between those classes. Such a class is referred to as class-AB. In practice, class-AB biasing is a way to compromise between the efficiency of class-B and the linearity and gain of class-A. As explained earlier, class-B is nonlinear due to non-idealities of the transistor including the soft turn-on voltage. In class-AB the non-linearity is reduced by biasing the gate away from the pinch-off voltage, thus avoiding the non-linearity due to the soft turn-on of the transistor. In order to explain the operation of class-AB we need to explain the concept of conduction angle. The conduction angle (α) refers to the portion of the signal where the amplifier is turned on and conducting power. For instance, in class-A the conduction angle is 2p since the amplifier is ON during the complete cycle of the input signal. In class-B, however, the conduction angle is π since the transistor is ON only for the positive half of the sinusoidal signal. The drain current waveform can be written in terms of the conduction angle as follows [9],

$$I_{DS} = \begin{cases} \frac{I_{max}}{1-cos(\frac{\pi}{2})}[cos(\theta) - cos(\frac{\pi}{2})] & -\frac{\alpha}{2} \leq \theta \leq \frac{\alpha}{2} \\ 0 & Otherwise \end{cases}. \tag{2.13}$$

The comparison between the drain current waveforms of class-A, class-B and class-AB is shown in Fig. 2.5

Based on the general term of the drain current we can deduce the DC and AC content using Fourier series expansion as given by,

$$\overline{I_{DS}} = \frac{1}{\pi}\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} \frac{I_{max}}{1-cos(\frac{\alpha}{2})}[cos(\theta) - cos(\frac{\alpha}{2})]d\theta, \tag{2.14}$$

$$I_{ds}^{n} = \frac{1}{\pi}\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} \frac{I_{max}}{1-cos(\frac{\alpha}{2})}[cos(\theta) - cos(\frac{\alpha}{2})]cos(n\theta)d\theta. \tag{2.15}$$

From Equations 2.14 and 2.15 we can deduce the maximum output power, gain and efficiency. The maximum power of class-AB is higher than that of class-A. This can be explained by looking at the magnitude of the fundamental component of I_{DS} normalized to that of class-A. Note that the voltage does not have any harmonics aside from the

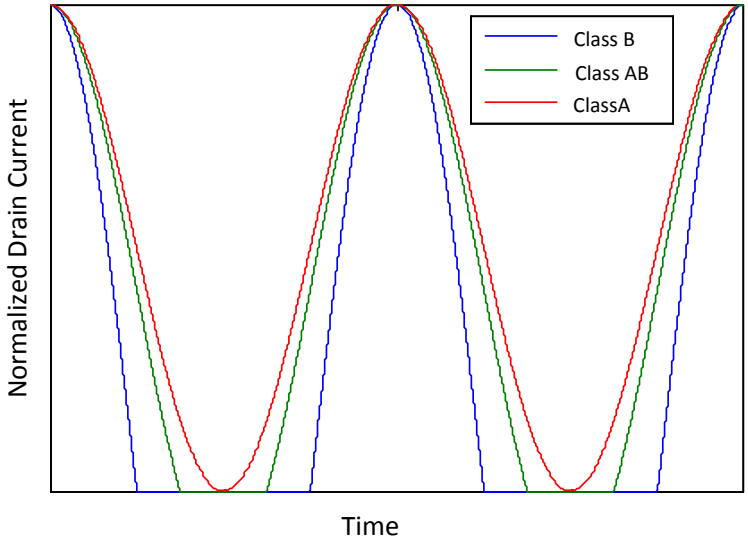


Figure 2.5: The comparison between the current waveforms of class-A, class-B and class-AB.

fundamental since the load is forced to be a short-circuit for all harmonics. The relationship between the fundamental current component and conduction angle is shown in Fig. 2.6.

Since the voltage swing is designed to be identical to that of class-A then the increase in fundamental current will reflect to an increase in output power. The maximum output power happens at a conduction angle of α=4.28 rad. The normalized linear power gain is also a function of the conduction angle and is given by,

$$G = \frac{[P_{out}]_{RF}}{[P_{in}]_{RF}} = \frac{[P_{out}]_{RF}^{class-A} \frac{1}{\pi} \int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} \frac{2}{1-cos(\frac{\alpha}{2})}[cos(\theta) - cos(\frac{\alpha}{2})]cos(\theta)d\theta}{[P_{in}]_{RF}^{class-A}(\frac{2}{1-cos(\frac{\alpha}{2})})^2}. \tag{2.16}$$

The efficiency is then computed based on the conduction angle at maximum power assuming all higher-order harmonics are short-circuited and V_{DS} is at full swing,

$$DE = \frac{[P_{out}]_{RF}}{[P_{in}]_{DC}} 100\% = \frac{\frac{1}{2}\frac{V_{max}}{2}\frac{1}{\pi}\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} \frac{I_{max}}{1-cos(\frac{\alpha}{2})}[cos(\theta) - cos(\frac{\alpha}{2})]cos(\theta)d\theta}{\frac{V_{max}}{2}\frac{1}{\pi}\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} \frac{I_{max}}{1-cos(\frac{\alpha}{2})}[cos(\theta) - cos(\frac{\alpha}{2})]d\theta} 100\%, \tag{2.17}$$

$$DE = \frac{\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}}[cos(\theta) - cos(\frac{\alpha}{2})]cos(\theta)d\theta}{\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}}[cos(\theta) - cos(\frac{\alpha}{2})]d\theta} 100\%. \tag{2.18}$$

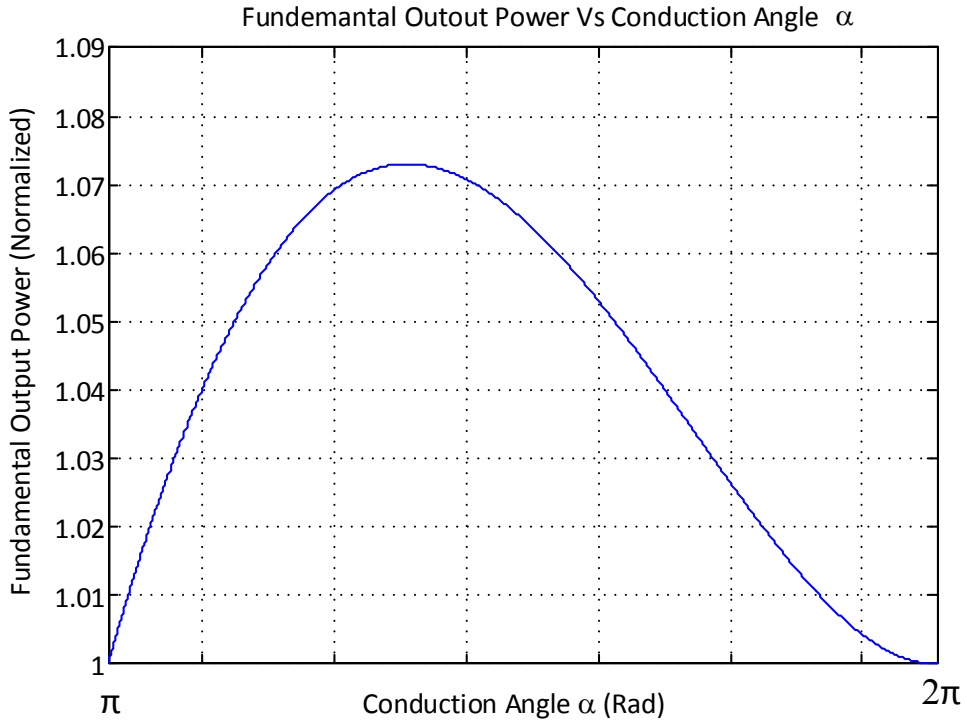


Figure 2.6: The normalized fundamental component of the output power given as a function of the conduction angle α in radians.

Fig. 2.7 shows the efficiency and gain of class-AB vs. the conduction angle. Note that the gain is normalized relative to class-A.

As mentioned before class-B is considered theoretically linear when assuming and ideal transistor model. Under the same assumption, class-AB is not linear for all power levels. The reason being that for every input power the conduction angle is prone to change depending on the bias voltages and currents. From Fig. 2.7 we can see that if the conduction angle changes the gain also changes leading to a nonlinear relationship between the input and output fundamental powers. Yet in practice, class-AB is more linear than class-B power amplifiers and there is no proper way to illustrate this using an ideal transistor model since the major contributor is the nonlinear device characteristics that are technology dependent [9].

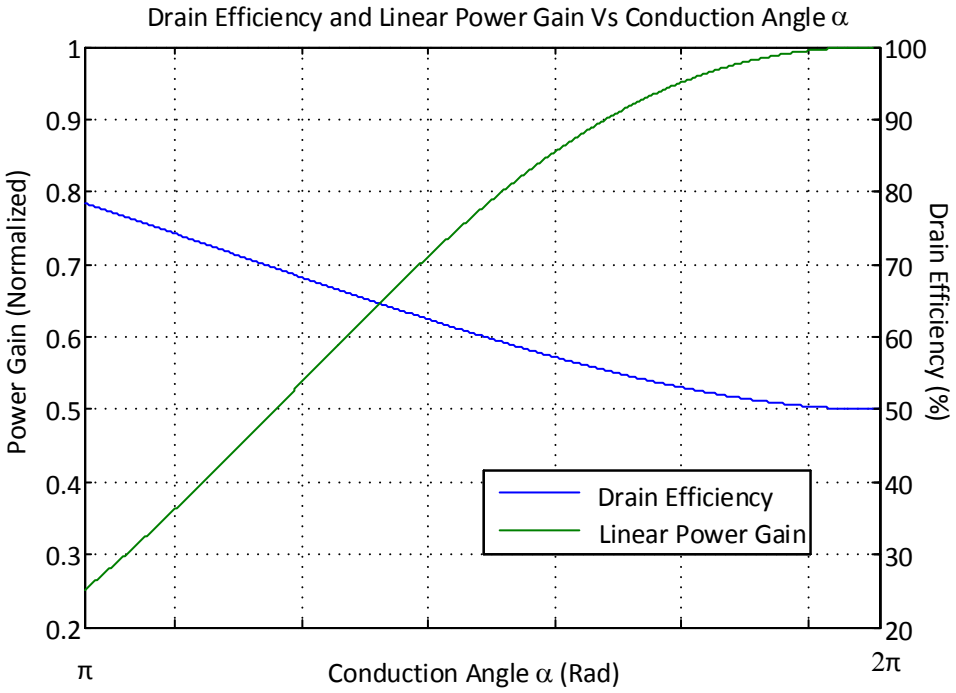


Figure 2.7: The Drain Efficiency and normalized power gain of class-AB vs. the conduction angle.

2.3.4 Class-C

Amplifiers biased in class-B or class-AB operate in a mode known as reduced conduction angle mode. Another variation on reduced conduction angle mode is class-C power amplifiers. Class-C has a gate bias voltage below the pinch-off voltage to further increase the ratio of the fundamental component to the DC component of I_{DS} hence increasing the efficiency of the power amplifier. The conduction angle of class-C is below π which means that the transistor does not conduct energy for more than half the time. Equations 2.14 and 2.15 introduced in the previous subsection apply for all values of α and can be used to plot the output power, gain and efficiency equations for class-C as shown in Fig. 2.8.

Regardless of the potential high efficiency of class-C, it suffers from major drawbacks. This class of operation is highly nonlinear and it does not amplify any signal below a certain threshold usually decided by the gate's bias voltage. The maximum output power is lower than that of class-A and the gain declines rapidly rendering the amplifier unusable at very low conduction angles.

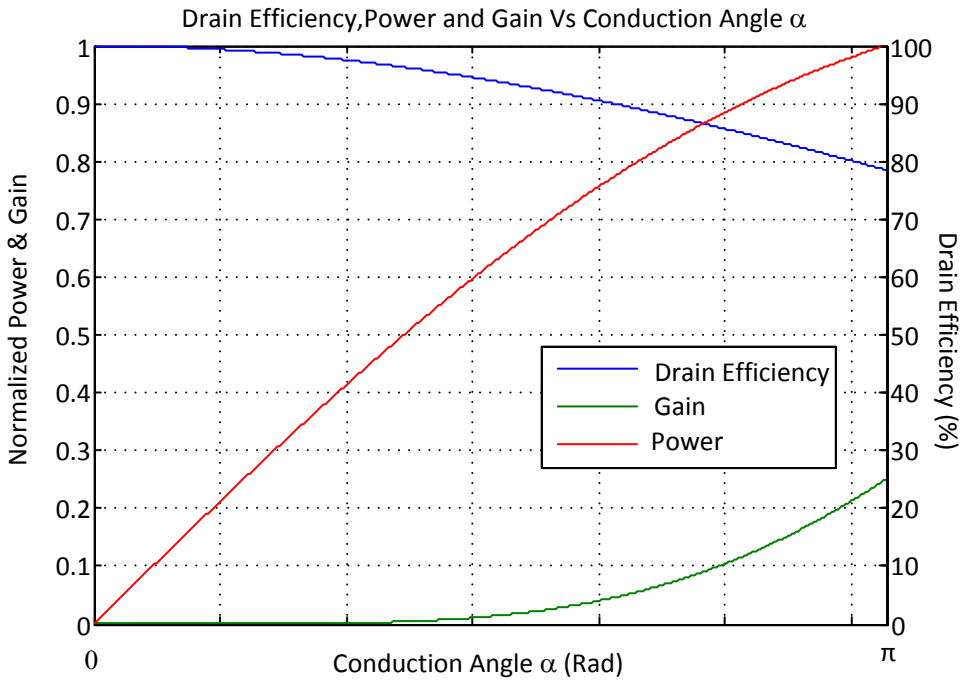


Figure 2.8: The drain efficiency, normalized output power and normalized Gain as a function of the conduction angle α.

2.4 Broadband Power amplifiers

2.4.1 Class-B/J

Conventional class-B power amplifier requires a short-circuit termination for all the higher-order harmonics. However, most practical class-B amplifiers focus only on terminating the second harmonic with a short-circuit, ignoring the higher-order harmonics. In broadband power amplifiers, a broadband short-circuit for the second harmonic limits the bandwidth of operation since providing a broadband short-circuit is very challenging for frequencies higher than 1 GHz. In order to study the sensitivity of class-B to the short-circuit termination the following experiment was performed. The fundamental impedance was kept constant at R_{opt} while the phase of the second harmonic termination was varied as shown in Fig. 2.9. It was evident that the efficiency will degrade for the same input power as the second harmonic termination shifts into other loads Fig. 2.10. The reason was attributed to the fact that the voltage is then forced beyond the knee region and the current

is significantly reduced as a result Fig. 2.11.

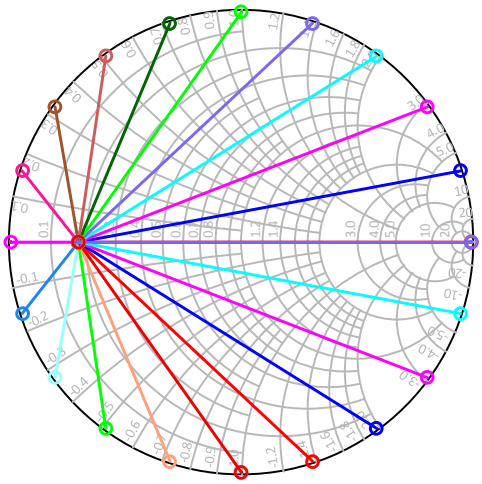


Figure 2.9: Swept second harmonic Termination with fixed Fundamental impedance at R_{opt}.

This reduction in current reduces the magnitude of the fundamental component reducing the gain and efficiency. However, by overdriving the transistor recovering some of output power and efficiency is possible at the cost of linearity degradation. If entering the knee region can be remedied by modifying a certain parameter then it is possible to preserve the high efficiency performance of class-B even when the second harmonic termination is not a short-circuit anymore. Researchers found that by changing the fundamental impedance it is possible to phase shift the voltage waveform such that the low voltage that used to push the device into the knee region coincides with a low current value to avoid a dip in current. A mathematical expression was derived to link the waveforms with the fundamental and second harmonic impedances and the design space concept was therefore conceived.

It was shown in literature that a short-circuit harmonic termination is not a unique solution for class-B operation [10] and a new class of operation was introduced. The new class of operation presented the design space concept to expand the set of possible combinations under which the efficiency is maintained. This class of operation is referred to as class-B/J. Class-B/J, unlike other classes of operation, requires a complex fundamental load impedance and is not restricted to any specific load impedance for neither the fundamental nor the second harmonic. The current waveform for this class-is always a half sine

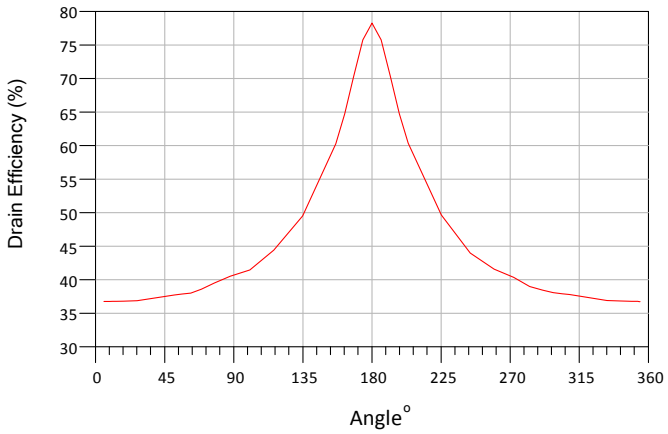


Figure 2.10: Drain Efficiency as a function of the angle of the second harmonic termination.

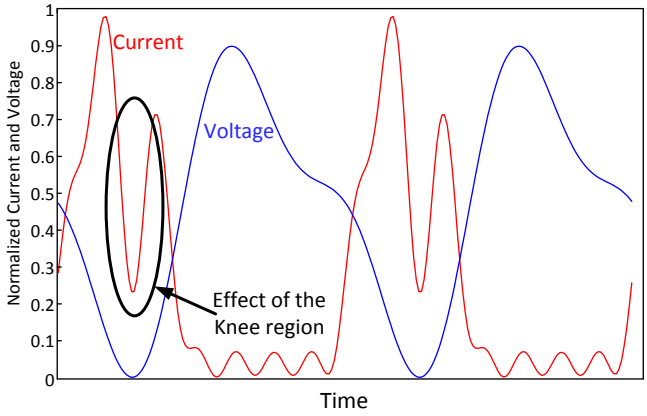


Figure 2.11: Example of a poorly terminated second harmonic shows the distorted current waveform as the transistor operates in the knee region.

wave while the voltage waveform has the following expression,

$$V_{DS} = \overline{V_{DS}}(1 - cos(\theta))(1 - \gamma sin(\theta)) \quad -1 \leq \gamma \leq 1. \tag{2.19}$$

The waveform can be visualized for various values of γ as shown in Fig. 2.12. Note that class-B operation occurs at $\alpha = 0$. The pairing between the fundamental and second harmonic terminations is shows in Fig. 2.13.

One of the drawbacks of class-B/J is the fact that the voltage can reach values as high as three times the bias voltage $\overline{V_{DS}}$ which makes this class of operation unsuitable for low

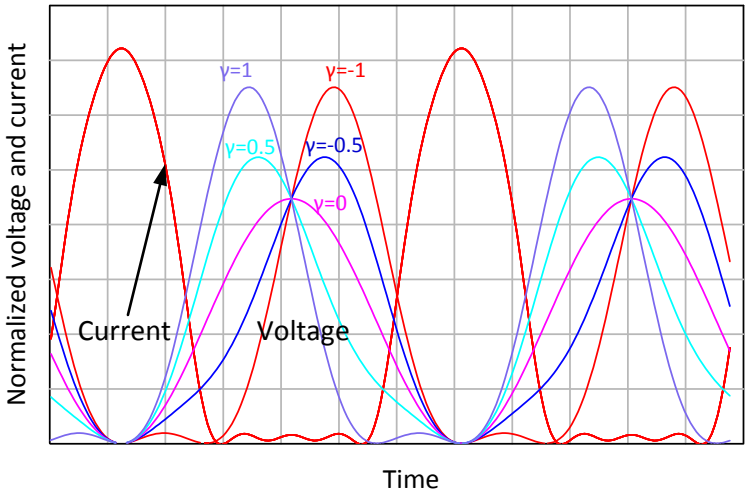


Figure 2.12: Current and Voltage waveforms of Class-B/J for various values of γ.

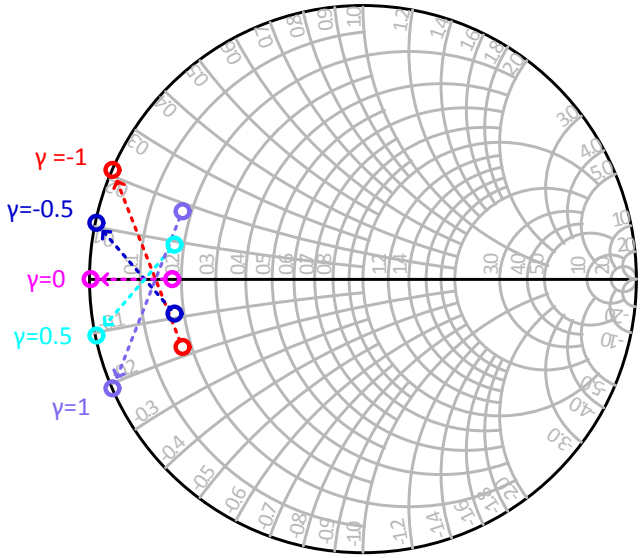


Figure 2.13: The pairing between fundamental and second harmonic terminations of Ideal class-B/J.

breakdown voltage devices. The power and efficiency performance is identical to that of class-B power amplifiers. The theoretical limitation of class-B/J lay in having a maximum bandwidth of a single octave when implemented according to the theory. Such limitation

arises due to having to terminate the second harmonic at the edge of the Smith chart with a reactive load rendering the frequencies unusable for real power transmission.

2.4.2 Push-Pull Topology

As explained earlier there is a theoretical bandwidth limitation on class-B/J power amplifiers. The push-pull topology does not have such limitation as it isolates the load termination of the second harmonic from that of the fundamental impedance. When implementing the push-pull topology along with class-B/J it is theoretically possible to achieve high efficiency broadband designs that exceed the an octave bandwidth. Fig. 2.14 shows a simplified diagram for push-pull amplifier topology.

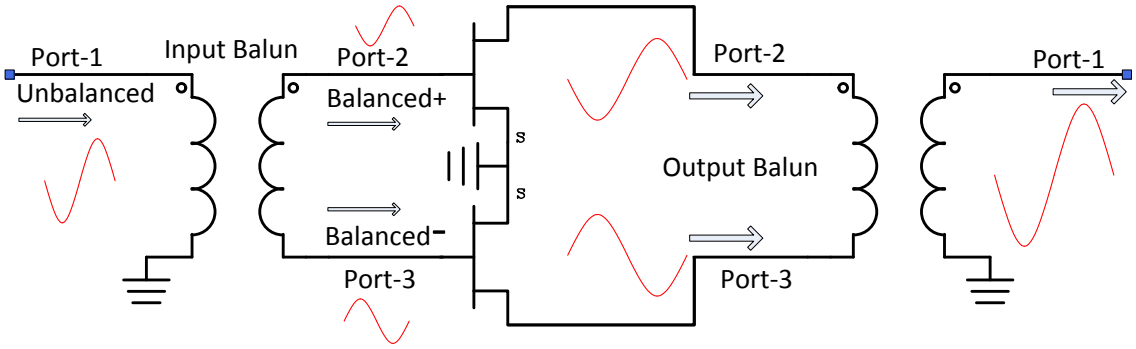


Figure 2.14: A simplified push-pull power amplifier schematic.

The main element in push-pull amplifiers is the anti-phase power combiner which is also known as balanced to unbalanced (balun) transformer. Baluns will be discussed in further details in the third chapter. However, there are several notes that must be pointed out in this section.

- Baluns behave differently under two modes of operation, namely the odd-mode and even-mode.
- High-frequency baluns behave differently than low frequency counterparts and most of the low frequency analysis does not apply to RF baluns.
- Baluns can be isolated or non-isolated. The isolated baluns have matched even-mode impedance. The non-isolated baluns have a purely reactive even-mode impedance.

- Baluns can incorporate an impedance transformation ratio that can be used in the input and output matching circuits.

It is worth noting that the input side of the push-pull power amplifier does not need a balun and can be fed directly through a DAC. The main purpose of the balun, in the context of PPPA, is to isolate the fundamental impedance from the even-mode harmonic impedances. When driving two transistors with anti-phased signals the output's fundamental will be out of phase while the output's even order harmonics will be in phase with each other. When using a balun as a power combiner then only the signals with opposite phases will be passed through to the load side while the in-phase counterparts will be rejected and terminated with a short, reactive or an open-circuit load.

2.5 Baluns

"[A] balun is a network for the transformation from an unbalanced transmission line, system or device to a balanced line, system or device. Baluns are also used for impedance transformation. [The term balun is] derived from balanced to unbalanced" [11]. Baluns can be implemented in several ways in practice. They are used as antenna feeds, inputs to differential circuits, anti-phase power combiners/splitters, transformers between transmission line types, etc. Most baluns are passive constructs. However, an amplifier that takes a single ended input and outputs a differential signal can be referred to as an active balun. This and other known structures such as the 180^o hybrid and a voltage transformer can be employed as baluns.

2.5.1 An Ideal Balun

In this thesis an ideal balun will be thought of as an ideal three ports transformer as shown in Fig. 2.15. The S-parameters for the ideal transformer balun are given by,

$$S = \begin{bmatrix} \frac{1-2T^2}{1+2T^2} & \frac{2T^2}{1+2T} & \frac{-2T^2}{1+2T} \\ \frac{2T^2}{1+2T^2} & \frac{1}{1+2T^2} & \frac{2T^2}{1+2T^2} \\ \frac{-2T}{1+2T^2} & \frac{2T^2}{1+2T^2} & \frac{1}{1+2T^2} \end{bmatrix}.$$

In the case of 50 Ohms at all ports, the transformation ratio (T) of the transformer for the ideal balun model adopted in this work is,

$$T = \frac{1}{\sqrt{2}}. \tag{2.20}$$

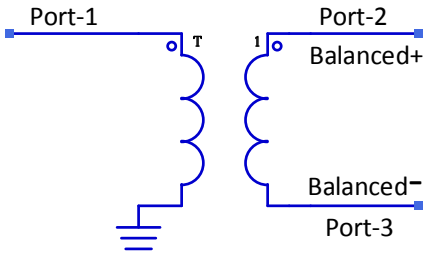


Figure 2.15: The ideal transformer employed as an ideal current balun.

For this value of T the balun will be matched at port 1 and the balun will be acting as an anti-phase power splitter for 50 Ω reference impedance at all ports with the following S-parameters,

$$S = \begin{bmatrix} 0 & \frac{1}{\sqrt{2}} & \frac{-1}{\sqrt{2}} \\ \frac{1}{\sqrt{2}} & \frac{1}{2} & \frac{1}{2} \\ \frac{-1}{\sqrt{2}} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}. \tag{2.21}$$

According to microwave theory, it is impossible to have a lossless, matched and reciprocal three port device [12]. Since the ideal balun is lossless and reciprocal then it must be unmatched at all or some of the ports. It can be noted from 2.21 that ports 2 and 3 are unmatched and non-isolated. However, under certain conditions these ports can behave as matched ports. To understand how a balun operates we must look at two operating modes which are the odd-mode and even-mode. When operating in odd-mode the balun combines the power coming from ports 2 and 3 and output them at port 1 Fig. 2.16. The impedance seen by terminals 2 and 3 in this mode is denoted by Z_{odd} and is given by 2.22 and is a function of the transformation ratio.

$$Z_{odd} = \frac{Z_o}{2T^2}. \tag{2.22}$$

When the balun is operating under even-mode conditions, Fig. 2.17, the power is completely reflected from ports 2 and 3 and the impedance seen at these ports is an open-circuit. A more general formulation which describes the reflection coefficient at the balanced ports in each mode when the unbalanced port is terminated by the characteristic impedance Z_o is given by,

$$S_{Odd} = \frac{1}{2}(S(2,2) - S(2,3) - S(3,2) + S(3,3)), \tag{2.23}$$

$$S_{Even} = \frac{1}{2}(S(2,2) + S(2,3) + S(3,2) + S(3,3)). \tag{2.24}$$

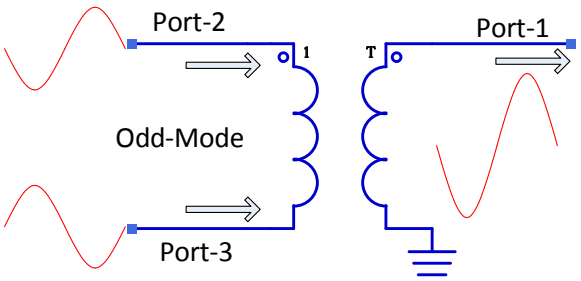


Figure 2.16: Odd-mode behavior of an ideal transformer-based balun.

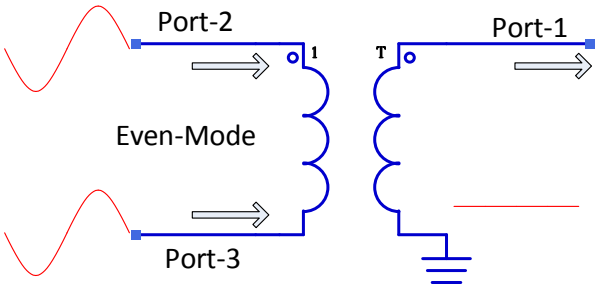


Figure 2.17: Even-mode behavior of an ideal transformer-based balun.

2.5.2 RF Balun Topologies

180^o Hybrid Couplers

A coupler can be used as an anti-phase power splitter behaving as a balun in some applications. Several researchers have reported this concept in literature and implemented baluns using modified 4-port networks terminated with a short, open or matched load at the unused port [13] and [14]. It is important to note that terminating with a short, open or a matched load results in a different behaviour and one should be aware of the difference in certain applications. To elaborate we need to recall the fact that three port networks cannot be matched, lossless, and reciprocal all at the same time. The Rat-Race hybrid coupler shown in Fig. 2.18 will be used as an example and it has the following S-parameters,

$$S = \frac{-j}{\sqrt{2}} \begin{bmatrix} 0 & 1 & 0 & -1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ -1 & 0 & 1 & 0 \end{bmatrix}.$$

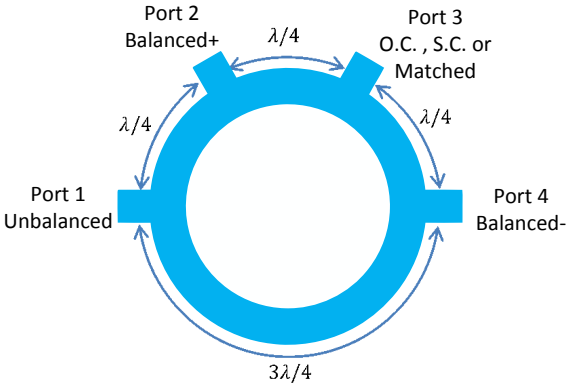


Figure 2.18: A 180^o hybrid coupler employed as balun by terminating port 3 with short-circuit, open-circuit or matched load.

From the S-parameters we can deduce that if power is incident on port 1 then ports 2 and 4 produce anti-phase signals while port 3 is considered isolated from port 1 as it receives nothing. If we chose to terminate port 3 with a matched load then the result will be a three port device that acts as an anti-phase power splitter with all ports matched and reciprocal. The resultant network has the following S-parameters,

$$S = \frac{-j}{\sqrt{2}} \begin{bmatrix} 0 & 1 & -1 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \end{bmatrix}.$$

As stated before, the resultant 3-port network cannot be lossless and this shows when we have two signals in phase incident at ports 2 and 4 (even-mode). In this scenario the input power is completely dissipated in the matched load at port 3 and there will be no output power at any of the other ports. The fact that ports 2 and 4 are isolated when port 3 is matched caused this response. Such a configuration is not suitable to be used at the output of push-pull amplifiers operating under class-B/J since the second harmonic is incident at ports 2 and 4 in phase and will be absorbed and dissipated into the matched load at port 3 reducing the efficiency of the amplifier. If the matched load at port 3 was replaced with a

short-circuit then the network will stay lossless and reciprocal. However, it will not remain matched anymore and will have the following S-parameters,

$$S = \frac{-j}{\sqrt{2}} \begin{bmatrix} 0 & 1 & -1 \\ 1 & \frac{j}{\sqrt{2}} & \frac{j}{\sqrt{2}} \\ -1 & \frac{j}{\sqrt{2}} & \frac{j}{\sqrt{2}} \end{bmatrix}.$$

The difference between the isolated balun and non-isolated lay mainly in the even-mode behavior. In fact, the odd-mode in both cases (matched and shorted) is identical. The even-mode in this configuration is presented with an open-circuit just like an ideal transformer balun this conclusion can be reached using 2.24. Similarly, when terminating port 3 in the rat-race coupler with an open-circuit, the even-mode impedance becomes a short-circuit instead. We need to note that having no isolation in baluns is important in some applications especially in push-pull amplifiers. For instance, class-B/J push-pull PA requires a purely reactive second harmonic impedance (i.e., even-mode impedance) which is the case in non-isolated baluns.

Guanella

The Guanella balun was first reported in 1944 in a paper titled "New Method of Impedance Matching in Radio-Frequency Circuits" [15]. The Guanella balun has several forms. The ideal Guanella is presented with an ideal transformer connected as shown in Fig. 2.19. The RF variation of Guanella can be modeled as a coupled line instead of the transformer Fig. 2.20. The transformation ratio of this topology is 1:1. This means if the termination at port 1 is 50 Ohms, then the balanced terminals need to be terminated by 25 Ohms each.

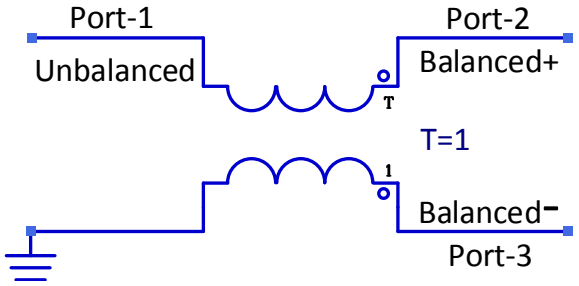


Figure 2.19: The ideal Guanella model based on the ideal transformer.

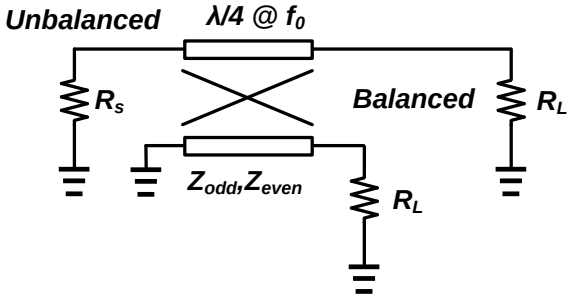


Figure 2.20: The ideal Guanella model based on the coupled line model.

The ideal high frequency distributed element Guanella equivalent is a coupled line with a unity coupling coefficient (K),

$$K = \frac{Z_{even} - Z_{odd}}{Z_{even} + Z_{odd}}, \tag{2.25}$$

where Z_{odd} and Z_{even} are the odd- and even-mode impedances of the coupled line respectively. In practice, unity coupling coefficient is unrealizable. However, high coupling coefficients are possible but depends on the fabrication process and the design to be implemented. The even-mode impedance needs to be as high as possible to increase the coupling coefficient as close as possible to unity. The higher the coupling coefficient of the balun the better the balance. The balance is defined by two measures namely the magnitude imbalance and the phase imbalance. Magnitude and phase imbalance are given by 2.26 and 2.27 respectively.

$$Magnitude\ Imbalance = \frac{|S_{21}|}{|S_{31}|}, \tag{2.26}$$

$$Phase\ Imbalance = \angle\frac{S_{21}}{S_{31}}. \tag{2.27}$$

For a coupling coefficient of $K = 0.7778$, it is possible to have the following Guanella balun performance Fig. 2.21. Moreover, the relationship between the magnitude imbalance and coupling coefficient is shown in Fig. 2.23. This relationship will be demonstrated in the body of this thesis to be given by,

$$Magnitude\ Imbalance = 20log(K). \tag{2.28}$$

This balun ideally exhibits periodic band-pass characteristics when using distributed elements due to the periodicity of the Richard domain [16] and [17]. However, this type

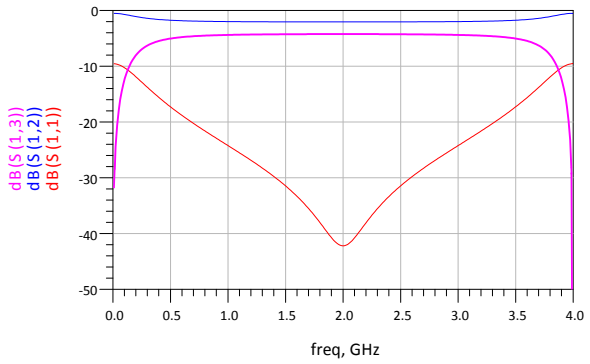


Figure 2.21: An illustration of the Guanella balun performance when the coupled line has K=0.7778.

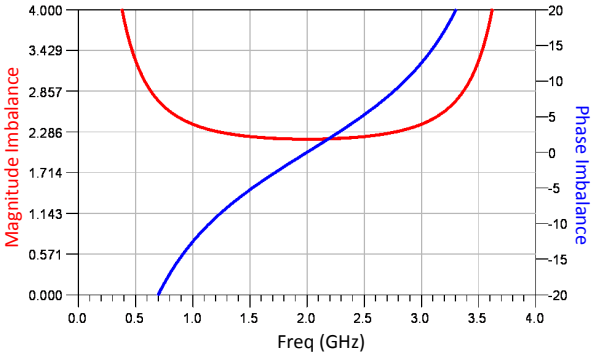


Figure 2.22: An illustration of the Guanella balun balance when a coupled line with K=0.7778 is used.

of balun has a better return loss bandwidth compared to other types such as a Marchand balun. The Guanella has a fixed transformation ratio per order of topology. Using more couplers increases the topology order hence increasing the transformation ratio between source and load impedances [18].

Marchand

The Marchand balun was introduced in a paper titled "Transmission-line conversion transformers" by N. Marchand in 1944 [19]. The original concept was developed using coaxial cables as shown in Fig. 2.24.

This balun has superior balance performance compared to other baluns but it has

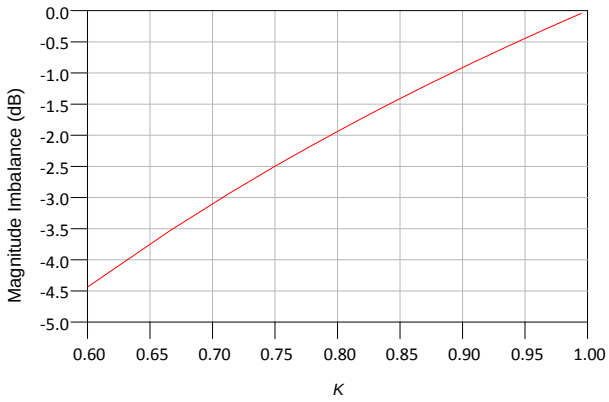


Figure 2.23: The magnitude imbalance vs coupling coefficient K.

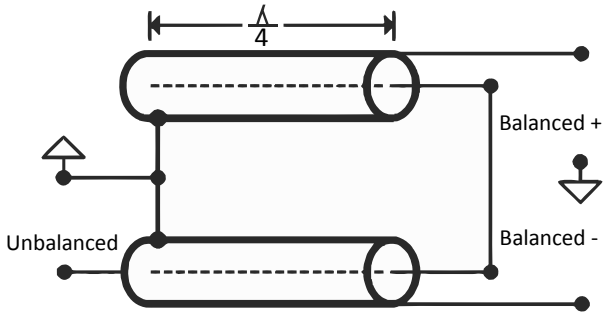


Figure 2.24: Coaxial representation of the Marchand balun [20].

a bandpass characteristics and its return-loss bandwidth is inferior to the uncompensated Marchand balun [20]. The Marchand balun has a well-established theory and it can achieve various transformation ratios between the source and load impedances without the need for more elements. The Marchand balun can be implemented in planar form using couplers instead of coaxial cable sections as shown in Fig. 2.25. The couplers can be defined using any two out of three parameters namely the odd-mode impedance (Z_{odd}), the even-mode impedance (Z_{even}), and the coupling coefficient (K). For perfect balance these coupled lines need to be identical even if the couplers themselves are asymmetrical. However, using identical couplers limits the maximum bandwidth achievable for a certain impedance transformation ratio. It is possible to use non identical couplers to obtain wider bandwidth for the same impedance transformation ratio. However, that will be at the expense of the balance of the balun.

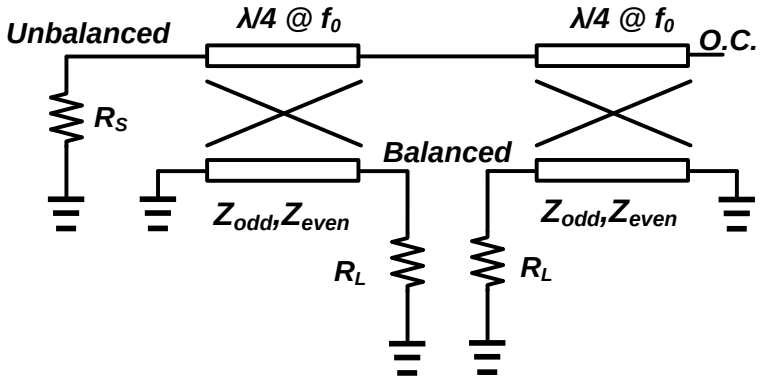


Figure 2.25: The planar equivalent of Marchand balun using two coupled lines.

When the two couplers are the identical, the Marchand balun can be viewed as a bandpass filter using three elements as shown in Fig. 2.26. When both couplers are $\lambda/4$ in length then each element in the filter equivalent topology is also $\lambda/4$ in length and their values can be computed from the couplers' parameters as follows [21],

$$Z_a = \frac{2Z_{even}Z_{odd}}{K(Z_{even} - Z_{odd})}, \tag{2.29}$$

$$Z_b = \frac{Z_{even} + Z_{odd}}{2}. \tag{2.30}$$

The balanced port impedance should be scaled by a factor of K^2 in order for it to be used in the filter representation accurately Fig. 2.26. There are several papers that did a study on numerical solutions for Marchand balun in terms of bandwidth and return loss requirements [16, 21–23].

Using this equivalent structure, we can compute S_{11} accurately but predicting the magnitude of S_{21} and S_{31} is not guaranteed except when using identical couplers then $Z_1 = Z_2$ and the magnitude of S_{21} and S_{31} is exactly 3 dB less than the transmission coefficient of the filter equivalent. As for the case where the couplers are not identical then there will be imbalance in the two branches. The even-mode. However, is modeled differently and is much simpler as it is composed of one element Fig. 2.27. If the application does not require a reactive even-mode behavior then it is possible to provide a broadband matched load instead by adding an even-mode matching network to the output of the balun [24]. Further increase in bandwidth can achieved using topologies with multiple stages [23, 25].

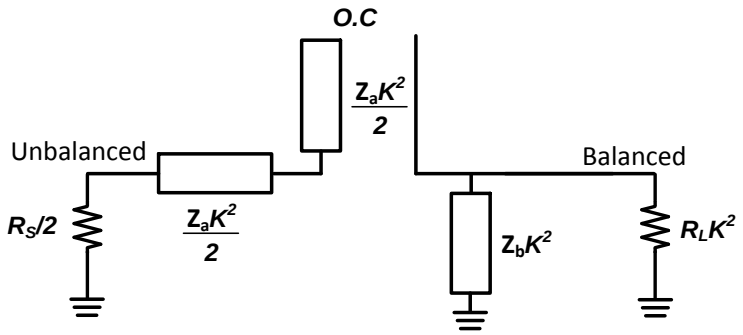


Figure 2.26: The three elements odd-mode band-pass filter equivalent of the Marchand balun.

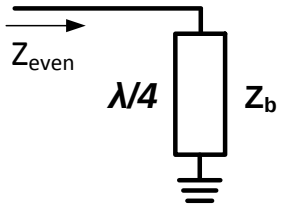


Figure 2.27: The even-mode equivalent circuit of the Marchand topology.

Uncompensated Marchand

A variation on the Guanella topology which includes a short-circuited stub to improve the phase balance from the original Guanella. To demonstrate, Fig. 2.28 shows the performance of a Guanella balun constructed with a coupling coefficient of K=0.8824. The uncompensated Marchand balun is shown in Fig. 2.29 which includes a short-circuit stub with an impedance equal to the average of Z_{odd} and Z_{even}. The stub allows the balun to have perfect phase balance over the entire bandwidth and makes the magnitude imbalance consistent over all frequencies as shown in Fig. 2.30. This topology has surfaced again recently in several publications [20] and [26] as it provided broadband operation and a sufficiently good balance.

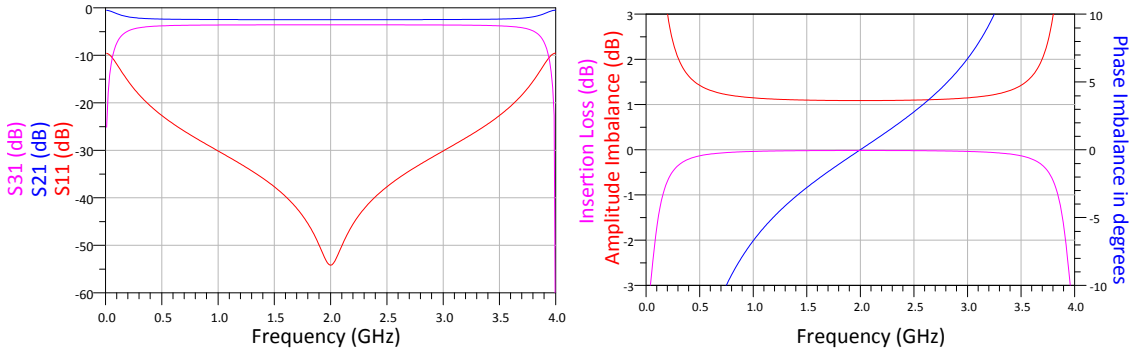


Figure 2.28: The performance of a Guanella balun using a coupled line with K=0.8824.

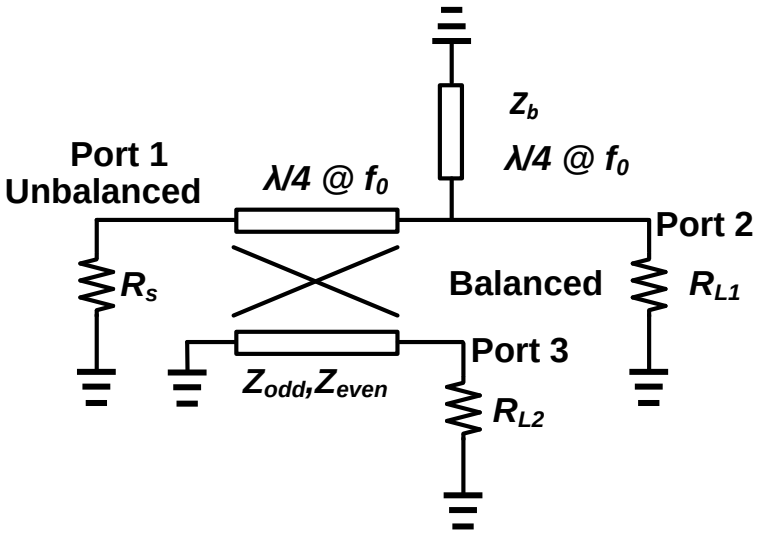


Figure 2.29: Uncompensated Marchand: a variation of the Guanella balun with added short-circuit stub.

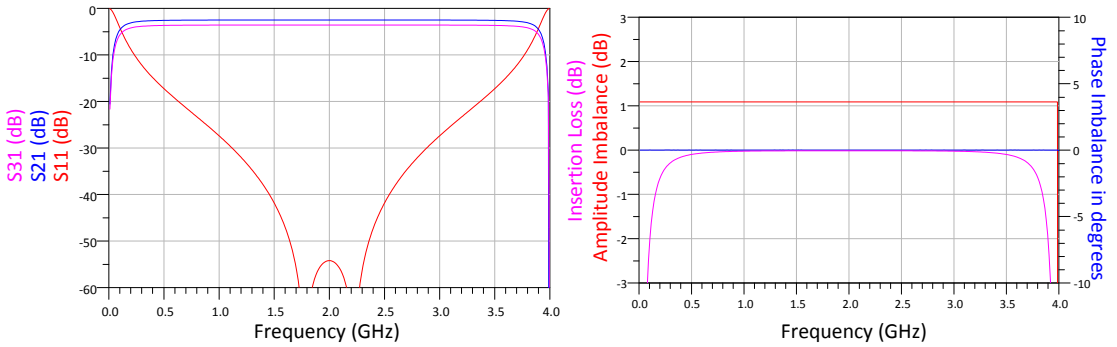


Figure 2.30: The performance of the uncompensated Marchand with improved balance.

2.6 Notable Publications on Push-Pull

There are many publications on push-pull power amplifiers in the literature. The push-pull topology is the topology of choice when it comes to frequencies lower than 1GHz. The bottleneck in extrapolating this topology to higher frequencies is in the parasitics of the passives used, such as baluns. The state-of-the-art low frequency balun use ferrite magnetic cores to enhance the bandwidth of the baluns. The bandwidths for the push-pull topologies using lower frequency ferrite baluns are close to 1GHz in absolute value and 200 % in FBW. These numbers are impressive and could potentially be replicated at higher frequencies after overcoming some design challenges. Table 2.1 shows a selected subset of the various publications in literature.

Table 2.1: Comparing publications of power amplifiers using the push-pull topology.

Ref	Frequency (GHz)	P_o (dBm)	PAE (%)	Gain (dB)	Technology	Balun	Supply (V)
[27]	0.002-1	40-43	14-27	20-24	GaAs FET	Guanella + ferrite	20
[28]	0.03-0.51	50-52.5	30-37	38-43	LDMOSFET	Guanella + ferrite	26
[29]	0.2-0.8	52-53	45-62	14.5-27	GaN HEMT	Guanella + ferrite	50
[30]	0.1-1	49-50.3	50.3-72	17.2-19.2	GaN HEMT	Guanella + ferrite	50
[26]	0.5-2.5	41-43	47-63.2	16-18	GaN HEMTs (Custom)	Uncomp Marchand	30
[31]	0.25-3.1	43-46	31-67.5	9-21	GaN HEMT	Guanella	28-30
[32]	1.4-3.4	38-41	50-62	7-10	GaN HEMT	Commercial balun	28

The most relevant publications to this thesis are [26], [31] and [32]. However, [26] did not use a balun at the output since the work was to investigate the effect of various even and odd-mode terminations on the performance of the PA and they employed a commercial off the shell balun for the input. On the otherhand, the authors of [31] did the opposite by employing a coaxial guannella balun at the output and used two seperate inputs avoiding the use of an input balun which simplified the design process and bandwidth limitation

significantly. Only the work done by [26] is a complete single input single output RF path. They employed an uncompensated Marchand balun at the input and output of the PA the baluns present 25 Ohms at each balanced terminal and the transistor is a custom designed MMIC matched to 25 Ohms at both the input and output as shown in Fig. 2.31.

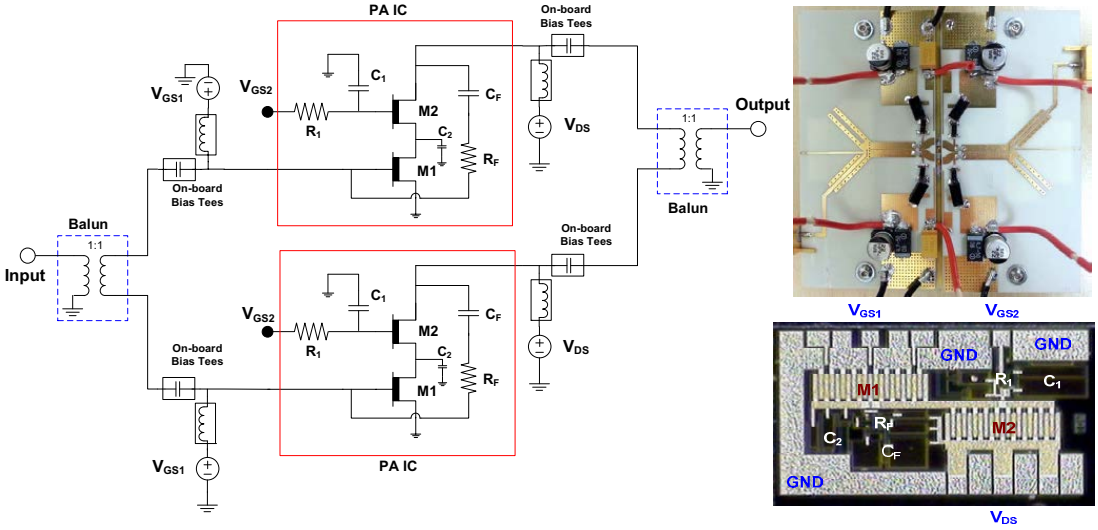


Figure 2.31: Schematic and photo of the PPPA. The amplifier measures to be 80 mm x 80 mm [26].

2.7 Back-off Efficiency Enhancement Techniques

The push-pull topology discussed earlier usually operates in class-B/J with a maximum theoretical efficiency of 78.5% occurring at maximum power level. Therefore, the efficiency of the push-pull will degrade when operating at back-off. Modern communication signals employ modulation schemes which lead to high PAPR hence forcing the PA to operate at back-off to allow for the peak power to be amplified with tolerable level of compression. As a result back-off efficiency enhancement techniques were introduced to provide high efficiency operation at back-off where the average power of the signal is located.

2.7.1 Envelope Tracking

ET is one of the popular back-off efficiency enhancement techniques. Earlier in this chapter the efficiency of a class-B PA was analyzed and was found to be a maximum value of 78.5% at the maximum power level given by 2.12. Therefore, if V_{DC} was allowed to change dynamically based on the output power level required it is theoretically possible to maintain the high efficiency operation of class-B for multiple output power levels. V_{DC} can be made to decrease with the input power level such that the output power is always at maximum efficiency point of operation. This way, the drain efficiency can, ideally, be maintained at 78.5% at all back-off power levels. However, if the load impedance is kept constant then the maximum current is not the same for all values of V_{DC} which should be taken into account. Techniques have been developed to modulate the drain bias, i.e.,V_{DC} of the PA to vary with the envelope of the signal in order to improve back-off power efficiency. A simplified block diagram of an ET system is given in Fig 2.32. The modulation of the drain voltage is achieved with the use of an envelope amplifier (EA) which modulates the drain supply voltage of the PA according to the signal's magnitude. This technique, however, has some drawbacks. The EA efficiency degrades the further in back-off the amplifier is being utilized and lowers the overall efficiency of the PA. For example, EA amplifiers with up to 80% efficiency have been achieved driving a wideband code division multiple access (WCDMA) signal with a 20 MHz bandwidth [33, 34]. If the efficiency of the PA was at the maximum value of what class-B can offer then the overall efficiency will be,

$$\eta_{overall} = \eta_{EA}\eta_{PA} = 0.80 \times 0.785 = 62.8\%, \tag{2.31}$$

where $\eta_{overall}$, η_{EA} and η_{PA} are the efficiencies of the overall ET system, the EA and PA respectively.

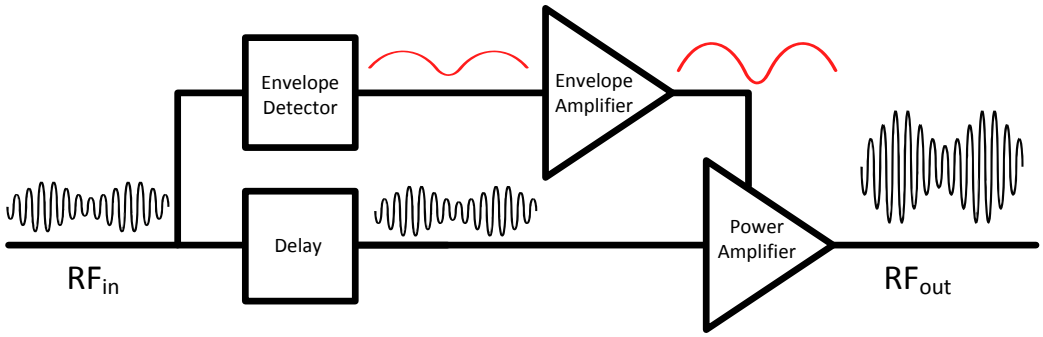


Figure 2.32: Simplified ET system block diagram.

The ET technique is mostly limited by the instantaneous bandwidth (i.e., modulation bandwidth) it is capable of supporting. However, it is not limited by the frequency range it can operate at and is capable of supporting the entire RF bandwidth of the PA employed. This means if broadband PA topology, such as push-pull was used to design the PA, then the ET system can achieve high efficiency performance across the entire frequency range. The modulation bandwidth is highly limited by the speed of the EA. Current state-of-the-art of EAs that modulate the supply in a continuous fashion are limited to around 20 MHz in bandwidth [34–37]. Significant progress have beem made during the past few years that lead to an improvement in bandwidth up to 120 MHz using discrete level of supply modulations such as [34, 38]. While the bandwidth improvements is quite impressive this was achieved over a single band only. A recent survey [39] has asserted that other efficiency enhancement techniques such as DPA which is an impedance modulation topology still has the advantage when it comes to modulation bandwidth.

2.7.2 Doherty Amplifier

The Doherty power amplifier topology was first introduced in 1936 by William Doherty to solve the problem of low back-off efficiency of radio signal amplifiers [40]. The problem that Doherty was trying to address is transmitting of modulated signals that have a PAPR higher than 0 dB efficiently. The main principle which DPA is based on is the use of load modulation technique.

load modulation

In the load modulation technique the apparent impedance presented to the transistor is varied as a function of power in order to keep the voltage swing maximized and hence the operation efficient at all power levels, i.e., efficient operation at back-off and peak power. Ideally, the PA needs to be presented with optimum impedance (R_{opt}) to operate with the maximum efficiency at a certain power. The value of R_{opt} varies with the targeted output power. One way to implement load modulation is shown in Fig. 2.33 as suggested by Doherty [40].

The DPA topology consists of two amplifiers in parallel one called the "main or carrier" where the RF signal is fully amplified and the other is called the "auxiliary (aux) or peaking" where the signal is only amplified after it exceeds a certain threshold so it is typically biased in class-C. To illustrate, Fig 2.34 shows the current and voltage profiles of a classical DPA architecture. When the input voltage is less than half the maximum,

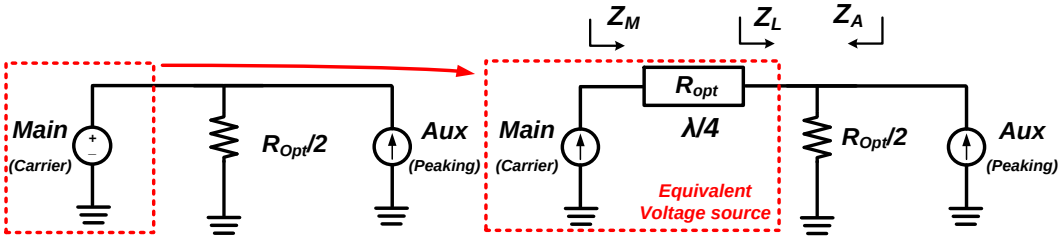
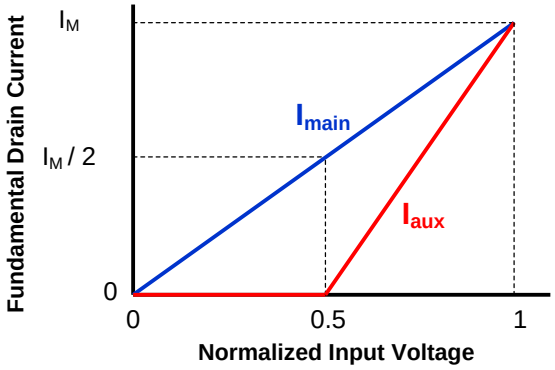
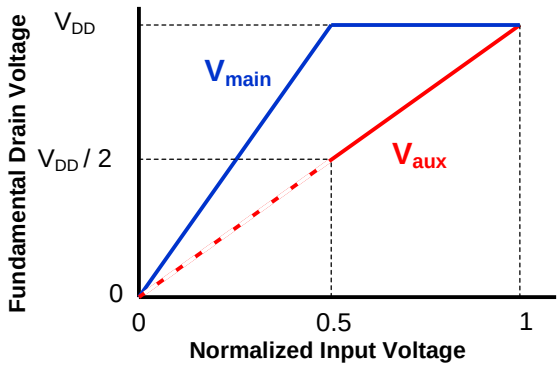


Figure 2.33: Simplified DPA topology block diagram.

input power is at 6 dB back-off, the main transistor is on while the auxiliary transistor is off, i.e., auxiliary current is 0 A. During this stage the main transistor sees $Z_M = 2R_{opt}$ which is the value of the impedance that provides the maximum efficiency at quarter the power level of both transistors combined. After the input voltage passes half it's maximum value the class-C auxiliary transistor starts conducting current. The current flowing into the load changes the apparent impedance presented to the main transistor Z_M gradually reducing it to the optimal value at full power as shown in Fig. 2.35. Fig. 2.36 shows the typical efficiency profile of a DPA architecture when the main and auxiliary transistors are biased in class-B for simplicity. Note that the auxiliary is usually biased in class-C which will alter the curves slightly from the ideal expectations.



a) The magnitude of the fundamental component of the drain current Vs the normalized input voltage magnitude



b) The magnitude of the fundamental component of the drain Voltage Vs the normalized input voltage magnitude

Figure 2.34: The fundamental current and voltage profiles of a classical DPA architecture.

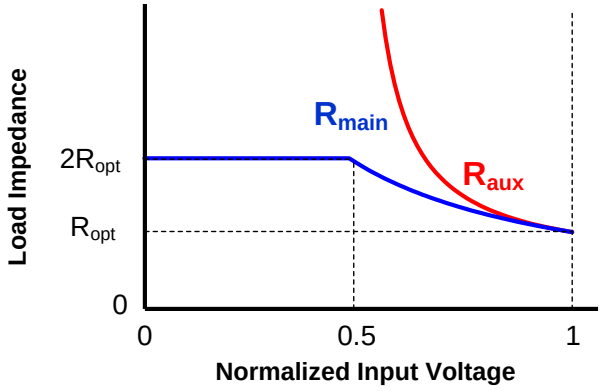
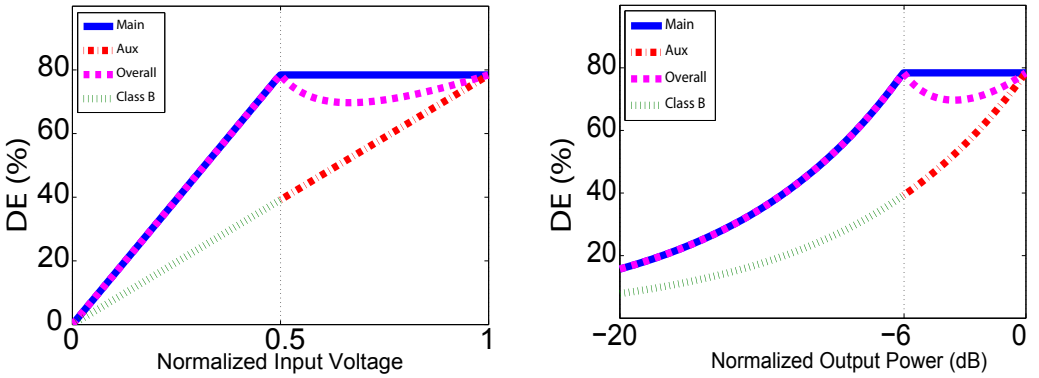


Figure 2.35: The load impedance of the main and auxiliary transistors as a function of normalized input voltage.



(a) Efficiency vs. normalized input voltage.

(b) Efficiency vs. normalized output power.

Figure 2.36: The efficiency profile of a standard DPA.

Notable DPA publications

There many publications on DPA which range in terms of specifications from low to high frequencies, low power to high power applications and narrowband to broadband performance. Notable publications which are relevant to this work are listed in Table. 2.2.

Table 2.2: Comparison table of notable Doherty PA publications.

Ref	Frequency (GHz)	BW (%)	P_{out} (dBm)	Peak DE (%)	Back-off DE (%)
[41]	2.1-2.96	34	$40-42$	$55-68$	$40-48$
[42]	1.7-2.25	28	48.2−49.6	$65-77$	$53-64$
[43]	1.96-2.46	23	39.5−41.7	$47-62$	$44-45$
[44]	0.7-1	35	$49-50.8$	$60-75$	$50-69$
[45]	1.6-2.4	40	42	$50-60$	$38-52$
[8]	0.47-0.803	52	$58.4-59$	$49-56^{(1)}$	$42-46^{(1)}$
[46]	0.79-0.96	20	$54.5-55$	$56-60$	$48-50$
[47]	1.8-2.2	20	$59-59.5$	$65-77$	$53-65$
[48]	1.7-2.7	45	52.7−54.3	$53-66$	$40-50$
[49]	0.65-0.95	37.5	53.7−54.2	$55-62$	$47-50$

(1) Based on the average efficiency of pulsed measurements.

2.8 Conclusion

In this chapter, multiple classes of operation and PA topologies where introduced. Based on the information in this chapter the push-pull topology was chosen to be the most suitable for broadband communication PAs given its ability to separate the even-mode harmonics easily from the fundamental path. As for the back-off efficiency enhancement techniques, current trends point to the necessity of broadband signal transmission which may require up to 100 MHz of bandwidth. Therefore, the DPA topology is the most suitable candidate for back-off efficiency enhancement techniques for next generation high power, high frequency PAs for wireless communication infrastructure.

Chapter 3

Co-Design Methodology for Push-Pull Based PAs

3.1 Introduction

This chapter introduces co-design as a methodology that utilizes planar baluns as a flexible design parameter while designing broadband push-pull based power amplifiers. The methodology resolves some of the challenges associated with the use of baluns with packaged transistors characterized by significant parasitics. The methodology allows the designer to separately control the odd- and even-mode impedances presented to the PA simultaneously by introducing additional flexibility in optimizing the balun's dimensions and placement within the overall input and output networks. This methodology enables high efficiency operation over a broad range of frequencies through better second harmonic control. This was achieved by placing the balun in close proximity to the transistors' terminals and re-purposing the packaged transistors' leads into a coupled-line with high coupling coefficient. Furthermore, independently controlled odd-mode terminations are realized using broadband matching networks at the unbalanced side of the baluns.

Using this methodology, an 85 W PPPA is designed using off-the-shelf packaged gallium nitride (GaN) high electron mobility transistors (HEMT). The fabricated PA demonstrated drain efficiency and output power above 45% and 46.5 dBm respectively over the frequency band spanning from 0.45 to 1.95 GHz. Furthermore, the fabricated PA is successfully linearized using digital pre-distrotion (DPD) when driven with single- and multi-band modulated signals. Overall, the fabricated PA has the best reported power, efficiency, and

bandwidth combination for a multi-octave PPPA designed with input and output baluns using packaged off-the-shelf transistors.

The co-design methodology is utilized to design a broadband Doherty power amplifier where the main and auxiliary transistors were connected in a push-pull topology. A mixed-signal push-pull DPA PP-DPA prototype using off-the-shelf packaged 90 W GaN HEMT demonstrated a drain efficiency of $52-64$ % and $51-58$ % at saturation and 6 dB back-off power levels, respectively, across a FBW of 80 % (0.6 GHz$-$1.4 GHz). It also maintained an output power of about 51.5 dBm $\pm$1.5 dB. The implementation and measurement results are presented along with a comparison table outlining the performance of the fabricated PP-DPA against relevant publications in literature.

3.2 On The Design of Multi-Octave High Power PPPAs

Publications such as [26–32, 50–55] focus on the odd-mode in-band performance metrics of the balun when designing a PPPA. Traditionally, the designer of a PPPA would follow a modular approach by treating the balun as a standalone block by assuming fixed impedances at the unbalanced and balanced ports (i.e., 50 Ω at the unbalanced port to 25 Ω at the balanced port). Then the designer incorporates an intermediate matching stage between the balun and the transistor to match the balanced ports to the transistor's gate or drain (see Fig. 3.1). This approach allows for easier optimization since each part of the circuit has to be designed separately. However, this approach does not take into account the dispersive effect of the matching network on the second harmonic termination introduced by the balun. The second harmonic termination can have an effect on efficiency, power, and linearity, hence poor control of the second harmonic termination can potentially lead to a reduction in these important performance metrics.

In most of the reported publications, the baluns were treated as independent power splitting/combining stages with certain in-band impedances and little has been presented about how the choice of a balun's topology, parameters and location relative to the transistor impacted the performance. There are several critical design consideration that should be addressed when designing a PPPA which are discussed later along with the proposed design procedure.

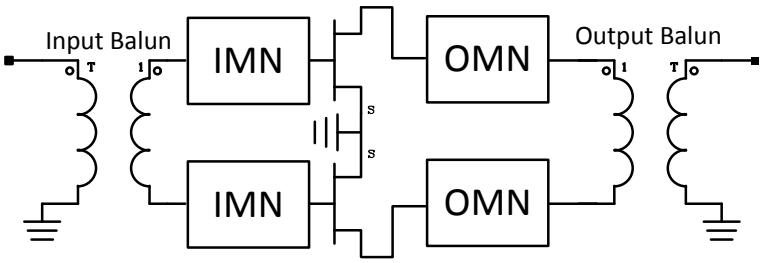


Figure 3.1: Traditional PPPA topology.

3.2.1 Second Harmonic Termination

Due to the broad bandwidth of multi-octave PPPAs, the second harmonic will cover a very wide range of frequencies which could be as much as twice that of the fundamental bandwidth. There are forbidden regions on the Smith chart where the second harmonic termination would severely degrade the performance of a PA in terms of efficiency, power and gain [32, 56]. This low performance region varies with parameters such as frequency, transistor topology, technology, and size. To elaborate, a simulation was conducted using Wolfspeed's CGH40090PP compact model which will be used later in the design of a prototype. The second harmonic termination was swept at the edge of the Smith chart at both the input and output of the transistor at the same time, hence simulating two baluns of similar electrical length at both the input and output. For every swept value of the second harmonic, a load pull was conducted at the fundamental frequency and the maximum DE value for that specific even-mode termination and frequency was plotted. The third harmonic was set to equal the fundamental since it sees the odd-mode impedance while the fourth and higher-order harmonics were set to be short-circuits. Fig. 3.2 shows the low performance associated with a purely reactive second harmonic termination under the various phase angles. This is more likely to be problematic when using packaged transistors as the parasitics will significantly affect both the fundamental and second harmonic impedances.

3.2.2 The Co-Design Methodology

Previous relevant publications [26–32, 50–55] did not elaborate on the methods used to control the second harmonic in PPPAs. Upon investigation, two viable approaches for avoiding low efficiency second harmonic terminations were identified. One, using an isolated balun architecture which presents a harmonic impedance away from the edge of the Smith

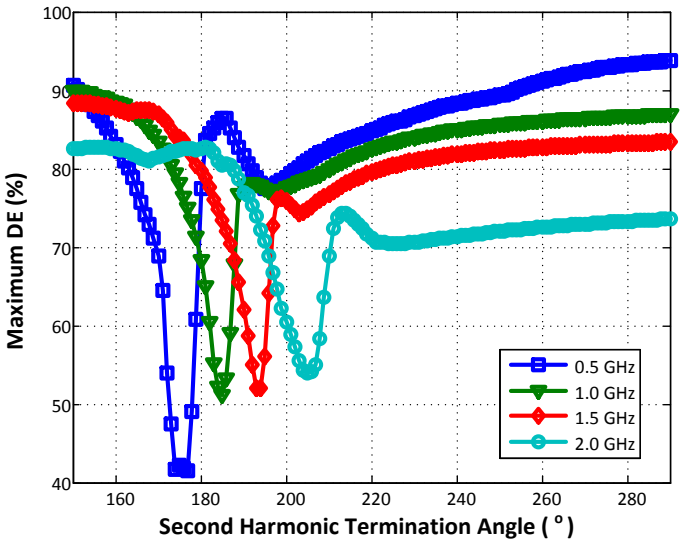


Figure 3.2: The effect of the second harmonic termination angle on the maximum possible DE.

chart, hence avoiding the region where the efficiency of the PA can be significantly reduced. A balun with isolated balanced ports will present a resistive load for even-mode signals [24], while a non-isolated balun will present a purely reactive termination (see Fig. 3.3). This approach adds considerable challenge to the balun design due to the addition of the isolation network and might limit the bandwidth that can be achieved.

Two, an even simpler approach to keep the second harmonic termination out of the low performance region of the PPPA is to limit dispersion of the even-mode impedance presented by the balun. This can be achieved by keeping the balanced ports of the balun as close to the transistor as possible. This ensures maximum control over the even-mode impedance seen by the transistor in the push- pull configuration, hence avoiding the case where the second harmonic termination falls in an undesirable region. In this work, the second approach was adopted as part of the proposed co-design methodology geared towards designing high power broadband PPPAs. The methodology starts by specifying the frequency range of operation, transistor technology, and power target. These specifications can then be used to determine the transistors that can be used, hence allowing the designer to conduct load and source pull simulations to determine the range of the second harmonic termination that limits the performance of the PA. Knowing the range of second harmonic impedances to avoid the designer can then select a balun architecture or layout that provides the desirable even-mode impedance that doesn't overlap with a

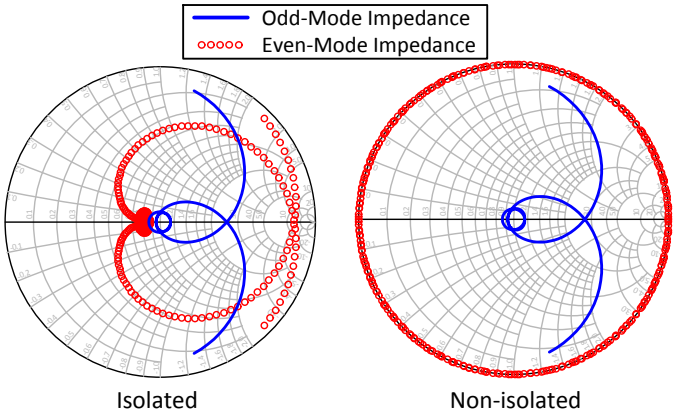


Figure 3.3: Comparison between non-isolated and isolated baluns showing the odd- and even-mode impedances.

low performance region over the operating frequency range. Then, in order to reduce the dispersion, the balun is moved as close as possible to the transistor and the matching network is placed on the unbalanced side of the balun away from the transistor Fig 3.4. This allows much tighter control over the second harmonic termination. Moreover, the balun can now be treated as a flexible design parameter where it is possible to control the odd-mode impedance using the balun's parameters. To Accurately predict the behavior of the balun, a schematic or EM based model can be used as long as the reliability of the model can be trusted. The model can be placed in the simulation environment where the overall PA can be simulated to fully account for the interaction of the balun with the transistor and the external matching networks. The input and output matching networks can then be synthesized or optimized for optimum performance over the entire band by targeting the desired fundamental impedance. The desired fundamental impedance can be determined using fundamental load- and source-pull simulations with the second harmonic termination set by the balun's even-mode impedance. The methodology is illustrated in the flow chart shown in Fig. 3.5.

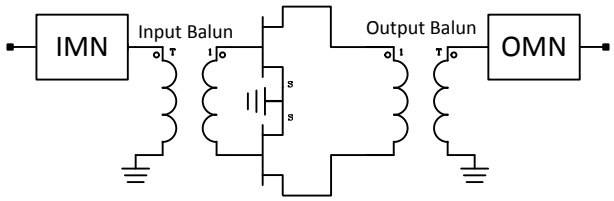


Figure 3.4: The PPPA topology with limited even-mode dispersion used in the proposed co-design methodology.

3.3 Prototype Design Using The Co-Design Methodology

3.3.1 Balun Transformers

As mentioned in the previous chapter, the baluns are the most critical passive components in a multi-octave PPPA design. There are two balun topologies that can be implemented with distributed elements which are suitable for high power multi-octave PPPAs. The two candidate architectures are the Marchand balun [20, 21, 24, 25, 57–62] Fig. 2.25, and the uncompensated Marchand balun [20, 63] Figs. 3.6 and 3.7. The main attraction of the Marchand balun topology is the excellent balance achieved between the two balanced ports. The balance is important for stability and for second harmonic rejection, as will be shown in sub-section 3.3.3. Theoretically, the Marchand balun is perfectly balanced when using identical ideal coupled lines. However, when implemented in the planar form using planar coupled lines, the balance is reduced due to several practical problems such as parasitics and the difference in phase velocities between the even and odd-mode propagation. Therefore, it becomes prudent to implement a topology with relatively wider bandwidth with a balance that is comparable to the non-idealized model of the Marchand balun.

The Guanella balun, and by association the uncompensated Marchand balun, is known for its superior bandwidth when compared to that of the Marchand balun, typically higher than 100% [20, 63, 64]. The bandwidth and balun balance are heavily dependent on the coupling coefficient of the coupled lines and this is one of the challenging aspects of planar-based design. The high coupling coefficient was achieved by patterning the ground plane around the coupler, thus significantly reducing the coupled line's capacitance to ground, which in turn increased the even-mode impedance [20, 58]. The uncompensated Marchand uses a shunt short-circuited transmission line at one of the balanced ports to compensate for the phase imbalance, as shown in Fig. 3.6. To illustrate how the phase balance is

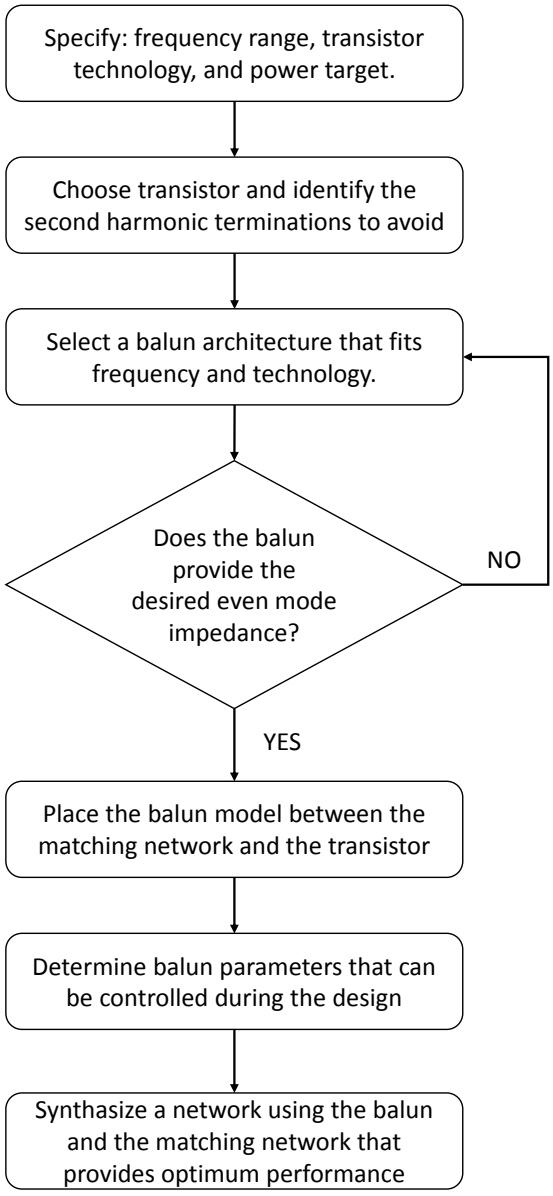


Figure 3.5: The co-design methodology flow chart.

achieved, the uncompensated Marchand was analyzed by deriving the simplified circuit of the balun using the coupler's equivalent circuit shown in Fig. 3.8. The values of N, Z_a and Z_b are given by equations (3.1), (3.2) and (3.3) which are re-listed here from chapter 2 for

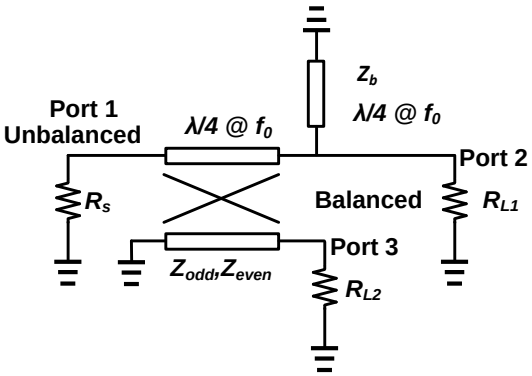


Figure 3.6: The schematic view of the planar version of the uncompensated Marchand balun.

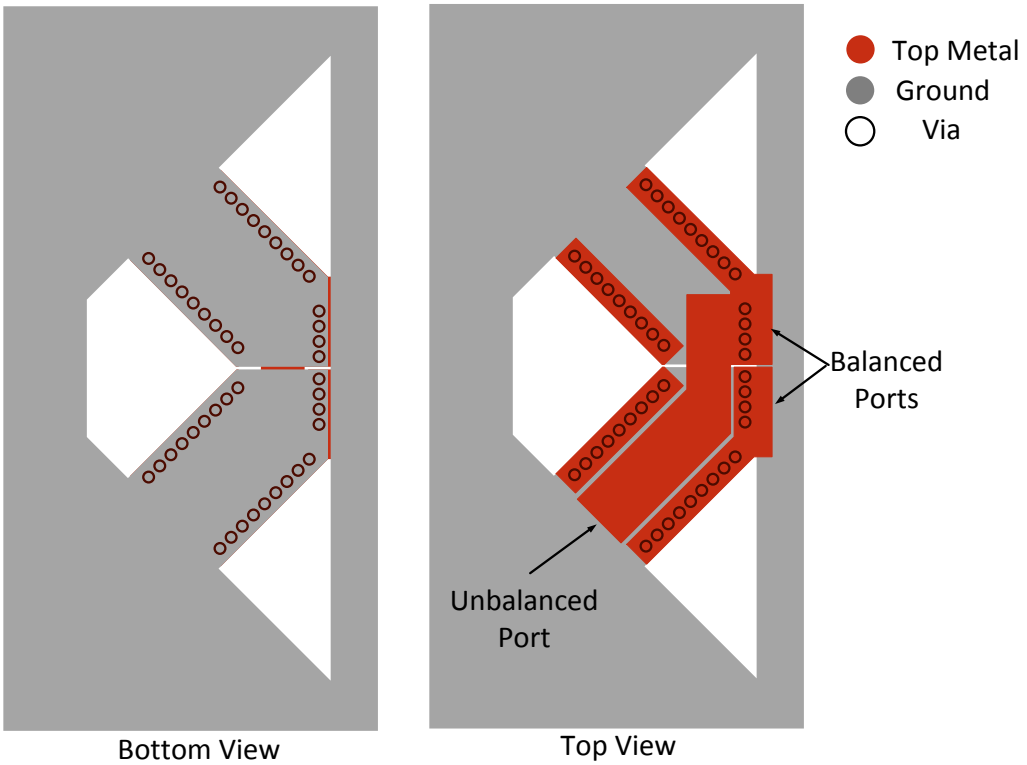


Figure 3.7: The layout view of the planar version of the uncompensated Marchand balun.

convenience.

$$\frac{1}{N} = K = \frac{Z_{even} - Z_{odd}}{Z_{even} + Z_{odd}} \tag{3.1}$$

$$Z_a = \frac{2Z_{even}Z_{odd}}{K(Z_{even} - Z_{odd})} \tag{3.2}$$

$$Z_b = \frac{Z_{even} + Z_{odd}}{2} \tag{3.3}$$

Where Z_{odd} and Z_{even} denote the odd- and even-mode impedances of the coupled lines, respectively.

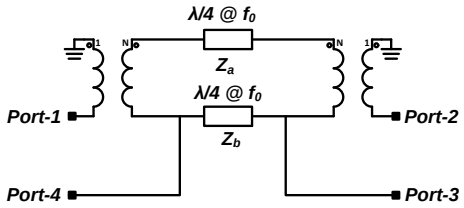


Figure 3.8: An ideal coupled line equivalent circuit.

The coupler used to construct the balun in Fig. 3.6 can be replaced by the equivalent model as shown in Fig. 3.9. The transformer on the unbalanced side can be simplified along with the source impedance (R_s)into their equivalent impedance using N^2 which can be computed from the coupler parameters as given in equation (3.1)(Fig. 3.10 a)). The circuit can then be rearranged as shown in Fig. 3.10 b). It can be seen that both of the balanced terminals have a parallel short-circuited stub equal to Z_b therefore the overall phase of the load seen at each terminal is the same. The phase is balanced in an uncompensated Marchand balun while it is not balanced in a Guanella balun except at the center frequency since the stub in that case presents an open-circuit. Finally, the second transformer and the load connected to it can be replaced by their equivalent value using N^2 (Fig. 3.10 c)). Due to the coupler's imperfect coupling, i.e., $K < 1$, an imbalance in the magnitude between the two terminals is inevitable. From the model, it can be deduced that the magnitude imbalance is equal to the coupling coefficient. Hence, for high coupling coefficients (i.e., K higher than -0.5 dB), the magnitude imbalance can be considered negligible.

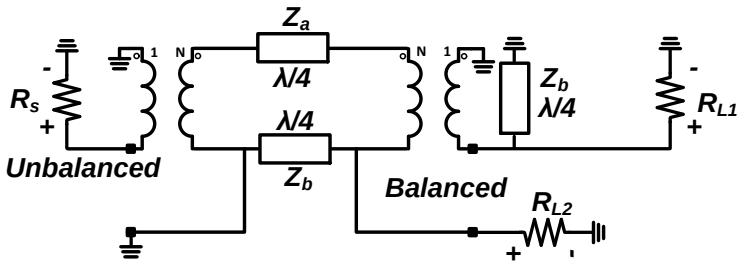


Figure 3.9: The planar version of the uncompensated Marchand balun with the coupler's equivelent model.

Balun Design

The general layout of the balun was chosen based on previous publications that demonstrated good performance [20, 26]. The layout can be seen in subsection 3.3.2, where W is the width of the TL which dictates the odd-mode impedance, and L controls the even-mode impedance and is related to the length of the coupled line and short stub. Note that the actual lengths of the coupled line and short stub depend on the actual layout, and L is not equal to the effective length. Fig. 3.11 shows the difference between an ideal schematic model, an EM simulated implementation of an uncompensated Marchand balun on a double sided PCB and the effect of transistor package leads. An additional TL to account for the size of the package leads of the CGH40090PP transistor is added to the layout of the balun. This figure demonstrates the significant effects of the parasitics of the balun and transistor package on the odd- and even-mode impedances.

Fig. 3.12 illustrates the effect of W and L on the odd- and even-mode impedances. In order to utilize the maximum amount of output power possible by the transistor, the balun with sufficiently low odd-mode impedance was targeted. The balun was designed for low odd-mode impedance, bandwidth, balance, and confined second harmonic impedances.

Second Harmonic Control

Using load and source pull characterization, the critical low performance second harmonic region was determined for reactive impedances with phase angles between 170^o and 210^o, as was shown previously in Fig. 3.2.

Due to the large package leads, there is a low impedance TL between the balun and the transistor. This TL adds significant capacitance which causes the second harmonic

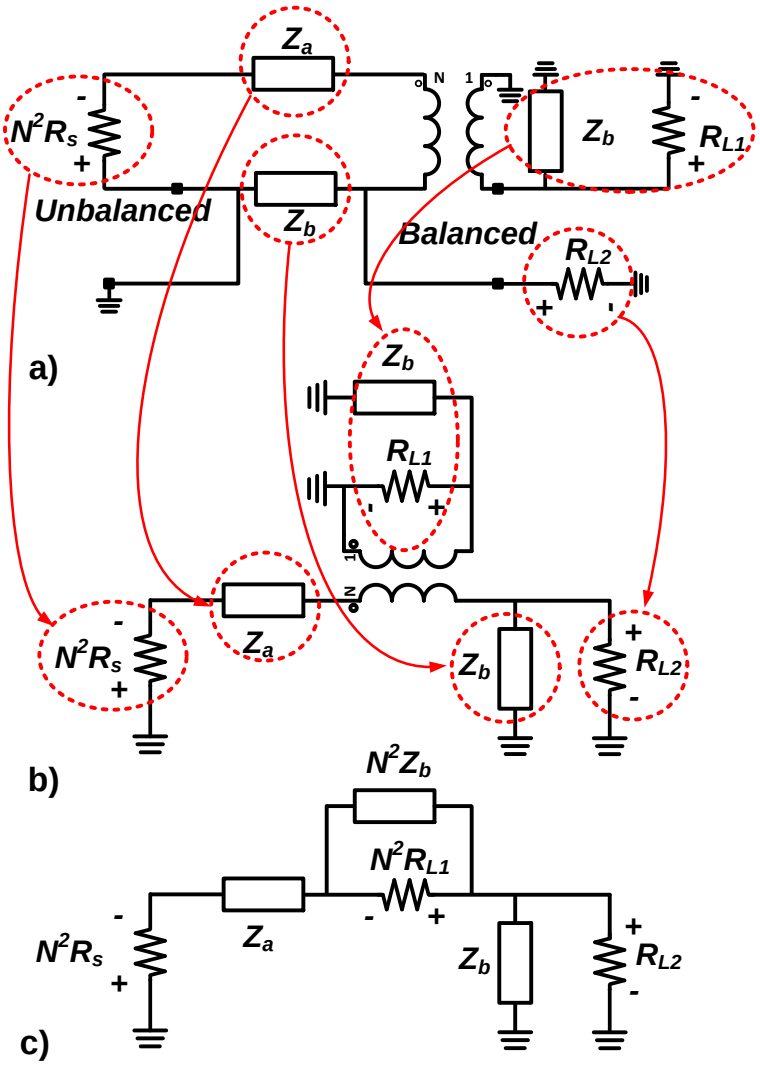


Figure 3.10: The last three simplification steps of the uncompensated Marchand balun. a) the simplification of the source impedance with the first transformer b) reorganized elements into a more friendly outline c) the equivalent circuit of the uncompensated Marchand balun after simplification.

terminations to enter the low performance region (Fig. 3.13 a). In order to increase the impedance of the line, its capacitance to ground was reduced by removing the ground metal layer underneath the line. This increased impedance greatly reduced the second harmonic dispersion (Fig. 3.13 b), however, it caused the odd-mode impedance to drift away from the

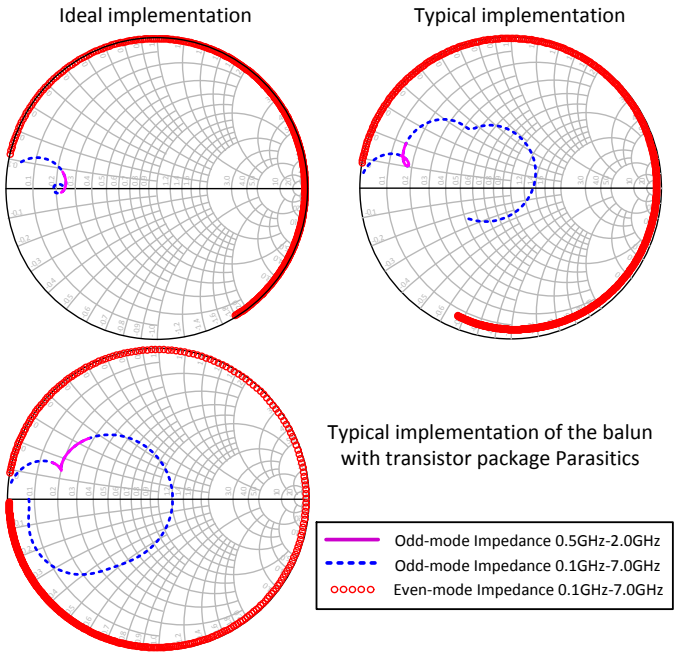


Figure 3.11: The effect of the balun's layout parasitics and transistor's package leads on the balun's odd, and even-mode impedances.

low impedance region as the impedance presented by the package leads was now relatively high. To preserve the low odd-mode impedance, a floating metal ground patch was placed under the transistor leads causing the coupling coefficient between the two transistor leads to increase and causing the even-mode impedance to be significantly higher than that of the odd-mode impedance. The floating metal served as a virtual ground for odd-mode signals and a virtual open for even-mode signals due to the symmetry (Fig. 3.14).

The virtual short plane will cause the floating metal to act as a virtual ground, hence increasing the capacitance to ground and lowering the odd-mode impedance. On the other hand, the virtual open in even-mode propagation will not ground the floating metal, keeping the capacitance to ground low and the even-mode impedance high. With this approach, it was possible to keep the low odd-mode impedance needed at the transistor terminals while maintaining high even-mode impedance to control second harmonic dispersion (Fig. 3.13 c).

The performance of the balun was further enhanced by two additional matching networks placed at the unbalanced ports of both the input and output baluns. These matching networks served two purposes, namely, to match the balun to a 50 Ohm load, and to pro-

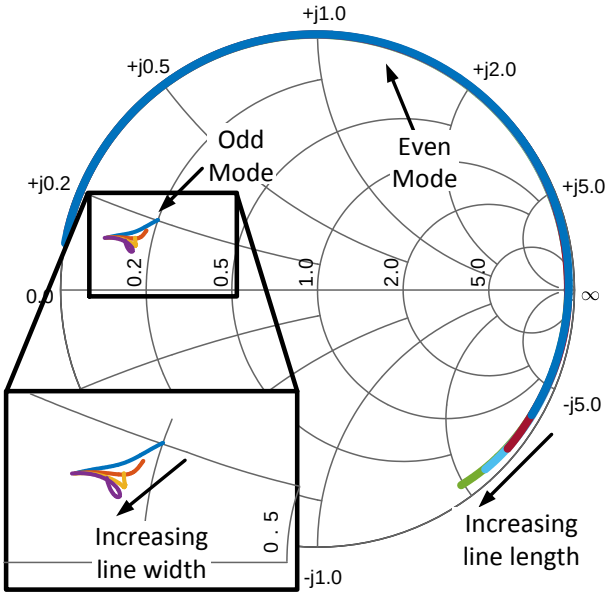


Figure 3.12: The effect of line width W [2:0.5:3.5] mm and length L [5:2:11] mm on the odd- and even-mode impedances.

vide additional flexibility for controlling the odd-mode impedance which enhances the PA performance. The resultant odd and even S-parameters of the baluns and the matching networks are shown in Fig. 3.15. The magnitude and phase imbalance are shown in Fig. 3.16.

3.3.2 Bias Network

The bias network was integrated into the balun's architecture to reduce the intrusive effect of the biasing which is typically added near the transistor. The employed baluns had inherent ground nodes in their architecture and these nodes were ac-coupled to the ground plane using DC blocking capacitors to provide an RF ground node. The biasing was incorporated into the balun architecture as shown in Fig. 3.17. Such integration minimized the effect of the bias network on the impedance matching presented at the transistor nodes.

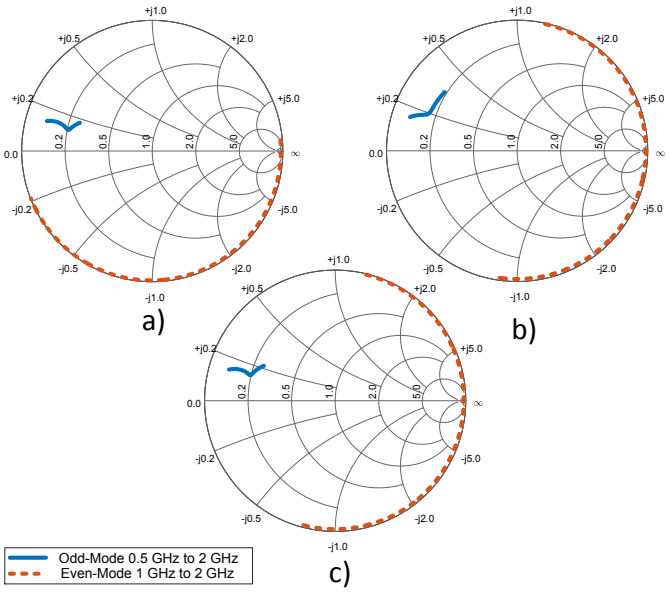


Figure 3.13: Simulation results showing the effect of the (CGH40090PP) transistor leads on the odd- and even-mode Impedances under three scenarios (a) low impedance TL (b) high impedance TL (c) coupled line.

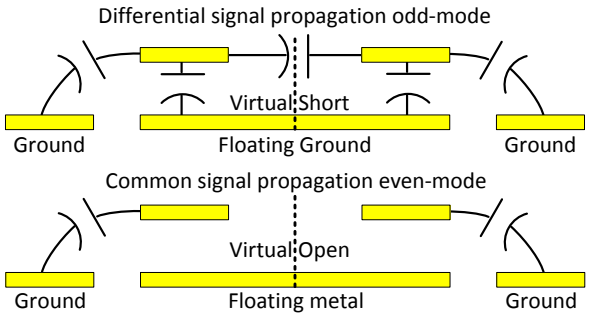


Figure 3.14: Illustration of total capacitance under odd-mode and even-mode propagation.

3.3.3 Stability and Balance

The stability analysis of PPPAs requires the designer to take care with both the differential and common mode oscillations. The magnitude imbalance introduced by the non-ideal balun will not only produce two different fundamental impedances but will also cause the second harmonic termination of one of the branches to lay outside the Smith chart

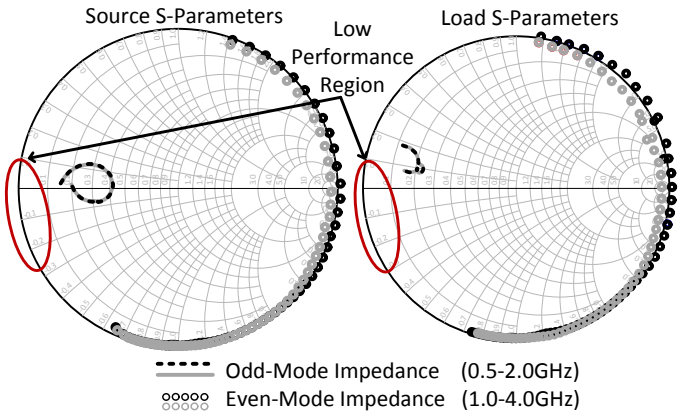


Figure 3.15: Final balun and matching network S-parameters showing the odd- and even-mode impedances for both branches of the balun.

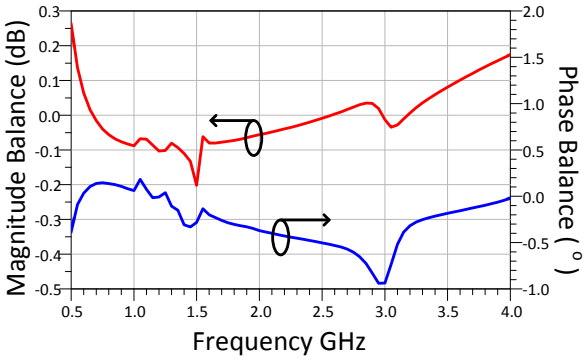


Figure 3.16: The magnitude and phase imbalance of the output balun including the bias and matching network. The simulation uses measured S-parameters data for all SMDs used.

due to the imbalance of the transistors' currents at the balanced branches. This could cause oscillations even if the transistors are designed to be unconditionally stable at all frequencies. This is due to the possibility of the second harmonic impedance getting into the instability circles outside the Smith chart. In this work, the baluns were designed to have a magnitude imbalance of less than 0.25 dB which helps in reducing the potential for instability PPPA. For the case where the magnitude imbalance is equal to 0.25 dB, the second harmonic termination is shown in Fig. 3.18. The stability of the push-pull PA was maintained by including a stabilization network between the balun and each transistor gate as shown in the finalized layout which also shows the matching networks and baluns

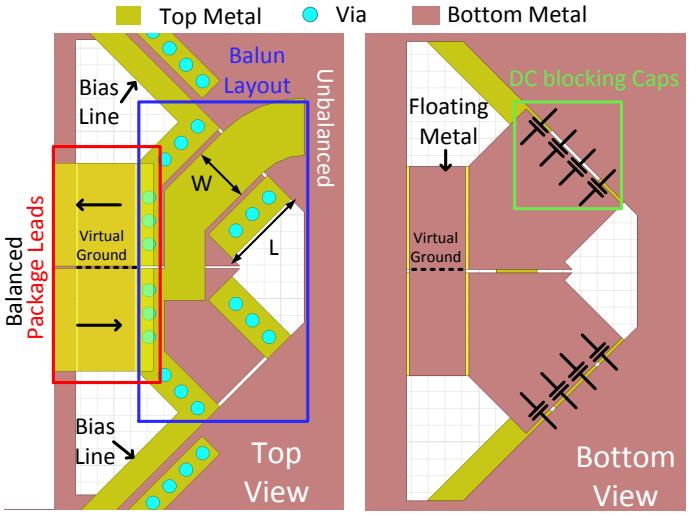


Figure 3.17: The final output balun showing the general balun layout, the RF grounding, biasing feed, floating metal, package leads and ground patterning.

Fig. 3.19.

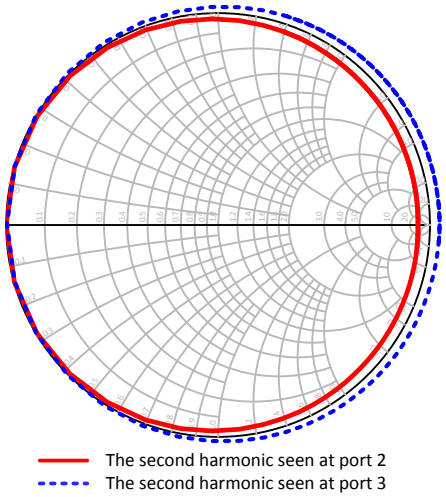


Figure 3.18: The effect of 0.25 dB magnitude imbalance on the second harmonic seen at the balanced terminals when the balanced terminals are driven by current sources.

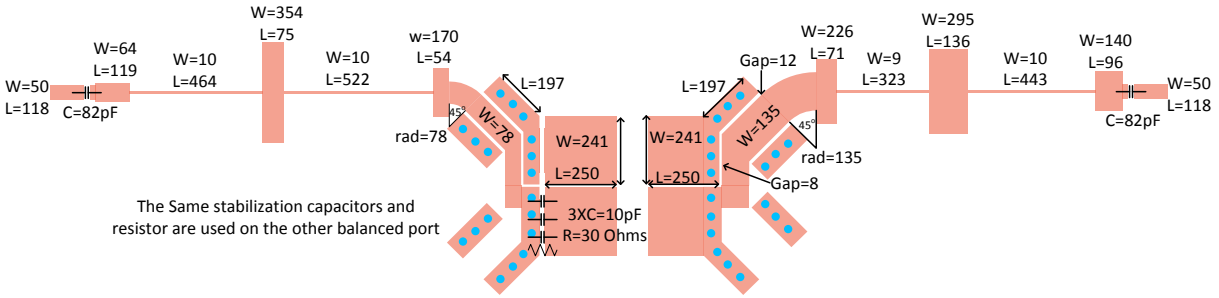


Figure 3.19: The finalized matching networks and baluns' dimensions in (mil) including the stabilization network and DC blocking capacitors.

3.3.4 Simulation Results

The completed layout comprised of the input and output matching networks, baluns, and bias networks was simulated using Ansoft's high frequency structure simulator (HFSS) from 10 MHz to 12 GHz. The resulting S-parameters and Keysight's compact transistor model were used to obtain the simulation results. Keysight's advanced design systems (ADS) was used to simulate the entire design using the harmonic balance simulator. The results show a high power high efficiency performance from 0.45 GHz to 2 GHz (Fig. 3.20).

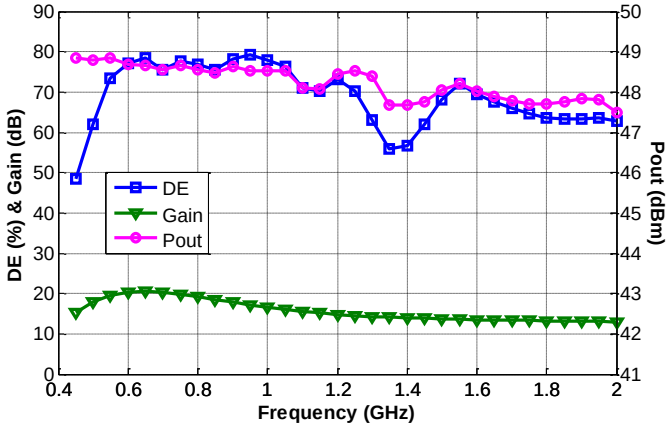


Figure 3.20: Large signal CW simulation results using Cree's transistor compact model and full layout EM simulation using HFSS.

3.4 Measurement Results

The PPPA depicted in Fig. 3.21 was fabricated using RO4003C 12 mil substrate with ground patterning to obtain high quality baluns (i.e., broadband, low-loss and excellent balance). The assembly was completed using off-the-shelf transistors from Wolfspeed. The transistor (i.e., CGH40090PP) has 2X45 W transistors which can be used in a push-pull configuration. The transistors were biased in deep class-AB at 200 mA each and with a drain bias voltage of 28 V.

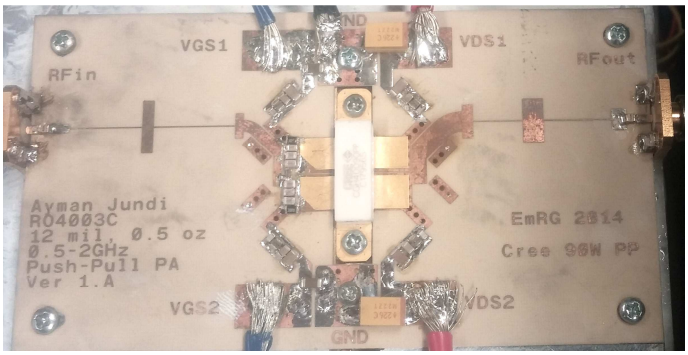


Figure 3.21: A photograph of the assembled PPPA.

The measurement setup used for testing is shown in Fig. 3.22. The equipment used in the setup are listed in Table. 3.1. From the table, it is important to note that two different drivers were used to cover the entire frequency range. On the other hand, the use of two different power supplies was due to convince at the time of the measurement. The arbitrary wave generator (AWG) was used to generate signals at RF frequencies directly the signal is then amplified using a driver and delivered to the device under test (DUT). The output of the DUT is then attenuated and delivered to the signal analyzer with part of the signal coupled to a power meter. The effect of the attenuator and coupler has been calibrated beforehand using a calibrated network analyzer. The signal analyzer is connected to a personal computer running MatLab as a control interface.

Large signal measurements were conducted under pulsed conditions with a duty cycle of 15% and a 2 ms period. Fig. 3.23 shows the performance of the PPPA as a function of the input power (Pin) at 1.2 GHz. Fig. 3.24 shows the large signal performance of the PPPA over the entire band of operation. The PA demonstrated an output power between $46.6 - 49.3$ dBm and a DE between $45 - 85$ % over the bandwidth from $0.45 - 1.95$ GHz. The PA was designed to operate in back-off under modulated signal conditions where the gain is higher than that at saturated power and the efficiency is lower. This PA delivers

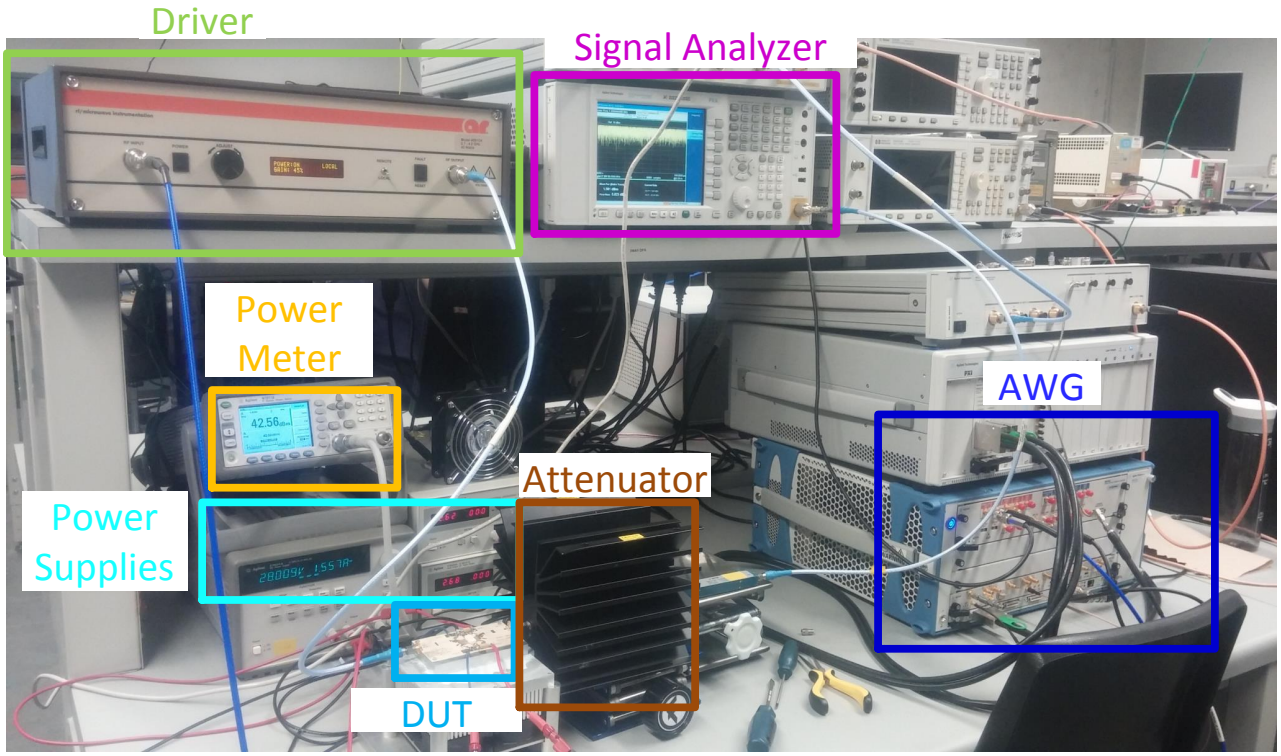


Figure 3.22: A photograph of the measurement setup.

Table 3.1: List of equipment used in the measurement setup.

Component	Model	Notes
AWG	Keysight M8190A	12 GSa/s which can generate signal at RF
Power Meter	Keysight N1911A	Offset with measured attenuator value
Driver 1	Freescale MRF6V3090N	Used over 0.47-0.7 GHz
Driver 2	AR 40S1G4	Used over 0.65-2.0 GHz
Supply1	Keysight N6705B	Used with CW measurements
Supply2	Keysight E3634A	Used with modulated signal measurements
Attenuator		Rated 300 Watts average with 30 dB attenuation
PXA	Keysight N9030A	Effective IF bandwidth of 160 MHz

significantly higher output power and competitive DE compared to other publications using custom made MMIC transistors [26] (see Table. 3.2).

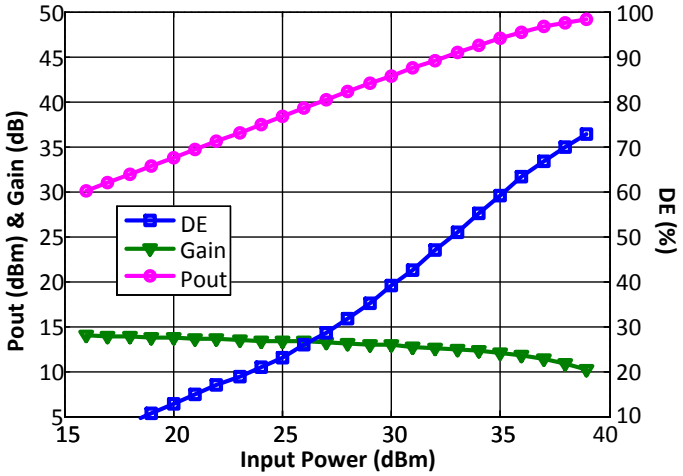


Figure 3.23: Large signal measurements of the designed PPPA at 1.2 GHz showing gain, DE and saturated output power as a function of Pin.

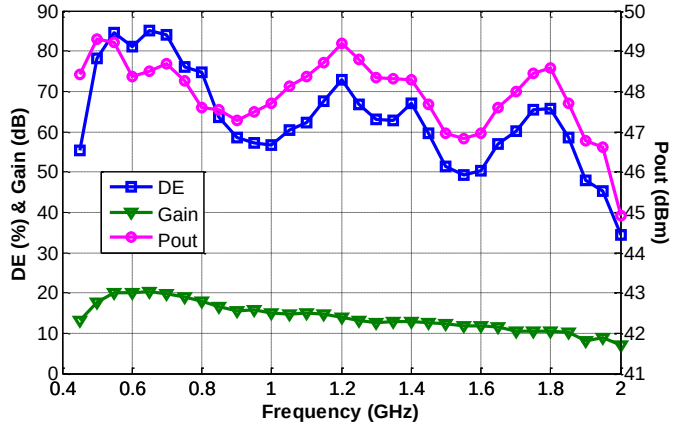


Figure 3.24: Large signal measurements of the designed PPPA showing gain, DE and saturated output power.

Further measurements were conducted to test the linearizability of the PA under single-band modulated signals. The test signal applied was a four carrier WCDMA 1001 signal with a bandwidth of 20 MHz and a PAPR around 7.2 dB. The input power level was

Table 3.2: Comparison of RF PCB based push-pull PAs.

Ref	Frequency (GHz)	FBW (%)	Input balun	Output balun	Packaged transistor	DE (%)	P_{out} (dBm)
[31]	0.25-3.1	170	No	Yes	Yes	35-73	43-46
[26]	0.5-2.5	133	Yes	Yes	No	48-65	41-43
This work	0.45-1.95	125	Yes	Yes	Yes	45-85	46.6-49.3

varied depending on the gain of the PA and the average output power before and after linearization was kept the same. It was possible to linearize the signal with DPD using a dynamic deviation reduction-based Volterra approach as outlined in [65]. The adjacent channel leakage ratio (ACLR) was measured over the bandwidth to be around −50 dBc, which is 20 dB lower than the case without DPD. The measured average DE was between 25% and 42%, and the output power was above 39 dBm between 0.65 and 1.95 GHz (Fig. 3.25). Various other test signals were successfully linearized including an 80 MHz broadband signal consisting of four carrier WCDMA and 20 MHz long term evolution (LTE) signals with a PAPR of 9.4 dB. The power spectral density (PSD) of the latter signal before and after linearizion is shown in Fig. 3.26.

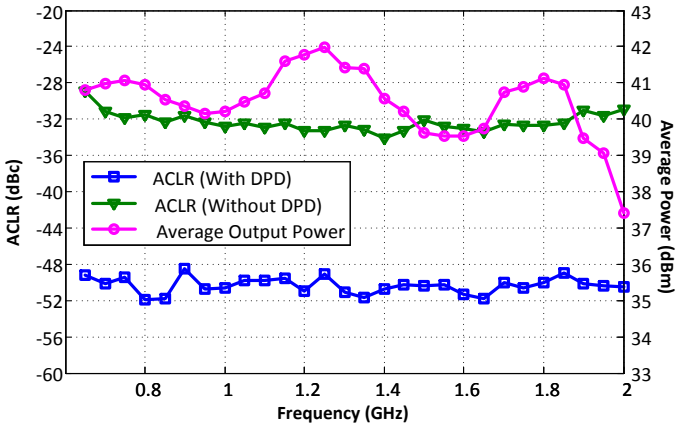


Figure 3.25: Measured ACLR and average output power (with and without DPD) at the PPPA output when driven with a single band signal 1001 WCDMA.

The PA was also tested with inter-band carrier aggregated dual- and tri-band signals. The dual-band signal consisted of a 15MHz 101 WCDMA and a 15 MHz LTE signal and

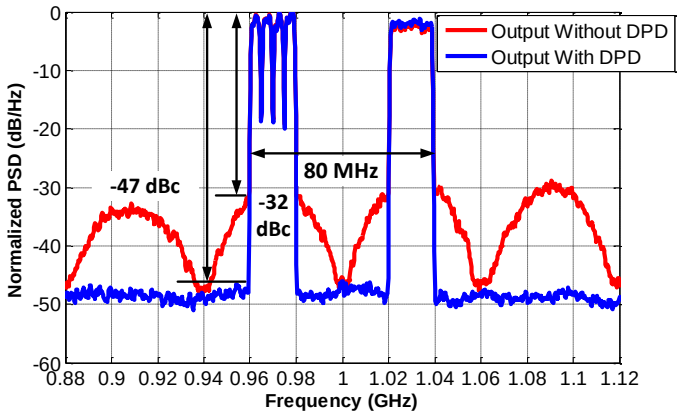


Figure 3.26: Measured output spectrum of the PPPA with and without DPD when driven with an 80 MHz broadband signal consisting of four carrier WCDMA and 20 MHz LTE signals with PAPR of 9.4 dB centred around 1.0 GHz.

had a PAPR of 9.3 dB, while the tri-band signal consisted of a 20 MHz 4C WCDMA signal, a 20 MHz LTE signal and a 20MHz 1001 WCDMA signal and had a PAPR of 9.4 dB. The inter-band signals were linearized successfully using a dual-band baseband equivalent (BBE) Volterra DPD approach, described in [66] and multi-band BBE volterra [67]. The tri-band measurement results are shown in Fig. 3.27. Ultimately, given the high PAPR of multi-band communication signals it is imperative to incorporate ET into PAs to enhance back-off efficiency and allow for truly multi-mode multi-band PA performance.

Ideally the PPPA should suppress all even order harmonic content at the output of the PA. However, due to transistor mismatch and balun imbalance, part of the second harmonic will leak out. After linearizing the single band 1001 WCDMA signal, the second harmonic power level was measured relative to the fundamental output power. The measured relative power of the second harmonic was below -40 dBc as shown in Fig. 3.28. This illustrates the relative robustness of the PPPA in comparison to single ended PAs as it requires less filtering for the second harmonic at the output of the PA. This helps in reducing the design requirements on the blocks following the PA.

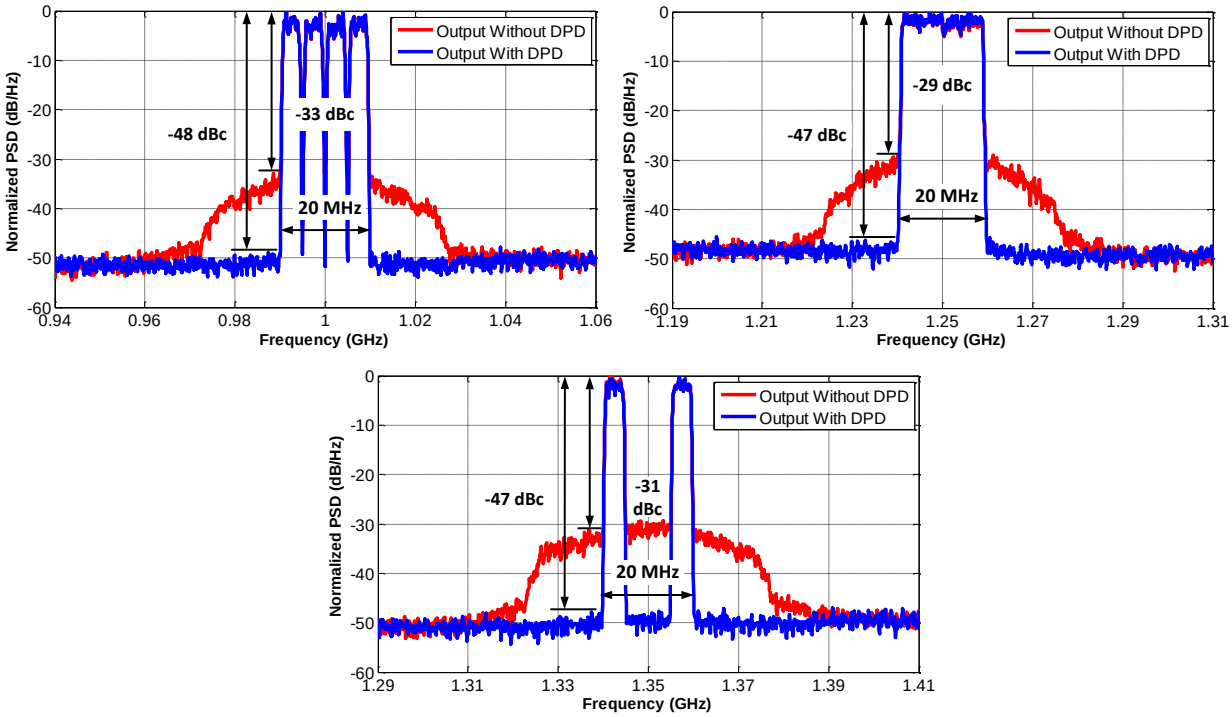


Figure 3.27: Measured output spectrum of the PPPA with and without DPD when driven with a tri-band signal consisting of four carrier WCDMA, 20MHz LTE and 101 WCDMA signals with PAPR of 9.4 dB centered around 1.0, 1.25 and 1.35 GHz respectively.

3.4.1 Sources of Error

There is a significant discrepancy between simulation and measurement which can be attributed to multiple sources of error. The typical sources of error in PA design are the inaccuracies of the transistor model, substrate permittivity, and substrate thickness. Those might explain some of the discrepancy. However, the majority of the discrepancy is attributed to differences between the exact assembly of surface mount device (SMD)s and how they were simulated. To elaborate, the discrete components placed on the layout were not accurately simulated in this work to account for pad parasitics. Moreover, the mounting structure was composed of two parts to allow for the use of a highly conductive liquid metal thermal compound. The liquid metal reacts with aluminum, hence the carrier for the transistor was is from brass. The main base is made from from aluminum as it is cheaper and easier to mill. The two parts are shown in Fig. 3.29. When these two were put together the contact between them might have been imperfect enough to cause a weak

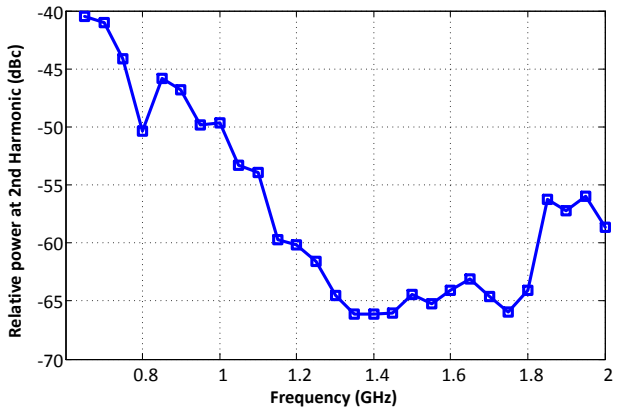


Figure 3.28: The measured relative power density of the second harmonic relative to the fundamental power density vs the fundamental frequency of the modulated signal.

contact between the grounds of the transistor and the ground of the PCB. These issues were accounted for in later designs which led to much better match between simulation and measurement.

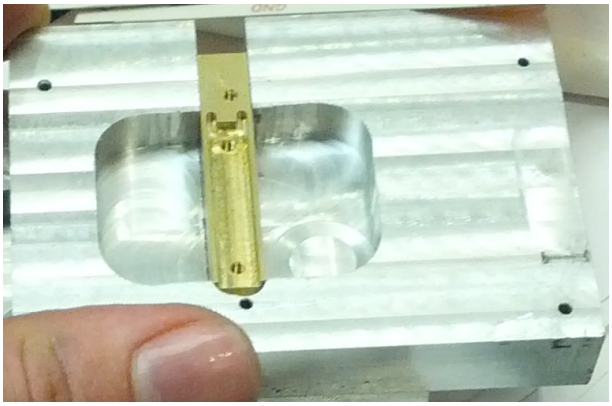


Figure 3.29: The PPPA mounting structure showing the carrier (brass) and main base (Aluminum).

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3.5 Push-Pull DPA

Modern communication systems utilize signals with high PAPR to increase spectral efficiency. These large PAPR signals require power amplifiers with high back-off drain efficiency compared to classical PAs. The most popular efficiency enhancement technique is load modulation which is most commonly utilized in the Doherty architecture as introduced in Chapter 2. The classical DPA realization was severely band-limited by its output-combining network, but recent publications have demonstrated an alternate output combiner network capable of producing broadband DPA operation [8, 46]. However, most broadband DPA litrature do not provide sufficient insight into harmonics. This can be detrimental to the performance of the amplifier especially when it comes to the second harmonic. The push-pull topology has been demonstrated to allow for independent control of both the fundamental and second harmonic terminations and thus allow for a larger design space and consequently wider bandwidth. To the author's knowledge, only a single publication has noted the usefulness of a push-pull topology in controlling the second harmonic termination in a DPA, but the authors did not provide a sufficiently high bandwidth of operation to confirm the push-pull's potential to exceed an octave bandwidth of high efficiency performance [7]. The co-design methodology is then used to integrate push-pull into the Doherty architecture to demonstrate the potential bandwidth enhancement capability of this solution. This work presents a broadband PP-DPA with broadband second harmonic control, integrated bias networks, and asymmetric biasing. We begin by discussing the advantages of a PP-DPA topology in terms of second harmonic termination control, then presents balun integration techniques into the output combiner network which enables the implementation of an octave PP-DPA. The implementation and measurement results are then presented along with a comparison table outlining the performance of the fabricated PP-DPA against state-of-the-art publications.

3.6 PP-DPA With Controlled Second Harmonic Termination

Several broadband DPA publications have demonstrated the use of a broadband impedance inverter in the output-combining network of a DPA. However, most of these publications, such as [8] did not discuss the second harmonic termination, therefore are missing an important design consideration. This oversight has the potential to significantly reduce the efficiency of the PA [68]. One way to solve this problem is by utilizing a balun in a push-pull topology. The balun provides a unique ability to isolate the odd harmonics from the even

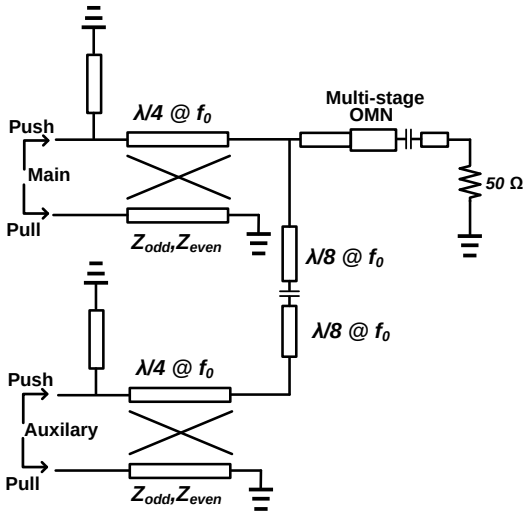

Figure 3.30: The schematic of a broadband combining network for Doherty Power Amplifiers with push-pull transistor topology.

harmonics and exceed an octave bandwidth with high efficiency operation [26, 31, 68]. A recent work has realized the advantages of push-pull and has combined it with the broadband DPA output network. However, the authors did not demonstrate an octave performance, possibly due to the placement of the transmission line between the balun and the transistor, and the choice of a Guanella based balun [7]. The challenge of PP-DPA is in the integration of the baluns in the output combiner network to maintain tight control over the second harmonic and allow for proper fundamental impedance matching. Fig. 3.30 shows the proposed output-combining network using the uncompensated Marchand balun topology.

This topology was chosen based on the following key inherent characteristics: the even-mode termination is concentrated around the open-circuit region, the magnitude and phase balance that can be achieved is quite good and sufficient for the application, and it has a very broad bandwidth that can easily exceed an octave [26, 31]. Contrary to the placement of transmission lines proposed in [7], for the balun to be used effectively it must be placed in very close proximity to the transistor, otherwise the second harmonic termination might be dispersed into a low performance region if the bandwidth is large [68]. The second harmonic dispersion at the input is contained using a floating ground plane under the transistor's package leads, which was proposed in [68]. In this work, however, the output leads are placed on an inverted balun structure eliminating the need for any transmission line between the transistor and the balun (Fig. 3.31).

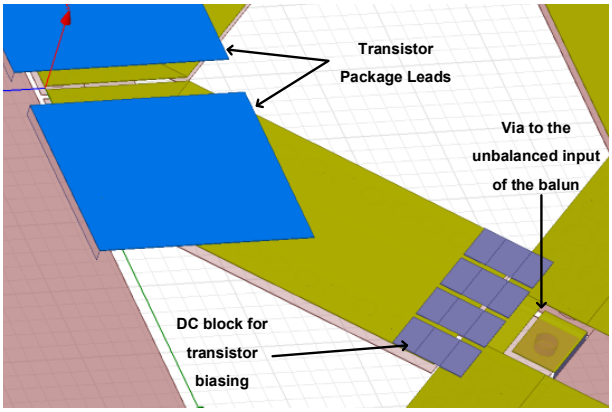

Figure 3.31: The planar version of the Uncompensated Marchand balun.

3.7 Implementation and Measurement results

A study was conducted on off the shelf high power transistors, namely the CGH40090PP by Wolfspeed, and it was found that the region of second harmonic terminations to avoid is between the angles 170^o to 200^o. To avoid these angles, two baluns were placed as close as possible to the transistors by replacing two quarter wavelength transmission lines from the combiner network with baluns of equal electrical length (Fig. 3.30). The resulting second harmonic termination is shown in Fig. 3.32 and the balance of the implemented balun is illustrated in Fig. 3.33. Asymmetric biasing was used to boost the output power of the main amplifier for increased performance. Moreover, the biasing networks were integrated into the balun by connecting them to the RF short nodes of the baluns at the input and output (Fig. 3.34).

The designed DPA was fabricated on a 12 mil Rogers RO4003C substrate using two CGH40090PP packaged transistors from Wolfspeed. Each package contains two 60 W GaN HEMT dies and the package is rated at 90 W of peak power. The completed layout is shown in Fig. 3.34.

The gates of the main transistors were biased in deep class-AB around 500 mA each, while the auxiliary was biased in class-C operation. The drains were biased with 35 V for the main amplifier and 28 V for the auxiliary. The continuous wave (CW) measurements were conducted over frequencies from 0.6 GHz to 1.5 GHz. The results for three of these frequencies are shown in Fig. 3.35. The CW measurements showed good performance over an 80% bandwidth. The output power, small signal gain and DE for both peak and back-off powers are shown in Fig. 3.36.

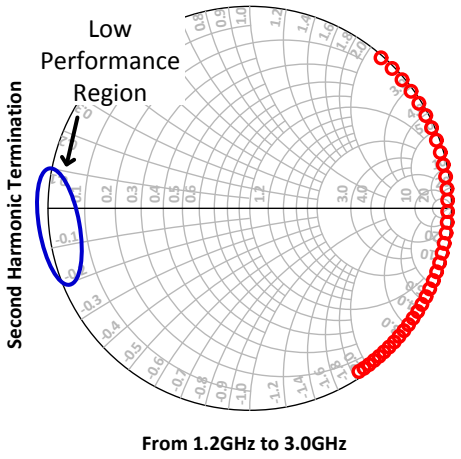

Figure 3.32: The controlled second harmonic termination at the load side.

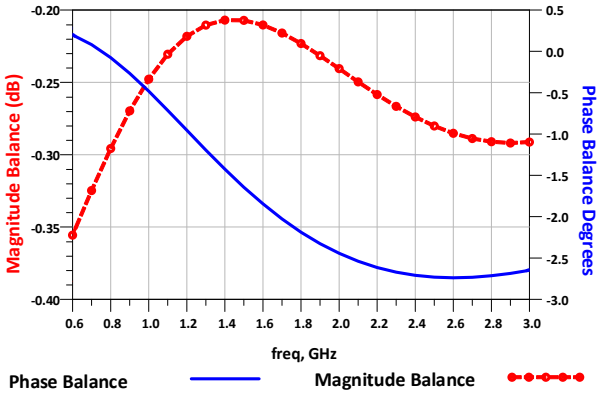

Figure 3.33: The magnitude and phase balance of the designed inverted balun at the load side.

The data was compiled and compared to other state-of-the-art broadband DPAs and PP-DPAs in Table 3.3. This work has demonstrated a wide band operation in excess of an octave which is significantly higher than comparable publications. The 6 dB back-off efficiency was also demonstrated to be above 50% over the entire band which is a significant advantage especially that the bandwidth has been has been extended. It is also important to note that the maximum frequency of operation is significantly higher which is often more challenging to design for.

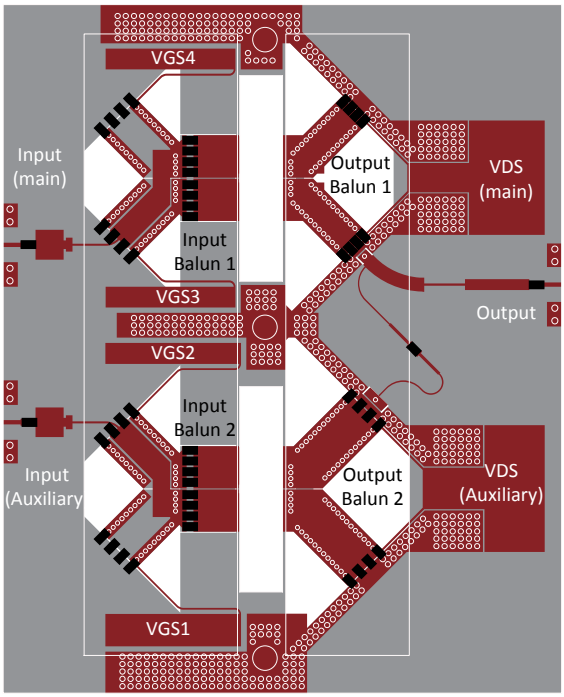

Figure 3.34: The layout of the PP-DPA demonstrator.

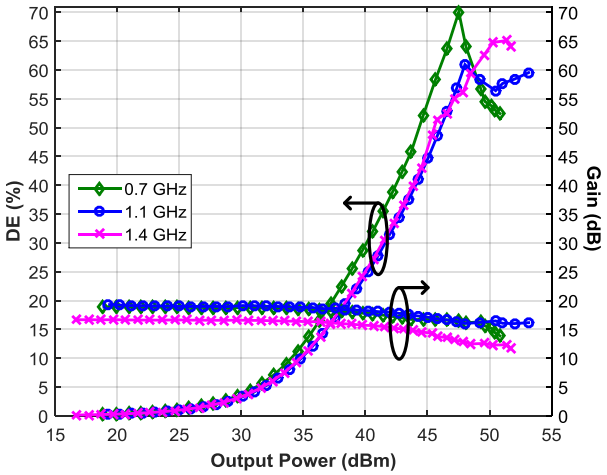

Figure 3.35: Measured drain efficiency and output power vs input power at 0.7, 1.1, and 1.4 GHz.

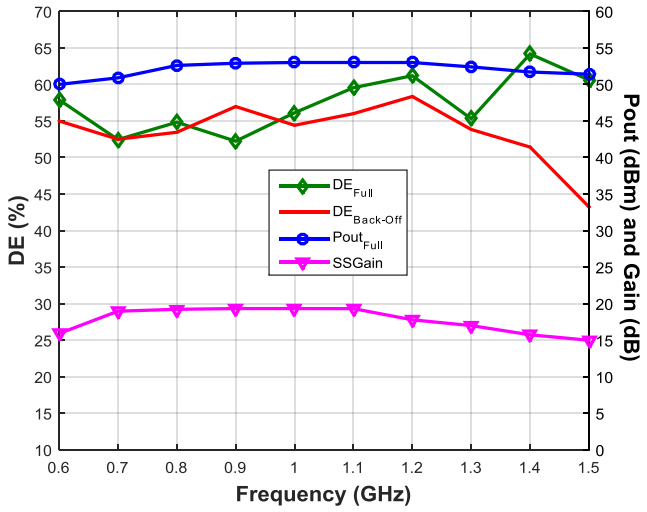

Figure 3.36: Measured peak and back-off drain efficiencies, saturated output power and small-signal gain vs frequency under CW stimulus.

3.8 Conclusion

In this Chapter the effect of the second harmonic termination on efficiency was illustrated. A strict control of the second harmonic termination using planar baluns was shown to allow for better efficiency over a wider bandwidth. A co-design methodology that incorporates the balun as a design aspect to improve the bandwidth potential of broadband push-pull based power amplifiers was introduced. The proposed methodology was used to design a multi-octave PPPA with planar baluns and packaged off-the-shelf transistors. A maximum output power of 85 W and a DE between 45% and 85% were demonstrated. The resulting PPPA was linearizable under single- and multi-band signals. The co-design methodology was then utilized to design a push-pull based DPA with an octave bandwidth. A mixed-signal PP-DPA demonstrator was successfully designed using two packaged 90 W GaN HEMT transistors. The PP-DPA demonstrated a saturated output power of 51.5 dBm $\pm$1.5 dB and a 6 dB back-off efficiency between 51% and 58% from 0.6 GHz to 1.4 GHz while the saturated power efficiency was between 52% and 64%.

Table 3.3: Comparison between this work and other state-of-the-art DPAs and PP-DPAs.

Parameter	[8]	[46]	[7]	This work
Freq (MHz)	470-803	790-960	522-762	600-1400
Topology	DPA	DPA	PP-DPA	PP-DPA
BW (%)	52	19.5	37.5	80
Min/Max P_{6dB} (dBm)	52.5/53	48.5/49	51.5/52.5	44/47
Min/Max P_{Sat} (dBm)	58.4/59	54.5/55	57.5/58.6	50/53
Min/Max DE_{6dB} (%)	42/46[(1)]	48/50	42/50	51/58
Min/Max DE_{Sat} (%)	49/56[(1)]	56/60	55/63	52/64

[(1)] Based on the average efficiency of pulsed measurements.

Chapter 4

A Series-Connected-Load Doherty Power Amplifier With Push-Pull Main and Auxiliary Amplifiers for High-Power Applications

4.1 Introduction

The previous chapter introduced the co-design methodology and demonstrated its usefulness through two prototypes. The first is a multi-octave PPPA and the second is an octave PP-DPA. The methodology enables the designer to exploit the balun's ability to control the second harmonic termination independently of the fundamental impedance at the same frequency. Now that an approach to designing broadband high efficiency Doherty PAs has been developed around 200 W, we investigated the potential challenges of implementation at even higher powers. High power Doherty PAs have been widely researched and several DPAs with high average efficiency and extended fractional fractional bandwidths have been reported [8, 46–49, 69–71]. It is worth noting that nearly all the prior publications on DPA are based on the conventional PCL architecture first introduced in [40], and shown in Fig. 4.1(a). This is mainly driven by the simplicity of the underlying PCL combiner circuitry which encouraged research to significantly improve the bandwidth of the PCL architecture rather than the SCL one. It was demonstrated in the previous chapter that PCL architecture can be used to achieve an octave bandwidth using digital Doherty. However, this architecture imposes a load impedance R_L that is generally equal to half of the optimum

impedance,R_{opt}, of the transistor. Deviating from this value has a significant impact on bandwidth when digital Doherty is not being utilized to compensate for the imperfection of the output combiner. Despite the mobilization of the increased breakdown voltage of GaN transistors to increase the drain supply voltage and consequently R_{opt} and R_L, when targeting hundreds of Watts of output power for macro-base stations, the value of R_L can be very low such that the size and complexity of the matching network at the output can become quite significant. This is most clearly demonstrated in [8] where a relatively long nine-segment impedance transformer based on Dolph-Tchebycheff transmission-line taper was used to synthesize 1.25 Ω from 50 Ω in order to preserve the bandwidth [72]. Unfortunately, this approach is not applicable in both high frequency applications where the substrate losses are high enough that reaching impedances around 1 Ω is not feasible.

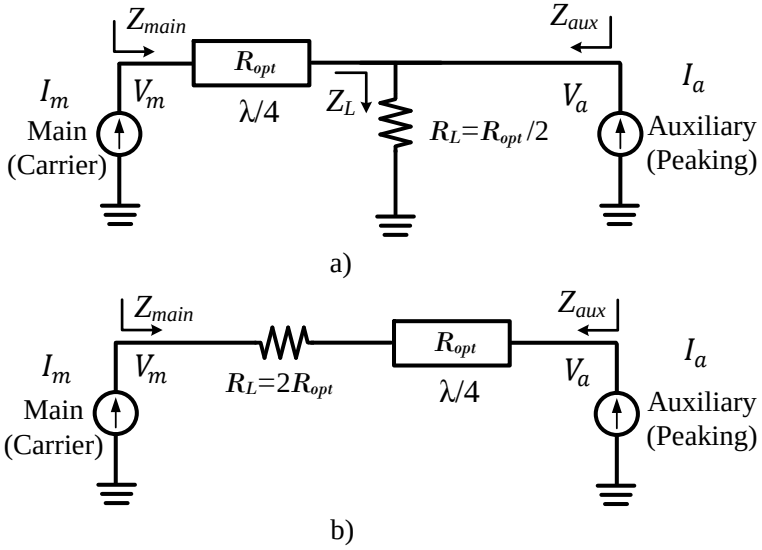

Figure 4.1: Simplified original DPA block diagrams. a) PCL DPA, b) SCL DPA.

Other publications [46, 48, 49, 69, 70] which have implemented high power PCL DPAs have demonstrated an inverse relationship between bandwidth and optimum impedance Fig. 4.2. This can be attributed to two design bottlenecks currently present in PCL DPA which are the use of higher load impedance than the conventional topology or a limitation on output impedance synthesis due to the limitations of the matching network at higher frequencies.

In this chapter, the SCL DPA architecture presented in [40] is shown in Fig. 4.1(b). SCL DPA is considered as an alternative to PCL DPA to increase the required R_L and

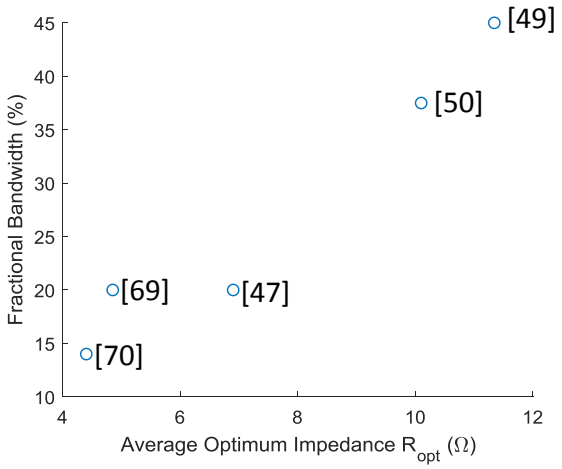

Figure 4.2: PCL DPA Bandwidth tradeoff Vs optimal impedance.

consequently alleviating the bottleneck on the bandwidth of high power DPAs caused by the output matching network. SCL DPA is a popular topology in integrated circuits. This is mostly due to the inherently differential nature of most integrated circuits which utilize the resulting virtual ground to reduce losses due to poor ground contact in the standard RF CMOS process [73–78]. As for SCL DPAs using a fully off-chip output combiners, both [71] and [79] have noted the usefulness of the basic SCL DPA for high power application due to the higher load impedance requirement. However, both publications did not demonstrate that advantage instead choosing to target low power instead where the optimal impedance is 50 Ω. Moreover, these publications did not address the variability of R_L and the implication on the rest of the combiner network.

In this chapter, the SCL DPA architecture is further generalized and used as an alternative to PCL to increase the required R_L. This increase alleviates the bottleneck on the bandwidth of high power DPAs caused by the output matching network. It starts in section 4.2, with deriving generalized ABCD parameters for the output combiner of the SCL Doherty topology as function of R_{opt} and R_L. It also provides a thorough analysis of the impedances seen by the main and auxiliary transistors as function of R_L and R_{opt}. This analysis highlighted the intrinsic advantage of using SCL which allows an increase in R_L by a significant factor compared to the one used in conventional PCL DPAs. This increase, consequently, broadens the achievable bandwidth for a given high power transistor size (i.e., R_{opt}). To further increase the value of R_L by a factor of two, the high power SCL DPA incorporated push-pull main and auxiliary power stages. Section 4.3 discuses the methodology used to design a proof-of-concept high power push-pull SCL DPA. Section

4.4 outlines the prototype's assembly and measurement results. Then this chapter will end with the conclusion.

4.2 Generalized SCL DPA Output Combiner with Push-Pull Main and Auxiliary Amplifiers

In this section a generalized formulation of the output combiner of SCL DPA topology will be presented. Using the new formulation, a new design space will be defined to allow for an arbitrary load impedance to be selected. In combination with push-pull topology this proposed architecture offers more than an order of magnitude up scaling of the load impedance.

4.2.1 SCL DPA with arbitrary load impedance

The conventional PCL DPA as presented in the simplified schematic in Fig. 4.1(a) requires a load impedance that's half the value of the optimum impedance of the transistors at peak power. Under this condition, the two transistors, i.e., main and auxiliary both see R_{opt} at full power due to the parallel nature of power combining. The original topology doesn't allow the change of the load resistance without changing the voltage and current profiles. A later improvement on this architecture came through the addition of two quarter wave length lines between the auxiliary and combining node as shown in Fig. 4.3. The additional degrees of freedom allowed researchers to define a much wider spectrum of solutions that allowed for significantly boosted operational bandwidth of the PCL DPA architecture and an arbitrary control of some parameters such as the load resistance R_L [46]. On the other hand, in the case of the SCL implementation shown in Fig. 4.1(b), the output load impedance is double that of the optimum impedance. Hence, by migrating from the PCL to the SCL Doherty architecture there is an immediate quadrupling of the load impedance required for the same output power, voltage and current profiles. However, the original SCL DPA topology presented in [40] and shown in Fig. 4.1(b) is not suitable for high frequency implementation due to the transistor parasitics causing a significant phase shift at the package plane. Thus, the assumption that the current source of the main amplifier is connected directly to the load is not valid at high frequencies.

To solve this problem a new output combiner topology is needed. Firstly, the output combiner representation will be generalized into a two-port network with the main current

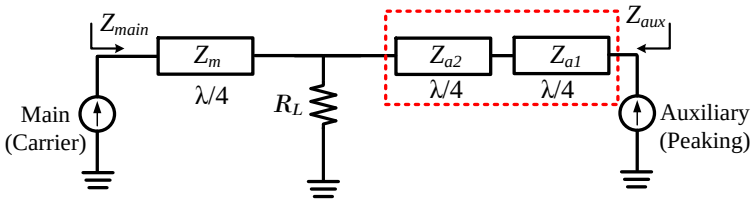

Figure 4.3: PCL DPA topology with improved bandwidth (highlighted by the dashed line).

source connected at port one and the auxiliary current source connected at port two as shown in Fig. 4.4.

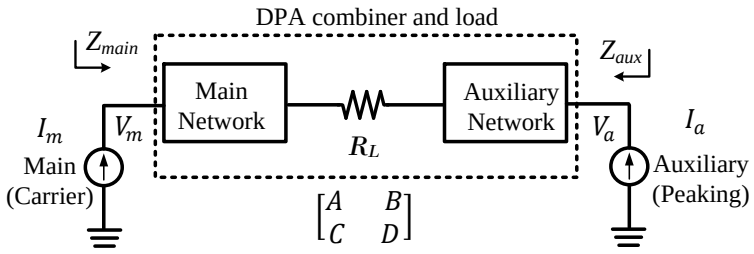

Figure 4.4: General representation of the output combiner of Doherty as a single two-port network.

The resulting relationship between the voltages and currents at the two ports are given below.

$$\begin{bmatrix} V_m \\ I_m \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_a \\ -I_a \end{bmatrix} \tag{4.1}$$

Where V_m and I_m are the voltage and current of the main current source and V_a and I_a are the voltage and current of the auxiliary current source respectively. By evaluating (4.1) at back-off and saturation conditions the following relationships can be obtained.

$$V_m^B = AV_a^B - BI_a^B \tag{4.2}$$
$$I_m^B = CV_a^B - DI_a^B \tag{4.3}$$
$$V_m^S = AV_a^S - BI_a^S \tag{4.4}$$
$$I_m^S = CV_a^S - DI_a^S \tag{4.5}$$

Where the superscripts B and S denote back-off and saturation conditions, respectively. In order to solve for A, B, C and D the voltage, current and load modulation profiles need to be defined. There is an infinite number of these profiles depending on the bias conditions, sizes of the transistors i.e., maximum current and transconductance, back-off level, and phase relationship between the main and auxiliary transistors. In this work, the drain voltage and current profile as a function of the back-off level (k). This is the typical approach used the literature which will be used as a way of illustration. The analysis can be repeated for any voltage and current profiles and the resulting change will affect the boundary conditions which will lead to another solution. The voltage, current and load modulation profiles are shown in Fig. 4.5. Using the voltage and current profiles and assuming that the phase of the auxiliary voltage is constant for all power levels, it is possible to derive the following relationships for a real load DPA.

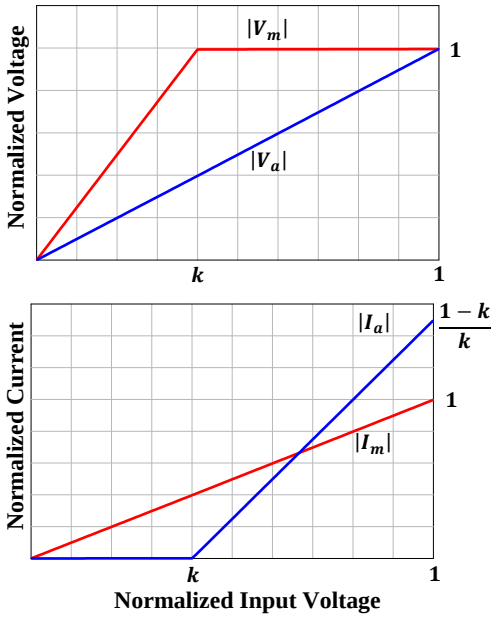

Figure 4.5: Voltage, Current and load modulation profiles for symmetric drain bias and arbitrary back-off level.

$$\frac{V_m^B}{I_m^B} = \frac{R_{opt}}{k} \tag{4.6}$$

$$\frac{V_m^S}{I_m^S} = R_{opt} \tag{4.7}$$

$$I_a^B = 0 \tag{4.8}$$

$$\frac{I_m^S}{I_a^S} = \frac{k}{1-k} e^{-j\theta} \tag{4.9}$$

$$\frac{V_m^B}{V_a^B} = \frac{1}{k} e^{-j\theta} \tag{4.10}$$

Where R_{opt} is the optimum impedance of the main transistor at peak power and θ is the phase of the auxiliary current I_a relative to the main current I_m. Based on these boundary conditions the generalized matrix can be defined as shown in (4.11).

$$ABCD = \begin{bmatrix} \frac{e^{-j\theta}}{k} & \frac{R_{opt}}{e^{j\theta}} \\ \frac{e^{-j\theta}}{R_{opt}} & 0 \end{bmatrix} \tag{4.11}$$

It was shown in [80] that θ can only take a discrete set of values for the network to be realizable using passive elements. In this simplified analysis θ can take one of two values $[\pm 90^o]$. The value of $\theta = 90^o$ is used in the following example. Now that the overall ABCD matrix is derived for an arbitrary back-off level, it is possible to derive the individual ABCD matrices for generalized SCL Doherty. To do that, the output combiner was defined as three separate networks which are the main, load, and auxiliary networks as shown in Fig. 4.6. The main and auxiliary networks are assumed to be lossless and reciprocal which leads to the conclusion that the diagonal elements are real values while the off diagonal elements are purely imaginary [81]. As a result, the problem is simplified and the number of unknowns we need to solve for is reduced.

The combination of the three individual networks can be easily obtained by multiplying all three ABCD matrices symbolically resulting in (4.12)

$$ABCD = \begin{bmatrix} jC_a\eta + A_mA_a & D_a\eta + jB_aA_m \\ jC_a\zeta + C_mA_a & D_a\zeta - C_mB_a \end{bmatrix} \tag{4.12}$$

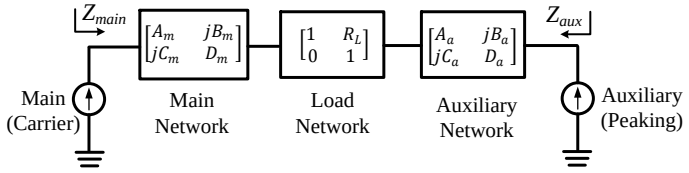

Figure 4.6: Generalized SCL DPA topology with real load impedance R_L.

Where

$$\eta = (jB_m + A_m R_L) \tag{4.13}$$

$$\zeta = (D_m + jC_m R_L) \tag{4.14}$$

By equating (4.11) with (4.12), it is possible to solve for the individual networks. The main and auxiliary networks are given by equations (4.15) and (4.16), respectively. B_m and R_L are free variables such that when B_m is set to zero we can get a unique set of networks for an arbitrary value of R_L. It is important to note that using the resulting network parameters, the main and auxiliary networks can be synthesized at the center frequency using an infinite set of network topologies which are not necessarily equivalent at other frequencies.

$$\begin{bmatrix} A_m & jB_m \\ jC_m & D_m \end{bmatrix} = \begin{bmatrix} -\sqrt{\frac{R_{opt}}{kR_L}} & jB_m \\ 0 & -\sqrt{\frac{kR_L}{R_{opt}}} \end{bmatrix} \tag{4.15}$$

$$\begin{bmatrix} A_a & jB_a \\ jC_a & D_a \end{bmatrix} = \begin{bmatrix} \frac{-B_m}{R_{opt}} & j\sqrt{kR_L R_{opt}} \\ \frac{j}{\sqrt{kR_L R_{opt}}} & 0 \end{bmatrix} \tag{4.16}$$

To demonstrate the findings, an example composed of a set of three quarter wave transmission lines were arranged as shown in Fig. 4.7. The values of these transmission lines were deduced using the ABCD parameters derived in (4.15) and (4.16), and are given by (4.17), (4.18) and (4.19)

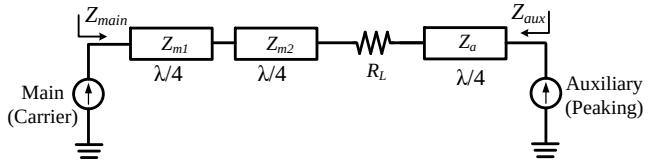

Figure 4.7: SCL DPA topology with arbitrary real load impedance R_L.

$$Z_{m1} = \frac{R_{opt}}{k} \tag{4.17}$$

$$Z_{m2} = \sqrt{\frac{R_{opt}R_L}{k}} \tag{4.18}$$

$$Z_a = \sqrt{kR_{opt}R_L} \tag{4.19}$$

The resulting Doherty combiner was then evaluated for different value of R_L and the impedances presented to the main are shown in Figs 4.8 and 4.9 at back-off and saturation respectively. It can be seen that for this particular topology, increasing R_L reduces the variation of the impedance vs frequency for the main amplifier. Consequently, using a value of R_L that is higher than that in the original SCL DPA is advantageous and desirable in high power applications.

However, it is observed that for the specific topology shown in Fig. 4.7, the variation in the real value of the impedance presented to the auxiliary amplifier is non-negligible. However, when compared to the PCL topology using the the same R_L values, it presents less variations.

4.2.2 Push-Pull in the Doherty Architecture

The use of the push-pull topology in the Doherty architecture offers two major advantages. Firstly, the baluns provide a unique ability to separate the second harmonic termination from that of the fundamental impedance. Secondly, the use of a balun to combine power doubles the required impedance at the current source of the transistors at the expense of added complexity. Moreover, there are other minor advantages to using a push-pull

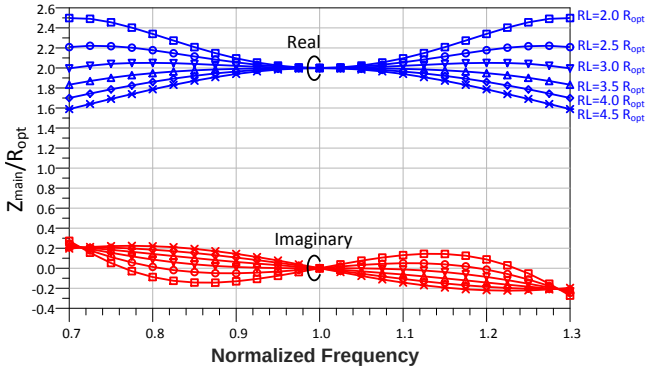

Figure 4.8: The impedance presented to the main amplifier at back-off as a function of frequency for multiple R_L values.

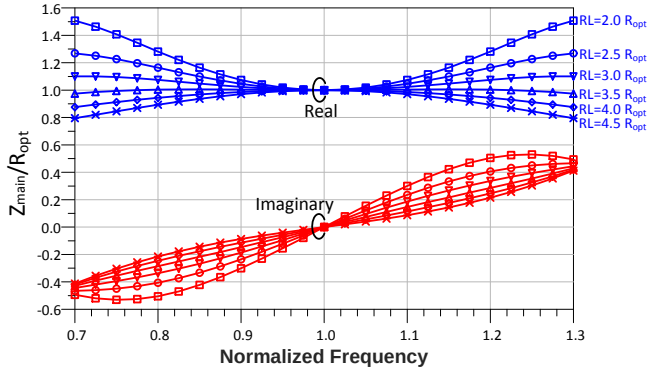

Figure 4.9: The impedance presented to the main amplifier at full power as a function of frequency for multiple R_L values.

topology in DPA architectures. For instance, undesired load modulation can occur at the second harmonic frequencies and standard DPA implementation do not typically deal with the harmonic current leaking from the auxiliary to the main and vice versa. These currents can be significant enough to push the transistor's 2^{nd} harmonic termination well outside the Smith chart in trajectories that are difficult to predict. This is especially true for the auxiliary transistor when it is off where the leakage current from the main transistor is relatively high [26, 31, 68]. When it comes to baluns, the impedance transformation ratio, bandwidth, magnitude and phase balance are some of the balun's parameters of interest when designing a power amplifier. The uncompensated Marchand balun topology was found to have superior balance and bandwidth and was previously demonstrated to

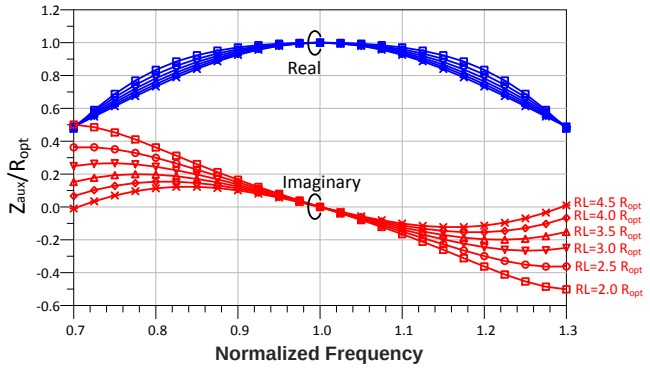

Figure 4.10: The impedance presented to the auxiliary amplifier at full power as a function of frequency for multiple R_L values.

be suitable for the use in standalone push-pull topologies and in Doherty power amplifiers [26, 31, 68, 82]. It was also demonstrated in [68, 82] that the baluns are best placed in close proximity to the transistor to prevent the second harmonic termination from dispersing into a low performance region.

4.3 On The Design of SCL DPA with Push-Pull Main and Auxiliary Amplifiers

In order to demonstrate the principle of load impedance scaling while limiting the output power to fall within the capability of our equipment, 28 volts transistors were chosen instead of higher voltage alternatives. This choice, along with a targeted power of around 350 Watts results in an optimum impedance that is extremely low in comparison to literature. The communication bands between 700 MHz and 950 MHz are targeted given the popularity of these bands in high power macro cell base stations. In the case of PCL Doherty, from Fig. 4.3 it can be seen that the required load impedance Z_L at the junction is half the optimum impedance required by the main current source, i.e., main transistor at peak power. For the case of a 350 Watts Doherty power amplifier R_{opt} is around 2.24 Ω this implies that Z_L should be equal to 1.12 Ω for the PCL DPA case. This is a very low impedance which is challenging to match to from 50 Ω especially for broadband designs. For the SCL DPA, as shown in Fig. 4.1(b), the Z_L value required is 4.5 Ω. However, the original SCL DPA topology is not suitable for high frequency applications where the transistor and package parasitic introduce significant phase shift between the intrinsic current source and package

planes. The generalized solution given by (4.15) and (4.16) introduced in 4.2, can help resolve this issue as they expand the design space significantly. For instance, the topology exemplified in Fig. 4.7 can be used instead of the original topology to allow for parasitic absorption into the output combiner using techniques presented in [8, 83].

4.3.1 Parasitic absorption

In practice, the effects of the transistor's parasitics cannot be ignored especially as the transistor operates higher in frequency. In this design the parasitics were significant around the band of operation and needed to be absorbed into the output combiner during the design process. Moreover, since the main and auxiliary amplifiers are connected in push-pull topology to doubles the required R_{opt} in turn doubling the required Z_L to $9\,\Omega$, the use of push-pull introduces additional transmission line and parasitics which limits the parasitic absorption of the transistor parasitics. Hence, the next viable option for this architecture is to replace the quarter wave line composing the auxiliary network with a three quarters wave transmission line of the same impedance as shown in Fig. 4.11. This sub-optimal but simple remedy should satisfy the auxiliary's ABCD matrix when solved for $\theta = -90^o$ and allows for a much wider degree of freedom in the auxiliary network to allow for better parasitic absorption over a wider band. Moreover, it was found that the phase difference between the auxiliary and main transistor's current leads to less impedance dispersion when kept to 90^o over the entire band rather than assuming a linear phase shift with frequency.

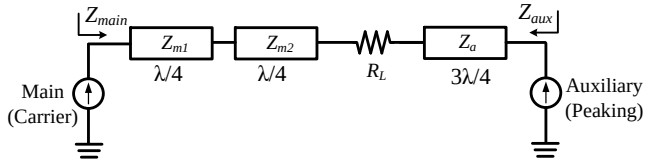

Figure 4.11: SCL DPA topology with arbitrary real load impedance R_L and extended auxiliary network.

4.3.2 Output combiner

The combiner shown in Fig. 4.11 covers a new subset of solutions that satisfy our general ABCD derivations. Hence, it produces a different frequency response as a function of R_L when compared to the exemplified topology shown in Fig. 4.7. For the new structure

the optimum value of R_L that presents the flattest real impedance for the main is around seven times the value of R_{opt} which leads to $R_L = 31.4\,\Omega$. The output combiner was then designed using the co-design methodology proposed in [68] to present the targeted response which is set by the simplified schematic model presented in Fig. 4.11. The absorption of the main transistor's parasitics into the combiner network was successfully accomplished. The comparison between the targeted impedances and the achieved ones are shown in Figs 4.12, 4.13 and 4.14. The resulting optimized network uses a differing values of R_L which was around $18\,\Omega$. The limited variability of the baluns included in the EM-simulated database and balun parasitics, introduced a practical limitation on the achievable scaling of the output impedance in this specific design. It is speculated that increasing the electrical length of the balun would allow for further scaling. However, the value achieved for R_L is already more than a magnitude higher than the initial value of $1.12\,\Omega$ and can be easily matched to from $50\,\Omega$. The possible gains to be achieved with additional balun variations are not essential to demonstrate the concept especially when the difference between the target and the realized networks is relatively small and further optimization's are needed in the realization of the complete layout.

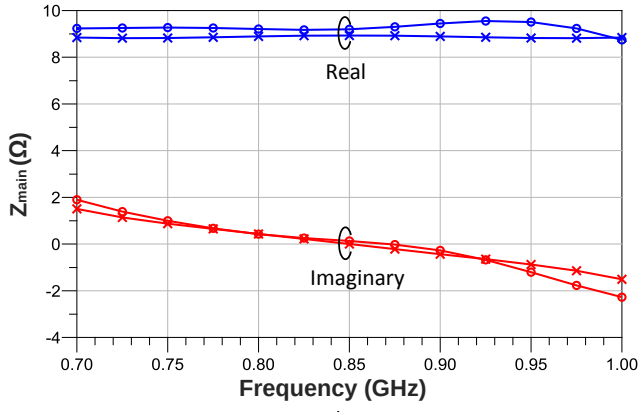

Figure 4.12: The impedance presented to the main amplifier at back-off as a function of frequency. Xs represent the impedance from the ideal auxiliary network while circles represent the impedance of the optimized network including transistor and EM simulated baluns with parasitics.

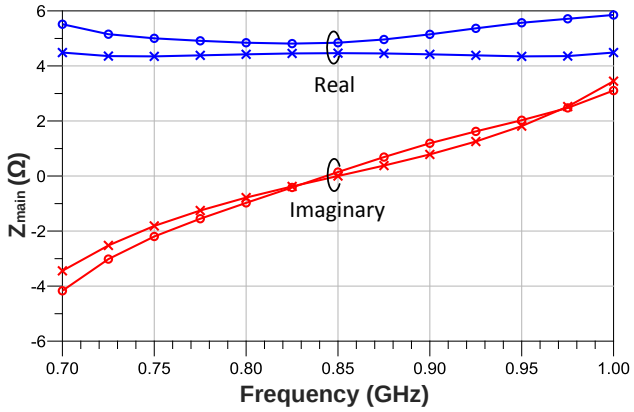

Figure 4.13: The impedance presented to the main amplifier at full power as a function of frequency. Xs represent the impedance from the ideal combiner network while circles represent the impedance of the synthesized network including transistor and baluns parasitics.

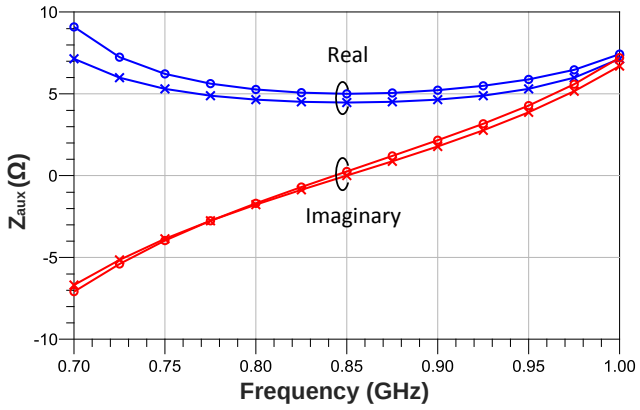

Figure 4.14: The impedance presented to the auxiliary amplifier at full power as a function of frequency. Xs represent the impedance from the ideal auxiliary network while circles represent the impedance of the optimized network including transistor and EM simulated baluns with parasitics.

4.3.3 Input Splitter

Based on the obtained output combiner, the input matching was designed to provide impedances that produce sufficient gain for the DPA operation and a phase shift around

90^o between the main and auxiliary intrinsic current sources. The splitting was done using X3C09A2-03 from Anaren which is a 90^o surface mount hybrid coupler with sufficiently good isolation to minimize the effect of the input reflection. The initially designed input and output networks were further optimized together to improve bandwidth in terms of power, back-off efficiency and phase difference. The intrinsic current sources had phase difference difference between $85^o - 103^o$ at saturation which is close to the targeted 90^o.

4.3.4 RF Balun Layout and considerations

The balun used in this design is based on the uncompensated Marchand balun topology and the balun layout is illustrated in Fig. 4.15. This particular layout was also used in the design of the PP-DPA presented in the previous chapter. While the layout was originally adapted from literature [20], there are two novel changes in the adaptation used in this work. First, the balun's top and bottom metal layers are flipped to allow the transistor's package leads to be placed on top of the balun. This minimized the effect of the parasitic capacitance added by the package leads which is important to maintain the second harmonic impedance within an acceptable range. Second, the balun's grounding was established using capacitors which allows us to have a ground at RF and a suitable place to insert the biasing network. Note also that these capacitors can be placed on the top metal due to the flipped nature of the balun. The two parameters, L and W were used to control the balun's odd and even mode impedances. This balun layout is suitable for sub 6 GHz applications using standard substrates. However, possible implementations using low temperature co-fired ceramic (LTCC) or thin film for example can extend the usability of this balun layout to frequencies over 6 GHz.

4.3.5 simulation results

The final schematic of the EM simulated layout is shown in Fig. 4.16. The EM simulation of the input and output networks where conducted separately to reduce memory usage. All SMDs were placed as lumped ports as accurately as possible to represent the physical placement for higher accuracy. The simulation was done using Ansys HFSS due to its excellent 3D simulation capability which is needed for the baluns used in the design. It is important to note that after fabrication there were large signal oscillation issues which were dealt with at the expense of lower bandwidth than the original design. The results of the fully EM simulated are shown in Fig. 4.17. Based on the simulation results, the bandwidth defined by 55 dBm ± 1 dB is from 670 MHz to 985 Mhz which translates to

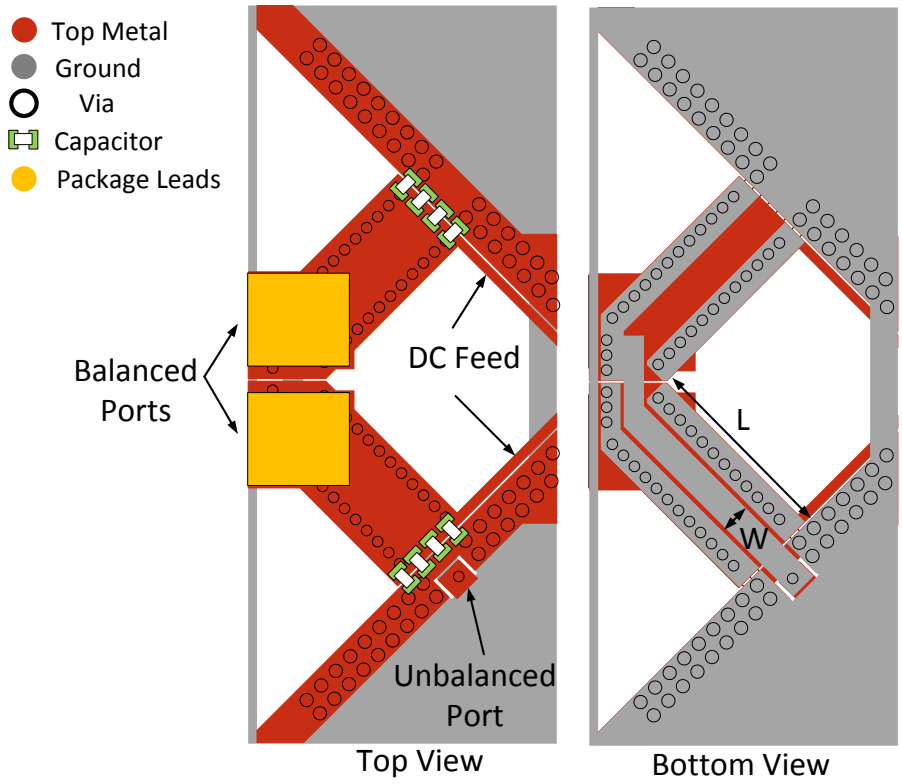

Figure 4.15: The layout view of the inverted planar version of the uncompensated Marchand balun.

38% of factional bandwidth in simulation. The back-off efficiency was found to be between 46% and 57% which is comparable if not better than literature. This is achieved using the lowest relative value of R_{opt} given the power and drain voltage. Our objective is to demonstrate the ability of this topology in significantly raising the required value of R_L while maintaining high bandwidth and back-off efficiency. The value of R_L was raised by an order of magnitude when compared to conventional PCL DPA without push-pull.

4.4 Prototyping and Measurements

The push-pull based SCL DPA prototype was fabricated on a Roger's substrate RO4003C with 12 mil thickness. Four Wolfspeed CGH40120P transistors were used in the design with a 28 V drain supply. The overall prototype was 7 inches in height and 5.8 inches in

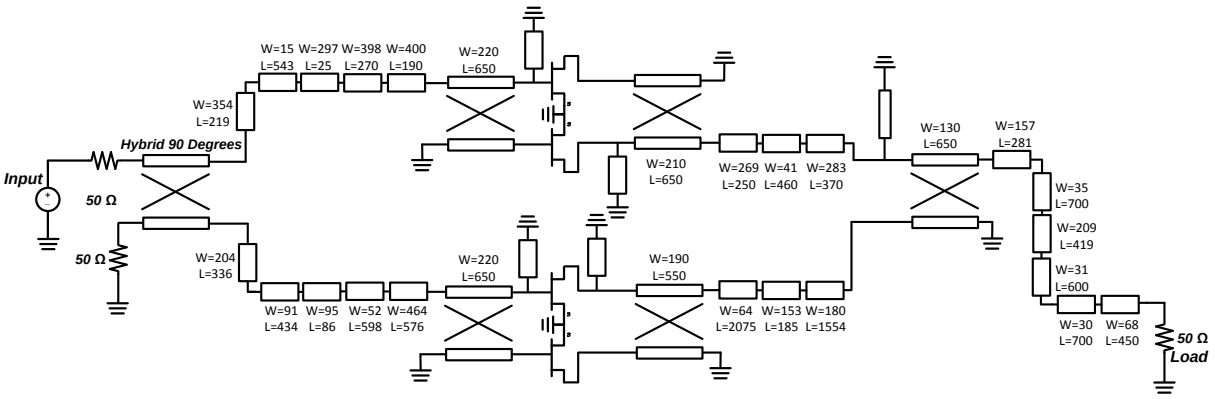

Figure 4.16: Simplified schematic with all units defined in mil. Note that the balun dimensions are defined in the same manner done in [68].

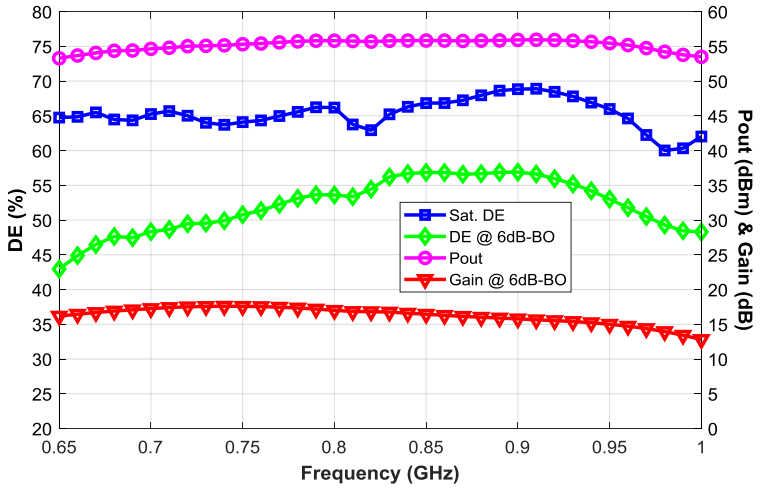

Figure 4.17: Simulation results over frequency of the EM simulated layout.

width and is shown in Fig. 4.18. In order for the baluns to provide high coupling coefficient for better magnitude balance the base on which the layout is mounted was fabricated with five cavities to accommodate the 5 planar baluns as shown in Fig. 4.19.

The pulsed measurements were done using two pulsed signals with a 10% and 15% duty cycle and repetition period of $100\mu s$ for both. The two measurements were used to extrapolate the drain current value at 100% duty cycle and the results are shown over frequency in Fig. 4.20 and vs output power in Fig. 4.21. The assumption used during the extrapolation is that the off state current is equal in all duty cycles. This assumption

Figure 4.18: Photograph of the push-pull based SCL DPA prototype.

Figure 4.19: Photograph of the base with balun cavities.

was verified at low power and was found to be a reasonable assumption with some error. Normally this technique cannot be used in DPA designs where the main and auxiliary use the same supply. However, in this case the auxiliary and main are biased independently

and the average current was measured separately.

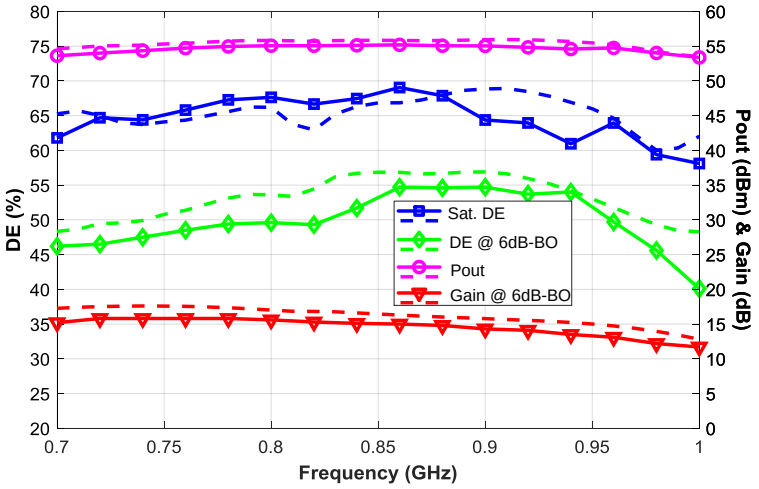

Figure 4.20: Pulsed signal results Vs Frequency showing measurement results (Solid) compared to simulation (Dashed).

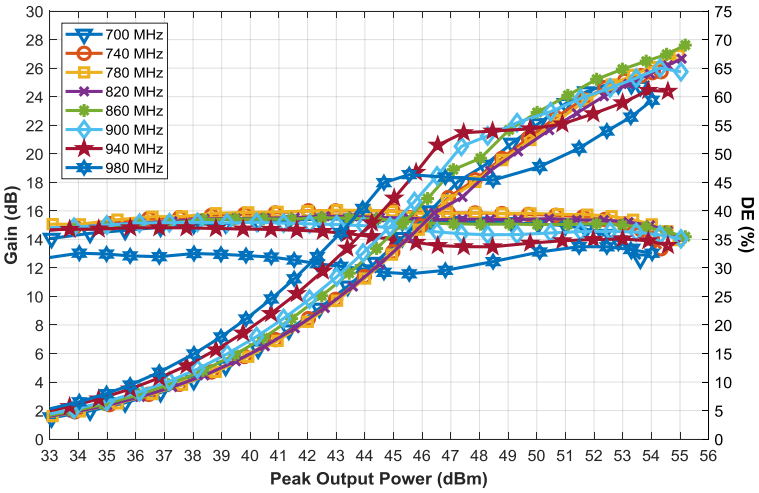

Figure 4.21: pulsed signal results Vs Output power.

The modulated signal measurements was conducted using the measurement setup photographed and annotated in Fig. 4.22. The measurements were done using a $20MHz$ and $40Mhz$ signals with a PAPR of $7.1dB$ and $8.8dB$ respectively. The signal with lower

PAPR was used to test the performance of the PA under realistic practical conditions. The $20MHz$ signal was successfully linearized as shown in Fig. 4.23. The linearizion was conducted within the band at key frequencies and the performance of the PA such as average and peak output power, average drain efficiency and ACLR was measured as shown in Fig. 4.24. It is important to note the higher than expected average efficiency for the signal when compared to the efficiency at $6dB$ back-off. This difference could be attributed to the fact that the pulsed signal was kept to safe low levels to avoid possible thermal damage to the transistors especially at such high powers. This policy might have underestimated the saturation power obtained using pulsed measurements and by extension underestimated the corresponding $6dB$ back-off power and efficiency. The resulting average efficiency was maintained above 50% between $740MHz$ and $960MHz$ while being successfully linearized with an ACLR between $48 - 50.5dBc$

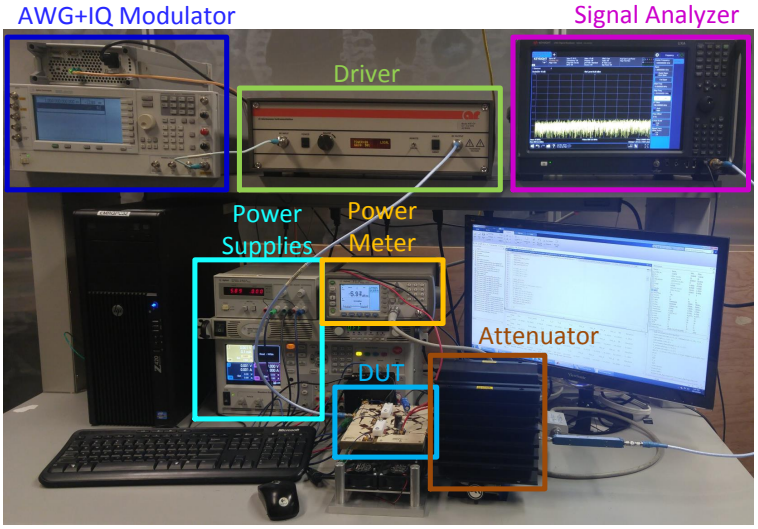

Figure 4.22: Photograph of the measurement setup used to test the prototype design.

In order to test signals with wider bandwidth a $40MHz$ 8 carrier CDMA signal was chosen and the linearizion was successful as shown in Fig. 4.25. Linearizion of wider bandwidth signals became challenging due to practical limitations in terms of limited dynamic range due to driver nonlinearity at such high power levels.

This work was then compared to similar state-of-the-art publications as shown in table 4.1. This design has successfully demonstrated the advantage of push-pull based SCL DPA in significantly raising the required load impedance for easier broadband matching. It can be seen that there is a clear inverse relationship between the targeted optimal impedance

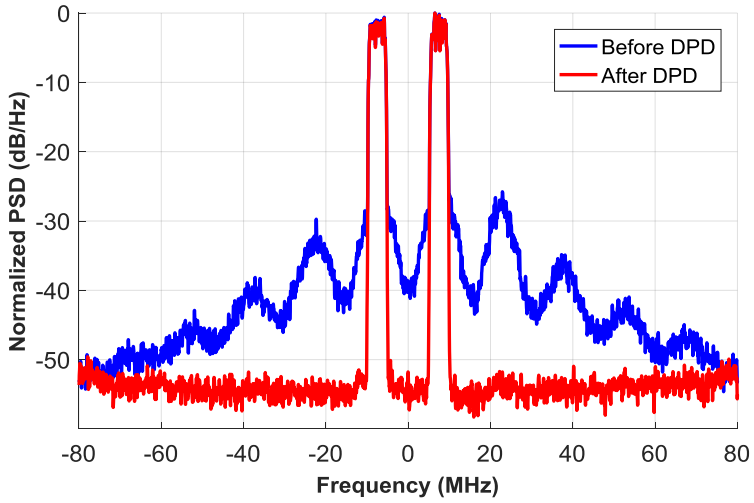

Figure 4.23: 20MHz 1001 WCDMA Modulated signal output before and after DPD.

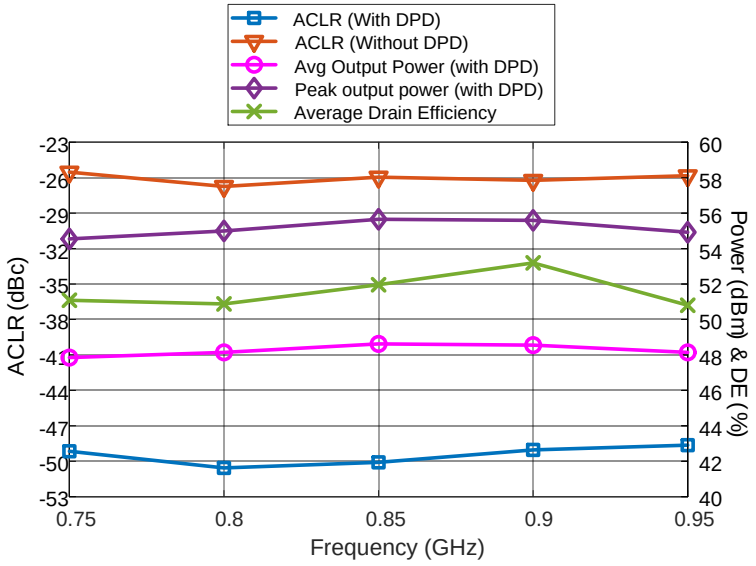

Figure 4.24: Modulated signal results Vs Frequency.

and bandwidth which is possibly caused by the trade-off between bandwidth and load impedance in the case of PCL DPA.

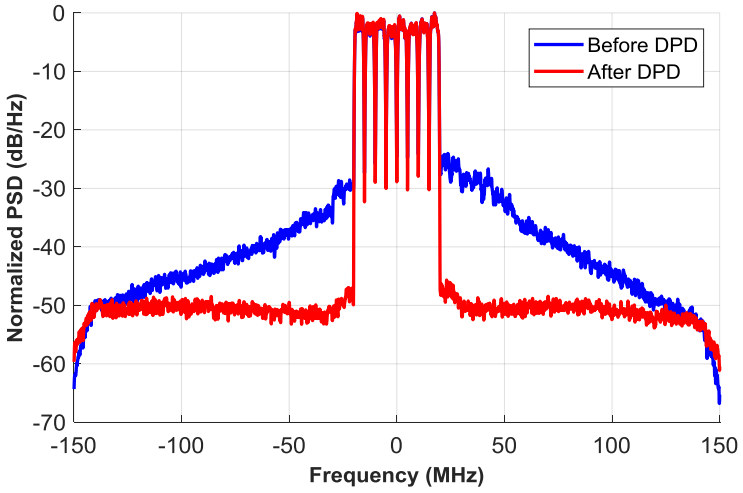

Figure 4.25: 40MHz 8 Carrier WCDMA Modulated signal output before and after DPD.

Table 4.1: Comparison table with relevant publications.

Work	Frequency MHz (%)	$P_{o_{Sat}}$ (dBm)	DE_{-6dB} (%)	DE_{Sat} (%)	VDS	Norm. R_{opt}
[8]	$470-803(52\%)$	$58.4-59$	$42-46^{(1)}$	$49-56^{(1)}$	50	$3.12-3.57\Omega$
[48]	$1700-2700(45\%)$	$52.7-54.3$	$40-50$	$53-66$	50	$9.29-13.4\Omega$
[49]	$650-950(37.5\%)$	$53.7-54.2$	$48-58$	$51-72$	50	$9.5-10.7\Omega$
[46]	$790-960(20\%)$	$55-55.5$	$48-50$	$55-62$	48	$6.5-7.3\Omega$
[69]	$1800-2200(20\%)$	$56.7-57.6$	>50	–	50	$4.4-5.3\Omega$
[70]	$820-940(14\%)$	$56.5-58$	>50	–	48	$3.65-5.15\Omega$
T.W.	$720-980(30\%)$	$54-55.5$	$45.2-54.6$	$59-69$	28	$2.2-3.1\Omega$

(1) Based on the average efficiency of pulsed measurements.

4.4.1 Sources of Error

There is minor discrepancy between simulation and measurement which can be attributed to multiple sources of error. The typical sources of error in PA design are the inaccuracies of the transistor model, substrate permittivity, substrate thickness and assembly. Moreover,

process and temperature variations have been noticed during the measurements which affected the peak power measured during the pulsed measurement. These errors collectively can explain the discrepancies between the measurement and simulations.

4.5 Conclusion

This chapter has demonstrated a new technique to extend the bandwidth of high power DPAs when constrained by very low load impedance. The SCL Doherty architecture was analyzed and the output combiner was generalized to accommodate an arbitrary R_L. The new derivations enabled a significant increase to the required R_L without the drawbacks that are associated with increasing R_L in PCL DPA architecture. Moreover, to maintain strict second harmonic termination for high efficiency performance, push-pull main and auxiliary transistors were used. The use of push-pull adds an additional doubling of the required R_L for the same power. The proposed technique was tested with a demonstrator that achieved powers around 55 dBm $\pm$1 dB over a fractional bandwidth of 30% with a 6dB back-off efficiency around 50 % when measured with a pulsed signal. The modulated signal test showed a linearity greater than 48 dBc with an average efficiency greater than 50% for a signal with 7.1 dB PAPR over the majority of the covered bandwidth.

Chapter 5

Conclusion

The transition into data-centric services and increased demand for more bandwidth stems for the growth of infotainment applications which spurred rapid advances in wireless communication technology. The network capacity was increased by the allocation of additional bands of the RF spectrum to service providers. Furthermore, spectrally efficient communication standards were created using advanced modulation schemes which typically have high PAPR and require PAs with high back-off efficiency. Back-off efficiency enhancement techniques such as ET and Doherty introduce bottlenecks on the operational bandwidth. It is quite challenging to resolve these bottlenecks in order to service all bands with a single RF front-end. Moreover, this problem is more pronounced in very high output power PAs as high output power PAs utilise low output impedance and broadband matching networks are harder to design the closer the impedance is to the edge of the Smith chart. This thesis introduced a new design methodology specific to push-pull based PAs and a new topology which reduces the bandwidth problem that stems for matching to very low impedance for high power PAs employing the Doherty architecture.

In this thesis, various balun implantations were investigated and a push-pull based amplifier co-design approach was introduced along with a proof of concept prototype. The prototype PA demonstrated a multi-octave high efficiency operation which is among the best in its class of high power using packaged off-the-shelf devices. Moreover, it was also demonstrated that the output combiner of a DPA can be modified to incorporate a push-pull topology for its main and auxiliary branches without bottle-necking the bandwidth. A prototype DPA was built with a dual input single output approach to demonstrate the broadband potential of the proposed output combiner topology. Finally, the low output impedance requirement for high power parallel connected DPAs was significantly increased. It was shown how PCL DPA implementation favours output impedance values much lower

than the optimum impedance for each transistor. It was later demonstrated that a SCL Doherty topology favours output impedance values much higher than the optimum impedance. This advantage was leveraged further through the use of push-pull for an order of magnitude increase in the output impedance required when compared to more conventional DPA implementations.

5.1 Summary of Contributions

The main objective of this work was to develop a new methodology to design broadband high output power PAs with high back-off efficiency that is suitable for base stations applications. Targeting these objectives has led to the following contributions:

1. In this work, we have introduced a co-design methodology specific to push-pull based PAs. The methodology addressed the importance of controlling the second harmonic impedance in order to realize a high efficiency performance of high power and high frequency PAs. It was demonstrated how the modular approach which is typically used in designing high power push-pull based PAs could result in significant dispersion of the second harmonic termination at frequencies around and over 1 GHz. It was demonstrated how this dispersion could affect broadband PAs as it could place the second harmonic impedance in a low efficiency range for part of the bandwidth. The dispersion of the second harmonic was significantly reduced by bringing the balun as close as possible to the transistor terminals. The co-design methodology addressed the challenges with this approach as the balun has to become an integral part of the design process. The co-design methodology treated the balun as one of the variable design parameters that can be synthesized in conjunction with the rest of the network. As a demonstration, a multi-octave push-pull PA was designed using the proposed co-design methodology. Practical challenges dealing with the package parasitics and bias network have been addressed during the design of the prototype. The measurement results showed a fractional bandwidth of 125% and an output power around 48 dBm peaking at 85 Watts. The a peak power efficiency was between 45-85%. The prototype PA was also successfully linearized under modulated signal conditions using a 7.1 dB PAPR signal. The performance was comparable to relevant works in literature while using off-the-shelf package transistors at a relatively higher power. This contribution provided a methodology to design broadband PAs with high peak-power efficiency.

2. The co-design methodology was then extended to design broadband DPAs in order to

boost the back-off efficiency of broadband PAs. While existing literature on broadband DPAs demonstrated the incorporation of baluns in the output combiner of PCL DPA topology, they did not minimize the second harmonic dispersion and the balun was placed after the package leads. The package leads were not electrically long enough to affect their performance since they were operating at a relatively lower frequency. Moreover, the balun was fixed during the network synthesis process. The co-design methodology was adapted to broadband PCL DPAs by completely absorbing the package leads into the balun's structure and allowing dynamic balun parameters to vary during the synthesis of the output combiner. A dual input prototype PP-DPA was designed to operate over an octave of bandwidth with a 6 dB back-off efficiency greater than 50%. This performance was better than existing literature in terms of bandwidth and back-off efficiency combination.

3. The output combiner of SCL DPA was investigated as a solution for the low load impedance requirements of high power DPA where the requirement for the load impedance (R_L) can approach 1 Ω. The PCL DPA output combiner requires an R_L that is half the optimum impedance of the transistor while the output combiner of SCL DPA requires an R_L that is two times the optimum impedance of the same transistor. This four times advantage of the SCL DPA's output combiner has lead further investigation of this topology. A generalized formulation of the SCL DPA's output combiner was introduced. This resulted in a topology where an even higher scaling of the required R_L can be achieved while improving the bandwidth compared to the starting value of two times the optimum impedance. This formulation was also used to guide the synthesis of the output combiner using the extended co-design methodology for DPAs. A broadband high power SCL DPA with push-pull main and auxiliary transistors was designed with an output impedance which is 12 times higher than the conventional approach. The design demonstrated a measured bandwidth of 30% between 720 to 980 MHz and a peak power of 350 W with a peak power drain efficiency between 58 and 70% across the band and a back-off efficiency between $45 - 55\%$. A Modulated signal with 20MHz bandwidth and PAPR of 7.1 dB was successfully linearized with an average efficiency in excess of 50%. Moreover, a 40 MHz signal with PAPR of 8.8 dB was also linearizable. This was achieved with a design that had the lowest equivalent optimum impedance when compared to relevant literature.

5.2 Future Work

The work presented in this thesis was focused on bandwidth and back-off efficiency enhancement for PAs with high output power used in mobile communication base stations and broadcast transmitters. Typically, these applications rely on heavy utilization of DPD since the additional power overhead required for linearization is insignificant when compared to the total power consumed by the transceiver chain. However, in some cases the non-linearity can be quite significant that a PA cannot be linearized with a DPD. Hence, it is important in this case to investigate the linearity of the PA. The proposed topology allows for incorporating linearity enhancement techniques through the control of both second harmonic and baseband impedances. Both of which are subject to the even-mode impedance of the balun. Therefore, the balun's even-mode impedance can be used to improve linearity by controlling these impedances in isolation of the fundamental impedance.

An interesting area of research would be to investigate the potential bandwidth enhancement using transistors with on-chip matching that is particularly optimized for push-pull series connected load DPAs. Higher bandwidth is likely achievable when access to the intrinsic current source is granted as it allows for much better parasitic absorption with an optimal output combiner design. Moreover, custom integrated circuit designs of the transistor can be necessary during implementation of the topology at higher frequency. The balun's layout presented in this work might not be suitable for frequencies over 6 GHz using standard PCBs. LTCC or thin film might allow for reduction in balun layout parasitics for frequencies over 6 GHz. Alternative balun layouts might be necessary at even higher frequencies such as 60 GHz.

Lastly, it would be interesting to identify an optimum topology that is specifically suitable for SCL DPAs based on the ABCD network derived at the center frequency. The explored variations has not been shown to be optimum and there might be potential for improvement in this area.

5.3 List of Publications

Journal Papers

1. **A. Jundi** and S. Boumaiza, "A Series Connected Load Doherty Power Amplifier With Push-Pull Main and Auxiliary Amplifiers for Base Station Applications" (Accepted with major revision) in *IEEE Transactions on Microwave Theory and Techniques*, December 2018. (Based on Chapter 4)

2. **A. Jundi**, H. Sarbishaei, and S. Boumaiza, "An 85-W Multi-Octave Push-Pull GaN HEMT Power Amplifier for High-Efficiency Communication Applications at Microwave Frequencies,"*IEEE Transactions on Microwave Theory and Techniques*,vol. 63, pp. 3691-3700, November 2015. (Based on Chapter 3)

Conference Papers

1. **A. Jundi**, K. Patel, and S. Boumaiza, "An Octave High Power Push-Pull Doherty Amplifier With Broadband 2nd Harmonic Termination Control," in 2016 *IEEE MTT-S International Microwave Symposium Digest*, pp. 1–4, 2016. (Based on Chapter 3)

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