# Concurrent Dual-band Doherty Power Amplifiers for Carrier Aggregation

by

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A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Master of Applied Science
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2017

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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## Abstract

Carrier aggregation is the main feature of the Long Term Evolution advanced (LTE-A) standard to increase the spectral efficiency and communication bandwidth. It calls for wireless transmitters to be multi-band and multi-standard to meet the demands of various deployment scenarios. In addition, these transmit radios must efficiently amplify signals characterized with a high peak-to-average power ratio (PAPR), which is caused by advanced modulation schemes. These two factors highlight the need for the multi-band Doherty power amplifier (DPA), which allows the transmitter remain in high efficiency at back-off power levels and maintain that high efficiency over multiple frequency bands.

In this work, a novel output combining network is presented for the dual-band DPA design with extended fractional bandwidth for carrier aggregated signals. The proposed output combiner employs a modified Π-shape network, which enables the absorption of output capacitances from both the main and peaking devices and eliminates the need for phase offset lines which are major sources of bandwidth limitation in the existing multi-band DPAs. In addition to performing the impedance inversion, the proposed combiner incorporates the biasing feeds and presents small low-frequency impedances to both the main and peaking transistors. The inclusion of the bias feeds and small low low-frequency impedance feature improves the linearizability of the DPA when stimulated with concurrent dual-band modulated signals. Lastly, by using the gain contour at the back-off power level, the non-linear AM-AM response caused by the varying input capacitance of the main transistor is mitigated.

The proposed dual-band output power combiner and the back-off gain contour technique were applied to design of a dual-band two-way Doherty PA using the commercialized 25W Gallium Nitride (GaN) transistor. Measurement of the two-way DPA shows a gain of 7.5 - 9.5 dB at 2.05 - 2.3 GHz and 9 - 11 dB at 3.2 - 3.62 GHz. The efficiency at 6 dB back-off is greater than 49% and 47% across the two frequency bands. The linearizability of the dual-band DPA is validated using various carrier aggregated signals. The PA exhibits linear behaviour when driven by up to 80 MHz intra-band carrier aggregated signal and 20 MHz concurrent dual-band signal after DPD.

Additionally, carrier aggregated signals usually lead to a PAPR value between 8-10 dB. The efficiency of classic two-way DPA deteriorates when dealing with such signals. To cope with the efficiency deterioration, a three-way DPA was designed. Simulations of the three-way DPA show that the gain is greater than 9 dB within the two frequency bands, 2.05 - 2.32 GHz and 3.35 - 3.65 GHz. The efficiency at 10-dB back-off is greater than 40% in the two frequency bands.

**Acknowledgements**

I would like to express my profound gratitude to my supervisor Prof. Slim Boumaiza for giving me the opportunity to learn in EmRG and providing me guidance on my research. Without Prof. Boumaiza's continued support and supervision on my work, it would have been impossible to achieve my goals.

I would also like to thank all my colleagues in EmRG for being very supportive during my studies, especially Hamed and Yushi for their valuable technical discussions on PAs. Thanks to Ayman and Kasyap for their help with the fabrication of heat sinks, Hai for his help with digital pre-distortion, Arthur and Eric for proofreading my thesis.

Finally, I would like to thank my family and my husband for their unconditional love, support and encouragement the entire way.

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# Chapter 1

# Introduction

## 1.1 Motivation

The communication services have evolved from pure speech or text towards more diversified multimedia over the years. These applications require the wireless systems to have wider communication bandwidth, higher data throughput resulting in the co-existence of new communication standards, such as Long Term Evolution Advanced (LTE-A), and existing legacy systems, such as Wide-band Code Division Multiple Access (WCDMA).

The new wireless standards use the concept of carrier aggregation which enables them to increase the communication bandwidth, and thereby increase the data throughput. Figure 1.1 presents three cases in carrier aggregation, (a) intra-band, contiguous, (b) intra-band, non-contiguous and (c) inter-band, non-contiguous. These application scenarios call for the radio frequency (RF) units capable of operating at multiple bands and concurrently processing various signals over a wide range of carrier frequencies within each band. Moreover, the modern wireless standards impose high linearity requirements on radio transmitters to minimize out-of-band leakage such that the leakage does not interfere with the signals in the adjacent channels.

Additionally to further increase the data throughput, wireless communication standards employ advanced modulation schemes resulting in communication signals with a high peak to average power ratio (PAPR). Figure 1.2 shows an example of a four-carrier WCDMA signal's time domain envelope waveform along with its probability density function (PDF). As seen, the amplitude of the signal shows a large variation over time. This requires transmitter to operate at a power backed off from the nominal peak power in order to

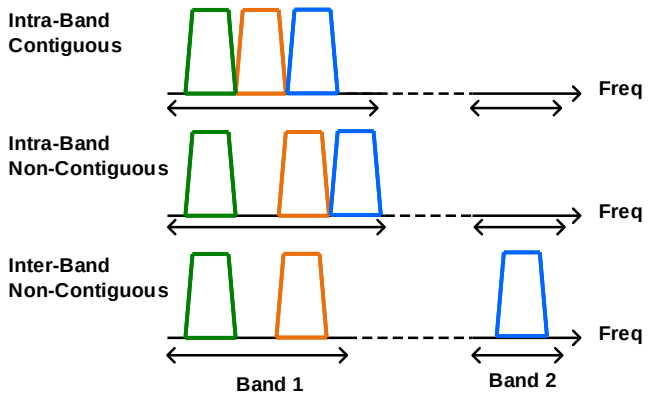


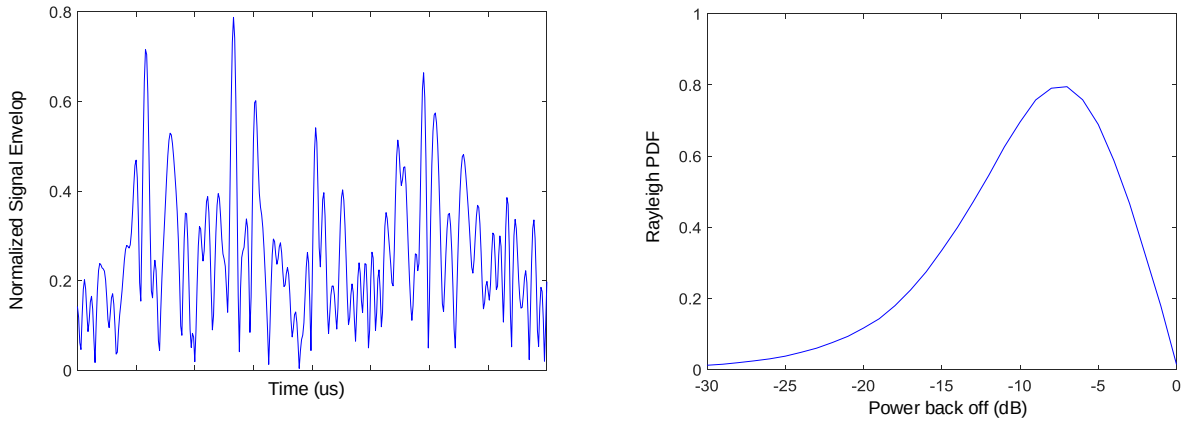

Figure 1.1: Three carrier aggregation scenarios

prevent clipping of the signal. According to the signal statistics, the transmitter will mostly likely operate at this back-off power level most of the time. Hence on average, the power efficiency of these transmitters are degraded.

In conclusion, the modern wireless standards have eventually highlighted the need for radio transmitters to have high average power efficiency, high linearity, multi-band operational capability and good fractional bandwidth in each band to meet the stringent performance requirement of the wireless communication system.

## 1.2 Problem Statement

The PA is typically the last stage of the transmitter and consumes the most power in the transceiver. The power efficiency of the PA dominates the total power consumption of the overall system. A PA with a low efficiency will result in large amounts of heat generation in the transistors and will reduce the reliability of the device. Different classes of operation modes have been proposed to enhance the efficiency performance of the PA like Class AB, B/J, C, F, $F^{-1}$, etc. In these operation modes, the transistor have a great efficiency improvement around the saturation region, while at the power back off, the efficiency degrades quickly. For example, the achieved average efficiency in the modern transmitter with a Class AB/J PA falls in the range of 15%-25% [4][30], which can not satisfy the efficiency requirements in modern communication systems.




(a) (b)

Figure 1.2: (a) Envelop waveform of 4C-WCDMA signal. (b) Probability density function of the signal

Several approaches, such as envelope tracking (ET) [28][15], linear amplification using non-linear components (LINC) [22] and Load Modulation Technique (also called Doherty) [5] have been addressed to deal with efficiency degradation in the single ended PAs. Among these techniques, the Doherty Power Amplifier (DPA) is investigated heavily due to its simple implementation, good capability of maintaining linearity and large potential fractional bandwidth compared to the other approaches.

In the recent years, there has been an increasing amount of research in multi-band DPAs. However, most of these works were focused on the building block approach where the single-band output matching network, phase offset lines and dual-band impedance inverters are pre-implemented and their main focuses are on replacing each building block with its dual-band equivalent circuits [27],[26]. This has caused a large design complexity and a significant bandwidth degradation and performance deterioration in at least one of the targeted frequency bands. Moreover, they have not demonstrated the capability of dual/multi-band DPA for carrier aggregation scenarios.

In this thesis, a novel output combiner network (OCN) and a back-off gain contour based input matching network (IMN) are presented for the design of dual-band two-way and three-way DPA. The proposed output combiner reduces the design complexity and extends the operational bandwidth of the existing dual-band DPAs. This approach enables the concurrent amplification of the carrier aggregated signals and reduces the cost and complexity of base-station transmitters.

## 1.3 Thesis Organization

The thesis is organized into the following chapters. An overview of high frequency PA is introduced in Chapter 2 summarizing the basic operation modes of a PA and a certain design strategy to achieve wideband PA design. This includes the continuum Class B/J mode which will be utilized in the Doherty PA design. The chapter will conclude with the literature review where past approaches are summarized along with the results from the state-of-the-art implementations of a dual/multi-band DPA. Chapter 3 presents a novel approach to the design of the output power combiner for the dual-band DPA. Then a implementation and simulation results for a dual-band DPA designed using the methodology are shown. To further improve the efficiency of amplifying signals with a higher PAPR, the proposed methodology was extended on designing a three-way DPA in Chapter 4. Theoretical analysis and measurement results are demonstrated. Finally, Chapter 5 concludes the research and provides suggestions for future works.

# Chapter 2

# High Power Amplifier Overview

## 2.1 Classic Operation Modes of Power Amplifier

The power amplifier is a critical component in RF transmit chain. It takes the small input power and amplifies it by consuming certain amount of DC power. The amount of amplification is defined as the gain (transducer gain). It can be calculated using the following equation

$$G = \frac{P_{del}}{P_{avs}} \tag{2.1}$$

where $P_{del}$ is the power in Watts delivered from the PA to the load and $P_{avs}$ is the power available from the source in Watts. Since the PA is located at the last stage of the transmitter, it consumes the largest power and its efficiency dominants the whole efficiency of the transmitter. The drain efficiency ($DE$) of the PA is describes as

$$DE = \eta = \frac{P_{del}}{P_{dc}} \tag{2.2}$$

where $P_{dc}$ is the DC power consumption at the drain of the transistor. $P_{del}$ is the fundamental RF frequency power delivered to the load. The equation does not contain the gain information of the PA. Hence the efficiency of the PA can also be calculated as power added efficiency (PAE) as defined by the following equation.

$$PAE = \frac{P_{del} - P_{avs}}{P_{dc}} = \eta \times (1 - \frac{1}{G}) \tag{2.3}$$

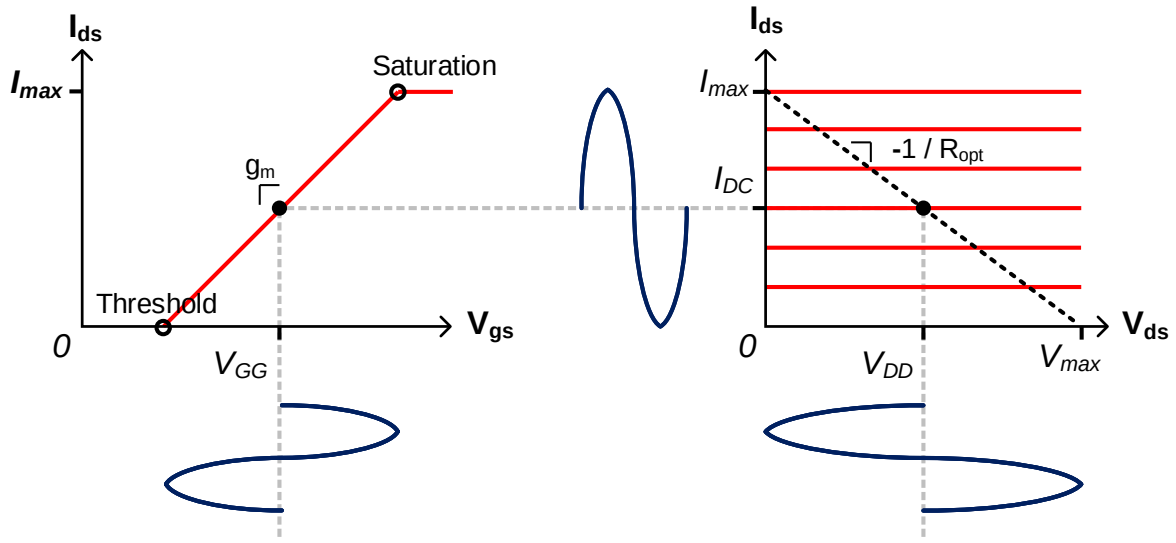



Figure 2.1: Class A operation mode

### 2.1.1 Class A Power Amplifier Mode

To show an ideal Class A power amplifier, the ideal MOSFET transistor model with zero knee voltage is developed in Keysight advanced design system (ADS). The gate biasing point for a Class A is located at the centre between the threshold and saturation as seen in Figure 2.1. The drain biasing point is set at the centre between the knee voltage and maximum supportable voltage $V_{max}$ at the drain. The instantaneous voltage and current will travel along the black-dashed line with an output impedance of $R_{opt}$ as shown in the figure.

Class A is the operation mode that the transistor is always conducting regardless of the signal is there or not. The main drawback of Class A power amplifier is that when there is no signal at the input, the transistor is still consuming a huge DC current and transforming to heat and leading to wasted power. With a zero knee voltage, Class A has a maximum drain efficiency of 50% at the peak power level when its voltage and current are reaching the maximum swing $\frac{V_{max}}{2}$ and $\frac{I_{max}}{2}$, respectively. As a result, the optimum load of the Class A has the following load impedance.

$$R_{opt} = \frac{V_{max}/2}{I_{max}/2} \tag{2.4}$$

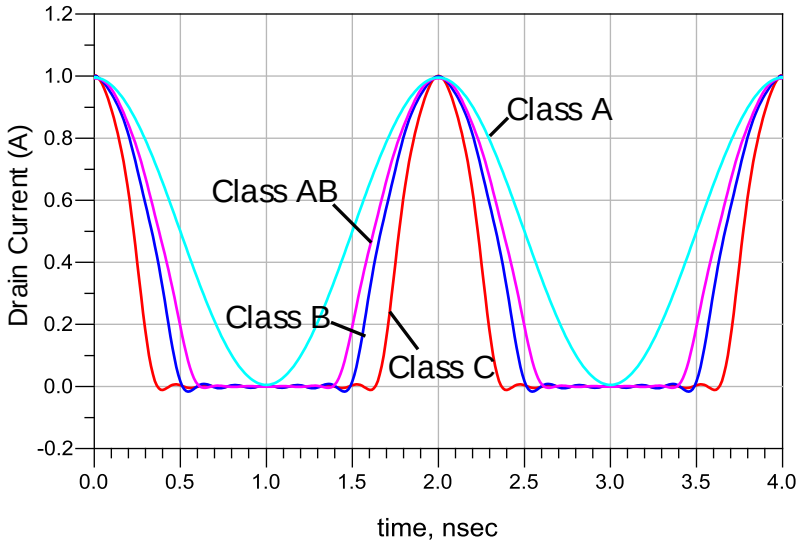



Figure 2.2: The current waveforms of Classes A, AB, B and C

When the knee voltage is non-negligible, the efficiency will be even worse. Though in low efficiency, Class A operation mode has the advantages of high linearity and high gain since the transistor always stays in the active linear region. In some application scenarios, the linearity is a more stringent requirement to the system while the efficiency is not that important, such as the low noise amplifier (LNA) in the receiver, then Class A is the top choice in these applications.

### 2.1.2 Reduced Conduction Angle mode Classes AB,B,C

Unlike the Class A operation mode, the conduction angle of Class AB, B, C mode are reduced to improve the efficiency. Conduction angle is defined as the total angle in one sinusoidal cycle that the transistor is conducting. Figure 2.2 shows the drain current waveforms for Classes A, B, AB and C. As shown in the figure, the conduction angle of class A is $2\pi$, the angle for Class B is $\pi$, the conduction angle for Class AB is between $\pi$ and $2\pi$ and for Class C, the angle is less than $\pi$. As shown in Figure 2.2, the current waveforms are clipped resulting in the appearance of harmonic components.

By decreasing the gate biasing of the transistor, the conduction angle of the device is reduced. A large portion of dynamic load line will travel along the x-axis as shown in 2.3,

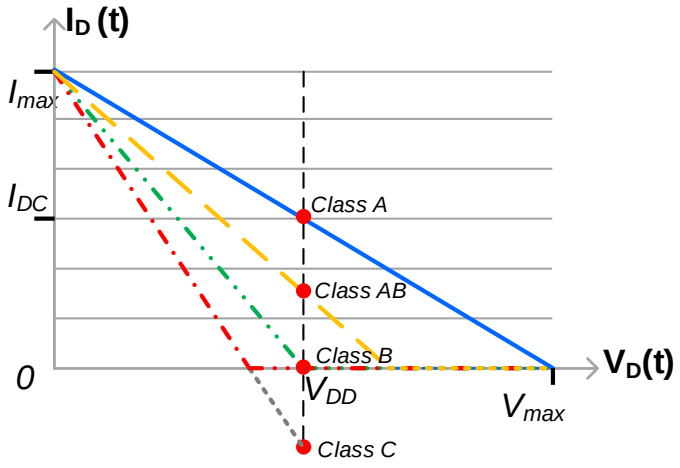



Figure 2.3: Biasing point and dynamic load line of Class A, AB, B and C

which is indicating a zero DC power consumption, ie. the transistor enters cut-off region. The Class C mode has the largest ratio of cut-off period, shown as the red dash-dot line in Figure 2.3, hence the efficiency of class C is the highest among these mentioned operation modes. A detailed numerical analysis is shown in the following paragraphs.

Assume that the transistor is terminating with an ideal harmonic short and experiencing a maximum drain current with amplitude of $I_{max}$. Knee voltage is assumed to be zero. Therefore, the drain voltage waveform will be pure sinusoidal in the time domain with a maximum swing of $\frac{V_{max}}{2}$ or equivalently $V_{DD}$, while the current waveform will be described as

$$I(\theta) = \begin{cases} 0, & -\pi \leq \theta \leq -\frac{\alpha}{2}, \\ \frac{I_{max}}{1-cos(\frac{\alpha}{2})}[cos(\theta) - cos(\frac{\alpha}{2})], & -\frac{\alpha}{2} < \theta \leq \frac{\alpha}{2}, \\ 0, & \frac{\alpha}{2} < \theta \leq \pi, \end{cases} \tag{2.5}$$

where $\alpha$ is the conduction angle and $\theta = \omega t$. By Fourier analysis, the DC and fundamental component of the drain current will be given as

$$I_{DC} = \frac{I_{max}}{2\pi} \cdot \frac{2sin(\frac{\alpha}{2}) - \alpha cos(\frac{\alpha}{2})}{1 - cos(\frac{\alpha}{2})} \tag{2.6}$$

$$I_1 = \frac{I_{max}}{2\pi} \cdot \frac{\alpha - sin(\alpha)}{1 - cos(\frac{\alpha}{2})} \tag{2.7}$$

Hence the DC power consumption, RF power output and drain efficiency can be calculated as the following (2.8),(2.9),(2.10).

$$P_{DC} = V_{DD} \cdot I_{DC} \tag{2.8}$$

$$P_{OUT} = \frac{V_{DD}}{\sqrt{2}} \cdot \frac{I_1}{\sqrt{2}} \tag{2.9}$$

$$DE = \frac{P_{OUT}}{P_{DC}} \tag{2.10}$$

In the mean time, the optimum impedance of the amplifier to obtain this output power level and efficiency would be:

$$R_{opt} = \frac{V_{DD}}{I_1} \tag{2.11}$$

From the above analysis, it is noticeable when $\alpha = 2\pi$, the transistor will obtain an efficiency of 50%. This is the maximum drain efficiency of Class A. When the conduction angle $\alpha$ is reduced to $\pi$, the drain efficiency of the transistor is 78.5% corresponding the maximum drain efficiency of Class B mode. When the transistor is biased more deeply as Class C, the drain efficiency of the transistor will fall between 78.5% and 100%. However, the transistor suffers more from intrinsic non-linear issues since the transconductance of the transistor experiences non-linearities by using in between the cut off and saturation region. This is the main drawback of the Class C operation mode.

It can also be shown that, with the same maximum output drain current, more input voltage is needed to drive the transistor with a reduced conduction angle. Thus, when the transistor is shifting from Class A to Class C, the achievable gain from the transistor decreases.

Lastly, as mentioned at the beginning of this section, since harmonic components in current are present in the reduced conduction angle modes, the harmonic impedance of the these operation modes have to be carefully controlled to obtain certain linearity and efficiency. This might complicate the design whereas only the fundamental impedance needs to be considered in Class A mode. Table 2.1 summarizes the performances of the classical operation modes.

Table 2.1: Summary of performances of classical operation modes

| Operation Mode | Gain | Linearity | Efficiency |
|---|---|---|---|
| Class A | Excellent | Excellent | Poor |
| Class AB | Good | Satisfactory | Satisfactory |
| Class B | Good | Good | Good |
| Class C | Poor | Poor | Excellent |

## 2.2 Waveform Engineered Power Amplifiers

### 2.2.1 Class F/F$^{-1}$ power amplifier

In classical operation modes, the higher order harmonic impedances are short circuited. The Class F/F$^{-1}$ amplifier, instead, utilizes the harmonics to shape the voltage/current waveform at the drain to increase the efficiency. Figure 2.4 shows the current and voltage waveform of the ideal Class F operation mode. Different from the loadline in class B mode shown as the dashed-purple line in Figure 2.4, the dynamic load line of the Class F travels along the $L-$ shape bold-red line as shown in the figure, where the product of the DC voltage and current is always zero. Hence the ideal Class F mode offers a maximum drain efficiency of 100%. Conversely, the ideal Class F$^{-1}$ operation mode has a square shape current waveform and half-sine wave voltage waveform.

Analysis has demonstrated that the power amplifier will show good efficiency performance with harmonic control up to the third[4]. Higher order harmonics control will end up with a unrealizable matching circuit to be implemented, while only obtaining small efficiency enhancements. Even that, the Class F or F$^{-1}$ for wideband or multi-band application is quite complex due to its stringent requirements on harmonic terminations. In Class F mode, the fundamental voltage component will be larger than $V_{max}$ when doing the Fourier analysis of the square voltage waveform. Therefore, the fundamental optimum impedance of the Class F mode is higher than that of Class B. It has been shown that the optimum impedance of Class F can be related to Class B through the equation 2.12.

$$R_{opt}^{F} = \frac{4}{\pi} R_{opt}^{B} \tag{2.12}$$

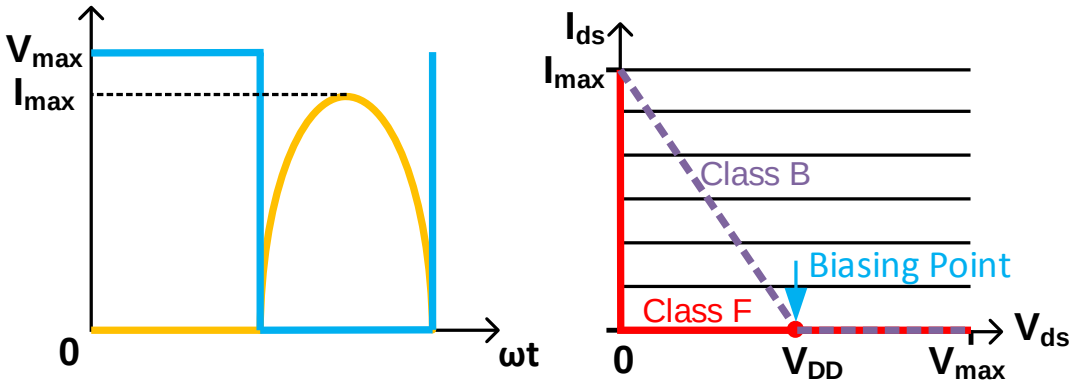



Figure 2.4: Current and Voltage waveform of Class F and dynamic loadline

### 2.2.2 Class B/J power amplifier

The continuous Class B/J operation mode is deduced from Class B mode [30, 29] by leverage the harmonic terminations to a achieve wide band operation. The current waveform of Class B/J is the same as the Class B mode as in the Equation 2.5. Using the Fourier series expansion, the current waveform of continuous Class B/J can also be described as Equation 2.13 and the voltage waveforms can be written as Equation 2.14. $I_n$ is the amplitude of the $n$th harmonic component of current. $V_1$ is the amplitude of fundamental voltage which equals $V_{DD}$ when the knee voltage of the transistor is zero. By manipulating $\beta$ from -1 to 1, a series of voltage waveforms can be generated which will maintain the same output power, efficiency and linearity theoretically as Class B ($\beta = 0$).

$$I(t) = I_{dc} + I_1 cos(\omega t) + I_2 cos(2\omega t) + \sum_{n=3}^{\infty} I_n cos(n\omega t) \tag{2.13}$$

$$V(t) = V_{DD} - V_1(cos(\omega t) - \beta sin(\omega t) + \frac{\beta}{2} sin(2\omega t)) \tag{2.14}$$

As is shown in [4, 29], the second harmonic current, $I_2$ has a relationship with fundamental current $I_1$ and conduction angle $\alpha$

$$I_2 = \frac{4}{3} \frac{sin^3(\frac{\alpha}{2})}{(\alpha - sin(\alpha))} I_1 \tag{2.15}$$

When the transistor is biased in Class B, the conduction angle equals $\pi$ and the second harmonic current component has the value of $I_2 = \frac{4}{3\pi} I_1$. The impedance profile of the transistor follows the following relationship.

$$Z_n = \frac{V_n}{I_n}, \quad n = 1, 2, 3.... \tag{2.16}$$

Combining Equation 2.13, 2.14, the fundamental impedance ($Z_1$) and the second harmonic impedance ($Z_2$) can be described as the following equations

$$Z_1 = R_{opt} \cdot (1 + j\beta) \qquad (-1 \leq \beta \leq 1) \tag{2.17}$$

$$Z_2 = -j\frac{3\pi}{8} R_{opt} \cdot \beta \qquad (-1 \leq \beta \leq 1) \tag{2.18}$$

$Z_1$ and $Z_2$ are the optimum impedances at the fundamental and second harmonic frequency, respectively. The higher order harmonics are short circuited. As shown here, $\beta = 0$ corresponds to Class B operation mode; in range $0 < \beta \leq 1$, it represents a Class J* mode; in the range of $-1 \leq \beta \leq 0$, it is called Class J mode. Figure 2.5 shows the normalized optimum impedances with different $\beta$ values. The third and higher order harmonics are shorted. The Class J and J* mode has a symmitrical design space.

Figure 2.6 shows the current and voltage waveforms at the intrinsic drain reference plane in the Class J*, J and Class B mode. The peak drain voltage of the Class J*/J is almost 1.5 times higher than Class B mode due the existence of imaginary part in the fundamental impedance. They all share the same drain current since they are biased at the same $V_{gs}$. Comparing with the Class B mode, by adding the second harmonic impedance $Z_2$, an imaginary part is allowed to appear in the fundamental impedance. This is beneficial to wideband design where it is not feasible to keep a constant real impedance and zero second harmonic impedance in a wideband frequency range practically. Taking advantage of this concept, there will be multiple impedance profiles (different $\beta$ values) that correspond to the same output power, efficiency and linearity. This continuous design space adds more design freedom of class B mode and makes Class B/J mode a good candidate for broadband amplifer design.

In the real life, the design space of continuous Class B/J mode will be shifted due to the inherent drain to source capacitance $C_{ds}$ and package effect from the transistor. Research on the design space and the sensitivity of harmonic mismatch in Class B/J mode has been explored in [32]. According to [32], due to the output parasitics from the transistor, the design space of Class J and J* is asymmetrical and the design space of Class J* is much larger than Class J. As a verification, Figure 2.7 shows an example of the design space at

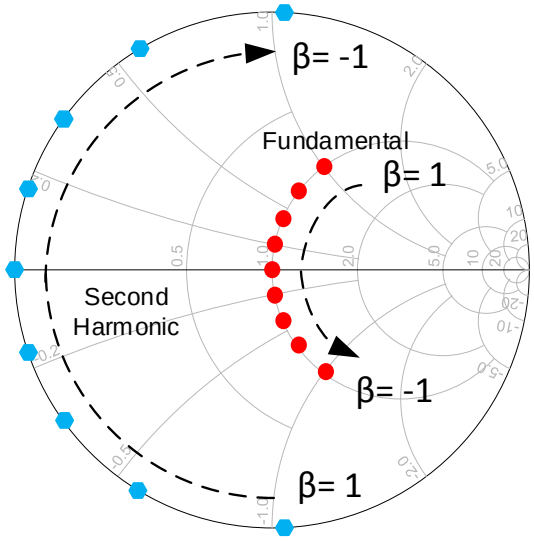



Figure 2.5: Design space of fundamental and second harmonic impedance of Class B/J mode

second harmonic for Class J and J*. It presents the simulation results of drain efficiency versus the impedance termination at second harmonic frequency at the load side with the 25 Watts gallium nitride (GaN) high-electron-mobility transistor (HEMT) from Wolfspeed. As shown in the figure, in Class J* mode ($\beta$=1), the drain efficiency remains higher than 66% when the $2^{nd}$ harmonic impedances at the package reference plane are locating within the blue-shaded range of the smith chart. However, in Class J mode ($\beta$=-1), the efficiency can only maintain at certain level within a specific narrow phase range in the smith chart and any harmonic impedance out of that region will cause a significant efficiency drop. In this sense, the Class J* has more flexibility on second harmonic termination over class Class J. The feature of the relaxed design space in Class J* mode for the packaged transistor makes it a promising candidate for broadband and multi-band PA design.

## 2.3 Doherty Power Amplifier Techniques

For the efficiency enhancement techniques mentioned in the previous section, such as the reduced conduction angle operation modes in Class AB/B/J/C and waveform engineering

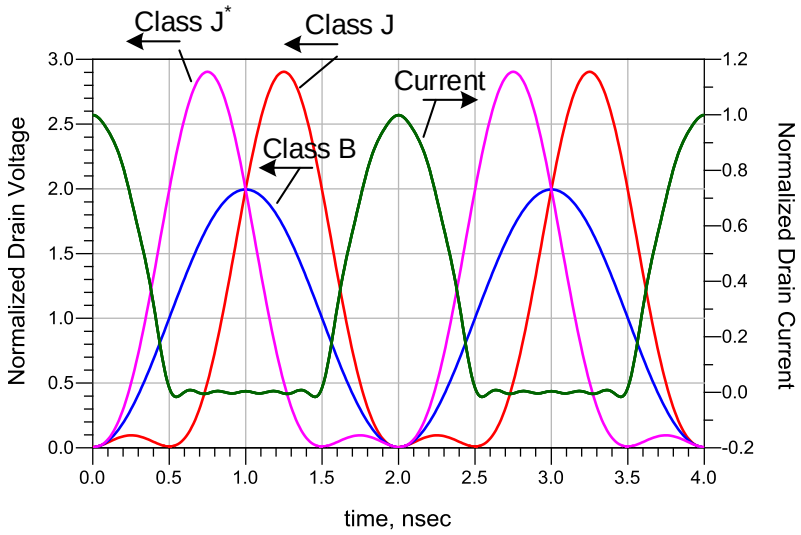



Figure 2.6: Drain Current and Voltage waveforms in Class J*,J and B mode

techniques in Class F/F$^{-1}$, the efficiency is only improved significantly at peak power level. However, the PA will still suffer from low efficiency when it is excited by modern modulated signals with high PAPR [2],[8]. Since on average the PA is operated at the back-off power levels where the efficiency of PA is still low. Studies on trying to solve the low back-off efficiency of the power amplifier has been made over the years [1],[22],[28]. The most popular approaches include envelop tracking (ET), Outphasing, and the load modulation technique also called the Doherty PA. Among these three techniques, the Doherty PA has drawn the most attention for its simple implementation and the great efficacy in efficiency improvements at back-off power levels.

### 2.3.1 The Theory of Doherty Power Amplifier

The Doherty power amplifier is proposed by W.H. Doherty to improve the efficiency of the transistor when driven by the modulated waves [5]. It successfully maintains its peak efficiency at 6-dB power back off. It contains two transistors, the main (carrier) transistor and the auxiliary (peaking) transistor, and a load modulation network (impedance inverter). Two types of Doherty topologies are developed based on the way that the load is connected with the network. Figure 2.8 shows the two topologies. In 2.8a, the load impedance, which is $R_{opt}/2$, is in shunt connection with the circuit whereas in 2.8b, the

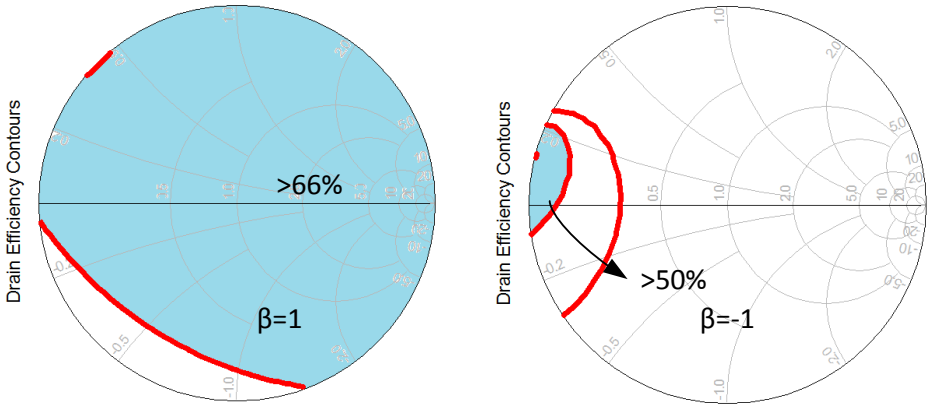
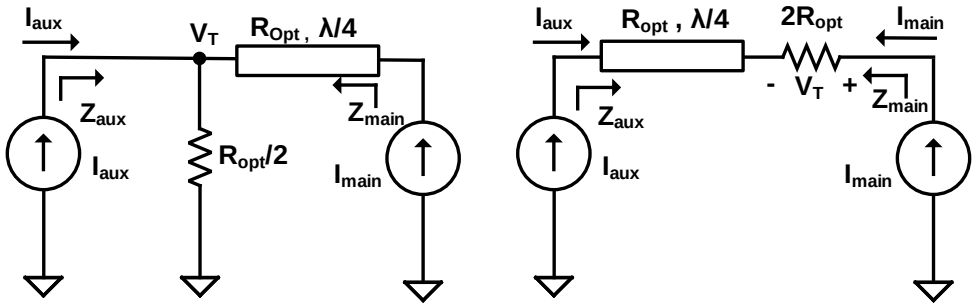



Figure 2.7: Design space of second harmonic impedance of Class J* and J mode at the package plane

load impedance, which is $2R_{opt}$, is series connected. Here, $R_{opt}$ is the optimum impedance of the main transistor and the transistors are taken as an ideal voltage controlled current source. Though in different topologies, both of the Doherty circuits share the same voltage and current profile at the centre frequency. Since in most of the applications, the load is single-end, the research on shunt-connection type Doherty PA has been well explored over the years.

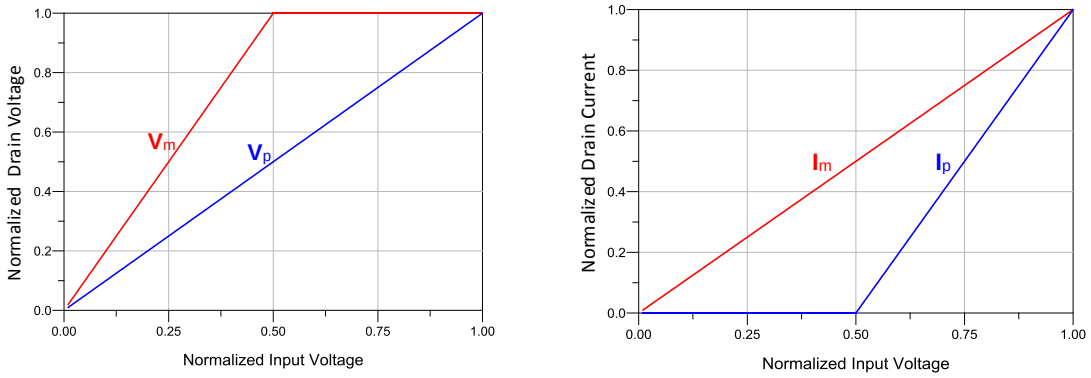
In both topologies, the main transistors are biased in Class B/AB mode and the auxiliary transistors are biased in deep Class C mode. When the input signal is still low, the auxiliary transistor is off. The peaking transistor presents a infinite impedance to the circuit. The load seen by the main transistor, $Z_m$, remains at a constant value of $2R_{opt}$ until the input power level reaches -6dB peak power level. Since the input impedance seen by the drain of main transistor is two times bigger than the normal cases, the main transistor reaches the saturation point at -6dB back off. In high power regime, the peaking transistor starts to inject current into the load. Through the impedance inverter, $Z_m$ starts to decrease until both of the transistors come to the saturation point with a load impedance of $R_{opt}$. The voltage and current profile of the Doherty is shown in Figure 2.9. The efficiency of the overall circuit is shown in Figure 2.10.The impedances seen by both of the main and auxiliary transistor are shown in Figure 2.11.

It is noticeable that the voltage profile for the main transistor and the current profile for the auxiliary transistor are non-linear. However, the output load resistance in both




(a) shunt-connection (b) series-connection

Figure 2.8: Doherty topologies in[5]




(a) Voltage Profile (b) Current Profile

Figure 2.9: Voltage and current profile in Doherty power amplifier[5]

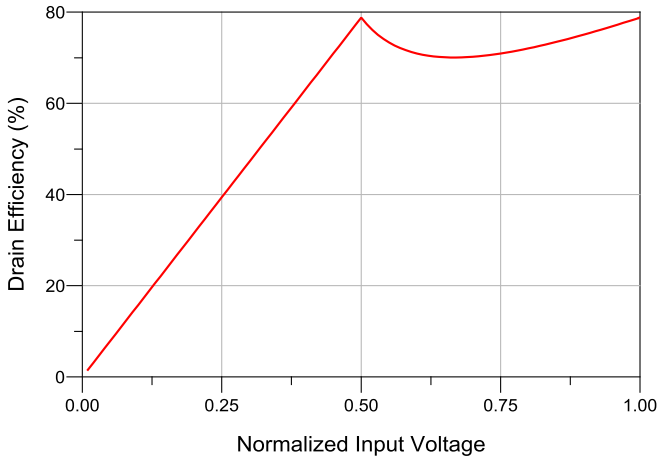



Figure 2.10: Overall drain efficiency of the Doherty ampliifer

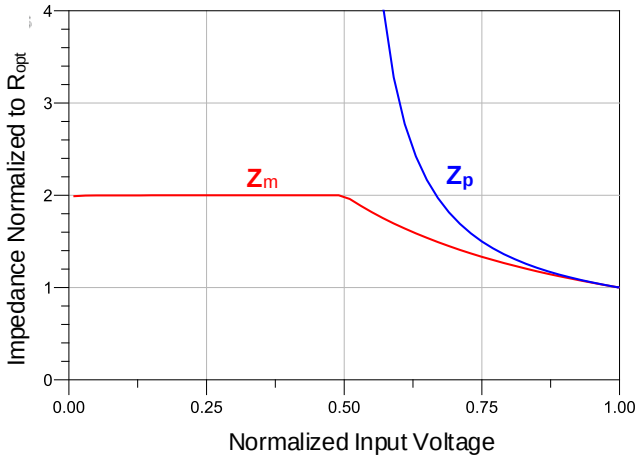



Figure 2.11: Impedance profile of the Doherty power amplifier

topologies, experiences linear transfer characteristics during the entire Doherty operation. For example in the shunt shunt-connection type, the output voltage at the load $V_T$ is linear versus input voltage since this voltage is imposed by the drain current of the main transistor through the impedance inverter as shown in Figure 2.9b. For the series-connection type, the current flowing through the load impedance, $2R_{opt}$, is always equal to the current from the main transistor due to the series connection. Hence, the voltage generating at the load is linear as well.

Therefore, it is significant to know: The Doherty power amplifier is an linear efficiency enhancement technique that improves the back-off efficiency without undermining the linearity of the circuit. This is crucial because any efficiency enhancement on the cost of sacrificing the linearity will require a more complex DPD model which will eventually lead to an increased power consumption in the system and decrease the overall efficiency. In the worst case scenario, it may cause the PA to become non-linearizable by feasible DPD models to correct due to the strong non-linearities.

## 2.4 Practical Issues of Power Amplifier Design

All of the theoretical analysis so far about the power amplifier are based on the assumption that the transistor has a zero knee voltage and can be modelled as a linear voltage controlled current source. In the practical case, the transistor will have a non-negligible knee voltage that degrades the performance of the circuit including the efficiency and linearity. Furthermore, the transistor has non-linear parasitics which are bias dependent and as a result, the non-linear parasitics are a source of some of the harmonic distortions. All of these are the major sources of non-linearities in the power amplifier circuits.

### 2.4.1 Internal Capacitor and Package effect of the Device

Due to the physical structure of the transistor, parasitic intrinsic capacitors affect the transistors performances such as the gain, transition frequency etc. For the field effect transistors, the three most important capacitors are $C_{gs}$, $C_{gd}$, $C_{ds}$, also referred to internal parameters. In addition to these intrinsic capacitors, the transistor packages such as the inner bond wires and leads also introduces parasitics, called external parameters. Package effect parasitics can be extracted by Cold-FET methods. Figure 2.12 shows the simplified small signal model of a packaged transistor with both internal and external parameters. The internal parameters are outlined in the red dash box. Normally the internal parameters

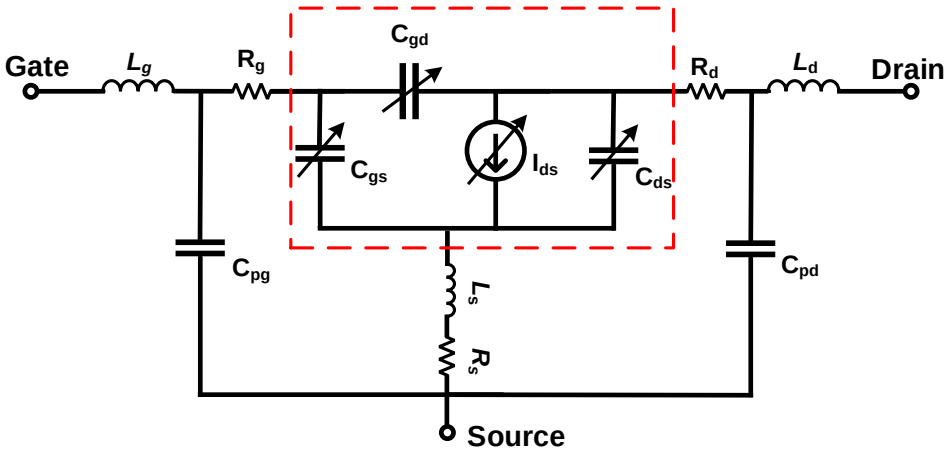



Figure 2.12: Simplified small signal model of a packaged transistor

are non-linear and affect the circuit performance more. Therefore the internal parasitic capacitors are discussed in detail here.

For GaN devices, the $C_{gs}$ at the gate side are strongly non-linear. Figure 2.13 presents the value of $C_{gs}$ versus gate voltage with the 25W die transistor. The threshold voltage of the transistor is around -2.8V. As seen, the capacitance almost doubles its value after the transistor turns on. This non-linear capacitor will generate second and higher order harmonic components that distort the signal voltage at the gate. Due to this non-linear capacitance, the second harmonic impedance termination is very critical to achieve certain efficiency and linearity in circuit. Any improper $2^{nd}$ harmonic terminations will result in a severe signal distortion and efficiency degradation as reported in [23]. The simplest solution to avoid this effects is to put second harmonic short terminations to filter out the harmonics voltages. While, this is quite challenging for wideband design. For harmonic orders higher than two, the circuit performance is normally not as sensitive. The efficiency will only differ by less than 3% for all load impedances within the Smith chart.

At drain side, the $C_{ds}$ is relatively constant as seen in Figure 2.14. This output capacitance will affect the optimal impedance matching, bandwidth, harmonic terminations, etc. For example in Doherty power amplifier design, this capacitance shifts the real optimum impedance to a complex number, hence parasitic absorption structure has to be facilitated to maintain the proper load modulation behaviour.

The bridging capacitance $C_{gd}$ provides a feedback path from the output side to the

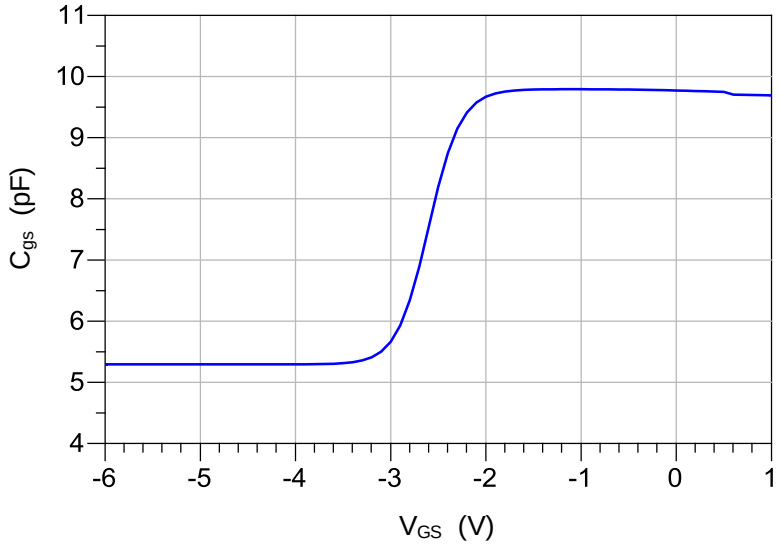



Figure 2.13: $C_{gs}$ of the 25W die transistor from Wolfspeed

input. Normally $C_{gd}$ is much smaller comparing to $C_{gs}$ and $C_{ds}$ as seen in Figure 2.15. At low frequencies, the admittance of the $C_{gd}$ is negligible and the transistor can be treated as unilateral approximately. While at high RF frequencies, the effect of this feedback path starts to become more significant and the transistor is not unilateral any more. This is also called the Miller effect. As a consequence, the optimum impedances at the fundamental and harmonic frequency range at the output are dependent on the input impedance terminations at the gate and the vice versa. As such, in the practical design, the input and output matching network designs have to be performed iteratively to obtain the desired performance.

### 2.4.2 Knee Region Interaction

The DC-IV curves shown in Figure 2.1, 2.3 in the previous section are assuming the knee voltage of the transistor is zero. In the real life, the knee voltage takes a significant portion of the drain supply. This is one of the main reasons that the efficiency of Class B amplifier cannot reach the theoretical 78.5% without over driving the transistor. Figure 2.16 shows the actual DC-IV curves of the 25W GaN HEMT transistor from Wolfspeed. As shown in Figure 2.16, the knee voltage is approximately 10V and the drain supply is 40 V. To

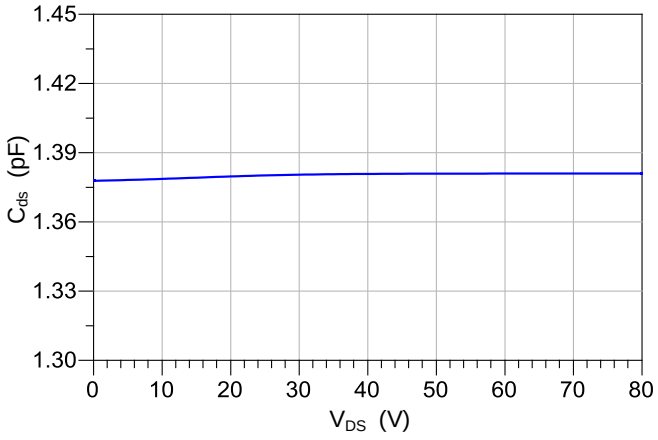



Figure 2.14: $C_{ds}$ of the 25W GaN HEMT transistor

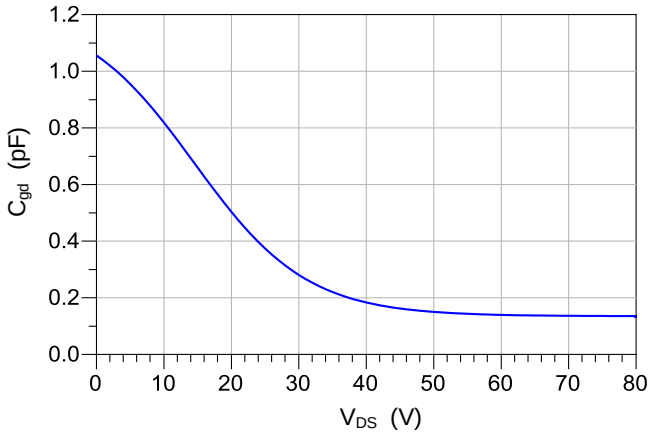



Figure 2.15: Bridging $C_{gd}$ of the 25W GaN HEMT transistor

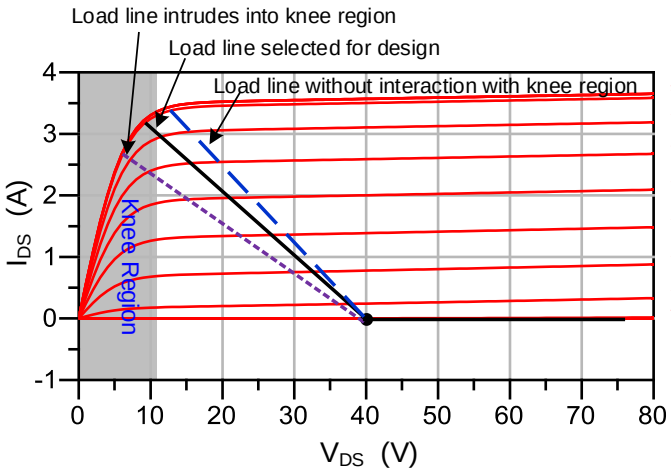



Figure 2.16: DC-IV sweep for 25W GaN HEMT transistor from Wolfspeed

completely avoid the knee region, the load line can be selected as blue-dashed line. The voltage swing will be kept above the knee region and distortion is avoided. However, since the voltage swing is small, the RF power delivery will be reduced and eventually the efficiency will be sacrificed.

Load line selected as the purple-dash line will result in a larger voltage swing. Therefore, good efficiency can be expected. While due to the intrusion into the knee region of the voltage swing, the dip will show up in the current waveform as shown in Figure 2.17. Due to the distorted drain current, the linearity performance including AM-AM and AM-PM will be affected consequently.

In reality, a trade-off load line will be picked to make a suitable compromise between efficiency and linearity which is shown as the black solid line in Figure 2.16. This load line allows a slight intrusion into the knee region when operating at the high power regime and have some distortions, while maintaining the efficiency at a reasonable level.

### 2.4.3 Stability Issues of PA Design

An important requirement for a PA circuit is being stable. At the low frequency range, the gain of the transistor is high and the circuit easily oscillates with an improper impedance at the input or output. A stability circuit has to be inserted to avoid oscillation. The stability of the small signal amplifier circuit is analyzed in [24]. For PA design, where the

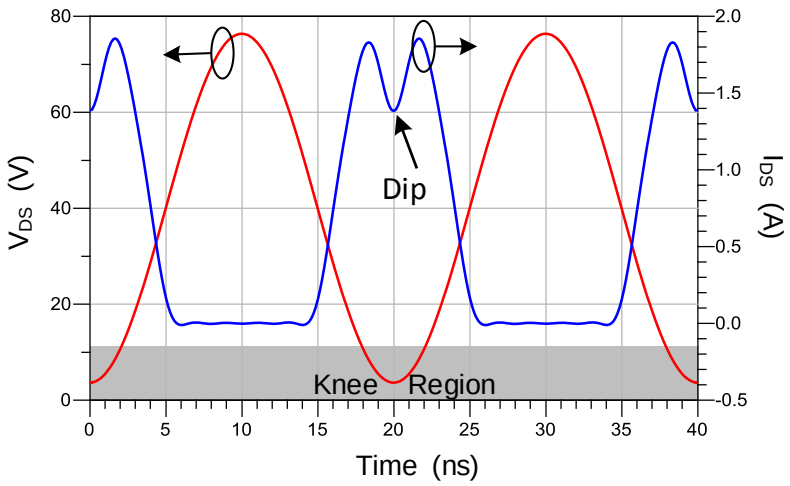



Figure 2.17: Voltage and current waveforms with knee voltage interaction with 25W GaN HEMT device

efficiency of the circuit is important, a resistor in parallel with a capacitor at the input side is normally adopted to stabilize the circuit without decreasing efficiency. At the low frequency range, the resistor is chosen to attenuate the signal and move the matching area out of the unstable region. The capacitor in parallel has to be properly selected to let the RF signal pass through at the interested frequency range so that the gain of the circuit will not sacrifice too much. By tuning the value of the capacitor, the achievable gain and the stability coefficient of the transistor can be manipulated. Normally at the low frequency range, the circuit is absolutely stable, while at the RF region the circuit is conditionally stable. Therefore, it is important to check the stable region both of the input and output at the desired RF frequency range after adding the R-C circuit, such that the targeted input and output impedances are away from the unstable region.

## 2.5 Multiband and Broadband Doherty Power Amplifier Literature Review

The evolution of wireless communication standards from GSM to third generation wideband CDMA to the fourth generation long-term evolution advanced calls for the radio

transmitters to be multi-band and multi-standard. In the mean time, these radios must efficiently amplify the signals with a high PAPR. Muti-band and broadband Doherty amplifier is an appealing solution to this trend. Traditionally, each Doherty is designed for each communication standard and the multiple Doherty PAs are implemented. Then switches array are used to accommodate the multi-standard concepts. However, this approach is very costly and more importantly it can not support the multi-standard applications concurrently.

Research has targeted the multi-band Doherty PAs since the year 2012 [3, 14, 16, 21, 26, 27]. Most of them were designed using a modular approach from the single band design concept, in which every module including the output matching network, impedance inverter, offsets line, input matching network is replaced with its dual-band equivalent. It is worth mentioning that, the impedance matching network that needs to be constructed in the module target not only at multiple fundamental frequencies but also the corresponding harmonics (mainly second harmonic frequency). Along with the multi-band impedance inverters and phase-offset tuning lines, the multi-frequency Doherty power amplifier is a very complicated task in this approach. More importantly, this high complexity leads to a high circuit sensitivity. The phase offset-lines are empirically tuned to meet the load modulation condition at the centre frequencies. When the frequency deviates from the centre, the load modulation condition quickly collapses. Hence the Doherty behaviour can not be maintained and the bandwidth is significantly degraded.

For instance, Saad et al proposed a Dual-Band Doherty in [27]. Figure 2.18 shows the proposed circuit diagram. It contains all of the dual-band building blocks mentioned above. The dual-band inverting networks, as shown in Figure 2.19, are analyzed and implemented. The circuit is capable of working at 1.8 GHz and 2.4 GHz concurrently. However, due to the complicated circuit topology and high circuit sensitivity, the bandwidth reported in each band is narrow and there is performance degradation at the second band as reported.

Similarly, Rawat et al. in [26] introduced the new dual-band offset lines which is shown in Figure 2.20 to compensate the limited output impedance of the off-state auxiliary amplifier at two arbitrary frequencies, such that load modulation condition can be further improved. This phase offset has been applied to design a concurrent dual-band Doherty PA. However, due to the limitation of the circuit structure, this technique has the major drawback of narrow bandwidth and performances degradation which is similar to that reported in paper [27].

Based on the methodology mentioned in [27], an attempt was also tried at the input side to improve the back-off efficiency of dual-band Doherty PA. Chen et al. in [3] proposed an adaptive power division at two arbitrary frequencies to minimize the early soft turn-on

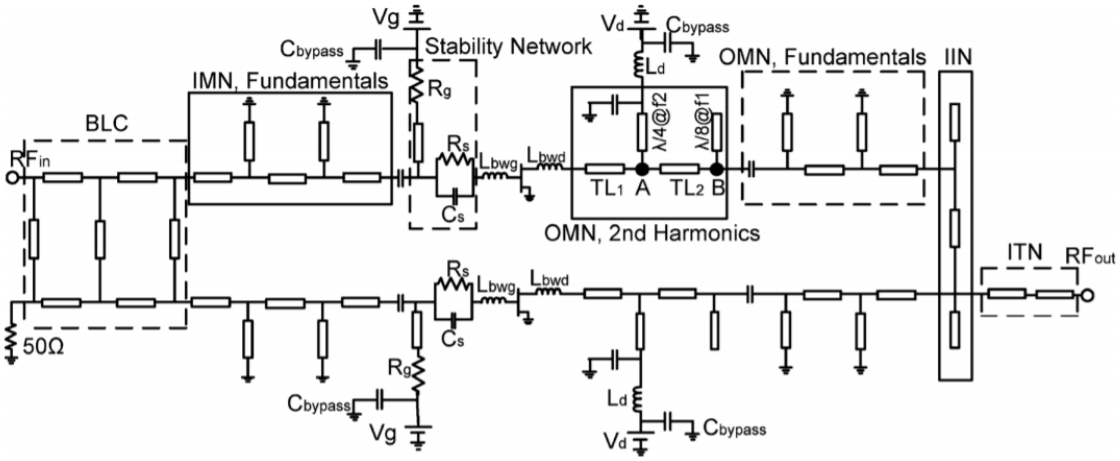
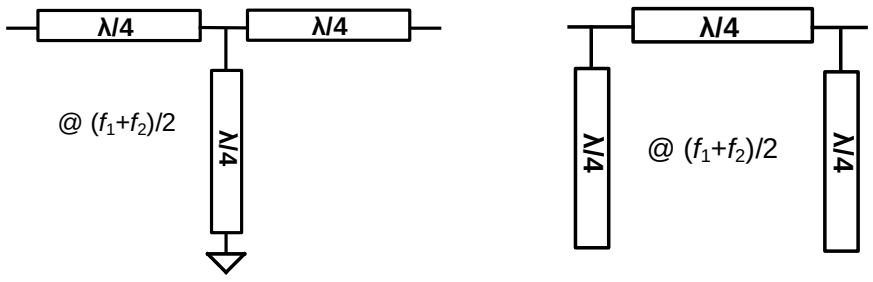



Figure 2.18: Dual-band Circuit Diagram [27]




(a) T-shape with short ended stub (b) Pi-shape with open stub

Figure 2.19: Conventional dual-band quarter-wave transformers in [27][3]

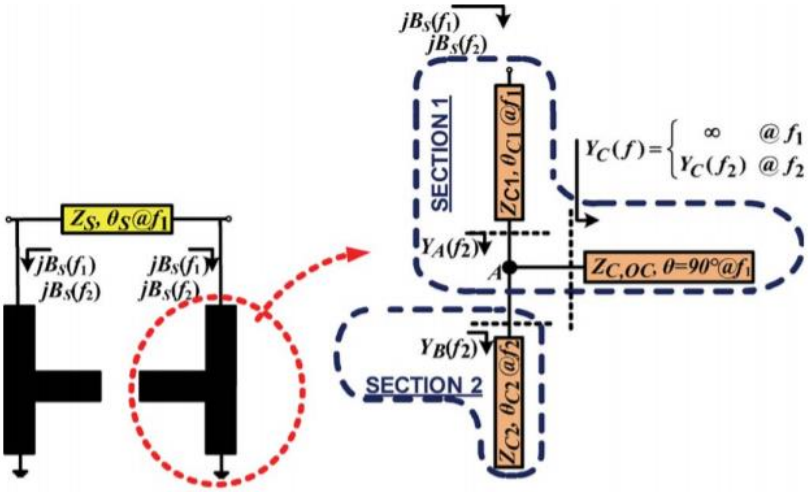



Figure 2.20: Dual-band phase offset lines [26]

effect of the peaking PA. The premise of this approach is that the designed auxiliary PA has different breaking points at the two frequencies of interest. By designing the proper power splitting ratio at the different frequencies correspondingly, the efficiency drop caused by the early turn on effect of the peaking device can be minimized. This technique provides 3%-5% improvements in simulation. Unfortunately, non-satisfactory Doherty baviour was observed in the measurement results due to the same drawback caused by the circuit structure described in [26][27].

Three and more operating bands are also reported in the literature [17], [21], [14]. Their methodologies are derived from the dual-band structure that were discussed at the beginning of the section and their efforts are mainly focusing on the realization of the multiband impedance inverters or phase offset lines. Nghiem et al. in [21] first proposed the tri-band impedance inverters as shown in Figure 2.21. The transformer is successfully applied to a tri-band Doherty design. However, the three frequencies are interrelated and cannot be arbitrarily selected. A more complex structure is explored to realize the tri-band impedance inverting networks at arbitrary frequencies as shown in Figure 2.22a. Recently Li et al. [17] presented a quad-band Doherty by implementing a quad-band transformer as shown in Figure 2.22b. But again due to their high circuit complexity and sensitivities, the bandwidth of the Doherty PA is limited. According to their modulated signal measurements, they can hardly support the wideband modulated signals under carrier aggregation

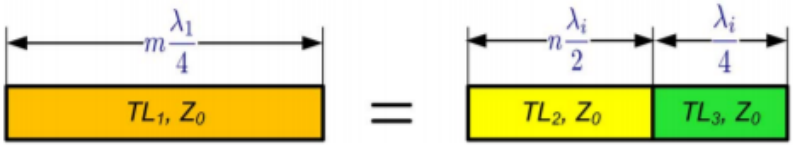
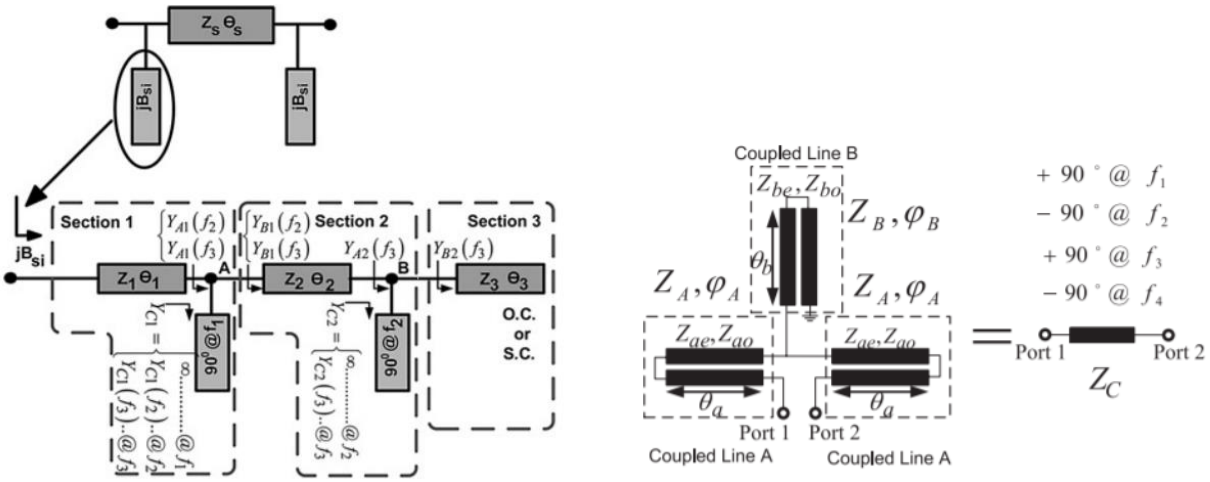



Figure 2.21: Tri-band transformer [17]




(a) Triband inverter [14]

(b) Quad band inverter [17]

Figure 2.22: Proposed Tri/Quad-band transformers

concept.

Alternatively, researchers have explored the applications of electrically tunable devices, like the RF MEMS switches and p-i-n diodes to realize a reconfigurable input/output matching circuits. Mohamed et al. in [20] proposed reconfigurable matching networks using MEMS switches and developed a frequency agile Doherty power amplifier. Figure 2.23 gives one of the design examples in the paper. Yet, this approach suffers from a significant drawback that it does not allow concurrent working at multi-frequencies. Moreover, the slow switching speed and limited power handling capabilities of the MEMS devices may cause another issue for the circuit. Kalyan et al. [13] proposed an interesting approach to design of a Doherty PA which can be reconfigured to two different pairs of concurrent

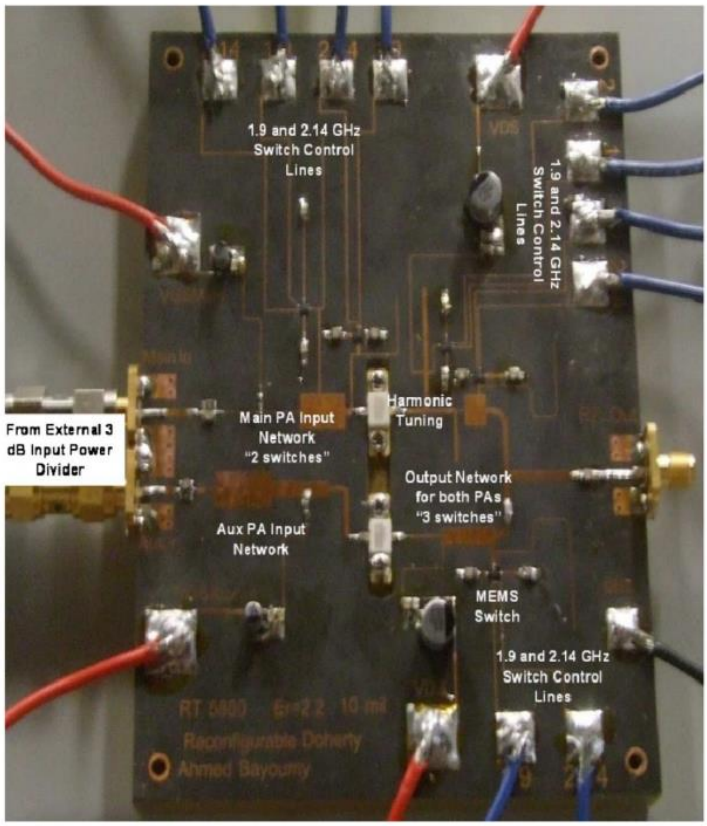



Figure 2.23: Reconfigurable Doherty amplifier prototype [20]

dual bands using p-i-n diodes. In each state, the PA is designed to work at two arbitrary frequencies simultaneously. In spite of possessing the appealing functions, the PA is only validated under the continuous wave (CW) measurement and the modulated signal tests are not provided.

Another approach to realize the multi-band multi-standard Doherty PA is to envisage a broadband DPA to cover the entire frequency range of interest to meet the application requirements of modern transmitters. However, the fractional bandwidth of such DPAs is limited to 30-50% according to most publications [31, 6, 25]. For instance, in [31], an asymmetrical biasing configuration was proposed to extend the impedance bandwidth at back off power level. By modifying the voltage and current profiles, a constant back-off impedance was obtained regardless of the frequency, theoretically. This work showed

good performance, achieving a bandwidth of 35%. However, the main disadvantage of this approach is that the peaking transistor has to be biased much higher (twice as much) than the main PA, which requires a much higher breakdown voltage for the peaking transistor. This may decrease the reliability of the device. To solve this issue, Fang et al. in [6] added a auxiliary transformer at the peaking path to transform the impedance of $4R_{opt}$ at the combining node to $R_{opt}$ at the drain side. Hence the drain biasing of the peaking transistor can be lowered. This work obtained 40% bandwidth with a reduced drain supply for the peaking. In recent work, a modified output combiner was proposed in [25] where the $\lambda/2$ transformer was implemented between the peaking transistor and combining node to extend the back-off impedance bandwidth. The half-wavelength transformer compensated the impedance variation at back-off power level and achieved 52% bandwidth performance from 470MHz to 803MHz with a peak power delivery of 700 Watts. However, these broadband DPAs are still not wide enough to cover the multi-band amplification scenarios especially when the two band are widely spaced. Moreover, their overall RF performances are usually sacrificed to obtain the continuous bandwidth compared to their narrow band or multi-band counterparts.

Furthermore, the carrier aggregation concept in LTE-A causes the PAPR value of the signals between 8-10dB. The efficiency of the traditional two-way DPA collapses when dealing with such signals with a high PAPR. To deal with this problem, three-way Doherty power amplifier was proposed in the literature where two efficiency peaks occur in the back-off power levels. In [10], an interesting analysis was conducted with the modified output combiner. As shown in the paper, by carefully selecting the optimum load impedance at the combining node, the bandwidth of the three-way DPA can be optimized. The work shows good results and achieves 35% operational bandwidth from 0.7 GHz to 1.0 GHz with a back-off efficiency over 49% at 9.0 dB back off. However, to the author's best knowledge, there is still no published dual-band three-way DPA capable of handling the multi/dual-band carrier aggregated signals. A summary of works on multi-band and broadband DPA is listed in Table 2.2.

Table 2.2: Literature review on dual/multi-band and broadband DPAs

| Ref. | Approach | Frequency (GHz) | $P_{out}$ (dBm) | $\eta_{-6dB}$ (%) | Year |
|---|---|---|---|---|---|
| [27] | Modular | 1.8/2.4 | 43/43 | 60/44 | 2012 |
| [3] | Dependent splitter ratio | 0.85/2.33 | 44/42.5 | 45/41 | 2014 |
| [26] | Phase offset lines | 1.96/3.5 | 41.6/42.3 | 44/32 | 2012 |
| [17] | $T-$shape inverter | 0.73/1.65/ 2.67/3.57 | 42.5 | 44.6-58.9 | 2016 |
| [21] | Tri-band inverter | 1.5/2.14/2.65 | 45.2/43/41.5 | 60/45/35 | 2013 |
| [14] | Multi-band inverter | 1.6/1.9/2.2 | 43.5/43.8/42.4 | 46/40/42 | 2015 |
| [13] | Reconfigurable (p-i-n diode) | 1.5/2.4 or 1.85/2.35 | 42-43 | 52/56 ($\eta_{-6dB}$) 43/48 ($\eta_{-9dB}$) | 2017 |
| [20] | Reconfigurable | 1.9/2.14/2.6 | 40-41 | 60 | 2013 |
| [31] | Asymmetrical biasing | 0.7-1.0 | 49.9 | 67 | 2012 |
| [6] | Bandpass transformer | 1.6-2.3 | 43 | 55-63 | 2015 |
| [10] | Modified combiner | 0.7-1.0 | 44 | 42-61 ($\eta_{-6dB}$) 49-64 ($\eta_{-9dB}$) | 2013 |

# Chapter 3

# Dual-band Two-way Doherty Power Amplifier Design and Results

In this chapter, a systematic methodology on the design of dual-band output and input matching network is proposed and applied for a bandwidth extended dual-band Doherty power amplifier. The proposed output network reduces the design complexity of the traditional dual-band Doherty PA and extends the achievable operational bandwidth in each band with exploiting the continuous design space of the Class B/J. Afterwards, a back-off gain contour technique for input matching of the main amplifier is introduced to smooth the overall gain variation during the entire Doherty operation. Finally the proposed method was applied to the design of a concurrent dual-band Doherty PA. Simulation and measurement results are provided.

The work in this chapter was previously presented in [18].

## 3.1 The Output Power Combining Networks of Dual-band DPA Design

### 3.1.1 The Dual-band Impedance Inverters

To avoid implementing the cumbersome structure and bandwidth limited phase offset lines as discussed in the literature, a modified dual-band impedance inverter is proposed as shown in Figure 3.1. This inverter is derived equivalently from the conventional $T$-shape

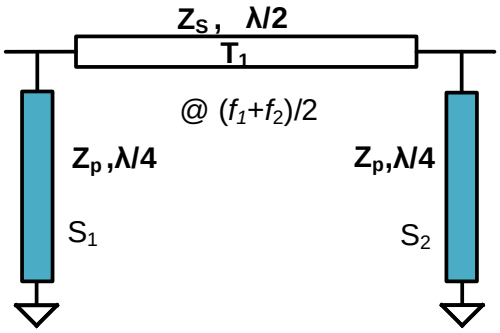



Figure 3.1: Proposed dual-band impedance inverter

transformer (see Figure 2.19a) by splitting the centre short-end resonator to both ends. The equations to calculate the characteristic of the stubs are given by

$$Z_S = \frac{Z_T}{sin(\pi \times \frac{2f_1}{f_1+f_2})} \tag{3.1}$$

$$Z_P = -\frac{Z_S tan(\pi \times \frac{2f_1}{f_1+f_2})}{tan(\pi \times \frac{f_1}{f_1+f_2})} \tag{3.2}$$

where $Z_T$ is the characteristic impedance of the original impedance inverter, $f_1$ and $f_2$ are the centre frequency of the two targeted bands. Note the proposed inverter is different from the $\Pi$ networks commonly used (see Figure 2.19b) , since the shunt stubs $S_1, S_2$ are $90^o$ short-circuited and the line in the middle $T_1$ has an electrical length of $180^o$ at $f_0 = (f_1+f_2)/2$ instead of the 90 of the conventional $\Pi$-inverter. This transformer is equivalent to the conventional $T$-inverter electrically, the phase shift of the proposed inverter is $-90^o/90^o$ at $f_1$ and $f_2$, same as the $T$-shape inverter.

The proposed $\Pi$ network has several advantages: the output capacitance of the main and the peaking transistors can be absorbed into the short-ended shunt stubs ($S_1$ and $S_2$) as shown in Figure 3.2. Second, the short circuited stubs can be served as biasing feed which provides a small low frequency impedance and helps to minimize the memory effect and improves the linearity of the circuit. This will be further discussed in the later section.

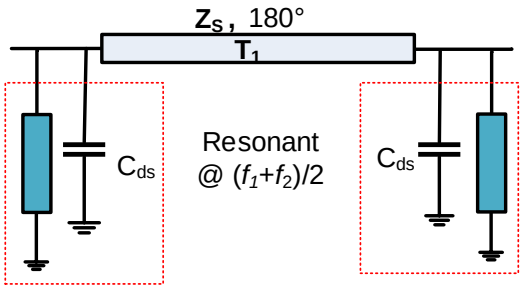



Figure 3.2: Proposed dual-band impedance inverter after parasitic absorption

### 3.1.2 Dual-band Output Combiner for Packaged Devices

The proposed output power combiner is composed of three networks, designated by the red boxes in Figure 3.3. Network I is the proposed dual-band Π-inverter and will absorb the parasitic of the transistor into itself. The same topology is used in network II, which, together with a conventional Π network, forms a $180^o/0^o$ transformer at the two bands, required by the wideband DPA theory [25]. The input impedance, looking into the load direction at the combining node, is $R_{opt}/2$. Network III is a two-section dual-band impedance transformer [27], converting the impedance from 50Ω to the $R_{opt}/2$. When the peaking transistor is off, Networks I transforms the input impedance $R_{opt}/2$ at the combining node to $2R_{opt}$ at the current source plane, which will saturate the main transistor at 6dB power back-off. The $180^o/0^o$ transformer at the peaking path will compensate the back-off impedance variation seen by the main over an certain bandwidth.

It is worth mentioning that absorbing the transistor's output parasitics into the output combiner allows the designer to take advantage of the exploded transistor model provided by the foundry and gain access to the current source plane. This eliminates the need for phase-offset lines commonly used in narrow-band DPA implementations [26], which are major sources of bandwidth limitation and circuit sensitivity.

### 3.1.3 Low-frequency Impedance

The low-frequency impedance is the major source of drain modulation which lies in the even-order non-linearities of the transistor. To explain the importance of the low-frequency impedance and the mechanism of the caused drain modulation, consider the PA is driven

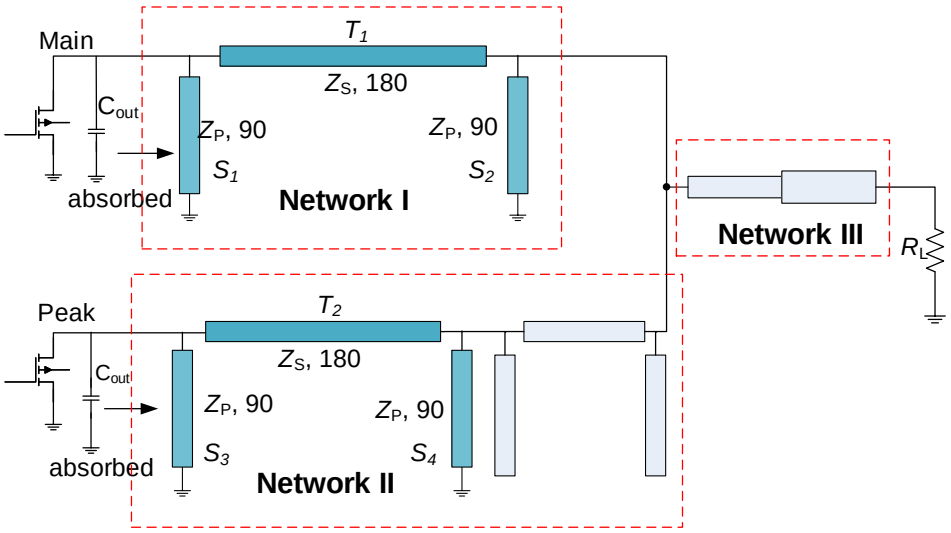



Figure 3.3: Schematic of proposed output combiner network

by a two-tone signals at $f_1$ and $f_2$. Due to the inherent non-linearities of the transistor, multiple distortion current products will be generated. Among them, the second order inter-modulation is critical since it is usually low frequency less than 100MHz (depends on the $f_2$-$f_1$). This current component at the drain times the low-frequency impedance resulting in a low frequency drain voltage which dynamically modulates the DC supply of the transistor. This undesired voltage variation at the drain will push the RF swing into knee region and cause the dynamic gain compression as shown in Figure 3.4, which is also analyzed as drain induced memory effect.

The bandwidth of the low-frequency impedance determines the bandwidth of the modulated stimuli since any signal components beyond this bandwidth will experience drain induced memory effects. For dual-band power amplifier design, the low-frequency impedance bandwidth has to be wide enough to cover the range of all the possible $f_2$-$f_1$. For concurrent amplification case, $f_2$-$f_1$ can be as wide as gigahertz.

In this design, the short circuited stubs in the output combiner are re-utilized as DC biasing. Unlike the traditional high-Z quarter wave length biasing line which will cause huge resonance with DC decouple capacitors in the low frequency region, it provides a small low-frequency impedance for both of the main and peaking transistor across a wide frequency range. As seen in Figure 3.5, the magnitude of low frequency impedance is below 20 $\Omega$ from a small frequency up to 1.6GHz, which helps minimize the drain modulation

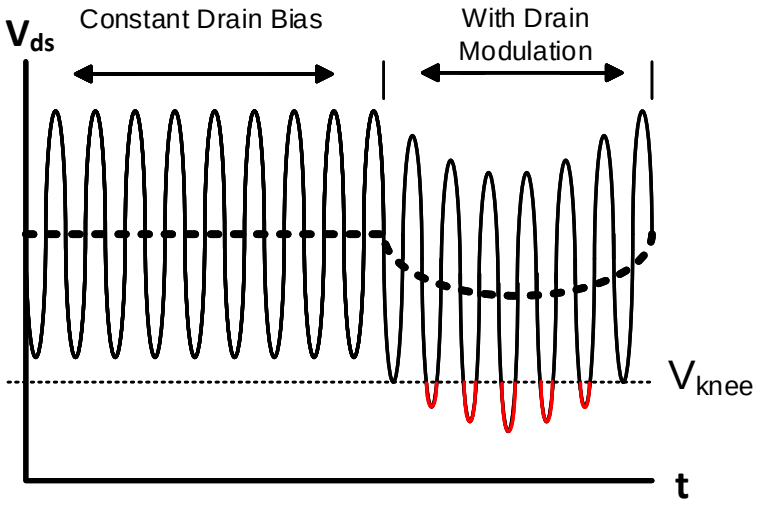



Figure 3.4: Voltage waveform with and without drain modulation

and eventually improves the linearizability of the PA under concurrent dual-band stimuli.

## 3.2 Dual-band Input Matching Network Design

The output power combining network in the section 3.1 provides the correct impedances for the main transistor at 6-dB back off and both of the transistors at saturation. To maintain the proper load modulation behaviour, the input matching network is also critical since it dictates not only the current profiles of both transistors but also the gain flatness of the PA during the entire Doherty operation.

### 3.2.1 Carrier Amplifier Design

The authors in [9] [23] proposed the current contour technique for the main transistor such that the transistor will inject the desired amount of current to the load modulation network at peak power level. This method guarantees the current profiles and power output at the saturation point. However, at the low power level, as the input admittance

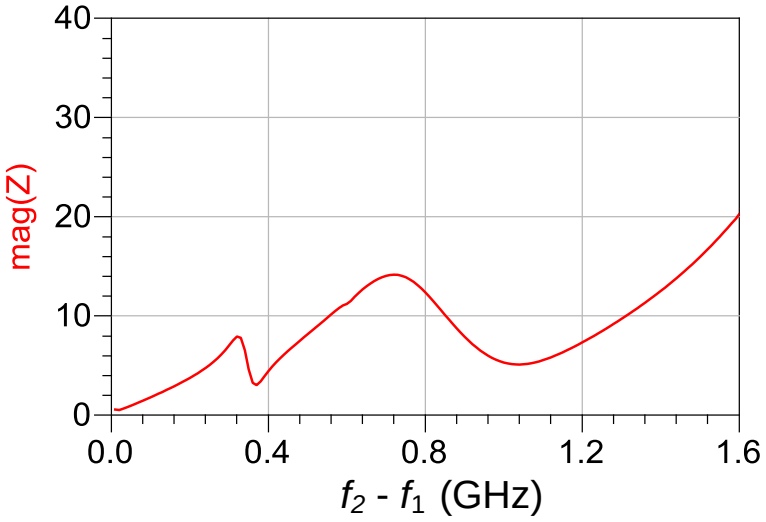



Figure 3.5: Low frequency impedance of the main transistor

of the transistor varies, this targeted impedance selected by the current contour can not guarantee the required gain to compensate the power loss at the power splitter. For ease of analysis, the equivalent circuit of the main PA can be simplified as the schematic shown in Figure 3.6. By applying the Mason's rule [19], the voltage transfer function from the $V_S$ to the load $V_L$ is given by equation below.

$$A_T = \frac{V_L}{V_S} = \frac{A_v}{1 + j\omega C_{gd} Z_s + j\omega C_{gs} Z_s - j\omega C_{gd} Z_s A_v} \tag{3.3}$$

$$C_{in} = C_{gs} + C_{gd}(1 - A_v) \tag{3.4}$$

where $A_v$ is the transfer function of the transistor from $V_g$ to $V_L$. Assume in the design frequency range, the feedback effect due to $C_{gd}$ is weak and the gain of the transistor is mainly contributed by the active current source. Hence,

$$A_v \approx -g_m R_L \tag{3.5}$$

Substituting Equation 3.4 and 3.5 into 3.3, one ends up with

$$A_T = \frac{-g_m R_L}{1 + j\omega Z_s C_{in}} \tag{3.6}$$

Interestingly, as seen in the equation, the total gain of the circuit relates to both the load impedance $R_L$ and the input capacitance $C_{in}$. As we know, the load resistance $R_L$

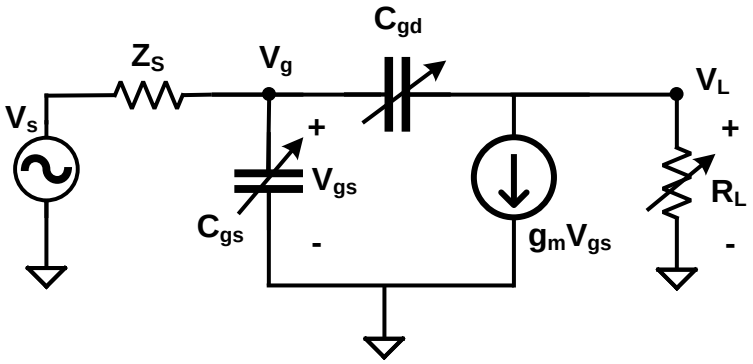



Figure 3.6: Equivalent circuit schematic of the main transistor

is modulated from $2R_{opt}$ to $R_{opt}$ from the low power region to peak power level. Hence, $A_v$ at low power region is twice as much as that at peak power approximately, given $g_m$ is constant. Recall $C_{gs}$ in Chapter 1 in Figure 2.13, the $C_{gs}$ increases versus input power. Due the change of $A_v$ in the load modulation, the miller capacitance varies during the process. Therefore, the value of $C_{in}$ varies from low power region to peak power and the gain increase at the low power region is not 3 dB as expected.

This effect can also be observed by the gain contour though fundamental impedance source pull simulations. Figure 3.7 shows the 10 and 13 dB gain circles at small signal level and peak power level, respectively, with 25W GaN HEMT device at 3.5GHz. As shown, the two circles does not overlap due to the varying $C_{in}$. The impedances that fall on the edge of 10-dB gain circle will cause an gain of lower than 13dB at the small signal region. While the impedances fall on the edge of 13-dB gain circle will lead to the designated power delivery and meet the gain requirement at low power region. Since at peak power level, the power delivery saturates. These source impedances locating inside the 10-dB gain circles will not cause a evident gain increase. Therefore, choose the impedances on the 13-dB gain circles will guarantee the required gain at the small signal regime and the designated power output at the peak power level.

To sum up, picking the fundamental sources impedance on the edge of gain circles at the backed off power level rather than at the peak power level will maintain a overall flat gain of the Doherty amplifier, thereby improving the linearity of the Doherty amplifier circuit. This technique provides the insight of choosing the fundamental impedances at the input. In terms of the second harmonic, a second harmonic source-pull has to be implemented beforehand, such that the second harmonic termination will not fall into the

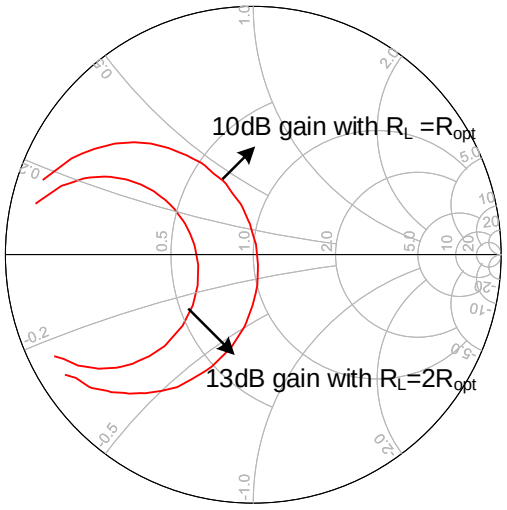
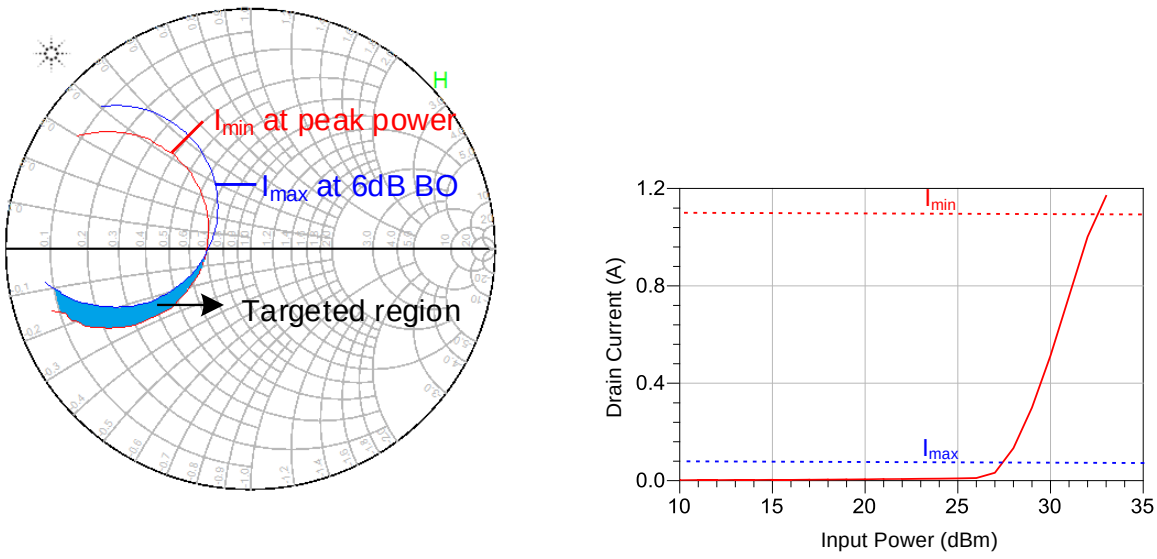



Figure 3.7: Gain circles contour with fundamental source pull simulation

sensitive region in the smith chart, where the power and efficiency will deteriorate.

### 3.2.2 Auxiliary Amplifier Design

The method of fundamental source impedance matching for the auxiliary amplifier is referred to the thesis in [23]. The current contour is plotted at the peak power level and 6dB-back off level respectively, as shown in Figure 3.8. Next an overlap region was selected, shown as the blue-shaded area in the smith chart. This overlap region sets the maximum turn-on current and minimum peak current, required by the Doherty as shown in 3.8b. Again after the fundamental impedance is selected, the second harmonic impedances will have to be taken good care of, such that the sensitive region is avoided in the smith chart.




(a) (b)

Figure 3.8: (a) Current contour at peak power level and 6dB back-off respectively (b) the corresponding current profile versus input drive

## 3.3 Dual-band Doherty Power Amplifier Design and Simulations

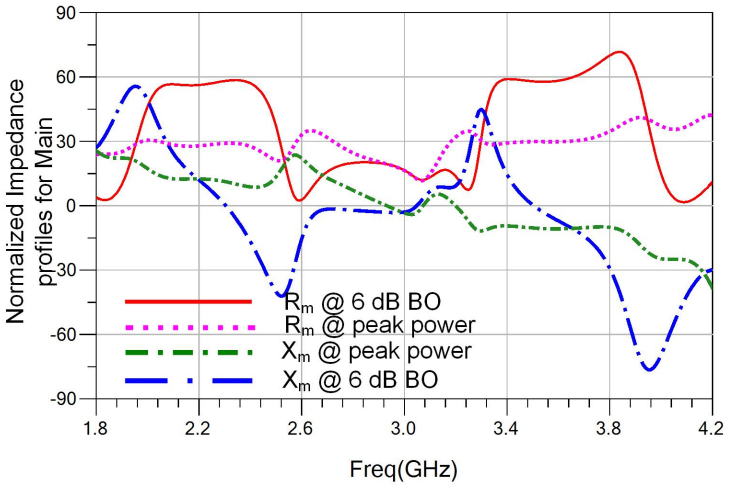
To validate the proposed dual-band design methodology, a 50-W dual-band Doherty power amplifier was designed using the commercialized 25W GaN HEMT transistors from Wolfspeed. The targeted design frequency bands were 2.0 - 2.4 GHz and 3.4 - 3.8 GHz. As noticed, the targeted design band has a fractional bandwidth of 18% and 11% respectively. This differs from the existing dual-band DPAs where only the two centre frequencies were claimed and reported. The details of designing the output combiner and input matching networks are provided in the following sections.

### 3.3.1 Output Combiner Network

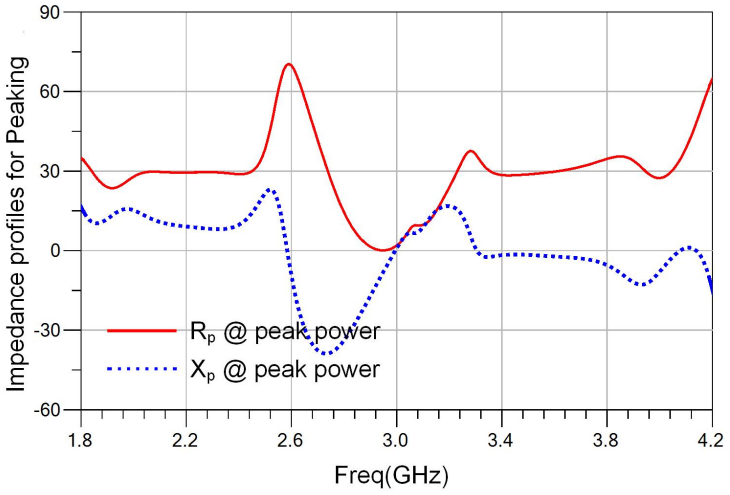
The OCN of the DPA was realized using transmission lines with the topology proposed in section 3.1. By performing the DC-IV sweep and loadpull simulations, the optimum output impedance $R_{opt}$ was found to be 30 Ω. Applying the Equation 3.2 and 3.2, the design parameters $Z_s$ and $Z_p$ of dual-band impedance inverter that has an equivalent characteristic impedance of 30 Ω are 43.6 Ω and 16.5 Ω. After implementing the calculated dual-band inverter in the output combiner in Figure 3.3, the impedance profile seen by the intrinsic drain of the main and auxiliary transistor was obtained after parasitic absorption. Figure 3.9 shows the impedance profile including both the real ($R_m$ and $R_p$) and imaginary part ($X_m$ and $X_p$) seen by the drain of main and peaking devices. As can been seen, the real impedance, $R_m$ and $R_p$, both at back-off power level and peak power, can be maintained within the design bandwidth at both bands. The continuous Class B/J design space was fully exploited here since both the imaginary part $X_m$ and $X_p$ are not zero over the two bands. The $X_m$ and $X_p$ at both bands were properly controlled such that the transistors were working in the Class B and J$^*$ mode where the second harmonic has a large freedom in the smith chart.

### 3.3.2 Input Matching Networks

The input matching networks for the main and peaking transistor were implemented using the methodology discussed in the section 3.2. The input matching for peaking transistor was designed first, since the gain of the peaking transistor is normally limited by the deep biased Class C mode. After the achievable gain of the peaking is confirmed, the desired




(a)




(b)

Figure 3.9: Impedance Profiles seen by the intrinsic drain of the transistors (a) main transistor (b) peaking transistor

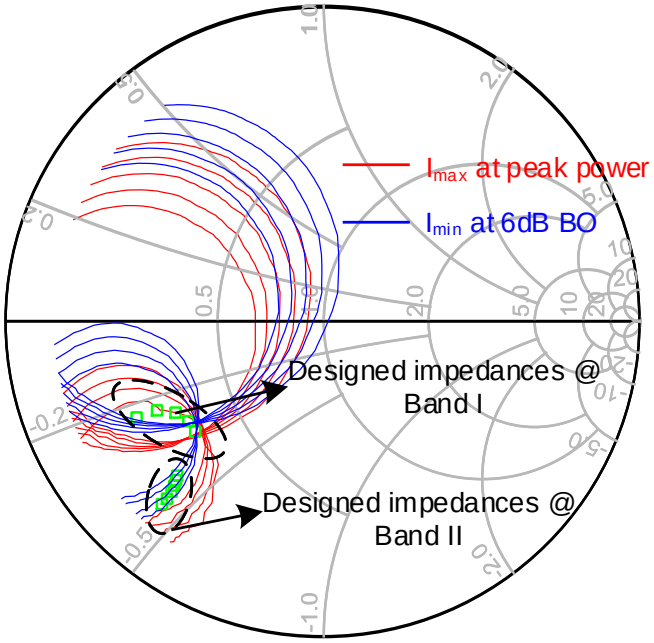



Figure 3.10: Designed fundamental impedances with the current contour technique

small signal gain of the main PA and the power splitting ratio of the power divider can be calculated accordingly.

Figure 3.10 shows the current contours at the peak and back-off power level across the two bands. The fundamental impedances, shown as the scattered rectangles, were synthesised within the accepted region in the smith chart through simplified real frequency technique (SRFT). Then the lump elements L-C generated by the SRFT were transformed to transmission lines and series connected capacitors. Second harmonic impedances have to be carefully monitored to avoid falling into the bad region. The achievable gain at the peak power level for these source impedances are 9dB across the two bands.

To obtain an overall 10-dB Doherty power amplifier, an 1dB uneven splitting ratio power divider is needed to compensate the gain of deep biased Class C PA. Hence the small signal gain required for the main PA would be 14 dB gain. Thus the input matching network for the main amplifier was designed based on the 14-dB gain circles contour at 8 dB back off power level (slightly backed from -6dB) with a load impedance of $2R_{opt}$. Figure

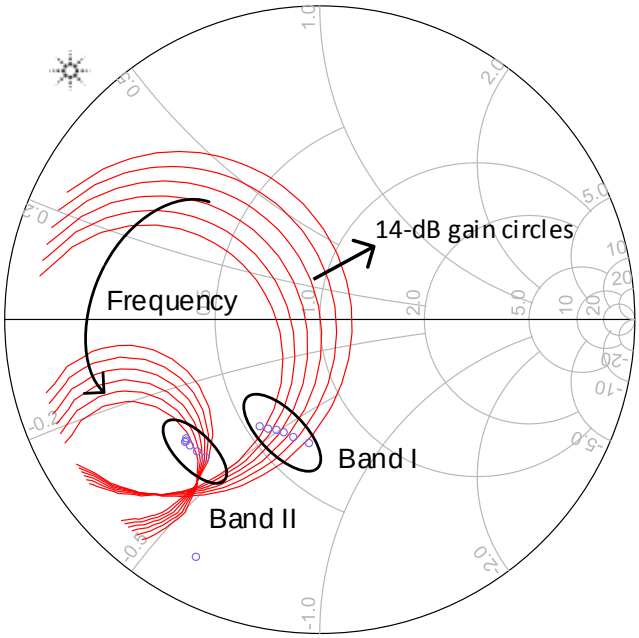



Figure 3.11: Designed fundamental impedances on 14-dB gain circles at 6dB back-off

3.11 shows the gain circles across the two bands and the achieved source impedances in the smith chart. These impedances over the two bands were constructed by the SRFT technique and then transferred to transmission line version.

### 3.3.3 Simulation Results of the Dual-band DPA

Having finished the IMN and OCN of the DPA, a phase shifter [26] was added at input of the main path to compensate the phase difference between the current profiles of the main and peaking. A three-section Wilkinson divider with 1-dB uneven power split ratio was designed to compensate the lower gain performances of the Class-C biased peaking device. It covers 1.9 - 7.6GHz frequency band to provide sufficient return loss and isolation between the two output ports over the fundamental and second harmonic ranges.

Figure 3.12 shows the simulated drain efficiency and peak power output versus frequency over the two bands. As can be seen, the 6-dB back off efficiency are above 42% over the

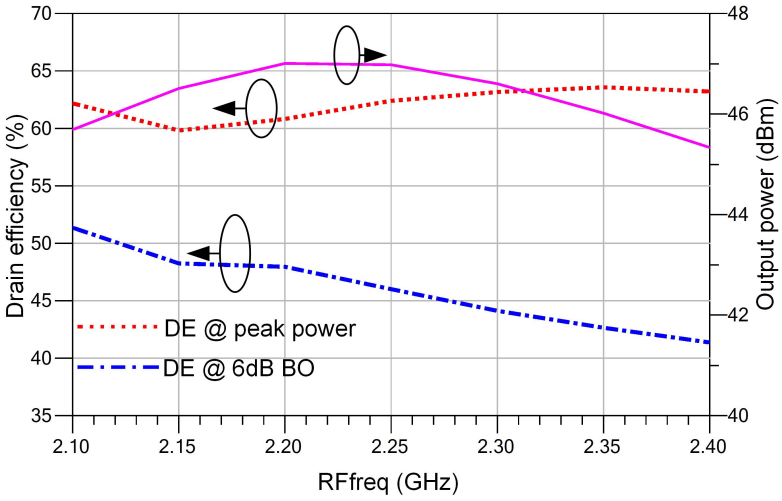
frequency range 2.1-2.4 GHz and 3.35-3.8 GHz. As well the peak power output in both bands are greater than 46 dBm. The gain versus input power is shown in Figure 3.13. The gain is over 8 dB and 9.5 dB over the first and second band, respectively and shows minimum variation during the whole Doherty operation. As noticed, the gain performances are not consistent 10-dB across the frequencies. That is because the impedance bandwidth limited dual-band phase alignment shifted the designed source impedances for the main transistor. The drain efficiency versus output power is presented in Figure 3.14. As shown in the figure, good Doherty behaviour is maintained in both of the bands and there is no performance degradation as that reported in the literature [2],[26].

## 3.4 Concurrent Dual-band Doherty Power Amplifier Measurements

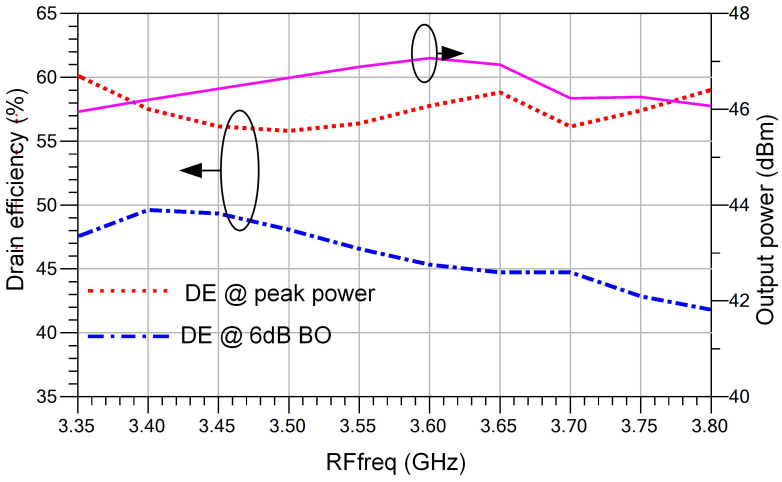
The DPA was fabricated on a Rogers 4003C 20-mil thick substrate. Figure 3.15 depicts the photograph of the fabricated DPA prototype. The implemented uneven splitter, input matching for main transistor, phase alignment network and the output combiner are labelled in the red dashed box.

Continuous wave measurements were initially performed to access the gain and efficiency performance of the DPA. To mitigate the thermal effect of the transistor, 15% duty cycle pulsed wave stimuli was applied in the set up. The measured CW drain efficiency and gain versus frequency across the two bands are plotted in Figure 3.16 and 3.17. 50 W peak output power are obtained at both bands. At the lower band, the gain is 7.5 - 9.5 dB over 2.05 - 2.3 GHz (12%) range. At the upper band, the gain is 9 - 11 dB over a 3.2 - 3.62 GHz range (12%). The drain effciency at the 6-dB output back-off are larger than 49% and 47% across the lower and upper bands, respectively. There is a frequency shift at the upper band which is attributed to the lack of accuracy in transistor models and board fabrication. Figure 3.18 and 3.19 demonstrate the drain efficiency versus output power at the two bands. As can be seen, nice Doherty behaviour and flat gain performances are observed at both targeted bands.

To gain insight of the linearizability of the fabricated dual-band DPA, single band and concurrent dual-band carrier aggregated WCDMA/LTE signals were applied to the DPA demonstrator. The first signal was two-carrier 20 MHz WCDMA signal with a 7.2 dB PAPR. The second signal was 80 MHz WCDMA and LTE intra-band carrier aggregated signal with a 10.6 dB PAPR. The third signal was the 20 MHz WCDMA and 20 MHz LTE inter-band carrier aggregated signal (concurrent dual-band) with a 9.6 dB PAPR.

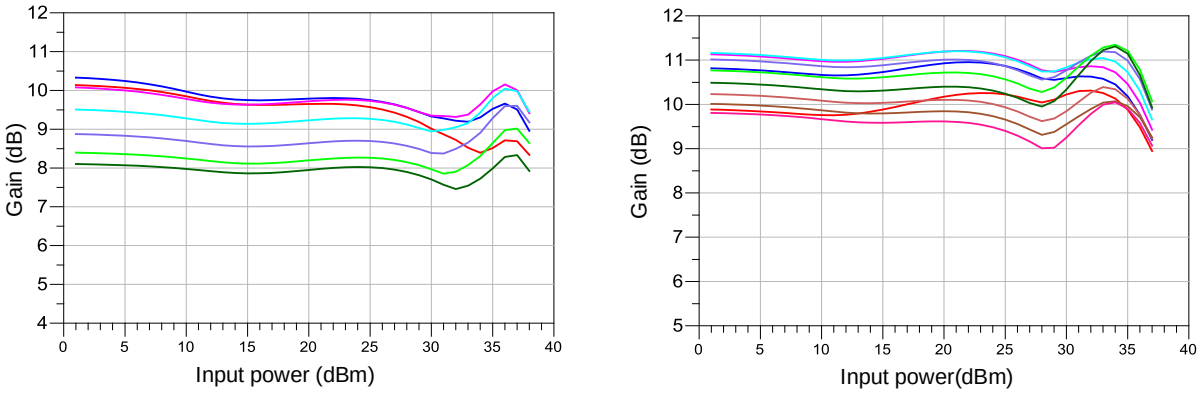



(a)



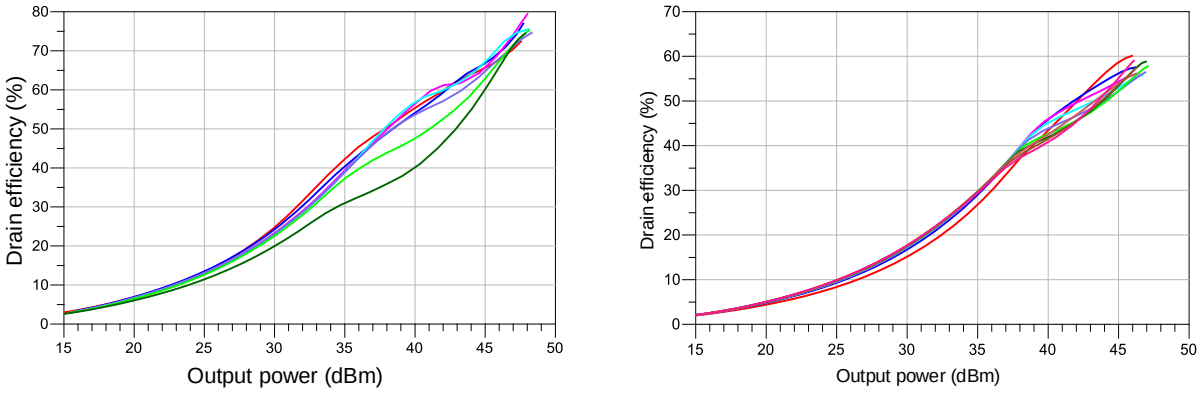

(b)

Figure 3.12: Simulated drain efficiency and peak output power versus frequency. (a) Lower band (b) Upper band




(a) (b)

Figure 3.13: Simulated gain versus input power (a) 2.1-2.4 GHz (b) 3.35-3.8 GHz




(a) (b)

Figure 3.14: Simulated gain versus input power (a) 2.1-2.4 GHz (b) 3.35-3.8 GHz

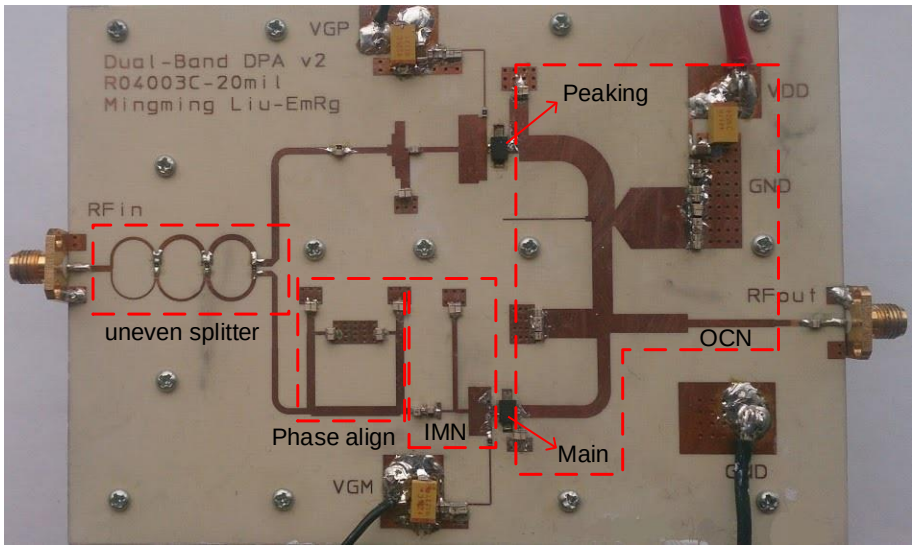



Figure 3.15: Photo of the dual-band DPA prototype

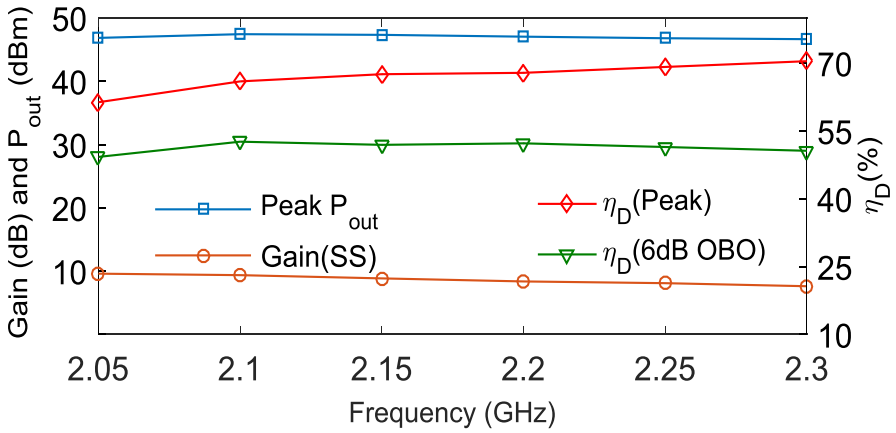



Figure 3.16: Measured CW drain efficiency and gain versus frequency at lower band

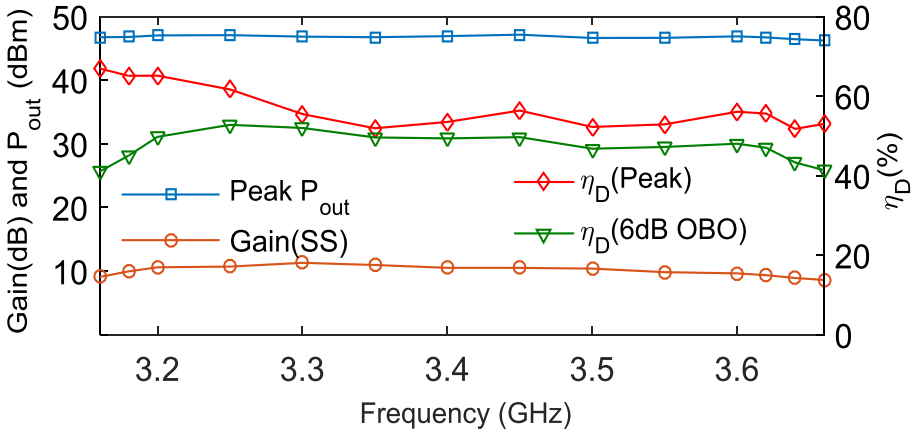



Figure 3.17: Measured CW drain efficiency and gain versus frequency at upper band

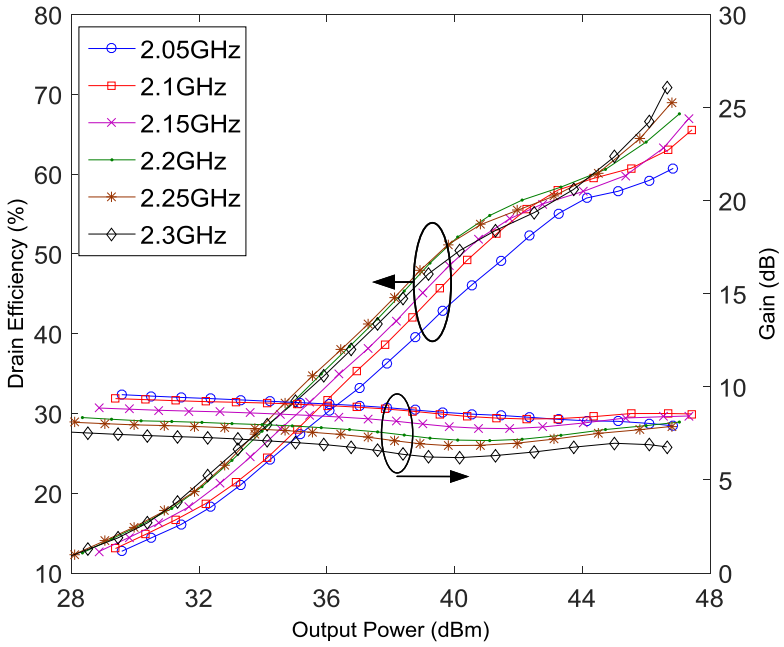



Figure 3.18: Measured CW drain efficiency and gain versus output power at lower band

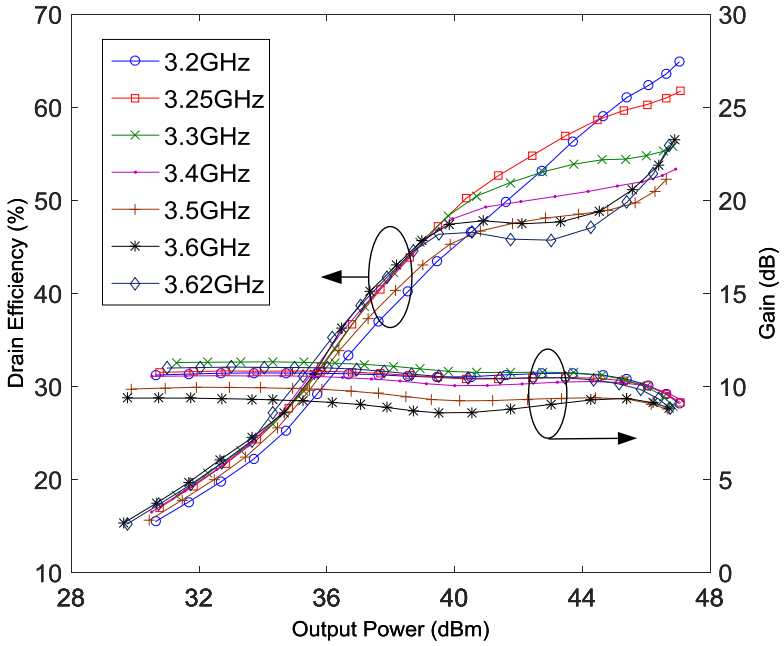



Figure 3.19: Measured CW drain efficiency and gain versus output power at upper band

Table 3.1: Comparison with published dual-band DPAs

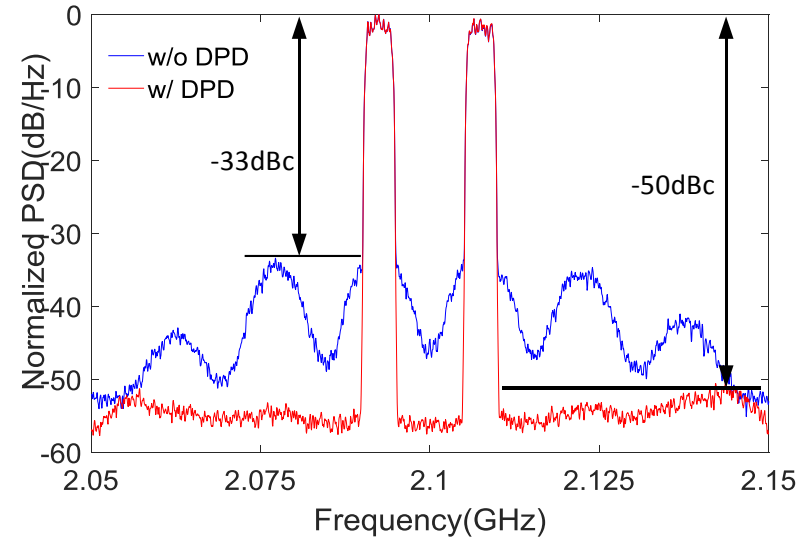
| | First Band/Second Band | | | | Modulated Signals | |
|---|---|---|---|---|---|---|
| Ref. | Frequency (GHz) | Peak Power (dBm) | $\eta_D$(%) @ 6 dB OBO | FBW (%) | Single Mode | Concurrent Mode |
| [27] | 1.8/2.4 | 43/43 | 60/44 | - | 10 MHz | 10 MHz |
| [3] | 0.85/2.33 | 44/42.5 | 45/41 | - | 10 MHz | - |
| [26] | 1.96/3.5 | 41.6/42.3 | 44/32 | - | 5 MHz | - |
| [11] | 0.75/2.15 | 45/46 | 43/45 | 13/5 | - | - |
| **T.W** | **2.15/3.4** | **47.3/47** | **52/51** | **12/12** | **up to 80 MHz** | **20 MHz** |

Figure 3.20 shows the measured power spectrum density (PSD) of the DPA before and after applying DPDs under a 20 MHz WCDMA stimuli. As seen, in the both bands, the PA achieved linear results after DPD with a ACLR of -50 dBc at the output. The obtained average power in the lower and upper band are 39.5 dBm and 39.1 dBm with an average drain efficiency of 41.5% and 43.4% respectively.

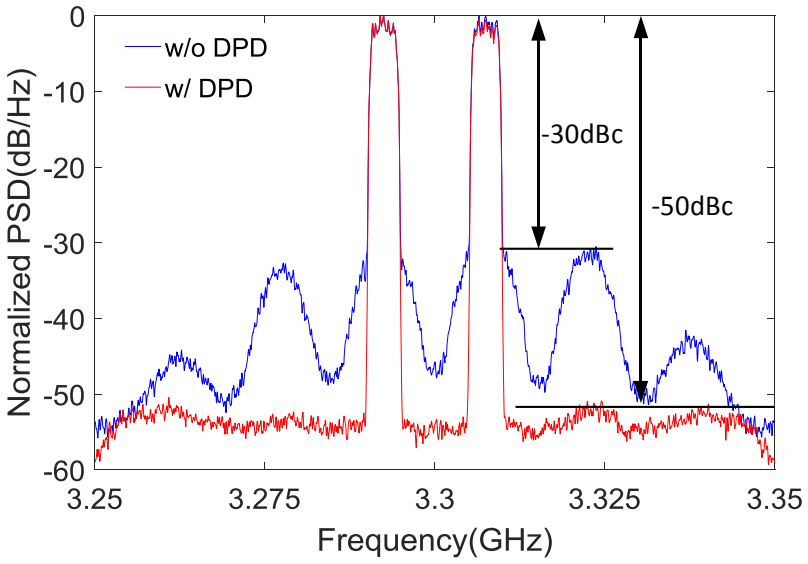
To validate the linearizability under carrier aggregated signals, a 80 MHz WCMDA and LTE aggregated signal was applied to the PA and the test results are shown in Figure 3.21. In the lower and upper band, the PA exhibited linear results with a ACLR of -45dBc and -46dBc after DPD. The achieved average output power are 36.3dBm and 36.5dBm and the drain efficiency at this power level are 33% and 33.4%, respectively.

To further confirm the capability of the PA working under inter-band carrier aggregated signals, the PA was driven by 20 MHz 4C-WCDMA signal and 20MHz LTE signal at 2.25 GHz and 3.25 GHz concurrently. The dual-band DPD [7] successfully linearized the circuit with a ACLR of -46dBc and -49dBc in the lower and upper band accordingly at 37.1 dBm average power output. The obtained drain efficiency is 34.8%.

To sum up, the linearity of the PA was validated by applying the DPD under the various carrier aggregation stimuli. Table 3.1 compares this work against state-of-the-art concurrent dual-band DPAs from the literature. Though in highest power level and frequency range, the dual-band DPA in this work outperforms all others in terms of efficiency, linearity and the fractional bandwidth in each band.

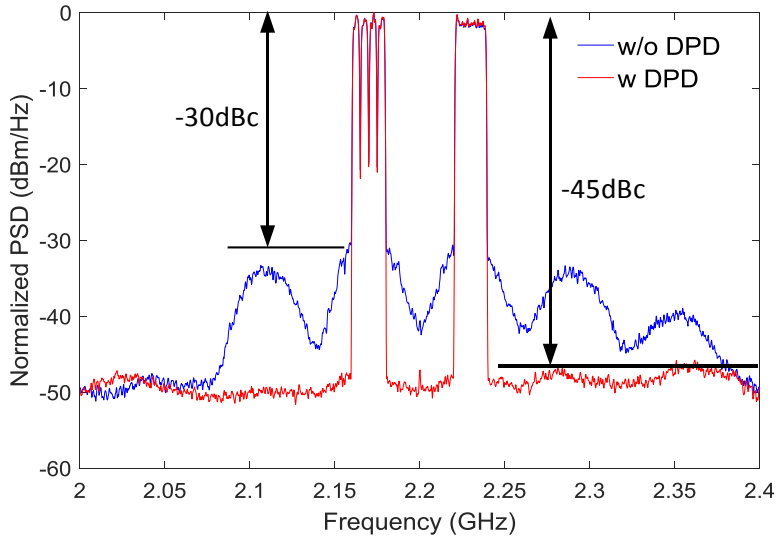



(a)

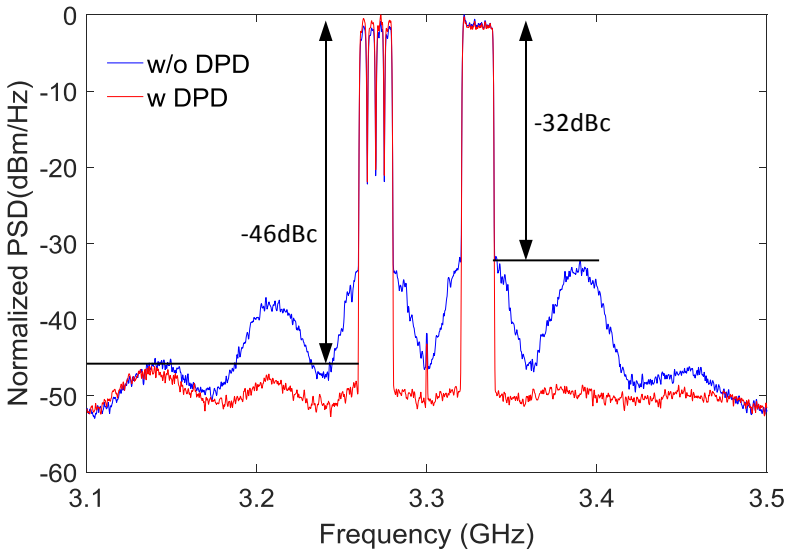



(b)

Figure 3.20: Measured output spectrum of the DPA before and after linearization under 20 MHz WCDMA modulated signal. (a) Lower band (b) Upper band

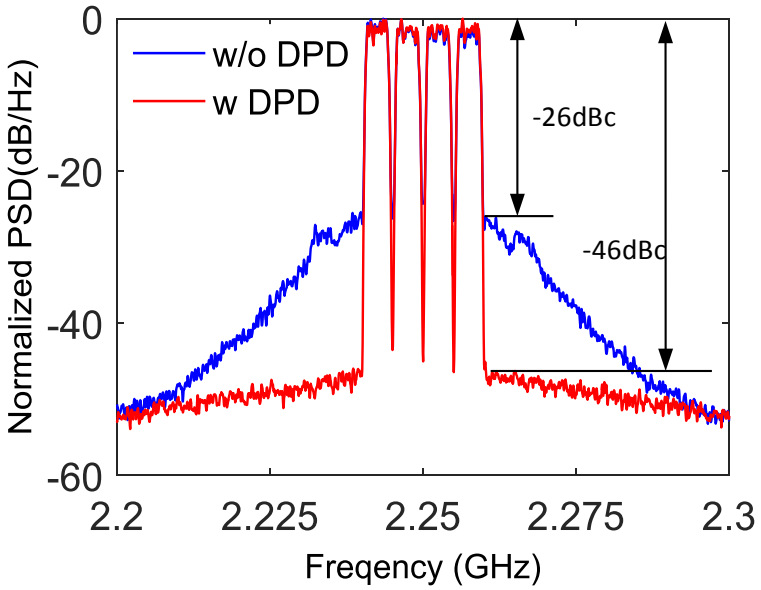



(a)

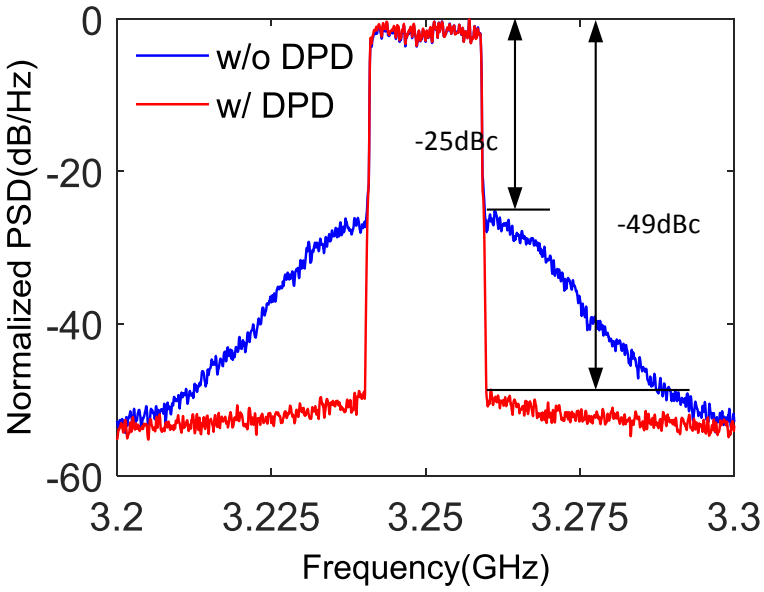



(b)

Figure 3.21: Measured output spectrum of the DPA before and after linearization under 80 MHz WCDMA and LTE aggregated signal. (a) Lower band (b) Upper band




(a)




(b)

Figure 3.22: Measured output spectrum of the DPA before and after linearization under concurrent dual-band WCDMA and LTE aggregated signal with 20 MHz modulation bandwidth. (a) Lower band (b) Upper band

# Chapter 4

# Dual-band Three-way Doherty Power Amplifier Design and Results

It is evident from the measurement results in Chapter 3, the PAPR of carrier aggregated signals normally falls between 8 - 10 dB. For example, the PAPR value of 80 MHz WCDMA and LTE aggregated signals reaches as high as 10.6 dB. The drain efficiency of the classic two-way Doherty PA drops to 33% when handling such signals since the first efficiency peak of the classic DPA happens at 6 dB back-off. Therefore, a three-way Doherty power amplifier is needed to amplify such carrier aggregated signals with a higher PAPR. This chapter provides the theory and design of a dual-band three-way DPA.

## 4.1 Introduction of the Three-way Doherty Power Amplifier

The theory of the three-way Doherty PA design was given in [10], as shown in Figure 4.1. For ease of theoretical analysis, the transistors are modelled as voltage controlled current sources. The current profiles of the transistors are expressed as

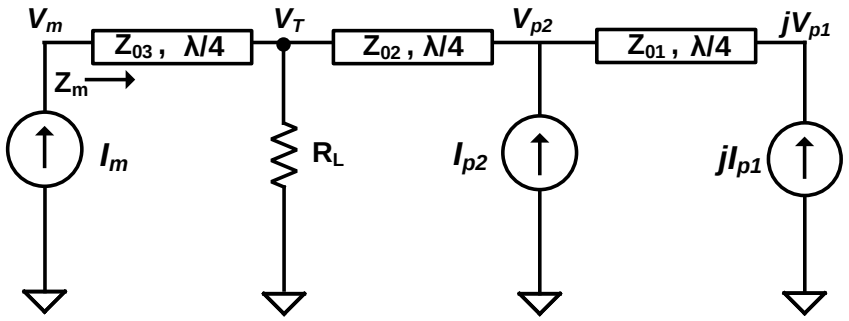



Figure 4.1: Three-way Doherty in [10]

$$I_m(v_{in}) = \begin{cases} I_M \cdot v_{in}, & 0 \leq v_{in} \leq 1, \\ I_M, & v_{in} > 1, \\ 0, & elsewhere, \end{cases} \tag{4.1}$$

$$I_{p1}(v_{in}) = \begin{cases} I_{P1} \cdot \frac{v_{in}-k_1}{1-k_1}, & k_1 \leq v_{in} \leq 1, \\ I_{P1}, & v_{in} > 1, \\ 0, & elsewhere, \end{cases} \tag{4.2}$$

$$I_{p2}(v_{in}) = \begin{cases} I_{P2} \cdot \frac{v_{in}-k_2}{1-k_2}, & k_2 \leq v_{in} \leq 1, \\ I_{P2}, & v_{in} > 1, \\ 0, & elsewhere, \end{cases} \tag{4.3}$$

where $k_1$ and $k_2$ are the breakpoints of the peaking devices where the peak efficiency of the DPA occurs. Consider the output combiner network as a 3-port network that delivers the power to a included load resistor $R_L$. The 3-port output network is then reciprocal but lossy. By inspection and making use of the network reciprocity, the relationship between the voltage and current profiles can be written as

$$\begin{pmatrix} V_m \\ jV_{p1} \\ V_{p2} \end{pmatrix} = \begin{pmatrix} \frac{Z_{03}^2}{R_L} & \frac{jZ_{01}Z_{03}}{Z_{02}} & 0 \\ \frac{jZ_{01}Z_{03}}{Z_{02}} & 0 & -jZ_{01} \\ 0 & -jZ_{01} & 0 \end{pmatrix} \cdot \begin{pmatrix} I_m \\ jI_{p1} \\ I_{p2} \end{pmatrix} \tag{4.4}$$

By writing out $V_m$ in equation 4.4 and dividing $I_m$ on both sides of the equation

$$Z_m = \frac{Z_{03}^2}{R_L} - \frac{Z_{01}Z_{03}}{Z_{02}} \frac{I_{p1}}{I_m} \tag{4.5}$$

Similarly,

$$Z_{p1} = \frac{Z_{01}Z_{03}}{Z_{02}}\frac{I_m}{I_{p1}} - Z_{01}\frac{I_{p2}}{I_{p1}} \tag{4.6}$$

$$Z_{p2} = Z_{01}\frac{I_{p1}}{I_{p2}} \tag{4.7}$$

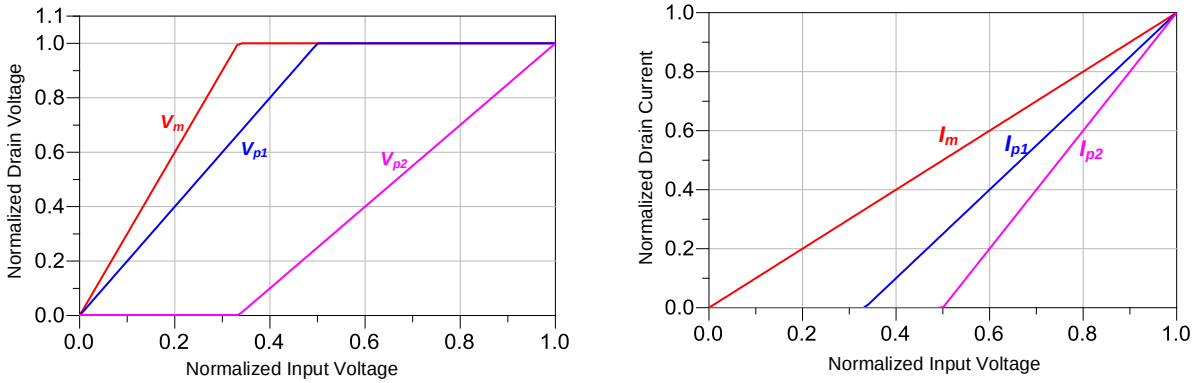
As can be seen in equations 4.5 - 4.7, load impedance seen by the main is only modulated by the drain current from peaking #1 but has no effect from the current from peaking #2. The current from peaking #2 will only modulate the impedance seen by peaking #1. This load modulation behaviour is dictated by the topology of the output combiner. Seen by the main device, peaking #1 and #2 together behave like a larger peaking device which can be treated as a voltage controlled current source. Hence the voltage at the load $V_T$ is determined solely by the main current which enforces the linearity of the DPA. This conclusion is the same as the two-way Doherty in Chapter 2. Following the design equations in [10] as shown in 4.8 - 4.10 and setting $k_1 = 1/3$ and $k_2 = 1/2$, the achieved current and voltage profiles for the three-way Doherty are shown in Figure 4.2. As seen, the current from the main device is linear, the output voltage at the load is linear as well. The peak efficiency points happen at -9.5 dB and -6 dB back-off levels, respectively, as illustrated in Figure 4.3.

The load modulation behaviour mentioned above happens at the centre frequency. As seen in equation 4.8 - 4.10, with fixed value of $k_1$, $k_2$ and $R_{opt}$, any chosen load impedance $R_L$ will correspond to a solution, $Z_{01}$, $Z_{02}$ and $Z_{03}$, generating the same voltage and current profiles as shown in Figure 4.2 at the center frequency. While the bandwidth (BW) of these solutions are different. According to [10], the BW of the three-way DPA shows strong dependence on the value of $R_L$ and can be optimized through choosing a proper $R_L$.

$$Z_{01} = \frac{R_{opt}}{k_2(1/k_1 - 1)} \tag{4.8}$$

$$Z_{02} = \frac{1}{1/k_1 - 1}\sqrt{1/k_1 R_L R_{opt}} \tag{4.9}$$

$$Z_{03} = \sqrt{\frac{1}{k_1}R_L R_{opt}} \tag{4.10}$$




(a) (b)

Figure 4.2: Voltage and current profiles for three-Way Doherty PA with $k_1 = 1/3$ and $k_2 = 1/2$

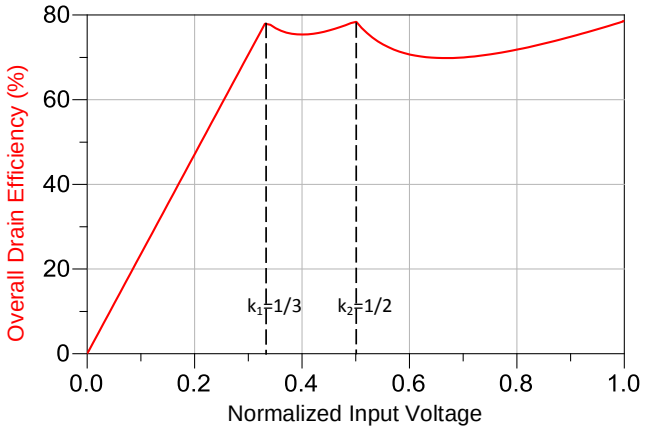



Figure 4.3: Overall Drain Efficiency of the three-way Doherty with $k_1 = 1/3$, $k_2 = 1/2$

Table 4.1: Design parameters of the three-way Doherty(units:Ω)

| $Z_{01}$ | $Z_{02}$ | $Z_{03}$ | $Z_T$ | $R_L$ |
|---|---|---|---|---|
| 25 | 16.4 | 33 | 12 | 50 |

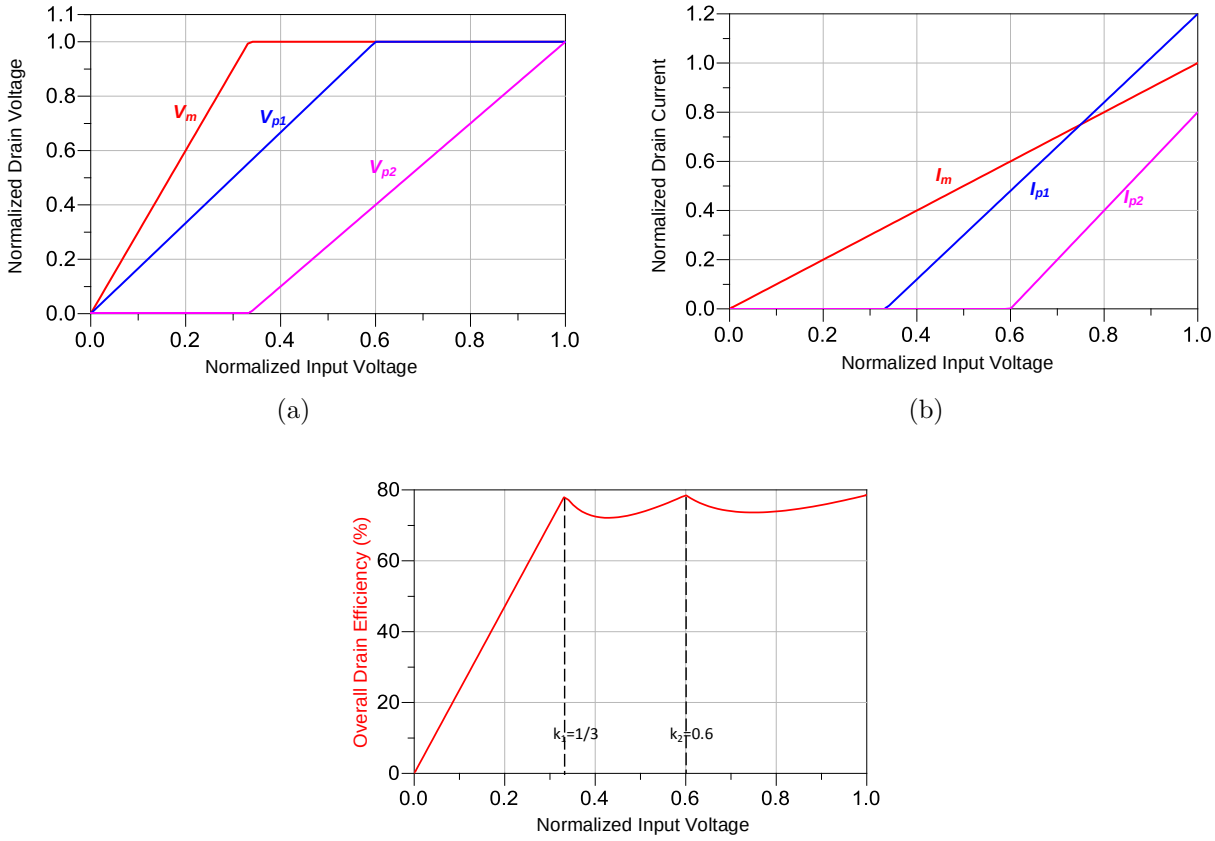
## 4.2 Dual-band Three-way Doherty Power Amplifier Design

### 4.2.1 Output Power Combiner

The proposed design methodology in Chapter 3 can also be applied to the three-way Doherty power amplifier implementation. To evenly distribute the peak efficiency points, $k_1 = 1/3$ and $k_2 = 0.6$ are chosen in this design which corresponds to a peak efficiency at -9.5 dB and -4.5 dB power back off, respectively. The ideal current and voltage profiles change accordingly as shown in Figure 4.4. The output combiner is implemented as shown in Figure 4.5. The parasitic capacitances from the devices are integrated with the dual-band impedance inverters that have the equivalent characteristic impedances $Z_{01}$ and $Z_{03}$, as seen in the magenta-dashed box. The optimum output impedance for the main transistor is 30 Ω. The input impedance $Z_T$ looking into the combining node is 12 Ω for achieving the best bandwidth [10]. With the design equations 4.8 - 4.10 and the designated $k_1$ and $k_2$, the design parameters for the three-way DPA are listed in Table 4.1. The simulated impedance profile for the main transistor is shown in Figure 4.6. As demonstrated in the figure, the desired back-off and full power impedance profile can be maintained over the two designed bands. The fundamental impedance profile is properly controlled such that the transistor is operating in continuous Class B/J* mode where the requirements on second harmonic termination are relaxed.

### 4.2.2 Input Matching Networks

Three equal-sized devices are deployed in this design. The maximum fundamental current from the main, peaking #1 and peaking #2 are 1.1 $A$, 1.3 $A$, 0.9 $A$, respectively. The total output power from the three devices is around 60 Watts. The current circles contour technique was implemented to realize the required current profiles as shown in 4.4b. The gain contour for the main transistor were performed at the 10 dB back-off region with a load impedance of $3R_{OPT}$. Current contours for peaking #1 and peaking #2 were implemented




(a) (b)

(c)

Figure 4.4: Doherty profiles (a) voltage (b) current (c) overall Drain efficiency for three-way Doherty PA with $k_1 = 1/3$ and $k_2 = 0.6$

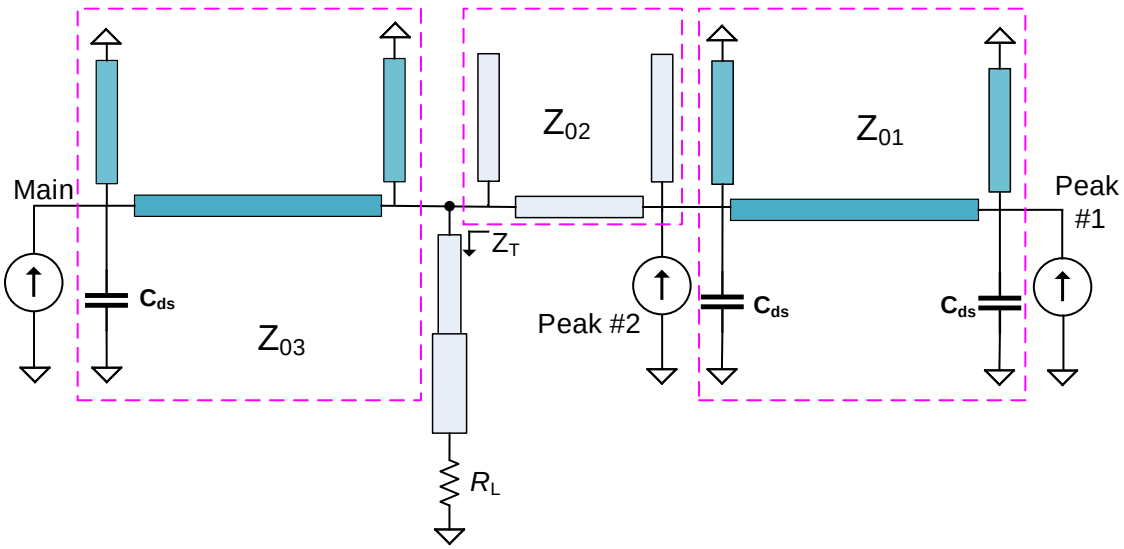



Figure 4.5: Implemented output combiner of the three-way Doherty PA

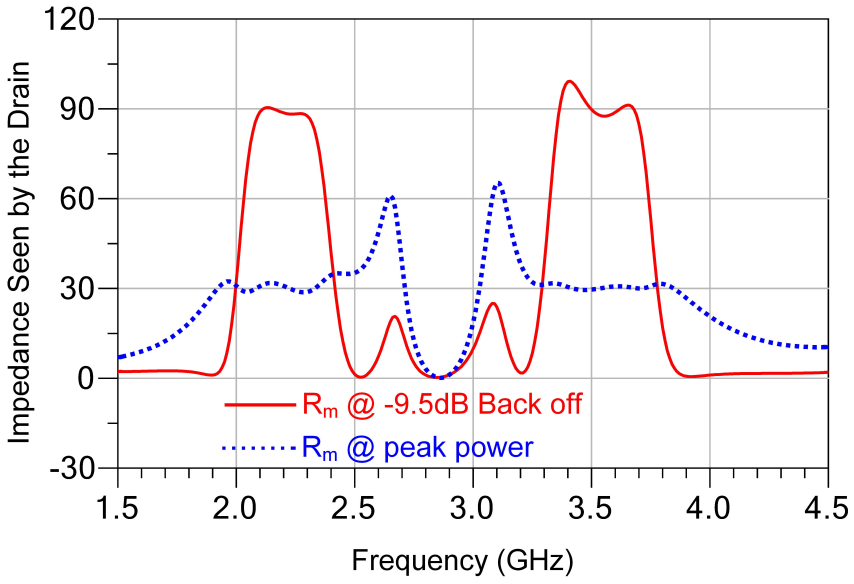


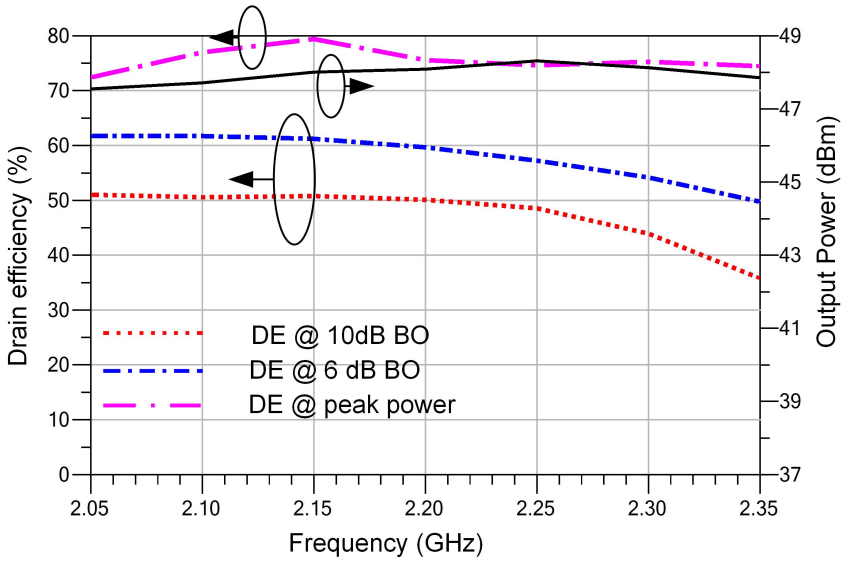

Figure 4.6: Impedance seen by the main transistor

to guarantee the necessary transconductance over the two frequency bands. Again the second harmonic at the input of the three devices are carefully monitored to avoid any unwanted distortions and efficiency drop.

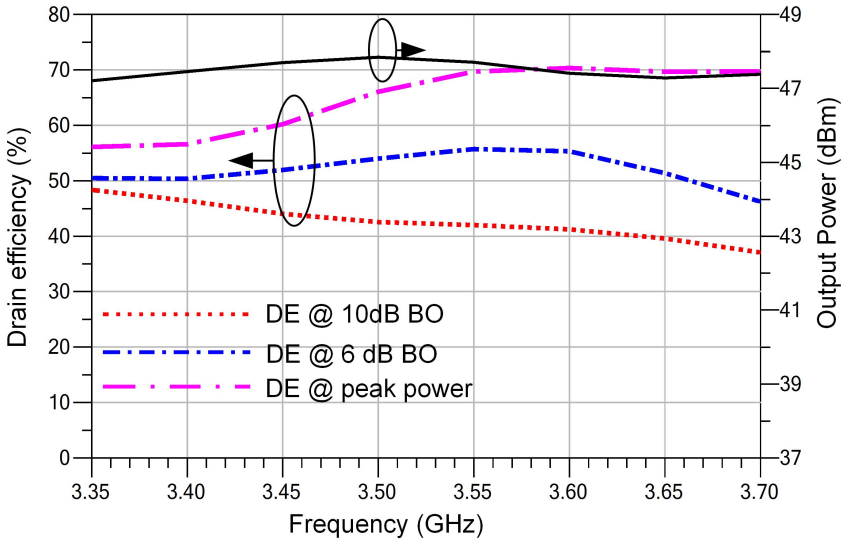
### 4.2.3 Dual-band Three-way Doherty Power Amplifier Simulations

Once the output power combiner and the three input matching networks for the three transistors were completed, a wideband three-way equal-ratio power splitter was designed to connect the three paths. It provides enough isolation between the three branches from the fundamental to the second harmonic frequency. Two dual-band phase alignment networks were enforced at the main and peaking #2 paths separately to assure the required phase relationship between the current profiles.

The simulated drain efficiency and output power versus frequency are plotted in Figure 4.7. As seen, the drain efficiency is above 40% across 2.05-2.32 GHz and 3.35-3.65 GHz at 10 dB back-off. As well, the output power is within 47.5-48.3 dBm at the first band and 47.2-47.8 dBm at the second band. Figure 4.8 shows the gain versus input power over the two bands. The gain is above 9 dB and shows a minimum variation in the whole Doherty operation. The drain efficiency versus output power is shown in Figure 4.9. As shown in the figure, good Doherty behaviour is maintained in both the designed frequency bands.

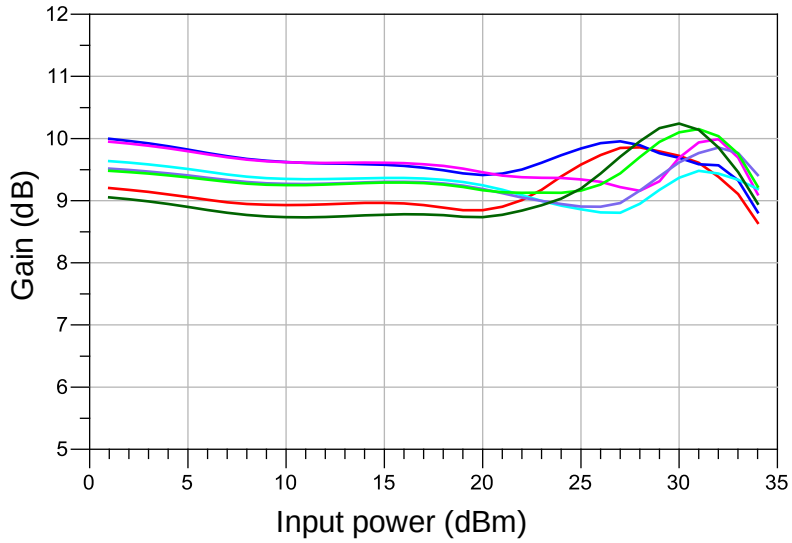



(a)

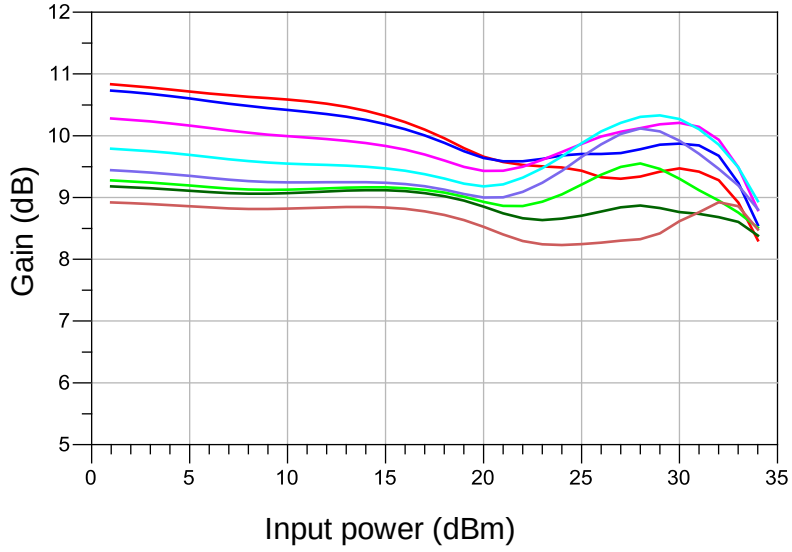



(b)

Figure 4.7: Simulated efficiency and output power versus frequency (a) Lower band (b) Upper band

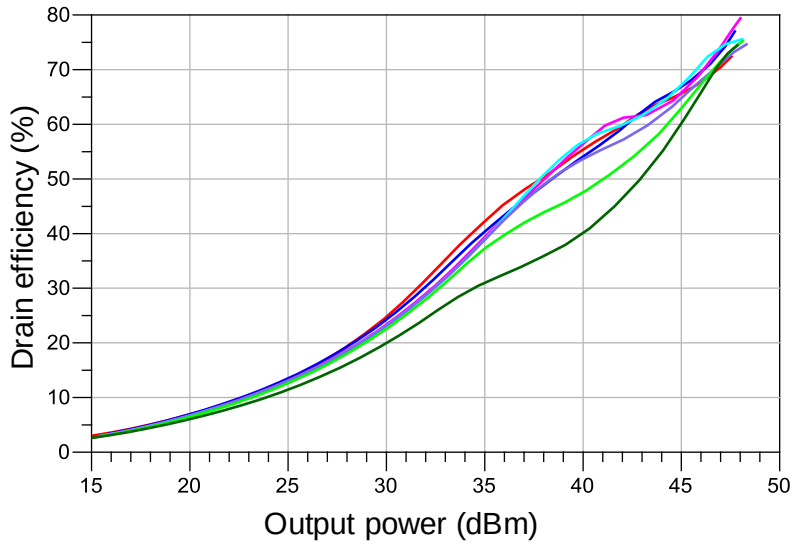



(a)

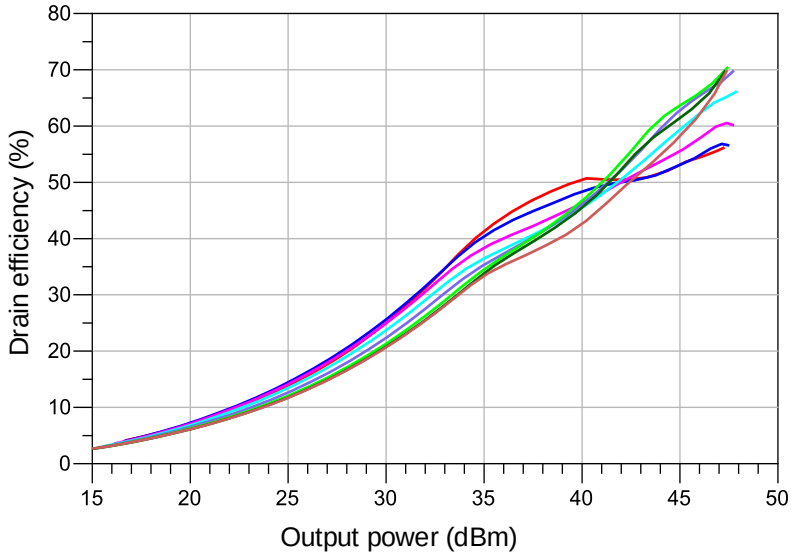



(b)

Figure 4.8: Simulated gain versus input power (a) 2.05-2.35 GHz (b) 3.35-3.7 GHz




(a)




(b)

Figure 4.9: Simulated drain efficiency versus output power (a) 2.05-2.35 GHz (b) 3.35-3.7 GHz

# Chapter 5

# Conclusion and Future Work

## 5.1 Conclusion

This thesis first discusses the evolution of wireless communication systems to achieve the high spectral efficiency with the deployment of carrier aggregation concept and high power efficiency when amplifying signals with a high PAPR. Various classes of operation modes in PA design are discussed, but these single-ended PA topologies do not provide a good enough efficiency at power back-off levels. The dual/multi-band Doherty power amplifiers is a promising solution to solve the stringent requirements of the modern transmitters including high efficiency at power back-off levels, high linearity and multi/dual-band operational capability.

Most of the existing dual-band Doherty power amplifiers were designed using a modularized building block approach. In this approach, a pre-implemented single-band output matching networks, phase offset lines, impedance inverters were replaced into the dual-band equivalent circuits. This design flow leads to a very complicated and sensitive multi-band Doherty PA design. As a result of the increased sensitivity to the circuit parameters, the load modulation condition deteriorates quickly and the operational bandwidth is compromised. Moreover, the reported results in these publications show performance degradation in one of the targeted bands. Hence the existing dual-band Doherty PA can hardly support the carrier aggregated signals in modern wireless communication system.

To combat the existing issues, a modified impedance inverter is proposed and a novel output combiner network is presented in this thesis to facilitate the absorption of the transistor output parasitics, which allows the designer to gain the access to current source

plane of the device. As a result, the bandwidth limiting dual-band phase offset lines can be eliminated and the fractional bandwidth can be enlarged. In addition, a low impedance short-end stub implemented in the output combiner can serve as a bias feed for both devices, which provides a small low frequency impedance to both transistors, thereby improving the linearizability of the PA under various carrier aggregated stimuli. Lastly, a gain contour at the back-off power level was proposed to improve gain flatness during the whole load modulation process and mitigated adverse the effect caused by the non-linear input capacitance. This input design methodology further enhances the AM-AM performances of the DPA.

Next using the proposed design methodology, a 50 W two-way GaN HEMT DPA was developed with the Keysight ADS software. The targeted two bands are 2.0-2.4 GHz and 3.4-3.8 GHz. The simulated results showed a gain of over 9 dB across the two bands and an efficiency of more than 43% at 6-dB back off. To validate the simulations, the designed dual-band DPA was fabricated and tested. The measured gain is 7.5-9.5 dB and 9-11 dB gain at the lower band and upper band, respectively. At 6 dB back off, the drain efficiency of the measured PA is larger than 49% and 47% at lower and upper band, respectively. The linearity of the DPA was verified by applying intra-band carrier aggregated signals with a bandwidth of up to 80-MHz, PAPR of 10.6 dB. The PA exhibits linear results after DPD with an ACLR of -45 dBc and -46 dBc at the average power output of 36 dBm and drain efficiency of around 33%. Under concurrent mode, the PA was successfully linearized and obtained 37% drain efficiency when driven by a inter-band carrier aggregated signal with a 20 MHz modulation bandwidth in each band and an overall PAPR of 9.6 dB.

Additionally, the application of the carrier aggregated signals usually leads to a high PAPR value that falls between 8-10 dB. The efficiency of the classic two-way DPA with equally sized transistors deteriorates when dealing with such signals. To solve this problem, a three-way Doherty PA is designed with the proposed design methodology. The targeted two bands are 2.05-2.32 GHz and 3.35-3.7 GHz which corresponds to a fractional bandwidth of 13% and 10%. The simulated PA shows a flat gain greater than 9 dB across the two bands. The simulated drain efficiency at 10 dB power back-off are greater than 40 % in the both bands.

## 5.2 Future Work

With the development of this work, three main areas were identified for further research work. First, as reported in Chapter 4, the measurements of the three-way dual-band DPA needs to be done to validate the simulation results. Second, the proposed topology

required that the 2nd harmonic frequencies of the first band do not overlap with the fundamental frequency of second band. During operation, the overlap may cause a problem with the circuit efficiency and power delivery. The design methodology can be revised to use a balun like structure [12] to allow the designers to control the fundamental and harmonic impedance independently, such that the centre frequencies of the two band can be selected arbitrarily. Lastly, the proposed output combiner can also be extended to higher microwave frequencies (6-30 GHz) as well as millimetre-wave frequencies (30-70 GHz) to meet the requirements of next generation (eg. 5G) base-station PAs. For example in Silicon base technologies, the low quality factor of the passive devices makes integration of the conventional dual-band DPA extremely challenging. The proposed impedance inverter in this thesis can be transformed into its compact lumped-element equivalent such that the loss in passive circuit can be minimized, while being capable of absorbing the output parasitics from the active devices. From this point of view, the integration of dual-band DPA at higher frequencies can be possible.

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