Noise and Clock Jitter Analysis of Sigma-Delta Modulators and Periodically Switched Linear Networks

by

Yikui Dong

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Abstract

This thesis investigates general computer-aided noise and clock jitter analysis of sigma-delta modulators. The circuit is formulated at electrical circuit level. Modulators with either switched-capacitor, switched-current, or continuous-time loop-filters can be analyzed. The methods and algorithms are also applicable to periodically switched linear networks, such as switched-capacitor and switched-current filters.

Thermal noise is an important source limiting circuit resolution, but traditional frequency domain noise analysis is not applicable to sigma-delta modulators. Noise analysis of sigma-delta modulators has not been presented before. In this thesis we give a new time domain method. It is applied to thermal noise analysis and dithering analysis.

Clock jitter is another major source that results in performance degradation of analog sampled-data circuits. Despite the fact that clock jitter is usually random, previous methods were restricted to periodic jitter analysis. They are based on classical switched-capacitor methods that analyze the circuit by exploiting its periodic switching nature. The introduction of random jitter destroys the periodic switching pattern, and classical methods are not applicable. To overcome this problem, we present a new *varying-step* sampled-data method for analysis of linear time invariant circuits. It is applied to clock jitter analysis of periodically switched linear networks and sigma-delta modulators. No restrictions on the jitter waveform were imposed. It can handle either periodic or random clock jitter analysis.

Transition matrix and input-transfer vector play important roles in circuit theory. Evaluations of their time derivatives are needed for the special sampled-data method. In this thesis, direct computation methods for the derivative matrices and vectors are presented. They are based on circuit theory concepts and aimed at numerical computation.

The theories have been implemented in a computer program, and validated on nu-

merical examples. Comparisons are made with exact analysis, physical measurements, or experimental observations. The algorithms are efficient, and transient analysis of a typical sigma-delta modulator for several hundred thousand clock cycles is obtained in the order of minutes.

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I would like to thank all my friends who have provided me with joy and warmth throughout these years.

To my parents

for

their love and encouragement

Contents

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List of Abbreviations

A/D	Analog to digital
BDF	Backward differentiation formulae
CT	Continuous-time
D/A	Digital to analog
DAE	Differential algebraic equation
DR	Dynamic range
DSP	Digital signal processing
FFT	Fast Fourier transform
IF	Intermediate frequency
IV	Current-voltage
LLTI	Lumped linear time invariant
LPTV	Linear periodically time varying
LTI	Linear time invariant

MNA	Modified nodal analysis
ODE	Ordinary differential equation
opamp	Operational amplifier
PSD	Power spectrum density
PSL	Periodically switched linear
PWL	Piecewise linear
QV	Charge-voltage
RF	Radio frequency
RHS	Right hand side
rms	Root mean square
SC	Switched-capacitor
SDM	Sigma-delta modulator
SI	Switched-current
SNR	Signal-to-noise ratio

Chapter 1

Introduction

1.1 Motivation

Sigma-delta modulators (SDMs) are an important type of circuits that draw attention from both academia and industry. They are undergoing active research and development. In the last decade, hundreds of papers devoted to the design and analysis of SDMs have appeared in major electronics conferences each year. A paper collection [1] and a book for state-of-the-art reviews and tutorials [2] were also published recently.

Sigma-delta modulators are used for data conversion between analog and digital domains. One of their significant advantages is that the resolution of the overall converter can be much higher than the resolution of the internal quantizer and the precision of the analog circuitry. This enables fabrication of high resolution data converters with digital signal processing (DSP) circuits in a digital compatible process. SDMs are typically implemented as switched-capacitor (SC) circuits. Because of the increasing interest in low-power, low-voltage, and compact electronic circuits in telecommunication, switched-current (SI) and continuous-time (CT) SDMs have also emerged recently.

The performance of a SDM is usually characterized by its signal-to-noise ratio (SNR), which is the ratio of signal power to in-band noise power, or by its dynamic range (DR), which is defined as the input-signal range between 0 dB and maximum SNR. When most of the quantization noise is shaped out of the signal-band, the noise floor of a SDM is dominated by thermal noise, clock jitter, or other noise and distortion effects.

Thermal noise is generated by random thermal motion of electrons in resistors and semiconductors. It limits the resolution of a SDM in a fundamental way, and is a major factor restricting the performance of a voice-band SC SDM [3, 4]. Clock jitter is a small deviation of the clocking from its desired time instants. It increases noise level at the output of a circuit performing sampling operations [5, 6, 7, 8]. Clock jitter is another major contributor to performance degradation. It severely affects modulators designed for high frequency signals, especially when the loop-filters are continuous-time [9].

Although thermal noise and clock jitter are among the major factors limiting circuit performance, their contributions to total noise level remain unknown until physical measurements on the prototype chip are made. During the design cycle, knowledge of the noise and clock jitter performance still depends on guesswork of experienced designers. The hand analysis involved is often difficult and exhaustive. It lengthens the concept-to-market cycle.

With a harsh nonlinearity – the quantizer – placed in the feedback loop, a SDM is difficult to analyze. Many methods and tools [10, 11, 12, 13, 14, 15, 16, 17, 18, 19] have been described in the literature. However, after more than 15 years of constant research and development, methods for noise and clock jitter analysis of SDMs at the electrical circuit level are still not available.

Noise analysis is traditionally done in frequency domain. This includes the classical methods for linear time invariant circuits [20], and the methods developed for switched-

capacitor networks [21, 22, 23, 24, 25]. But because of the highly nonlinear nature of SDMs, frequency domain analysis is not applicable.

Time-domain noise analysis is the only possibility. Approaches based on linearization at each time step using Taylor series [26] or other expansion methods fail, as the state of the circuit is not solely decided by the signal content. At some time point, the noise can be comparable to the signal, and can change the comparator output. A new method for time domain noise analysis is needed. It must be able to work with the circuit without linearizing the quantizer, and, it must be efficient to facilitate the long transient simulation needs. Additional requirements include simulation accuracy to detect noise information in the presence of large signal waveforms. Time domain noise analysis of SDMs is not an easy task, as the circuits are high resolution and their performance measures are based on statistical averages over a very large number of samples.

In real life, clock jitter usually comes from the noise in the clock generating circuitry, or through coupling of various interference sources. It is not necessarily periodic, but often contains a broadband spectrum. Despite the importance of clock jitter on the performance of analog sampled data circuits like SC and SI filters, only a few researchers [27, 28] have touched upon this topic, and they simplified the analysis by restricting their attention to periodic jitter waveforms.

Both SC and PSL (periodically switched linear) network analysis methods are based on the periodic switching nature of the circuit. By partitioning the circuit into a ***finite*** number of phases, a set of charge-transfer or differential equations can be written. The circuit is analyzed by recursively solving these equations. If only periodic clock jitter exists, a circuit can still be partitioned into a finite, although larger, number of phases [27, 28]. Classical methods can be extended to accommodate their analysis [27, 28].

The introduction of random clock jitter results in an infinite number of phases. This

violates the ***fundamental assumption*** which classical SC and PSL circuit analysis methods are based on. A new method that can analyze the circuit with periodic and, more importantly, random jitter in the clocking is needed.

All sigma-delta modulator structures suffer from the idle-channel tone phenomenon. These tones degrade the quality of signal conversion [29]. Dithering is a technique that aims at eliminating the unwanted tones by adding small amount of noise to the circuit [30]. Dithering noise can be considered as additional noise source, and the method developed for noise analysis of SDMs can be extended for dithering analysis.

In summary, new methods are needed for thermal noise, clock jitter, and dithering analysis of SDMs at electrical circuit level. The desirable attributes include (i) efficiency and accuracy; (ii) applicable to switched-capacitor, switched-current, and continuous-time SDMs; (iii) suitable for computer application.

1.2 Objectives

This thesis proposes new methods for noise analysis, clock jitter analysis, and dithering analysis. It develops corresponding computational algorithms, and implements them in a computer program.

The result of this research is a set of new methods and algorithms as well as a simulation tool. Equations are formulated at electrical circuit level, and the simulator targets a wide variety of SDMs. The following elements can be included in the circuit representation: ideal or single-pole operational amplifiers, transistors working in small signal condition, external clocked switches, capacitors, resistors, inductors, independent current or voltage sources, all four types of linear controlled sources, and latched comparators or quantizers. General nonlinear and transistor level descriptions are not allowed.

The research is conducted in three steps:

1. Propose new methods and develop computational algorithms;
2. Implement the algorithms in a computer program;
3. Validate the methods, algorithms, and tool on numerical examples by comparing the simulation results with theory predictions, physical measurements, or experimental observations.

1.3 Thesis Organization

Chapter 2 reviews the background information associated with this thesis. After a brief introduction of SDMs, we discuss the trend from the early switched-capacitor to recent switched-current and continuous-time implementations. Comments on the advantages and drawbacks of each implementation are given. The methods and tools for analysis of SDMs are critically reviewed based on the following classifications: block level for conceptual design phase, electrical circuit level for circuit design phase, and low level full circuit simulation for design verification phase. Thermal noise, clock jitter, and dithering analysis at these three levels are discussed. At the end, sampled data analysis methods and a numerical Laplace inversion method are revisited.

Chapter 3 proposes a new method for noise analysis of SDMs. The method is general and systematic. Important electrical noise sources in integrated circuits are identified, and the modeling of thermal noise in frequency domain and time domain is reviewed. An overview of noise analysis methods is given, and an efficient time-domain method is proposed. By using this new noise analysis method, numerical examples are given on LTI (linear time invariant) circuits, PSL networks, and SDMs. The results are compared with exact analysis or physical measurements.

Chapter 4 extends the noise analysis method of chapter 3 to dithering analysis of SDMs. The present state of dithering analysis is briefly reviewed. Numerical examples are given to show the effect of dithering in breaking up limit-cycle patterns, and to demonstrate the effect of thermal noise acting as dithering noise.

Chapter 5 presents a new method for arbitrary waveform clock-jitter analysis of PSL networks. Formulation methods and computational algorithms for the time derivatives of the circuit transition matrix and the input transfer vector are provided. Simulation examples on the influence of random and sinusoidal clock-jitter on SC and SI filter performance are given.

Chapter 6 extends the method of chapter 5 to clock jitter analysis of SDMs. Examples are given to show the usefulness of the method. In particular, we study the role of clock jitter on the performance degradation of SDMs involved in direct RF/IF conversion. Simulation results are compared with experimental observations.

Chapter 7 summarizes the work presented in this thesis. Areas of further research are suggested.

Appendix A gives a brief description of the simulation tool developed – SDNoise. A block diagram of the program structure is included.

1.4 Original Contribution

Original contributions in this thesis are made in deriving new methods and algorithms for computer-aided analysis of SDMs, and in implementing them in a practical computer program. The phenomena studied include thermal noise, clock jitter, and dithering noise. To the best of the author's knowledge, they are the ***first ever*** noise analysis and the ***first ever*** clock jitter analysis methods available for SDMs at electrical circuit level.

In addition, this thesis ***contributes to circuit theory***: (1) by giving a *varying step* sampled data analysis method for LTI circuits; (2) by defining time derivatives of the circuit transition matrix and of the input transfer vector, and providing corresponding computational algorithms.

- The methods are ***general*** in that no restrictions on circuit topologies or jitter waveforms are made. They are applicable to both switched-capacitor, switched-current, and continuous-time SDMs.
- The methods and the tool can also be used for noise analysis of PSL networks where direct frequency domain analysis is not straightforward.
- The formulation is at electrical circuit level. It allows the study of noise contributions by individual circuit elements. The tool relieves the designer from exhaustive hand analysis and provides accurate results.
- The algorithms are efficient and accurate. Transient simulation of a typical SDM over several hundred thousand clock-cycles is obtained in the order of minutes.

Chapter 2

Sigma Delta Modulators: Background Review

In this chapter we review the background associated with noise and clock jitter analysis of SDMs. After a brief introduction of the basic concepts, we give an overview of the trends in circuit implementation. The simulation methods and tools are reviewed with emphasis on the noise and clock jitter analysis. Finally, sampled data analysis methods and a numerical Laplace inversion method are revisited.

2.1 Introduction to Sigma Delta Modulators

In this section, we briefly introduce oversampled sigma-delta modulators. Many excellent papers on this subject are also available [31, 32].

In modern VLSI technology, it is possible to fabricate large and complex digital signal processing circuits on a single chip. Compared with their analog counterparts, digital circuits have many benefits. For example, they are more suitable for design automation

and have higher noise immunity. Modern signal processing circuits are usually digital, but signals in the real world are analog. Data converters are needed to convert signals between analog and digital domains.

There are many types of data converters. Among them, oversampled sigma-delta modulation converters are known for trading off speed for resolution, and for shifting complexity from analog circuitry to digital circuitry. The resolution of the converter is much higher than the resolution of its internal quantizer and the precision of its analog circuitry. The price paid for low precision analog circuitry and high conversion resolution is increased complexity of the digital circuitry and low-to-medium signal bandwidth. The benefit brought by low precision analog circuitry is that the circuit can be fabricated in a digital compatible technology.

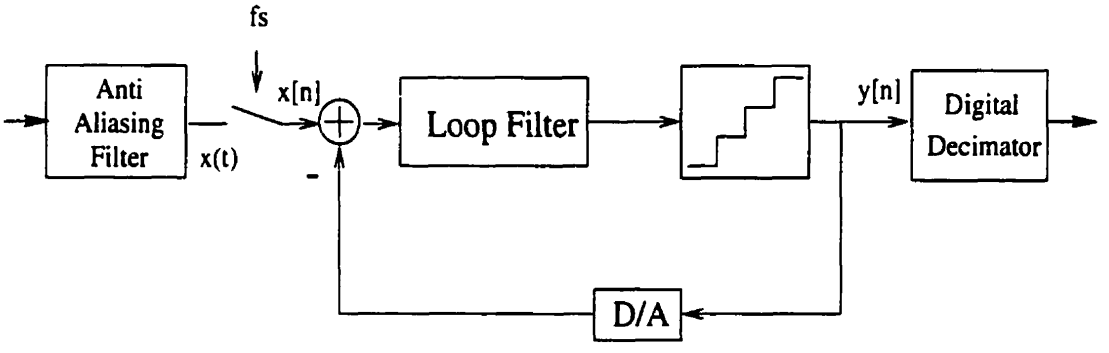


Figure 2.1: A sigma-delta modulation A/D converter

Two steps are needed to convert an analog signal into digital domain. First, the signal is sampled at discrete instants of time, then its amplitude is quantized into a finite set of values. The block level structure of a typical SDM is shown in Fig. 2.1. The anti-aliasing filter limits the bandwidth of the input signal before sampling. The SDM is used to perform the sampling and the quantization operations. Different transfer characteristics are applied to the input signal and the quantization noise. The power spectrum of the quantization noise is shaped over the sampling frequency band $[-f_s/2, f_s/2]$, with most

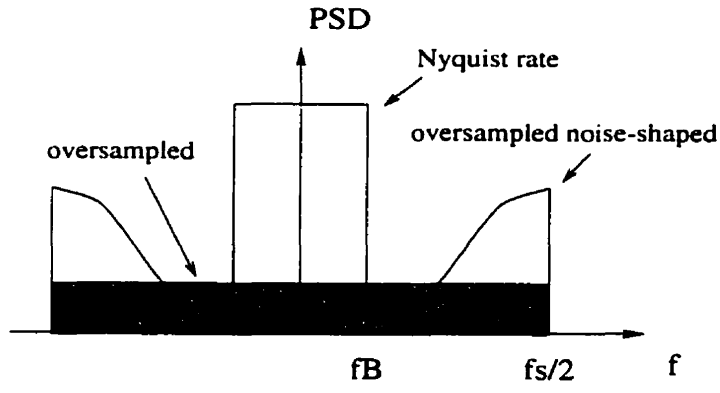


Figure 2.2: Quantization noise power spectrum density

of the noise power moved from low frequencies to high frequencies. This is shown in Fig. 2.2, along with a comparison with the power spectrum densities (PSDs) of Nyquist rate and oversampled data converters. In contrast to the noise shaping of the quantization noise, the signal transfer characteristics are not changed. A digital decimator is employed after the modulator to attenuate out-of-band noise and down-sample the signal to the Nyquist rate for digital signal processing or storage.

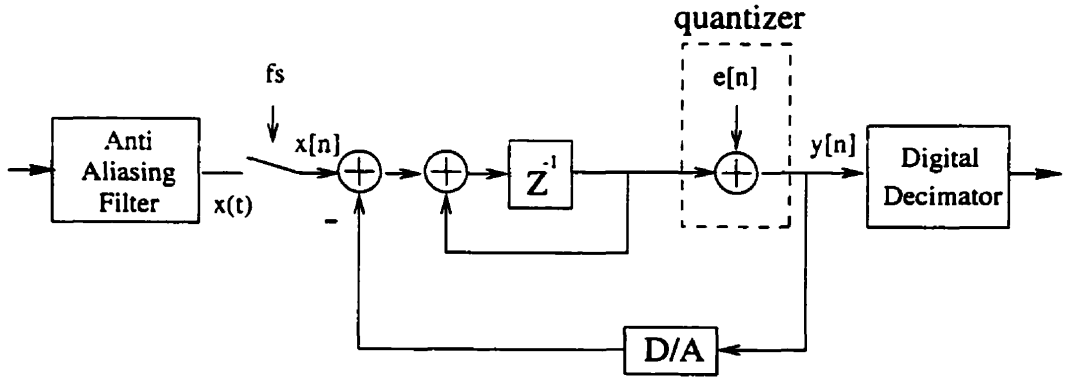


Figure 2.3: First-order sigma-delta modulation A/D converter

A first-order SDM consists of an integrator and a single or multi-bit quantizer in the

feedback loop, as shown in Fig. 2.3. Its transfer function in z-domain is [32]:

$$Y(z) = X(z)z^{-1} + E(z)(1 - z^{-1}) \tag{2.1}$$

where the output, $Y(z)$, is a function of the input, $X(z)$, and of the quantization noise, $E(z)$. The signal is delayed by one sample only, while the quantization noise is shaped by a first-order z-domain differentiator. A popular method[1] linearizes the circuit by replacing the quantizer with a noise source, usually a white noise of uniform probability density function over $\pm\Delta/2$, where Δ is the input step-size of the quantizer [34]. Based on this model, the in-band quantization noise power is [32]:

$$\sigma_{eq}^2 = \frac{\Delta^2}{12}\frac{\pi^2}{3}(\frac{2f_B}{f_s})^3 \tag{2.2}$$

where f_B is the signal bandwidth, and f_s is the sampling frequency. Note that the quantization noise power is inversely proportional to the cube of the oversampling ratio – the ratio of $f_s/2f_B$. Higher oversampling ratios result in lower in-band quantization noise power, and higher conversion resolution is obtained. Nevertheless, an upper limit on the oversampling ratio exists because of the fixed signal-bandwidth and the maximum operating speed available in a given technology. Higher order modulators are needed to further improve the conversion resolution.

A second-order SDM structure is shown in Fig. 2.4. Its z-domain transfer function is [32]:

$$Y(z) = X(z)z^{-1} + E(z)(1 - z^{-1})^2 \tag{2.3}$$

The signal is still delayed by one sample only, while the quantization noise is shaped by a second-order z-domain differentiator. Its in-band quantization noise power is [32]:

$$\sigma_{eq}^2 = \frac{\Delta^2}{12}\frac{\pi^4}{5}(\frac{2f_B}{f_s})^5 \tag{2.4}$$

[1]Although this approach produces useful insight, it fails to take into account the true nonlinear nature of the system. Many important effects, such as the tonal behavior and the modulator instability, cannot be studied [33]. This method will not be discussed further.

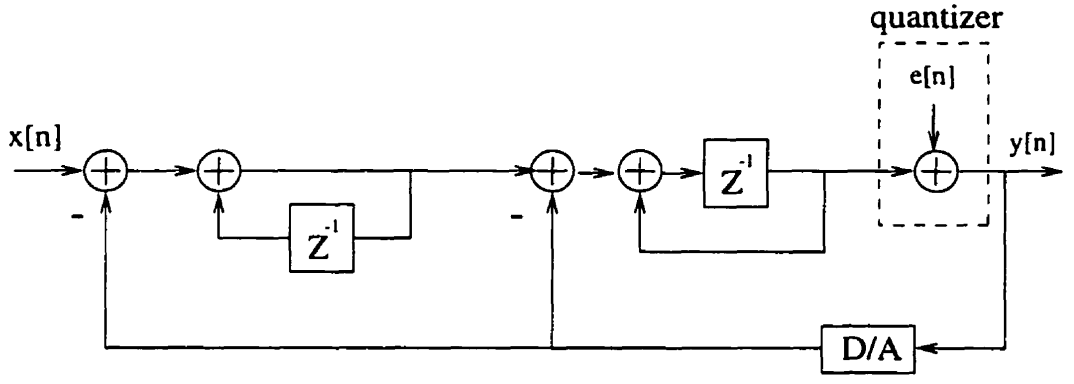


Figure 2.4: Second-order sigma-delta modulator

As shown in Fig. 2.5, high order SDMs can be employed to move even more quantization noise power out of the signal-band. They can be constructed as a simple expansion of the first and the second order modulators. However, modulators with this type of topology often suffer from stability problems [35]. An alternative for high-order noise transfer function is the multi-stage (MASH) configuration [36, 37], where the circuit is built by cascading stable single stages. An excellent review of high-order sigma-delta data converters can be found in [38].

Besides traditional lowpass sigma-delta circuits, bandpass systems [39, 40, 41] have also been studied and implemented in recent years.

2.2 Trends in Circuit Implementation

Monolithic analog filters can be classified as either discrete or continuous time circuits. The former include SC and SI filters, the latter include passive RLC, RC active, and G_m-C filters.

Sigma-delta modulators can be built with either discrete or continuous-time loop-filters. Discrete time implementations, especially SC SDMs, gained most of the attention

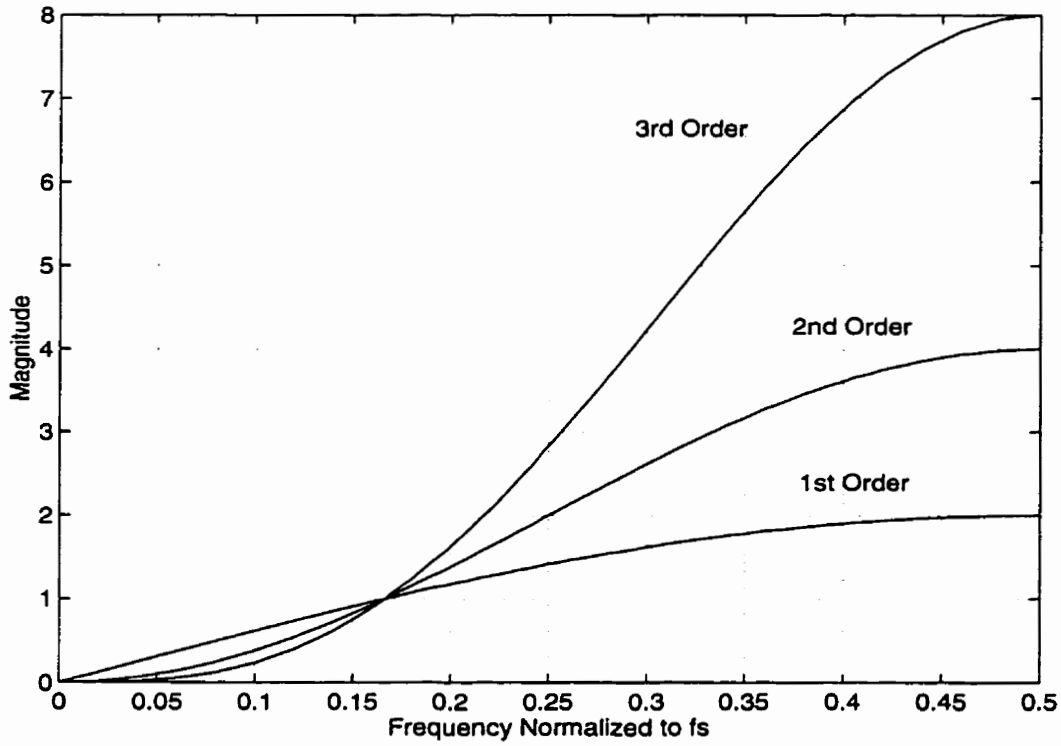


Figure 2.5: Noise transfer characteristics of sigma-delta modulators

in the past. However, SI and CT designs have experienced rapid development in recent years. A brief discussion of the reasons behind the evolution is given in this section.

2.2.1 Switched-Capacitor Sigma-Delta Modulators

A SC filter is formed by capacitors, operational amplifiers, and periodically operated switches. Its transfer function is defined by the clock frequency and the capacitor ratios, which are insensitive to process parameter and temperature variations [42]. SC techniques are ideal for realization of stable and accurate analog filters in low-cost digital compatible MOS technology. Most of the early designs of SDMs were implemented in SC technique [1].

The use of SC technique in high frequency applications, however, is limited by their requirement of the operational amplifiers and floating capacitors. Operational amplifiers (opamps) have to be fast enough to settle within half of the clock period. As a rule of thumb, the opamp bandwidth has to be at least 7 times larger than the clock frequency [42]. In addition, an extra layer of polysilicon is required on top of a pure digital CMOS process to implement linear floating capacitors. This is costly when most of the circuitry on the same chip is digital. The additional layer of polysilicon is even more difficult to obtain as the CMOS technologies move to the deep sub-micron range [43].

The trend towards deep sub-micron process also leads to reduced power supply voltages. This makes the design of wide dynamic range, high gain, and high speed voltage-mode circuit more difficult [43].

2.2.2 Switched-Current Sigma-Delta Modulators

Switched-current circuits operate with currents instead of voltages. They have the potential of high-speed and low voltage operation [43].

SI circuits can be implemented in a fully digital technology, as neither floating capacitors nor operational amplifiers are required, and the only building elements are transistors and switches. In addition, by eliminating operational amplifiers, SI circuits can operate at high sampling rates with much lower power consumption [44]. They also have the advantage of smaller size due to simplified circuit structure without floating capacitors [44]. SI technique is an ideal alternative for discrete-time analog circuit design, especially in low voltage and low power applications. It has attracted considerable interest from the integrated circuit design community [45, 46], and was quickly applied to SDMs [47, 48, 49, 44].

A major disadvantage of SI circuits is clock feedthrough, which increases both the

noise and distortion levels [50]. Due to the absence of large capacitors, this effect is much more severe than in SC circuits [42]. The impact of clock feedthrough can be reduced by using lower clock rates [44] with the side effect of limited operating speed.

2.2.3 Continuous-Time Sigma-Delta Modulators

By placing the data converters closer to the antenna, the complexity of a wireless communication system can be reduced and the reliability can be increased [51]. High frequency data converters are needed in this situation.

The majority of SDMs reported to date have discrete-time loop-filters in CMOS technology. The signal bandwidth of these SDMs is very restricted, usually to the audio range [6]. On the other hand, the realization of discrete-time SDMs in other high speed technologies, such as bipolar, is difficult [6].

Additional disadvantages associated with discrete-time SDMs are:

1. The design is complicated by the use of anti-aliasing continuous-time filters [42].
2. Large amounts of high-frequency noise can be aliased into the baseband. The increased in-band noise power can drastically reduce the dynamic range of a modulator [42]. Due to aliasing, it is well recognized that thermal noise is a major source that limits the resolution of a voice-band SC SDM.

It has been demonstrated that a continuous-time SDM designed in a given technology usually possesses higher signal bandwidth than its discrete-time counterparts [6]. Traditional continuous-time filters, such as passive RLC and active RC filters, are not suitable for monolithic implementation [52]. Fortunately, transconductor-C (G_m-C) filters can be implemented in a fully integrated form in any technology [52]. The frequency range of

transconductance circuits in CMOS technology extends well into 50 MHz range, and a frequency range larger than 500 MHz is possible in bipolar technology [52]. Because of the application of G_m-C filters, design of high-frequency continuous-time telecommunication circuits becomes feasible.

Sigma-delta modulators with G_m-C loop-filter were widely reported in recent years. The use of CMOS technology in high-frequency applications was explored in [5]. Another investigation in CMOS technology [9] studied low-power design for voice-band applications. Bandpass design in BICMOS technology [7] was also reported. The possible extension of the use of SDMs to intermediate/radio frequencies (IF/RF) by using high speed technologies was demonstrated in [6, 51].

The major complications in continuous-time modulators are:

1. Clock jitter contributes to the noise level and can become a significant problem [5, 6, 7, 8]. In a SC circuit, the charge is transferred in a short period of time after the clock edge. But in a CT circuit, the charge is transferred over the entire cycle. It is expected to be more sensitive to clock jitter [9].

2. The frequency characteristics of a CT loop-filter are decided by element values and subject to process spread; also, they do not scale with the sampling frequency [9].

2.3 Simulation Methods and Tools

SPICE type transistor level simulation tools are widely used for the analysis of integrated circuits. The circuit is modeled at transistor level, and simulated with device models. This level of analysis provides circuit details, and allows investigation of various circuit imperfections and nonlinearities. However, excessive simulation time for SDM reaches the limits of these simulators [53].

2.3.1 Challenge

The difficulties associated with computer-aided analysis of SDMs are:

1. *Components with harsh nonlinearity –quantizers – exist in the feedback loop.*
   Direct frequency domain analysis is not possible. Transient analysis is the only choice.

2. *The circuit is a dual-time system with a rapidly varying clock and a slowly varying input signal.*
   The typical clock frequency is in the MHz range, while the input signal is in the kHz range. Transient analysis for thousands of clock cycles is needed just to observe a few cycles of the signal.

3. *Circuit performance is characterized by frequency components.*
   The performance is typically specified by the signal-to-noise ratio or dynamic range, which are based on statistical averages over a very large number of samples. Simulation results over several cycles of the input signal, usually tens of thousands of clock cycles, have to be obtained to evaluate the SNR for one particular input amplitude. Furthermore, the dynamic-range is estimated from the SNR versus input-amplitude curve, where many long transient simulations are needed.

4. *High simulation accuracy is required.*
   In order to observe the true circuit behavior, the numerical noise brought by the simulation algorithm and finite precision arithmetic has to be kept much lower than the actual circuit noise floor. Sigma-delta modulators with SNR in excess of 120 dB have been reported [54]. Such high simulation accuracy is hard to obtain with transistor level simulators. SPICE type general purpose analog simulators use classical numerical integration methods, and the accuracy is limited by the

local truncation error. The local truncation error can be reduced by decreasing the integration step, but the penalty is increased simulation time. There is a lower bound on the local truncation error. Beyond this limit, smaller time step will result in increasing error [55].

Simultaneous need of long and accurate transient simulation reaches the limit of a transistor level simulator, and often results in extremely long CPU time, which might be counted in days.

Efficient special purpose simulation methods for SDMs are needed, especially for use in the design cycle. They can be classified into three categories: block level, electrical circuit level, and transistor level. In this section, based on the above classifications, we give a review of the simulation methods and tools for SDMs. Other overviews on this subject can be found in [53, 56].

2.3.2 Classification and Review

Simulation methods for SDMs can be classified by the model abstraction level. Simple models usually lead to fast simulation; detailed models provide more realistic results. Trade-offs between simulation speed and model accuracy are often made in different stages during the design cycle.

Block Level Simulation for Conceptual Design Phase

In the conceptual design phase, the circuit architecture is determined according to high level specifications. The block level simulation is suitable at this stage. It does not require electrical details of the circuit which are not available at this stage, and provides fast simulation that enables architecture selection from a wide variety of circuit topologies.

The noise shaping and signal transfer functions for a SDM can be designed in the z-domain. This is the easiest and most widely used method. Difference equation simulation for z-domain transfer function is straightforward, and can be easily programmed with several lines of Matlab coding. But such codes are restricted to a specific circuit topology. Dedicated hand analysis is needed for each change of the topology, and a new set of codes has to be developed. This method lacks the flexibility for quick examination of several architectures.

General purpose block level simulation tools like *MIDAS(1992)* [15] are used. In this type of simulator, the circuit is represented by highly abstract function blocks, such as delay, adder, and quantizer. A simple signal-flow-chart type simulation is performed. The functional blocks in MIDAS are defined in model files, where circuit limitations may be added to the description. However, many circuit nonidealities, like frequency dependent characteristics, are difficult to model.

Simulation tools in this category are event driven. Digital simulation techniques like event tracing and scheduling are used. Typical elements are logic and delay functions. Electrical details of the circuit are avoided, and the circuit operation is characterized by highly abstract mathematical models. Simplicity in the circuit model enables fast simulation.

Additive noise sources can be added to the block level representation. Some general understanding of the noise performance can be obtained this way. However, thermal or other circuit noise analysis by this method could be prohibitively complicated, and the accuracy is not assured: Exhaustive hand-analysis is needed to calculate the noise power for each loop-filter; Caution must be paid to details such as how much wideband noise is aliased into the baseband; It is next to impossible to find a pseudo-random number sequence whose spectrum has the same shape as the filter noise response; Each change of the circuit requires a new hand-analysis and random noise source mapping process.

The clock jitter effect has been studied by some researchers at this level [57, 58]. Sampling of the input signal is considered as the only source of error, and a data sequence of the input sinusoid sampled at unequally spaced time instants is fed to the block level simulation. Again, although this approach can provide general insight during the conceptual design phase, it is not suitable for detailed circuit design or design verification. Additional comments will be given in chapter 5 and chapter 6.

In summary, the block level representation is highly abstract and mathematically oriented. No circuit implementation details are available. It is only suitable for conceptual design.

Electrical-Circuit Level Simulation for Circuit Design Phase

In the circuit design phase, electrical details are added to the circuit. Specific parameters, like gain-bandwidth of the operational amplifiers and capacitor values, are considered.

Most of the simulation tools for SDMs in this category evolved from those originally designed for SC filters. Additional digital functions like latched comparators and logic gates are included to accommodate the analysis of SDMs. Because of the nonlinear nature of the circuit, simulation is only performed in the time domain.

Switched-capacitor networks can be analyzed either in the charge-voltage (QV) regime or the current-voltage (IV) regime. Approaches in the first category are called ideal switched-capacitor methods. They simplify the analysis by eliminating current from the formulation. This is achieved by restricting the element types to capacitors, ideal switches (open/short circuits), voltage sources, voltage controlled voltage sources, and ideal or finite-gain operational amplifiers. The analysis proceeds by recursively solving a finite set of charge-transfer equations. Tools for analysis of SDMs in this category in-

clude *SWITCAP2(1990)* [11] and *TOSCA(1992)*[2] [16]. They are limited to discrete-time SDMs. Modulators with CT loop-filters cannot be handled.

Periodically switched-linear network analysis is necessary when some circuit nonidealities, like finite bandwidth of operational amplifiers and switch ON-resistances, cannot be neglected; or when elements like controlled current sources are critical to model the circuit. Methods in this category view the network as a linear circuit, and the formulation is done in the IV regime. All linear elements are allowed. Simulation tools in this category can be applied not only to SC but also to SI and CT circuits.

Transient analysis in the IV regime usually requires time integration. It is computationally expensive if ordinary numerical integration methods are involved, and can result in extremely long CPU time for dual-time circuits like SDMs and switched analog filters. Some strategies must be followed to speed up the simulation. In *SAMBA(1990)* [13], the nonlinearities are approximated by piecewise linear (PWL) models. The idea is that if a circuit is restricted to any particular segment of the PWL model, it can be solved as a linear circuit. The responses for these linear circuits are computed symbolically before the simulation starts. During transient analysis, the symbolic expressions are evaluated at the switching instants. This approach has the disadvantage that each combination of PWL segments must be solved separately, which leads to a large number of linear circuit approximations. In *AWEswit(1993)* [18], an IV formulation is adopted in addition to the conventional QV formulation. This means that while the SC parts are handled in the QV regime, the resistive portions are solved in some form of numerical integration. Asymptotic Waveform Evaluation (AWE) [59] is applied to approximate the transfer function by a low-order dominant pole model. The evaluation of this simplified model can be, depending on circuit size, significantly faster than the classical transient analysis. A sampled-data analysis technique [60] was applied in *DELTA(1994)* [61] and

[2]also has block level simulation capability.

SDSIM(1994) [19, 62] for fast and accurate simulation of SDMs. This method was improved and presented systematically in [19, 62]. Some constant matrices and vectors are computed numerically only once before the simulation starts. During transient analysis, the circuit response at discrete time instants is obtained by manipulation of the precomputed matrices and vectors. A review of this method, together with a summary of the sampled data analysis of analog circuits, is given in section 2.4.

Noise and clock jitter analysis of SDMs at the electrical circuit level are not available elsewhere. A comprehensive overview of noise analysis is given in section 3.3. Clock jitter, especially random jitter, destroys the regular pattern of the circuit operation. Special treatment, other than the conventional circuit analysis techniques, is needed. A state-of-the-art review of the clock jitter analysis of PSL network is given in chapter 5, and additional comments for SDMs are given in chapter 6.

Low Level Full Circuit Simulation for Design Verification

Although transistor level analysis allows investigation of many circuit nonidealities and nonlinearities, it is used only in the design verification phase. This is because (1) extremely long simulation time is required; (2) the transistor level circuit details are not available at earlier stages.

In *ZSIM(1988)* [63, 10], a clever *table look-up method* is adopted. Some important sub-circuits, such as integrators, are simulated for a single clock cycle under different operating conditions by an external transistor level simulator. The results are saved in look-up-tables. Then, with reference to the interpolated table points, a difference equation simulator is used to simulate the performance of the whole circuit. This approach is useful when the critical blocks have been implemented at transistor level, and quick design verification is needed. Nevertheless, this method has its limitations. The major

drawbacks are: (1) table generation is tedious and requires extensive human interaction and design experience. New tables have to be generated each time the circuit is modified; (2) simulation accuracy is limited by table interpolation error; (3) large memory is needed to store the tables; (4) noise and clock jitter effects cannot be analyzed.

The noise analysis algorithms implemented in SPICE type simulators are applicable only to circuits obtained by linearizing the original network around its DC operating point [64]. Due to the highly nonlinear nature of SDMs, neither thermal noise, nor clock jitter, nor dithering effects can be analyzed this way.

Additional time-domain noise sources might be added to the clocking signal to model clock jitter, and added throughout the circuit to model thermal noise and dithering noise. These noise sources can be included in SPICE transient simulation of SDMs. However, such an approach is hindered by the inherent limitations of the SPICE type transient analysis algorithm:

1. In typical versions of SPICE, the accuracy of transient analysis is of the order of 120 dB or less [65]. For a high resolution circuit like a SDM, the noise effects obtained from such a simulation algorithm are more likely to be *numerical noise*, not true circuit noise.

2. The inclusion of many noise sources in the transient analysis will result in excessive increase of the computational burden. It lengthens the already prohibitively long simulation time. Furthermore, in order to model the high frequency noise that might be aliased into the baseband, either a large number of sinusoidal noise sources with random phases [66] must be included, or very small steps [67] must be maintained throughout the analysis. Both cases make the situation even worse.

3. In time domain noise analysis, attention must be paid to the amount of noise power injected into the circuit. Noise power is related to the noise bandwidth in frequency

domain. In time domain, it is usually related to the step-size of transient analysis. In SPICE, this step-size is controlled internally. It is not known *a priori*, and makes time domain noise power modeling difficult.

In summary, transistor level simulation of SDMs is restricted to design verification. Noise and clock jitter analysis capabilities at this level are very limited.

2.3.3 Summary

The features of the simulation tools available for SDMs are summarized in Table 2.1. They are evaluated on the element abstraction level, the simulation accuracy and efficiency achieved, the computer memory needed, and the noise analysis capabilities. The goal of this research is listed in the column marked as *objective*.

	SPICE	**ZSIM**	**SWITCAP2**	**SAMBA**	**MIDAS**
year	1975	1988	1990	1990	1992
model accuracy	transistor	transistor block	ideal SC	PSLN	block
simulation acc	low	medium	high	high	high
efficiency	extremely slow	block(fast) table(slow)	fast	medium	fast
memory needed	large	large	medium	large	small
thermal noise	×	×	×	×	general
clock jitter	×	×	×	×	noise
dithering effect	×	×	×	×	effects

	TOSCA	**AWEswit**	**SDSIM / DELTA**	*objective*
year	1992	1993	1994	
model accuracy	block, ideal SC	PSLN	PSLN	PSLN
simulation acc	high	medium	high	high
efficiency	fast	medium	fast	fast
memory needed	medium	medium	medium	medium
thermal noise	general	×	×	√
clock jitter	noise	×	×	√
dithering effect	effects	×	×	√

Table 2.1: Simulators for Sigma-delta Modulators

2.4 Sampled Data Analysis of Analog Circuits

Sampled-data analysis can simultaneously maintain the accuracy and efficiency of simulation. In this thesis, new sampled-data methods for noise and clock jitter analysis are developed. A brief review of the background is provided in this section.

Given a linear time invariant network, the state variable vector $\mathbf{x}(t)$, its initial state $\mathbf{x}_0$ and the input $u(t)$ for $t \geq t_0$, we wish to find the output $\mathbf{y}(t)$ for $t \geq t_0$. The State Space equations can be formulated as:

$$\begin{aligned} \dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t) + \mathbf{B}u(t), \quad \mathbf{x}(t_0) = \mathbf{x}_0 \\ \mathbf{y}(t) &= \mathbf{C}\mathbf{x}(t) + \mathbf{D}u(t) \end{aligned} \tag{2.5}$$

where $\mathbf{A}, \mathbf{B}, \mathbf{C}, \mathbf{D}$ are constant coefficient matrices.

The time-domain solution [68] of the State Space equation (2.5) is:

$$\mathbf{x}(t) = e^{\mathbf{A}(t-t_0)}\mathbf{x}(t_0) + e^{\mathbf{A}t}\int_{t_0}^{t} e^{-\mathbf{A}\tau}\mathbf{B}u(\tau)d\tau \tag{2.6}$$

where the first term corresponds to the *natural response* or the *zero-input response*, and the second term corresponds to the *forced response* or the *zero-state response*. The matrix exponential $e^{\mathbf{A}t}$ is defined as an infinite series:

$$e^{\mathbf{A}t} = \mathbf{I} + \mathbf{A}t + \frac{1}{2!}(\mathbf{A}t)^2 + \cdots + \frac{1}{k!}(\mathbf{A}t)^k + \cdots . \tag{2.7}$$

The output $y(t)$ can be obtained by straightforward algebraic operations once the solution for $x(t)$ is known.

Chua and Lin [68] considered the time-domain sampled-data analysis of the state equation (2.5). Both $\mathbf{x}(t)$ and $\mathbf{y}(t)$ were determined only for some discrete values of t, for example,

$$t = t_0, t_0 + T, t_0 + 2T, \cdots, t_0 + kT, \cdots \tag{2.8}$$

where k is an integer and T is a suitably chosen time interval. The input $u(kT)$ is assumed to be known for all k, and an equation that relates $\mathbf{x}(kT+T)$ to $\mathbf{x}(kT)$ and $u(kT)$ is looked for. Once this difference equation is obtained, $\mathbf{x}(kT)$ can be calculated successively for all k, which is a special form of numerical integration. Let $t_0 = kT$ and $t = kT + T$, equation (2.6) can be written as

$$\mathbf{x}(kT+T) = e^{\mathbf{A}(T)}\mathbf{x}(kT) + e^{\mathbf{A}(kT+T)} \int_{kT}^{kT+T} e^{-\mathbf{A}\tau}\mathbf{B}u(\tau)d\tau \qquad (2.9)$$

Equation (2.9) was transferred into exact difference equation formula for two special input cases, namely, piecewise constant inputs and continuous piecewise linear inputs. For general continuous-time inputs, the forcing function $u(t)$ was approximated by piecewise-constant or piecewise-linear waveforms, and (2.9) was transferred into approximate difference equations.

Sampled data analysis of analog circuits, or analysis of analog circuits by difference equations, reveals the circuit behavior with full analog details at discrete instants of time. The associated computational cost is a cheap difference equation simulation. The usefulness of the approach by Chua and Lin is limited, however, due to the fact that

1. It is based on State-Space formulation, where the *state transition matrix*, $e^{\mathbf{A}T}$, is computed, and the simulation is carried out by solving state-variables in a successive fashion. Although useful in theoretical studies, the State-Space formulation is no longer used in computer applications [55]. Approaches based on formulation methods widely used in modern computer-aided analysis tools, such as Modified Nodal Analysis (MNA), are preferred.

2. The *state transition matrix* is approximated by a finite number of terms of the infinite series expansion in (2.7). A large number of terms is needed to avoid the numerical instability problem [68].

3. The representation of the integral by difference equation is exact only for piece-wise constant or piece-wise linear inputs. For other common inputs like sinusoids, it is obtained by approximation. This not only complicates the computer code, but also results in significant errors, especially when simulated over a large number of time points.

Opal [19] recognized that for a complex exponential input

$$u(t) = e^{st}, \quad t \geq t_0, \tag{2.10}$$

the integral part of (2.6) corresponding to the zero-state response can be written in closed form as

$$\begin{aligned} \mathbf{x}_{ZS}(t) &= e^{\mathbf{A}t} \int_{t_0}^{t} e^{-\mathbf{A}\tau} \mathbf{B} u(\tau) d\tau \\ &= e^{st_0} (s\mathbf{I} - \mathbf{A})^{-1} [e^{s(t-t_0)}\mathbf{I} - e^{\mathbf{A}(t-t_0)}]\mathbf{B}. \end{aligned} \tag{2.11}$$

Define a constant matrix $\mathbf{M}$ and a constant vector $\mathbf{P}$ as:

$$\begin{aligned} \mathbf{M} &= e^{\mathbf{A}T}, \\ \mathbf{P} &= (s\mathbf{I} - \mathbf{A})^{-1} [e^{sT}\mathbf{I} - e^{\mathbf{A}T}]\mathbf{B}. \end{aligned} \tag{2.12}$$

With $t_0 = 0$, formula (2.9) can be written as a difference equation:

$$\begin{aligned} \mathbf{x}(T) &= \mathbf{M}\mathbf{x}_0 + \mathbf{P}, \\ \mathbf{x}(nT + T) &= \mathbf{M}\mathbf{x}(nT) + \mathbf{P}e^{snT}. \end{aligned} \tag{2.13}$$

Multiple complex exponential inputs can be included by applying the superposition rule for linear circuits

$$\mathbf{x}(nT + T) = \mathbf{M}\mathbf{x}(nT) + \sum_{i=1}^{k} \mathbf{P}_i e^{s_i nT}, \tag{2.14}$$

where k is the number of inputs. The benefit of considering complex exponential inputs is obvious. It enables the *exact* expression of the circuit response for a wide variety of common input functions. Sinusoidal inputs are included by setting $s = j\omega$, and in the case of $u(t) = \cos(\omega t)$, equation (2.13) is modified to:

$$\mathbf{x}(nT+T) = \mathbf{M}\mathbf{x}(nT) + Re(\mathbf{P}e^{j\omega nT}), \tag{2.15}$$

where $Re(.)$ denotes the real part of a complex argument. For input $u(t) = \sin(\omega t)$, the imaginary part is used instead. Step inputs are included by setting $\omega = 0$ in equation (2.15), and the introduction of additional input functions is discussed in [19].

The MNA equations for a LTI circuit are [55]

$$\mathbf{G}\mathbf{v}(t) + \mathbf{C}\frac{d\mathbf{v}(t)}{dt} = \mathbf{d}u(t), \quad \mathbf{v}(0) = \mathbf{v}_0 \tag{2.16}$$

where all conductances and constants arising in the formulation are stored in the matrix $\mathbf{G}$, all capacitor and inductor values are stored in the matrix $\mathbf{C}$, the connection of the input source to the circuit is in $\mathbf{d}$, $\mathbf{v}(t)$ is the vector of node voltages and some branch currents needed for MNA, and $\mathbf{v}_0$ is the initial condition vector.

The derivations of the matrix M and vector P in MNA are given in [62], together with the numerical computation algorithms. It provides a solid foundation for the utility of this sampled-data method in computer applications. The matrix M and vector P are defined as

$$\begin{aligned} \mathbf{M} &= \mathcal{L}^{-1}[(\mathbf{G}+p\mathbf{C})^{-1}]\Big|_{t=T}\mathbf{C}, \\ \mathbf{P} &= \mathcal{L}^{-1}[(\mathbf{G}+p\mathbf{C})^{-1}\mathbf{d}U(p)]\Big|_{t=T}, \end{aligned} \tag{2.17}$$

where p is the Laplace complex parameter, and $\mathcal{L}^{-1}(.)$ denotes the inverse-Laplace transform. For an input given by (2.10), the solution of (2.16) at $t = nT$ can be written in a similar way to (2.13):

$$\mathbf{v}(nT+T) = \mathbf{M}\mathbf{v}(nT) + \mathbf{P}e^{snT}. \tag{2.18}$$

This method is efficient. For a given time interval, a constant matrix M and a constant vector P are computed only once. The computational cost associated with each point during simulation is in the order of $O(m^2)$, where m is the size of the system matrix. It is also accurate. Since the constant matrices are computed only once, extra effort can be spent on computing them as accurately as necessary. Because a stable system will damp out any numerical errors [19], the error introduced by finite precision arithmetic will not increase with the increase of simulation time. Besides the transient analysis of LTI circuits at fixed discrete instants of time, this method is also applicable to PSL networks and SDMs [19, 62].

2.5 A Numerical Laplace Transform Inversion Method

In this section, we review a numerical Laplace Transform inversion method [69, 70, 71]. It can be used for time domain solution of LTI networks, and is equivalent to numerical integration of differential equations. Because this method can provide accurate results and can handle discontinuous functions like Dirac impulses, it was chosen as the integration method for the differential equations formulated in this thesis. In particular, it was used for the computation of the time derivatives of the transition matrix and of the input transfer vector.

The method is based on numerical evaluation of the Laplace transform inversion integral

$$v(t) = \frac{1}{2\pi j} \int_{c-j\infty}^{c+j\infty} V(s) e^{st} ds \tag{2.19}$$

where s is the complex frequency and $V(s)$ is the Laplace transform. Exact inversion is possible only if the poles of $V(s)$ are known, and some approximations are necessary to avoid root-finding procedures. The change of variables $z = st$ was introduced, and

equation (2.19) becomes

$$v(t) = \frac{1}{2\pi jt} \int_{c'-j\infty}^{c'+j\infty} V(z/t)e^z dz. \tag{2.20}$$

Next, e^z was approximated by a Padé rational function

$$R_{N,M} = \frac{\sum_{i=0}^{N}(M+N-i)!\binom{N}{i}z^i}{\sum_{i=0}^{M}(-1)^i(M+N-i)!\binom{M}{i}z^i}. \tag{2.21}$$

The approximation $\hat{v}(t)$ to $v(t)$ becomes

$$\hat{v}(t) = \frac{1}{2\pi jt} \int_{c'-j\infty}^{c'+j\infty} V(z/t)R_{N,M}(z)dz. \tag{2.22}$$

Parameters M and N must be chosen so that the function $V(z/t)R_{N,M}(z)$ has at least two more finite poles than zeros. For $N < M$,

$$R_{N,M}(z) = \sum_{i=1}^{M} \frac{K_i}{z - z_i} \tag{2.23}$$

where z_i are the poles and K_i are the residues of $R_{N,M}$. They were computed with high precision and recorded in tables. The integral in (2.22) can be calculated by residue calculus as

$$\hat{v}(t) = -\frac{1}{t}\sum_{i=1}^{M} K_i V(z_i/t). \tag{2.24}$$

For a given function $V(s)$, its time domain waveform is computed numerically from (2.24). Real-time functions can be evaluated using only the poles in the upper half plane, and the computational cost is reduced by one-half.

The formula (2.24) is exact for time domain functions that are polynomials of t of order upto $M + N$. For general functions, it exactly inverts the first $M + N + 1$ terms of the Taylor series expansion. Due to the division by t in (2.24), this method cannot be used for $t = 0$, but discontinuous functions like unit-step and Dirac impulses at time zero do not cause any problem.

The inversion by (2.24) is very accurate for small values of t, but error grows with time. In order to preserve accuracy, a stepping algorithm is used to reset the time origin after each step. The resetting is easy to apply for lumped linear networks, and is equivalent to numerical integration of differential equations. The order of integration can be changed between 1 and 46 without any difficulty. It is a very high order and absolutely stable integration method. Compared with ordinary integration methods, an additional advantage is: it can correctly handle discontinuous functions, and can be used across the switching instants. The disadvantages are: (1) It is based on the Laplace transform formula, and loses its advantages if the functions are nonlinear; (2) It is based on complex number arithmetic, and requires network solution at multiple frequencies for each integration step. The per step computational cost is usually larger than ordinary integration methods.

The time domain derivatives of the network function can also be evaluated. They are based on the property of Laplace transform

$$\mathcal{L}[v^{(n)}(t)] = s^n V(s) - \sum_{k=1}^{n} v^{(k-1)}(0^-) s^{n-k}. \tag{2.25}$$

Select N and M so that $(z/t)^n V(z/t) R_{N,M}(z)$ has at least two more finite poles than zeros. Then all terms after the summation in (2.25) do not contribute to the inversion, and the formula for the n-th derivative of $v(t)$ is obtained as

$$\hat{v}^n(t) = -\frac{1}{t} \sum_{i=1}^{M} K_i (z_i/t)^n V(z_i/t), \quad t > 0. \tag{2.26}$$

The derivative can be computed with little extra effort, as most of the time is spent on the evaluation of $V(z_i/t)$.

Chapter 3

Noise Analysis

Although during the design cycle of SDMs, information on the circuit thermal noise performance is very useful [3, 4], general noise analysis methods for SDMs are still not available.

This chapter presents a new time domain noise analysis method at electrical circuit level. It can be applied to thermal noise analysis of SDMs, and is useful for PSL networks, where frequency domain noise analysis cannot be done easily.

The theories were implemented in a computer program. Numerical examples are given and, where possible, comparisons with exact analysis or physical measurements are made. Primitive results of this chapter were reported in [72, 73].

3.1 Introduction

Electrical noise is usually small in comparison to other signals and may be ignored. However, given the present trend towards low voltage and low power designs, it can become significant and limit the circuit performance in a fundamental way. Accurate

prediction of noise at the output of a circuit becomes necessary to evaluate performance measures like SNR and DR. This is especially true for high resolution circuits like SDMs.

In traditional SPICE type simulators, noise simulation is available in frequency domain. However, frequency domain noise analysis of SDMs is not possible. General methods for simulation of SDMs have been presented by many researchers [63, 10, 65, 14, 11, 16, 18, 61, 19], but nobody has given a method for noise analysis of SDMs at electrical circuit level. Their noise performance remains unknown until physical measurements are made on the manufactured samples.

In this chapter, we present algorithms for *time domain* noise analysis of SDMs. In addition, the algorithms can be applied to periodically switched linear networks, such as SC and SI filters, where frequency domain analysis is complicated. The method computes the complete transient response to noise and other desired signals in a sampled data manner. It simultaneously addresses the issues of accuracy and efficiency. A brief introduction to circuit noise sources in integrated circuits is given in section 3.2. Noise analysis methods for LTI circuits, PSL networks, and nonlinear circuits are reviewed in section 3.3. The new method is presented in section 3.4, and numerical results for the noise analysis of a few circuits are given in section 3.5.

3.2 Circuit Noise Sources and Models

Electrical noise is random fluctuations in currents and voltages due to the discrete nature of electronic charge. These fluctuations are called thermal, shot, or flicker noise, based on the physical mechanism that produces them [74]. In this section, we give a brief review of circuit noise sources and their modeling techniques.

Thermal noise arises from random thermal motion of free electrons in a conducting medium. The net effect of the thermal motion of all electrons constitutes a noise current flowing through the conductor with random directions and zero mean value. Thermal noise spectrum is flat up to 6000 GHz [75], which is much higher than the bandwidth of most circuits. For practical purposes, thermal noise is considered *white* and contains all frequencies in equal amount. For a conductance of value G, the power spectrum density of the thermal noise current is given as

$$S(f) = 4kTG \quad \text{A}^2/\text{Hz}, \quad f \geq 0 \tag{3.1}$$

Frequency domain representation of thermal noise consists of a constant PSD $S(f) = \eta$ versus frequency. It is shown in Fig. 3.1.

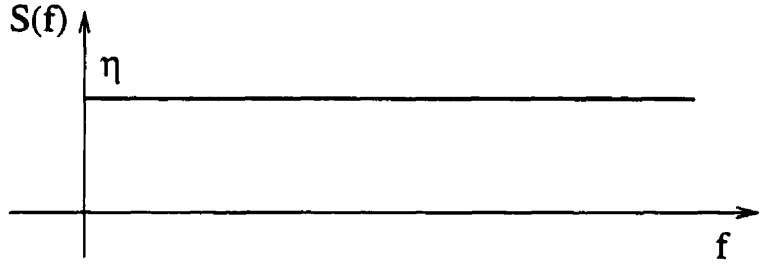


Figure 3.1: Power spectrum density for thermal noise

A noisy resistor can be modeled, either by its Norton equivalent as a noiseless resistor in parallel with a current noise source with power $4kTG\Delta f$, where Δf is the noise bandwidth of interest, or by its Thevenin equivalent as a voltage source in series with the noiseless resistor, as shown in Fig. 3.2.

Shot noise is always associated with direct-current flow. Its power spectrum is [76]

$$S(f) = 2qI_D \quad \text{A}^2/\text{Hz}, \quad f \geq 0 \tag{3.2}$$

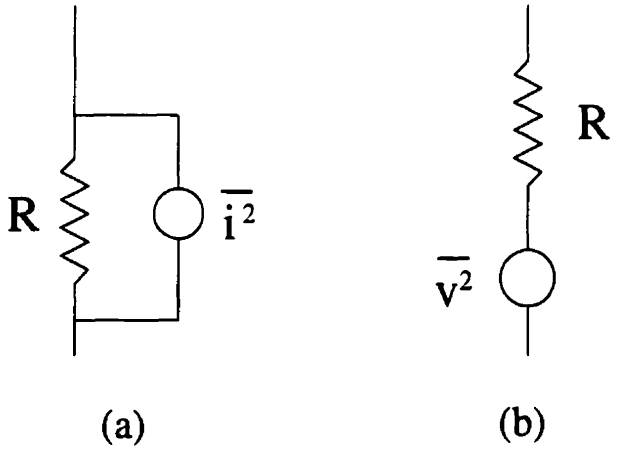


Figure 3.2: Resistor thermal noise model

where q is the electronic charge, and I_D is the average forward-bias current. Equation (3.2) holds up to gigahertz frequency range.

Flicker noise, also known as $1/f$ noise, exists in active devices and some discrete passive elements like carbon resistors. In bipolar transistors, it arises from the random capture and release of charge carriers by traps associated with contamination and crystal defects. Flicker noise is always associated with direct current flow. Its power spectrum is [76]

$$S(f) = K_1 \frac{I^a}{f^b} \quad \text{A}^2/\text{Hz}, \quad f \geq 0 \tag{3.3}$$

where I is the direct current in Amperes, f is frequency in Hertz, K_1 is a device dependent constant, and a, b are constants used in modeling.

Noise in a MOSFET switch is dominated by the thermal noise associated with its channel ON-resistance, while the noise generated in the OFF state is usually neglected [25]. A common model for a MOSFET switch is shown in Fig. 3.3, as an ideal switch in series with a noisy resistor. An operational amplifier is a complex functional block with a large

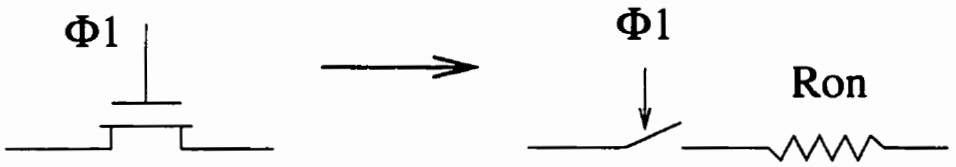


Figure 3.3: Switch thermal noise model

number of noise sources. Its noise behavior is usually characterized by lumped equivalent noise current and noise voltage sources at the input [76], as shown in Fig. 3.4(A). The input noise currents of modern opamps are very small, and are usually neglected [25]. A widely used thermal noise model for opamps is shown in Fig. 3.4(B), where R_{eq} is the equivalent thermal noise resistance.

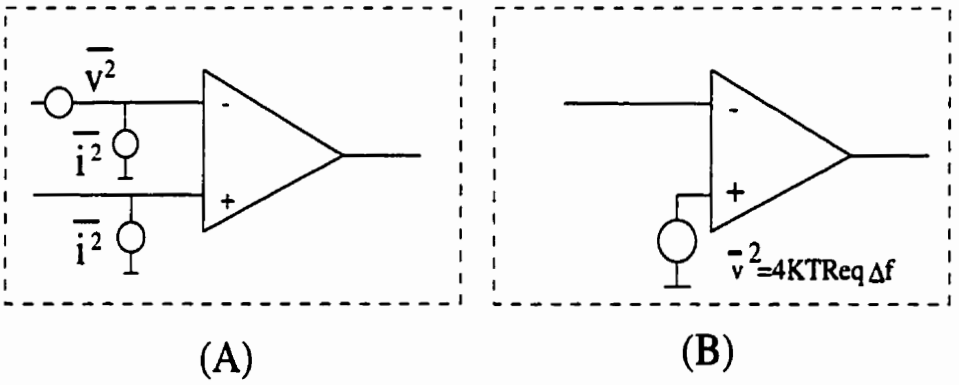


Figure 3.4: Opamp thermal noise model

3.3 Noise Analysis Methods: Review

Noise analysis of electrical circuits is performed either in time or frequency domain. Electrical circuits are generally classified as linear circuits, where frequency domain analysis methods are used, or as nonlinear circuits, where time domain analysis methods

are used. In the following, the noise analysis methods based on these classifications are reviewed.

3.3.1 Linear Circuits and Frequency Domain Noise Analysis

In frequency domain noise analysis, the PSD of the noise source is given and the circuit is generally restricted to be lumped, linear and time-invariant (LLTI). If the circuit is nonlinear, it is assumed to have a fixed bias and can be linearized around the DC operating point. Noise analysis is done on the linear small signal model. For LLTI circuits the noise power at the output, $S_o(f)$, is related to the input noise power, $S^i(f)$, by the frequency domain transfer function from the noise source to the output, $H(f)$, by the relation

$$S_o(f) = |H(f)|^2 S^i(f) \tag{3.4}$$

Typically, there are many uncorrelated noise sources, and it is necessary to compute the transfer function from each noise source to the output at each frequency of interest. The total noise at the output is then

$$S_o(f) = \sum_{n=1}^{N} |H_n(f)|^2 S_n^i(f) \tag{3.5}$$

where $H_n(f)$ is the transfer function from the n-th noise source $S_n^i(f)$ to the output, and N is the total number of noise sources in the circuit. If we are interested in the noise power at only one output, then the computational cost can be reduced by using the adjoint network concept [20, 77]. Noise analysis of LLTI circuits in frequency domain is well established and is available in most SPICE-like analog simulators.

Closely related to LLTI circuits are PSL networks, which are lumped linear circuits with periodically operated switches. Direct frequency analysis of these circuits is possible [78, 79, 80]. As in the case of LLTI circuits, the noise analysis is done in the

frequency domain and requires calculation of frequency transfer functions. The use of the adjoint network concept [20, 77] can reduce the computational cost in case of many uncorrelated noise sources.

Noise analysis of PSL circuits is complicated by another factor. Frequency domain representation of electronic noise is generally wide-band and typically extends well into the GHz range [81]. Due to the switching nature of these circuits, the high frequency noise is aliased, or folded, into the lower frequency bands [21], as illustrated in Fig. 3.5. It becomes necessary to compute the aliasing transfer functions for each noise source.

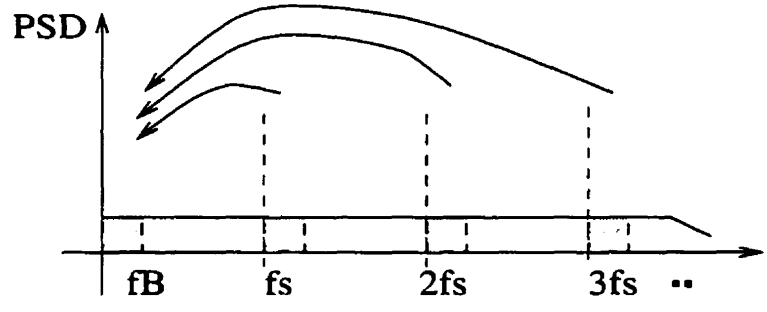


Figure 3.5: Aliasing into baseband

The total noise power at the output due to the aliased components becomes

$$S_o(f) = \sum_{m=-\infty}^{\infty} \sum_{n=1}^{N} |H_n^m(f)|^2 S_n^i(f + mf_s) \tag{3.6}$$

where the first summation over m takes into account the effect of aliased frequency components, f_s is the clock frequency and $H_n^m(f)$ is the transfer function from the input at frequency $(f + mf_s)$ to the aliased output at frequency f. The cost increases due to the need to compute additional, possibly a large number of, aliasing transfer functions.

3.3.2 Nonlinear Circuits and Time Domain Noise Analysis

Time domain noise analysis becomes necessary either for nonlinear circuits, where the small signal model is not acceptable, or for time varying circuits where direct frequency domain analysis is not straightforward. Two distinct approaches have been used for time-domain noise simulation. One method employs a random number generator to provide a time-domain waveform that approximates noise. The other is based on the solution of stochastic differential equations. Both methods will be reviewed in the following.

The basic idea of the first method is to generate a time domain waveform that mimics the underlying physical process and causes random fluctuation in voltages and currents. One approach is described in [66], where each noise source is represented by a sum of a fixed number of sinusoids with random phases. The frequencies of these sinusoids are distributed in the desired frequency-band, and the magnitude of each sinusoid is proportional to the noise power in that frequency slot. Many simulation runs are carried out by a classical transient analysis algorithm, and statistical averages of the noise power at each time step are computed [66]. Very high frequency sinusoids have to be included to approximate white noise sources. This is especially important in switched circuits. When the desired frequency-band is wide, the noise representation may have poor spectrum resolution. Additional frequency components can be included to improve the resolution, but with the penalty of increased computational cost.

Another way to generate a noise waveform was described in [67]. The noise source is modeled as a random amplitude pulse waveform. It consists of pulses of width h with the amplitude of each pulse given by a Gaussian random number generator, as shown in Fig. 3.6. The variance of the Gaussian random number generator controls the power level, and the width of each pulse is inversely proportional to the maximum frequency up to which we want to model the noise spectrum [67].

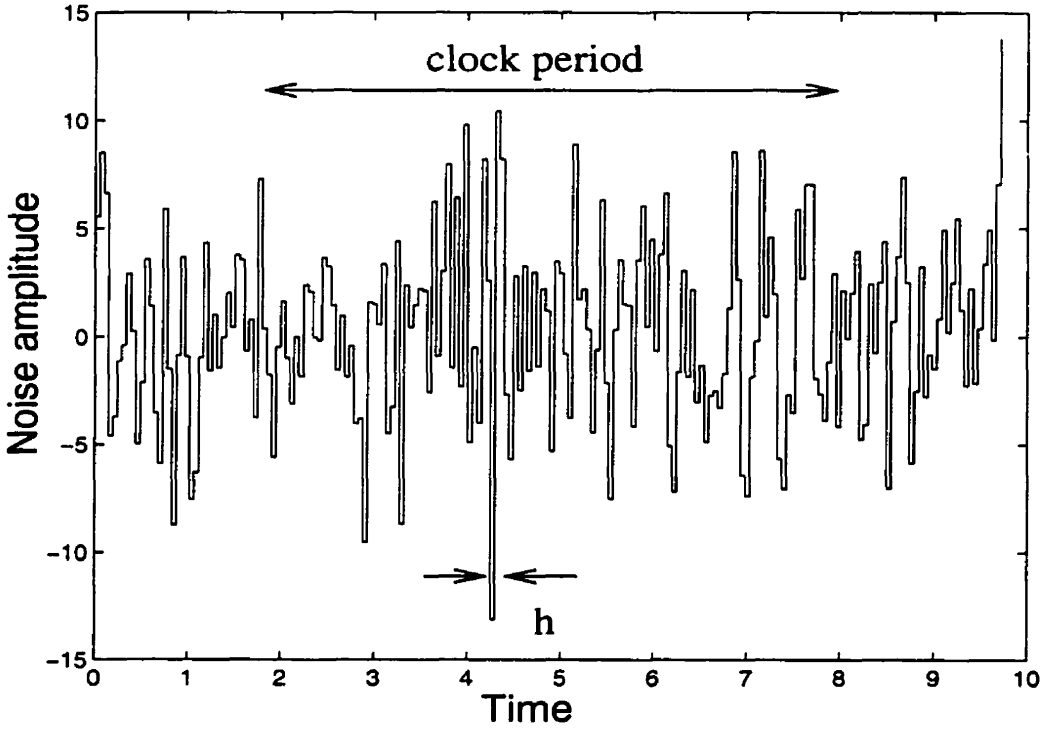


Figure 3.6: Random noise waveform

Since superposition does not apply, all noise sources and signals must be applied simultaneously. Transient analysis is performed to compute the complete response of the circuit. Typically, this is followed by a Fast Fourier Transform (FFT) to estimate the frequency spectrum at the output of the circuit and to calculate performance measures, such as SNR.

The second method for time domain noise analysis [26, 108] is based on the solution of stochastic differential equations. It assumes that the noise power level is much smaller than the signal power level, and the state of the nonlinear circuit is decided exclusively by the signal contents. The circuit is linearized at each time step using the first two terms of the Taylor series expansion, and the noise variance is computed on this linearized circuit.

This method requires the solution of very large systems of equations at each time step to compute the noise results.

Another closely related method assumes the noise to be much smaller than the primary signal, and linearizes the nonlinear equations using Backward Differentiation Formulae (BDF). The network obtained is linear periodically time varying (LPTV). The noise is applied to the LPTV circuit and the output is calculated by means of time varying transfer functions [82].

The approach based on circuit linearization at each time step is not suitable for sigma-delta modulators, where the state of the quantizer output is not decided exclusively by the large deterministic signal. At some time points, the noise power may be comparable in magnitude to the signal power and change the quantizer output. Also, due to its highly nonlinear nature, the circuit cannot be represented by an equivalent small signal model.

3.4 New Time Domain Noise Analysis Method

In this section we present algorithms for the time domain noise analysis of LLTI circuits. It can also be applied to circuits that contain mainly linear elements and some time varying or nonlinear elements, such as clocked switches and single or multi-bit quantizers. This extends the application of the algorithms to SC and SI circuits, and to SDMs. Both SC, SI, and CT SDMs can be analyzed. The time domain noise waveforms are generated with a desired noise amplitude and a flat spectrum over a limited range of frequencies. We present a sampled data noise analysis method that computes the complete response to noise and signals in one step. There are no restrictions on the relative power levels between the deterministic and noise signals, which is an advantage over the methods given in [26, 82].

3.4.1 Time Domain Thermal Noise Model

A time domain waveform with a given PSD in the frequency domain has to be generated to represent noise. An exact time domain representation of white noise is not possible. However, a reasonable approximation that gives correct results can be generated. One method is to generate a series of pulses of width h seconds with the amplitudes given by a Gaussian random number generator [67], as shown in Fig. 3.6. A study is given in [67] to show this approximation is reasonable for modeling thermal noise. The maximum frequency up to which the noise model is correct can be controlled by reducing the width of the pulse. The power spectral density is controlled by the variance σ^2 of the random number generator, and is given by

$$\sigma^2 = \frac{\eta}{h} \tag{3.7}$$

where η is the noise power level, as shown in Fig. 3.1. Setting the power level to $\eta = 0.2$, $h = 0.001$ and taking $N = 256$ samples of the time domain noise waveform, the Fast Fourier Transform (FFT) is shown in Fig. 3.7(A). The power in the waveform is 175.5 W, which compares approximately with the expected power of 200 W given by (3.7). Note that the waveform is not smooth, does not represent a uniform PSD as needed for a white noise spectrum, and has a variance of 0.58. Averaging the FFT over 10 sets of data gives a smoother curve, as shown in Fig. 3.7(B), with the variance reduced by a factor of 10 to 0.058, and the averaged power is 192.5 W. This averaging of the noise spectrum leads to smoother curves but increases the execution time of noise analysis. In most cases we integrate the noise power over a frequency band and, in this case, multiple simulations to perform smoothing are generally not needed. Another method to smoothen data and which does not require multiple simulation runs is to use a moving window to compute a weighted average of neighboring points. In our work we have used a Hann window of length 61 for data smoothing of FFT spectra of length 64k samples.

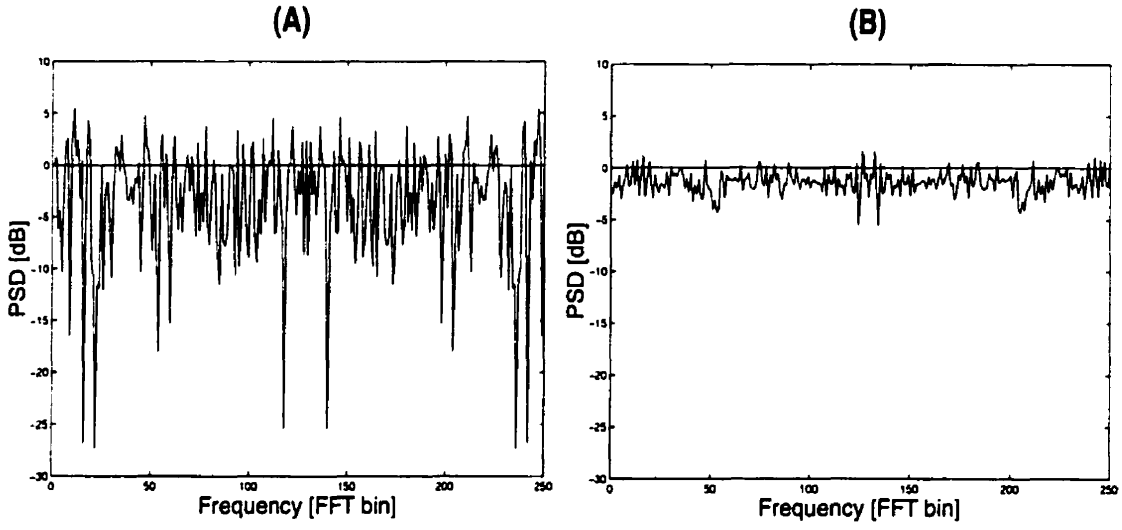


Figure 3.7: PSD of a noise waveform (A) 256 samples (B) 10 sets of 256 samples

In time domain analysis, all noise sources are modeled in the manner discussed above. In each time slot of width h, the $i-$th source is modeled as a pulse of amplitude u_i given by

$$u_i = \sigma_i N(0,1) \tag{3.8}$$

where the power level σ_i is obtained from (3.7), and $N(0,1)$ is a normally distributed random number generator with zero mean and standard deviation of unity. Since all sources are uncorrelated, a new random value is used for each source in each time slot. Unlike the frequency domain analysis, all noise sources, including the primary input signal, are applied to the circuit simultaneously, and the complete transient response is calculated. The adjoint network concept is not needed.

Pseudo random number generators have a finite period. For reliable simulation, it is necessary to make the period much longer than that needed in the simulation. If we consider typical values of a clock frequency of 10 MHz, simulation of 100,000 clock cycles, 100 uncorrelated noise sources in the circuit, and a noise bandwidth of 1 GHz,

then approximately 10^{10} random numbers are needed for simulation. This does not pose a problem for modern random number generators, where periods of the order of 10^{50} or more can be easily obtained [83].

3.4.2 Noise Simulation Method

Time domain noise analysis of SDMs demands a transient algorithm that simultaneously addresses the issues of efficiency and accuracy. Efficiency is needed because of the large number of time points required for noise analysis. Accuracy is needed to detect the effect of a small noise waveform in the presence of large signals.

The sampled data analysis algorithm given in [19, 62], as reviewed in section 2.4, is an efficient and accurate method for transient analysis of LLTI circuits. For input $u(t) = e^{st}$, $t \geq t_0$, this algorithm calculates the network response at fixed and equally spaced time instants of $t = nT$, as given in (2.18):

$$\mathbf{v}(nT+T) \;=\; \mathbf{M}\mathbf{v}(nT) + \mathbf{P}e^{snT}.$$

The fixed-time interval T can be chosen arbitrarily and does not depend on the circuit time constants. The only operations needed during simulation are one matrix-vector multiplication and one vector addition. This algorithm can also be applied to PSL networks and SDMs. It is chosen as the simulation engine for the proposed noise analysis method.

Thermal noise is modeled by a waveform similar to Fig. 3.6, and is treated as a step source in each time slot of width h. Equation (2.18) is modified to accommodate additional noise sources

$$\mathbf{v}(nh+h) \;=\; \mathbf{M}(h)\mathbf{v}(nh) + \sum_{i=1}^{K_1} \mathbf{P}_{s_i}(h)e^{s_i nh} + \sum_{j=1}^{K_2} \mathbf{P}_{n_j}(h)u_j(nh) \qquad (3.9)$$

where $\mathbf{P}_{n_j}$ is the zero-state unit-step response due to the j-th noise source, u_j is the amplitude of the noise source in that time slot given by (3.8), $\mathbf{P}_{s_i}$ is the zero-state response

due to the i-th signal $e^{s_i t}$, and K_2 and K_1 are the total number of noise and signal sources in the circuit. The simulation step-size is set as the width of the noise pulse h.

Periodically switched linear networks change topologies at switching instants only. Within each phase, the network is lumped, linear and time invariant. The time domain noise analysis proposed in (3.9) can be applied. One set of constant matrix and vectors is computed for each phase, and stored before the simulation starts. During simulation, the complete response to deterministic and noise signals is calculated successively by (3.9), and sets the initial condition for the following phase. Simulation proceeds by repeating the process.

Often, only the solution at the end of each phase of a PSL network is of interest. The step-size of the time-domain noise analysis is limited by the pulse width of the random noise waveform. It is usually much smaller than the phase duration, due to the need to model the noise power at high frequencies that might be aliased into the baseband. Nevertheless, because the circuit is linear and time invariant within each phase, the noise analysis can be speeded up by using different step-sizes to compute the noise and the signal response. The step-size for analysis of the signal is set to be the phase duration. While the noise analysis step-size is set to be a fraction of the phase duration. It is given by the number of sidebands that the user is concerned for noise fold-over effects. Equation (3.9) is modified to

$$\mathbf{w}(nT + kh + h) = \mathbf{M}(h)\mathbf{w}(nT + kh) + \sum_{j=1}^{K_2} \mathbf{P}_{n_j}(h) u_j(nT + kh) \quad (3.10a)$$

$$\mathbf{v}(nT + T) = \mathbf{M}(T)\mathbf{v}(nT) + \sum_{i=1}^{K_1} \mathbf{P}_{s_i}(T) e^{s_i nT} + \mathbf{w}(nT + T) \quad (3.10b)$$

where vector $\mathbf{w}$ saves the zero-state noise response. It is re-set to zero at the beginning of each phase at nT, and is computed successively through many small steps of h, until the end of the phase at $nT + T$. The complete response at $nT + T$ is formed as the

summation of $\mathbf{w}(nT + T)$, the zero-state signal response, and the zero-input response. The circuit performance in the frequency domain is obtained by FFT on the time domain data. In this method, the matrices $\mathbf{M}(h)$, $\mathbf{M}(T)$, and vectors $\mathbf{P}_{n_j}(h)$, $\mathbf{P}_{s_i}(T)$ are constant for given step-sizes of h and T, and are computed only once before simulation starts.

A SDM can be partitioned into a nonlinear block – the quantizer, which updates its outputs at external clock edges only, and a linear block – the rest of the circuit. Between clock edges, the output to the linear block can be computed with feedbacks from the latched quantizers treated as step inputs [19]. Noise analysis of a SDM proceeds by computing the output of the linear block at the clock edges based on equation (3.10), updating the quantizer outputs, and repeating the process for next clock cycle.

3.5 Numerical Examples

The method has been applied to thermal noise analysis, and implemented in a computer program, SIMthermal. In this section, we give the simulation results for a few circuits to show the usefulness of the method. Where possible, our results are compared with previously published results or measurements. All CPU execution times are given for a Sun Sparc 20/71 workstation. All frequency spectrums are obtained by FFT on 64k time-domain simulation data. The prefix 'k' is used to represent $2^{10} = 1024$ data points.

3.5.1 Simulation Accuracy: A Simple RC Circuit

The simulation accuracy of SIMthermal is illustrated on a simple RC circuit shown in Fig. 3.8. The input to the circuit is a mixture of sinusoids of 1-volt peak-voltage, and

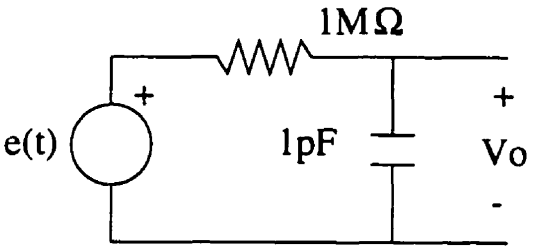


Figure 3.8: A RC circuit

with 10 kHz, 1 MHz, 2 MHz, 3 MHz, 4 MHz frequencies

$$e(t) = \sum_{i=1}^{5} \sin(2\pi f_i t) \text{ V} \tag{3.11}$$

Frequency [Hz]	Simulated [V]	Exact [V]	Absolute Error [V]
10 k	0.49901595225213	0.49901595225182	3.0642155479654E-13
1 M	0.07858836273894	0.07858836273879	1.4765966227515E-13
2 M	0.03966334842189	0.03966334842183	0.6518396933330E-13
3 M	0.02648857429385	0.02648857429390	0.4671610320806E-13
4 M	0.01987863874078	0.01987863874060	1.7697995846611E-13

Table 3.1: Magnitudes at Fundamental Frequencies (Bilateral)

The transient response is computed until the steady-state is reached and FFT is performed on a section of the transient waveform. The FFT plot in Fig. 3.9(A) shows that the simulation noise floor is 220 dB below the signals. Comparisons of the FFT magnitudes at the fundamental frequencies with direct frequency analysis are listed in Table 3.1, where accuracy of 13 decimal digits is demonstrated.

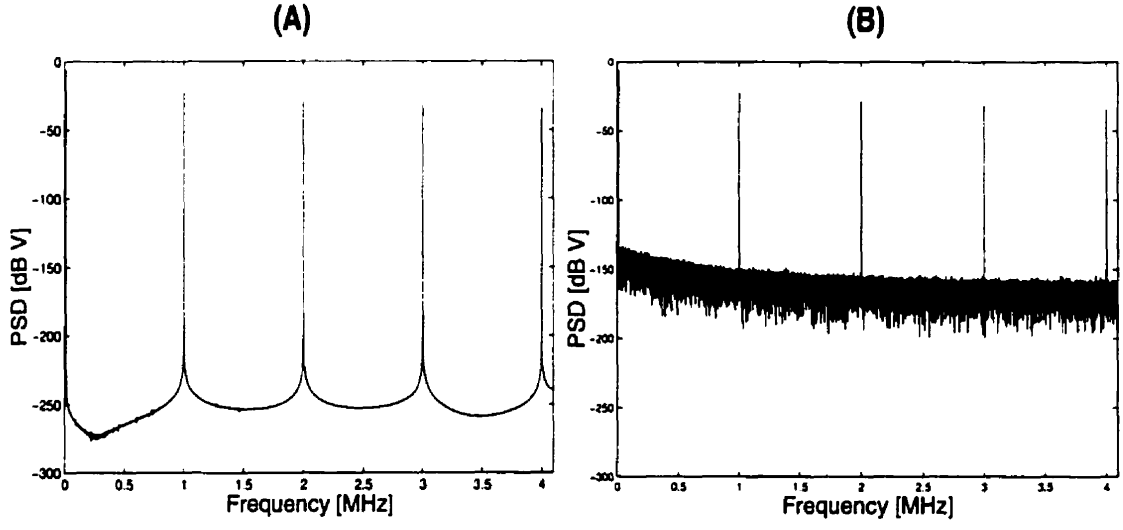


Figure 3.9: RC circuit: simulation accuracy

The same circuit is analyzed again when both thermal noise generated by the resistor and input signal $e(t)$ are present. Thermal noise is modeled by a random pulse waveform shown in Fig. 3.6, and is treated as a step source in each time slot of width h. The thermal noise power generated by the resistor in the RC circuit at room temperature is given by

$$\eta = 4kTR = 16.18 \times 10^{-15} \quad \text{V}^2/\text{Hz} \tag{3.12}$$

Note that the thermal noise is many orders of magnitude smaller than the primary signal $e(t)$. The transient noise analysis is carried out with $h = 1.2207 \times 10^{-7}$ s, corresponding to a noise bandwidth of 8.192 MHz. The FFT results in Fig. 3.9(B) show the presence of both the input frequencies and the noise floor due to thermal noise. Since the thermal noise floor is about 160 dB below, and the simulation noise is more than 220 dB below the input frequencies, the thermal noise result can be expected to be accurate. Its noise spectrum is *clean*, which suggests that the simulation accuracy is adequate and the thermal noise analysis results are not distorted when computed with large signal waveforms.

These examples show that SIMthermal can provide accurate simulation. A numerical

noise floor of -220 dB is observed. It can meet the challenge of noise analysis of high-resolution SDMs.

For this LTI circuit, direct frequency-domain noise analysis is possible. Its thermal noise power spectrum density is

$$\begin{aligned} PSD(f) &= \sqrt{4kTR}\,|H(f)|, \quad 0 < f < +\infty \\ &= \sqrt{\frac{4kTR}{1+4\pi^2R^2C^2f^2}} \ \mathrm{V}/\sqrt{\mathrm{Hz}} \end{aligned} \tag{3.13}$$

where $H(f)$ is the transfer function from noise source to output. Excellent agreement between frequency domain analysis and FFT spectra of time-domain simulation data is shown in Fig. 3.10(A). In this experiment, the time-domain noise simulation was done once, and the FFT spectra smoothed by a moving Hann window. If necessary, multiple simulations with different seeds can be done to average the noise spectra for a closer agreement.

The noise power in frequency band $[0,\ f]$ is

$$\begin{aligned} Power(f) &= \int_0^f 4kTR\,|H(\tau)|^2 d\tau \\ &= \frac{2kT}{\pi C}\tan^{-1}(2\pi RCf) \ \mathrm{V}^2 \end{aligned} \tag{3.14}$$

The noise power computed from FFT spectra matches equation (3.14) in Fig. 3.10(B), and shows the theoretical limit of $\frac{kT}{C}$ expected for this circuit.

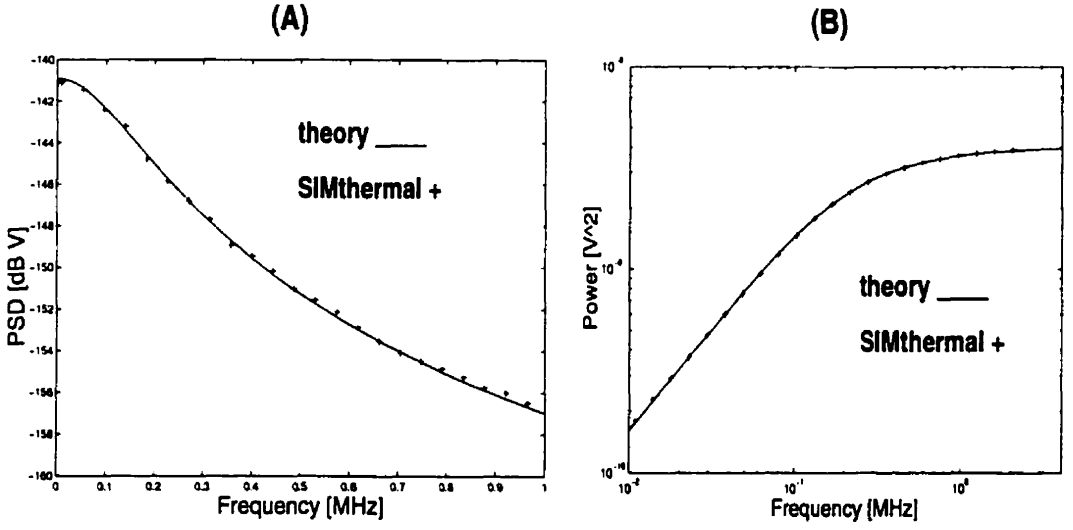


Figure 3.10: RC circuit: thermal noise simulation

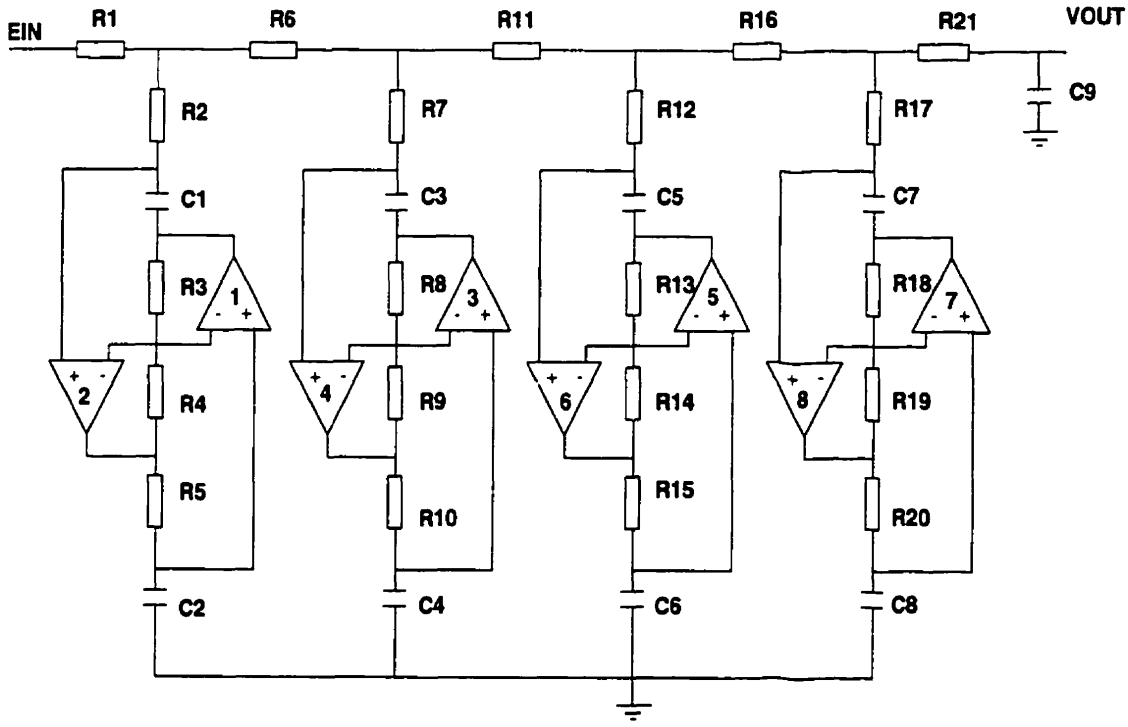
3.5.2 Linear Time Invariant Circuits

In order to validate the proposed technique, the ninth order filter [55] in Fig. 3.11 was analyzed and the results are compared with HSPICE frequency-domain noise analysis. In this circuit, thermal noise is generated by all resistors. The noise pulse-width $h = 5\ \mu s$ was used.

The plots in Fig. 3.12 show the excellent agreement between the HSPICE frequency-domain analysis and the FFT spectrum of SIMthermal time-domain simulation. In this experiment, the SIMthermal results were smoothed by a 61-point moving Hann window.

In order to make comparison easy, the FFT spectrum of SIMthermal simulation has been scaled up by 3.0103 dB. This is because HSPICE gives unilateral results in frequency domain, whereas the standard FFT spectrum is bilateral. The HSPICE thermal noise power curve is obtained by numerical integration of its frequency-domain noise analysis. As shown in the figure, SIMthermal results closely follow the HSPICE noise-

power curve and converge to the same constant.



C1= 12	R1 = 5.4779	R10= 4.25725	R19= 3.3
C2= 10	R2 = 2.0076	R11= 3.2201	R20= 5.808498
C3= 6.8	R3 = 3.3	R12= 5.88327	R21= 1.2201
C4= 10	R4 = 3.3	R13= 3.3	
C5= 4.7	R5 = 4.5898	R14= 3.3	R in kΩ
C6= 10	R6 = 4.44	R15= 5.62599	C in nF
C7= 6.8	R7 = 5.9999	R16= 3.63678	
C8= 10	R8 = 3.3	R17= 1.0301	
C9= 10	R9 = 3.3	R18= 3.3	

Figure 3.11: A ninth order low-pass filter

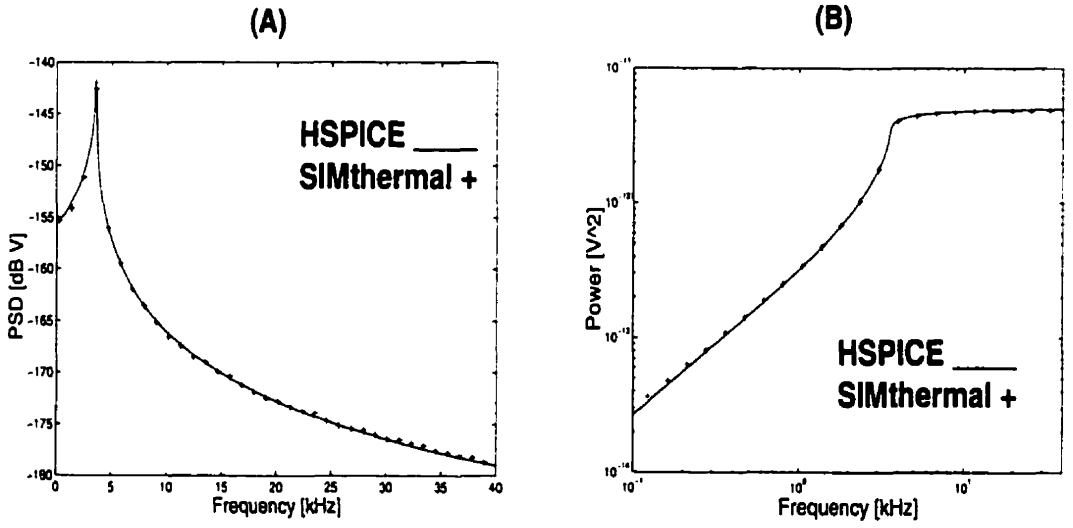


Figure 3.12: 9th-order filter: thermal noise simulation

3.5.3 Periodically Switched Linear Circuits

The circuit in Fig. 3.13 is a SC integrator from [22]. The clock frequency is 10 kHz, and there are four phases with equal widths of 25 μs. The capacitors are 10 pF each, and the switches have 3.5 $k\Omega$ ON-resistances. The operational amplifier has 700 kHz unity gain-bandwidth and an equivalent noise resistance of 1.55 $M\Omega$. In this circuit, thermal noise is generated by the switches and the opamp. As mentioned in section 3.3.1, high frequency noise can be aliased into the baseband due to switching. We can control the simulated noise bandwidth by changing the pulse-width in the noise waveform used in transient analysis. The noise bandwidth is inversely proportional to the pulse width and a narrower pulse will result in more thermal noise being aliased into the baseband. The noise power in the baseband will eventually saturate, due to the fact that the circuit will not be able to respond to very high frequency signals.

The phenomenon of increased noise power in the baseband with increasing noise bandwidth is shown in Fig. 3.14(A), for noise bandwidths of 400 kHz, 2 MHz, 10 MHz,

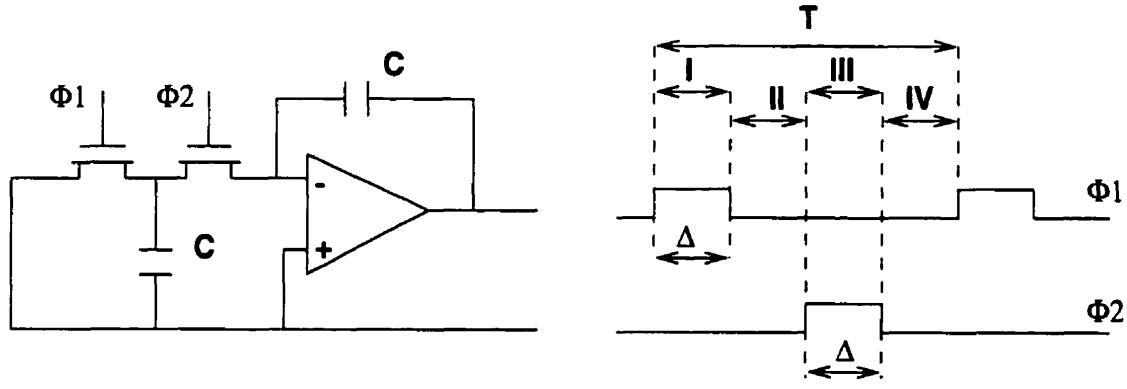


Figure 3.13: A switched-capacitor integrator

and 50 MHz. The curves for noise bandwidth of 10 MHz and 50 MHz are virtually identical, indicating that the noise power in the baseband has saturated to its final limit. The physical measurement data for this circuit were provided in [22]. They are shown in Fig. 3.14 by the circle symbol. The small differences between simulation and measurement validate our algorithms.

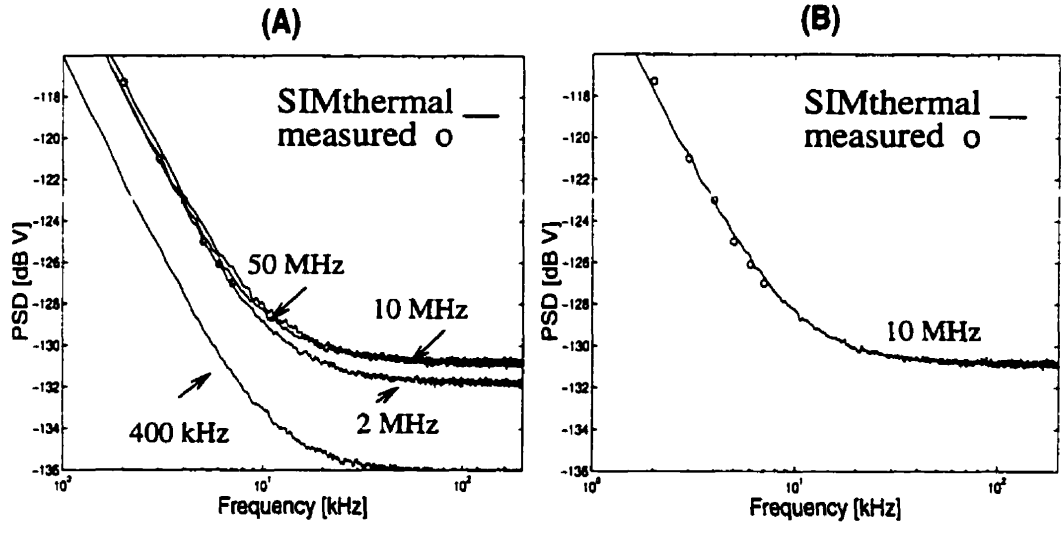


Figure 3.14: SC integrator: thermal noise simulation

3.5.4 Oversampled Sigma-Delta Modulators

In this section, a SC and a CT SDM are simulated to show the usefulness of the proposed algorithm. Comparisons with experimental observations are made.

A Switched-Capacitor Sigma-Delta Modulator

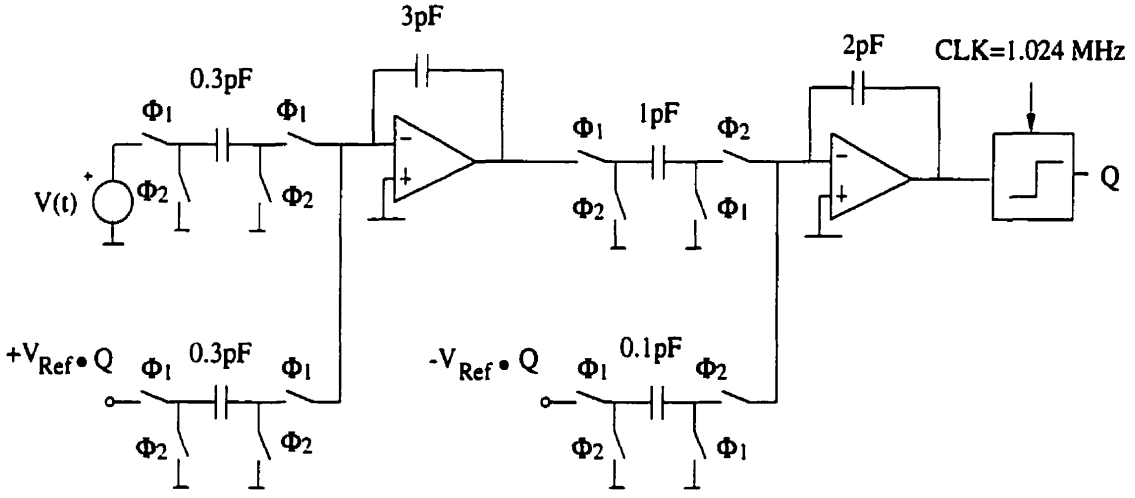


Figure 3.15: A second order switched-capacitor SDM

The circuit in Fig. 3.15 is a second-order switched-capacitor sigma-delta modulator. It is clocked at 1.024 MHz and the input signal is a 1 kHz sinusoid of amplitude 0.75 V. The circuit is simulated initially with ideal elements, i.e., the switches have zero conductance in their OFF state and zero resistance in their ON state. The opamps have infinite unity gain-bandwidth, and there is no thermal noise generated by elements in the circuit. It takes SIMthermal 18.64 seconds to simulate 74k clock cycles. The output spectrum obtained by FFT on the last 64k data is shown in Fig. 3.16(A). It displays the typical high-pass quantization noise shaping of the modulator with a zero at DC. Assuming a 4 kHz bandwidth, the signal to quantization noise ratio for this ideal case is 80.5 dB.

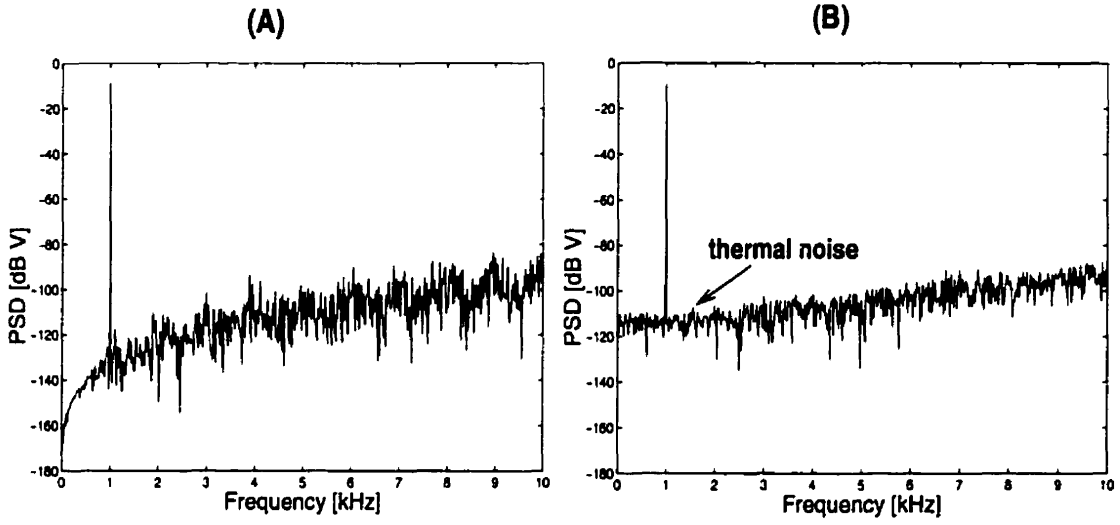


Figure 3.16: SC SDM: (A) ideal elements (B) with thermal noise

The same circuit is simulated again, this time with non-ideal elements. The switches have ON-resistances of 3.5 $k\Omega$ and are accompanied by thermal noise. The opamps have unity gain-bandwidth of 7 MHz and equivalent noise resistance of 1.55 MΩ. Simulation of 74k clock cycles now takes 12.3 minutes for a noise bandwidth of 102.4 MHz. FFT results are shown in Fig. 3.16(B). Due to the presence of thermal noise, there is now a noise floor at lower frequencies around -115 dB, instead of a zero at DC. At higher frequencies the quantization noise dominates, and the circuit still displays quantization noise shaping. Smoother output spectra compared with Fig. 3.16(A) are also observed. This indicates that the thermal noise acts as a dithering signal in the circuit. Assuming a 4 kHz bandwidth, the signal to quantization and thermal noise ratio for this non-ideal case is 77.7 dB, a drop of 3 dB from the previous case with ideal elements.

An oversampled sigma-delta modulator achieves high resolution by shaping most of the quantization noise out of the signal-band. In theory, higher order noise shaping results in higher resolution. In reality, this is not always true. A lower limit of the output

noise power exists because of the electrical noise floor [3, 4]. When in-band quantization noise power decreases, the total noise power will eventually be dominated by electrical noise. Simulation results in this section match the above predictions.

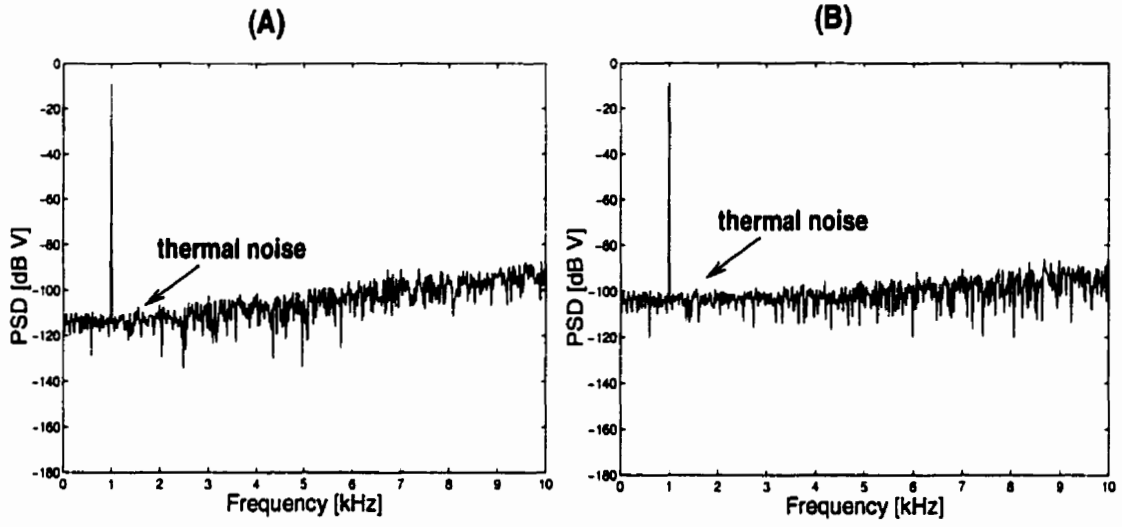


Figure 3.17: SC SDM: (A) with thermal noise (B) with increased thermal noise

As an experiment, all thermal noise powers in the network were increased by 20 dB and the circuit was re-simulated. The simulation results in Fig. 3.17(B) show that the thermal noise floor increases by the same amount at low frequencies while quantization noise eventually dominates at high frequencies. The signal to quantization and thermal noise ratio is now 70.2 dB, an additional drop of 7 dB compared with the previous case of non-ideal elements. The loss in performance due to higher electrical noise is evident. Further testing has shown that, as expected, the thermal noise generated by the input stages dominates the noise floor at the output. This example shows that thermal noise limits the resolution of a SDM in a fundamental way.

A Continuous-Time Sigma-Delta Modulator

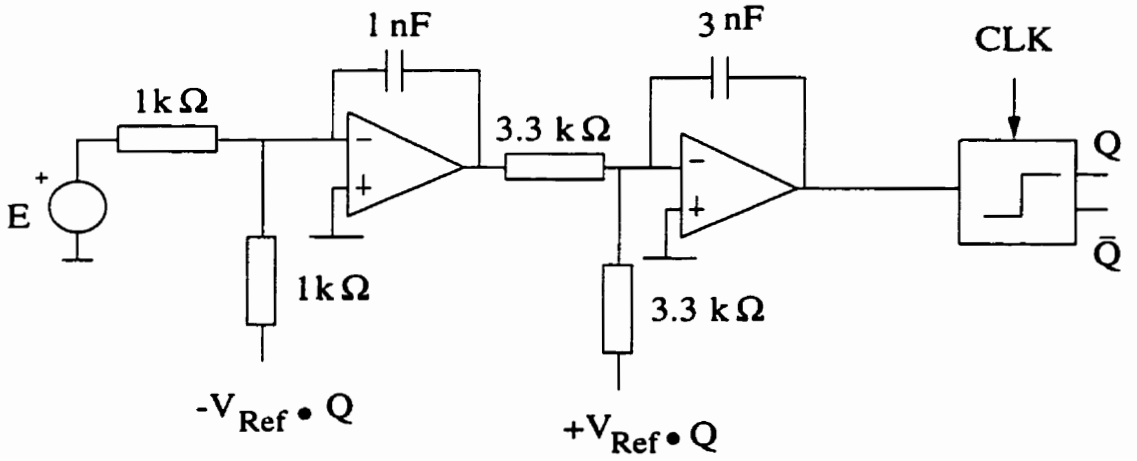


Figure 3.18: A second order continuous-time SDM

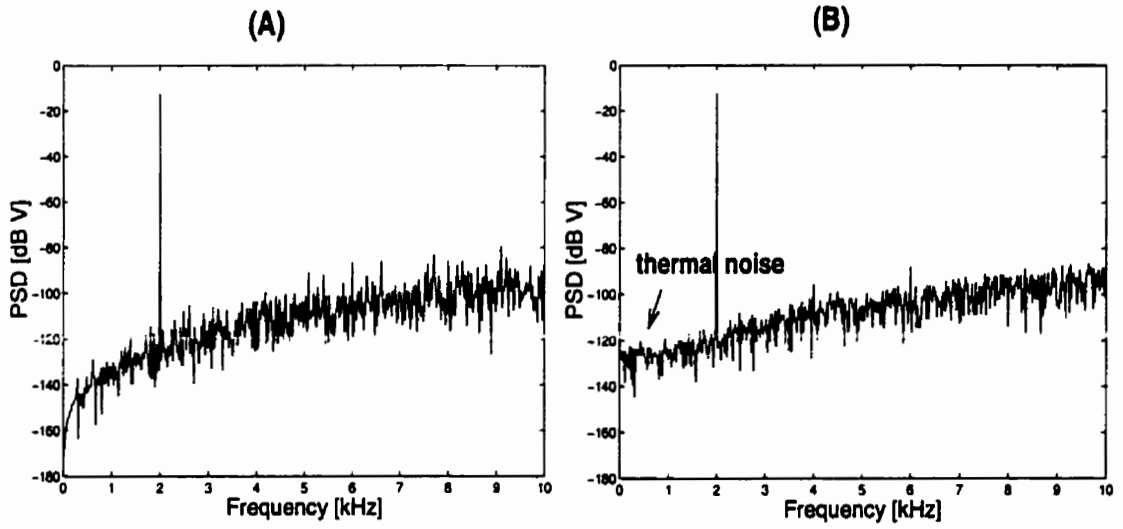


Figure 3.19: CT SDM: (A) ideal elements (B) with thermal noise

The second example, the SDM in Fig. 3.18, uses continuous-time instead of switched-capacitor integrators. The circuit is clocked at 1.024 MHz and the input is a 2 kHz sinusoid of amplitude 0.5 V. Simulation results with ideal elements are shown in Fig. 3.19(A).

They took 8.83 seconds of CPU time for 74k clock-cycle simulation. The results display a high-pass quantization noise transfer with a zero at DC.

The circuit is simulated again with non-ideal elements such that the resistors and opamps are associated with thermal noise. The opamps have a unity gain-bandwidth of 10 MHz and equivalent noise resistance of 1.55 MΩ. Computation of 74k clock cycles now takes 1.73 minutes and the results are shown in Fig. 3.19(B). The thermal noise floor can be observed at low frequencies.

Comparison With Prototype Chip Measurement

In the idle channel test, the signal is shorted to ground. In this case, clock jitter has little effect on the circuit performance. The noise floor is dominated by quantization noise and circuit noise – especially thermal noise. The idle channel measurement result of a second-order switched-capacitor SDM was provided in [85]. It is reprinted in Fig. 3.20[1]. This measurement result displays a flat noise spectrum at low frequencies and high-pass quantization noise shaping, which is very similar to the SDM thermal noise simulation results shown in Fig. 3.16(B). The simulation and measurement examples are both second-order SC SDMs. Although they are different circuits, the similarity between their spectrum shapes gives confidence to our method.

3.6 Chapter Summary

In this chapter, we presented an efficient method for time-domain computer-aided noise analysis of sigma-delta modulators. To the best of the author's knowledge, general noise analysis methods for SDMs at the electrical circuit level have not been presented before.

[1]Reprinted with permission from [85].

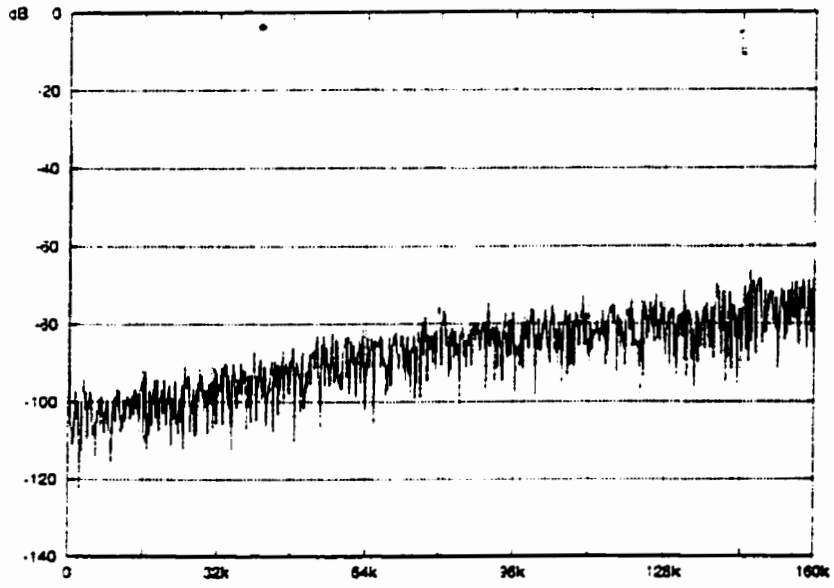


Figure 3.20: S. Sen, PhD thesis: f_s = 10MHz, Idle channel test

The new method gives full details of analog simulation, and the noise contributions by individual elements can be easily studied. It is useful in detailed circuit design and verification phases for SDMs.

The method can also be applied to periodically switched linear networks. Compared with the frequency-domain noise analysis of PSL circuits, it has its advantages. The computation of aliasing transfer functions is not needed. This offsets the computational cost by the use of a narrow pulse to model high frequency noise. Since all uncorrelated noise sources are applied simultaneously, the adjoint network concept used in frequency

domain noise analysis is not needed either.

The algorithms have been implemented in a computer program. Examples of thermal noise simulation were given. Simulation results were compared with exact analysis, direct frequency analysis, or measurements where available. Good agreement was shown. Thermal noise analysis for 75776 clock cycles of typical SDMs is obtained in less than 20 minutes of CPU time on a Sun Sparc workstation.

The method is illustrated with thermal noise analysis only. It can be readily extended to other types of noise, including colored ones, when a suitable random waveform representing the noise [85] is available.

Chapter 4

Dithering Analysis

This chapter proposes a new method for electrical circuit level dithering analysis of SDMs. It is an application of the time domain noise analysis method presented in chapter 3. The algorithm has been implemented in a computer program, and can be used to study dithering effects in SDMs with or without the presence of thermal noise and clock jitter.

Simulation examples of a switched-capacitor and a continuous-time SDM are given. The influence of dithering in breaking up the limit-cycle pattern is shown, and the role of thermal noise in acting as dithering noise is demonstrated. The results of this chapter were presented in [86].

4.1 Introduction

SDMs are popular in digital audio and telephony applications, where high conversion resolution is required and the signal bandwidth is small to modest. With the highly nonlinear element – quantizer – in the feedback loop, all sigma-delta modulators suffer

from performance degradation due to unwanted tones in the signal-band [29]. These tones are usually signal dependent, and are generated from the periodic noise structure, pattern-noise, at the input of the quantizer. The tonal phenomenon can be severe if the input signal is slowly varying or if its amplitude is small, and are often referred as idle channel tones [29]. The Human ear is very sensitive to pattern-noise [30]. In order to improve the quality of signal conversion, additional noise can be added to the circuit [30, 87, 88, 89, 90, 91, 92] to break up the noise pattern and eliminate unwanted tones. This technique is referred to as dithering.

The effect of dithering has been studied extensively at block level [29, 30, 89, 87]. It is useful for digital modulators. For analog modulators, it is useful in the conceptual design phase, but encounters great difficulty in circuit design phase. The limitations are:

1. Dithering noise can be inserted at the beginning or at the end of each block only. The locations for exploring dithering are restricted.

2. Although thermal noise information is important for the study of the dithering effect,[1] it is not available at block level.

3. Continuous-time SDMs cannot be handled.

Electrical circuit level dithering analysis is needed, but such a method was not available elsewhere. In this chapter, we give a new electrical circuit level method for computer-aided dithering analysis of SDMs. It can be used to study dithering effects in SC, SI, and CT SDMs, with or without the presence of thermal noise and clock jitter. The method is presented in section 4.2, and the simulation results of a SC and a CT SDM are given in section 4.3.

[1] It is observed that thermal noise can smooth out most of the small in-band tones [30].

4.2 New Dithering Analysis Method

The general noise analysis method described in chapter 3 can be extended to handle dithering analysis. A random dithering noise is represented in time domain as a random amplitude pulse waveform, as shown in Fig. 3.6. The pulse amplitude is assigned by the dithering noise sequence, which can be generated by a pseudo-random number generator. The noise-bandwidth is controlled by the pulse width, and the noise power is controlled by the variance of the random pulse-amplitudes. Both parameters are given by the user.

Equation (3.9) is modified to accommodate dithering noise

$$\mathbf{v}(nh+h) = \mathbf{M}\mathbf{v}(nh) + \sum_{i=1}^{K_1} \mathbf{P}_{s_i} e^{s_i nh} + \sum_{j=1}^{K_2} \mathbf{P}_{n_j} u_j(nh) + \sum_{l=1}^{K_3} \mathbf{P}_{\xi_l}(h)\xi_l(nh) \quad (4.1)$$

where K_3 is the number of dithering noise sources added to the circuit, vector $\mathbf{P}_{\xi_l}(h)$ is the zero-state unit-step response from the l-th dithering noise source to the output, and $\xi_l(nh)$ represents the noise amplitude in time slot (nh). The vectors $\mathbf{P}_{\xi_l}(h)$ are constant, and are computed only once in a preprocessing step. During simulation, the circuit is analyzed by solving (4.1) successively. Dithering noise added to any node in the circuit can be handled and can be studied with thermal noise. This is a major advantage over block-level analysis.

4.3 Numerical Examples

The algorithm has been implemented in a computer program, SIMdither. It accepts all types of linear elements, clock controlled ideal switches, and latched comparators as building blocks. Here we give simulations for a SC and a CT SDM to show the usefulness of the method. The results are compared with experimental observations.

4.3.1 A Switched-Capacitor Sigma-Delta Modulator

The second-order SC SDM shown in Fig. 3.15 is studied with the input

$$v(t) = 0.01\sin(2\pi ft) \text{ V}, \quad f = 1\text{kHz}. \tag{4.2}$$

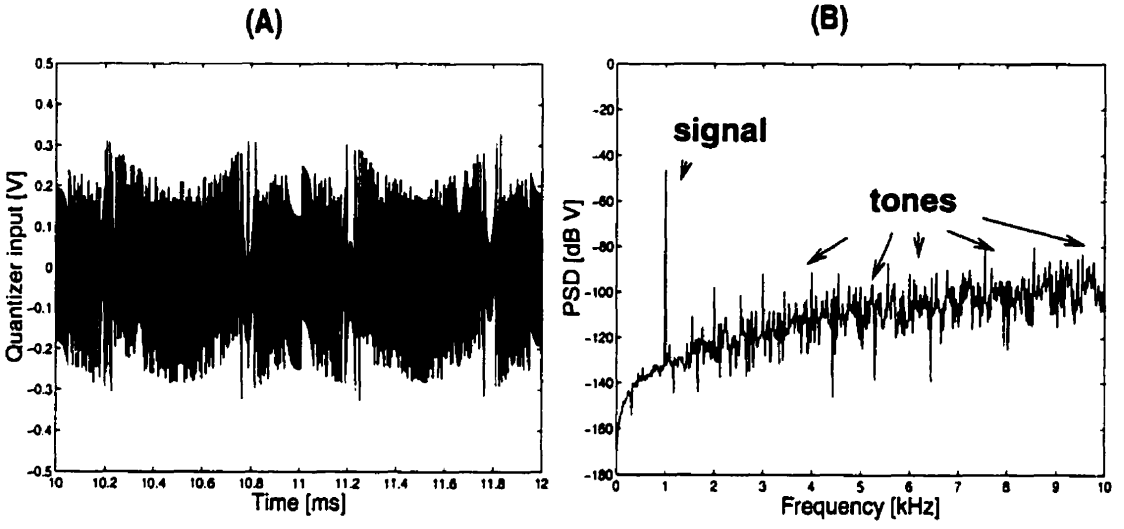


Figure 4.1: SC SDM: ideal elements (A) comparator input (B) output spectrum

The modulator is first analyzed with ideal switches and ideal opamps. As shown in Fig. 4.1(A), pattern-noise is visible at the input of the quantizer. The PSD of the quantizer output sequence is shown in Fig. 4.1(B). It clearly displays idle channel tones at multiple frequencies. These tones are large, and severely degrade the conversion quality.

The modulator is next analyzed with the assumption that all switches are non-ideal with 3.5 $k\Omega$ ON-resistance and infinite OFF-resistance, and the operational amplifiers are non-ideal with 7 MHz unity-gain bandwidth and 1.55 MΩ equivalent noise resistance. The output plots are similar to what are shown in Fig. 4.1.

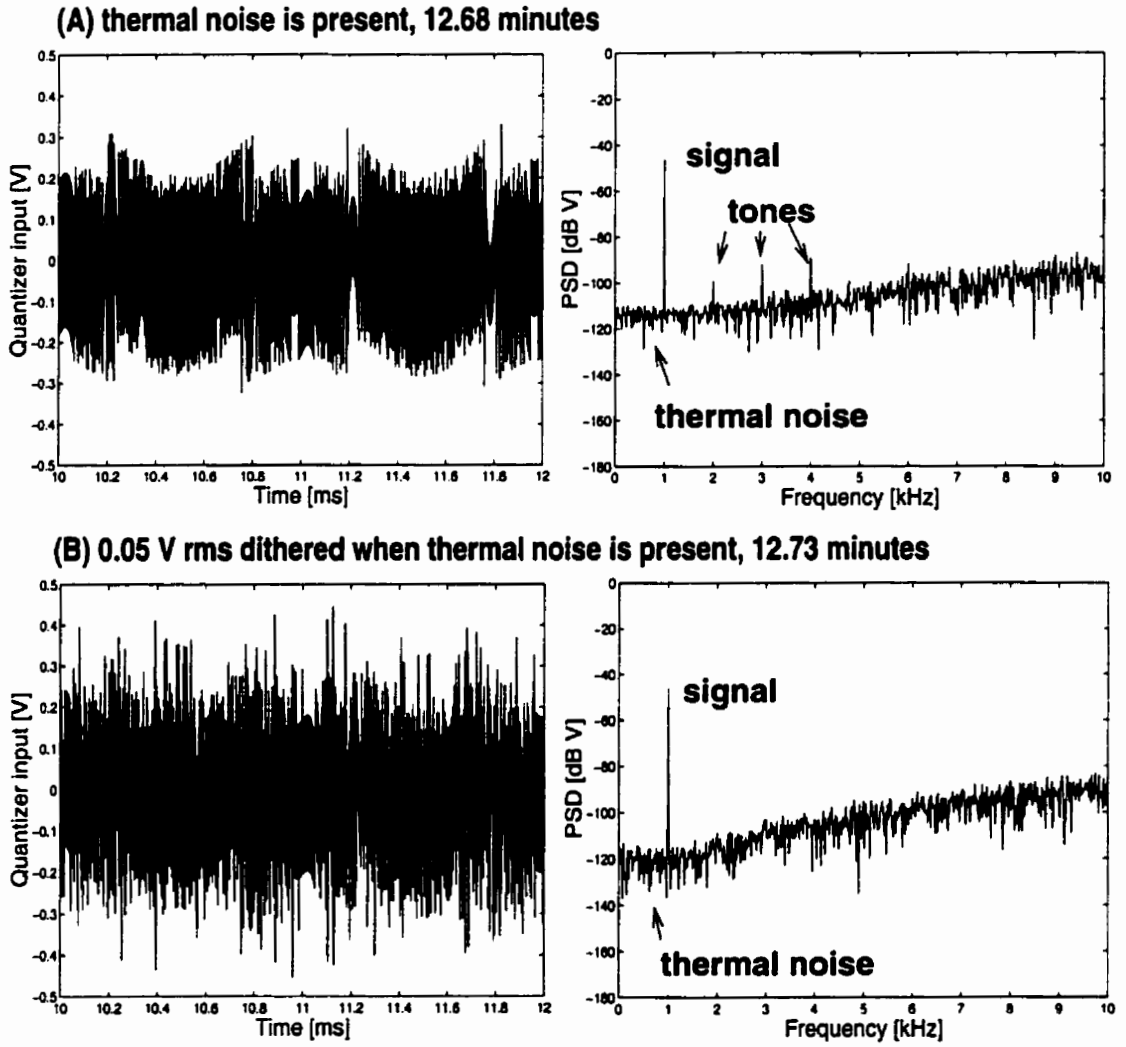


Figure 4.2: SC SDM: thermal noise is present (A) original (B) dithered

When non-ideal switches and non-ideal opamps generate thermal noise, the output plots are quite different from the previous case. As shown in Fig. 4.2(A), the PSD of the output sequence displays much smoother noise floor, where the small idle channel tones have disappeared. Only harmonic distortion of the input signal is visible. The noise floor in the low frequency range is determined by thermal noise, while in higher frequency

ranges, it is dominated by quantization noise. The comparator input waveform shown in Fig. 4.2(A) exhibits the same noise pattern as before.

In an attempt to remove the remaining nonlinear distortion, a 0.05 V rms (root-mean-square) random dithering noise is added to the input of the comparator. Simulation over 74k clock cycles takes 12.73 minutes with the presence of thermal noise. As shown in Fig. 4.2(B): (1) The periodic noise pattern at the comparator input is destroyed; (2) The harmonic distortion disappears, and a smooth noise floor is obtained; (3) The dithering noise added at the input of the quantizer experiences the same noise-shaping as the quantization noise, and increases the quantization noise floor; (4) Thermal noise still dominates in the low frequency range.

The simulation results agree with experimental observations [30] that there exist idle channel tones at the output of SDMs; thermal noise can ease out most of the small in-band tones, and additional dithering noise is needed to remove the remaining ones.

4.3.2 A Continuous-Time Sigma-Delta Modulator

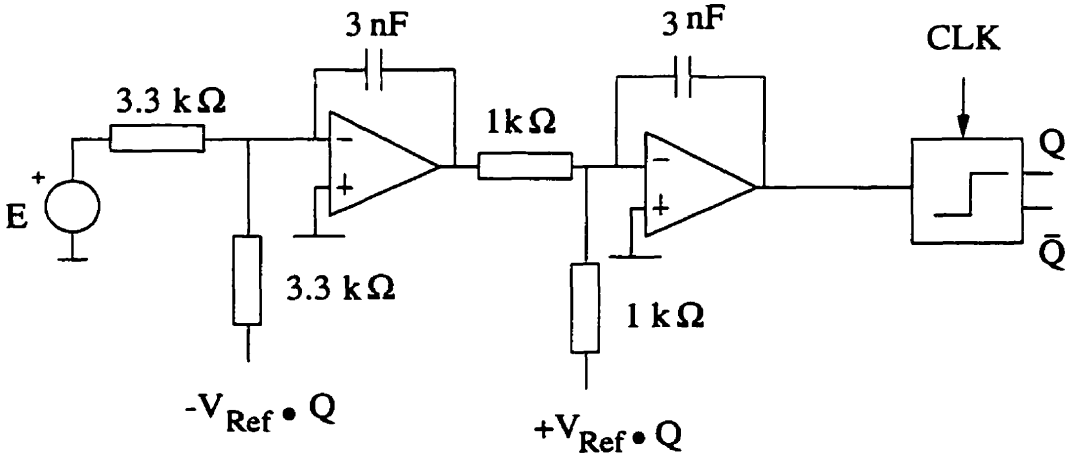


Figure 4.3: A continuous-time second order sigma-delta modulator

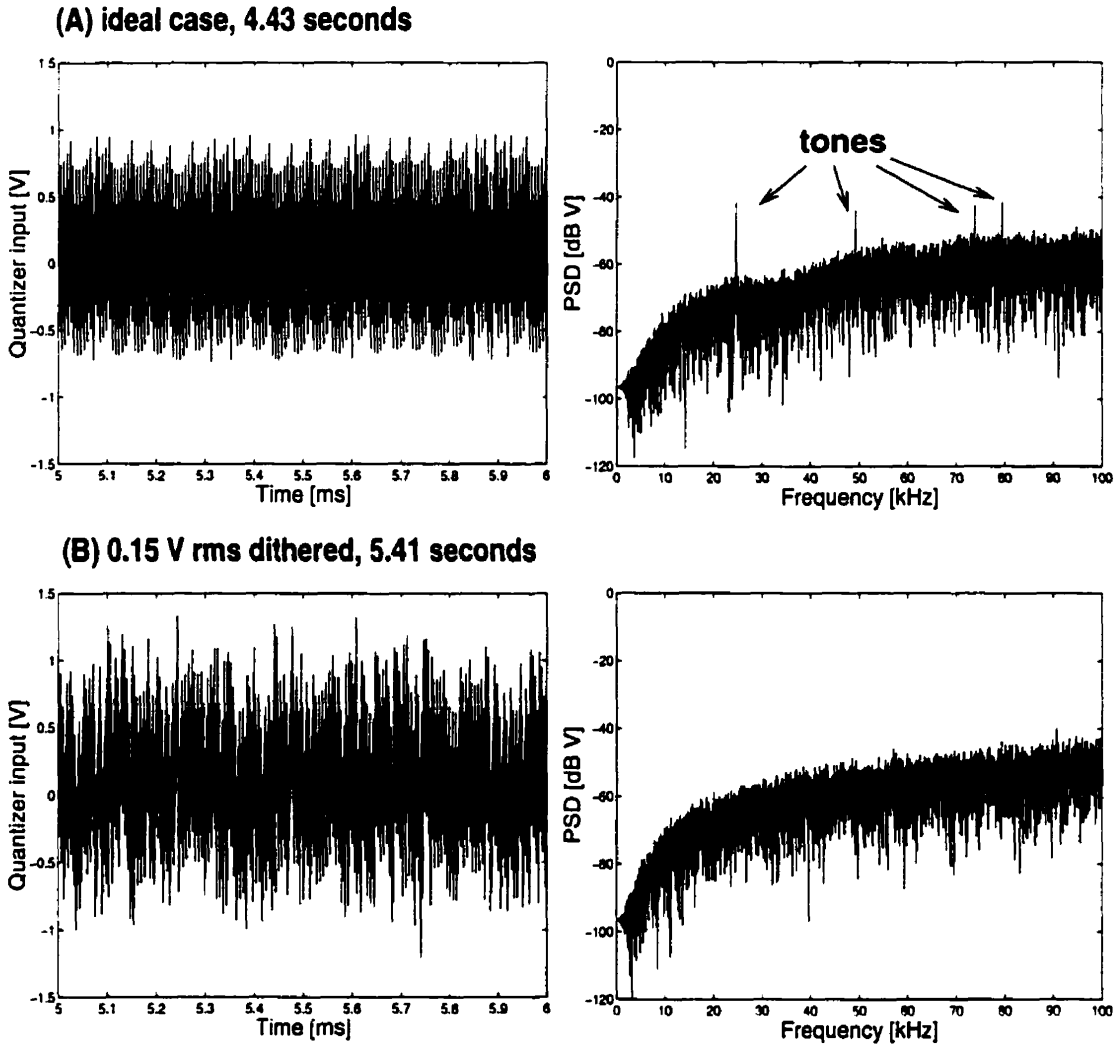


Figure 4.4: CT SDM: DC input, ideal elements (A) original (B) dithered

As the second example, we consider the CT SDM in Fig. 4.3. The clock frequency is 1.024 MHz and the reference voltages are ± 2.5V. The input to the modulator is a small constant voltage $v(t) = 0.375$ V. As shown in Fig. 4.4(A), the comparator input waveform clearly displays pattern-noise, and multiple tones appear in the plots of the output power spectrum. Random dithering noise of 0.15 V rms is applied to the comparator

input. The noise pattern is destroyed and the idle channel tones disappear. This is shown in Fig. 4.4(B).

4.4 Chapter Summary

In this chapter, we presented an efficient dithering analysis algorithm for SDMs. To the best knowledge of the author, it is the *first-ever* method available at electrical circuit level. The advantages over block level analysis are: (1) there are more freedoms in the study of dithering effect. Dithering noise can be added to many nodes in the circuit, not just at the beginning/end of each block; (2) The effect of dithering can be studied in conjunction with the study of thermal noise and clock jitter effects; (3) SDMs with continuous-time loopfilters can be easily simulated. This dithering analysis method is useful in the detailed circuit design phase of analog modulators.

Chapter 5

Varying-Step Sampled-Data Analysis

This chapter presents a new method for sampled data analysis of LTI circuits. It differs *fundamentally* from classical sampled data analysis in that the data points can be spaced with slightly varying time intervals.

The special sampled data method can be used for clock jitter analysis of SC and SI filters, as well as SDMs. *No* restriction is imposed on the jitter waveform. It enables random jitter analysis at the electrical circuit level. This is a major advance over previous approaches, where only periodic clock jitter could be analyzed.

The method needs numerical evaluation of the time derivatives of the transition matrix, a well known quantity in circuit theory, and the time derivatives of the input transfer vector. Methods for direct numerical computation of the derivatives are given in this chapter. They are based on circuit theory concepts, and are illustrated on modified nodal analysis.

The theory was implemented in a computer program. Numerical examples are given on the clock jitter analysis of a SC and a SI filter. Analysis of SDMs is addressed in chapter 6.

5.1 Introduction

Accurate reconstruction of a sampled signal requires that the sampling should have occurred at precisely known time instants. In reality, because of noise and various interferences coupled into the clock generating circuitry, the actual clocking instants deviate slightly from their nominal values. This small deviation is called clock jitter, as illustrated in Fig. 5.1. It introduces errors into the system.

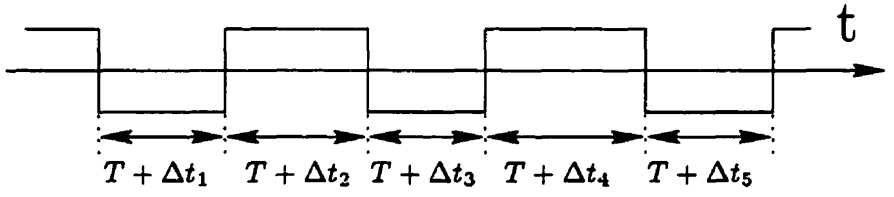


Figure 5.1: Clock jitter

Clock jitter in the input sampling circuit imposes fundamental limits on the quality of a sampled system. The error is directly added to the signal and cannot be corrected in later stages [93]. It is a major design issue, especially in high frequency and high resolution applications.

The performance of an analog sampled data circuit is critically affected by clock jitter. Theoretical analysis and experimental studies show that clock jitter can shift the frequency response of a SC filter and generate undesired sidebands [94]. The fact that clock jitter contributes significantly to the noise level in high frequency SDMs is well recognized [5, 6, 7, 8, 9]. Experimental studies [57] show that sinusoidal clock jitter reduces the height of the input sine component and introduces sideband frequency components, while random clock jitter results in an overall elevation of the noise floor.

Although clock jitter is usually wideband, previous methods [27, 28] at the electrical circuit level are *fundamentally* restricted to periodic jitter waveforms. They are also

limited to the analysis of ideal SC circuits. We present a new method at electrical circuit level. It is applicable to clock jitter analysis of SC and SI filters, as well as SDMs. *No* restriction on the jitter waveform is imposed. Both periodic and random clock jitter can be analyzed.

A state-of-the-art review of clock jitter analysis is given in section 5.2. The method is described in section 5.3. It requires numerical evaluation of time derivatives of the transition matrix and of the input transfer vector. Direct numerical computation methods for these derivative matrices and vectors are given in section 5.4. Numerical examples of random and periodic clock jitter analysis of a SC and a SI filter are given in section 5.5, and the simulation results are compared with experimental observations.

5.2 Clock Jitter Analysis: Review

Two distinct approaches have been used for clock jitter analysis: the *digital* and the *electrical circuit* approaches. Methods in the first category assume that input sampling is the only source of error, and view the circuit as digital. The analysis is done on the z-domain transfer function or on the difference equation describing the digital filter. Methods in the second category view the circuit as electrical, and apply circuit analysis techniques. An overview is given in the following.

5.2.1 Digital Circuit Approach

A typical example in this category is described in [94]. The key points are: (1) Nonuniform input sampling is viewed as the only source of error introduced by clock jitter; (2) An analog sampled data circuit is assumed to perform discrete-time mathematical operations only, and the analog side of circuit effects is disregarded; (3) The analysis is

performed on either the z-domain transfer function or the difference equation describing the circuit. The process is as following: The input signal is sampled by a switch associated with timing jitter, and is fed into the transfer function of the digital filter; The output sequence of the digital filter is then converted into a continuous-time waveform by a sample-and-hold arrangement driven by the same clock as the sampling switch.

Due to the simplifications in the analysis, no restriction on the jitter waveform is imposed. But this approach is highly abstract and mathematical, and the drawbacks are:

1. Tedious hand-analysis is needed to obtain the z-domain transfer function or the difference equation. This is often not an easy task [95]. Furthermore, in some cases, when the signals are not sampled-and-held, the z-domain or difference equation solution is not valid [95];

2. Transient information is missing. The input and output of the circuit are viewed as data sequences, regardless the exact timing when the sampling occurs. But circuit nonidealities like switch ON-resistances and opamp finite frequency response have the consequence that the capacitor voltages never charge or discharge fully during a switching interval [95]. As far as the effect of clock jitter is concerned, the exact switching time is important. It can severely affect the performance estimation of high frequency and high resolution circuits, such as high frequency SC filters and SDMs.

5.2.2 Electrical Circuit Approach

Methods in this category apply circuit analysis techniques, and usually no hand derivations of the transfer function are required.

Previous methods in this category [27, 28] are based on classical SC analysis techniques which exploit the periodic switching nature of the circuit. They are *fundamentally* restricted to periodic clock jitter. In addition, these methods are formulated in the QV regime, where time-domain integration is avoided by eliminating current from the formulation. Some circuit nonidealities, like switch ON-resistances and finite frequency response of the amplifiers, cannot be included. Some important elements for modeling SI filters, like controlled current sources, are not available as well. The formulation in the QV regime limits the usefulness of these methods.

General methods, which are applicable to both SC and SI circuits and can be used to analyze the effects of random clock jitter, are needed. Such a method is given in this chapter.

5.3 Varying-Step Sampled-Data Analysis

5.3.1 Background

Transient analysis of dynamic linear networks usually requires time integration with many small steps [68]. The demand for accuracy leads to an exceedingly long execution time [19]. Simulation accuracy and efficiency are often traded off.

Frequently, we are interested in the solutions at some discrete time instants only. An example is the transient analysis of PSL networks. Only the circuit outputs just before switching are of interest. Information about the waveforms between switching instants is usually not needed. In this case, it is possible to simultaneously maintain simulation accuracy and efficiency.

Sampled data analysis of analog circuits, reviewed in section 2.4, can be used to compute the circuit response successively at fixed discrete time instants. The simulation

is carried out by difference equation manipulations on pre-computed constant matrices and vectors. Simulation efficiency and accuracy can be achieved at the same time. It is useful when long and accurate transient analysis is needed at discrete time instants. The underlying condition is that these discrete time instants are known *a priori*, that is, no uncertainty in the timing is allowed. In addition, the time instants should be equally spaced, or at least the spacing between them should belong to a finite set of fixed time intervals. These two conditions ensure that only a finite, and preferably a small set of constant matrices and vectors need be pre-computed.

We are interested in clock jitter analysis of PSL networks and SDMs. As explained in section 2.3, they are dual time circuits with a rapidly varying clock and a slowly varying input signal. Transient analysis over a large number of clock cycles is required to evaluate their performance measures. In addition, SDMs are high resolution circuits. Simulation accuracy has to be addressed. Fortunately, for these circuits only the solution just before switching is of interest. Sampled data analysis is suitable in this situation.

Random clock jitter brings fluctuations to the switching period. Because of the uncertainty in switching, the exact timing when the circuit changes its state is not known in advance. The conditions to apply classical sampled data analysis are not satisfied.

We present a new sampled data analysis method that can be used to compute circuit response at discrete time instants separated by slightly varying intervals. The simulation is done by difference equation manipulation on a set of precomputed constant matrices and vectors. Both simulation accuracy and efficiency can be maintained. It can be applied to clock jitter analysis of PSL networks and SDMs. No restrictions are imposed on the jitter waveform. The effects of either random or arbitrarily defined deterministic clock jitter on the circuit performance can be analyzed.

5.3.2 The Algorithm

Time domain solution of linear system of equations (2.5) can be written in closed form [19] for complex exponential input $u(t) = e^{st}$, $t \geq t_0$:

$$\mathbf{x}(t) = e^{\mathbf{A}(t-t_0)}\mathbf{x}(t_0) + e^{st_0}(s\mathbf{I} - \mathbf{A})^{-1}[e^{s(t-t_0)}\mathbf{I} - e^{\mathbf{A}(t-t_0)}]\mathbf{B}. \tag{5.1}$$

Defining

$$\begin{aligned} \mathbf{M}(t-t_0) &= e^{\mathbf{A}(t-t_0)} \\ \mathbf{P}(t-t_0) &= (s\mathbf{I} - \mathbf{A})^{-1}[e^{s(t-t_0)}\mathbf{I} - e^{\mathbf{A}(t-t_0)}]\mathbf{B}, \end{aligned} \tag{5.2}$$

equation (5.1) can be written as

$$\mathbf{x}(t) = \mathbf{M}(t-t_0)\mathbf{x}(t_0) + \mathbf{P}(t-t_0)e^{st_0}. \tag{5.3}$$

We are interested in the solution of (5.1) at discrete time instants separated from each other by $(T + \Delta t)$, where T is a fixed time interval and Δt is a small deviation varying from step to step. A sampled data formula relating the solution at t_0 and $(t_0 + T + \Delta t)$ can be written as

$$\mathbf{x}(t_0 + T + \Delta t) = \mathbf{M}(T + \Delta t)\mathbf{x}(t_0) + \mathbf{P}(T + \Delta t)e^{st_0}. \tag{5.4}$$

The matrix $\mathbf{M}(T + \Delta t)$ and vector $\mathbf{P}(T + \Delta t)$ vary from step to step with Δt. Direct evaluation of them at every step is too expensive. A solution is to approximate them by a mixture of precomputed constant matrices and vectors. When the deviation Δt is small compared with the fixed time interval T, only a few terms of the Taylor series expansion around T can give good approximations:

$$\begin{aligned} \tilde{\mathbf{M}}(T + \Delta t) &= \mathbf{M}(T) + \sum_{i=1}^{k} \frac{(\Delta t)^i}{i!} \frac{d^i\mathbf{M}(t)}{dt^i}\Big|_{t=T} \\ \tilde{\mathbf{P}}(T + \Delta t) &= \mathbf{P}(T) + \sum_{i=1}^{k} \frac{(\Delta t)^i}{i!} \frac{d^i\mathbf{P}(t)}{dt^i}\Big|_{t=T} \end{aligned} \tag{5.5}$$

where k is the number of the differential terms. Methods for direct numerical computation of $\mathbf{M}(T)$ and $\mathbf{P}(T)$ were given in [19, 62], and methods for the derivative matrices and vectors are given in section 5.4. Constant matrix $\mathbf{M}(T)$, vector $\mathbf{P}(T)$, and their time derivatives up to the k-th term are computed before the simulation starts. At each step of $(T + \Delta t)$, matrix $\mathbf{M}(T + \Delta t)$ and vector $\mathbf{P}(T + \Delta t)$ are approximated by equation (5.5). The response at $(t_0 + T + \Delta t)$ is evaluated by (5.4). The circuit solution can be computed successively by recursively repeating the process.

This method is an extension of the sampled data analysis method presented in [19, 62]. The major differences between them are:

1. The previous method can only be used to compute equally spaced data points, while the new method can be used to compute data points spaced with slightly varying time intervals;

2. The previous method only precomputes a constant matrix M and a vector P, while the new method precomputes their time derivatives as well.

Many properties of the new method, such as the way how multiple inputs are handled, and the types of input functions allowed, are the same as presented in [19, 62]. They will not be discussed again in this thesis.

5.3.3 Simulation Accuracy

If the matrix $\mathbf{M}(T)$, vector $\mathbf{P}(T)$, and their derivatives are known at each simulation point, the only operations involved in (5.4) and (5.5) are matrix/vector multiplications and additions. The simulation accuracy is controlled by the accuracy with which $\mathbf{M}(T)$, $\mathbf{P}(T)$, and their derivatives are computed, and the number of terms used in the Taylor series approximations of $\mathbf{M}(T + \Delta t)$ and $\mathbf{P}(T + \Delta t)$.

The constant matrices and vectors are computed only once in a preprocessing step. Extra effort can be spent to calculate them accurately. Another important factor that limits the overall accuracy is how well $\mathbf{M}(T+\Delta t)$ and $\mathbf{P}(T+\Delta t)$ are approximated. This is controlled by the number of terms used in the Taylor series approximations. The remainders of Lagrange's form for the approximations are

$$\begin{aligned} \mathbf{M}\_R_{(k+1)} &= \frac{(\Delta t)^{(k+1)}}{(k+1)!}\left(\frac{d}{dt}\right)^{(k+1)}\mathbf{M}(\xi_1) \\ \mathbf{P}\_R_{(k+1)} &= \frac{(\Delta t)^{(k+1)}}{(k+1)!}\left(\frac{d}{dt}\right)^{(k+1)}\mathbf{P}(\xi_2) \end{aligned} \tag{5.6}$$

where ξ_1, ξ_2 exist between T and $(T+\Delta t)$. The error ϵ at simulation instant $t = t_0 + T + \Delta t$ is bounded by

$$\begin{aligned} |\epsilon(t_0+T+\Delta t)| &= |\mathbf{x}(t_0+T+\Delta t) - \tilde{\mathbf{x}}(t_0+T+\Delta t)| \\ &= \frac{|\Delta t|^{(k+1)}}{(k+1)!}\left(\left|\mathbf{M}^{(k+1)}(\xi_1)\mathbf{x}(t_0) + \mathbf{P}^{(k+1)}(\xi_2)e^{j\omega t_0}\right|\right) \\ &\leq \frac{|\Delta t|^{(k+1)}}{(k+1)!}\left(\left|\mathbf{M}^{(k+1)}(\xi_1)\mathbf{x}(t_0)\right| + \left|\mathbf{P}^{(k+1)}(\xi_2)\right|\right). \end{aligned} \tag{5.7}$$

where $\tilde{\mathbf{x}}(t_0+T+\Delta t)$ is the vector of variables computed by (5.4) when M and P are approximated by (5.5). If Δt is insignificant compared with T, accurate approximations can be obtained even with small k. This is the case for clock jitter analysis, where the uncertainty is usually less than 1% of the clock period. Typically, relative per step truncation error of the simulation algorithm can be set in the range of $10^{-9} - 10^{-12}$ with $k = 3$ to 5 only. Tests on a typical circuit show that for $k = 5$ and $\Delta t = 10\%T$, $\mathbf{M}(T+\Delta t)$ and $\mathbf{P}(T+\Delta t)$ were approximated with 12 decimal-digits accuracy.

5.3.4 Simulation Cost

The computational cost for M and P, and their time derivatives may not be trivial, but these matrices and vectors are computed only once and the cost is amortized over a long

transient analysis.

Assuming dense matrices and vectors, the total computational cost at each simulation point for evaluation of (5.4) and (5.5) is $((k+1)m^2 + (k+1)m + 2k - 2)$ multiplies and $((k+1)m^2 + (k-1)m + 1)$ additions. It is in the order of $O((k+1)m^2)$, where m is the size of the system matrix. When k is small, the computational cost per point is comparable to the equal-step sampled data method in [19, 62]. Normally, equations (5.4) and (5.5) are evaluated only once for each phase of a PSL network. For a two phase circuit, two simulation points are needed for each clock cycle. The computational cost per clock cycle is $O(2(k+1)m^2)$.

5.3.5 Storage Requirements

The storage requirements for each pair of M and P matrices of double precision accuracy are [19]:

$$\text{Memory} = 8B^2D + 16BCD \text{ bytes}$$

where B denotes the number of system variables (voltages and currents), C the number of input sources, and D the number of phases in a clocked circuit.

For the new method, the storage of M, P, and their derivatives up to the kth term are needed. The memory requirements grow to

$$\text{Memory} = 8(k+1)B^2D + 16(k+1)BCD \text{ bytes.}$$

When $k = 3$, the memory required to store the matrices for a circuit with $B = 100$ variables, $C = 2$ input sources, and $D = 2$ phases is 650k bytes.

5.3.6 Application: Arbitrary Waveform Clock Jitter Analysis

The sampled data method is also applicable to a restricted set of time varying and/or nonlinear circuits, in a similar way to [19]. These circuits change characteristics at discrete time instants only. Between those instants, the circuits are lumped, linear, and time invariant. Typical examples of circuits in this category are SC and SI filters, as well as SDMs.

Consider the case of SC and SI filters. These circuits are externally clocked, and change topologies at switching instants only. The network inside each phase is lumped, linear, and time invariant. Clock jitter analysis of these circuits is illustrated in the following. Assume a two phase circuit, and that the nominal durations for phases I and II are T_1 and T_2. Because of clock jitter, there is a small deviation of Δt varying from switching interval to interval, and the actual phase duration becomes $T_1 + \Delta t_1$, $T_2 + \Delta t_2$, $T_1 + \Delta t_3$, $T_2 + \Delta t_4$ ... Before the simulation starts, constant matrices and vectors $\mathbf{M}_1(T_1)$, $\mathbf{P}_1(T_1)$, $\mathbf{M}_2(T_2)$, $\mathbf{P}_2(T_2)$ and upto their k-th time derivatives are computed numerically for both phases, and stored for future reference. At each simulation step, $M(T+\Delta t)$ and $P(T+\Delta t)$ are computed from those constant matrices and vectors according to formula (5.5). The simulation process is shown in Fig. 5.2. The circuit

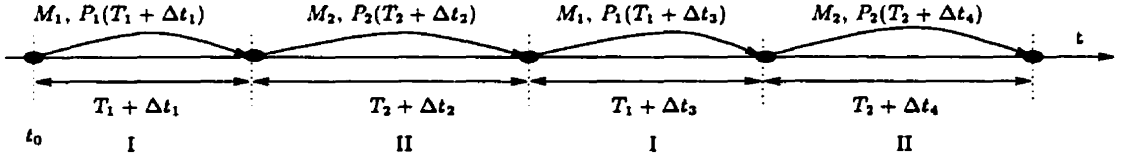


Figure 5.2: Simulation of periodically switched linear networks

response is evaluated at the end of each phase, as marked by the black dots in the graph, and the solution becomes the initial condition for the succeeding phase. The process can

be expressed by the following formula:

$$\begin{aligned}
&\mathbf{x}(t_0 + T_1 + \Delta t_1) = \\
&\quad \mathbf{M}_1(T_1 + \Delta t_1)\mathbf{x}(t_0) + \mathbf{P}_1(T_1 + \Delta t_1)e^{st_0} \\
&\mathbf{x}(t_0 + T_1 + \Delta t_1 + T_2 + \Delta t_2) = \\
&\quad \mathbf{M}_2(T_2 + \Delta t_2)\mathbf{x}(t_0 + T_1 + \Delta t_1) + \mathbf{P}_2(T_2 + \Delta t_2)e^{s(t_0+T_1+\Delta t_1)} \\
&\mathbf{x}(t_0 + T_1 + \Delta t_1 + T_2 + \Delta t_2 + T_1 + \Delta t_3) = \\
&\quad \mathbf{M}_1(T_1 + \Delta t_3)\mathbf{x}(t_0 + T_1 + \Delta t_1 + T_2 + \Delta t_2) + \mathbf{P}_1(T_1 + \Delta t_3)e^{s(t_0+T_1+\Delta t_1+T_2+\Delta t_2)} \\
&\qquad \vdots
\end{aligned} \tag{5.8}$$

which explains how the circuit solution is computed successively at the end of each phase.

There are two major advantages of this method. First, no restriction is imposed on the jitter waveform. The small deviation Δt can belong to a random process, or vary according to a deterministic function. The method can be applied to arbitrary waveform clock jitter analysis. Second, matrix M and vector P stand for the zero-input and zero-state circuit responses respectively. They are formulated at the linear circuit level. All linear circuit elements are accepted in the formulation. This enables the modeling of a wide variety of circuit implementations. The method can be applied to the clock jitter analysis of both SC and SI circuits. It is also applicable to SDMs, and this will be discussed in detail in chapter 6.

5.4 Time Derivatives of the Transition Matrix and Input Transfer Vector

The transition matrix M is related to the zero-input response and the input transfer vector P is related to the zero-state response of the circuit. They can form the complete response at discrete time instants separated by a varying step $(T + \Delta t)$, as given in equation (5.4). Matrix $\mathbf{M}(T + \Delta t)$ and vector $\mathbf{P}(T + \Delta t)$ vary from step to step with Δt. Although direct evaluation is possible [19], it is too expensive to perform at each step of a long simulation. Because jitter Δt is usually small compared with nominal clock duration T, it is possible to approximate $\mathbf{M}(T + \Delta t)$ and $\mathbf{P}(T + \Delta t)$ with high accuracy by a few terms of their Taylor series expansion around T. Numerical evaluation of the time derivatives of M and P are needed.

Popular formulation approaches for circuit analysis include the state-variable, modified nodal and tableau method. The state-variable formulation leads to a set of ordinary differential equations (ODE's), while modified nodal and tableau methods result in a set of differential-algebraic equations (DAE's) [62]. The transition matrix for ODE's is the matrix exponential $e^{\mathbf{A}T}$; it has many nice properties, including [68]:

$$\frac{de^{\mathbf{A}t}}{dt} = \mathbf{A}e^{\mathbf{A}t} = e^{\mathbf{A}t}\mathbf{A}. \tag{5.9}$$

Thus, if $e^{\mathbf{A}T}$ is computed, evaluation of its time derivatives is straightforward. Closed form analytical solution for DAE's is also available, for example, in the review paper [96], but it is mathematically oriented and highly complicated. Time derivatives of the transition matrix cannot be obtained by simple matrix manipulations as in the case of ODE's. Although DAE's can sometimes be transformed into ODE's, it is not always possible, for example, when the coefficient matrix is singular. This is the case for the

MNA equations

$$\mathbf{G}\mathbf{v}(t) + \mathbf{C}\frac{d\mathbf{v}(t)}{dt} = \mathbf{d}u(t), \quad \mathbf{v}(0) = \mathbf{v}_0, \tag{5.10}$$

where the matrix C is often singular. Direct methods to compute the derivative matrices and vectors for DAE's are needed.

In this section, we present a new method for direct numerical computation of arbitrary order time derivatives of the transition matrix and of the input transfer vector. It is based on circuit theory concepts. Although the algorithms are illustrated on modified nodal analysis, they are readily extensible to tableau and state-space formulations.

5.4.1 The method

Since M and P are solutions to circuit equations, it is natural to consider methods based on numerical integration of differential equations to compute their derivatives. However, physical meanings of their derivatives are not well defined. Careful examination has to be done on how to formulate the differential equations. Fortunately, LTI systems have the property that if the response to the input $x(t)$ is the output $y(t)$, then the response to $x'(t)$ is $y'(t)$ [97]. Differential equations for the time derivatives of M and P can be formulated using this property.

The MNA equations for a LLTI circuit are [55]

$$\mathbf{G}\mathbf{v}(t) + \mathbf{C}\frac{d\mathbf{v}(t)}{dt} = \mathbf{w}(t) + \mathbf{C}\mathbf{v}(0^-), \tag{5.11}$$

where $\mathbf{w}(t)$ is the input source vector, and $\mathbf{v}(0^-)$ is the initial condition. Because the superposition rule apples to linear circuits, the complete response can be obtained as a sum of the zero-state response, $\mathbf{v}_{ZS}(t)$, which is the solution of

$$\mathbf{G}\mathbf{v}(t) + \mathbf{C}\frac{d\mathbf{v}(t)}{dt} = \mathbf{w}(t), \tag{5.12}$$

and the zero-input response, $\mathbf{v}_{ZI}(t)$, which is the solution of

$$\mathbf{G}\mathbf{v}(t) + \mathbf{C}\frac{d\mathbf{v}(t)}{dt} = \mathbf{C}\mathbf{v}(0^-). \tag{5.13}$$

Methods for direct computation of $\mathbf{M}(T)$ and $\mathbf{P}(T)$ were given in [62]. The vector $\mathbf{P}(T)$ was evaluated by numerically integrating (5.12) over the time interval $[0, T]$. Based on the relationship

$$\mathbf{v}_{ZI}(t) = \mathbf{M}(t)\mathbf{v}(0^-), \tag{5.14}$$

the matrix M was constructed as

$$\mathbf{M}(t) = \mathbf{N}(t)\mathbf{C}, \tag{5.15}$$

where the intermediate matrix $\mathbf{N}(t)$ was evaluated, one column at a time, as the response to a unit impulse excitation appearing in the corresponding row of the RHS (right-hand-side) vector. For example, the first column of $\mathbf{N}(t)$ was obtained as the solution to

$$\mathbf{G}\mathbf{v}(t) + \mathbf{C}\frac{d\mathbf{v}(t)}{dt} = \begin{bmatrix} \delta(t) \\ 0 \\ \vdots \\ 0 \end{bmatrix}. \tag{5.16}$$

By using the derivative property of LTI systems, the n-th time derivative of P can be computed as the zero-state response when the excitation is the n-th derivative of the source function:

$$\mathbf{G}\mathbf{v}(t) + \mathbf{C}\frac{d\mathbf{v}(t)}{dt} = \frac{d^{(n)}\mathbf{w}(t)}{dt^n}, \tag{5.17}$$

and vector $\mathbf{P}^{(n)}(T)$ is computed by numerical integration of (5.17) over $[0, T]$.

The n-th time derivative of M is given by

$$\mathbf{M}^{(n)}(t) = \mathbf{N}^{(n)}(t)\mathbf{C} \tag{5.18}$$

where the j-th column of the intermediate matrix $\mathbf{N}^{(n)}(t)$ is obtained as the response to $\delta^{(n)}(t)$ appearing in j-th row of the RHS vector, which is the solution to

$$\mathbf{G}\mathbf{v}(t) + \mathbf{C}\frac{d\mathbf{v}(t)}{dt} = \begin{bmatrix} 0 \\ \vdots \\ 0 \\ \delta^{(n)}(t) \\ 0 \\ \vdots \\ 0 \end{bmatrix} \leftarrow j. \tag{5.19}$$

Computation of the derivatives of M and P requires numerical integration of the differential equations (5.17) and (5.19). Because the Dirac impulse and its derivatives are involved, we select the numerical Laplace inversion method [69, 70, 71], reviewed in section 2.5, for the integration. The major reasons are: (1) this method can correctly handle discontinuous functions, like the unit step, Dirac impulse, and even its derivatives; (2) It can provide accurate results.

5.4.2 Example: A RLC Circuit

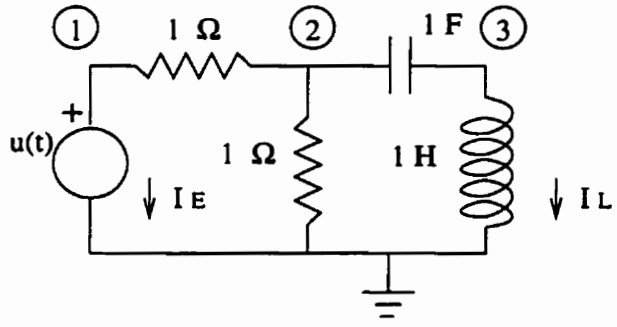


Figure 5.3: A simple RLC circuit

A computer program was written to compute the derivatives of M and P. Here the LTI circuit in Fig. 5.3 is used to illustrate the method and test the accuracy of the program. When the excitation is the unit-step function, $u(t)$, the MNA matrices are

$$\mathbf{G} = \begin{bmatrix} 1 & -1 & 0 & 1 & 0 \\ -1 & 2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \end{bmatrix}, \quad \mathbf{C} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 \end{bmatrix},$$

$$\mathbf{v}(t) = \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ I_E \\ I_L \end{bmatrix}, \quad \mathbf{w}(t) = \begin{bmatrix} 0 \\ 0 \\ 0 \\ u(t) \\ 0 \end{bmatrix}.$$

The first-order derivative of P is the solution to

$$\mathbf{G}\mathbf{v}(t) + \mathbf{C}\frac{d\mathbf{v}(t)}{dt} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ u'(t) = \delta(t) \\ 0 \end{bmatrix}. \tag{5.20}$$

It can be written analytically as

$$\mathbf{P}'(t) = \frac{e^{-t/4}}{120} \begin{bmatrix} 120\delta(t) \\ 60\delta(t) + 2\sqrt{15}\sin\theta - 30\cos\theta \\ 60\delta(t) - 14\sqrt{15}\sin\theta - 30\cos\theta \\ -60\delta(t) + 2\sqrt{15}\sin\theta - 30\cos\theta \\ -4\sqrt{15}\sin\theta + 60\cos\theta \end{bmatrix},$$

where $t \geq 0$ and $\theta = \sqrt{15}t/4$. The same expression is obtained as compared with direct differentiation of P(t), which was provided in [62].

The value of $P'(T)$ is computed by numerical Laplace inversion of

$$[\mathbf{G} + s\mathbf{C}]\mathbf{V}(s) = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \\ 0 \end{bmatrix}, \tag{5.21}$$

which is the Laplace domain representation of (5.20). When $T = 0.35$ second,

$$\mathbf{P}'(0.35) = \begin{bmatrix} 0 \\ -0.1963664988743 \\ -0.3536534006128 \\ -0.1963664988743 \\ 0.3927329977486 \end{bmatrix}.$$

This result was computed by the program, and accuracy of 12 decimal digits is achieved.

The second column [1] of $\mathbf{N}'(t)$ is the solution of

$$\mathbf{G}\mathbf{v}(t) + \mathbf{C}\frac{d\mathbf{v}(t)}{dt} = \begin{bmatrix} 0 \\ \delta'(t) \\ 0 \\ 0 \\ 0 \end{bmatrix}. \tag{5.22}$$

[1] Since the first and fourth rows of the matrix C are zero-vectors, computation of the first and fourth columns of $\mathbf{N}'(t)$ is not necessary, as they will not contribute to $\mathbf{M}'(t)$. This is similar to what was described in [62].

Its value is obtained by numerical Laplace inversion of the system of equations

$$[\mathbf{G} + s\mathbf{C}]\mathbf{V}(s) = \begin{bmatrix} 0 \\ s \\ 0 \\ 0 \\ 0 \end{bmatrix}. \tag{5.23}$$

When $t = 0.35$ second, it equals

$$\begin{bmatrix} 0 \\ 0.1768267003064 \\ -0.2159062974422 \\ 0.1768267003064 \\ -0.3536534006128 \end{bmatrix}. \tag{5.24}$$

Other columns of $\mathbf{N}'(0.35)$ can be computed in a similar way, and the matrix $M'(t)$ is obtained as

$$\begin{aligned} \mathbf{M}'(0.35) &= \mathbf{N}'(0.35)\mathbf{C} \\ &= \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0.3927329977486 & -0.3927329977486 & 0 & 0.3536534006128 \\ 0 & 0.7073068012253 & -0.7073068012253 & 0 & -0.4318125948844 \\ 0 & 0.3927329977486 & -0.3927329977486 & 0 & 0.3536534006128 \\ 0 & -0.7854659954973 & 0.7854659954973 & 0 & -0.7073068012256 \end{bmatrix}, \end{aligned}$$

where accuracy of 12 decimal digits is obtained as compared with analytical results.

5.4.3 Comments

In this section, systems of linear differential equations are formulated for direct computation of the time derivatives of M and P. The derivative matrices and vectors are ob-

tained by numerical integration of differential equations. The numerical Laplace inversion method was chosen as the integration method, because it can provide very accurate results and can correctly handle Dirac impulses and their derivatives. Although the inversion requires network solution at multiple complex frequencies for each integration time step [19], the high computational cost can be tolerated, because the derivative matrices and vectors are evaluated only *once* in a pre-processing step before the simulation starts. The computational cost is in exchange for the computation accuracy, which is important for the application of clock jitter analysis of high resolution circuits.

A formula was given to compute derivatives of the time response $v(t)$ to a s-domain function $V(s)$ with the numerical Laplace inversion method [69, 70, 71]. Only a few steps are necessary in addition to the computation of $v(t)$. This formula is based on the properties of the Laplace transform, and is done in complex arithmetic. Along with the computation of M and P, it can be used to evaluate their time derivatives. This approach is different from the method provided in this section, which directly gives the time domain formulation of the derivative matrices and vectors. Nevertheless, they provide the same results.

5.5 Numerical Examples

The theories have been implemented in a computer program, SIMjitter. It can be used to analyze the effects of arbitrary waveform clock jitter on PSL networks and SDMs. Here we give simulation results of a few circuits to show the usefulness of the method.

Because of clock jitter, there is uncertainty in the clock period. The time instants when the switching is taking place are not regularly spaced, but the Fast Fourier Transform is based on equally spaced data. In order to fulfill the conditions for power spectrum estimation by the FFT, additional circuit outputs on equally spaced grids are computed

by SIMjitter. In this thesis, all the PSD plots for the clock jitter analysis examples were obtained by FFT on equally spaced data from SIMjitter.

5.5.1 Simulation Accuracy: A Bandpass Filter

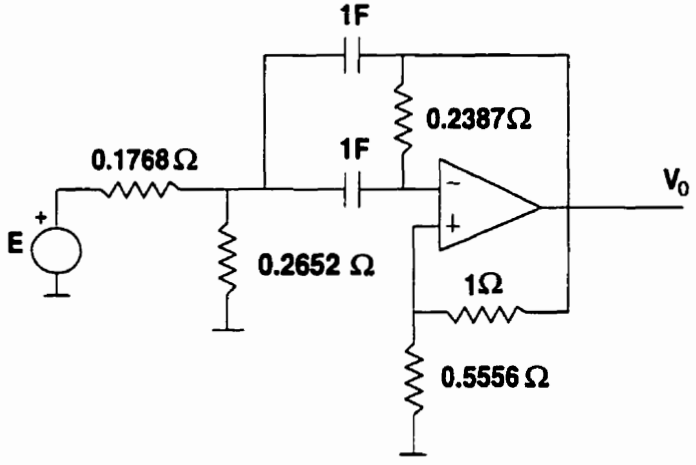


Figure 5.4: A bandpass filter

Accuracy of the clock jitter analysis was tested on a LTI circuit – the bandpass filter shown in Fig. 5.4. The circuit response at unequally spaced data points was computed by the varying-step sampled-data algorithm implemented in SIMjitter, and the results were compared with exact analysis.

When the input $e(t) = \sin(2\pi t)$ V, the output can be written analytically:

$$v(t) = A_1 e^{-\alpha t} \cos(\omega_1 t + \theta_1) + A_2 \cos(\omega_2 t + \theta_2), \tag{5.25}$$

where the constants are

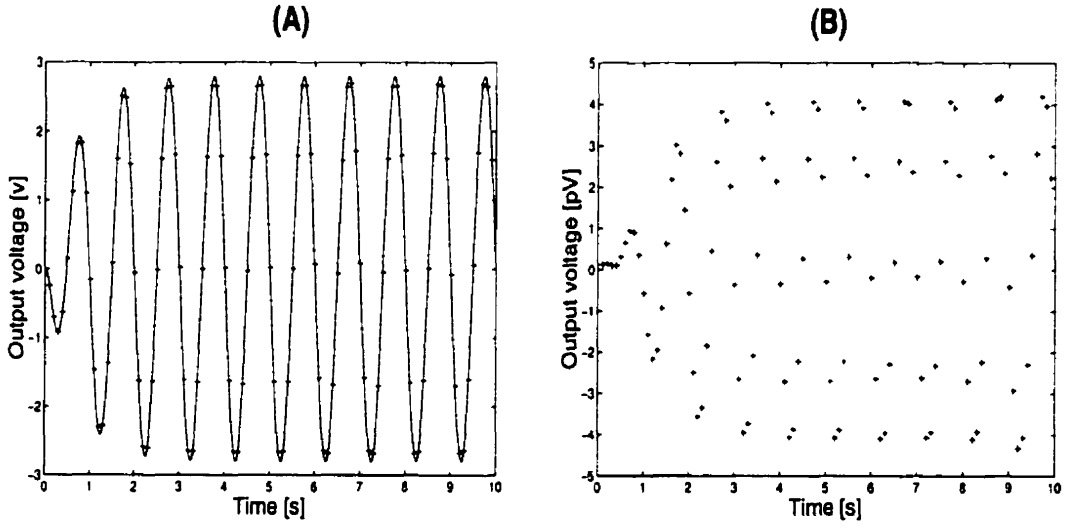


Figure 5.5: Bandpass filter (A) simulation results match exact analysis (B) difference in the order of pV

$$A_1 = 2.89288084256738$$
$$A_2 = 2.80107862143781$$
$$\alpha = 1.57058074752572$$
$$\omega_1 = 6.08487678389001$$
$$\omega_2 = 6.28318530717959$$
$$\theta_1 = -1.57010793363597$$
$$\theta_2 = 1.57150728127396.$$

The analytical result of $v(t)$ is plotted in Fig. 5.5(A) as the continuous curve, and the data points, marked by small "crosses", were obtained by SIMjitter simulation when 1 ms rms Normally distributed random fluctuation existed in the nominal simulation step of 0.1 second. This is equivalent to 1% jitter. The SIMjitter simulation results were based on 4-term Taylor series approximation of $\mathbf{M}(T + \Delta t)$ and $\mathbf{P}(T + \Delta t)$. The difference between SIMjitter simulation and exact analysis is displayed in Fig. 5.5(B), where simulation accuracy in the order of 10^{-12} was obtained. This example shows that SIMjitter can provide accurate results.

5.5.2 A Switched-Capacitor Filter

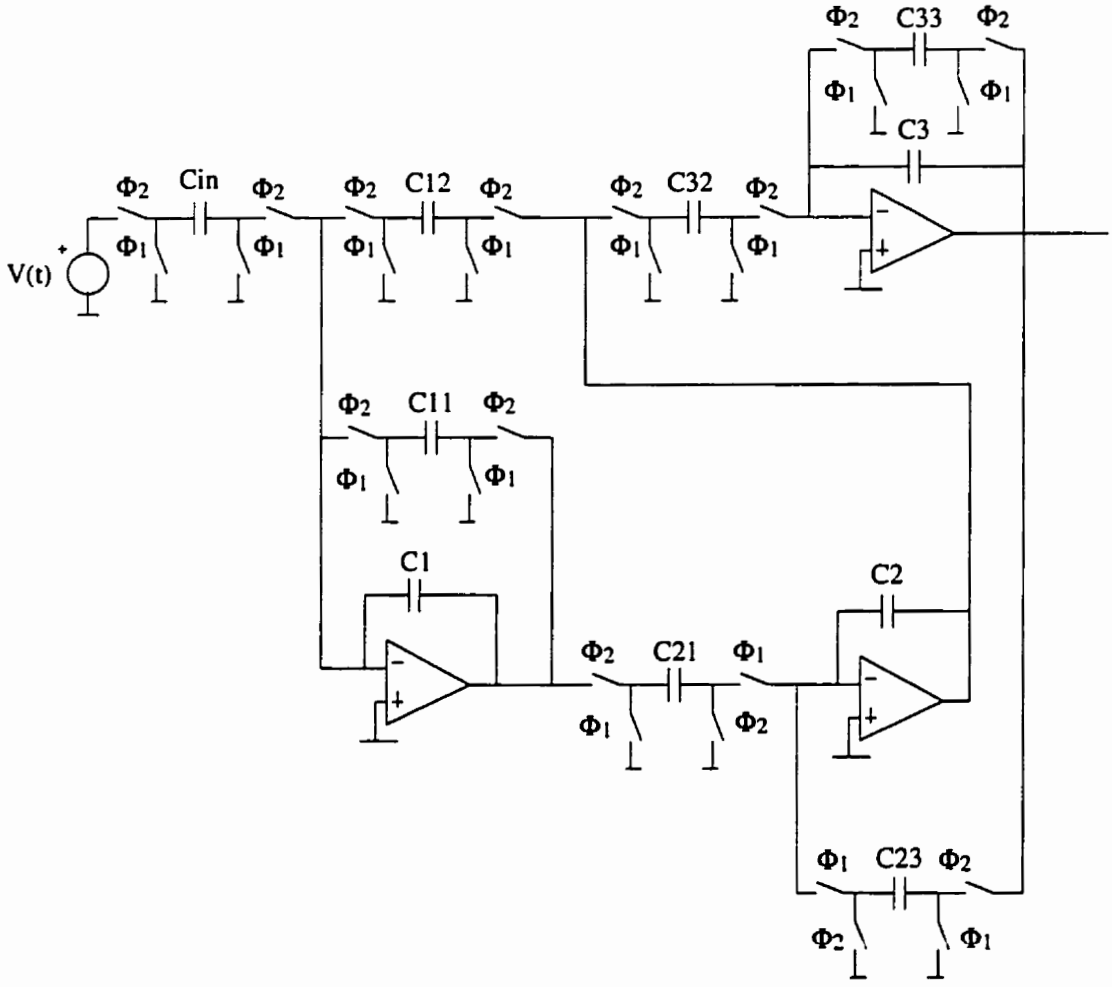


Figure 5.6: Third-order Chebyshev switched-capacitor filter

The circuit shown in Fig. 5.6 is a third-order Chebyshev SC filter, one of the design examples presented in [98]. It was clocked at 100 kHz, and the capacitor ratios are listed in Table 5.1. The switch ON-resistances are 500 Ω, and opamps have unity-gain bandwidth of 700 kHz.

The input to the circuit is a 1 V peak-to-peak sinusoid of 0.5 kHz. When the clock-

ing happens at precisely desired time instants, a 'clean' sinusoid can be observed from the simulation results shown in Fig. 5.7. Once the clock is fluctuating, the circuit performance deteriorates drastically. As shown in Fig. 5.8(A), when 5 ns-rms sinusoidal jitter of 100 Hz is present in the clocking, large sideband frequency components appear equally spaced on both sides of the input component, at distances equal to the multiples of the jitter frequency. When 5 ns-rms uniformly distributed jitter is present in the clocking, the overall noise floor was heightened, as shown in Fig. 5.8(B). These phenomena agree with what was observed experimentally [57, 94].

$C_{in} = 1.5609$	$C_{11} = 1.0000$	$C_{12} = 1.6252$	$C_1 = 31.7120$
	$C_{21} = 1.2813$	$C_{23} = 1.0000$	$C_2 = 32.9520$
	$C_{32} = 2.0824$	$C_{33} = 1.0000$	$C_3 = 31.7120$

Table 5.1: SC Filter: Capacitor Ratios

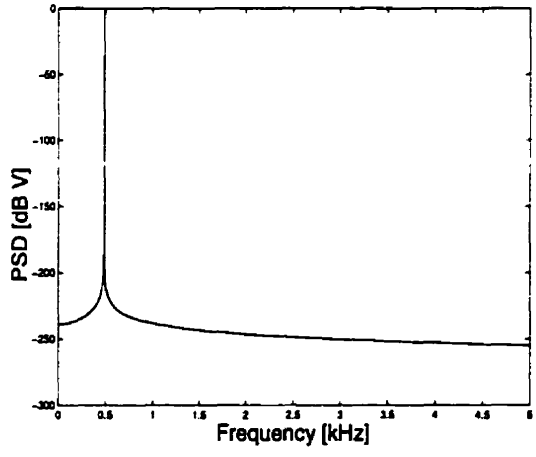


Figure 5.7: SC filter output spectrum: no jitter

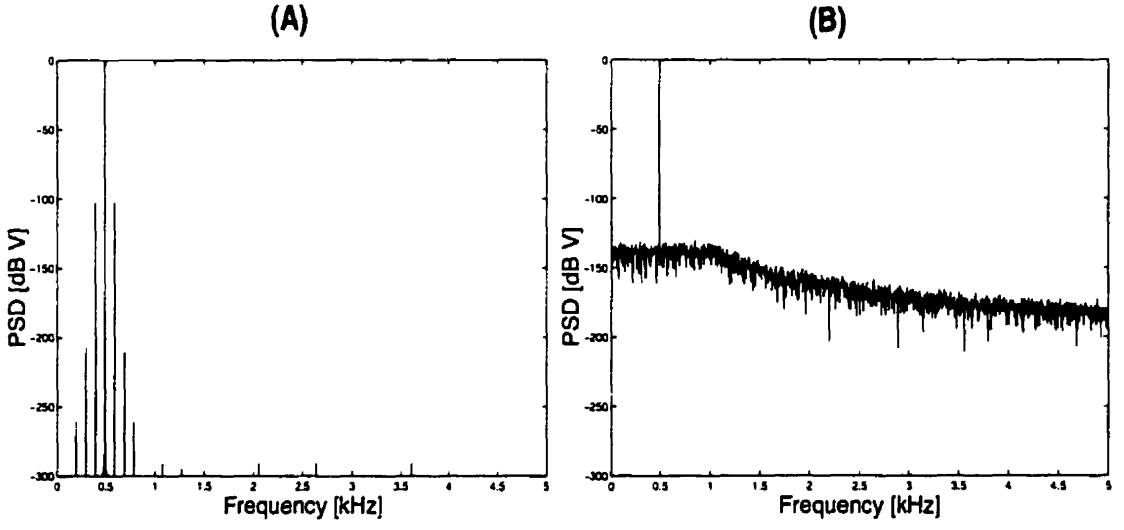


Figure 5.8: SC filter: with 0.1% (A) sinusoidal jitter (B) random jitter

5.5.3 A Switched-Current Filter

The switched-current filter [98] shown in Fig. 5.9 was studied with small signal models replacing the transistors and biasing current sources. A first-order small signal model was used for the transistors, and open-circuit was used for the biasing current sources. The clock was at 100 kHz, and the input was a 0.1μA sinusoid of 0.5 kHz.

Multiple simulations under the same condition as the SC filter were performed. When there is no jitter, and there is 0.1% sinusoidal jitter in the clocking, the simulation results are similar to the results of the SC filter, as plotted in Fig. 5.10 and Fig. 5.11(A). When there is 0.1% random jitter in the clocking, a whitened noise floor is shown, but with slightly different shape as compared with the SC filter in the same operating condition. This is shown in Fig 5.11(B).

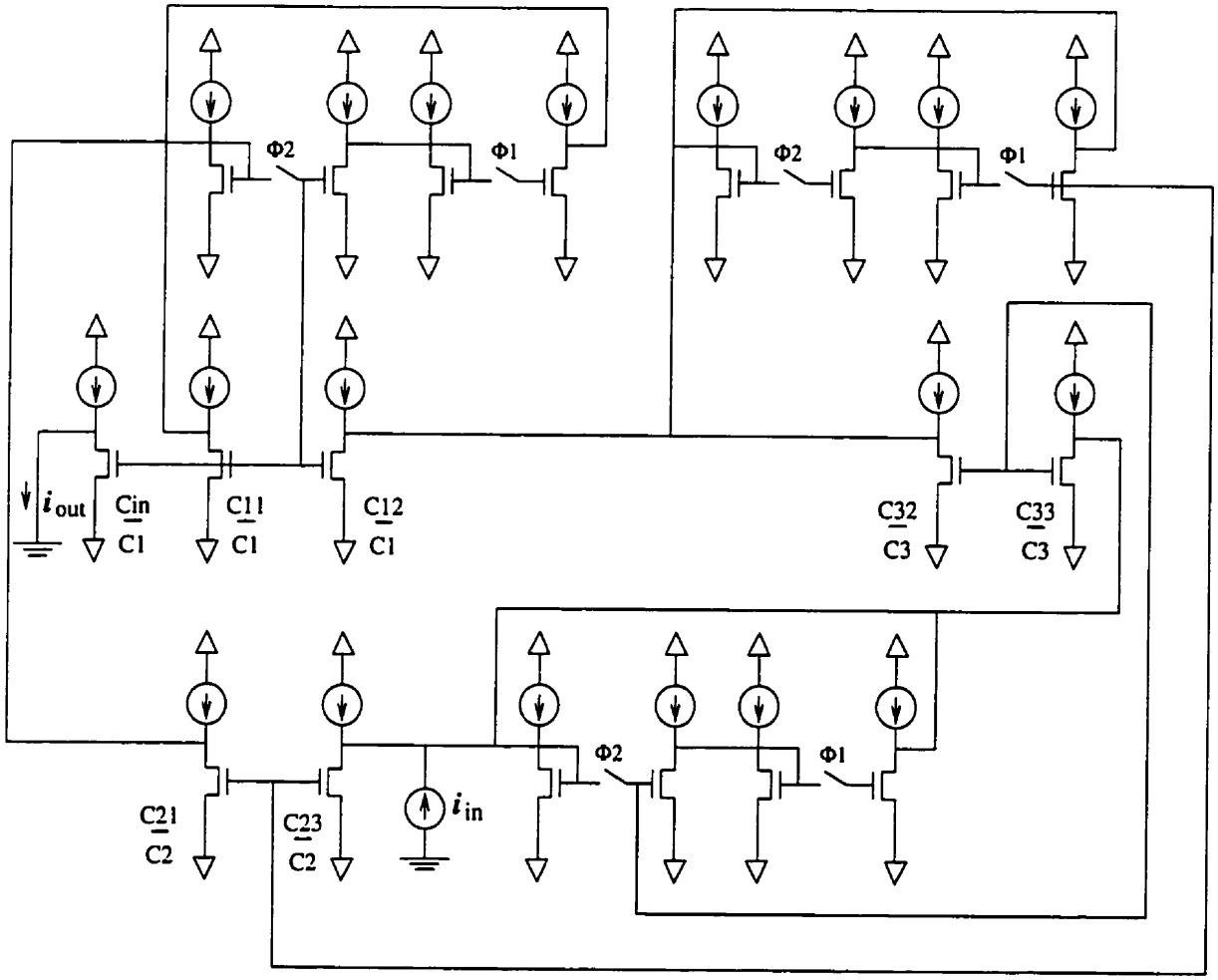


Figure 5.9: Third-order Chebyshev switched-current filter

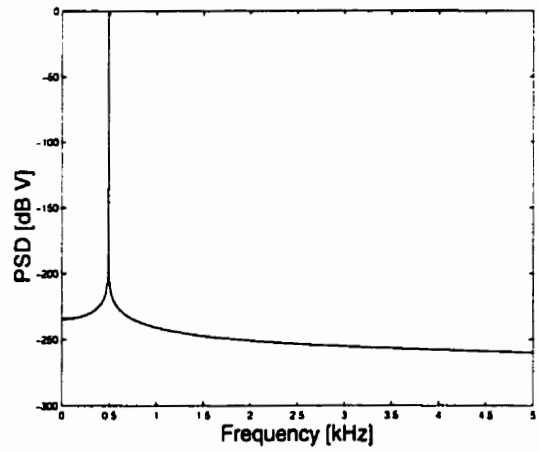


Figure 5.10: SI filter output spectrum: no jitter

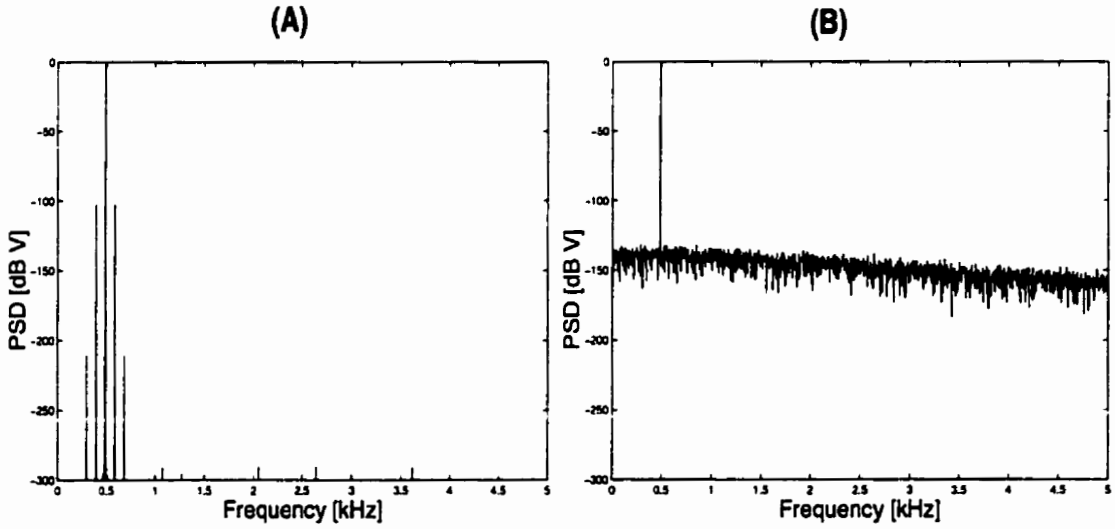


Figure 5.11: SI filter: with 0.1% (A) sinusoidal jitter (B) random jitter

5.6 Chapter Summary

This chapter presented a special sampled data analysis method for LTI circuits. The method differs fundamentally from classical sampled data analysis in that small variations in the spacing between the discrete data points is allowed. It can be applied to the clock jitter analysis of PSL networks and SDMs.

The major advantages of clock jitter analysis by this method are: (1) No restriction is imposed on the jitter waveform; (2) It is a general method and suitable for computer application; (3) It is at electrical circuit level, and applicable to a wide variety of circuits.

We introduced a new method for numerical computation of arbitrary-order time derivatives of the transition matrix M and of the input transfer vector P. A set of differential-algebraic equations (DAEs) was formulated, and the time derivatives of M and P were computed by direct numerical integration of the DAEs. The method is based on circuit theory concepts. Although it was illustrated on modified nodal analysis, this approach can be readily extended to the state-space formulation or tableau method.

A state-of-the-art review of clock jitter analysis of PSL networks was given. Numerical examples for clock jitter analysis of a SC and a SI filter were presented. The simulation results confirmed the theoretical predictions and experimental observations in [57, 94, 99]: (1) Sinusoidal clock jitter introduces sideband tones equally spaced on both sides of the input component, at a distance equal to multiples of the jitter frequency; (2) Random clock jitter leads to overall elevation of the noise floor.

Chapter 6

Clock Jitter Analysis

This chapter deals with clock jitter analysis of sigma-delta modulators at electrical circuit level. It is an application of the special sampled data analysis method presented in chapter 5.

Numerical examples are given for a switched-capacitor and a continuous-time sigma-delta modulator. The influence of clock jitter on the performance degradation of SDMs involved in direct RF/IF conversion is studied, and simulation results are compared with experimental observations. Primitive results of this chapter were presented in [73].

6.1 Introduction

Clock jitter is one of the major causes of performance degradation of SDMs, especially in high frequency applications [100, 7, 9]. Sigma-delta data converters are traditionally designed to convert low-frequency, "baseband", signals with high resolution. In baseband designs, the output error resulting from clock jitter is most likely masked by the electrical noise floor. In high-frequency designs, however, the effect of clock jitter becomes

significant.

Recently, because of the increasing interest in compact and low power transceivers for wireless communication systems, various RF (radio-frequency) front-end conversion architectures are being proposed as alternatives to the conventional super-heterodyne schemes, which require significant numbers of discrete components [101]. One of the architectures is a direct conversion which mixes the RF signal down to the baseband directly by setting the sampling frequency equal to the incoming RF carrier frequency. Another more promising approach is the sub-sampling technique [102] which down-converts the RF signal by setting the sampling frequency as a sub-multiple of the RF carrier frequency. These schemes are presently under active research. Some recent works [100, 103, 104, 84] have used the sub-sampling technique in sigma-delta data converters to down-convert IF (intermediate frequency) signals.

RF front-end designs are much more sensitive to clock jitter than baseband applications. In SDMs used for direct RF/IF conversion, output error resulting from clock jitter could surpass thermal noise and become the dominant factor limiting conversion accuracy.[1] Because of clock jitter effects, a bandpass modulator [7] achieved only 25 dB SNR over a 2 MHz signal-band centered at a 25 MHz carrier frequency. This was much lower than the 56 dB performance obtained from transistor level full circuit simulation.

Although clock jitter analysis methods are needed in the design of SDMs, they are not available at electrical circuit level. Block level clock jitter analysis can be found in the literature [57, 58], but its usefulness is limited due to the following drawbacks:

1. The model is highly abstract and mathematical, without details of electrical realization. This level of analysis is useful only in the conceptual design phase.

2. Thermal noise is one of the major factors that limit the resolution of a SDM. Clock

[1]This will be shown in the following simulation examples.

jitter effects become concern only after they surpass the thermal noise floor. However, thermal noise information is not available in the block level simulation.

3. Continuous-time SDMs are very sensitive to clock jitter [105, 7, 8], but block level simulation of this type of modulator is difficult [8].

In summary, methods for clock jitter analysis at electrical circuit level, and applicable to CT SDMs, are needed. Furthermore, it would be desirable to include the thermal noise information. A method that possesses all of the above attributes is presented in section 6.2, and its usefulness is demonstrated on simulation examples in section 6.3.

6.2 Clock Jitter Analysis Method

A SDM can be partitioned into a nonlinear block (the quantizer), which changes its characteristics at external clock edges only, and a linear block (the rest of the circuit). The output to the linear block can be computed with feedback from the latched quantizer treated as a step input [19]. The linear block could be a LTI circuit for a CT SDM, or a PSL network for a SC or a SI SDM.

The varying-step sampled data analysis method for LTI circuits is given in (5.4) and (5.5). Its application to clock jitter analysis of PSL networks is given in (5.8).

Additional procedures are needed for the simulation of SDMs: because of clock jitter, in general, the clock edges are not regularly spaced. At a clock edge, the output to the linear block is computed by (5.4) and (5.5), or by (5.8), depending on whether it is a continuous or a discrete-time SDM. The state of the quantizer is updated according to the output of the linear block, and this process is repeated for the following clock cycles.

6.3 Numerical Examples

In this section, a few examples are given to show the usefulness of the method.

6.3.1 A Switched-Capacitor Sigma-Delta Modulator

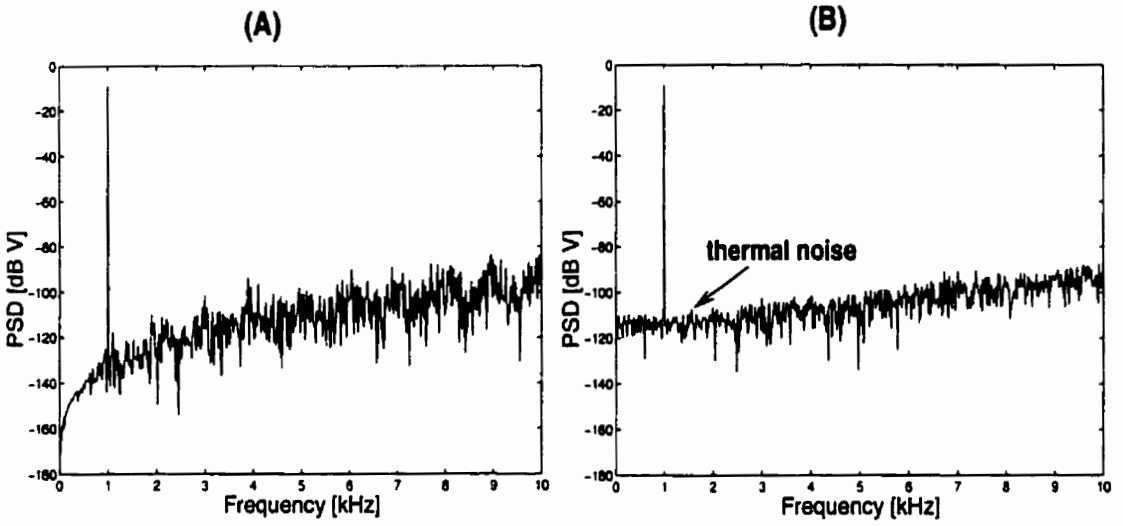


Figure 6.1: SC SDM: (A) ideal elements (B) with thermal noise

We have mentioned in the introduction that the output error due to clock jitter is relatively small in baseband applications. It is most likely masked by the electrical noise floor. In RF/IF front-end designs, the effect of clock jitter becomes important, and can become a dominant factor limiting the resolution. The following experiments are used to illustrate these points.

As an example, we study the SC SDM shown in Fig. 3.15. Its ideal operation and its thermal noise performance were presented in section 3.5.4. They are plotted again in Fig. 6.1 for reference.

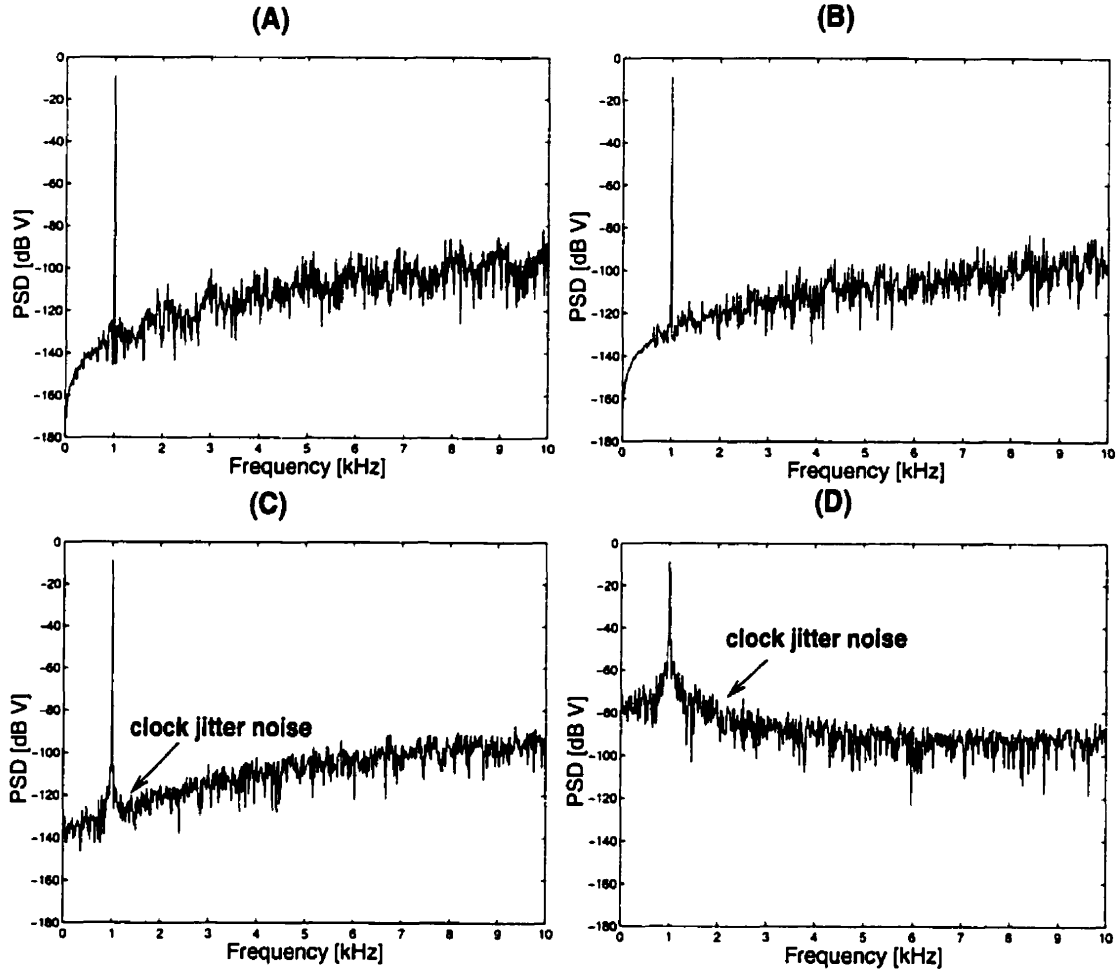


Figure 6.2: SC SDM: (A) 1 kHz input: no jitter (B) 1025 kHz input: no jitter (C) 1 kHz input: 0.01% jitter (D) 1025 kHz input: 0.01% jitter

In order to check only the clock jitter effects, thermal noise is not taken into account in the following examples. First, we considered a baseband signal with 1 kHz frequency and 0.75 V amplitude. Then, an IF sinusoid of 1.025 MHz frequency and the same amplitude was used. With the circuit clocked at 1.024 MHz, the IF signal is expected to be down-converted to 1 kHz in the baseband according to the sub-sampling theory.

Without clock jitter, the IF signal was down-converted to 1 kHz correctly, as shown in Fig. 6.2(B). A smoother noise spectrum is also observed compared with Fig. 6.2(A). A possible reason is that the high-frequency IF signal keeps the quantizer busy and breaks the limit cycles.

When clock jitter is present, the noise spectrum is different. The circuit was simulated again with 0.01% random jitter in the clocking, or equivalently, a small random fluctuation of 48.8 ps rms in the phase duration. The simulation results for the baseband version is shown in Fig. 6.2(C). The error resulting from clock jitter appears in the noise spectrum from 0 to 1 kHz, and exhibits a noise "skirt" around the signal component. It is, however, much lower than the thermal noise floor around -120 dB, shown in Fig. 6.1(B), and will be covered by the thermal noise floor. In strong contra-distinction, the in-band noise power increases dramatically for the IF version. The noise "skirt" stays at -80 dB in the signal-band, which is 40 dB above the thermal noise floor. It will dominate the total in-band noise power and determine the performance measures for the modulator.

The effect of periodic clock jitter was also studied. The circuit was simulated with 48.8 ps rms sinusoidal jitter of 500 Hz in the phase duration of the clocking. As shown in Fig. 6.3(B), large tones appeared on both sides of the signal component. The distance between them is 500 Hz, which happens to be the jitter frequency. These tones are very large, and are much higher than the noise skirt resulting from random clock jitter with the same rms value, as shown in Fig. 6.3(A).

In summary, a noise "skirt" around the signal component was observed when random jitter appeared in the clocking. When sinusoidal clock jitter was present, large sideband tones appeared on both sides of the signal component at the distance of the jitter frequency. Information on thermal noise performance is important for SDMs intended for baseband applications, and information on the error due to clock jitter is important for SDMs intended for RF/IF applications. Our method can simulate both noise effects sep-

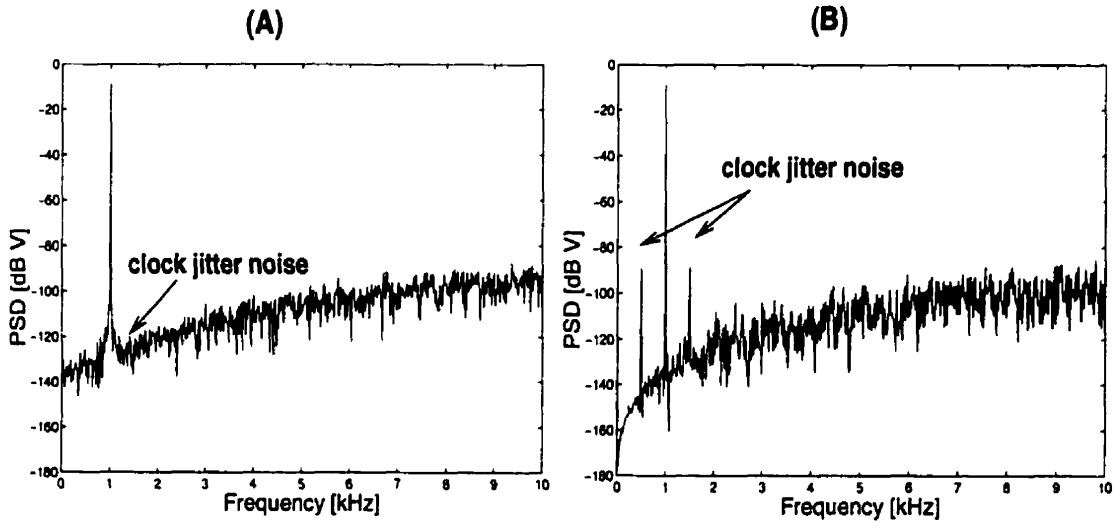


Figure 6.3: SC SDM, 1 kHz input: 0.01% (A) Normally distributed (B) 500 Hz sinusoidal clock jitter

arately or simultaneously.

6.3.2 A Continuous-Time Sigma-Delta Modulator

As a second example, we consider the CT SDM shown in Fig. 3.18. Its ideal operation and its thermal noise performance were studied in section 3.5.4. The simulation results are plotted again in Fig. 6.4.

The input to the modulator was a sinusoid of 2 kHz. The circuit was simulated first with Normally distributed random jitter, and then with sinusoidal jitter of 500 Hz in the clocking. The jitter power was 48.8 ps rms for both cases.

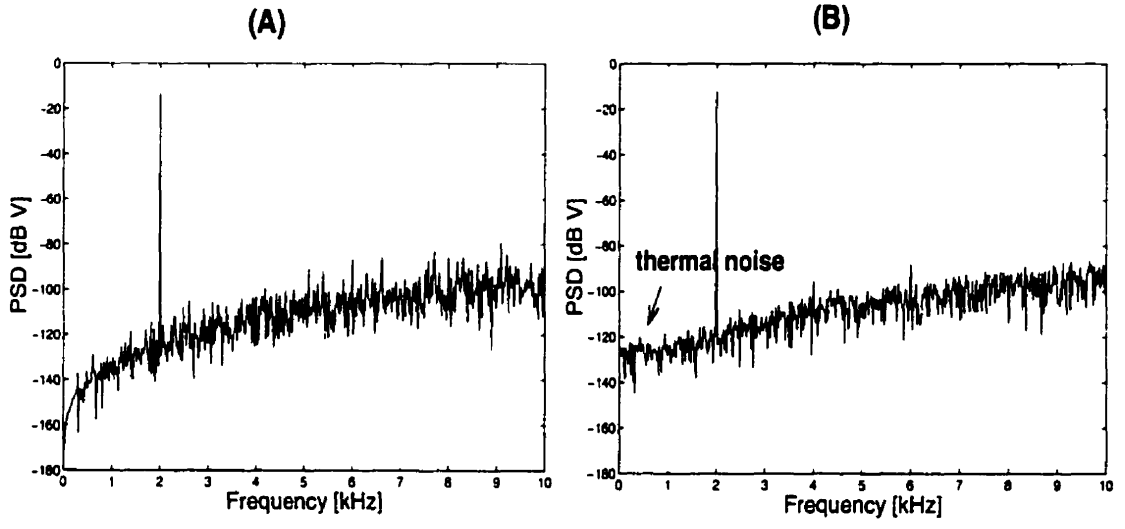


Figure 6.4: CT SDM: (A) ideal elements (B) with thermal noise

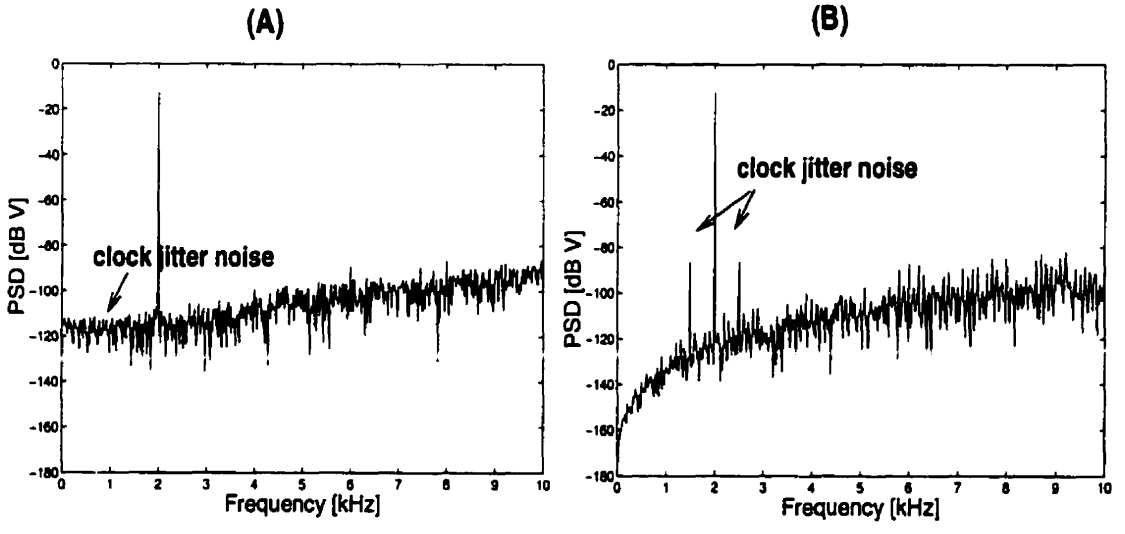


Figure 6.5: CT SDM: with 0.01% (A) Normally (B) 500 Hz sinusoidal clock jitter

As shown in Fig. 6.5, random clock jitter leads to an overall elevation of the noise floor, and no obvious noise "skirt" can be observed. Sinusoidal jitter introduces large sideband tones on both sides of the signal component, at the distance of the jitter fre-

quency. In this continuous-time modulator, the effect of clock jitter is much more severe than in the switched-capacitor modulator. Clocked at the same rate, and with the same amount of jitter, the elevated noise floor shown in Fig. 6.5(A) is much higher than that in Fig. 6.3(A). It surpasses the thermal noise floor shown in Fig. 6.4(B), and dominates the in-band noise power.

The simulation times by the SDNoise program were collected in Table 6.1. They are based on the time needed for transient analysis over 74k clock cycles of the CT and the SC SDM, and are classified in three categories, namely, ideal analysis, thermal noise analysis, and clock jitter analysis. Simulation time in the order of minutes is shown.

	ideal elements	thermal noise	clock jitter
CT SDM	8.83 seconds	1.73 minutes	1.70 minutes
SC SDM	18.64 seconds	12.30 minutes	3.82 minutes

Table 6.1: Simulation Time for 74k Clock Cycles

6.3.3 Comparison with Measurements

This research provides the first-ever method available at the electrical circuit level for clock jitter analysis of SDMs. Its validity can be tested by comparing the simulation results with measurements. In the following, two comparisons are made.

First, we compare the measurements in [103] and in [84]. A second-order passive SC SDM was designed in [103] for low IF signal (10 MHz) conversion. The IF signal at 10.005 MHz was sampled by a clock at 10 MHz, and a baseband tone of 5 kHz was obtained. As shown in Fig. 6.6,[2] the noise floor was at least 80 dB down from the fundamental. It is similar to the results of a baseband version where the signal was at 5 kHz.

[2]Reprinted with permission from [103].

The measurements suggest that clock jitter had little influence in this IF application, and the noise floor of the modulator was still dominated by thermal and other noise effects.

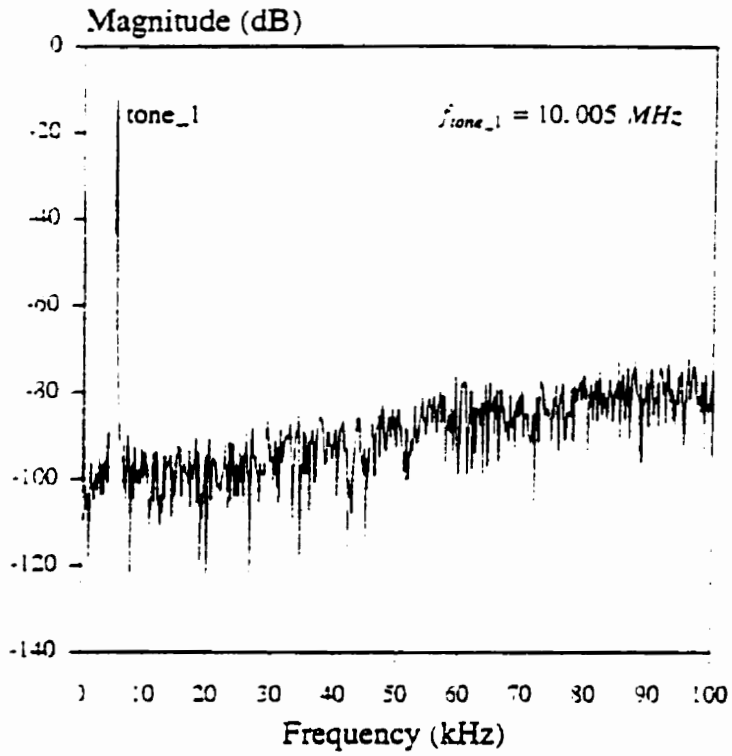


Figure 6.6: F. Chen PhD thesis: Clocked at 10 MHz, 10.005 MHz IF input

The use of SDMs in high IF (100 MHz and beyond) signal conversion was demonstrated in [84]. A second-order passive SC SDM was designed. The circuit was clocked at 10 MHz, and the signal was slightly higher than 100 MHz. As shown in Fig. 6.7,[3] the noise floor was much higher than the idle channel test shown in Fig. 3.20, and a noise "skirt" was clearly visible around the signal component. This suggests that clock jitter

[3]Reprinted with permission from [84].

had significant influence on the performance of the SDM; it surpassed thermal noise and determined the performance measures.

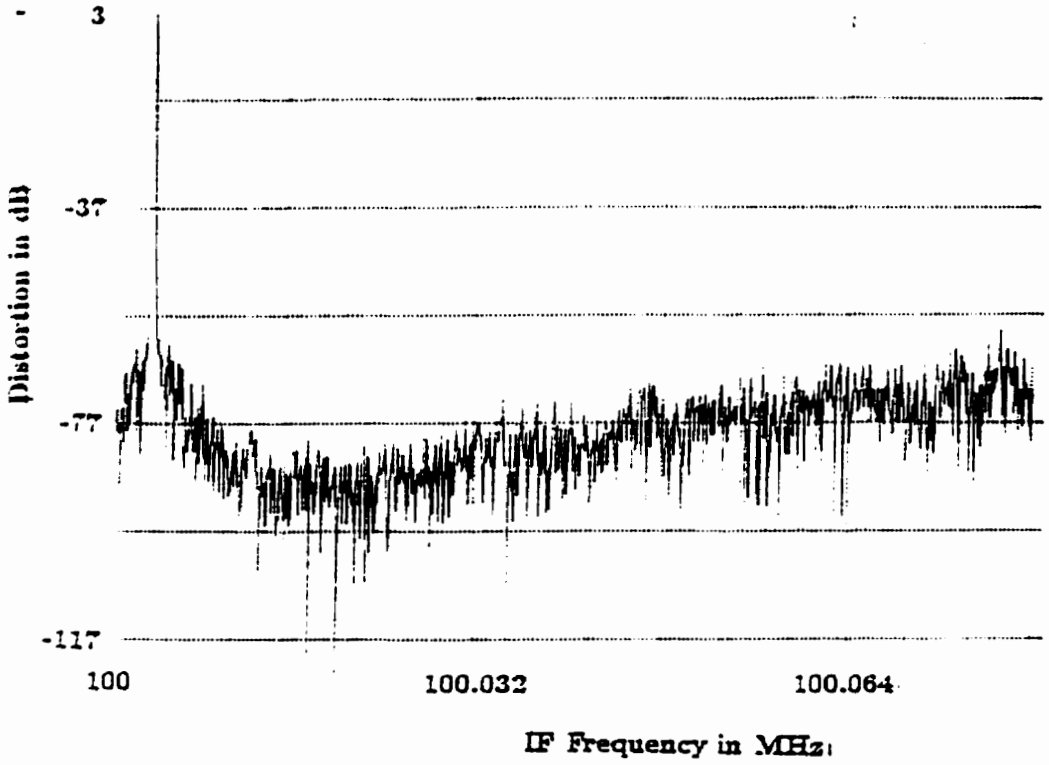


Figure 6.7: S. Sen PhD thesis: Clocked at 10 MHz, 100 MHz IF input

The circuits in [103] and [84] were similar, and the same test instruments were used. Their measurements can be compared. The phenomena shown in their measurements are in accordance with our simulation results shown in Fig. 6.1 and Fig. 6.2.

As an alternative way to validate the method, the observations summarized from our simulation results were used to diagnose what was happening in a practical circuit. In [100], a low-pass SC SDM was used to down convert an IF signal into baseband by

the sub-sampling principle. The clock frequency was 2.5 MHz, and the IF signal was 10 kHz above it. The measurements were shown in Figure 4 of [100]. Although the signal was successfully converted to baseband at 10 kHz, the effect of clock jitter is obvious: excessive amounts of noise exist, and the noise "skirt" is only 40 dB down from the signal. Large sideband tones appear on both sides of the signal component in a regular pattern. This figure suggests that clock jitter contributed significantly to the performance deterioration of the modulator, and there were both random and periodic contents in the jitter. The measurements show agreement with the trend observed from our simulation results in Fig. 6.2(D) and Fig. 6.3(B).

6.4 Chapter Summary

This chapter extended the varying-step sampled data analysis method proposed in chapter 5 to clock jitter analysis of SDMs. It is the first-ever method available at the electrical circuit level for SDMs, and is applicable to modulators with either SC, SI, or CT loop-filters.

Numerical examples of clock jitter analysis were given for a SC SDM when it was used to convert baseband signals, and when it was used as an IF front-end to convert IF signals by the sub-sampling technique. The effect of random and sinusoidal clock jitter was studied on the SC SDM and a CT SDM. Random clock jitter was shown to lead to an overall elevation of the noise floor, and sinusoidal clock jitter to introduce large side-band tones on both sides of the signal component, at the distance of jitter frequency. The CT SDM was observed to be more sensitive to clock jitter than the SC SDM.

The simulation results were compared with measurements, and good agreement was obtained. Simulation time in the order of minutes was shown for analysis of a typical SDM over 74k clock cycles when thermal noise and clock jitter were present.

Chapter 7

Conclusion

7.1 Summary and Discussion

This thesis developed computer-aided methods for analysis of sigma-delta modulators when there are noise sources in the circuit or jitter in the clocking. The algorithms are also applicable to periodically switched linear networks.

Thermal noise is an important source limiting the resolution, but traditional frequency domain noise analysis is not applicable to SDMs. On the other hand, performance estimation of SDMs requires extremely long and accurate transient simulation, resulting in difficult time domain noise analysis. In this thesis, we presented a new time domain method. The noise sources are modeled as random amplitude pulse waveforms, and a sampled data method is used to compute the transient response when the signal and noise sources exist in the circuit simultaneously. The method was applied to thermal noise and dithering analysis of SDMs. It can also be applied to PSL networks, for which frequency-domain noise analysis is not straightforward.

Clock jitter is another major source that results in performance degradation of SDMs.

Despite the fact that clock jitter is usually random, previous methods were restricted to periodic jitter analysis. They are based on classical SC methods that analyze the circuit by exploiting its periodic switching nature. The introduction of random clock jitter destroys the periodic switching pattern, and classical SC methods are not applicable. In this thesis, we gave a new sampled-data method for LTI circuits. It differs fundamentally from traditional sampled-data analysis in that it is a *varying-step* method. Small fluctuations in the spacing between the discrete data points are allowed. It was applied to clock jitter analysis of PSL networks and SDMs. *No* restrictions on the jitter waveform were imposed. It can handle either periodic or random clock jitter analysis.

The transition matrix and input-transfer vector play important roles in circuit theory. They are related to the zero-input and zero-state circuit responses. Evaluations of their time derivatives are needed for the special sampled-data method. This thesis presented methods for direct computation of the derivative matrices and vectors. They are based on circuit theory concepts and aimed at numerical computation. Sets of differential equations are formulated, and the derivative matrices and vectors are computed by numerical integration of the equations.

The methods for noise, clock jitter, and dithering analysis are the *first-ever* available for SDMs at electrical circuit level. Modulators with either switched-capacitor, switched-current, or continuous-time loop-filters can be analyzed. The methods are general, systematic, and suitable for computer application. No restrictions are imposed on circuit topologies.

The theories we developed were implemented in a computer program, which can perform thermal noise, dithering, and clock jitter analysis of SDMs. Simulation examples were given, and comparisons were made with exact analysis, physical measurements, or experimental observations. The program is fast and analysis of a typical SDM over several hundred thousand clock cycles is completed in the order of minutes.

7.2 Future Work

The work can be extended in many areas. One possibility is to consider distortion analysis of SDMs. Distortion generates undesirable tones in the passband spectrum, and limits the resolution of the converter. It is caused by nonlinearities in the feedback loop, such as opamp gain nonlinearity, capacitor voltage dependence, and quantizer nonlinearity [106].

This thesis and previous investigations [19, 61] allow some linear imperfections, like the switch ON-resistances and finite gain-bandwidth product of opamps, and a harsh nonlinearity, the quantizer, in the formulation, but mild nonlinearities cannot be included. It was pointed out that the first opamp and capacitor nonlinearities are significant sources of distortion [3, 107]. As a future research direction, the possibility of allowing mild nonlinearities, like nonlinear capacitors, could be explored. Once this feature is obtained, both harmonic and intermodulation distortion could be studied in a general and systematic way at the electrical circuit level.

Appendix A

SDNoise Simulator

A simulator, SDNoise (Sigma-Delta Noise analysis program), was developed using the theories and algorithms presented in this thesis. It is interactive and written in Fortran. Its structure is shown in Fig. A.1. SDNoise accepts as input a netlist of any network made up of externally controlled switches (ideal or nonideal switch with finite ON-resistances), passive linear elements R, L, C, independent current and voltage sources, linear dependent sources VVT, VCT, CCT, CVT, ideal or finite gain opamps, nonideal opamps modeled with a finite gain-bandwidth product, MOS transistors working in small signal condition, and single or multi-bit quantizers. All numerical examples presented in this thesis were obtained from SDNoise simulation.

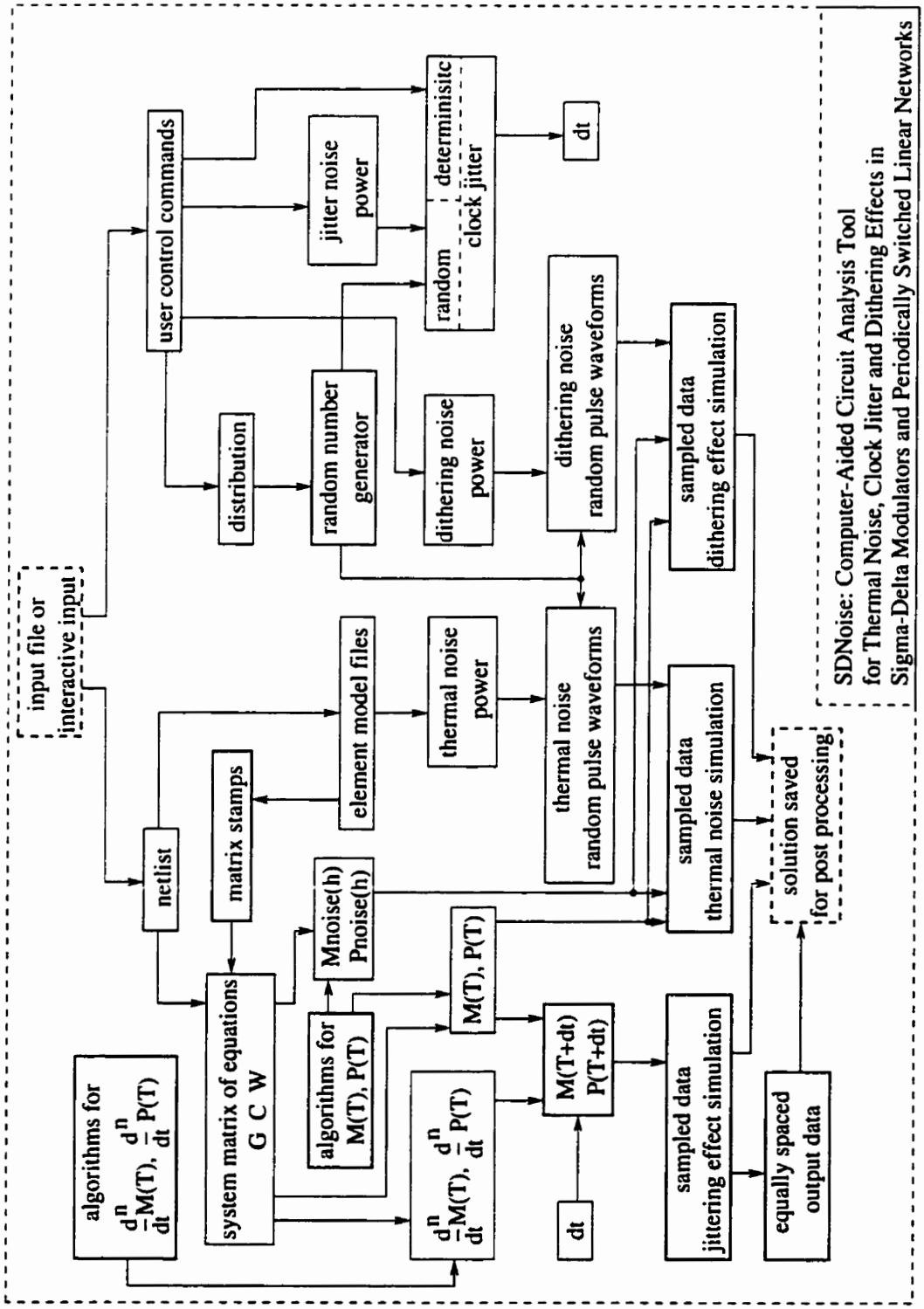


Figure A.1: Block Diagram of SDNoise

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